Product Specification

(Preliminary)

Part Name: Monochrome LCD Display Module

Part No.: BGG24064-02 SERIES

Doc No.: SAS1-1710-A

Customer:
Approved by:

From: Blaze Display Technology Co., Ltd.
Approved by:

Blaze Display Technology Co., Ltd.

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Notes:

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2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Blaze Display Technology Co., Ltd. for any intellectual property claims or other problems that may result application based on the module described herein.

Revised History

Part Number	Revision	Revision Content	Revised on
BGG24064-02-LY-SPTWD-1.0	1.0	New	Feb 06th, 2017

CONFIDENTIAL

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Contents

1. Basic Specifications

1.1 Display Specifications

1) Display Type:	STN(YELLOW-GREEB) / Positive
2) Display Format:	240×64 Dots
3) Character Color (ON):	BLUE
4) Background Color (ON):	YELLOW-GREEN
Background Color (OFF):	YELLOW-GREEN
5) Drive Method:	1/65 Duty; 1/9Bias
6) Viewing Direction:	6:00
7) Polarizer Type:	Transflective

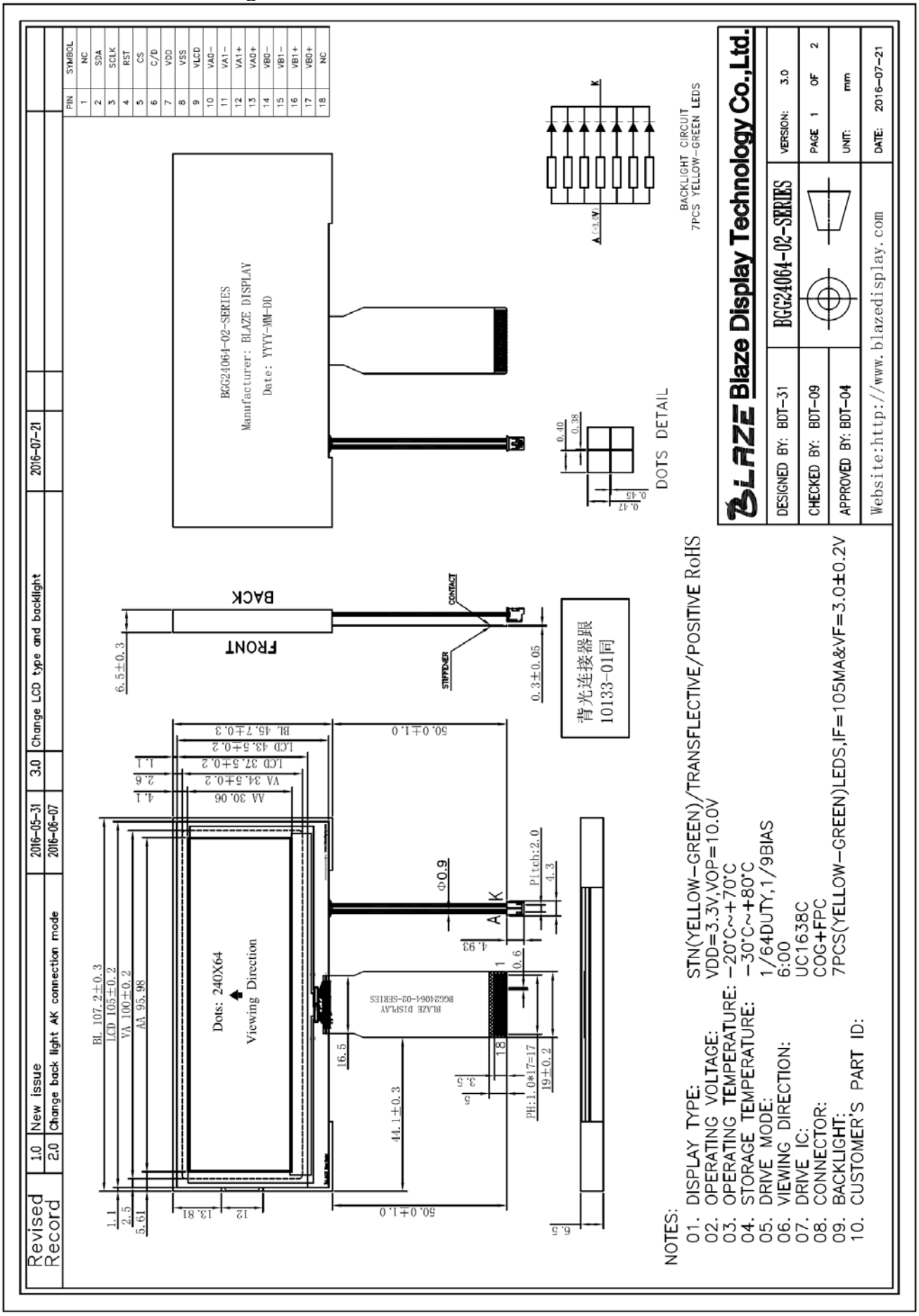
1.2 Mechanical Specifications

1) Outline Dimensions:	According to the annexed outline drawing on the next page
2) Viewing Area:	100.00 W × 34.50 H (mm)
3) Active Area:	95.98 W × 30.06 H (mm)
4) Dot Pitch:	0.40 W × 0.47 H (mm)
5) Dot Size:	0.38 W × 0.45 H (mm)
6) Weight:	TBD

1.3 Others

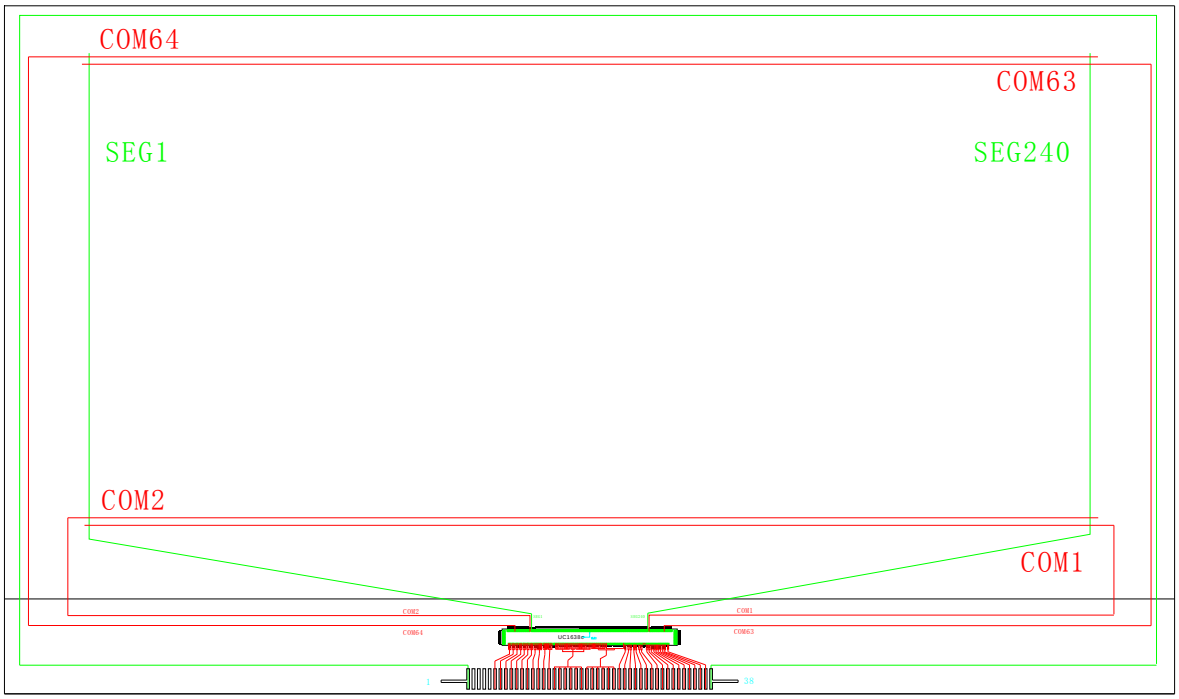
1) Driver IC:	UC1638C
2) Backlight:	LED, YELLOW-GREEN, If = 105mA, Vf = 3.0±0.2V
3) Operating Temperature:	-20°C－+70°C
4) Storage Temperature:	-30°C－+80°C
5) RoHS Compliant:	Yes

1.4 Mechanical Drawing

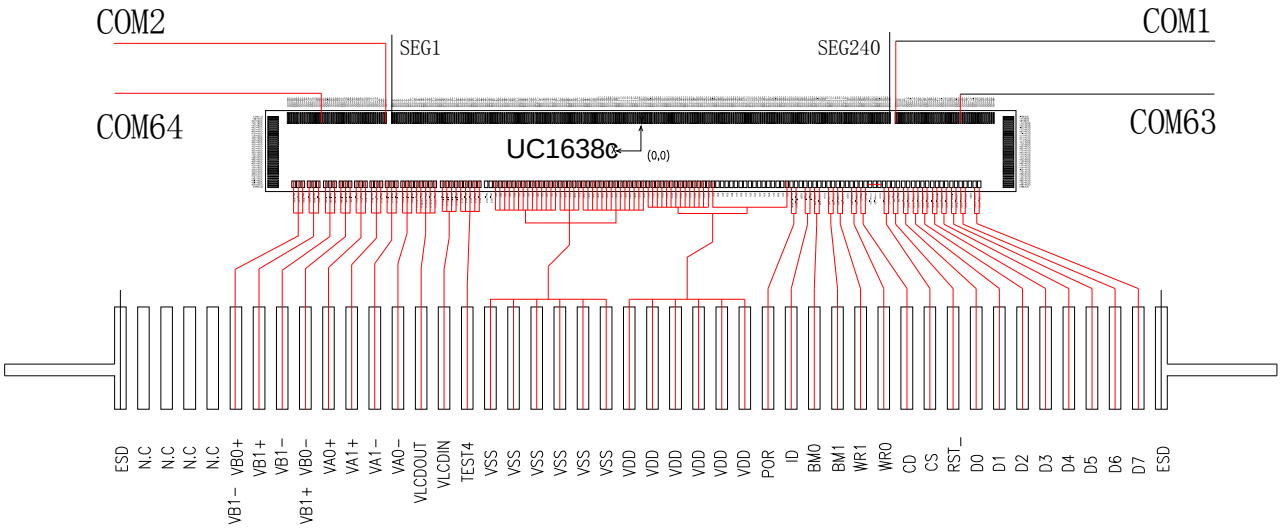


2. Electrical Specification

2.1 Block Diagram



2.2 IC LAYOUT



2.3 Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Power Supply for Logic	Vdd	−0.3	+4.0	V
Power supply for LCD Drive	Vlcd	9.7	10.3	V
Input Voltage	Vin	−0.3	Vdd + 0.3	V
Operating Temperature	Topr	−20	+70	°C
Storage Temperature	Tstg	−30	+80	°C

2.4 Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.7	1.8~3.3	3.6	V
$V_{DD2/3}$	Supply for bias & pump		2.7	2.8~3.3	3.6	V
V_{LCD}	Charge pump output	$V_{DD2/3}$ ≥ 2.7V, 25°C		14.5	17.49	V
V_D	LCD data voltage	$V_{DD2/3}$ ≥ 2.7V, 25°C	0.99		1.59	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current	V_{IN} = V_{DD} or Vss			1.5	µA
I_{SB}	Standby current	V_{DD} = $V_{DD2/3}$ = 3.3V, Temp = 85 °C			50	µA
C_{IN}	Input capacitance			5	10	pF
C_{OUT}	Output capacitance			5	10	pF
$R_{ON(SEG)}$	SEG output impedance	V_{LCD} = 17.49V		1.20	1.70	kΩ
$R_{ON(COM)}$	Upward COM output impedance	V_{LCD} = 17.49V		1.20	1.70	kΩ
f_{LINE}	Average Line rate	LC[4:3] = 10b	-10%	26.0	+10%	klps

POWER CONSUMPTION

V_{DD} = 2.7 V, Bias Ratio = 11b , PM = 84,
V_{LCD} = 14.51 V, Line Rate = 26 Klps, Mux Rate = 160
Bus mode = 6800, C_L =330 nF, C_B = 2.2 µF,
Temperature = 25°C, All HV outputs are open circuit.

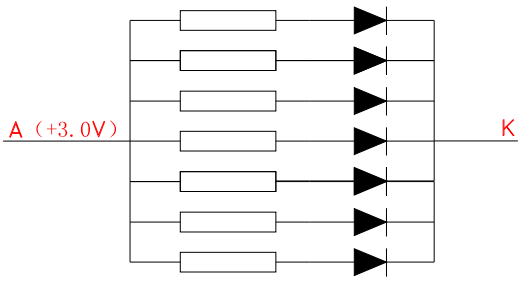
Display Pattern	Conditions	Typical	Maximum	Unit
All-OFF	Bus = idle	1173	1467	µA
All-ON	Bus = idle	1205	1507	µA
2-pixel checker	Bus = idle	1445	1807	µA
-	Reset (standby current)	< 3	5	µA

2.5 Pin Definition

PIN NO.	FUNCTION DESCRIPTIONS	SYMBOL
1	**NC**	NC
2	**Serial data input**	SDA
3	**Serial clock input**	SCLK
4	**Reset input pin. Active "L"**	RST
5	**Chip Select input pin. Active "L"**	CS
6	**Data or Command select. DATA is "H" , COMMAND is "L"**	C/D
7	**POWER**	VDD
8	**GROUND**	VSS
9	**High voltage LCD Power Supply**	VLCD
10	**LCD Bias Voltages**	VA0-
11	**LCD Bias Voltages**	VA1-
12	**LCD Bias Voltages**	VA1+
13	**LCD Bias Voltages**	VA0+
14	**LCD Bias Voltages**	VB0-
15	**LCD Bias Voltages**	VB1-
16	**LCD Bias Voltages**	VB1+
17	**LCD Bias Voltages**	VB0+
18	**NC**	NC

3. LED Backlight

3.1 Power Supply for LED Backlight



BACKLIGHT CIRCUIT
7PCS YELLOW-GREEN LEDS

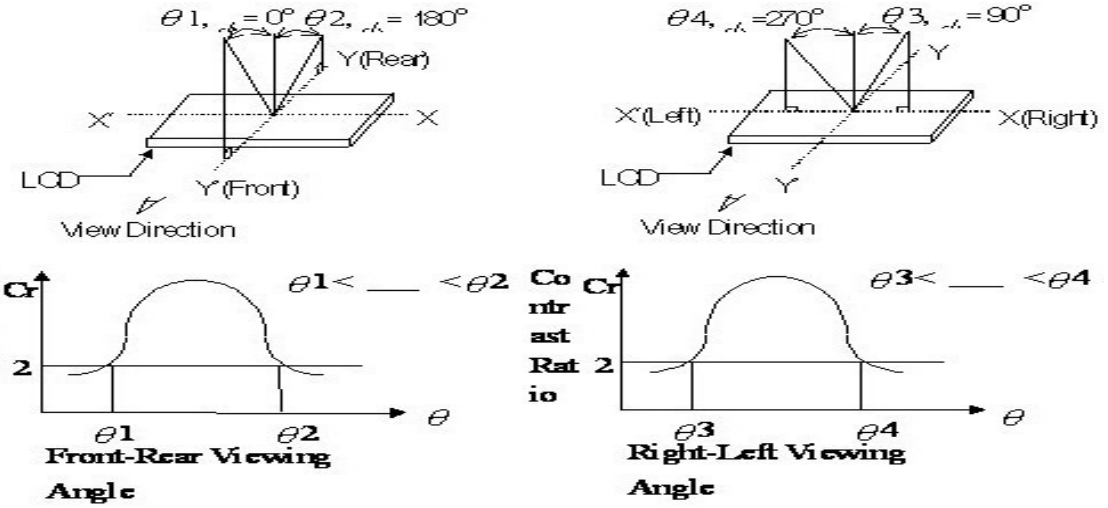
3.2 Electrical Optical Characteristics

(Ta=25℃.Unless specified,The Ambient temperature Ta=25℃)

Item	Symbol	CONDITIONS	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Forward Voltage	Vf	If=105mA	2.9	3.0	3.1	V
Reverse Current	Ir	Vr=5.0V	-	-	100	uA
Spectral Line Half width	△λ	IF=105mA T=25℃	-	-	-	nm
Peak wave length	λp		567	-	572	nm
Chromaticity Coordinates	X		-	-	-	
	Y		-	-	-	
Luminance	Lv	IF=105mA	50	--	-	Cd/m²
Uniformity	△	MIN/MAX=100%	80	-		%

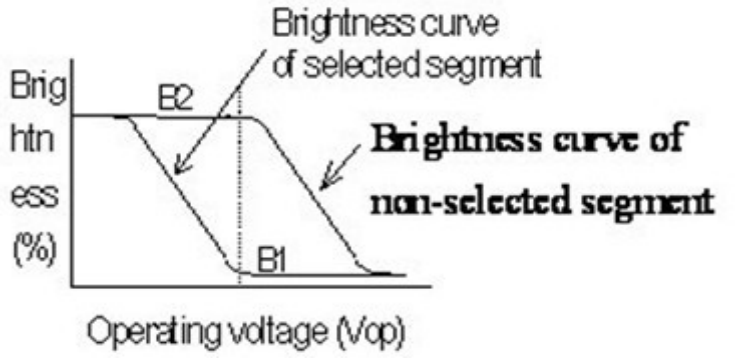
4. Optical Characteristics

4.1 Definition of Viewing Angle

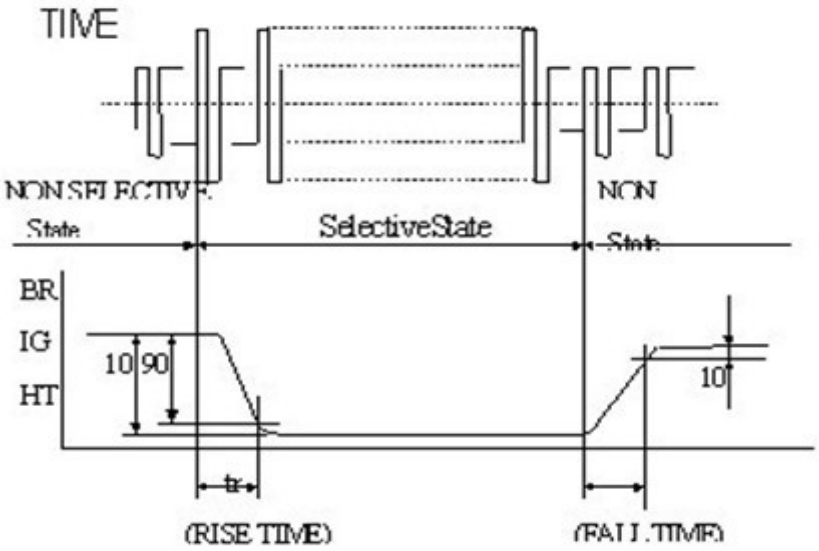


4.2 Definition of Contrast

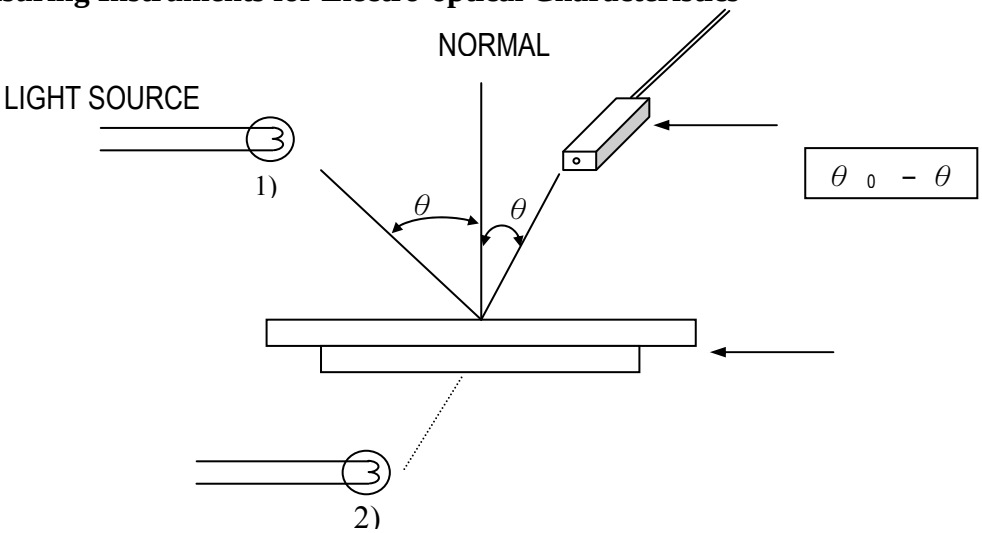
$$C.R = \frac{\text{Brightness of nonselected segment (B2)}}{\text{Brightness of selected segment}} \quad \text{RATIO}$$



4.3 Definition of Response



4.4 Measuring Instruments for Electro-optical Characteristics



*** Note:**

1) Light source position for measuring the reflective type of LCD panel;
2) Light source position for measuring the transflective / transmissive types of LCD panel.

5. AC Characteristics and Input Timing Characteristics

5.1 Serial Mode

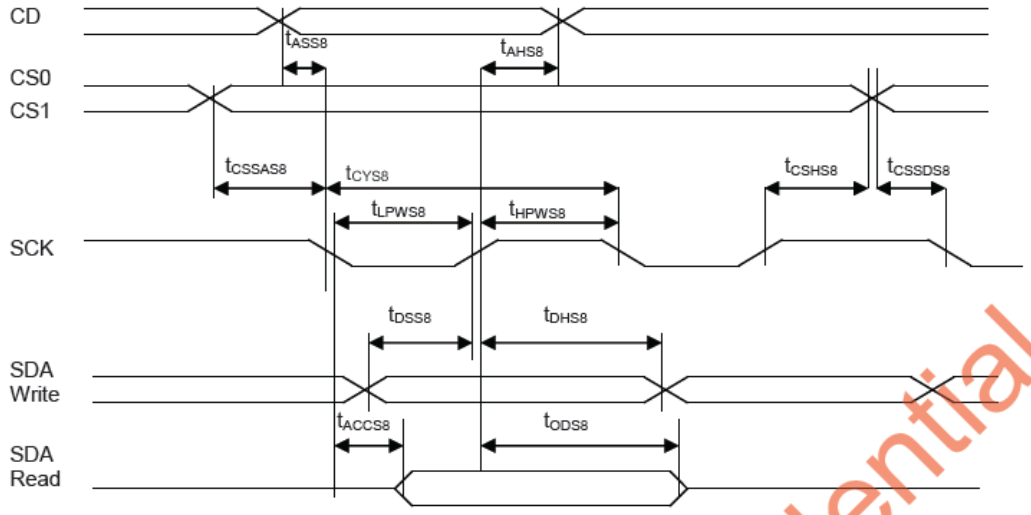


FIGURE 18: Serial Bus Timing Characteristics (for S8)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ≤ V_{DD} ≤ 3.6V, Ta= –30 to +85°C)				(read / write)		
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		15		
t_{CSSAS8}	CS1/CS0	Chip select setup time		5	–	nS
t_{CSHS8}		Chip select hold time		15		
t_{CYS8}	SCK	System cycle time		430 / 220	–	nS
t_{LPWS8}		Low pulse width		200 / 95		
t_{HPWS8}		High pulse width		200 / 95		
t_{DSS8}	SDA (Write)	Data setup time		-- / 25	–	nS
t_{DHS8}		Data hold time		-- / 15		
t_{ACCS8}	SDA (Read)	Read access time	C_L = 100pF	– / --	200	nS
t_{ODS8}		Output disable time		30 / --	–	

Note: tr (rising time), tf (falling time) : ≤ 15nS

5.2 6800 Series Mode

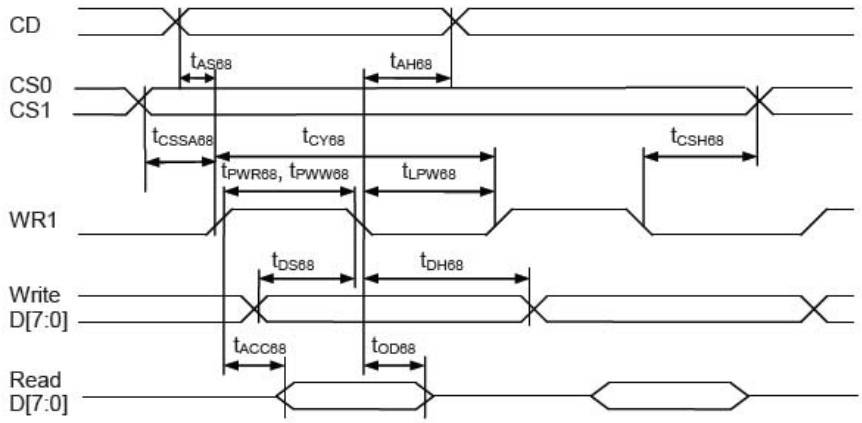


FIGURE 17: Parallel Bus Timing Characteristics (for 6800 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ≤ V_{DD} ≤ 3.6V, Ta= –30 to +85°C)				(read / write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		15 20	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CY68}	WR0, WR1	System cycle time		430 / 280	–	nS
t_{PWR68}		Pulse width		200 / —		
t_{PWW68}		Pulse width		— / 125		
t_{LPW68}		High pulse width		200 / 125		
t_{DS68} t_{DH68}	Write D7~D0	Data setup time Data hold time		– / 45 – / 10	–	nS
t_{ACC68} t_{OD68}	Read D7~D0	Read access time Output disable time	C_L = 100pF	– / – 100 / –	200 –	nS

Note: tr (rising time), tf (falling time) : ≤ 15nS

5.3 8080 Series Mode

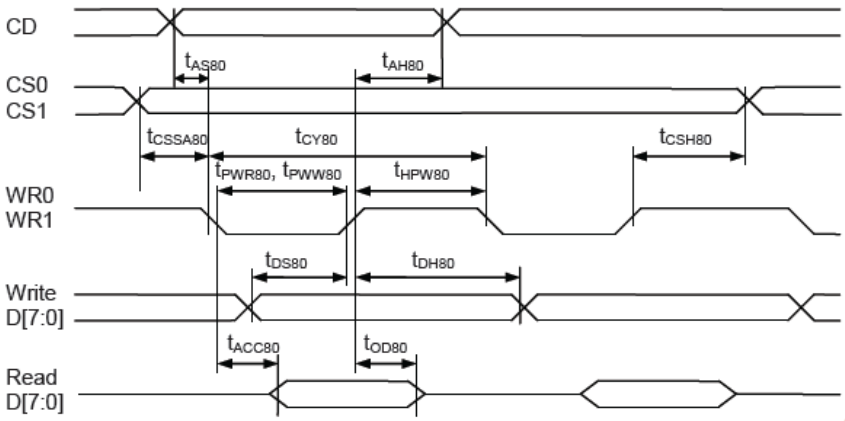


FIGURE 16: Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ≤ V_{DD} ≤ 3.6V, Ta= –30 to +85°C)				(read / write)		
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		15 20	–	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CY80}	WR0, WR1	System cycle time		430 / 280	–	nS
t_{PWR80}		Pulse width		200 / --		
t_{PWW80}		Pulse width		-- / 125		
t_{HPW80}		High pulse width		200 / 125		
t_{DS80} t_{DH80}	Write D7~D0	Data setup time Data hold time		-- / 45 -- / 10	–	nS
t_{ACC80} t_{OD80}	Read D7~D0	Read access time Output disable time	C_L = 100pF	– / -- 100 / --	200 –	nS

Note: tr (rising time), tf (falling time) ≤ 15nS

5.4 Hardware Reset Timing

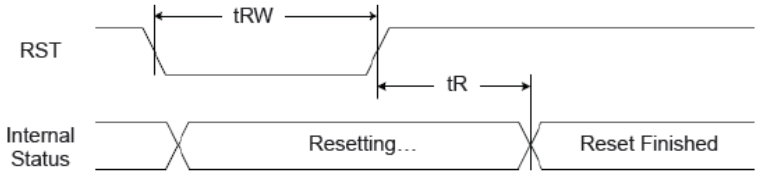


FIGURE 21: Reset Characteristics

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ≤ V_{DD} ≤ 3.6V, Ta= –30 to +85°C)						
t_{RW}	RST	Reset low pulse width		5	–	mS
t_R	RST, Internal Status	Reset to Internal Status pulse delay		10	–	uS
		Wait before Power Down		1	–	mS

6. INSTRUCTION TABLE

The following is a list of host commands supported by UC1638c:

C/D: 0: Control, 1: Data W/R: 0: Write Cycle, 1: Read Cycle D7-D0: # : Useful Data bits –: Don't Care

No	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte (multiple-byte command)	0	0	0	0	0	0	0	0	0	1	Write byte by byte	N/A
		1	0	#	#	#	#	#	#	#	#		
		:	:	:	:	:	:	:	:	:	:		
2.	Read Data Byte (multiple-byte command)	0	0	0	0	0	0	0	0	1	0	Read byte by byte	N/A
		1	1	#	#	#	#	#	#	#	#		
		:	:	:	:	:	:	:	:	:	:		
3.	Get Status (triple-byte command)	0	0	0	0	0	0	0	0	1	1	Get Status	N/A
		1	1	POR	MX	MY	PID	DE	WS	MD	MS		
		1	1	Ver[1:0]		PMO[5:0]							
4.	Set Column Address (double-byte command)	0	0	0	0	0	0	0	1	0	0	Set CA[7:0]	00H
		1	0	#	#	#	#	#	#	#	#		
5.	Set Temp. Compensation	0	0	0	0	1	0	0	#	#	#	Set TC[2:0]	100b
6.	Set Pump Control	0	0	0	0	1	0	1	1	0	#	Set PC	1b
7.	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	R	R	R	R = 0~5, Set APC[R][7:0]	N/A
		1	0	#	#	#	#	#	#	#	#		
8.	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0H
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0H
9.	Set Page Address LSB	0	0	0	1	1	0	#	#	#	#	Set PA[3:0]	0H
	Set Page Address MSB	0	0	0	1	1	1	0	0	#	#	Set PA[5:4]	0H
10.	Set V_{BIAS} Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	54H
		1	0	#	#	#	#	#	#	#	#		
11.	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[8]	0: Disable
12.	Set COM Scan Function	0	0	1	0	0	0	0	1	1	#	Set CSF	0b
13.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14.	Set Display mode	0	0	1	0	0	1	0	1	#	#	Set DC[5:4]	00b
15.	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[3:2]	10b
16.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
17.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
18.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	0	Set LC[1:0]	00b
19.	Set N-Line Inversion (double-byte command)	0	0	1	1	0	0	1	0	0	0	Set NIV[6:0]	00H
		1	0	0	#	#	#	#	#	#	#		
20.	Set Display Enable (double-byte command)	0	0	1	1	0	0	1	0	0	1	Set DC[3:2]	10b
		1	0	1	0	1	0	1	1	#	#		
21.	Set LCD Gray Shade 1	0	0	1	1	0	1	0	0	#	#	Set LC[5:4]	01b
22.	Set LCD Gray Shade 2	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
23.	System Reset (double-byte command)	0	0	1	1	1	0	0	0	0	1	System Reset	N/A
		1	0	1	1	1	0	0	0	1	0		
24.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25.	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		1	0	#	#	#	#	#	#	#	#		
26.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 12
27.	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[4]=0, CA=CR	N/A
28.	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[4]=1, CR=CA	N/A
29.	Set COM End (double-byte command)	0	0	1	1	1	1	0	0	0	1	Set CEN[7:0]	159
		1	0	#	#	#	#	#	#	#	#		
30.	Set Partial Display Start (double-byte command)	0	0	1	1	1	1	0	0	1	0	Set DST[7:0]	0
		1	0	#	#	#	#	#	#	#	#		
31.	Set Partial Display End (double-byte command)	0	0	1	1	1	1	0	0	1	1	Set DEN[7:0]	159
		1	0	#	#	#	#	#	#	#	#		

No	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
32.	Set Window Programming Starting Column Address	0	0	1	1	1	1	0	1	0	0	Set WPC0[7:0]	0
		1	0	#	#	#	#	#	#	#	#		
33.	Set Window Programming Starting Page Address	0	0	1	1	1	1	0	1	0	1	Set WPP0[5:0]	0
		1	0	0	0	#	#	#	#	#	#		
34.	Set Window Programming Ending Column Address	0	0	1	1	1	1	0	1	1	0	Set WPC1[7:0]	239
		1	0	#	#	#	#	#	#	#	#		
35.	Set Window Programming Ending Page Address	0	0	1	1	1	1	0	1	1	1	Set WPP1[5:0]	39
		1	0	0	0	#	#	#	#	#	#		
36.	Enable Window Program	0	0	1	1	1	1	1	0	0	#	Set AC[3]	0: Disable
37.	Set MTP Operation control (double-byte command)	0	0	1	0	1	1	1	0	0	0	Set MTPC[4:0]	10H
		1	0	0	0	0	#	#	#	#	#		
38.	Set MTP Write Mask (double-byte command)	0	0	1	0	1	1	1	0	0	1	Set MTPM[5:0]	00H
		1	0	0	0	#	#	#	#	#	#		
39.	Set MTP Read Potentiometer	0	0	1	1	1	1	1	0	1	0	Set RV[7:0] (BR=00b)	00H
		1	0	#	#	#	#	#	#	#	#		
40.	Set MTP Program/Erase Potentiometer	0	0	1	1	1	1	1	0	1	1	Set WV[7:0] (BR=10b)	46H
		1	0	#	#	#	#	#	#	#	#		
41.	Set MTP Write Timer (double-byte command)	0	0	1	1	1	1	1	1	0	0	Set WT[7:0]	40H
		1	0	#	#	#	#	#	#	#	#		
42.	Set MTP Read Timer (double-byte command)	0	0	1	1	1	1	1	1	0	1	Set RT[7:0]	03H
		1	0	#	#	#	#	#	#	#	#		

Warning: Any bit patterns other than the commands listed above may result in undefined behavior.

Notes:

(1) Any bit patterns other than the commands listed above may result in undefined behavior.

(2) The interpretation of commands (37)~(42) depends on register MTPC[3].

(3) After MTP-ERASE or MTP-PROGRAM operation, before resuming normal operation, please always
a) Remove TST4 power source,
b) Do a full VDD ON-OFF-ON cycle.

7. Reliability Specification

7.1 Contents of Reliability Tests

No.	Test Item	Content of Test	Test Condition
1	High Temperature Storage	Endurance test applying the high storage temperature for a long time	+80°C 96H
2	Low Temperature Storage	Endurance test applying the low storage temperature for a long time	−30°C 96H
3	High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the thermal stress to the element for a long time	+70°C 96H
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time	−20°C 96H
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and humidity storage for a long time	40°C 90%RH 96H
6	Temperature Cycle	Endurance test applying the low and high temperature cycle −20°C ⟷ 25°C ⟷ 70°C ⟷ 25°C 30min 5min 30min 5min ⟷ 1 cycle	−20°C/70°C 10 cycles
7	Vibration Test (Package State)	Endurance test applying the vibration during transportation	10Hz－55Hz, 50m/s, 15min
8	Shock Test (Package State)	Endurance test applying the shock during transportation	Half-sinewave, 100m/s, 11ms
9	Atmospheric Pressure Test	Endurance test applying the atmospheric pressure during transportation by air	40 kPa 16 H

7.2 Life Time

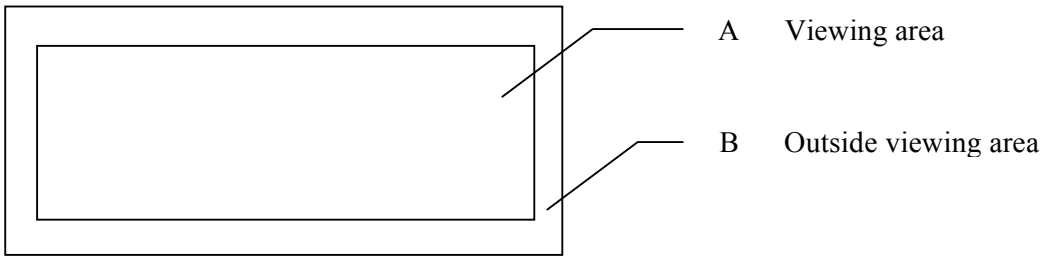
Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions of room temperature (25±10°C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.

*** Note: Test Condition**

1) Temperature and humidity: If no specification, Temperature set at 25±2°C, Humidity set at 60±5%RH;
2) Operating state: Samples subject to the tests shall be in " Operating " condition.

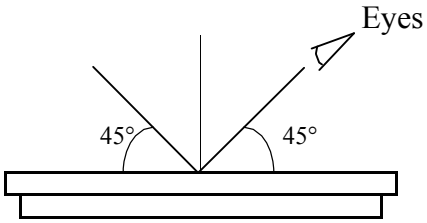
8. Quality Level

8.1 Zone Definition



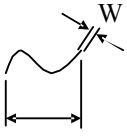
8.2 Visual Inspection

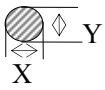
1) Inspect under 2x20W or 40W fluorescent lamp (approximately 3000 lux) leaving 25 to 30 cm between the module and the lamp and 30 cm between the module and the eye (measuring position).
2) Appearance is inspected at the best contrast voltage (best contrast is adjusted considering clearness and crosstalk on screen).
3) Inspect the module at 45° right and left, top and bottom.
4) Use the optimum viewing angle during the contrast inspection.

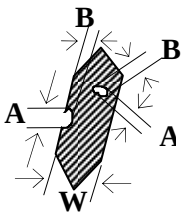


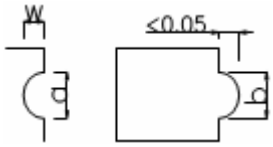
8.3 Standard of Apperance Inspection

<table>
<tr><th>No.</th><th>Item</th><th>Criteria</th></tr>
<tr><td>1</td><td>Black spot
White spot
Dust</td><td>
Round type: as per following drawing
Φ = (X+Y)/2

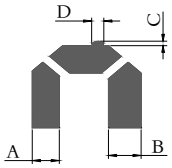
X
<table>
<tr><th colspan="3">Acceptable quantity</th></tr>
<tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr>
<tr><td>Φ <0.1</td><td>Any number</td><td rowspan="4">Any number</td></tr>
<tr><td>0.1< Φ <0.2</td><td>2</td></tr>
<tr><td>0.2< Φ <0.25</td><td>1</td></tr>
<tr><td>0.25< Φ</td><td>0</td></tr>
</table>
Line type: as per following drawing

W
L
<table>
<tr><th colspan="4">Acceptable quantity</th></tr>
<tr><th>Length</th><th>Width</th><th>Zone A</th><th>Zone B</th></tr>
<tr><td>—</td><td>W≤0.02</td><td>Any number</td><td rowspan="4">Any number</td></tr>
<tr><td>L≤3.0</td><td>0.02<W≤0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≤2.5</td><td>0.03<W≤0.05</td></tr>
<tr><td>—</td><td>0.05<W</td><td>As round type</td></tr>
</table>
Total acceptable quantity: 3
</td></tr>
<tr><td>2</td><td>Polariser scratch</td><td>Scratch on protective film is permitted</td></tr>
</table>

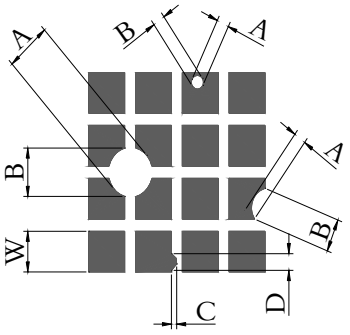
<table>
<tr><td></td><td></td><td>Scratch on polariser: same as No. 1</td></tr>
<tr><td>3</td><td>Polariser bubble</td><td>Φ = (X+Y)/2
 

<table>
<tr><td colspan="3">Acceptable quantity</td></tr>
<tr><td>Size</td><td>Zone A</td><td>Zone B</td></tr>
<tr><td>Φ <0.2</td><td>Any number</td><td rowspan="4">Any number</td></tr>
<tr><td>0.2< Φ <0.5</td><td>2</td></tr>
<tr><td>0.5< Φ <1.0</td><td>1</td></tr>
<tr><td>1.0< Φ</td><td>0</td></tr>
</table>
Total acceptable quantity: 3</td></tr>
<tr><td>4</td><td>Segment deformation</td><td>4.1 Pin hole on segmented display
W: segment width
Φ = (A+B)/2
 

<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Width</td><td>Quantity</td></tr>
<tr><td>W≤0.4</td><td>Φ ≤0.2 and Φ ≤1/2W</td></tr>
<tr><td>W>0.4</td><td>Φ ≤0.25 and
Φ ≤1/3W</td></tr>
<tr><td colspan="2">Total acceptable quantity: 1 defect per segment
Pin holes with Φ under 0.10 mm are acceptable</td></tr>
</table>
4.2 Pin hole on dot matrix display
 

<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>a, b<0.1</td><td>Any number</td></tr>
<tr><td>(a+b)/2≤0.1</td><td>Any number</td></tr>
<tr><td>0.5< Φ <1.0</td><td>3</td></tr>
</table>
Total acceptable quantity: 7

4.3 Segments / dots with different width
 

<table>
<tr><td colspan="2">Acceptable</td></tr>
<tr><td>a≥b</td><td>a/b≤4/3</td></tr>
<tr><td>a<b</td><td>a/b>4/3</td></tr>
</table>
4.4 Alignment layer defect
Φ = (A+B)/2
 

<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>Φ ≤0.4</td><td>Any number</td></tr>
<tr><td>0.4< Φ ≤1.0</td><td>5</td></tr>
<tr><td>1.0< Φ ≤1.5</td><td>3</td></tr>
<tr><td>1.5< Φ ≤2.0</td><td>2</td></tr>
</table>
Total acceptable quantity: 7</td></tr>
<tr><td>5</td><td>Colour uniformity</td><td>Level of sample for approval set as limit sample</td></tr>
</table>

<table>
<tr><td>6</td><td>Backlight</td><td>The backlight colour should correspond to the product specification
Flashing and or unlit backlight is not allowed
Dust larger than 0.25 mm is not allowed</td></tr>
<tr><td>7</td><td>COB</td><td>Exposed wire bond pad is not allowed
Insufficient covering with resin is not allowed (wire bond line exposed) Dust or bubble on the resin are not allowed</td></tr>
<tr><td>8</td><td>PCB</td><td>No unmelted solder paste should be present on PCB
Cold solder joints, missing solder connections, or oxidation are not allowed
No residue or solder balls on PCB are allowed
Short circuits on components are not allowed</td></tr>
<tr><td>9</td><td>Tray particles</td><td>
<table>
<tr><td colspan="3">Acceptable quantity</td></tr>
<tr><td></td><td>Size</td><td>Quantity</td></tr>
<tr><td rowspan="2">On tray</td><td>Φ <0.2</td><td>Any number</td></tr>
<tr><td>Φ >0.25</td><td>4</td></tr>
<tr><td rowspan="2">On display</td><td>Φ ≥0.25</td><td>2</td></tr>
<tr><td>L = 3</td><td>1</td></tr>
</table>
</td></tr>
</table>

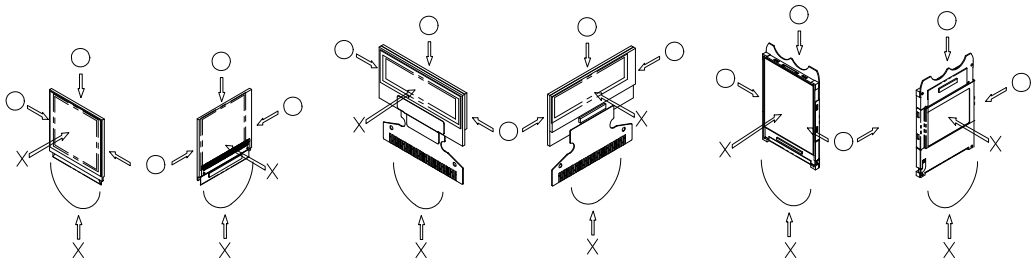
9. Package Specifications

TBD

10. Percautions When Using These LCD Display Modules

10.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the LCD Module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the LCD Module is soft and easily scratched. Please be careful when handling the LCD Module.
5) When the surface of the polarizer of the LCD Module has soil, clean the surface. It takes dvantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent.
   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold LCD Module very carefully when palcing LCD Module into the system housing. Do not apply excessive stress or pressure to LCD Module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the LCD Module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing LCD Modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling LCD Modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the LCD Module. Be careful since static electricity may be generated when exfoliating the protective film.
    * Protective film is being applied to the surface of the display panel of the LCD Module. Be careful since static electricity may be generated when exfoliating the protective film
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the LCD Module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the LCD Module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

10.2 Storage Precautions

1) When storing LCD Modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Blaze Display Technology Co., Ltd.)
   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the LCD Module, when the LCD Module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

10.3 Designing Precautions

1) The absolute maximum ratings are the ratings which can not be exceeded for LCD Module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as

possible.

3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)

5) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.

6) As for EMI, take necessary measures on the equipment side basically.
When fastening the LCD Module, fasten the external plastic housing section.

7) If power supply to the LCD Module is forcibly shut down by such errors as taking out the main battery while the LCD Panel is in operation, we cannot guarantee the quality of this LCD Module.

8) The electric potential to be connected to the rear face of the IC chip should be as follows:

* Connection (contact) to any other potential than the above may lead to rupture of the IC.

10.4 Precautions When Disposing of the LCD Modules

Request the qualified companies to handle industrial wastes when disposing of the LCD Modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

10.5 Other Precautions

1) When a LCD Module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module

2) To protect LCD Modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the LCD Modules.
* Pins and electrodes
* Pattern layouts such as the TCP & FPC

3) With this LCD Module, the LCD Module driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this LCD Module driver is exposed to light, malfunctioning may occur.
* Design the product and installation method so that the LCD Module driver may be shielded from light in actual usage.
* Design the product and installation method so that the LCD Module driver may be shielded from light during the inspection processes.

4) Although this LCD Module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.