

Product Specification

(Preliminary)

Part Name: Monochrome LCD Display Module

Part No.: BGB320240-06A SERIES

Doc No.: SAS1-1628-A

Customer: Blaze Display's Standard Part

Approved by:

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Revised History

Part Number	Revision	Revision Content	Revised on
BGB320240-06A-LW-FPTWD-V1.0	1.0	New	Apr. 27th, 2016
CONFIDENTIAL			



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1. Basic Specifications

1.1 Display Specifications

- | | |
|---------------------------|----------------------|
| 1) Display Type: | FSTN / Positive |
| 2) Display Format: | 320 × 240 Dots |
| 3) Graphic Color (ON): | Grey |
| 4) Background Color (ON): | Grey |
| Background Color (OFF): | Blue |
| 5) Drive Method: | 1/240 Duty; 1/17Bias |
| 6) Viewing Direction: | 6:00 |
| 7) Polarizer Type: | Transflective |

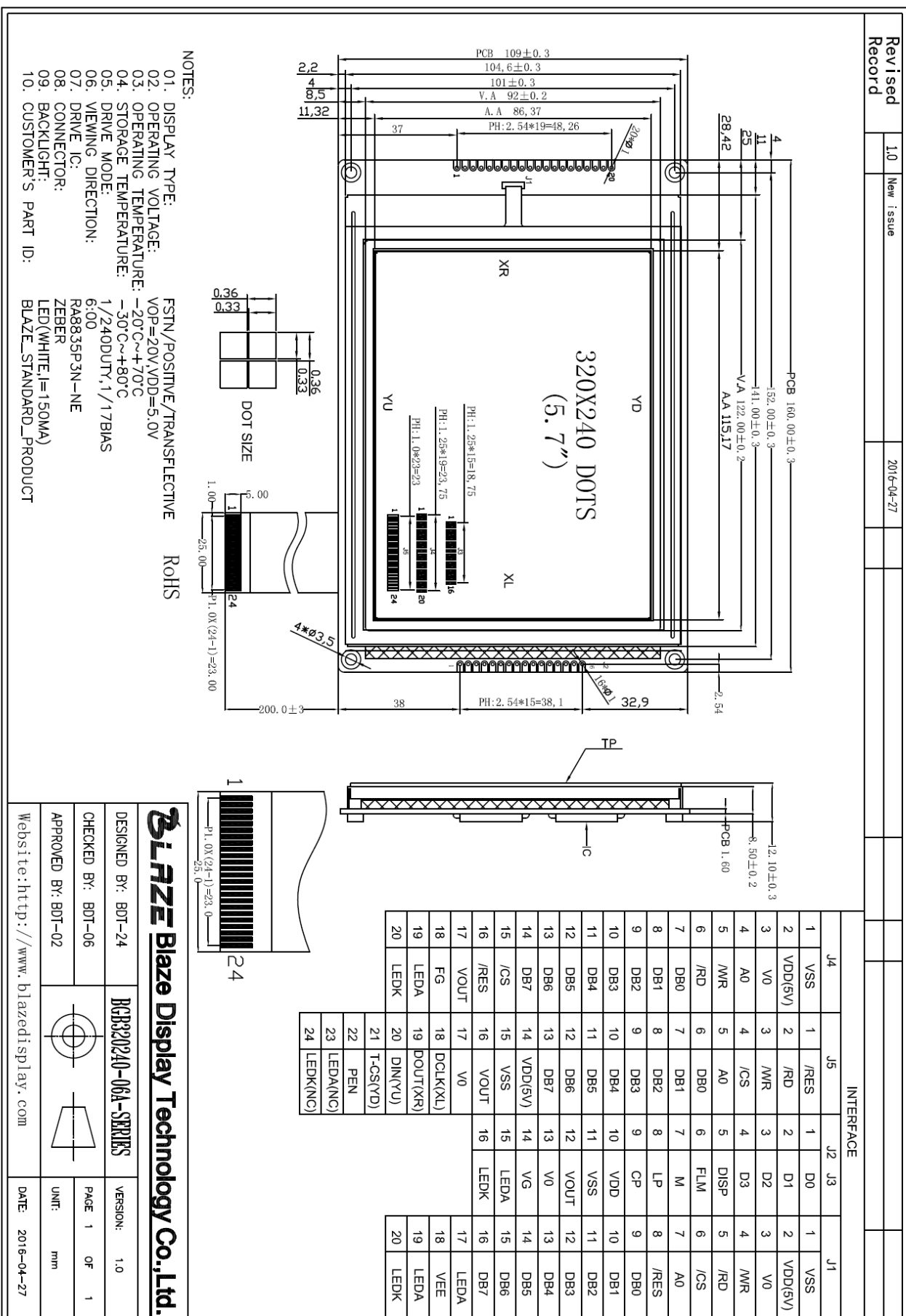
1.2 Mechanical Specifications

- | | |
|------------------------|---|
| 1) Outline Dimensions: | According to the annexed outline drawing on the next page |
| 2) Viewing Area: | 122.00 W × 92.00 H (mm) |
| 3) Active Area: | 115.17 W × 86.37 H (mm) |
| 4) Dot Pitch: | 0.36 W × 0.36 H (mm) |
| 5) Dot Size: | 0.33 W × 0.33H (mm) |
| 6) Weight: | 215g |

1.3 Others

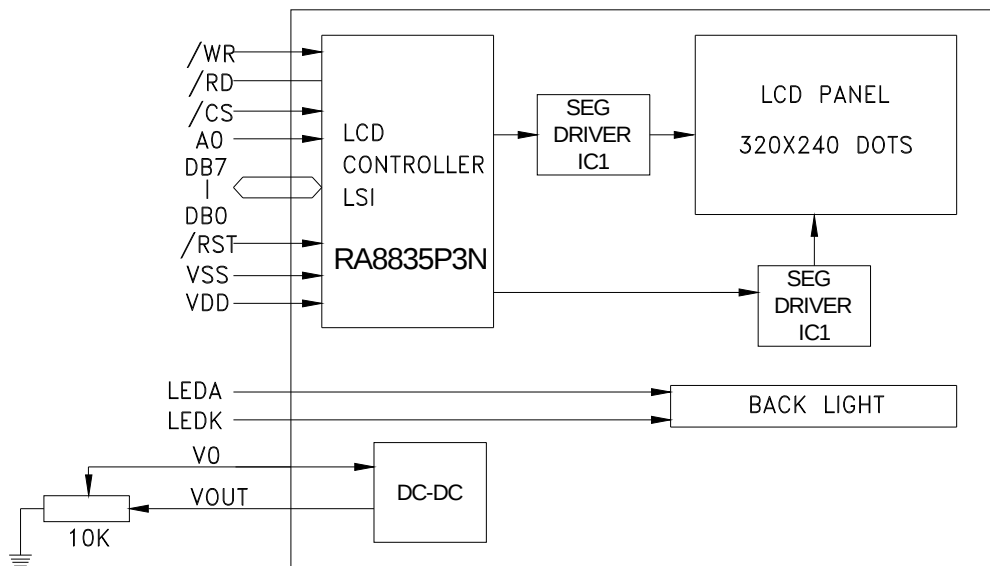
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|---------------------------|---|
| 1) Driver IC: | RA8835P3N or QEU |
| 2) Backlight: | LED, White, If = 150mA, Vf = 5.0 ± 0.2V |
| 3) Operating Temperature: | -20°C — + 70°C |
| 4) Storage Temperature: | -30°C — + 80°C |
| 5) RoHS Compliant: | Yes |

1.4 Mechanical Drawing



2. Electrical Specification

2.1 Block Diagram



2.2 Absolute Maximum Ratings

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply for Logic	$V_{DD}-V_{SS}$	-0.3	—	+7.0	V
Power supply for LCD Drive	$V_{DD}-V_0$	-0.3	—	25.0	V
Input Voltage	V_I	V_{SS}	—	V_{DD}	V
Operating Temperature	T_{OP}	-20	—	+70	°C
Storage Temperature	T_{ST}	-30	—	+80	°C
Static Electricity	Be sure that you are grounded when handling LCM				

2.3 Electrical Characteristics

$T_a = 25^{\circ}\text{C}$; $V_{dd} = 4.5 \sim 5.0\text{V}$, otherwise specified

Item	Symbol	Standard Value			Test Condition	Unit
		Min.	Typ.	Max.		
Supply Current for Logic	V_{DD}	+4.7	+5.0	+5.3	—	V
Supply Current for Logic	I_{DD}	—	TBD	—	—	mA
Supply Current for LCD	V_{LCD}	+18	+20	+22	25	°C

2.4 Pin Definition**J1:**

Pin No.	Symbol	Function
1	VSS	Ground (0V)
2	VDD	Power supply input for driver IC (+5V)
3	VO	LCD driver supply voltages, Contrast Adjust (-18V)
4	/WR	Write/Read-Write
5	/RD	Enable/Read Enable
6	/CS	L: Chip enable
7	A0	Register/Memory Select
8	/RST	H: Normal L: Initialize
9—16	DB0—DB7	Data bus line
17	LEDA	BACKLIGHT + (5V)
18	Vout	Negative Voltage output (-22V)
19	LEDA	BACKLIGHT + (5V)
20	LEDK	BACKLIGHT - (0V)

J2/J3:

Pin No.	Symbol	Function
1	D0	Display Data
2	D1	Display Data
3	D2	Display Data
4	D3	Display Data
5	DISP	H:ON L:OFF
6	FLM	First Line Marker
7	M	AC Drive Output
8	LP	Data Latch
9	CP	Data Shift
10	VDD	Power supply input for driver IC (+5V)
11	VSS	Ground (0V)
12	Vout	Negative Voltage output (-22V)
13	VO	LCD driver supply voltages, Contrast Adjust (-18V)
14	FG	Frame(Bezel)
15	LEDA	BACKLIGHT + (5V)
16	LEDK	BACKLIGHT - (0V)

J4:

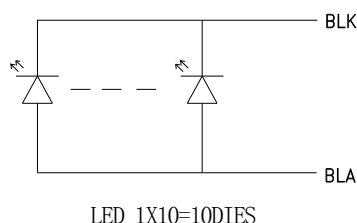
Pin No.	Symbol	Function
1	VSS	Ground (0V)
2	VDD	Power supply input for driver IC (+5V)
3	VO	LCD driver supply voltages, Contrast Adjust (-18V)
4	A0	Register/Memory Select
5	/WR	Write/Read-Write
6	/RD	Enable/Read Enable
7—14	DB0—DB7	Data bus line
15	/CS	L: Chip enable
16	/RST	H: Normal L: Initialize
17	Vout	Negative Voltage output (-22V)
18	FG	Frame(Bezel)
19	LEDA	BACKLIGHT + (5V)
20	LEDK	BACKLIGHT - (0V)

J5:

Pin No.	Symbol	Function
1	/RST	L: Chip enable
2	/RD	Enable/Read Enable
3	/WR	Write/Read-Write
4	/CS	L: Chip enable
5	A0	Register/Memory Select
6—13	DB0—DB7	Data bus line
14	VDD	Power supply input for driver IC (+5V)
15	VSS	Ground (0V)
16	Vout	Negative Voltage output(-22V)
17	VO	LCD driver supply voltages, Contrast Adjust(-18V)
18	DCLK(XL)	TP Serial Clock/ TP Left signal in X Axis
19	DOUT(XR)	TP Serial Data In/ TP Right signal in X Axis
20	DIN(YU)	TP Serial Data In/ TP Upper signal in Y Axis
21	T-CS(YD)	TP Chip Select/ TP Lower signal in Y Axis
22	PEN	TP Pen Interrupt
23	LEDA(NC)	BACKLIGHT + (5V)
24	LEDK(NC)	BACKLIGHT - (0V)

3. LED Backlight

3.1 Power Supply for LED Backlight



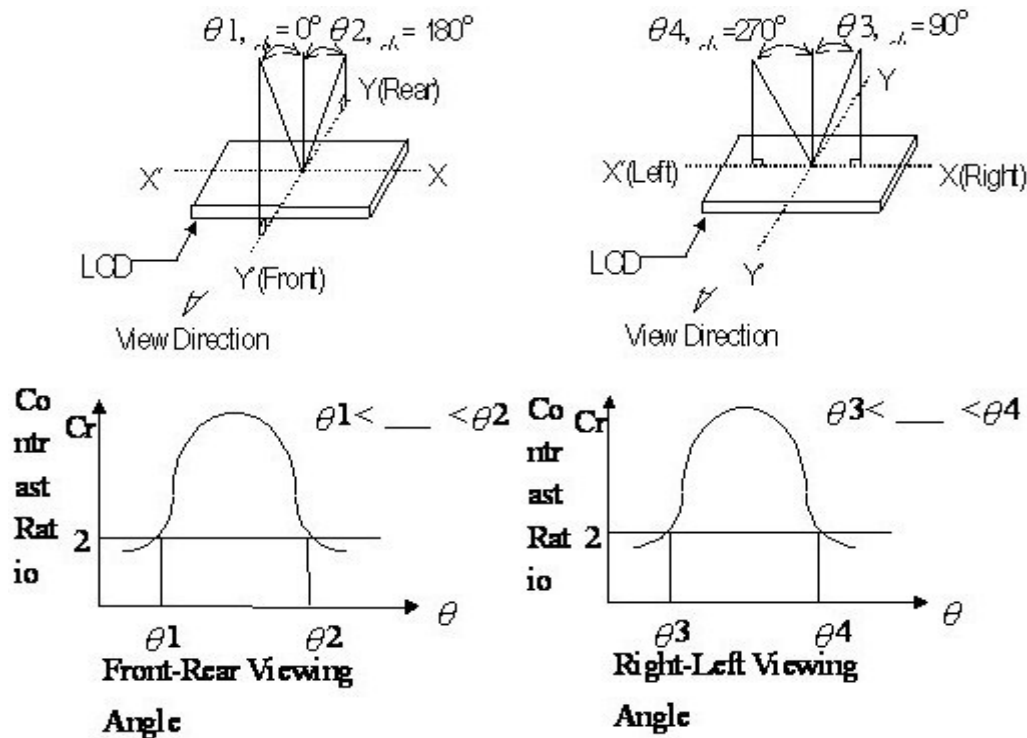
3.2 Electrical Optical Characteristics

Ta = 25°C; Vdd = 4.5~5.0V, otherwise specified

Item	Symbol	Conditions	Standard Value			Unit
			Min.	Typ.	Max.	
Forward Voltage	Vf	If = 150mA	2.8	3.0	3.2	V
Reverse Current	Ir	Vr = 5V	—	—	100	uA
Spectral Line Half Width	$\Delta\lambda$	IF = 150mA T = 25°C	—	—	—	nm
Peak Wave Length	λ_p		—	—	—	nm
Luminance	Lv	IF = 150mA	70	-	—	Cd/m ²
Uniformity	Δ	Min / Max = 100%	70%	—	-	%

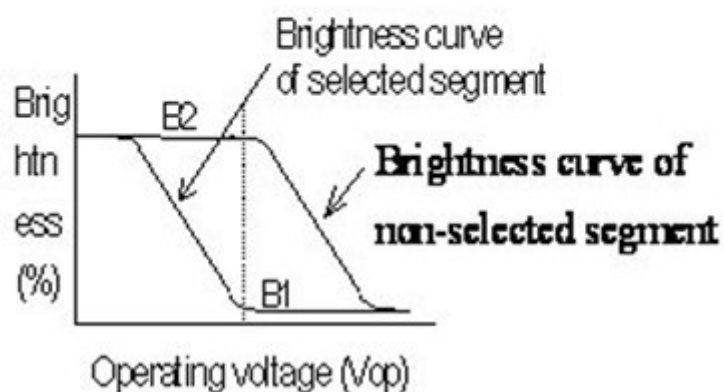
4. Optical Characteristics

4.1 Definition of Viewing Angle

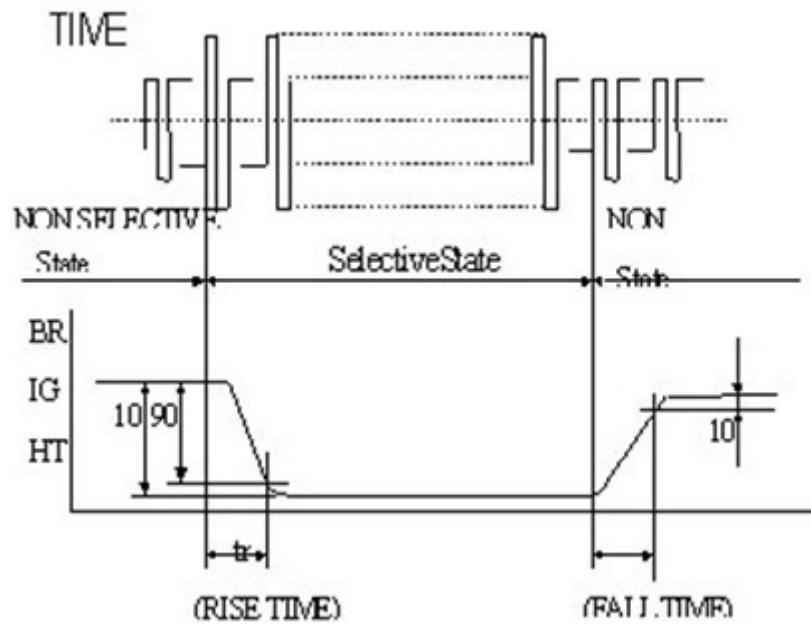


4.2 Definition of Contrast

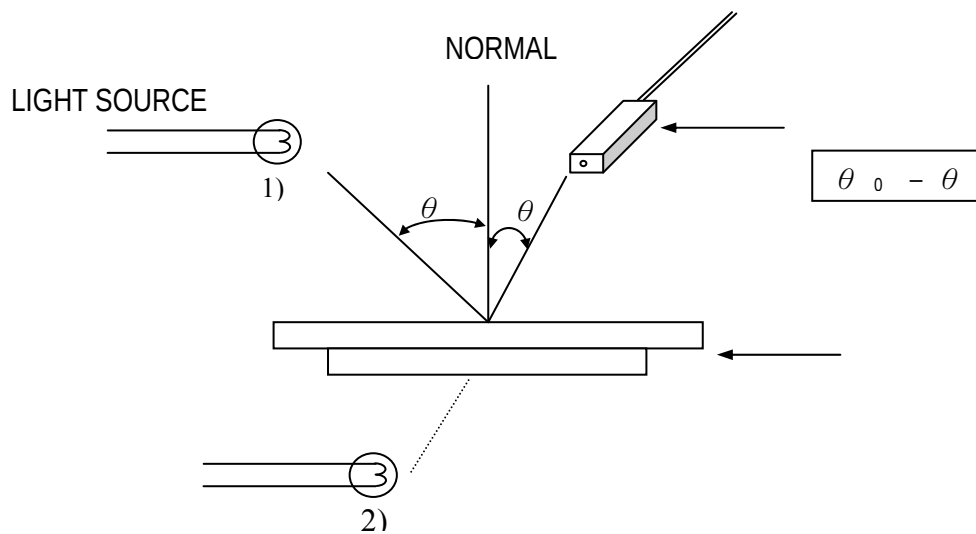
$$\text{C.R} = \frac{\text{Brightness of nonselected segment (E2)}}{\text{Brightness of selected segment}}$$



4.3 Definition of Response



4.4 Measuring Instruments For Electro-optical Characteristics

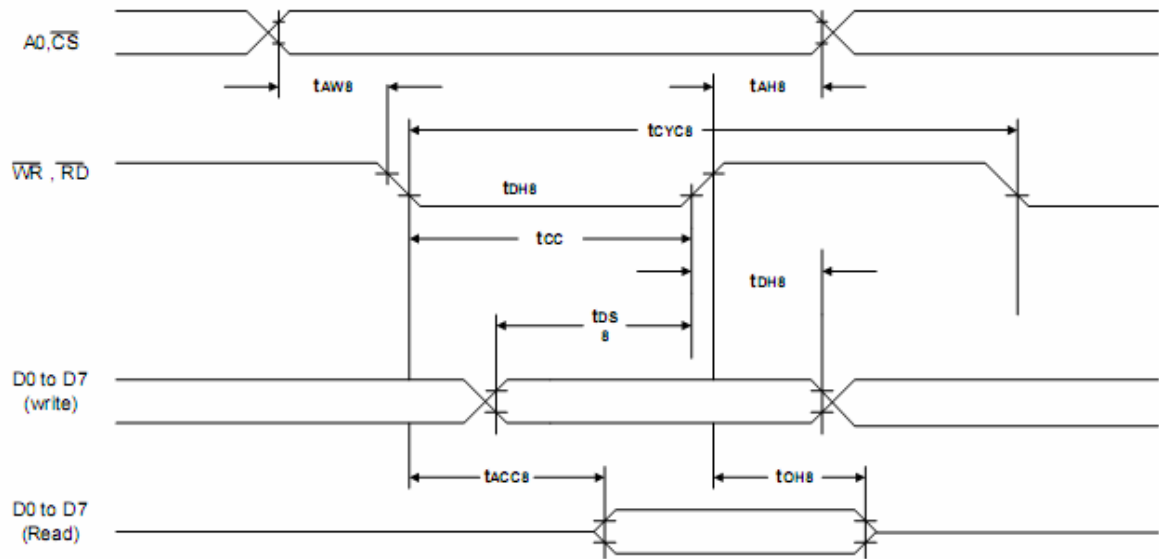


*** Note:**

- 1) Light source position for measuring the reflective type of LCD panel;
- 2) Light source position for measuring the transmissive / transmissive types of LCD panel.

5. Timing Diagrams

5.1 8080 Family Interface Timing



$T_a = -20$ to 75°C

Signal	Symbol	Parameter	$V_{DD} = 4.5$ to 5.5V		$V_{DD} = 2.7$ to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
$A0, \overline{CS}$	t_{AHB}	Address hold time	10	—	10	—	ns	CL = 100pF
	t_{AWB}	Address setup time	0	—	0	—	ns	
$\overline{WR}, \overline{RD}$	t_{CYB}	System cycle time	note.	—	note.	—	ns	
	t_{CC}	Strobe pulse width	120	—	150	—	ns	
D0 to D7	t_{DSB}	Data setup time	120	—	120	—	ns	
	t_{DHB}	Data hold time	5	—	5	—	ns	
	t_{ACCB}	$\overline{RD}$ access time	—	50	—	80	ns	
	t_{OHB}	Output disable time	10	50	10	55	ns	

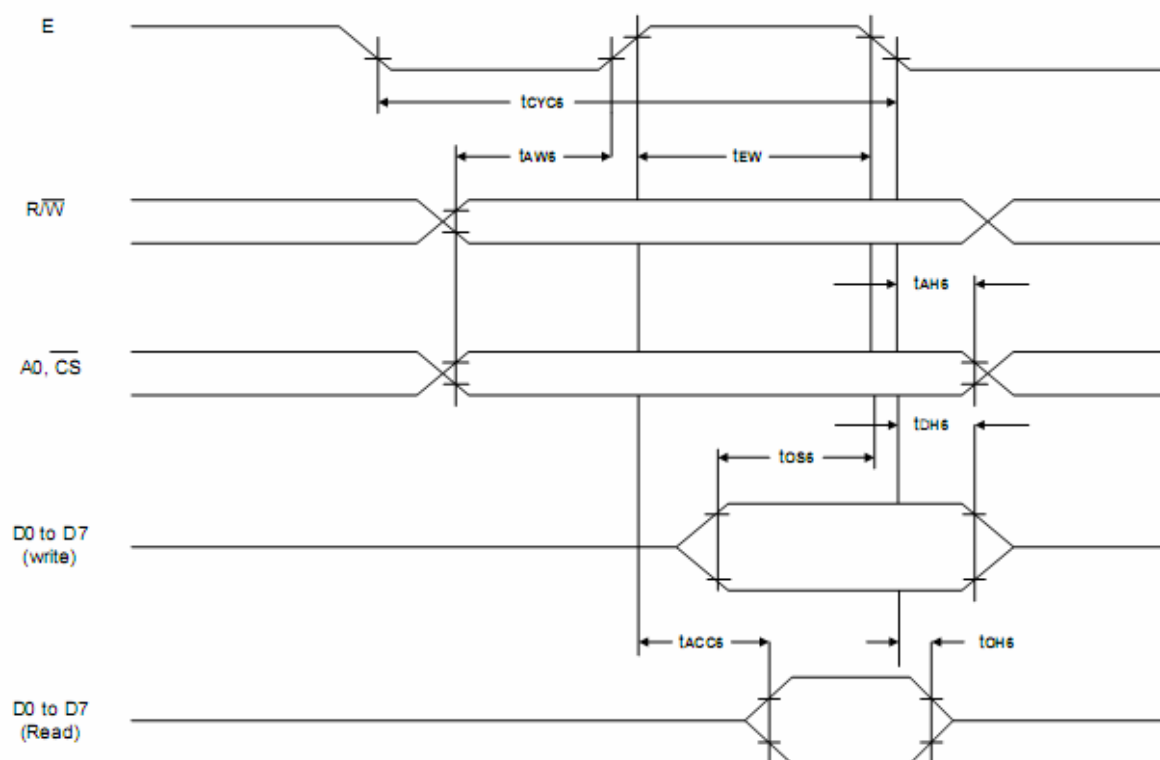
Note: For memory control and system control commands:

$$t_{CYB} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$$

For all other commands:

$$t_{CYB} = 4t_C + t_{CC} + 30$$

5.2 6800 Family Interface Timing



Ta = -20 to 75°C

Signal	Symbol	Parameter	V _{DD} = 4.5 to 5.5V		V _{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
A0, $\overline{\text{CS}}$, R/ $\overline{\text{W}}$	t _{CYC6}	System cycle time	note.	—	note.	—	ns	CL = 100 pF
	t _{AW6}	Address setup time	0	—	10	—	ns	
	t _{AH6}	Address hold time	0	—	0	—	ns	
D0 to D7	t _{DS6}	Data setup time	100	—	120	—	ns	
	t _{DH6}	Data hold time	0	—	0	—	ns	
	t _{OH6}	Output disable time	10	50	10	75	ns	
	t _{ACC6}	Access time	—	85	—	130	ns	
E	t _{EW}	Enable pulse width	120	—	150	—	ns	

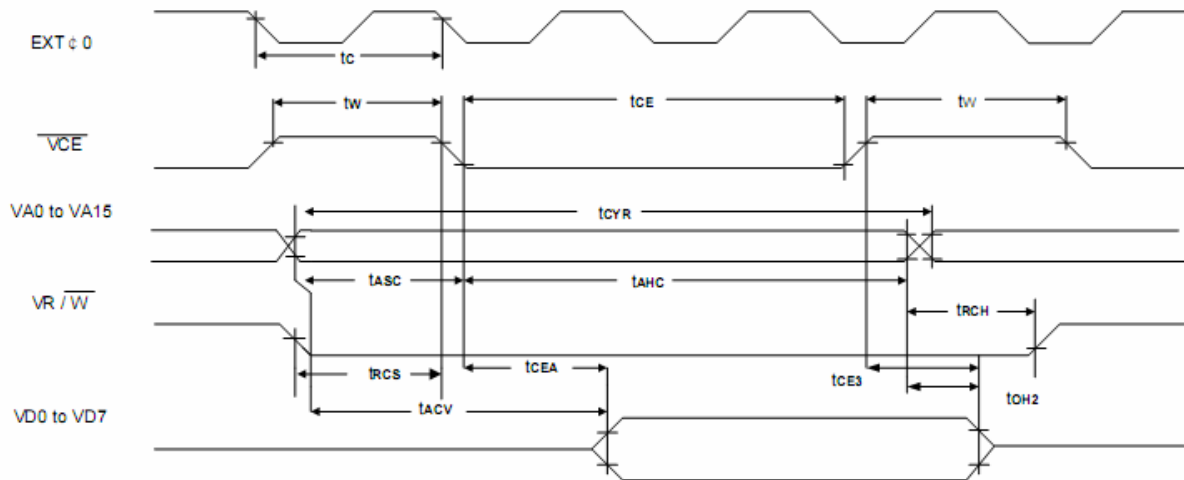
Note: For memory control and system control commands:

$$t_{\text{CYC6}} = 2t_{\text{C}} + t_{\text{EW}} + t_{\text{CEA}} + 75 > t_{\text{ACV}} + 245$$

For all other commands:

$$t_{\text{CYC6}} = 4t_{\text{C}} + t_{\text{EW}} + 30$$

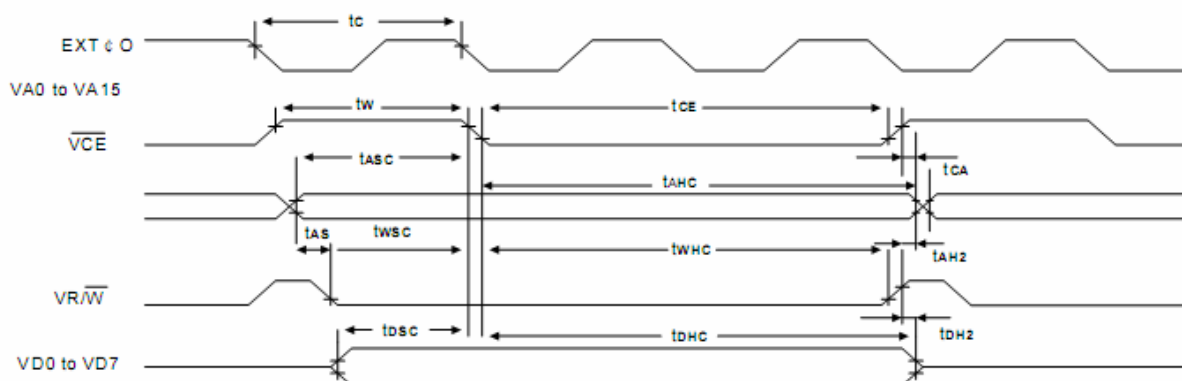
5.3 Display Memory Read Timing



Ta = -20 to 75°C

Signal	Symbol	Parameter	V _{DD} = 4.5 to 5.5V		V _{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
EXT Φ0	t _c	Clock period	100	—	125	—	ns	CL = 100 pF
VCE	t _w	VCE HIGH-level pulse width	t _c - 50	—	t _c - 50	—	ns	
	t _{CE}	VCE LOW-level pulse width	2t _c - 30	—	2t _c - 30	—	ns	
VA0 to VA15	t _{CYR}	Read cycle time	3t _c	—	3t _c	—	ns	
	t _{ASC}	Address setup time to falling edge of VCE	t _c - 70	—	t _c - 100	—	ns	
	t _{AHC}	Address hold time from falling edge of VCE	2t _c - 30	—	2t _c - 40	—	ns	
VRD	t _{RCS}	Read cycle setup time to falling edge of VCE	t _c - 45	—	t _c - 60	—	ns	
	t _{RCH}	Read cycle hold time from rising edge of VCE	0.5t _c	—	0.5t _c	—	ns	
VD0 to VD7	t _{ACV}	Address access time	—	3t _c - 100	—	3t _c - 115	Ns	
	t _{CEA}	VCE access time	—	2t _c - 80	—	2t _c - 90	Ns	
	t _{OH2}	Output data hold time	0	—	0	—	ns	
	t _{CE3}	VCE to data off time	0	—	0	—	ns	

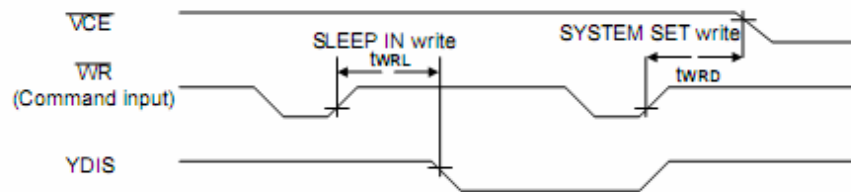
5.4 Display Memory Write Timing



$T_a = -20$ to 75°C

Signal	Symbol	Parameter	V _{DD} = 4.5 to 5.5V		V _{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
EXT Φ0	t _C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{\text{VCE}}$	t _W	VCE HIGH-level pulse width	t _C – 50	—	t _C – 50	—	ns	
	t _{CE}	VCE LOW-level pulse width	2t _C – 30	—	2t _C – 30	—	ns	
VA0 to VA15	t _{CYW}	Write cycle time	3t _C	—	3t _C	—	ns	
	t _{AHC}	Address hold time from falling edge of VCE	2t _C – 30	—	2t _C – 40	—	ns	
	t _{ASC}	Address setup time to falling edge of VCE	t _C – 70	—	t _C – 110	—	ns	
	t _{CA}	Address hold time from rising edge of $\overline{\text{VCE}}$	0	—	0	—	ns	
	t _{AS}	Address setup time to falling edge of $\overline{\text{WVR}}$	0	—	0	—	ns	
	t _{AH2}	Address hold time from rising edge of $\overline{\text{WVR}}$	10	—	10	—	ns	
$\overline{\text{WVR}}$	t _{WSC}	Write setup time to falling edge of VCE	t _C – 80	—	t _C – 115	—	ns	
	t _{WHC}	Write hold time from falling edge of VCE	2t _C – 20	—	2t _C – 20	—	ns	
VD0 to VD7	t _{DSC}	Data input setup time to falling edge of VCE	t _C – 85	—	t _C – 125	—	ns	
	t _{DHC}	Data input hold time from falling edge of VCE	2t _C – 30	—	2t _C – 30	—	ns	

5.5 Sleep In Command Timing



Ta = -20 to 75°C

Signal	Symbol	Parameter	V _{DD} = 4.5 to 5.5V		V _{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
$\overline{WR}$	t _{WRD}	$\overline{VCE}$ falling-edge delay time	note 1.	—	note 1.	—	ns	CL = 100 pF
	t _{WRL}	YDIS falling-edge delay time	—	note 2.	—	note 2.	ns	

Notes:

1. t_{WRD} = 18t_C + t_{oss} + 40 (t_{oss} is the time delay from the sleep state until stable operation)
2. t_{WRL} = 36t_C · [TC/R] · [L/F] + 70

6. Instruction Table

Table-1: Command Set

Class	Command	Code												Hex	Command Description	Command Read Parameters	
		RD	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	No. of Bytes			Section	
System Control	SYSTEM SET	1	0	1	0	1	0	0	0	0	0	0	40	Initialize device and display	8	9-2-1	
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enter standby mode	0	9-2-2	
Display Control	DISPLAY ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58, 59	Enable and disable display and display flashing	1	9-3-1	
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and display regions	10	9-3-2	
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor type	2	9-3-3	
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start address of character generator RAM	2	9-3-6	
	CSRDIR	1	0	1	0	1	0	0	1	1	CD 1	CD 0	4C to 4F	Set direction of cursor movement	0	9-3-4	
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position	1	9-3-7	
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format	1	9-3-5	
Drawing Control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address	2	9-r1	
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor address	2	9-4-2	
Memory Control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory	—	9-5-1	
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory	—	9-5-2	

Notes:

1. In general, the internal registers of the RA8835 series are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged. 2-byte parameters (where two bytes are treated as 1 data item) are handled as follows:

- CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.
- SYSTEM SET, SCROLL, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.

2. APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.

7. Reliability Specification

7.1 Contents of Reliability Tests

No.	Test Item	Content of Test	Test Condition
1	High Temperature Storage	Endurance test applying the high storage temperature for a long time	+70°C 96H
2	Low Temperature Storage	Endurance test applying the low storage temperature for a long time	-20°C 96H
3	High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the thermal stress to the element for a long time	+60°C 96H
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time	-10°C 96H
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and humidity storage for a long time	40°C 90%RH 96H
6	Temperature Cycle	Endurance test applying the low and high temperature cycle $ \begin{array}{ccccccc} -10^{\circ}\text{C} & \longleftrightarrow & 25^{\circ}\text{C} & \longleftrightarrow & 70^{\circ}\text{C} & \longleftrightarrow & 25^{\circ}\text{C} \\ 30\text{min} & & 5\text{min} & & 30\text{min} & & 5\text{min} \\ \longleftarrow & & & & & & \longrightarrow \\ & & & & & & 1 \text{ cycle} \end{array} $	-10°C/70°C 10 cycles
7	Vibration Test (Package State)	Endurance test applying the vibration during transportation	10Hz—55Hz, 50m/s, 15min
8	Shock Test (Package State)	Endurance test applying the shock during transportation	Half-sinewave, 100m/s, 11ms
9	Atmospheric Pressure Test	Endurance test applying the atmospheric pressure during transportation by air	40 kPa 16 H

7.2 Life Time

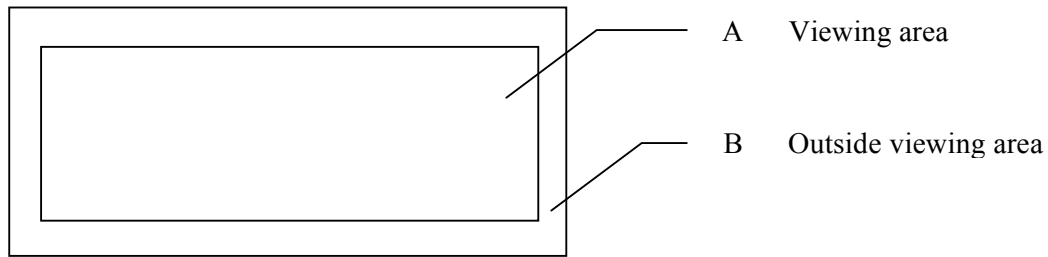
Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions of room temperature (25±10°C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.

* Note: Test Condition

- 1) Temperature and humidity: If no specification, Temperature set at 25±2°C, Humidity set at 60±5%RH;
- 2) Operating state: Samples subject to the tests shall be in “Operating” condition.

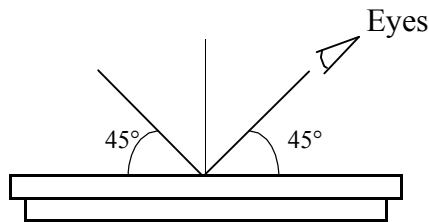
8. Quality Level

8.1 Zone Definition

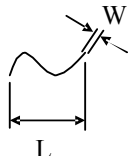
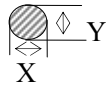
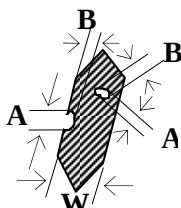
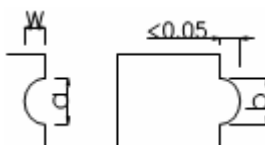


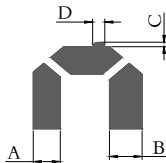
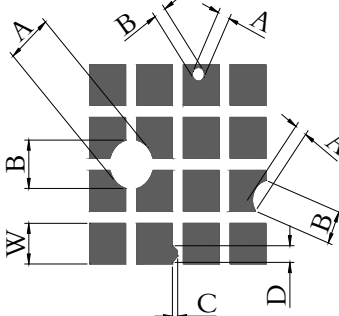
8.2 Visual Inspection

- 1) Inspect under 2x20W or 40W fluorescent lamp (approximately 3000 lux) leaving 25 to 30 cm between the module and the lamp and 30 cm between the module and the eye (measuring position).
- 2) Appearance is inspected at the best contrast voltage (best contrast is adjusted considering clearness and crosstalk on screen).
- 3) Inspect the module at 45° right and left, top and bottom.
- 4) Use the optimum viewing angle during the contrast inspection.



8.3 Standard of Apperance Inspection

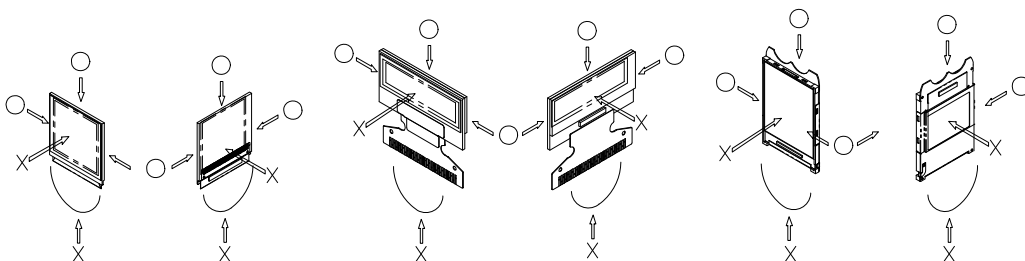
No.	Item	Criteria																		
1	Black spot White spot Dust	Round type: as per following drawing $\Phi = (X+Y)/2$  <table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>$\Phi < 0.1$</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>$0.1 < \Phi < 0.2$</td><td>2</td></tr><tr><td>$0.2 < \Phi < 0.25$</td><td>1</td></tr><tr><td>$0.25 < \Phi$</td><td>0</td></tr></table>	Acceptable quantity			Size	Zone A	Zone B	$\Phi < 0.1$	Any number	Any number	$0.1 < \Phi < 0.2$	2	$0.2 < \Phi < 0.25$	1	$0.25 < \Phi$	0			
		Acceptable quantity																		
		Size	Zone A	Zone B																
$\Phi < 0.1$	Any number	Any number																		
$0.1 < \Phi < 0.2$	2																			
$0.2 < \Phi < 0.25$	1																			
$0.25 < \Phi$	0																			
Line type: as per following drawing  <table><tr><th colspan="4">Acceptable quantity</th></tr><tr><th>Length</th><th>Width</th><th>Zone A</th><th>Zone B</th></tr><tr><td>—</td><td>$W \leq 0.02$</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>$L \leq 3.0$</td><td>$0.02 < W \leq 0.03$</td><td rowspan="2">2</td></tr><tr><td>$L \leq 2.5$</td><td>$0.03 < W \leq 0.05$</td></tr><tr><td>—</td><td>$0.05 < W$</td><td>As round type</td></tr></table>	Acceptable quantity				Length	Width	Zone A	Zone B	—	$W \leq 0.02$	Any number	Any number	$L \leq 3.0$	$0.02 < W \leq 0.03$	2	$L \leq 2.5$	$0.03 < W \leq 0.05$	—	$0.05 < W$	As round type
Acceptable quantity																				
Length	Width	Zone A	Zone B																	
—	$W \leq 0.02$	Any number	Any number																	
$L \leq 3.0$	$0.02 < W \leq 0.03$	2																		
$L \leq 2.5$	$0.03 < W \leq 0.05$																			
—	$0.05 < W$	As round type																		
		Total acceptable quantity: 3																		
2	Polariser scratch	Scratch on protective film is permitted Scratch on polariser: same as No. 1																		
3	Polariser bubble	$\Phi = (X+Y)/2$  <table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>$\Phi < 0.2$</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>$0.2 < \Phi < 0.5$</td><td>2</td></tr><tr><td>$0.5 < \Phi < 1.0$</td><td>1</td></tr><tr><td>$1.0 < \Phi$</td><td>0</td></tr></table>	Acceptable quantity			Size	Zone A	Zone B	$\Phi < 0.2$	Any number	Any number	$0.2 < \Phi < 0.5$	2	$0.5 < \Phi < 1.0$	1	$1.0 < \Phi$	0			
		Acceptable quantity																		
		Size	Zone A	Zone B																
$\Phi < 0.2$	Any number	Any number																		
$0.2 < \Phi < 0.5$	2																			
$0.5 < \Phi < 1.0$	1																			
$1.0 < \Phi$	0																			
		Total acceptable quantity: 3																		
4	Segment deformation	4.1 Pin hole on segmented display W: segment width $\Phi = (A+B)/2$  <table><tr><th colspan="2">Acceptable quantity</th></tr><tr><th>Width</th><th>Quantity</th></tr><tr><td>$W \leq 0.4$</td><td>$\Phi \leq 0.2$ and $\Phi \leq 1/2W$</td></tr><tr><td>$W > 0.4$</td><td>$\Phi \leq 0.25$ and $\Phi \leq 1/3W$</td></tr></table> Total acceptable quantity: 1 defect per segment Pin holes with Φ under 0.10 mm are acceptable	Acceptable quantity		Width	Quantity	$W \leq 0.4$	$\Phi \leq 0.2$ and $\Phi \leq 1/2W$	$W > 0.4$	$\Phi \leq 0.25$ and $\Phi \leq 1/3W$										
		Acceptable quantity																		
		Width	Quantity																	
$W \leq 0.4$	$\Phi \leq 0.2$ and $\Phi \leq 1/2W$																			
$W > 0.4$	$\Phi \leq 0.25$ and $\Phi \leq 1/3W$																			
4.2 Pin hole on dot matrix display  <table><tr><th colspan="2">Acceptable quantity</th></tr><tr><th>Size</th><th></th></tr><tr><td>a, b < 0.1</td><td>Any number</td></tr><tr><td>$(a+b)/2 \leq 0.1$</td><td>Any number</td></tr><tr><td>$0.5 < \Phi < 1.0$</td><td>3</td></tr></table>	Acceptable quantity		Size		a, b < 0.1	Any number	$(a+b)/2 \leq 0.1$	Any number	$0.5 < \Phi < 1.0$	3										
Acceptable quantity																				
Size																				
a, b < 0.1	Any number																			
$(a+b)/2 \leq 0.1$	Any number																			
$0.5 < \Phi < 1.0$	3																			
		Total acceptable quantity: 7																		
		4.3 Segments / dots with different width																		

		 <table><tr><th colspan="2">Acceptable</th></tr><tr><td>a>b</td><td>a/b≤4/3</td></tr><tr><td>a<b</td><td>a/b>4/3</td></tr></table> 4.4 Alignment layer defect Φ = (A+B)/2  <table><tr><th colspan="2">Acceptable quantity</th></tr><tr><th>Size</th><th></th></tr><tr><td>Φ≤0.4</td><td>Any number</td></tr><tr><td>0.4<Φ≤1.0</td><td>5</td></tr><tr><td>1.0<Φ≤1.5</td><td>3</td></tr><tr><td>1.5<Φ≤2.0</td><td>2</td></tr></table> Total acceptable quantity: 7	Acceptable		a>b	a/b≤4/3	a<b	a/b>4/3	Acceptable quantity		Size		Φ≤0.4	Any number	0.4<Φ≤1.0	5	1.0<Φ≤1.5	3	1.5<Φ≤2.0	2
Acceptable																				
a>b	a/b≤4/3																			
a<b	a/b>4/3																			
Acceptable quantity																				
Size																				
Φ≤0.4	Any number																			
0.4<Φ≤1.0	5																			
1.0<Φ≤1.5	3																			
1.5<Φ≤2.0	2																			
5	Colour uniformity	Level of sample for approval set as limit sample																		
6	Backlight	The backlight colour should correspond to the product specification Flashing and or unlit backlight is not allowed Dust larger than 0.25 mm is not allowed																		
7	COB	Exposed wire bond pad is not allowed Insufficient covering with resin is not allowed (wire bond line exposed) Dust or bubble on the resin are not allowed																		
8	PCB	No unmelted solder paste should be present on PCB Cold solder joints, missing solder connections, or oxidation are not allowed No residue or solder balls on PCB are allowed Short circuits on components are not allowed																		
9	Tray particles	<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th></th><th>Size</th><th>Quantity</th></tr><tr><td rowspan="2">On tray</td><td>Φ < 0.2</td><td>Any number</td></tr><tr><td>Φ > 0.25</td><td>4</td></tr><tr><td rowspan="2">On display</td><td>Φ ≥ 0.25</td><td>2</td></tr><tr><td>L = 3</td><td>1</td></tr></table>	Acceptable quantity				Size	Quantity	On tray	Φ < 0.2	Any number	Φ > 0.25	4	On display	Φ ≥ 0.25	2	L = 3	1		
Acceptable quantity																				
	Size	Quantity																		
On tray	Φ < 0.2	Any number																		
	Φ > 0.25	4																		
On display	Φ ≥ 0.25	2																		
	L = 3	1																		

9. Precautions When Using These LCD Modules

9.1 Handling Precautions

- 1) Since the display panel is being made of glass, do not apply mechanical impacts such as dropping from a high position.
- 2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
- 3) If pressure is applied to the display surface or its neighborhood of the LCD Module, the cell structure may be damaged and be careful not to apply pressure to these sections.
- 4) The polarizer covering the surface of the LCD Module is soft and easily scratched. Please be careful when handling the LCD Module.
- 5) When the surface of the polarizer of the LCD Module has soil, clean the surface. It takes dvantage of by using following adhesion tape.
 - * Scotch Mending Tape No. 810 or an equivalent.Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
Also, pay attention that the following liquid and solvent may spoil the polarizer:
 - * Water
 - * Ketone
 - * Aromatic Solvents
- 6) Hold LCD Module very carefully when palcing LCD Module into the system housing. Do not apply excessive stress or pressure to LCD Module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



- 7) Do not apply stress to the LSI chips and the surrounding molded sections.
- 8) Do not disassemble nor modify the LCD Module.
- 9) Do not apply input signals while the logic power is off.
- 10) Pay sufficient attention to the working environments when handing LCD Modules to prevent occurrence of element breakage accidents by static electricity.
 - * Be sure to make human body grounding when handling LCD Modules.
 - * Be sure to ground tools to use or assembly such as soldering irons.
 - * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
 - * Protective film is being applied to the surface of the display panel of the LCD Module. Be careful since static electricity may be generated when exfoliating the protective film.
 - * Protective film is being applied to the surface of the display panel of the LCD Module. Be careful since static electricity may be generated when exfoliating the protective film
- 11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the LCD Module has been stored

for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

- 12) If electric current is applied when the LCD Module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

9.2 Storage Precautions

- 1) When storing LCD Modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Blaze Display Technology Co., Ltd.)
At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
- 2) If electric current is applied when water drops are adhering to the surface of the LCD Module, when the LCD Module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

9.3 Designing Precautions

- 1) The absolute maximum ratings are the ratings which can not be exceeded for LCD Module, and if these values are exceeded, panel damage may be happen.
- 2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
- 3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
- 5) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
- 6) As for EMI, take necessary measures on the equipment side basically.
When fastening the LCD Module, fasten the external plastic housing section.
- 7) If power supply to the LCD Module is forcibly shut down by such errors as taking out the main battery while the LCD Panel is in operation, we cannot guarantee the quality of this LCD Module.
- 8) The electric potential to be connected to the rear face of the IC chip should be as follows:
 - * Connection (contact) to any other potential than the above may lead to rupture of the IC.

9.4 Precautions When Disposing of the LCD Modules

Request the qualified companies to handle industrial wastes when disposing of the LCD Modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.



9.5 Other Precautions

- 1) When a LCD Module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module
- 2) To protect LCD Modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the LCD Modules.
 - * Pins and electrodes
 - * Pattern layouts such as the TCP & FPC
- 3) With this LCD Module, the LCD Module driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this LCD Module driver is exposed to light, malfunctioning may occur.
 - * Design the product and installation method so that the LCD Module driver may be shielded from light in actual usage.
 - * Design the product and installation method so that the LCD Module driver may be shielded from light during the inspection processes.
- 4) Although this LCD Module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
- 5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.