Product Specification

(Preliminary)

Part Name: Monochrome LCD Display Module

Part No.: BGB320240-07 SERIES

Doc No.: SAS1-1518-A

Customer:
Approved by:

From: Blaze Display Technology Co., Ltd.
Approved by:

Blaze Display Technology Co., Ltd.

5/F, HSAE Tech Building, Hi-Tech Park, Nanshan, Shenzhen, China, 518057

Http://www.blazedisplay.com

Notes:

1. Please contact Blaze Display Technology Co., Ltd. before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Blaze Display Technology Co., Ltd. for any intellectual property claims or other problems that may result application based on the module described herein.

Revised History

Part Number	Revision	Revision Content	Revised on
BGB320240-07-LW-SNMWD-1.0	1.0	New	May 08th, 2015

CONFIDENTIAL

Notice:

Contents

1. Basic Specifications

1.1 Display Specifications

1) Display Type:	STN-Blue/ Negative
2) Display Format:	320 × 240
3) Character Color (ON):	White
4) Background Color (ON):	Blue
Background Color (OFF):	Blue
5) Drive Method:	1/240Duty; 1/17Bias
6) Viewing Direction:	6:00
7) Polarizer Type:	Transmissive

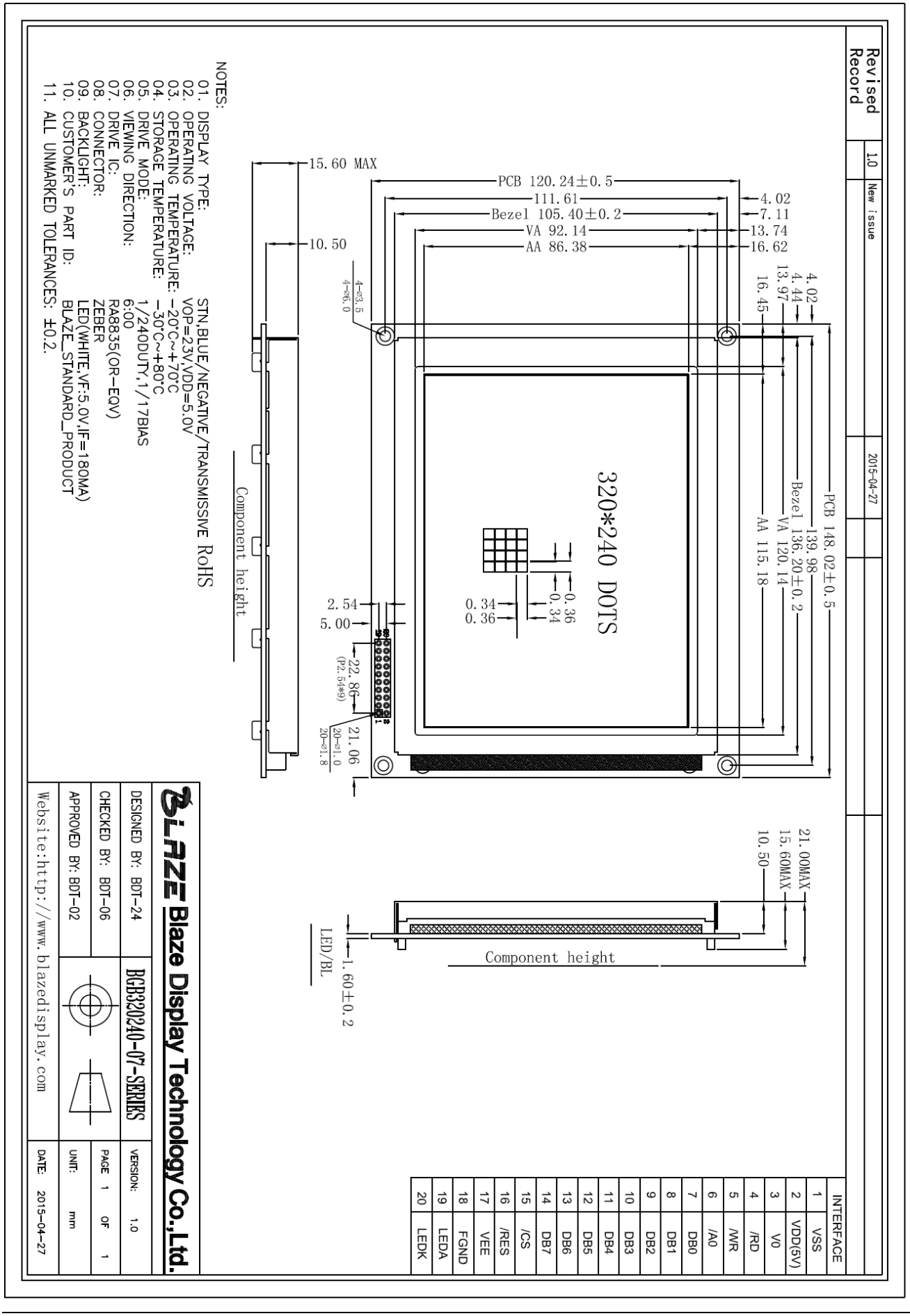
1.2 Mechanical Specifications

1) Outline Dimensions:	According to the annexed outline drawing on the next page
2) Viewing Area:	120.14 W × 92.14 H (mm)
3) Active Area:	115.18 W × 86.38 H (mm)
4) Dot Pitch:	0.36W × 0.36 H (mm)
5) Dot Size:	0.34 W × 0.34H (mm)
6) Weight:	T.B.D.

1.3 Others

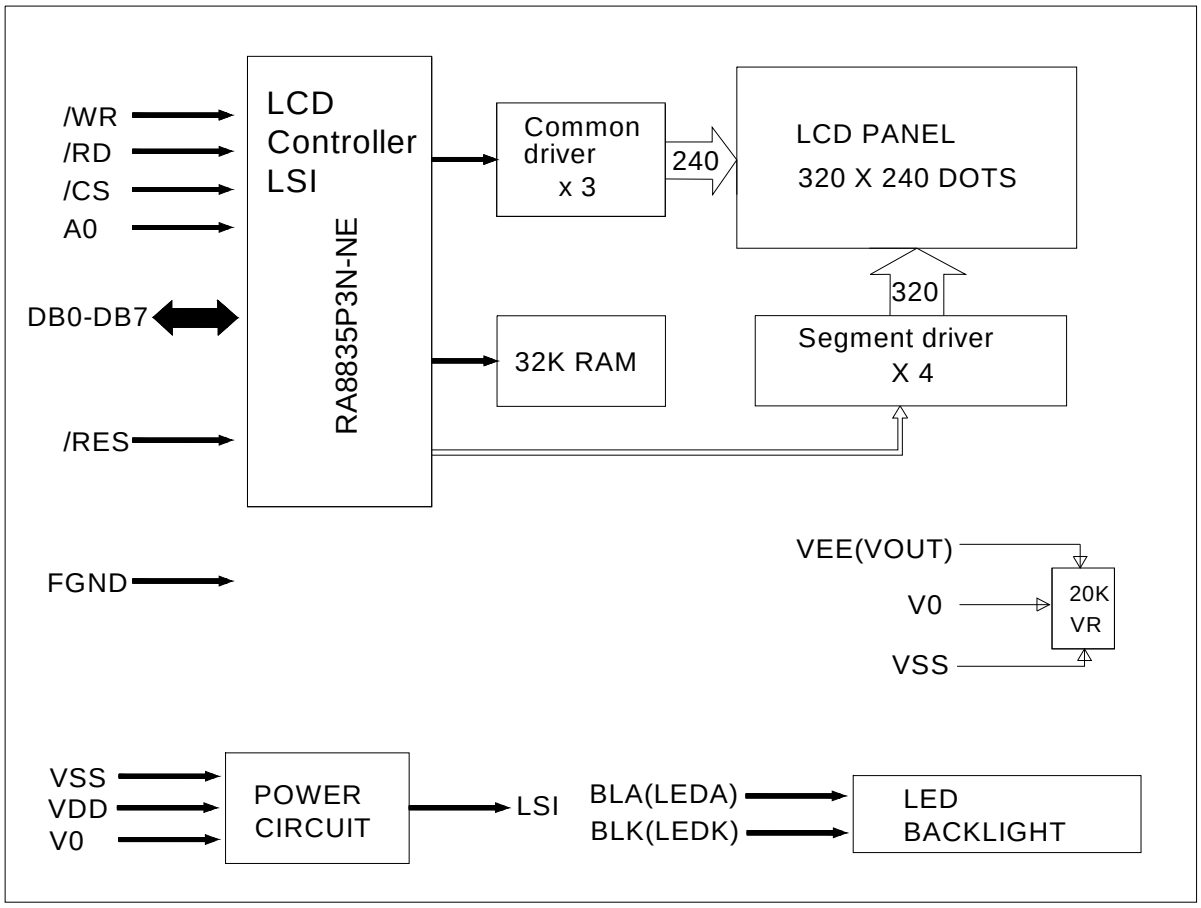
1) Driver IC:	RA8835P3N-NE or EQU
2) Backlight:	LED, White, If = 180mA, Vf = 5.0±0.2V
3) Operating Temperature:	-20°C— + 70°C
4) Storage Temperature:	-30°C— + 80°C
5) RoHS Compliant:	Yes

1.4 Mechanical Drawing



2. Electrical Specification

2.1 Block Diagram



2.2 Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Power Supply for Logic	Vdd	−0.3	+5.5	V
Power supply for LCD Drive	Vlcd	22.5	23.5	V
Input Voltage	Vin	−0.3	Vdd + 0.3	V
Operating Temperature	Topr	−20	+70	°C
Storage Temperature	Tstg	−30	+80	°C

2.3 Electrical Characteristics

V_{DD} = 2.7 to 5.5V, V_{SS} = 0V, Ta = –20 to 75℃

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	V
Supply voltage	V_{DD}		2.7	3.3/5.0	5.5	V
Register data retention voltage	V_{OH}		2.0	—	6.0	V
Input leakage current	I_{LI}	VI= VDD. See note 5.	—	0.05	2.0	μA
Output leakage current	I_{LO}	VI= VSS. See note 5.	—	0.10	5.0	μA
Operating supply current	Iopr	See note 4.	—	11	15	mA
Quiescent supply current	I_Q	Sleep mode, VOSC1= V($\overline{CS}$)= V($\overline{RD}$)= VDD	—	0.05	20.0	μA
Oscillator frequency	f_{OSC}	Measured at crystal, 47.5% duty cycle. See note 6.	1.0	—	18.0	MHz
External clock frequency	f_{CL}		1.0	—	10.0	MHz
Oscillator feedback resistance	Rf		0.5	1.0	3.0	MΩ
TTL						
HIGH-level input voltage	V_{IHT}	See note 1.	0.5V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILT}	See note 1.	V_{SS}	—	0.2 V_{DD}	V
HIGH-level output voltage	V_{OHT}	IOH= –5.0 mA. See note 1.	2.4	—	—	V
LOW-level output voltage	V_{OLT}	IOL= 5.0 mA. See note 1.	—	—	V_{SS} + 0.4	V
CMOS						
HIGH-level input voltage	V_{IHC}	See note 2.	0.8 V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILC}	See note 2.	V_{SS}	—	0.2 V_{DD}	V
HIGH-level output voltage	V_{OHC}	IOH= –2.0 mA. See note 2.	V_{DD} – 0.4	—	—	V
LOW-level output voltage	V_{OLC}	IOH= 1.6 mA. See note 2.	—	—	VSS+ 0.4	V
Open-drain						
LOW-level output voltage	V_{OLN}	IOL= 6.0 mA.	—	—	V_{SS} + 0.4V	V
Schmitt-trigger						
Rising-edge threshold voltage	V_{T+}	See note 3.	0.5 V_{DD}	0.7 V_{DD}	0.8 V_{DD}	V
Falling-edge threshold voltage	V_{T-}	See note 3.	0.2 V_{DD}	0.3 V_{DD}	0.5 V_{DD}	V

Notes:

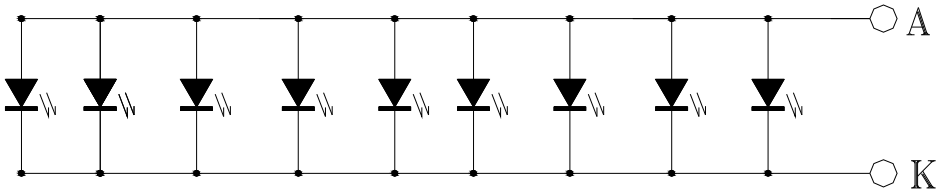
1. D0 to D7, A0, ($\overline{CS}$), ($\overline{RD}$), ($\overline{WR}$), VD0 to VD7, VA0 to VA15, ($\overline{VRD}$), ($\overline{VWR}$) and ($\overline{VCE}$) are TTL-level inputs.
2. SEL1 is CMOS-level inputs. YD, XD0 to XD3, XSCL, LP, WF, YDIS are CMOS-level outputs.
3. $\overline{RES}$ is an Schmitt-trigger input. The pulse width on ($\overline{RES}$) must be at least 200us. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.
4. f_{OSC} = 10 MHz, no load (no display memory), internal character generator, 256x200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.
5. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.
6. Because the oscillator circuit input bias current is in the order of uA, design the printed circuit board so as to reduce leakage currents.

2.4 Pin Definition(J1)

No.	Symbol	Function
1	VSS	Ground (0V)
2	VDD	Supply Voltage for Logic (+5.0V)
3	V0	Contrast Adjustment
4	/RD	Read Control or Enable
5	/WR	Write Control or Read/Write Control
6	A0	Command/Data Select
7-14	DB0-DB7	Data Bus
15	/CS	Chip select
16	/RES	Hardware Reset
17	VEE	Negative output
18	FGND	Frame Ground
19	LEDA	LED Power Supply + (5.0V)
20	LEDK	LED Power Supply - (0V)

3. LED Backlight

3.1 Power Supply for LED Backlight



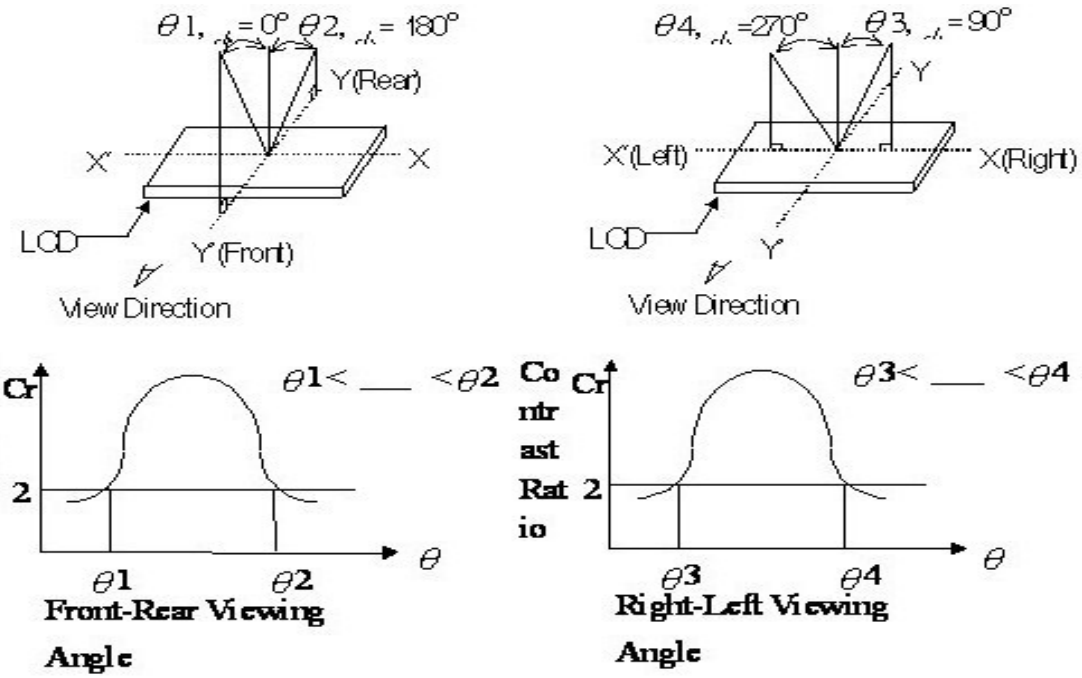
3.2 Electrical Optical Characteristics

Ta = 25°C; Vdd = 5.0V, otherwise specified

Item	Symbol	Conditions	Standard Value			Unit
			Min.	Typ.	Max.	
Forward Voltage	Vf	If = 180mA	4.9	5.0	5.1	V
Reverse Current	Ir	Vr = 5.0V	–	–	100	uA
Spectral Line Half Width	△λ	IF = 180mA T = 25℃	–	–	–	nm
Peak Wave Length	λp		–	–	–	nm
Luminance	Lv	IF =180mA	–	80	–	Cd/m^2
Uniformity	△	Min / Max = 100%	–	–	75%	%

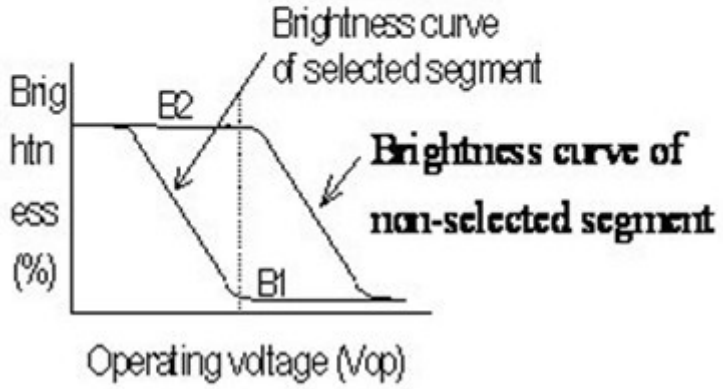
4. Optical Characteristics

4.1 Definition of Viewing Angle

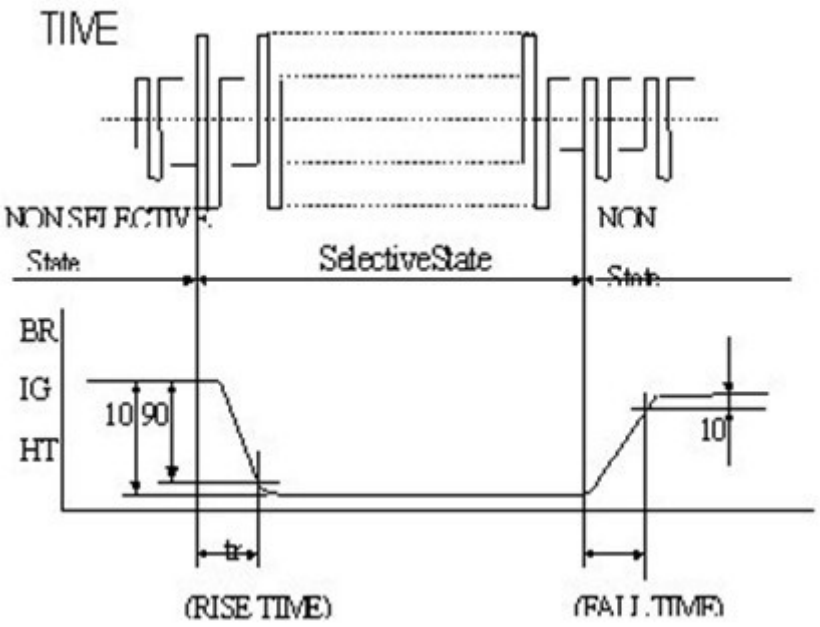


4.2 Definition of Contrast

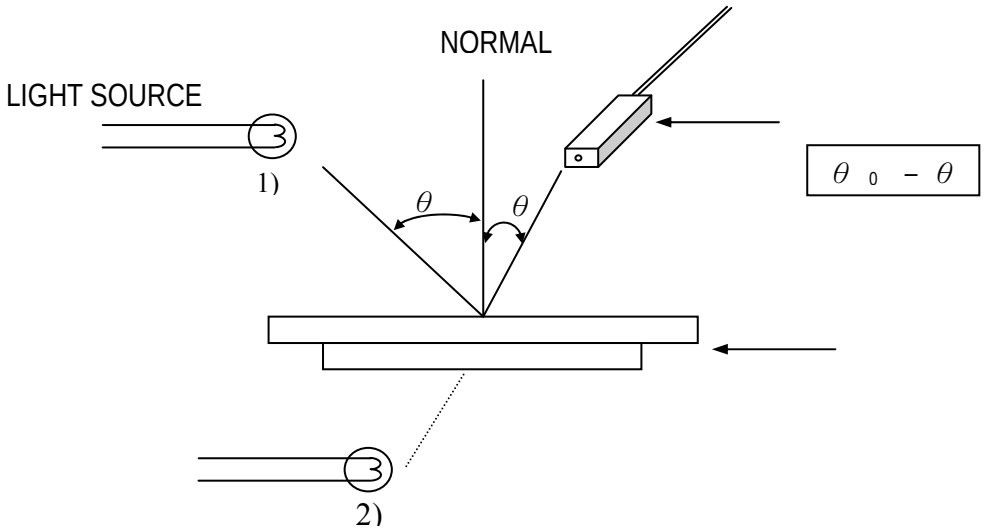
$$C.R = \frac{\text{RATIO Brightness of nonselected segment (B2)}}{\text{Brightness of selected segment}}$$



4.3 Definition of Response



4.4 Measuring Instruments For Electro-optical Characteristics



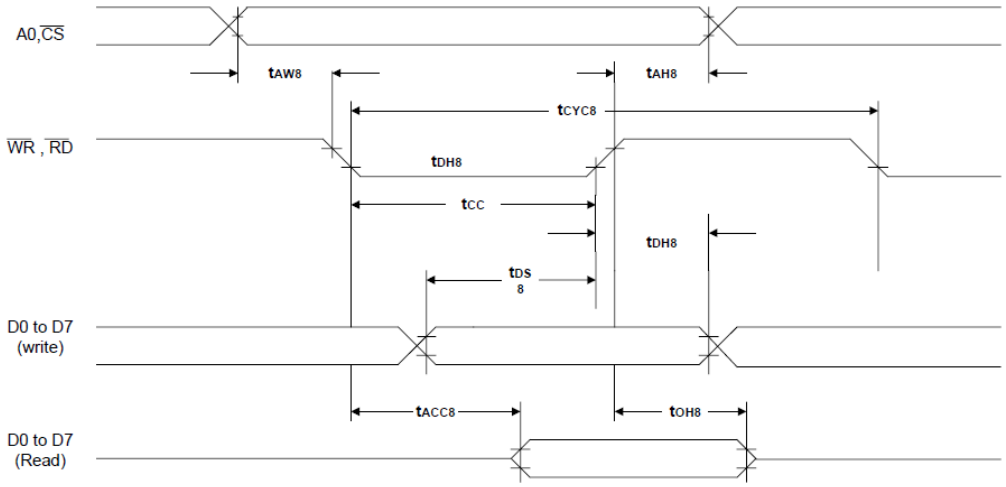
*** Note:**

1) Light source position for measuring the reflective type of LCD panel;
2) Light source position for measuring the transflective / transmissive types of LCD panel.

5. AC Characteristics and Input Timing Characteristics

5.1 AC characteristics (Vdd=5V, Vss=0V Ta=25°C)

10-3-1 8080 Family Interface Timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
A0, $\overline{CS}$	t_{AH8}	Address hold time	10	—	10	—	ns	CL = 100pF
	t_{AW8}	Address setup time	0	—	0	—	ns	
$\overline{WR}$, $\overline{RD}$	t_{CYC8}	System cycle time	note.	—	note.	—	ns	
	t_{CC}	Strobe pulse width	120	—	150	—	ns	
D0 to D7	t_{DS8}	Data setup time	120	—	120	—	ns	
	t_{DH8}	Data hold time	5	—	5	—	ns	
	t_{ACC8}	$\overline{RD}$ access time	—	50	—	80	ns	
	t_{OH8}	Output disable time	10	50	10	55	ns	

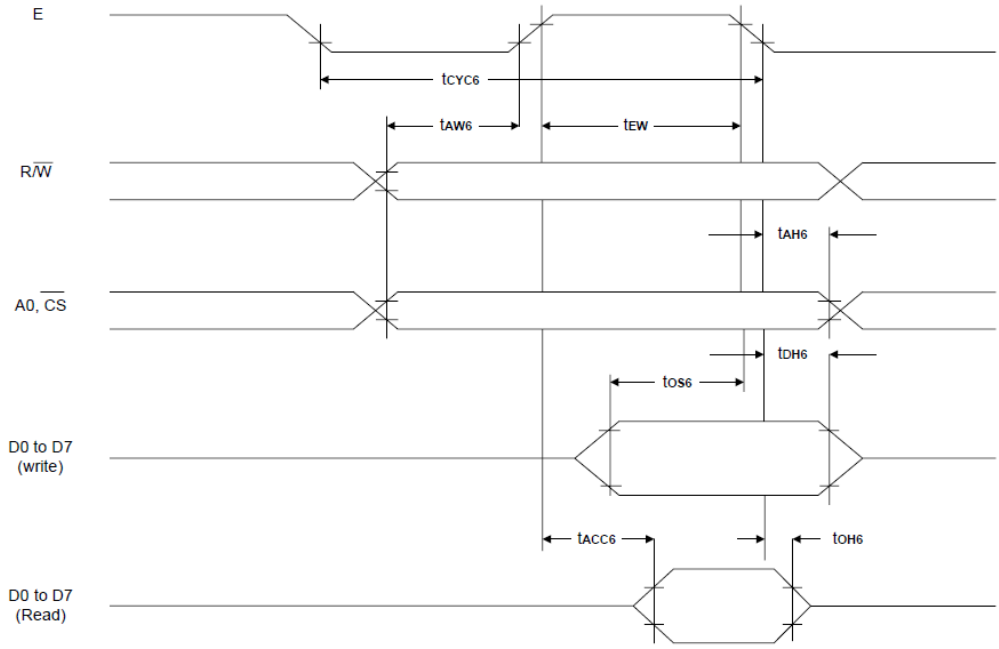
Note: For memory control and system control commands:

$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4t_C + t_{CC} + 30$

10-3-2 6800 Family Interface Timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
A0, $\overline{CS}$, R/(/W)	t_{CYC6}	System cycle time	note.	—	note.	—	ns	CL = 100 pF
	t_{AW6}	Address setup time	0	—	10	—	ns	
	t_{AH6}	Address hold time	0	—	0	—	ns	
D0 to D7	t_{DS6}	Data setup time	100	—	120	—	ns	
	t_{DH6}	Data hold time	0	—	0	—	ns	
	t_{OH6}	Output disable time	10	50	10	75	ns	
	t_{ACC6}	Access time	—	85	—	130	ns	
E	t_{EW}	Enable pulse width	120	—	150	—	ns	

Note: For memory control and system control commands:

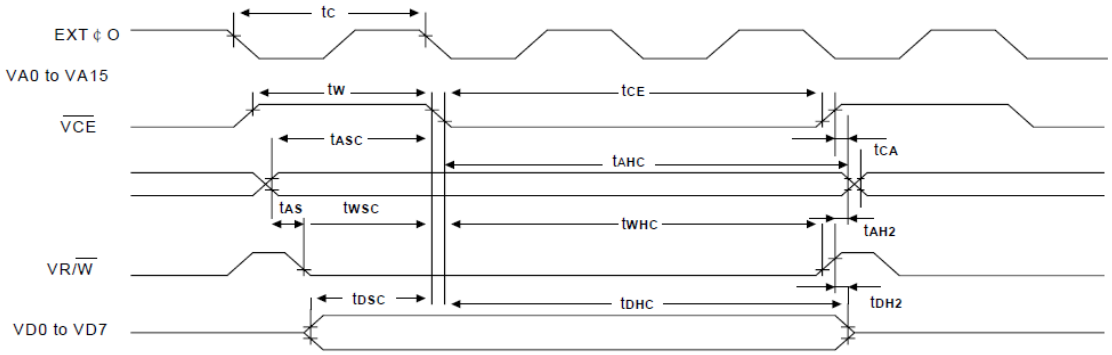
$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC6} = 4t_C + t_{EW} + 30$

5.2 Write Mode

10.3-4 Display Memory Write Timing



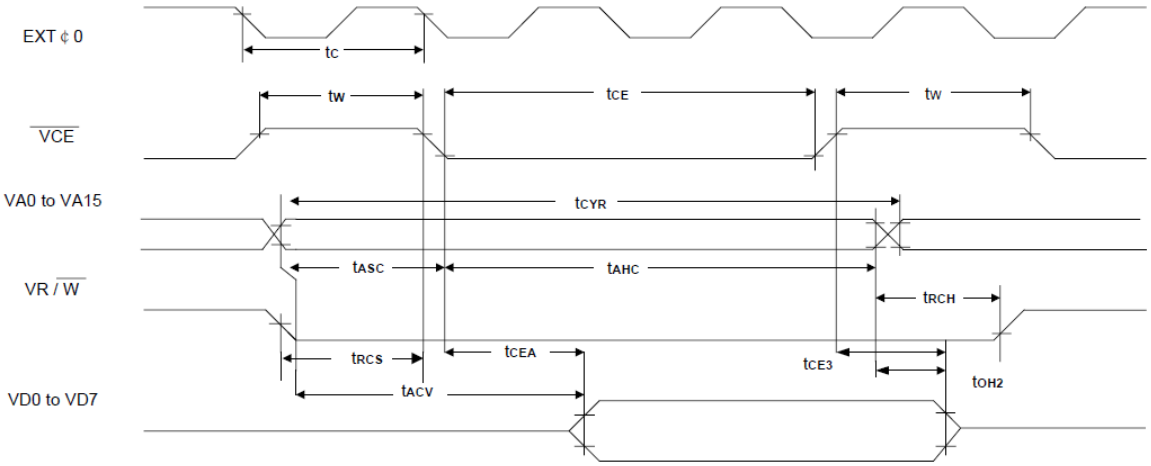
Ta = –20 to 75℃

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
EXT Φ0	t_C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	t_W	$\overline{VCE}$ HIGH-level pulse width	t_C – 50	—	t_C – 50	—	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulse width	$2t_C$ – 30	—	$2t_C$ – 30	—	ns	
VA0 to VA15	t_{CYW}	Write cycle time	3tC	—	$3t_C$	—	ns	
	t_{AHC}	Address hold time from falling edge of $\overline{VCE}$	$2t_C$ – 30	—	$2t_C$ – 40	—	ns	
	t_{ASC}	Address setup time to falling edge of $\overline{VCE}$	t_C – 70	—	t_C – 110	—	ns	
	t_{CA}	Address hold time from rising edge of $\overline{VCE}$	0	—	0	—	ns	
	t_{AS}	Address setup time to falling edge of $\overline{VWR}$	0	—	0	—	ns	
	t_{AH2}	Address hold time from rising edge of $\overline{VWR}$	10	—	10	—	ns	
$\overline{VWR}$	t_{WSC}	Write setup time to falling edge of $\overline{VCE}$	t_C – 80	—	t_C – 115	—	ns	
	t_{WHC}	Write hold time from falling edge of $\overline{VCE}$	$2t_C$ – 20	—	$2t_C$ – 20	—	ns	
VD0 to VD7	t_{DSC}	Data input setup time to falling edge of $\overline{VCE}$	t_C – 85	—	t_C – 125	—	ns	
	t_{DHC}	Data input hold time from falling edge of $\overline{VCE}$	$2t_C$ – 30	—	$2t_C$ – 30	—	ns	
	t_{DH2}	Data hold time from rising edge of $\overline{VWR}$	5	50	5	50	ns	

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

5.3 Read Mode

10-3-3 Display Memory Read Timing



Ta = –20 to 75℃

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
EXT Φ0	t_C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	t_W	$\overline{VCE}$ HIGH-level pulse width	t_C – 50	—	t_C – 50	—	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulse width	2t_C – 30	—	2 t_C – 30	—	ns	
VA0 to VA15	t_{CYR}	Read cycle time	3t_C	—	3t_C	—	ns	
	t_{ASC}	Address setup time to falling edge of $\overline{VCE}$	t_C – 70	—	t_C – 100	—	ns	
	t_{AHC}	Address hold time from falling edge of $\overline{VCE}$	2 t_C – 30	—	2t_C – 40	—	ns	
$\overline{VRD}$	t_{RCS}	Read cycle setup time to falling edge of $\overline{VCE}$	t_C – 45	—	t_C – 60	—	ns	
	t_{RCH}	Read cycle hold time from rising edge of $\overline{VCE}$	0.5t_C	—	0.5t_C	—	ns	
VD0 to VD7	t_{ACV}	Address access time	—	3t_C – 100	—	3t_C – 115	Ns	
	t_{CEA}	$\overline{VCE}$ access time	—	2t_C – 80	—	2t_C – 90	Ns	
	t_{OH2}	Output data hold time	0	—	0	—	ns	
	t_{CE3}	$\overline{VCE}$ to data off time	0	—	0	—	ns	

6. Instruction Table

Table-1: Command Set

Class	Command	Code											Hex	Command Description	Command Read Parameters	
		RD	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0			No. of Bytes	Section
System Control	SYSTEM SET	1	0	1	0	1	0	0	0	0	0	0	40	Initialize device and display	8	9-2-1
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enter standby mode	0	9-2-2
Display Control	DISPLAY ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58, 59	Enable and disable display and display flashing	1	9-3-1
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and display regions	10	9-3-2
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor type	2	9-3-3
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start address of character generator RAM	2	9-3-6
	CSRDIR	1	0	1	0	1	0	0	1	1	CD 1	CD 0	4C to 4F	Set direction of cursor movement	0	9-3-4
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position	1	9-3-7
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format	1	9-3-5
Drawing Control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address	2	9-r1
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor address	2	9-4-2
Memory Control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory	—	9-5-1
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory	—	9-5-2

Notes:

1. In general, the internal registers of the RA8835 series are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged. 2-byte parameters (where two bytes are treated as 1 data item) are handled as follows:

   a. CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.

   b. SYSTEM SET, SCROLL, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.

2. APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.

7. Reliability Specification

7.1 Contents of Reliability Tests

No.	Test Item	Content of Test	Test Condition
1	High Temperature Storage	Endurance test applying the high storage temperature for a long time	+80°C 96H
2	Low Temperature Storage	Endurance test applying the low storage temperature for a long time	−30°C 96H
3	High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the thermal stress to the element for a long time	+70°C 96H
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time	−20°C 96H
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and humidity storage for a long time	40°C 90%RH 96H
6	Temperature Cycle	Endurance test applying the low and high temperature cycle −20°C ⟷ 25°C ⟷ 70°C ⟷ 25°C 30min 5min 30min 5min ⟷ 1 cycle	−20°C/70°C 10 cycles
7	Vibration Test (Package State)	Endurance test applying the vibration during transportation	10Hz－55Hz, 50m/s,15min
8	Shock Test (Package State)	Endurance test applying the shock during transportation	Half-sinewave, 100m/s, 11ms
9	Atmospheric Pressure Test	Endurance test applying the atmospheric pressure during transportation by air	40 kPa 16 H

7.2 Life Time

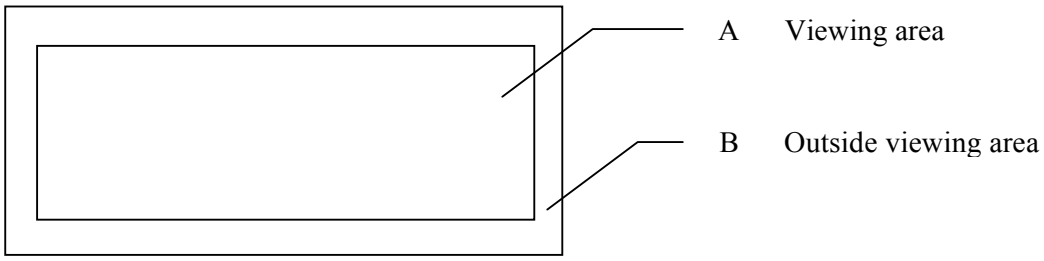
Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions of room temperature (25±10°C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.

*** Note: Test Condition**

1) Temperature and humidity: If no specification, Temperature set at 25±2°C, Humidity set at 60±5%RH;
2) Operating state: Samples subject to the tests shall be in " Operating " condition.

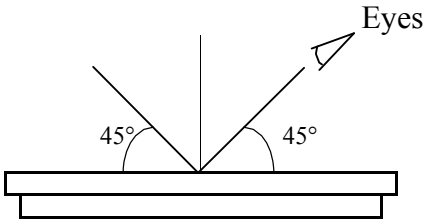
8. Quality Level

8.1 Zone Definition



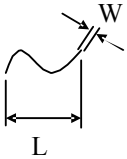
8.2 Visual Inspection

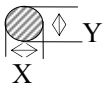
1) Inspect under 2x20W or 40W fluorescent lamp (approximately 3000 lux) leaving 25 to 30 cm between the module and the lamp and 30 cm between the module and the eye (measuring position).
2) Appearance is inspected at the best contrast voltage (best contrast is adjusted considering clearness and crosstalk on screen).
3) Inspect the module at 45° right and left, top and bottom.
4) Use the optimum viewing angle during the contrast inspection.

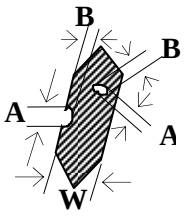


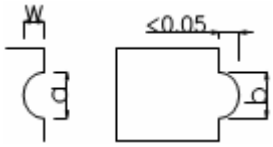
8.3 Standard of Apperance Inspection

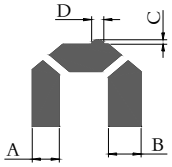
<table>
<tr><th>No.</th><th>Item</th><th>Criteria</th></tr>
<tr><td>1</td><td>Black spot
White spot
Dust</td><td>
Round type: as per following drawing
Φ = (X+Y)/2

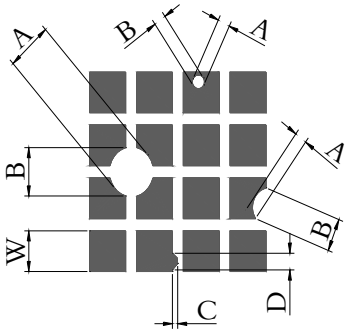
X
<table>
<tr><th colspan="3">Acceptable quantity</th></tr>
<tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr>
<tr><td>Φ <0.1</td><td>Any number</td><td rowspan="4">Any number</td></tr>
<tr><td>0.1< Φ <0.2</td><td>2</td></tr>
<tr><td>0.2< Φ <0.25</td><td>1</td></tr>
<tr><td>0.25< Φ</td><td>0</td></tr>
</table>
Line type: as per following drawing

W
L
<table>
<tr><th colspan="4">Acceptable quantity</th></tr>
<tr><th>Length</th><th>Width</th><th>Zone A</th><th>Zone B</th></tr>
<tr><td>—</td><td>W≤0.02</td><td>Any number</td><td rowspan="4">Any number</td></tr>
<tr><td>L≤3.0</td><td>0.02<W≤0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≤2.5</td><td>0.03<W≤0.05</td></tr>
<tr><td>—</td><td>0.05<W</td><td>As round type</td></tr>
</table>
Total acceptable quantity: 3
</td></tr>
</table>

<table>
<tr><td>2</td><td>Polariser scratch</td><td>Scratch on protective film is permitted
Scratch on polariser: same as No. 1</td></tr>
<tr><td>3</td><td>Polariser bubble</td><td>Φ = (X+Y)/2
 

<table>
<tr><td colspan="3">Acceptable quantity</td></tr>
<tr><td>Size</td><td>Zone A</td><td>Zone B</td></tr>
<tr><td>Φ <0.2</td><td>Any number</td><td rowspan="4">Any number</td></tr>
<tr><td>0.2< Φ <0.5</td><td>2</td></tr>
<tr><td>0.5< Φ <1.0</td><td>1</td></tr>
<tr><td>1.0< Φ</td><td>0</td></tr>
</table>
Total acceptable quantity: 3</td></tr>
<tr><td>4</td><td>Segment deformation</td><td>4.1 Pin hole on segmented display
W: segment width
Φ = (A+B)/2
 

<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Width</td><td>Quantity</td></tr>
<tr><td>W≤0.4</td><td>Φ ≤0.2 and Φ ≤1/2W</td></tr>
<tr><td>W>0.4</td><td>Φ ≤0.25 and
Φ ≤1/3W</td></tr>
<tr><td colspan="2">Total acceptable quantity: 1 defect per segment
Pin holes with Φ under 0.10 mm are acceptable</td></tr>
</table>
4.2 Pin hole on dot matrix display
 

<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>a, b<0.1</td><td>Any number</td></tr>
<tr><td>(a+b)/2≤0.1</td><td>Any number</td></tr>
<tr><td>0.5< Φ <1.0</td><td>3</td></tr>
</table>
Total acceptable quantity: 7
4.3 Segments / dots with different width
 

<table>
<tr><td colspan="2">Acceptable</td></tr>
<tr><td>a≥b</td><td>a/b≤4/3</td></tr>
<tr><td>a<b</td><td>a/b>4/3</td></tr>
</table>
4.4 Alignment layer defect
Φ = (A+B)/2
 

<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>Φ ≤0.4</td><td>Any number</td></tr>
<tr><td>0.4< Φ ≤1.0</td><td>5</td></tr>
<tr><td>1.0< Φ ≤1.5</td><td>3</td></tr>
<tr><td>1.5< Φ ≤2.0</td><td>2</td></tr>
</table>
Total acceptable quantity: 7</td></tr>
<tr><td>5</td><td>Colour uniformity</td><td>Level of sample for approval set as limit sample</td></tr>
</table>

<table>
<tr><td>6</td><td>Backlight</td><td>The backlight colour should correspond to the product specification
Flashing and or unlit backlight is not allowed
Dust larger than 0.25 mm is not allowed</td></tr>
<tr><td>7</td><td>COB</td><td>Exposed wire bond pad is not allowed
Insufficient covering with resin is not allowed (wire bond line exposed) Dust or bubble on the resin are not allowed</td></tr>
<tr><td>8</td><td>PCB</td><td>No unmelted solder paste should be present on PCB
Cold solder joints, missing solder connections, or oxidation are not allowed
No residue or solder balls on PCB are allowed
Short circuits on components are not allowed</td></tr>
<tr><td>9</td><td>Tray particles</td><td>
<table>
<tr><td colspan="3">Acceptable quantity</td></tr>
<tr><td></td><td>Size</td><td>Quantity</td></tr>
<tr><td rowspan="2">On tray</td><td>Φ <0.2</td><td>Any number</td></tr>
<tr><td>Φ >0.25</td><td>4</td></tr>
<tr><td rowspan="2">On display</td><td>Φ ≥0.25</td><td>2</td></tr>
<tr><td>L = 3</td><td>1</td></tr>
</table>
</td></tr>
</table>

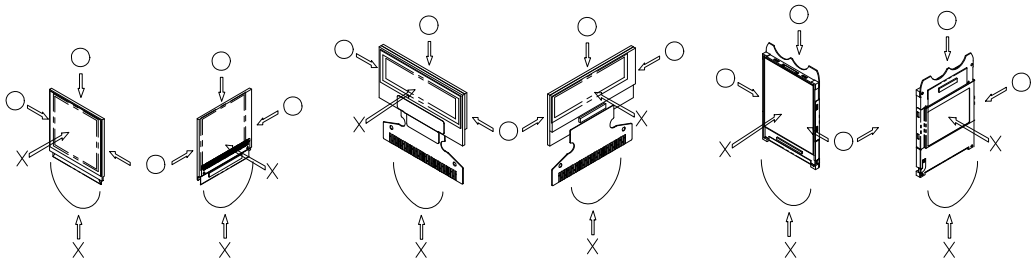
9. Package Specifications

T.B.D.

10. Percautions When Using These LCD Modules

10.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the LCD Module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the LCD Module is soft and easily scratched. Please be careful when handling the LCD Module.
5) When the surface of the polarizer of the LCD Module has soil, clean the surface. It takes dvantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent.
   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold LCD Module very carefully when palcing LCD Module into the system housing. Do not apply excessive stress or pressure to LCD Module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the LCD Module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing LCD Modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling LCD Modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the LCD Module. Be careful since static electricity may be generated when exfoliating the

protective film.
* Protective film is being applied to the surface of the display panel of the LCD Module. Be careful since static electricity may be generated when exfoliating the protective film

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the LCD Module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the LCD Module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

10.2 Storage Precautions

1) When storing LCD Modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Blaze Display Technology Co., Ltd.)
At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the LCD Module, when the LCD Module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

10.3 Designing Precautions

1) The absolute maximum ratings are the ratings which can not be exceeded for LCD Module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
5) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
6) As for EMI, take necessary measures on the equipment side basically.
When fastening the LCD Module, fasten the external plastic housing section.
7) If power supply to the LCD Module is forcibly shut down by such errors as taking out the main battery while the LCD Panel is in operation, we cannot guarantee the quality of this LCD Module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows:
* Connection (contact) to any other potential than the above may lead to rupture of the IC.

10.4 Precautions When Disposing of the LCD Modules

Request the qualified companies to handle industrial wastes when disposing of the LCD Modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

10.5 Other Precautions

1) When a LCD Module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module
2) To protect LCD Modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the LCD Modules.
   * Pins and electrodes
   * Pattern layouts such as the TCP & FPC
3) With this LCD Module, the LCD Module driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this LCD Module driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the LCD Module driver may be shielded from light in actual usage.
   * Design the product and installation method so that the LCD Module driver may be shielded from light during the inspection processes.
4) Although this LCD Module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.