CM210 Pin Definition

Ver 0.1

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www.armdesigner.com

Rev	Date	Description
V0.1	2012-01-17	Initial version

1. Introduction

1.1. About this Manual

This manual is intended to provide the user with an overview of the board and benefits, complete features specifications, and set up procedures. It contains important safety information as well.

1.2. Feedback and Update to this Manual

To help our customers make the most of our products, we are continually making additional and updated resources available on the Boardcon website (www.armdesigner.com).

These include manuals, application notes, programming examples, and updated software and hardware. Check in periodically to see what's new!

When we are prioritizing work on these updated resources, feedback from customers is the number one influence, If you have questions, comments, or concerns about your product or project, please no hesitate to contact us at support@armdesigner.com.

1.3. Limited Warranty

Boardcon warrants this product to be free of defects in material and workmanship for a period of one year from date of buy. During this warranty period Boardcon will repair or replace the defective unit in accordance with the following process:

A copy of the original invoice must be included when returning the defective unit to Boardcon. This limited warranty does not cover damages resulting from lighting or other power surges, misuse, abuse, abnormal conditions of operation, or attempts to alter or modify the function of the product.

This warranty is limited to the repair or replacement of the defective unit .In no event shall Boardcon be liable or responsible for any loss or damages, including but not limited to any lost profits, incidental or consequential damages, loss of business, or anticipatory profits arising from the use or inability to use this products.

Repairs make after the expiration of the warranty period are subject to a repair charge and the cost of return shipping. Please contact Boardcon to arrange for any repair service and to obtain repair charge information.

Catalogue

1 Pin Definition

1.1 Pin Definition of J2A

Pin Definition of J2A			
Pin	Signal	Pin	Signal
1	**GND**	19	**MMC0_D1**
2	**GND**	20	**MMC0_D2**
3	**DC_IN**	21	**MMC0_D3**
4	**DC_IN**	22	**MMC0_CLK**
5	**VDD_IO**	23	**MMC0_CMD**
6	**VDD_IO**	24	**MMC0_CDn**
7	**VDD_RTC**	25	**EINT7**
8	**EINT9**	26	**MMC1_D0**
9	**OTG_ID**	27	**MMC1_D1**
10	**OTG_DP**	28	**MMC1_D2**
11	**OTG_DM**	29	**MMC1_D3**
12	**VBUS**	30	**MMC1_CLK**
13	**OTG_DRVVBUS**	31	**MMC1_CMD**
14	**HOST_DP**	32	**MMC1_CDn**
15	**HOST_DN**	33	**EINT8**
16	**EINT11**	34	**MMC2_D0**
17	**EINT12**	35	**MMC2_D1**
18	**MMC0_D0**	36	**MMC2_D2**

1.2 Pin Definition of J2B

Pin Definition of J2B			
Pin	Signal	Pin	Signal
37	**MMC2_D3**	55	**HDMI_TX2P**
38	**MMC2_CLK**	56	**HDMI_TX1N**
39	**MMC2_CMD**	57	**HDMI_TX1P**
40	**MMC2_CDn**	58	**HDMI_TX0N**
41	**EINT13**	59	**HDMI_TX0P**
42	**EINT14**	60	**HDMI_TXCN**
43	**EINT15**	61	**HDMI_TXCP**
44	**TSXM1**	62	**VD0**
45	**TSXP1**	63	**VD1**
46	**TSYM1**	64	**VD2**
47	**TSYP1**	65	**VD3**
48	**EINT16**	66	**VD4**
49	**EINT17**	67	**VD5**
50	**EINT18**	68	**VD6**
51	**EINT19**	69	**VD7**
52	**EINT20**	70	**VD8**
53	**EINT21**	71	**VD9**
54	**HDMI_TX2N**	72	**VD10**

1.3 Pin Definition of J2C

Pin Definition of J2C			
Pin	Signal	Pin	Signal
73	**VD11**	91	**EINT22**
74	**VD12**	92	**EINT23**
75	**VD13**	93	**DAC_OUT0**
76	**VD14**	94	**EINT24**
77	**VD15**	95	**EINT25**
78	**VD16**	96	**AC97_SYNC/i2sLRCK1**
79	**VD17**	97	**AC97_BITCLK/i2sSCLK1**
80	**VD18**	98	**AC97_SDI/i2sSDI1**
81	**VD19**	99	**AC97_SDO/i2sSDO1**
82	**VD20**	100	**AC97_RSTn/i2sCDCLK1**
83	**VD21**	101	**EINT26**
84	**VD22**	102	**EINT27**
85	**VD23**	103	**TXD1**
86	**VSYNC**	104	**RXD1**
87	**HSYNC**	105	**TXD0**
88	**VCLK**	106	**RXD0**
89	**VDEN**	107	**SPI0_MOSI**
90	**PWMTOUT0**	108	**SPI0_MISO**

1.4 Pin Definition of J2D

Pin Definition of J2D			
Pin	Signal	Pin	Signal
109	**SPI0_CLK**	127	**CAM_VSYNC**
110	**SPI0_CSn**	128	**CAM_HREF**
111	**EINT28**	129	**CAM_FIELD**
112	**EINT29**	130	**I2C_SDA1**
113	**EINT30**	131	**I2C_SCL1**
114	**EINT31**	132	**EINT10**
115	**EINT0**	133	**EINT2**
116	**EINT1**	134	**OM5**
117	**CAM_D7**	135	**OM3**
118	**CAM_D6**	136	**OM2**
119	**CAM_D5**	137	**OM1**
120	**CAM_D4**	138	**EINT3**
121	**CAM_D3**	139	**EINT4**
122	**CAM_D2**	140	**EINT5**
123	**CAM_D1**	141	**KEY_RST**
124	**CAM_D0**	142	**EINT6**
125	**CAM_PCLK**	143	**ADCIN1**
126	**CAM_CLKOUT**	144	**ADCIN0**

2 Pin Signal

2.1 Details of the pin signal

Signal	Pin	Description	IO Initial state	IO Type	Working voltage	Pin Multiplying Function	I/O	Function
Power	1-2	GND	\	P	\	GND	\	GND
	3-4	DC_IN	I	P	3.3	DC_IN	I	Power Input
	5-6	VDD_IO	I	P	3.3	VDD_IO	I	IO
	7	VDD_RTC	I	P	3	VDD_RTC	I	RTC
Interrupt	8	EINT9	I	hag_a	1.8-3.3	EINT9	I	Interrupt
						GPH1_1	IO	GPIO
USB	9	OTG_ID	AI	htr	1.8-3.3	OTGID	I	USB Identifier
	10	OTG_DP	AI	htr	1.8-3.3	OTGDP	IO	USB Differential data (+)
	11	OTG_DM	AI	htr	1.8-3.3	OTGDM	IO	USB Differential data (-)
	12	VBUS	AI	htr	5	VBUS	O	USB BUS power input
	13	OTG_DRVVBUS	O(L)	hag	1.8-3.3	USBDRVBUS	O	OTG Power control pin
	14	HOST_DP	AI	usbl	\	uhDP	IO	USB HOST Differential data (+)
	15	HOST_DN	AI	usbl	\	uhDN	IO	USB HOST Differential data (-)
Interrupt	16	EINT11	I	hag_a	1.8-3.3	EINT11	I	Interrupt
						GPH1_3	IO	GPIO
	17	EINT12		hag_		EINT12	I	Interrupt

				a	1.8-3.3			
						GPH1_4	IO	GPIO
MMC0	18-21	MMC0_DATA [0:3]	I	hag	1.8-3.3	mmc0DAT[0:3]	IO	MMC0 Data
						GPG0_[3:6]	IO	GPIO
	22	MMC0_CLK	I	hag	1.8-3.3	mmc0CLK	IO	MMC0 Clock signal
						GPG0_0_	IO	GPIO
	23	MMC0_CMD	O	hag	1.8-3.3	mmc0CMD	IO	MMC0_CMD
						GPG0_1	IO	GPIO
	24	MMC0_CDn	I	hag	1.8-3.3	mmc0CDn	I	MMC0 Inquiry
						GPG0_2	IO	GPIO
	25	EINT7	I	hag_a	1.8-3.3	EINT7	I	Interrupt
						GPH0_7	IO	GPIO
MMC1	26-29	MMC1_DATA [0:3]	I	hag	1.8-3.3	mmc1DAT[0:3]	IO	MMC0 Data
						GPG1_[3:6]	IO	GPIO
	30	MMC1_CLK	I	hag	1.8-3.3	mmc1CLK	IO	MMC1 Clock signal
						GPG1_0	IO	GPIO
	31	MMC1_CMD	I	hag	1.8-3.3	mmc1CMD	IO	MMC1_CMD
						GPG1_1	IO	GPIO
	32	MMC1_CDn	O	hag	1.8-3.3	mmc1CDn	IO	MMC1 Inquiry
						GPG1_2	IO	GPIO
Interrupt	33	EINT8	I	hag_a	1.8-3.3	EINT8	I	Interrupt
						GPH1_0	IO	GPIO
MMC2	34-37	MMC2_DATA [0:3]	I	hag	1.8-3.3	mmcDAT1[0:3]	IO	MMC Data
						GPG2_[3:6]	IO	GPIO
	38	MMC2_CLK	I	hag	1.8-3.3	mmc2CLK	IO	MMC2 Clock signal
						GPG2_0	IO	GPIO
	39	MMC2_CMD	I	hag	1.8-3.3	mmc2CMD	IO	MMC2_CMD
						GPG2_1	IO	GPIO
	40	MMC2_CDn	I	hag_a	1.8-3.3	mmc2CDn	IO	MMC2 Inquiry
						GPG2_2	IO	GPIO
Interrupt	41-43	EINT[13:15]	I	hag_a	1.8-3.3	EINT[13:15]	I	Interrupt
						GPH1_[5:7]	IO	GPIO
ADC	44	TSXM1	AI	hr	1.8-3.3	adc_AIN8	AI	ADC Data input
	45	TSXP1	AI	hr	1.8-3.3	adc_AIN9	AI	

	46	TSYM1	AI	hr	1.8-3.3	adc_AIN6	AI	
	47	TSYP1	AI	hr	1.8-3.3	adc_AIN7	AI	
Interrupt	48-53	EINT[16:21]	I	hag_a	1.8-3.3	EINT[16:21]	I	Interrupt
						GPH2_[0:5]	IO	GPIO
HDMI	54	HDMI_TX2N	O	hag	1.8-3.3			
	55	HDMI_TX2P	O	hag	1.8-3.3			
	56	HDMI_TX1N	O	hag	1.8-3.3			
	57	HDMI_TX1P	O	hag	1.8-3.3			
	58	HDMI_TX0N	O	hag	1.8-3.3			
	59	HDMI_TX0P	O	hag	1.8-3.3			
	60	HDMI_TXCN	O	hag	1.8-3.3			
	61	HDMI_TXCP	O	hag	1.8-3.3			
LCD	62-85	VD[0:23]	I	hag_a	1.8-3.3	VD[0:23]	O	RGB Interface data
						GPF0_[4:7],GPF1_[0:7],GPF2_[0:7],GPF3_[0:3]	IO	GPIO
	86	VSYNC	I	hag_a	1.8-3.3	VSYNC	O	RGB Field Sync
						GPF0_0	IO	GPIO
	87	HSYNC	I	hag_a	1.8-3.3	HSYNC	O	RGB Line Sync
						GPF0_1	IO	GPIO
	88	VCLK	I	hag_a	1.8-3.3	VCLK	O	RGB Pixel clock
						GPF0_3	IO	GPIO
	89	VDEN	I	hag_a	1.8-3.3	VDEN	O	RGB Data enable
						GPF0_2	IO	GPIO
PWM[0]	90	PWMTOUT0	I	hag	1.8-3.3	pwmTOUT[0]	O	PWM Output
						GPD0_0	IO	GPIO
Interrupt	91-92	EINT[22:23]	I	hag_a	1.8-3.3	EINT[22:23]	I	Interrupt
						GPH2_[6:7]	IO	GPIO
DAC	93	DAC_OUT0	A0	hr	1.8-3.3	dacOUT[0]	A0	DAC Analog output
Interrupt	94-95	EINT[24:25]	I	hag_a	1.8-3.3	EINT[24:25]	I	Interrupt
						GPH3_[0:1]	IO	GPIO
Audio	96	AC97_SYNC	I	hag	1.8-3.3	AC97SYNC	O	AC97 Sync signal
						i2sLRCLK[]1	IO	I2S Left /right channel selection clock
						GPC0_2	IO	GPIO
	97	AC97_BITCLK	I	hag	1.8-3.3	AC97BITCLK	I	AC97 Bit clock
						i2sSCLK[1]	IO	I2S Serial clock

						GPC0_0	IO	GPIO
	98	AC97_SDI	I	hag	1.8-3.3	AC97SDI	I	AC97 Serial data input
						i2sSDI[1]	I	I2S Serial data input
						GPC0_3	IO	GPIO
	99	AC97_SDO	O	hag	1.8-3.3	AC97SDO	O	AC97 Serial data output
						i2sSDO[1]	O	I2S Serial data output
						GPC0_4	IO	GPIO
	100	AC97_RSTn	I	hag	1.8-3.3	AC97RESETn	O	AC97 Reset signal
						i2sCDCLK1	O	I2S Codec system clock
						GPC0_1	IO	GPIO
Interrupt	101-102	EINT[26:27]	I	hag_a	1.3-3.3	EINT[26:27]	I	Interrupt
						GPH3_[2:3]	IO	GPIO
UART1	103	TXD1	O	hag	1.8-3.3	TXD[1]	O	UART1 Sending data output
						GPA0_5	IO	GPIO
	104	RXD1	I	hag	1.8-3.3	RXD[1]	I	UART1 Receiving data input
						GPA0_4	IO	GPIO
UART0	105	TXD0	O	hag	1.8-3.3	TXD[0]	O	UART0 Sending Data output
						GPA0_1	IO	GPIO
	106	RXD0	I	hag	1.8-3.3	RXD[0]	I	UART0 Receiving Data input
						GPA0_0	IO	GPIO
SPI	107	SPI0_MOSI	I	hag	1.8-3.3	spiMOSI[0]	O	SPI0 Output(Host) / Input(Device)
						GPB2	IO	GPIO
	108	SPI0_MISO	I	hag	1.8-3.3	spiMISO[0]	O	SPI[0] SPI0 Input (Host) / Output (Device)
						GPB3	IO	GPIO
	109	SPI0_CLK	I	hag	1.8-3.3	spiCLK[0]	O	SPI[0] Clock
						GPB0	IO	GPIO
	110	SPI0_CSn	O	hag	1.8-3.3	spiCSn[0]	I	SPI[0] Chip Select
						GPB1	IO	GPIO
Interrupt	111-116	EINT{[23:31][0:1]}	I	hag	1.8-3.3	EINT{[23:31],[0:1]}	I	Interrupt
						GPH2_7,GPH3_[0:7],GPH0_[0:1]	IO	GPIO
Camera	117-1	CAM_D[7:0]	O	hag	1.8-3.3	CAMDATA[0:	I	Camera data

	24					7]		
						GPE0_[3:7]GPE1_[0:2],	IO	GPIO
	125	CAM_PCLK	I	hag	1.8-3.3	CAMPCLK	I	Camera dot clock
						GPE0_0	IO	GPIO
	126	CAM_CLKOUT	I	hag	1.8-3.3	CAMCLK	O	Camera main clock
						GPE1_3	IO	GPIO
	127	CAM_VSYNC	O	hag	1.8-3.3	CAMVSYNC	O	Field sync
						GPE0_1	IO	GPIO
	128	CAM_HREF	O	hag	1.8-3.3	CAMHREF	O	Line sync
						GPE0_2	IO	GPIO
	129	CAM_FIELD	O	hag	1.8-3.3	CAMFIELD	O	
						GPE1_4	IO	GPIO
I2C	130	I2C_SDA[1]	O	hag	1.8-3.3	i2cSDAT[1]	O	I2C[1] Data
						GPD1_2	IO	GPIO
	131	I2C_SCL1	I	hag	1.8-3.3	i2cSCL[1]	O	I2C[1]Clock
						GPD1_3	IO	GPIO
Interrupt	132	EINT10	I	hag	1.8-3.3	EINT10	I	Interrupt
						GPH1_2	IO	GPIO
Interrupt	133	EITN2	I	hag	1.8-3.3	EINT2	I	Interrupt
						GPH0_2	IO	GPIO
Booting Mode	134-137	OM[5,3:1]	I	hag	1.8-3.3	OM[5,3:1]	I	Booting Mode setting
Interrupt	138-140	EINT[3:5]	I	hag	1.8-3.3	EINT[3:5]	I	Interrupt
						GPH0_[3:5]	IO	GPIO
Reset	141	KEY_RST	I	hag	1.8-3.3	XnRESET	I	External reset signal input
Interrupt	142	EINT6	I	hag	1.8-3.3	EINT6	I	Interrupt
						GPH0_6	IO	GPIO
ADC	143-144	ADCIN[1:0]	I	hag	1.8-3.3	XadcAIN[0:1]	I	AD converter analog input

Notice:

IO Types defined：

hag: 1.8～3.3V wide range of bi-directional buffer with Schmitt trigger input , which can be configured resistor with up / down pull and A-type output driver.

hag_a: 1.8～3.3V wide range of bi-directional buffer with Schmitt trigger input , which can be configured resistor with up / down pull and A-type output driver .

hbg: 1.8～3.3V wide range of bi-directional buffer with Schmitt trigger input , which can be configured resistor with up / down pull and B-type output driver.

dth: 1.8~3.3V for external logic

hr: 1.8V~3.3V wide range of analog two-way path

htr: 1.8V~3.3V wide range of analog tolerance two-way path
usb1: USB 1.1Pin

3 Board voltage/current instructions

Number	Power network	Voltage	Current
1	VDD_5V	5V	100mA
2	VDD_IO	3.3V	60mA
3	VDD_RTC	3V	1mA

Finish