S5PV210

RISC Microprocessor

Revision 1.10

May 2010

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User's Manual

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User's Manual, Revision 1.10

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1.00	03 04, 2010	- Initial draft	G.H.CHA
1.10	05 03 2010	- first updated	G.H.CHA

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Revision Descriptions for Revision 1.10

Chapter (Rev 1.10)		Subjects (Major changes comparing with last version)
Chapter Name	**Page**	
1. Overview	**1-2**	Block Diagram and Key feature are updated.
	1-3	"JPEG codec supports up to 80 Mpixels/s" is removed. The content is indefinite.
	1-7	Maximum size of JPEG Compression/decompression is changed from 65536x65536 to 8192x8192
2. System	**1-2**	Add description about "Device ID" bit field
	3-2	3.2.1 Added a description for recommending using 24MHz crystal as XXTI/XUSBXTI input.
	3-2	3.2.1 Modified HDMI part of Figure 3-2
	3-3	3.2.2 Added a description for HDMI PHY
	3-4	3.3 Modified descriptions some points
	3-5	3.3.1 Modified the recommended PMS values for 800MHz, 1GHz from (6,200,1) (6, 250,1) to (3,100,1) (3,125,1)
	3-9	3.4 Modified Figure 3-3 to add the USB HOST PHY input and output clock.
	3-10	3.4 Added the "caution" for using glitch free mux.
	3-12	3.5 Removed the description for PLL turn off and added a description as "Once you turned on any PLL, do not turn off that".
	3-13	3.6.1 Added the frequency range of special clocks and modified Table 3-7.
	3-19	3.7.2.1 Added lock time setting guide for PLLs.
	3-25	3.7.2.4 Modified usable range of Fref . 1MHz ≤ Fref ≤ 10MHz
	3-35	3.7.4 Modified max. operating freq. of SCLKAPLL from 800MHz to 1GHz.
	3-40	3.7.5.2 CLK_JPEG[28] in CLK_GATE_IP0 is modified to reserved region (CLK_JPEG -> Reserved)
	3-52/53	3.7.6.1 Modified register descriptions and Figure 3-4 for better understanding.
	ALL	* Globally deleted descriptions for SPI2 and HOST IF
	4-5/6	4.3.1 Modified Table 4-3 for better understanding and missing points of sub-blocks, audio block, top block and wakeup time. Also, wakeup time is

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Chapter (Rev 1.10)		Subjects (Major changes comparing with last version)
Chapter Name	Page	
		calculated based on 24Mhz input clock.
	4-7	4.3.2 Removed max. 100us lock time, miss printing.
	4-16	4.4 Removed a Figure - Internal Operation During Power Mode Transition that might lead to confusion.
	4-17	4.4.1 Modified wakerup source of DeepIdle mode with TOP block on as all interrupt source.
	4-24	4.7 Modified ADC power in sleep mode as "power-on".
	4-26	4.7.4 Modified some description of PLL for better understanding.
	4-27	4.7.4.1 Modified the clock status after wakeup for each low power mode of Table 4-8.
	4-32/33	4.9.2 Modified power on/off and sleep mode enter/exit sequence for better understanding.
	4-36	4.9.2 Modified initializing condition of inform registers by several resets. Inform 4~6 are reset by only alive POR. Inform 0~3 are reset by WDT reset, XnReset and alive POR.
	4-41	4.10.4.1 Modified CFG_STANDBYWFI description of PWR_CFG (00 : IDLE mode, 01 : DEEPIDLE mode, 10 : STOP/DEEPSTOP mode)
	4-41	4.10.4 Removed PWR_MODE register because the need.
	4-47/48	4.10.4.9/10/11/12/13 Added descriptions to calculate time and example for OSC_FREQ, OSC_STABLE, PWR_STABLE, CLAMP_STABLE, MTC_STABLE.
	4-53	4.10.5.4 Added descriptions for USB PHY0(=OTG device), USB PHY1(=HOST).
3. Address Space	**3-2**	Read-only area (0x003FFD00 ~ 0x003FFDFF) is renamed to Security Area.
4. Boot Loader	**4-3**	The bit properties for all OPRSEL register bits are corrected from 'R/W' to 'W'.
		Bit description for OPRSEL register is modified for better understandings.
		Note 4 is added: User must set both OPRSEL[1] and OPRSEL[3] at the same time.
	4-4	Bit description for OPRMON register is modified for better understandings.

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	4-5	The first step of Note is changed from: Set one bit which user would like to change in OPRSEL register Is now to read: Set one bit for OPRSEL[0]/OPRSEL[2] or two bits for OPRSEL[1]/OPRSEL[3] which user would like to change in OPRSEL register.
5. Memory	**1-1**	Introduction of DRAM Controller is added.
	1-19	I/O Description is modified.
	1-20	PAD Mux for Address Configuration are modified.
	1-40	Removed the comment -'t_wtr must be 0x1 in case of JEDEC LPDDR.' Removed the comment -'t_rtp must be 0x1 in case of JEDEC LPDDR.'
	4-26	Conversion code changes are added.
	4-27	MainMetaSel is added.
8. connectivity_storage	**4-10**	• [8:4] field of INSNREG06 register is revised
	5-39	• [23] field of GINTSTS register is changed to reserved
	5-43	• [23] field of GINTMSK register is changed to reserved
9. multimedia	**13-1**	• The previous "Supports up to 250 MHz core clock" sentence is modified to "Supports up to 222 MHz core clock".
12. Etc	**12-26**	• SDMMC I/F electrical spec (Figure 12-14 & Table 12-14) is changed.

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Chapter (Rev 1.10)		Subjects (Major changes comparing with last version)
Chapter Name	**Page**	
	1-2	• Absolute electrical spec (Table 12-1) is changed.
	1-5	• Caution of DVFS is added.
9. MULTIMEDIA	**2-8**	• Caution is deleted.
	2-67	• In InFlipMd[14:13], 'Note' is added.
	2-22~28	• Notes are deleted in REGISTER MAP, new note is added in front of CISRCFMTn
	2-81~82	• CIEXTENn[19:0] are updated
	3-10 **3-21** **3-23** **3-24** **3-25**	• T4 ≥ 0 clock cycle. • DSIM_CONFIG[4] is deleted and LaneEn[4:0] is modified in DSIM_CONFIG • From 1024 to 768 in DSIM_MDRESOL[26:16] • From 1024 to 768 in DSIM_ SDRESOL [26:16] • DSIM_INTSRC[28] is deleted and Reserved[28:26] is modified in DSIM_INTSRC
	8-24/25	• Not used SFRs are removed.
	11-2	• The diagram error was modified. In Figure 11-11 Channel coding.
	11-10	• Description of the DSTIMGSIZE & DST_XY are changed.
	13-1	• The previous "Supports up to 250 MHz core clock" sentence is modified to "Supports up to 222 MHz core clock".
	6-14 **6-14** **6-16** **6-18** **6-18**	• In ENC_MSLICE_BYTE (0xC514), name & description changed. • In RC_FRAME_RATE (0xD0D0), address is changed. • Registers (0x009C ~ 0x00E0) is added. • In HOST2RISC_ARG1(0x0034), VC9 decoding & VC1 decoding without start code is added. • In HOST2RISC_ARG1(0x0034), size of the memory is changed to 400KB. • In MFC_RISC2HOST_COMMAND (0x0044),

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Chapter Name	**Page**	
	6-19	RISC2HOST_CMD_BATCH_ENC_RET is added.
	6-20	• In RiSC2HOST_ARG1 (0x0048), Firmware memory size is changed to 400KB.
	6-21	• In INTERMEDIATE_STAGE_COUNTER (0x0064), description is changed.
	6-22~26	• 6.3.2.2 Error code table is changed. • 6.3.2.5 Buffer address of MPEG4, H263 Decoder, is changed.
	6-29	• 6.3.2.5 Buffer memory size table is changed for decoding.
	6-31	• 6.3.2.6 Buffer memory size table is changed for encoding.
	6-34	• In MFC_PROFILE (0x0830), PROFILE field description is changed.
	6-35	• In MFC_SI_CH0_INST_ID (0x2040, 0x2080), FRAME_BATCH_START is added.
	6-41	• In MFC_COMMON_SI_RG1, 2 (0x2004, 0x2008), description is changed.
	6-44	• In MFC_COMMON_SI_RG3 (0x200C) 'Note' is added.
	6-44	• In GET_FRAME_TAG_TOP & BOTTOM (0x0008, 0x000C), description is changed.
	6-64	• In PIC_TIME_TOP & BOTTOM (0x0010, 0x0014), description is changed, 'Note' is added.
	6-64	• In EXT_ENC_CONTROL (0x0028), HIERARCHICAL_P_ENABLE field is added.
	6-69	• In METADATA_ENABLE (0x0038), NUM_CONCEALED_MB_ENABLE field is added.
	6-76	• 6.5.1 SHARED MEMORY INTERFACE FOR DECODERS, – "Table 6-1 Payload in the Shared Memory" is changed. – "Figure 6-5 Shared Memory Input for Decoders" is changed. – "Figure 6-6 Shared Memory Output for Decoders" is changed. – "Figure 6-7 VC1 Parameters" is changed.
	6-79~82	
12. Etc	**12-4**	• Absolute maximum rate table be added symbol name of power.
	12-6	• In note, recommended voltage of each speed is added guarantee range of power.
	12-25	• LCD_WR_SETUP+1 -> LCD_WR_SETUP LCD_WR_ACT+1 -> LCD_WR_ACT LCD_WR_HOLD+1 -> LCD_WR_HOLD

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	1-26~28	• '1.12 camera interface ac electrical characteristic' is updated

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Section 1

OVERVIEW

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1 OVERVIEW OF S5PV210

1.1 ARCHITECTURAL OVERVIEW

S5PV210 is a 32-bit RISC cost-effective, low power, and high performance microprocessor solution for mobile phones and general applications. It integrates the ARM Cortex-A8 core, which implements the ARM architecture V7-A with supporting peripherals.

To provide optimized Hardware (H/W) performance for the 3G and 3.5G communication services, S5PV210 adopts 64-bit internal bus architecture. This includes many powerful hardware accelerators for tasks such as motion video processing, display control, and scaling. Integrated Multi Format Codec (MFC) supports encoding and decoding of MPEG-1/2/4, H.263, and H.264, and decoding of VC1. This hardware accelerator (MFC) supports real-time video conferencing and Analog TV out, HDMI for NTSC, and PAL mode.

S5PV210 has an interface to external memory that is capable of sustaining heavy memory bandwidths required in high-end communication services. The memory system has Flash/ ROM external memory ports for parallel access and DRAM port to meet high bandwidths. DRAM controller supports LPDDR1 (mobile DDR), DDR2, or LPDDR2.

Flash/ ROM port supports NAND Flash, NOR-Flash, OneNAND, SRAM, and ROM type external memory.

To reduce the total system cost and enhance the overall functionality, S5PV210 includes many hardware peripherals such as TFT 24-bit true color LCD controller, Camera Interface, MIPI DSI, CSI-2, System Manager for power management, ATA interface, four UARTs, 24-channel DMA, five Timers, General I/O Ports, three I2S, S/PDIF, three (general purpose) IIC-BUS interfaces, two HS-SPI, USB Host 2.0, USB 2.0 OTG operating at high speed (480Mbps), four SD Host and high-speed Multimedia Card Interface, and four PLLs for clock generation.

Package on Package (POP) option with MCP is available for small form factor applications.

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1.2 BLOCK DIAGRAM OF S5PV210

Figure 1-1 shows the complete block diagram of S5PV210.

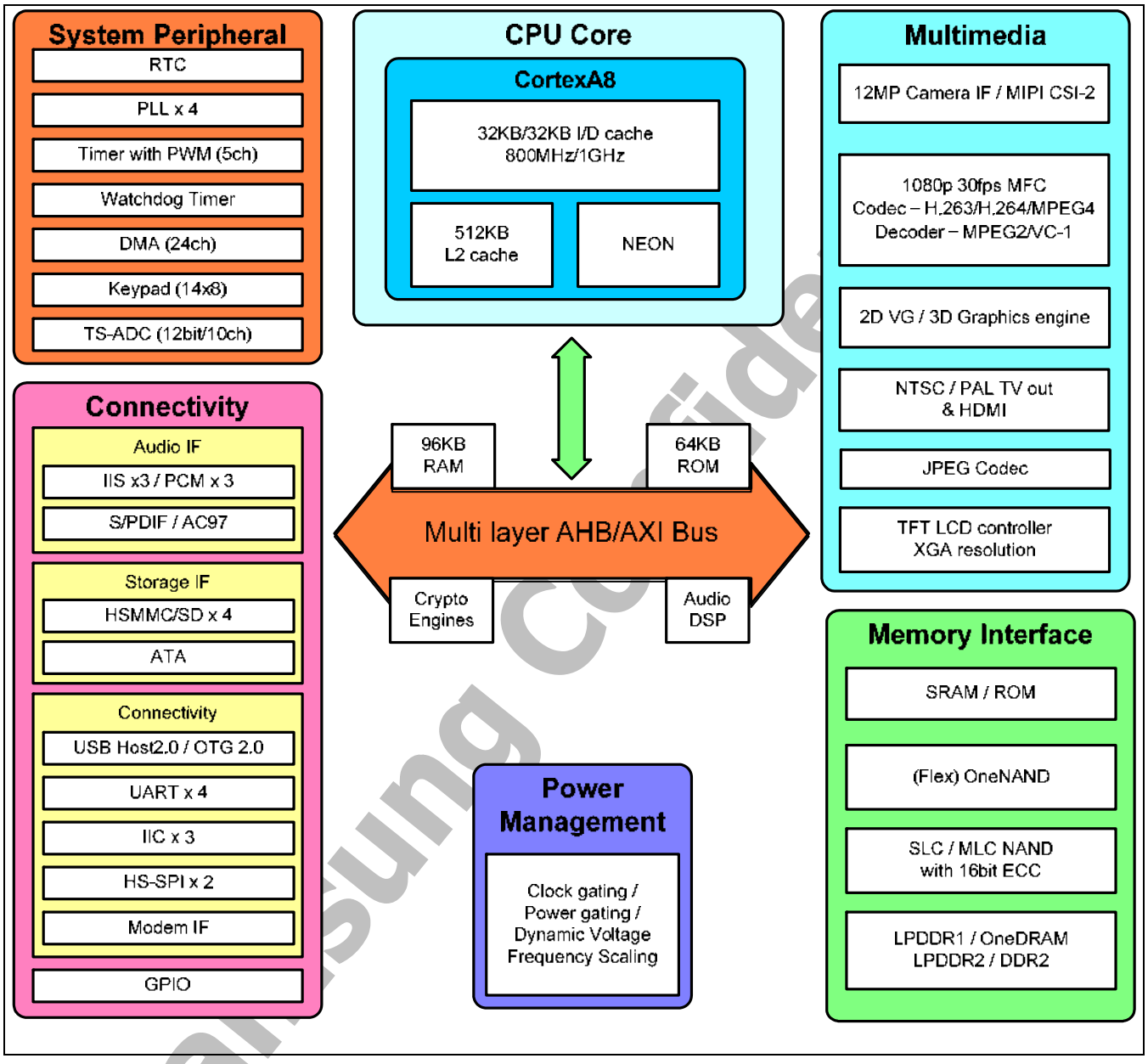

Figure 1-1 S5PV210 Block Diagram

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1.3 KEY FEATURES OF S5PV210

The key features of S5PV210 include:

- ARM CortexTM-A8 based CPU Subsystem with NEON
  - 32/ 32 KB I/D Cache, 512 KB L2 Cache
  - Operating frequency up to 800 MHz or 1 GHz
- 64-bit Multi-layer bus architecture
  - MSYS domain for ARM CortexTM-A8, 3D engine, Multi Format Codec and Interrupt Controller
- Operating frequency up to 200 MHz
  - DSYS domain mainly for Display IPs (such as LCD controller, Camera interface, and TVout), and MDMA
- Operating frequency up to 166 MHz
  - PSYS domain mainly for other system component such as system peripherals, external memory interface, peri DMAs, connectivity IPs, and Audio interfaces.
- Operating frequency up to 133 MHz
  - Audio domain for low power audio play
- Advanced power management for mobile applications
- 64 KB ROM for secure booting and 96 KB RAM for security function
- 8-bit ITU 601/656 Camera Interface supports horizontal size up to 4224 pixels for scaled and 8192 pixels for un-scaled resolution
- Multi Format Codec provides encoding and decoding of MPEG-4/H.263/H.264 up to 1080p@30fps and decoding of MPEG-2/VC1 video up to 1080p@30 fps
- 3D Graphics Acceleration with Programmable Shader up to 20M triangles/s and 1000 Mpixels/s
- 2D Graphics Acceleration up to 160Mpixels/s
- 1/ 2/ 4/ 8 bpp Palletized or 8/ 16/ 24 bpp Non-Palletized Color TFT recommend up to XGA resolution
- TV-out and HDMI interface support for NTSC and PAL mode with image enhancer
- MIPI-DSI and MIPI-CSI interface support
- One AC-97 audio codec interface and 3-channel PCM serial audio interface
- Three 24-bit I2S interface support
- One TX only S/PDIF interface support for digital audio
- Three I2C interface support
- Two SPI support
- Four UART supports three Mbps ports for Bluetooth 2.0
- On-chip USB 2.0 OTG supports high-speed (480 Mbps, on-chip transceiver)
- On-chip USB 2.0 Host support
- Asynchronous Modem Interface support
- Four SD/ SDIO/ HS-MMC interface support
- ATA/ ATAPI-6 standard interface support

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- 24-channel DMA controller (8 channels for Memory-to-memory DMA, 16 channels for Peripheral DMA)
- Supports 14x8 key matrix
- 10-channel 12-bit multiplexed ADC
- Configurable GPIOs
- Real time clock, PLL, timer with PWM and watch dog timer
- System timer support for accurate tick time in power down mode (except sleep mode)
- Memory Subsystem
  - Asynchronous SRAM/ ROM/ NOR Interface with x8 or x16 data bus
  - NAND Interface with x8 data bus
  - Muxed/ Demuxed OneNAND Interface with x16 data bus
  - LPDDR1 Interface with x16 or x32 data bus (up to 400 Mbps/ pin DDR)
  - DDR2 interface with x16 or x32 data bus (up to 400 Mbps/ pin DDR)
  - LPDDR2 interface (up to 400 Mbps/ pin DDR)

1.3.1 MICROPROCESSOR

The key features of this microprocessor include:

- The ARM CortexTM-A8 processor is the first application processor based on ARMv7 architecture.
- With the ability to scale in speed to 1 GHz, the ARM CortexTM-A8 processor meets the requirements of power-optimized mobile devices, which require operation in less than 300mW; and performance-optimized consumer applications require 2000 Dhrystone MIPS.
- Supports first superscalar processor featuring technology from ARM for enhanced code density and performance, NEONTM technology for multimedia and signal processing, and Jazelle® RCT technology for ahead-of-time and just-in-time compilation of Java and other byte code languages.
- Other features of ARM CortexTM-A8 include:
  - Thumb-2 technology for greater performance, energy efficiency, and code density
  - NEONTM signal processing extensions
  - Jazelle RCT Java-acceleration technology
  - TrustZone technology for secure transactions and DRM
  - 13-stage main integer pipeline
  - 10-stage NEONTM media pipeline
  - Integrated L2 Cache using standard compiled RAMs
  - Optimized L1 caches for performance and power

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1.3.2 MEMORY SUBSYSTEM

The key features of memory subsystem include:

- High bandwidth Memory Matrix subsystem
- Two independent external memory ports (1 x16 Static Hybrid Memory port and 2 x32 DRAM port)
- Matrix architecture increases the overall bandwidth with simultaneous access capability
  - SRAM/ ROM/ NOR Interface
    - x8 or x16 data bus
    - Address range support: 23-bit
    - Supports asynchronous interface
    - Supports byte and half-word access
  - OneNAND Interface
    - x16 data bus
    - Address range support: 16-bit
    - Supports byte and half-word access
    - Supports OneNAND and Flex OneNAND
    - Supports dedicated DMA
  - NAND Interface
    - Supports industry standard NAND interface
    - x8 data bus
  - LPDDR1 Interface
    - x32 data bus with 400 Mbps/ pin Double Data Rate (DDR)
    - 1.8V interface voltage
    - DMC0 port support up to 4 Gb and DMC1 port support up to 8 Gb
  - DDR2 Interface
    - x32 data bus with 400 Mbps/ pin double data rate (DDR)
    - 1.8V interface voltage
    - DMC0 port support up to 4 Gb and DMC1 port support up to 8 Gb
    - In case of 8 bank, only 1 CS is available in DMC 0&1
  - LPDDR2 interface
    - x32 data bus with up to 400 Mbps/pin
    - 1.2V/1.35V interface voltage
    - DMC0 port support up to 4 Gb and DMC1 port support up to 8 Gb

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1.3.3 MULTIMEDIA

The key features of multimedia include:

- Camera Interface
  - Multiple input support
    - ITU-R BT 601/656 mode
    - DMA (AXI 64-bit interface) mode
    - MIPI (CSI) mode
  - Multiple output support
    - DMA (AXI 64-bit interface) mode
    - Direct FIFO mode
  - Digital Zoom In (DZI) capability
  - Multiple camera input support
  - Programmable polarity of video sync signals
  - Input horizontal size support up to 4224 pixels for scaled and 8192 pixels for un-scaled resolution
  - Image mirror and rotation (X-axis mirror, Y-axis mirror, 90°, 180°, and 270° rotation)
  - Various image formats generation
  - Capture frame control support
  - Image effect support
- Multi-Format video Codec (MFC)
  - ITU-T H.264, ISO/IEC 14496-10
    - Decoding supports Baseline/ Main/ High Profile Level 4.0 (except Flexible Macro-block Ordering (FMO), Arbitrary Slice Ordering (ASO) and Redundant Slice (RS))
    - Encoding supports Baseline/ Main/ High Profile (except FMO, ASO, and RS)
  - ITU-T H.263 Profile level 3
    - Decoding supports Profile3, restricted up to SD resolution 30 fps (H.263 Annexes to be supported)

- Annex I: Advanced Intra Coding
- Annex J: De-blocking (in-loop) filter
- Annex K: Slice Structured Mode without FMO & ASO
- Annex T: Modified Quantization
- Annex D: Unrestricted Motion Vector Mode
- Annex F: Advanced Prediction Mode except overlapped motion compensation for luminance

    - Encoding supports Baseline Profile (supports customer size up to 1920x1088)
  - ISO/IEC 14496-2 MPEG-4
    - Decoding supports MPEG-4 Simple/ Advanced Simple Profile Level5

  - Encoding supports MPEG-4 Simple/ Advanced Simple Profile

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  - ISO/IEC 13818-2 MPEG-2
    - Decoding supports Main Profile High level
    - Decoding supports MPEG-1 except D-picture
  - SMPTE 421M VC-1
    - Decoding supports Simple Profile Medium Level/ Main Profile High Level/ Advanced Profile Level4
- JPEG Codec
  - Supports Compression/ decompression up to 8192x8192
  - Supported format of compression
    - Input raw image: YCbCr4:2:2 or RGB565
    - Output JPEG file: Baseline JPEG of YCbCr4:2:2 or YCbCr4:2:0
  - Supported format of decompression (Refer to Chapter 9.13. JPEG)
    - Input JPEG file: Baseline JPEG of YCbCr4:4:4, YCbCr4:2:2, YCbCr4:2:0, or gray
    - Output raw image: YCbCr4:2:2 or YCbCr4:2:0
  - Supports general-purpose color-space converter
- 3D Graphic Engine (SGX540)
  - Supports 3D graphics, vector graphics, and video encode and decode on common hardware
  - Tile-based architecture
  - Universal Scalable Shader Engine – multi-threaded engine incorporating Pixel and Vertex Shader functionality
  - Industry standard API support –OGL-ES 1.1 and 2.0 and OpenVG 1.0
  - Fine grained task switching, load balancing, and power management
  - Advanced geometry DMA driven operation for minimum CPU interaction
  - Programmable high-quality image anti-aliasing
  - Fully virtualized memory addressing for functioning of operating system in a unified memory architecture
- 2D Graphic Engine
  - BitBLT
  - Supports maximum 8000x8000 image size
  - Window clipping, 90˚ /180˚ /270˚ Rotation, X Flip / Y Flip
  - Reverse Addressing (X positive/negative, Y positive/negative)
  - Totally 4-operand raster operation (ROP4)
  - Alpha blending (fixed alpha value / per-pixel alpha value)
  - Arbitrary size pixel pattern drawing, Pattern cache
  - 16/24/32-bpp. Packed 24-bpp color format
- Analog TV interface
  - Out video format: NTSC-M/ NTSC-J/ NTSC4.43/ PAL-B, D, G, H, I/ PAL-M/ PAL-N/ PAL-Nc/ PAL-60 compliant
  - Supported input format: ITU-R BT.601 (YCbCr 4 :4 :4)
  - Supports 480i/p and 576i resolutions
  - Supports Composite

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- Digital TV Interface
  - High-definition Multimedia Interface (HDMI) 1.3
  - Supports up to 1080p 30Hz and 8-channel/ 112 kHz/ 24-bit audio
  - Supports 480p, 576p, 720p, 1080i, 1080p (cannot support 480i)
  - Supports HDCP v1.1
- Rotator
  - Supported image format: YCbCr422 (interleave), YCbCr420 (non-interleave), RGB565 and RGB888 (unpacked)
  - Supported rotate degree: 90, 180, 270, flip vertical, and flip horizontal
- Video processor: The video processor supports:
  - BOB/ 2D-IPC mode
  - Produces YCbCr 4:4:4 output to help the mixer blend video and graphics
  - 1/4X to 16X vertical scaling with 4-tap/ 16-phase polyphase filter
  - 1/4X to 16X horizontal scaling with 8-tap/ 16-phase polyphase filter
  - Pan and scan, Letterbox, and NTSC/ PAL conversion using scaling
  - Flexible scaled video positioning within display area
  - 1/16 pixel resolution Pan and Scan modes
  - Flexible post video processing
    - Color saturation, Brightness/ Contrast enhancement, Edge enhancement
    - Color space conversion between BT.601 and BT.709
  - Video input source size up to 1920x1080
- Video Mixer

The Video Mixer supports:

  - Overlapping and blending input video and graphic layers
  - 480i/p, 576i/p, 720p, and 1080i/p display size
  - Four layers (1 video layer, 2 graphic layer, and 1 background layer)
- TFT-LCD Interface

The TFT-LCD Interface supports:

  - 24/ 18/ 16-bpp parallel RGB Interface LCD
  - 8/ 6 bpp serial RGB Interface
  - Dual i80 Interface LCD
  - 1/ 2/ 4/ 8 bpp Palletized or 8/16/24-bpp Non-Palletized Color TFT
  - Typical actual screen size: 1024x768, 800x480, 640x480, 320x240, 160x160, and so on
  - Virtual image up to 16M pixel (4K pixel x4K pixel)
  - Five Window Layers for PIP or OSD
  - Real-time overlay plane multiplexing
  - Programmable OSD window positioning
  - 8-bit Alpha blending (Plane/Pixel)
  - ITU-BT601/656 format output

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1.3.4 AUDIO SUBSYSTEM

The key features of audio subsystem include:

- Audio processing is progressed by Reconfigurable Processor (RP)
- Low power audio subsystem
  - 5.1ch I2S with 32-bit-width 64-depth FIFO
  - 128 KB audio play output buffer
  - Hardware mixer mixes primary and secondary sounds

1.3.5 SECURITY SUBSYSTEM

The key features of security subsystem include:

- On-chip secure boot ROM
  - 64 KB secure boot ROM for secure boot
- On-chip secure RAM
  - 96 KB secure RAM for security function
- Hardware Crypto Accelerator
  - Securely integrated DES/ TDES, AES, SHA-1, PRNG and PKA
  - Access control (Security Domain Manager with the ARM TrustZone Hardware)
  - Enables enhanced secure platform for separate (secure/ non-secure) execution environment for security sensitive application
- Secure JTAG
  - Authentication of JTAG user
  - Access control in JTAG mode

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1.3.6 CONNECTIVITY

The key features of connectivity include:

- PCM Audio Interface
  - 16-bit mono audio interface
  - Master mode only
  - Supports three port PCM interface
- AC97 Audio Interface
  - Independent channels for stereo PCM In, stereo PCM Out, and mono MIC In
  - 16-bit stereo (2-channel) audio
  - Variable sampling rate AC97 Codec interface (48 kHz and below)
  - Supports AC97 Full Specification
- SPDIF Interface (TX only)
  - Linear PCM up to 24-bit per sample support
  - Non-Linear PCM formats such as AC3, MPEG1, and MPEG2 support
  - 2x24-bit buffers that are alternately filled with data
- I2S Bus Interface
  - Three I2S-bus for audio-codec interface with DMA-based operation
  - Serial, 8/ 16/ 24-bit per channel data transfers
  - Supports I2S, MSB-justified, and LSB-justified data format
  - Supports PCM 5.1 channel
  - Various bit clock frequency and codec clock frequency support
    - 16, 24, 32, 48 fs of bit clock frequency
    - 256, 384, 512, 768 fs of codec clock
  - Supports one port for 5.1 channel I2S (in Audio Subsystem) and two ports for 2 channel I2S
- Modem Interface
  - Asynchronous direct/ indirect 16-bit SRAM-style interface
  - On-chip 16 KB dual-ported SRAM buffer for direct interface
- I2C Bus Interface
  - Three Multi-Master IIC-Bus
  - Serial, 8-bit oriented and bi-directional data transfers can be made at up to 100 Kbit/s in the standard mode
  - Up to 400 Kbit/s in the fast mode
- ATA Controller
  - Compatible with the ATA/ATAPI-6 standard

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- UART
  - Four UART with DMA-based or interrupt-based operation
  - Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/ receive
  - Rx/Tx independent 256 byte FIFO for UART0, 64 byte FIFO for UART1 and 16 byte FIFO for UART2/3
  - Programmable baud rate
  - Supports IrDA 1.0 SIR (115.2 Kbps) mode
  - Loop back mode for testing
  - Non-integer clock divides in Baud clock generation
- USB 2.0 OTG
  - Complies with the OTG Revision 1.0a supplement to the USB 2.0
  - Supports high-speed up to 480 Mbps
  - On-chip USB transceiver
- USB Host 2.0
  - Complies with the USB Host 2.0
  - Supports high-speed up to 480 Mbps
  - On-chip USB transceiver
- HS-MMC/ SDIO Interface
  - Multimedia Card Protocol version 4.3 compatible (HS-MMC)
  - SD Memory Card Protocol version 2.0 compatible
  - DMA based or Interrupt based operation
  - 128 word FIFO for Tx/Rx
  - Four ports HS-MMC or four ports SDIO
- SPI Interface
  - Complies with three Serial Peripheral Interface Protocol version 2.11
  - Rx/Tx independent 64-Word FIFO for SPI0 and 16-Word FIFO for SPI1
  - DMA-based or interrupt-based operation

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- GPIO
  - 237 multi-functional input/ output ports
  - Controls 178 External Interrupts
  - GPA0: 8 in/out port – 2xUART with flow control
  - GPA1: 4 in/out port – 2xUART without flow control or 1xUART with flow control
  - GPB: 8 in/out port – 2x SPI
  - GPC0: 5 in/out port – I2S, PCM, AC97
  - GPC1: 5 in/out port – I2S, SPDIF, LCD_FRM
  - GPD0: 4 in/out port – PWM
  - GPD1: 6 in/out port – 3xI2C, PWM, IEM
  - GPE0,1: 13 in/out port – Camera Interface
  - GPF0,1,2,3: 30 in/out port – LCD Interface
  - GPG0,1,2,3: 28 in/out port – 4xMMC channel (Channel 0 and 2 support 4-bit and 8-bit modes, but channel 1 and 3 support only 4-bit mode)
  - GPH0,1,2,3: 32 in/out port – Key pad, External Wake-up (up-to 32-bit), HDMI
  - GPI: Low power I2S, PCM
  - GPJ0,1,2,3,4: 35 in/out port – Modem IF, CAMIF, CFCON, KEYPAD, SROM ADDR[22:16]
  - MP0_1,2,3: 20 in/out port – Control signals of EBI (SROM, NF, CF, and OneNAND)
  - MP0_4,5,6,7: 32 in/out memory port – EBI (For more information about EBI configuration, refer to Chapter 5.6. EBI)

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1.3.7 SYSTEM PERIPHERAL

The key features of system peripheral include:

- Real Time Clock
  - Full clock features: sec, min, hour, date, day, month, and year
  - 32.768kHz operation
  - Alarm interrupt
  - Time-tick interrupt
- PLL
  - Four on-chip PLLs, APLL/MPLL/EPLL/VPLL
  - APLL generates ARM core and MSYS clocks
  - MPLL generates a system bus clock and special clocks
  - EPLL generates special clocks
  - VPLL generates clocks for video interface
- Keypad
  - 14x8 Key Matrix support
  - Provides internal de-bounce filter
- Timer with Pulse Width Modulation
  - Five channel 32-bit internal timer with interrupt-based operation
  - Four channel 32-bit Timer with PWM
  - Programmable duty cycle, frequency, and polarity
  - Dead-zone generation
  - Supports external clock source
- System timer
  - Accurate timer provides exact 1ms tick at any power mode except sleep
  - Interrupt interval can be changed without stopping reference tick timer
- DMA
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility to program DMA transfers
  - Supports linked list DMA function
  - Supports three enhanced built-in DMA with eight channels per DMA, so the total number of channels supported are 24
  - Supports one Memory-to-memory type optimized DMA and two Peripheral-to-memory type optimized DMA
  - M2M DMA supports up to 16 burst and P2M DMA supports up to 8 burst
- A/D Converter and Touch Screen Interface
  - 10 channel multiplexed ADC
  - Maximum 500Ksamples/sec and 12-bit resolution
- Watch Dog Timer
  - 16-bit watch dog timer

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- Vectored Interrupt Controller
  - Software such as Interrupt device driver can mask out particular interrupt requests
  - Prioritization of interrupt sources for interrupt nesting
- Power Management
  - Clock-gating control for components
  - Various low power modes are available such as Idle, Stop, Deep Stop, Deep Idle, and Sleep modes
  - Wake up sources in sleep mode are external interrupts, RTC alarm, Tick timer and the key interface.
  - Stop and Deep Stop mode's wake up sources are MMC, Touch screen interface, system timer, and entire wake up sources of Sleep mode.
  - Deep Idle mode's wake up sources are 5.1ch I2S and wake up source of Stop mode.

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1.4 CONVENTIONS

1.4.1 REGISTER R/W CONVENTIONS

Symbol	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
W	Write Only	The application has permission to write in the Register field.
R/W	Read & Write	The application has permission to read and writes in the Register field. The application sets this field by writing 1’b1 and clears it by writing 1’b0.
R/WC	Read & Write to clear	The application has permission to read and writes in the Register field. The application clears this field by writing 1’b1. A register write of 1'b0 has no effect on this field.
R/WS	Read & Write to set	The application has permission to read and writes in the Register field. The application sets this field by writing 1’b1. A register write of 1'b0 has no effect on this field.

1.4.2 REGISTER VALUE CONVENTIONS

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

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2 MEMORY MAP

This chapter describes the memory map available in S5PV210 processor.

2.1 MEMORY ADDRESS MAP

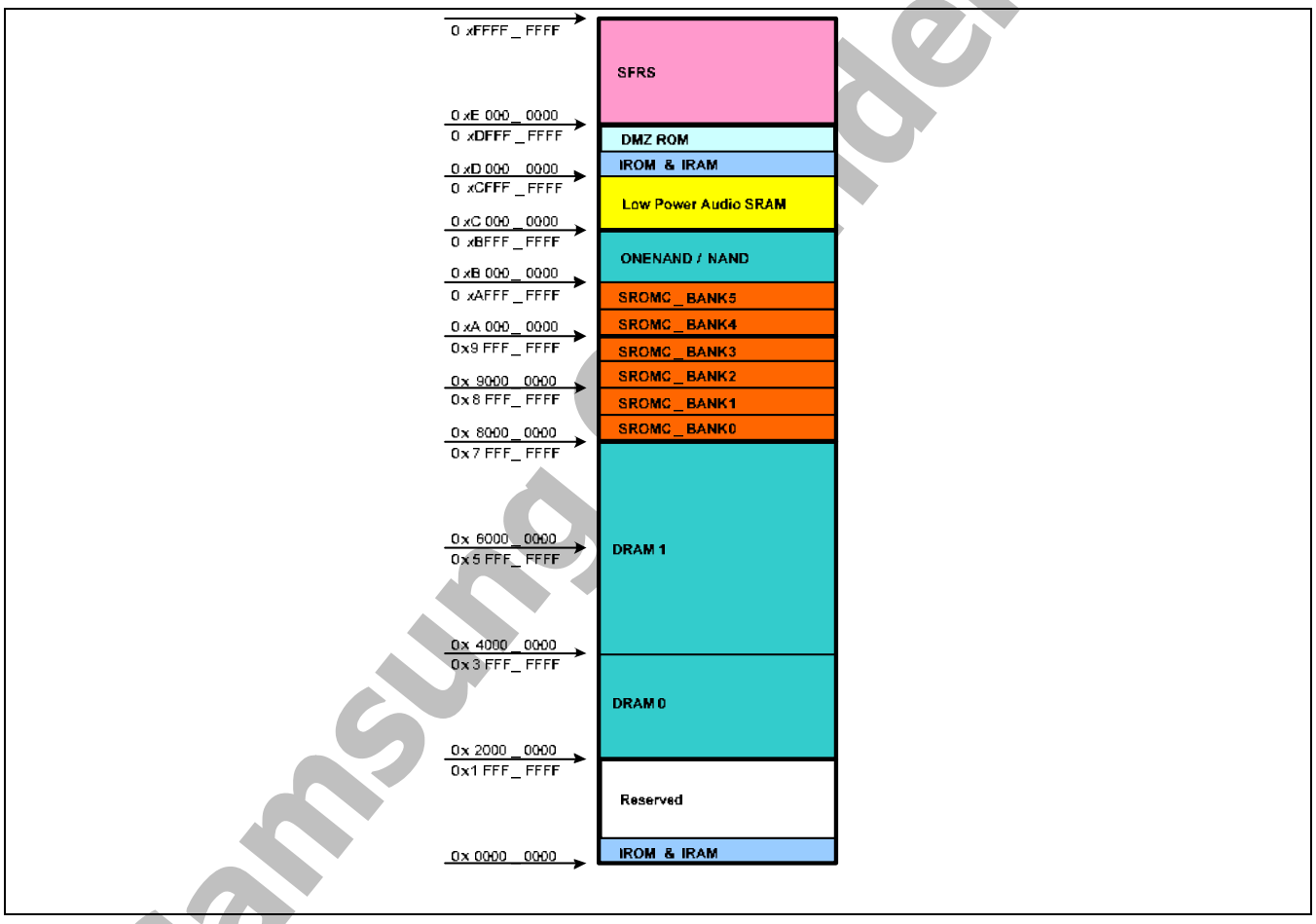

Figure 2-1 Address Map

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2.1.1 DEVICE SPECIFIC ADDRESS SPACE

Address		Size	Description	Note
0x0000_0000	0x1FFF_FFFF	512MB	Boot area	Mirrored region depending on the boot mode.
0x2000_0000	0x3FFF_FFFF	512MB	DRAM 0	
0x4000_0000	0x7FFF_FFFF	1024MB	DRAM 1	
0x8000_0000	0x87FF_FFFF	128MB	SROM Bank 0	
0x8800_0000	0x8FFF_FFFF	128MB	SROM Bank 1	
0x9000_0000	0x97FF_FFFF	128MB	SROM Bank 2	
0x9800_0000	0x9FFF_FFFF	128MB	SROM Bank 3	
0xA000_0000	0xA7FF_FFFF	128MB	SROM Bank 4	
0xA800_0000	0xAFFF_FFFF	128MB	SROM Bank 5	
0xB000_0000	0xBFFF_FFFF	256MB	OneNAND/NAND Controller and SFR	
0xC000_0000	0xCFFF_FFFF	256MB	MP3_SRAM output buffer	
0xD000_0000	0xD000_FFFF	64KB	IROM	
0xD001_0000	0xD001_FFFF	64KB	Reserved	
0xD002_0000	0xD003_7FFF	96KB	IRAM	
0xD800_0000	0xDFFF_FFFF	128MB	DMZ ROM	
0xE000_0000	0xFFFF_FFFF	512MB	SFR region	

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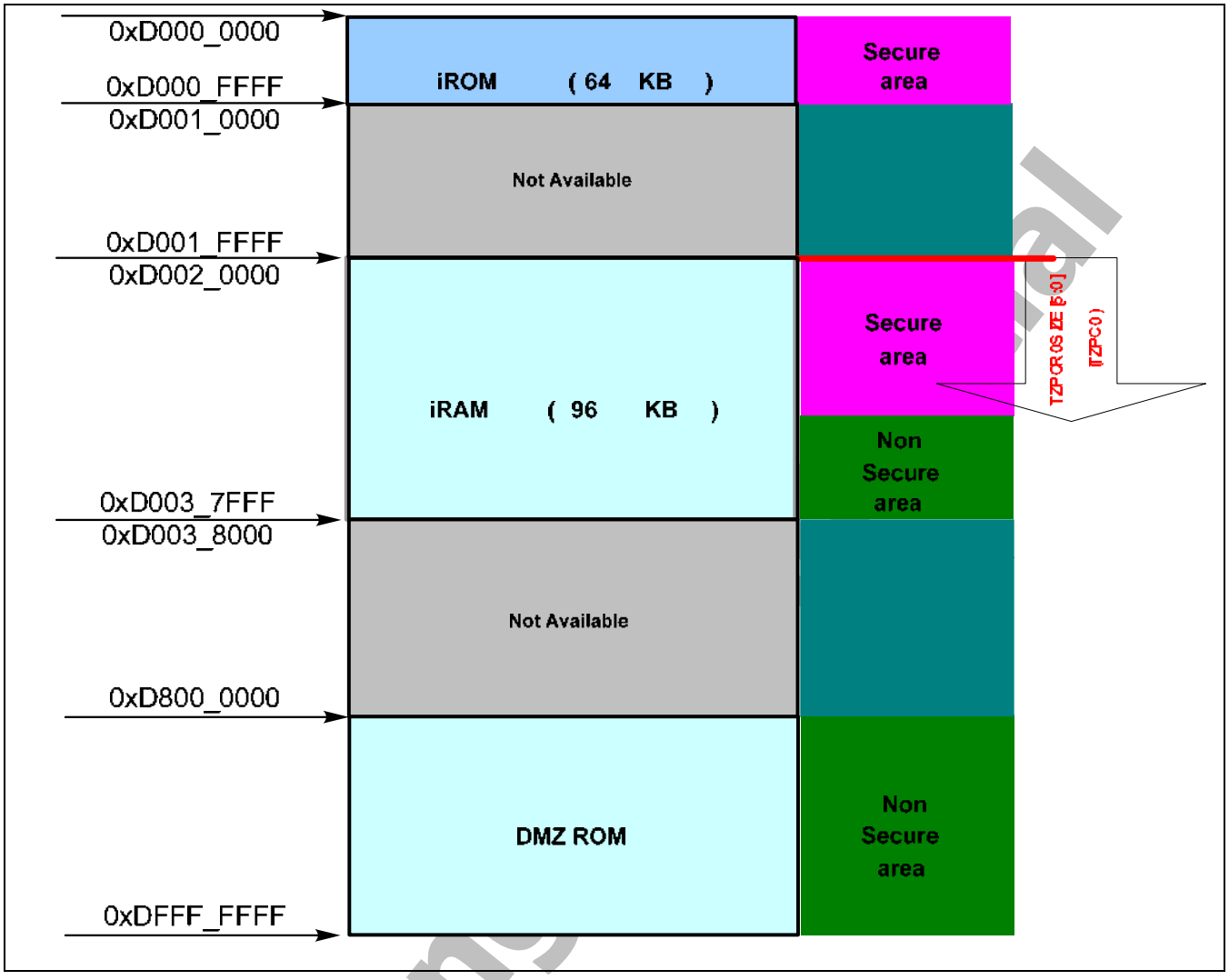

Figure 2-2 Internal Memory Address Map

NOTE: TZPCR0SIZE[5:0](TZPC0); (in TZPC SFR)
- 4KByte chunks
- Recommended value: 6'b00_0000 ~ 6'b10_0000
  * if (TZPCR0SIZE[5](TZPC0) == 1'b1), the full address range in iSRAM is configured as secure.
  * if (TZPCR0SIZE(TZPC0) == 6'b00_0000), there is non-secure region in iSRAM (0kB).
  * if (TZPCR0SIZE(TZPC0) == 6'b00_0001), the minimum secure region size is 4kB.
  * if (TZPCR0SIZE(TZPC0) == 6'b01_0000), the 64KB from iSRAM start address specifies the secure region.
- iROM is always secure area

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2.1.2 SPECIAL FUNCTION REGISTER MAP

Address		Description
0xE000_0000	0xE00F_FFFF	CHIPID
0xE010_0000	0xE01F_FFFF	SYSCON
0xE020_0000	0xE02F_FFFF	GPIO
0xE030_0000	0xE03F_FFFF	AXI_DMA
0xE040_0000	0xE04F_FFFF	AXI_PSYS
0xE050_0000	0xE05F_FFFF	AXI_PSFR
0xE060_0000	0xE06F_FFFF	TZPC2
0xE070_0000	0xE07F_FFFF	IEM_APC
0xE080_0000	0xE08F_FFFF	IEM_IEC
0xE090_0000	0xE09F_FFFF	PDMA0
0xE0A0_0000	0xE0AF_FFFF	PDMA1
0xE0D0_0000	0xE0DF_FFFF	CORESIGHT
0xE0E0_0000	0xE0EF_FFFF	SECKEY
0xE0F0_0000	0xE0FF_FFFF	ASYNC_AUDIO_PSYS
0xE110_0000	0xE11F_FFFF	SPDIF
0xE120_0000	0xE12F_FFFF	PCM1
0xE130_0000	0xE13F_FFFF	SPI0
0xE140_0000	0xE14F_FFFF	SPI1
0xE160_0000	0xE16F_FFFF	KEYIF
0xE170_0000	0xE17F_FFFF	TSADC
0xE180_0000	0xE18F_FFFF	I2C0 (general)
0xE1A0_0000	0xE1AF_FFFF	I2C2 (PMIC)
0xE1B0_0000	0xE1BF_FFFF	HDMI_CEC
0xE1C0_0000	0xE1CF_FFFF	TZPC3
0xE1D0_0000	0xE1DF_FFFF	AXI_GSYS
0xE1F0_0000	0xE1FF_FFFF	ASYNC_PSFR_AUDIO
0xE210_0000	0xE21F_FFFF	I2S1
0xE220_0000	0xE22F_FFFF	AC97
0xE230_0000	0xE23F_FFFF	PCM0
0xE250_0000	0xE25F_FFFF	PWM
0xE260_0000	0xE26F_FFFF	ST
0xE270_0000	0xE27F_FFFF	WDT
0xE280_0000	0xE28F_FFFF	RTC_APBIF
0xE290_0000	0xE29F_FFFF	UART
0xE800_0000	0xE80F_FFFF	SROMC

Address		Description
0xE820_0000	0xE82F_FFFF	CFCON
0xEA00_0000	0xEA0F_FFFF	SECSS
0xEB00_0000	0xEB0F_FFFF	SDMMC0
0xEB10_0000	0xEB1F_FFFF	SDMMC1
0xEB20_0000	0xEB2F_FFFF	SDMMC2
0xEB30_0000	0xEB3F_FFFF	SDMMC3
0xEB40_0000	0xEB4F_FFFF	TSI
0xEC00_0000	0xEC0F_FFFF	USBOTG
0xEC10_0000	0xEC1F_FFFF	USBOTG_PHY_CON
0xEC20_0000	0xEC2F_FFFF	USBHOST_EHCI
0xEC30_0000	0xEC3F_FFFF	USBHOST_OHCI
0xED00_0000	0xED0F_FFFF	MODEM
0xED10_0000	0xED1F_FFFF	HOST
0xEE00_0000	0xEE8F_FFFF	AUDIO_SS
0xEE90_0000	0xEE9F_FFFF	AUDIO_SS/ASS_DMA
0xEEA0_0000	0xEEAF_FFFF	AUDIO_SS/ASS_IBUF0
0xEEB0_0000	0xEEBF_FFFF	AUDIO_SS/ASS_IBUF1
0xEEC0_0000	0xEECF_FFFF	AUDIO_SS/ASS_OBUF0
0xEED0_0000	0xEEDF_FFFF	AUDIO_SS/ASS_OBUF1
0xEEE0_0000	0xEEEF_FFFF	AUDIO_SS/ASS_APB
0xEEF0_0000	0xEEFF_FFFF	AUDIO_SS/ASS_ODO
0xF000_0000	0xF00F_FFFF	DMC0_SFR
0xF100_0000	0xF10F_FFFF	AXI_MSYS
0xF110_0000	0xF11F_FFFF	AXI_MSFR
0xF120_0000	0xF12F_FFFF	AXI_VSYS
0xF140_0000	0xF14F_FFFF	DMC1_SFR
0xF150_0000	0xF15F_FFFF	TZPC0
0xF160_0000	0xF16F_FFFF	SDM
0xF170_0000	0xF17F_FFFF	MFC
0xF180_0000	0xF18F_FFFF	ASYNC_MFC_VSYS0
0xF190_0000	0xF19F_FFFF	ASYNC_MFC_VSYS1
0xF1A0_0000	0xF1AF_FFFF	ASYNC_DSYS_MSYS0
0xF1B0_0000	0xF1BF_FFFF	ASYNC_DSYS_MSYS1
0xF1C0_0000	0xF1CF_FFFF	ASYNC_MSFR_DSFR
0xF1D0_0000	0xF1DF_FFFF	ASYNC_MSFR_PSFR
0xF1E0_0000	0xF1EF_FFFF	ASYNC_MSYS_DMC0

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Address		Description
0xF1F0_0000	0xF1FF_FFFF	ASYNC_MSFR_MPERI
0xF200_0000	0xF20F_FFFF	VIC0
0xF210_0000	0xF21F_FFFF	VIC1
0xF220_0000	0xF22F_FFFF	VIC2
0xF230_0000	0xF23F_FFFF	VIC3
0xF280_0000	0xF28F_FFFF	TZIC0
0xF290_0000	0xF29F_FFFF	TZIC1
0xF2A0_0000	0xF2AF_FFFF	TZIC2
0xF2B0_0000	0xF2BF_FFFF	TZIC3
0xF300_0000	0xF3FF_FFFF	G3D
0xF800_0000	0xF80F_FFFF	FIMD
0xF900_0000	0xF90F_FFFF	TVENC
0xF910_0000	0xF91F_FFFF	VP
0xF920_0000	0xF92F_FFFF	MIXER
0xFA00_0000	0xFA0F_FFFF	G2D
0xFA10_0000	0xFA1F_FFFF	HDMI_LINK
0xFA20_0000	0xFA2F_FFFF	SMDMA
0xFA30_0000	0xFA3F_FFFF	ROT
0xFA40_0000	0xFA4F_FFFF	AXI_LSYS
0xFA50_0000	0xFA5F_FFFF	DSIM
0xFA60_0000	0xFA6F_FFFF	CSIS
0xFA70_0000	0xFA7F_FFFF	AXI_DSYS
0xFA80_0000	0xFA8F_FFFF	AXI_DSFR
0xFA90_0000	0xFA9F_FFFF	I2C_HDMI_PHY
0xFAA0_0000	0xFAAF_FFFF	AXI_TSYS
0xFAB0_0000	0xFABF_FFFF	I2C_HDMI_DDC
0xFAC0_0000	0xFACF_FFFF	AXI_XSYS
0xFAD0_0000	0xFADF_FFFF	TZPC1
0xFAF0_0000	0xFAFF_FFFF	ASYNC_PSYS_DSYS_u0
0xFB20_0000	0xFB2F_FFFF	FIMC0
0xFB30_0000	0xFB3F_FFFF	FIMC1
0xFB40_0000	0xFB4F_FFFF	FIMC2
0xFB60_0000	0xFB6F_FFFF	JPEG

3 SIZE & BALL MAP

3.1 PIN ASSIGNMENT

3.1.1 PIN ASSIGNMENT DIAGRAM - 584-BALL FCFBGA

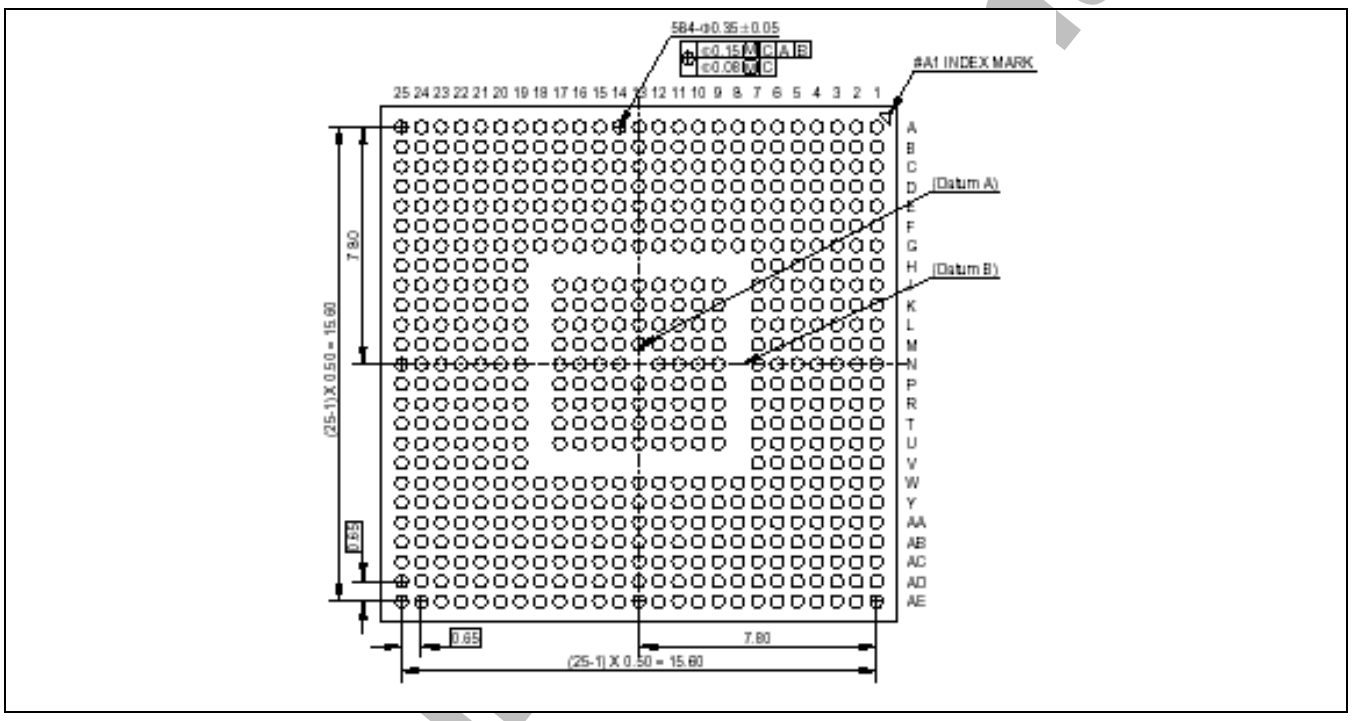

Figure 3-1 S5PV210 Pin Assignment (584-FCFBGA) Bottom View

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3.1.2 PIN NUMBER ORDER

Table 3-1 S5PV210 584 FCFBGA Pin Assignment – Pin Number Order (1/4)

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
A1	VSS	AA16	VSS_UHOST_AC	AC6	XVVD_22	AD21	XUOTGDP
A2	XMSMDATA_15	AA17	XCIDATA_7	AC7	XVVD_13	AD22	XI2C1SCL
A3	XMSMIRQN	AA18	XCICLKENB	AC8	XVVD_11	AD23	XUHOSTPWREN
A4	XMSMADVN	AA19	XCIDATA_3	AC9	XVVD_7	AD24	XEINT_28
A5	XMMC0DATA_1	AA20	XEINT_29	AC10	XADCAIN_3	AD25	XEINT_26
A6	XMMC1DATA_2	AA21	XEINT_20	AC11	XADCAIN_0	AE1	VSS
A7	XURTSN_0	AA22	XEINT_4	AC12	XADCAIN_1	AE2	XI2S0SDI
A8	XPWMTOUT_2	AA23	XEINT_21	AC13	XURXD_3	AE3	XI2S0LRCK
A9	XMMC3CLK	AA24	XEINT_12	AC14	XUTXD_2	AE4	XVSYS_OE
A10	XMMC3DATA_3	AA25	XEINT_7	AC15	XMIPIVREG_0P4V	AE5	XVVD_15
A11	XSPIMOSI_1	AB1	XPCM0FSYNC	AC16	XI2C2SDA	AE6	XVVD_10
A12	XM1DATA_31	AB2	XPCM0SIN	AC17	XUHOSTREXT	AE7	XVVD_6
A13	XM1DATA_29	AB3	XI2S1CDCLK	AC18	XUOTGVBUS	AE8	XMIPISDN3
A14	XM1DATA_26	AB4	XI2S1SDO	AC19	XUOTGDRVVBUS	AE9	XMIPISDN2
A15	XM1DQS_2	AB5	XVVD_20	AC20	XURXD_2	AE10	XMIPISDNCLK
A16	XM1SCLK	AB6	XVVD_5	AC21	XCIPCLK	AE11	XMIPISDN1
A17	XM1DATA_13	AB7	XVVD_3	AC22	XUHOSTOVERCUR	AE12	XMIPISDN0
A18	XM1DQSN_1	AB8	XVVD_2	AC23	XEINT_13	AE13	XMIPIMDP3
A19	XM1DATA_11	AB9	XVVD_1	AC24	XEINT_24	AE14	XMIPIMDP2
A20	XM1DATA_10	AB10	XVVDEN	AC25	XEINT_22	AE15	XMIPIMDPCLK
A21	XM1DATA_5	AB11	XADCAIN_2	AD1	XI2S1SCLK	AE16	XMIPIMDP1
A22	XM1DQSN_0	AB12	XADCAIN_9	AD2	XI2S0SCLK	AE17	XMIPIMDP0
A23	XM1DATA_3	AB13	XUTXD_3	AD3	XI2S0SDO_0	AE18	XUOTGREXT
A24	XM1DATA_0	AB14	XCIHREF	AD4	XEFFSOURCE_0	AE19	XUHOSTDP
A25	VSS	AB15	XCIDATA_0	AD5	XVVD_18	AE20	XUSBXTO
AA1	XPCM0EXTCLK	AB16	XCIDATA_1	AD6	XVVD_14	AE21	XUOTGDM
AA2	XPCM0SCLK	AB17	XCIDATA_6	AD7	XVVD_16	AE22	XI2C2SCL
AA3	XI2S0SDO_2	AB18	XDDR2SEL	AD8	XMIPISDP3	AE23	XI2C1SDA
AA4	XMMC2CDN	AB19	XCIFIELD	AD9	XMIPISDP2	AE24	XCLKOUT
AA5	XI2S1SDI	AB20	XCIDATA_2	AD10	XMIPISDPCLK	AE25	VSS
AA6	XVVD_19	AB21	XCIDATA_4	AD11	XMIPISDP1	B1	XMSMDATA_10
AA7	XVVD_17	AB22	XEINT_25	AD12	XMIPISDP0	B2	XMSMDATA_13
AA8	XVVD_8	AB23	XEINT_31	AD13	XMIPIMDN3	B3	XMSMDATA_14
AA9	XVVD_0	AB24	XEINT_19	AD14	XMIPIMDN2	B4	XMSMWEN

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Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
AA10	XVVCLK	AB25	XEINT_14	AD15	XMIPIMDNCLK	B5	XMMC0CLK
AA11	XADCAIN_8	AC1	XPCM0SOUT	AD16	XMIPIMDN1	B6	XMMC1CLK
AA12	XADCAIN_7	AC2	XI2S1LRCK	AD17	XMIPIMDN0	B7	XSPICLK_0
AA13	XVHSYNC	AC3	XI2S0SDO_1	AD18	XUOTGID	B8	XUCTSN_1
AA14	XCIVSYNC	AC4	XI2S0CDCLK	AD19	XUHOSTDM	B9	XPWMTOUT_1
AA15	VSS_UHOST_A	AC5	XVVD_21	AD20	XUSBXTI	B10	XMMC3DATA_0

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Table 3-2 S5PV210 584 FCFBGA Pin Assignment – Pin Number Order (2/4)

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
B11	XSPICSN_1	D1	XMSMDATA_4	E16	XM1ADDR_14	G6	XMSMADDR_1
B12	XM1DATA_30	D2	XMSMDATA_6	E17	XM1ADDR_2	G7	VSS
B13	XM1DATA_28	D3	XMSMDATA_3	E18	XM1ADDR_8	G8	XMSMCSN
B14	XM1DATA_25	D4	XMSMDATA_9	E19	XM1ADDR_12	G9	XMSMRN
B15	XM1DQSN_2	D5	XMSMADDR_7	E20	XM1ADDR_1	G10	XURXD_1
B16	XM1NSCLK	D6	XMMC0DATA_2	E21	XM1ADDR_0	G11	VDD_EXT2
B17	XM1DATA_14	D7	XMMC1DATA_0	E22	XM2DQM_3	G12	XSPICLK_1
B18	XM1DQS_1	D8	XUTXD_0	E23	XM2DATA_23	G13	XSPIMISO_1
B19	XM1DATA_8	D9	XUCTSN_0	E24	XM2DATA_22	G14	XM1CSN_1
B20	XM1DATA_9	D10	XMMC3CMD	E25	XM2DATA_21	G15	XM1CKE_0
B21	XM1DATA_4	D11	XMMC3DATA_2	F1	XMSMADDR_10	G16	XM1CKE_1
B22	XM1DQS_0	D12	XM1DQS_3	F2	XMSMADDR_13	G17	XM1WEN
B23	XM1DATA_2	D13	XM1DATA_24	F3	XMSMDATA_0	G18	XM1CSN_0
B24	XM2DATA_31	D14	XM1DQM_2	F4	XM0ADDR_14	G19	VSS
B25	XM2DATA_29	D15	XM1DATA_18	F5	XMSMADDR_6	G20	XM2ADDR_8
C1	XMSMDATA_7	D16	XM1DATA_16	F6	XMSMADDR_8	G21	XM2CKE_1
C2	XMSMDATA_8	D17	XM1DQM_1	F7	XMMC0CDN	G22	XM2DATA_19
C3	XMSMDATA_11	D18	XM1ADDR_4	F8	XMMC1CMD	G23	XM2DATA_18
C4	XMSMDATA_12	D19	XM1ADDR_6	F9	XMMC1DATA_3	G24	XM2SCLK
C5	XMMC0DATA_0	D20	XM1ADDR_7	F10	XUTXD_1	G25	XM2NSCLK
C6	XMMC0DATA_3	D21	XM1ADDR_15	F11	XI2C0SDA	H1	XMSMADDR_0
C7	XMMC1CDN	D22	XM2DATA_28	F12	XPWMTOUT_3	H2	XMSMADDR_5
C8	XURXD_0	D23	XM2DATA_26	F13	XM1DATA_22	H3	XM0ADDR_15
C9	XI2C0SCL	D24	XM2DATA_25	F14	XM1ADDR_11	H4	XM0ADDR_8
C10	XMMC3DATA_1	D25	XM2DATA_24	F15	XM1ADDR_5	H5	XM0ADDR_3
C11	XM1DQM_3	E1	XMSMDATA_2	F16	XM1ADDR_9	H6	XM0ADDR_12
C12	XM1DQSN_3	E2	XMSMDATA_1	F17	XM1CASN	H7	XMSMADDR_3
C13	XM1DATA_27	E3	XMSMDATA_5	F18	XM1ADDR_13	H19	XM2ADDR_9
C14	XM1DATA_23	E4	XMSMADDR_2	F19	XM1ADDR_10	H20	XM2ADDR_13
C15	XM1DATA_19	E5	XMSMADDR_12	F20	XM2ADDR_5	H21	XM2DQM_2
C16	XM1DATA_17	E6	XMMC0CMD	F21	XM2ADDR_4	H22	XM2ADDR_6
C17	XM1DATA_15	E7	XMMC1DATA_1	F22	XM2DATA_27	H23	XM2ADDR_11
C18	XM1DATA_12	E8	XPWMTOUT_0	F23	XM2DATA_20	H24	XM2DATA_17
C19	XM1DATA_7	E9	XSPICSN_0	F24	XM2DQS_2	H25	XM2DATA_16
C20	XM1DATA_6	E10	XURTSN_1	F25	XM2DQSN_2	J1	XM0CSN_2
C21	XM1DQM_0	E11	XMMC3CDN	G1	XMSMADDR_4	J2	XM0FWEN

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Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
C22	XM1DATA_1	E12	XM1RASN	G2	XMSMADDR_9	J3	XM0ADDR_10
C23	XM2DATA_30	E13	XM1DATA_20	G3	XMSMADDR_11	J4	XM0ADDR_2
C24	XM2DQS_3	E14	XM1DATA_21	G4	XM0ADDR_9	J5	XM0ADDR_7
C25	XM2DQSN_3	E15	XM1ADDR_3	G5	XM0ADDR_13	J6	XM0ADDR_4

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Table 3-3 S5PV210 584 FCFBGA Pin Assignment – Pin Number Order (3/4)

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
J7	VDD_MODEM	L1	XM0DATA_8	M20	VDD_APLL	P14	VDD_ARM
J9	XSPIMISO_0	L2	XM0DATA_9	M21	XM2DATA_8	P15	VDD_ARM
J10	VDD_EXT0	L3	XM0DATA_1	M22	XM2DATA_5	P16	VSS
J11	XSPIMOSI_0	L4	XM0DATA_10	M23	XM2DATA_7	P17	VDD_CKO
J12	VSS	L5	XM0DATA_2	M24	XM2DATA_9	P19	VSS_VPLL
J13	VDD_M1	L6	XM0FRNB_3	M25	XM2DATA_11	P20	VDD_VPLL
J14	VDD_M1	L7	XM0ADDR_1	N1	XM0DATA_4	P21	VDD_RTC
J15	VDD_M1	L9	VSS	N2	XM0DATA_5	P22	XM2WEN
J16	VDD_M1	L10	VDD_INT	N3	XM0CSN_4	P23	XM2DATA_0
J17	VDD_M2	L11	VDD_INT	N4	XM0DATA_7	P24	XM2DATA_3
J19	XM2ADDR_7	L12	VSS	N5	XM0DATA_14	P25	XM2DQM_0
J20	XM2ADDR_14	L13	VDD_ARM	N6	XM0BEN_1	R1	XHDMITXCN
J21	XM2RASN	L14	VDD_ARM	N7	XM0CSN_5	R2	XHDMITXCP
J22	XM2ADDR_12	L15	VDD_ARM	N9	XM0CSN_3	R3	XM0FRNB_0
J23	XM2CASN	L16	VSS	N10	VDD_INT	R4	XM0OEN
J24	XM2CKE_0	L17	VDD_M2	N11	VDD_INT	R5	XJTMS
J25	XM2DATA_14	L19	XM2ADDR_1	N12	VSS	R6	VDD_HDMI_PLL
K1	XM0FCLE	L20	XM2ADDR_0	N14	VDD_ARM	R7	VSS_HDMI
K2	XM0FALE	L21	XM2ADDR_2	N15	VDD_ARM	R9	VSS
K3	XM0DATA_0	L22	XM2DQM_1	N16	VDD_ARM	R10	VSS
K4	XM0ADDR_5	L23	XM2DATA_10	N17	VSS	R11	VDD_INT
K5	XM0ADDR_0	L24	XM2DQS_1	N19	VSS_MPLL	R12	VDD_INT
K6	XM0ADDR_6	L25	XM2DQSN_1	N20	VDD_MPLL	R13	VDD_INT
K7	XM0ADDR_11	M1	XM0DATA_11	N21	XM2CSN_0	R14	VSS
K9	VDD_M0	M2	XM0FREN	N22	XM2DATA_6	R15	VSS
K10	VSS	M3	XM0DATA_12	N23	XM2DATA_4	R16	VSS
K11	VSS	M4	XM0DATA_3	N24	XM2DQS_0	R17	VDD_ALIVE
K12	VSS	M5	XM0DATA_13	N25	XM2DQSN_0	R19	VSS_EPLL
K13	VDD_INT	M6	XM0FRNB_1	P1	XM0DATA_6	R20	VDD_EPLL
K14	VDD_INT	M7	XM0DATA_RDN	P2	XM0DATA_15	R21	XEPLLFILTER
K15	VDD_INT	M9	VDD_M0	P3	XJDBGSEL	R22	XRTCCLKO
K16	VSS	M10	VSS	P4	XM0WEN	R23	XM2ADDR_3
K17	VDD_M2	M11	VDD_INT	P5	XJTRSTN	R24	XM2DATA_1
K19	VSS	M12	VSS	P6	VDD_HDMI	R25	XM2DATA_2
K20	XM2ADDR_15	M13	VDD_ARM	P7	VSS_HDMI_PLL	T1	XHDMITX0N
K21	XM2CSN_1	M14	VDD_ARM	P9	VDD_SYS0	T2	XHDMITX0P

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Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
K22	XM2ADDR_10	M15	VDD_ARM	P10	VSS	T3	XM0BEN_0
K23	XM2DATA_13	M16	VSS	P11	VDD_INT	T4	XM0CSN_1
K24	XM2DATA_15	M17	VDD_M2	P12	VSS	T5	XJTDI
K25	XM2DATA_12	M19	VSS_APLL	P13	VSS	T6	VSS_HDMI_OSC

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Table 3-4 S5PV210 584 FCFBGA Pin Assignment – Pin Number Order (4/4)

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
T7	VDD_HDMI_OSC	V1	XHDMITX2N	Y2	XHDMIXTI		
T9	VDD_EXT1	V2	XHDMITX2P	Y3	XMMC2DATA_2		
T10	VSS	V3	XM0FRNB_2	Y4	XMMC2DATA_0		
T11	VDD_INT	V4	XDACCOMP	Y5	XMMC2DATA_1		
T12	VSS	V5	XDACVREF	Y6	XMMC2CLK		
T13	VSS	V6	VSS_DAC	Y7	XVVD_23		
T14	VSS	V7	VDD_DAC	Y8	XVVD_12		
T15	VSS	V19	VDD_CAM	Y9	XVVD_4		
T16	VSS	V20	XEINT_8	Y10	XVVSYNC		
T17	VDD_KEY	V21	XEINT_18	Y11	XADCAIN_4		
T19	VDD_SYS1	V22	XEINT_9	Y12	XADCAIN_6		
T20	XNRSTOUT	V23	XOM_2	Y13	VDD_MIPI_A		
T21	XNWRESET	V24	XOM_5	Y14	VSS_UHOST_D		
T22	XOM_1	V25	XOM_4	Y15	VSS_UOTG_AC		
T23	XOM_0	W1	XHDMIREXT	Y16	VDD_UHOST_A		
T24	XRTCXTI	W2	XM0WAITN	Y17	VSS_UOTG_A		
T25	XRTCXTO	W3	XJTDO	Y18	XCIDATA_5		
U1	XHDMITX1N	W4	XMMC2DATA_3	Y19	XEINT_30		
U2	XHDMITX1P	W5	XDACIREF	Y20	XEINT_23		
U3	XM0CSN_0	W6	XMMC2CMD	Y21	XEINT_0		
U4	XJTCK	W7	VSS	Y22	XEINT_27		
U5	XDACOUT	W8	XVVSYNC_LDI	Y23	XEINT_17		
U6	VSS_DAC_A	W9	XVVD_9	Y24	XEINT_10		
U7	VDD_DAC_A	W10	VDD_ADC	Y25	XEINT_3		
U9	VDD_AUD	W11	VSS_ADC				
U10	VDD_LCD	W12	XADCAIN_5				
U11	VSS_MIPI	W13	VDD_UHOST_D				
U12	VDD_MIPI_D	W14	VDD_MIPI_PLL				
U13	VDD_MIPI_D	W15	VDD_ALIVE				
U14	VSS_MIPI	W16	VDD_UOTG_A				
U15	VDD_UOTG_D	W17	VSS_UOTG_D				
U16	VDD_SYS0	W18	VDD_EXT1				
U17	VDD_SYS0	W19	VSS				
U19	VDD_AUD	W20	XEINT_15				
U20	XEINT_16	W21	XEINT_6				
U21	XOM_3	W22	XEINT_11				

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Ball	Pin Name	Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
U22	XPWRRGTON	W23	XEINT_2				
U23	XNRESET	W24	XEINT_5				
U24	XXTI	W25	XEINT_1				
U25	XXTO	Y1	XHDMIXTO				

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3.1.3 POWER PINS

Table 3-5 S5PV210 Power Pin to Ball Assignment (1/2)

Power Group	Pin Name	Ball	Description
Digital I/O	VDD_M2	J17, K17, L17, M17	MDDR 2
	VDD_M1	J13, J14, J15, J16	MDDR 1
	VDD_M0	K9, M9	OneNAND(EBI)
	VDD_LCD	U10	LCD
	VDD_CAM	V19	CAMIF
	VDD_AUD	U9, U19	AUDIO(I2S)
	VDD_MODEM	J7	MSM
	VDD_KEY	T17	KEY
	VDD_SYS0	P9, U16, U17	SYS0(EINT0~7,Clock, OM,Reset)
	VDD_SYS1	T19	SYS1(EINT8~15)
	VDD_EXT0	J10	EXT0
	VDD_EXT1	T9, W18	EXT1
	VDD_EXT2	G11	EXT2
	VDD_CKO	P17	RTC CLKO
	VDD_RTC	P21	RTC
Internal Logic	VDD_INT	K13, K14, K15, L10, L11, M11, N10, N11, P11, R11, R12, R13, T11	Internal logic
	VDD_ARM	L13, L14, L15, M13, M14, M15, N14, N15, N16, P14, P15	Cortex-A8 core
	VDD_ALIVE	R17, W15	Alive logic
Analog & High Speed	VDD_ADC	W10	ADC
	VDD_DAC_A	U7	DAC Analog
	VDD_DAC	V7	DAC Digital
	VDD_MIPI_A	Y13	MIPI 1.8V
	VDD_MIPI_D	U12, U13	MIPI 1.1V
	VDD_MIPI_PLL	W14	MIPI PLL
	VDD_HDMI	P6	HDMI TX
	VDD_HDMI_PLL	R6	HDMI PLL
	VDD_HDMI_OSC	T7	HDMI OSC
	VDD_UOTG_A	W16	USB OTG 3.3V
	VDD_UOTG_D	U15	USB OTG 1.1V
	VDD_UHOST_A	Y16	USB HOST 3.3V
	VDD_UHOST_D	W13	USB HOST 1.1V
	VDD_APLL	M20	APLL

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Power Group	Pin Name	Ball	Description
	VDD_MPLL	N20	MPLL
	VDD_VPLL	P20	VPLL
	VDD_EPLL	R20	EPLL

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Table 3-6 S5PV210 Power Pin to Ball Assignment (2/2)

Power Group	Pin Name	Ball
Internal Logic Digital I/O	VSS	A1, A25, AE1, AE25, G19, G7, J12, K10, K11, K12, K16, K19, L12, L16, L9, M10, M12, M16, M19, N12, N17, N19, P10, P12, P13, P16, P19, R10, R14, R15, R16, R19, R9, T10, T12, T13, T14, T15, T16, W19, W7
Analog IO	VSS_APLL	M20
	VSS_EPLL	R20
	VSS_MPLL	N20
	VSS_VPLL	P20
	VSS_ADC	W11
	VSS_DAC	V6
	VSS_DAC_A	U6
	VSS_HDMI	R7
	VSS_HDMI_OSC	T6
	VSS_HDMI_PLL	P7
	VSS_MIPI	U11, U14
	VSS_UHOST_A	AA15
	VSS_UHOST_AC	AA16
	VSS_UHOST_D	Y14
	VSS_UOTG_A	Y17
	VSS_UOTG_AC	Y15
	VSS_UOTG_D	W17

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3.2 PIN DISCRIPTION

- UART0 / UART1 / UART2 / UART3 / UART AUDIO

Ball Name	Func0		Func1		Func2		Default	Reset
	Signal	IO	Signal	IO	Signal	IO		
XURXD_0	UART_0_RXD	I					GPI	I(L)
XUTXD_0	UART_0_TXD	O					GPI	I(L)
XUCTSN_0	UART_0_CTSn	I					GPI	I(L)
XURTSN_0	UART_0_RTSn	O					GPI	I(L)
XURXD_1	UART_1_RXD	I					GPI	I(L)
XUTXD_1	UART_1_TXD	O					GPI	I(L)
XUCTSN_1	UART_1_CTSn	I					GPI	I(L)
XURTSN_1	UART_1_RTSn	O					GPI	I(L)
XURXD_2	UART_2_RXD	I			UART_AUDIO_RXD	I	GPI	I(L)
XUTXD_2	UART_2_TXD	O			UART_AUDIO_TXD	O	GPI	I(L)
XURXD_3	UART_3_RXD	I	UART_2_CTSn	I			GPI	I(L)
XUTXD_3	UART_3_TXD	O	UART_2_RTSn	O			GPI	I(L)

Signal	I/O	Description
UART_0_RXD	I	UART 0 receives data input
UART_0_TXD	O	UART 0 transmits data output
UART_0_CTSn	I	UART 0 clear to send input signal
UART_0_RTSn	O	UART 0 request to send output signal
UART_1_RXD	I	UART 1 receives data input
UART_1_TXD	O	UART 1 transmits data output
UART_1_CTSn	I	UART 1 clear to send input signal
UART_1_RTSn	O	UART 1 request to send output signal
UART_2_RXD	I	UART 2 receive data input
UART_2_TXD	O	UART 2 transmits data output
UART_3_RXD	I	UART 3 receives data input
UART_3_TXD	O	UART 3 transmits data output
UART_2_CTSn	I	UART 2 clear to send input signal
UART_2_RTSn	O	UART 2 request to send output signal
UART_AUDIO_RXD	I	UART AUDIO receives data input
UART_AUDIO_TXD	O	UART AUDIO transmits data output

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- SPI0 / SPI1

Ball Name	Func0		Func1		Func2		Default	Reset
	Signal	IO	Signal	IO	Signal	IO		
XSPICLK_0	SPI_0_CLK	IO					GPI	I(L)
XSPICSN_0	SPI_0_nSS	IO					GPI	I(L)
XSPIMISO_0	SPI_0_MISO	IO					GPI	I(L)
XSPIMOSI_0	SPI_0_MOSI	IO					GPI	I(L)
XSPICLK_1	SPI_1_CLK	IO					GPI	I(L)
XSPICSN_1	SPI_1_nSS	IO					GPI	I(L)
XSPIMISO_1	SPI_1_MISO	IO					GPI	I(L)
XSPIMOSI_1	SPI_1_MOSI	IO					GPI	I(L)

Signal	I/O	Description
SPI_0_CLK	IO	SPI clock for channel 0
SPI_0_nSS	IO	SPI chip select (only for slave mode) for channel 0
SPI_0_MISO	IO	SPI master input / slave output line for channel 0
SPI_0_MOSI	IO	SPI master output / slave input line for channel 0
SPI_1_CLK	IO	SPI clock for channel 1
SPI_1_nSS	IO	SPI chip select (only for slave mode) for channel 1
SPI_1_MISO	IO	SPI master input / slave output line for channel 1
SPI_1_MOSI	IO	SPI master output / slave input line for channel 1

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- I2S1 / I2S2 / PCM0 / PCM1 / SPDIF / AC97

Ball Name	Func0		Func1		Func2		Default	Reset
	Signal	IO	Signal	IO	Signal	IO		
XI2S1SCLK	I2S_1_SCLK	IO	PCM_1_SCLK	O	AC97BITCLK	I	GPI	I(L)
XI2S1CDCLK	I2S_1_CDCLK	IO	PCM_1_EXTCLK	I	AC97RESETn	O	GPI	I(L)
XI2S1LRCK	I2S_1_LRCK	IO	PCM_1_FSYNC	O	AC97SYNC	O	GPI	I(L)
XI2S1SDI	I2S_1_SDI	I	PCM_1_SIN	I	AC97SDI	I	GPI	I(L)
XI2S1SDO	I2S_1_SDO	O	PCM_1_SOUT	O	AC97SDO	O	GPI	I(L)
XPCM0SCLK	PCM_0_SCLK	O	SPDIF_0_OUT	O	I2S_2_SCLK	IO	GPI	I(L)
XPCM0EXTCLK	PCM_0_EXTCLK	I	SPDIF_EXTCLK	I	I2S_2_CDCLK	IO	GPI	I(L)
XPCM0FSYNC	PCM_0_FSYNC	O	LCD_FRM	O	I2S_2_LRCK	IO	GPI	I(L)
XPCM0SIN	PCM_0_SIN	I			I2S_2_SDI	I	GPI	I(L)
XPCM0SOUT	PCM_0_SOUT	O			I2S_2_SDO	O	GPI	I(L)

Signal	I/O	Description
I2S_1_SCLK	IO	IIS-bus serial clock for channel 1
I2S_1_CDCLK	IO	IIS CODEC system clock for channel 1
I2S_1_LRCK	IO	IIS-bus channel select clock for channel 1
I2S_1_SDI	I	IIS-bus serial data input for channel 1
I2S_1_SDO	O	IIS-bus serial data output for channel 1
PCM_0_SCLK	O	PCM Serial Shift Clock for channel 0
PCM_0_EXTCLK	I	PCM External Clock for channel 0
PCM_0_FSYNC	O	PCM Sync indicating start of word for channel 0
PCM_0_SIN	I	PCM Serial Data Input for channel 0
PCM_0_SOUT	O	PCM Serial Data Output for channel 0
PCM_1_SCLK	O	PCM Serial Shift Clock for channel 1
PCM_1_EXTCLK	I	PCM External Clock for channel 1
PCM_1_FSYNC	O	PCM Sync indicating start of word for channel 1
PCM_1_SIN	I	PCM Serial Data Input for channel 1
PCM_1_SOUT	O	PCM Serial Data Output for channel 1
SPDIF_0_OUT	O	SPDIFOUT data output
SPDIF_EXTCLK	I	SPDIF Global Audio Main Clock Input
LCD_FRM	O	FRM SYNC Signal
AC97BITCLK	I	AC-Link bit clock (12.288 MHz) from AC97 Codec to AC97 Controller
AC97RESETn	O	AC-link Reset to Codec

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Signal	I/O	Description
AC97SYNC	O	AC-link Frame Synchronization (Sampling Frequency 48 Khz) from AC97 Controller to AC97 Codec
AC97SDI	I	AC-link Serial Data input from AC97 Codec
AC97SDO	O	AC-link Serial Data output to AC97 Codec
I2S_2_SCLK	IO	IIS-bus serial clock for channel 2
I2S_2_CDCLK	IO	IIS CODEC system clock for channel 2
I2S_2_LRCK	IO	IIS-bus channel select clock for channel 2
I2S_2_SDI	I	IIS-bus serial data input for channel 2
I2S_2_SDO	O	IIS-bus serial data output for channel 2

- PWM / I2C0

Ball Name	Func0		Func1		Func2		Default	Reset
	Signal	IO	Signal	IO	Signal	IO		
XPWMTOUT_0	TOUT_0	O					GPI	I(L)
XPWMTOUT_1	TOUT_1	O					GPI	I(L)
XPWMTOUT_2	TOUT_2	O					GPI	I(L)
XPWMTOUT_3	TOUT_3	O	PWM_MIE/PWM_MDNIE	O			GPI	I(L)
XI2C0SDA	I2C0_SDA	IO					GPI	I(L)
XI2C0SCL	I2C0_SCL	IO					GPI	I(L)
XI2C1SDA	I2C1_SDA	IO					GPI	I(L)
XI2C1SCL	I2C1_SCL	IO					GPI	I(L)
XI2C2SDA	I2C2_SDA	IO	IEM_SCLK	IO			GPI	I(L)
XI2C2SCL	I2C2_SCL	IO	IEM_SPWI	IO			GPI	I(L)

Signal	I/O	Description
TOUT_0/1/2/3	O	PWM Timer Output
I2C0_SDA	IO	IIC-bus clock for channel 0
I2C0_SCL	IO	IIC-bus data for channel 0
I2C1_SDA	IO	IIC-bus clock for channel 1
I2C1_SCL	IO	IIC-bus data for channel 1
I2C2_SDA	IO	IIC-bus clock for channel 0
I2C2_SCL	IO	IIC-bus data for channel 0
PWM_MIE	O	PWM output from MIE
IEM_SCLK	IO	PWI Clock
IEM_SPWI	IO	PWI Serial data

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- CAMIF A

Ball Name	Func0		Func1		Func2		Default	Reset
	Signal	IO	Signal	IO	Signal	IO		
XCIPCLK	CAM_A_PCLK	I					GPI	I(L)
XCIVSYNC	CAM_A_VSYNC	I					GPI	I(L)
XCIHREF	CAM_A_HREF	I					GPI	I(L)
XCIDATA_0	CAM_A_DATA[0]	I					GPI	I(L)
XCIDATA_1	CAM_A_DATA[1]	I					GPI	I(L)
XCIDATA_2	CAM_A_DATA[2]	I					GPI	I(L)
XCIDATA_3	CAM_A_DATA[3]	I					GPI	I(L)
XCIDATA_4	CAM_A_DATA[4]	I					GPI	I(L)
XCIDATA_5	CAM_A_DATA[5]	I					GPI	I(L)
XCIDATA_6	CAM_A_DATA[6]	I					GPI	I(L)
XCIDATA_7	CAM_A_DATA[7]	I					GPI	I(L)
XCICLKENB	CAM_A_CLKOUT	O					GPI	I(L)
XCIFIELD	CAM_A_FIELD	I					GPI	I(L)

Signal	I/O	Description
CAM_A_PCLK	O	Pixel Clock, driven by the Camera processor A
CAM_A_VSYNC	IO	Vertical Sync, driven by the Camera processor A
CAM_A_HREF	IO	Horizontal Sync, driven by the Camera processor A
CAM_A_DATA[7:0]	IO	Pixel Data for YCbCr in 8-bit mode or for Y in 16-bit mode, driven by the Camera processor A
CAM_A_CLKOUT	IO	Master Clock to the Camera processor A
CAM_A_FIELD	IO	Specifies the Field signal driven by external Camera processor A

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- LCD

Ball Name	Func0		Func1		Func2		Default	Reset
	Signal	IO	Signal	IO	Signal	IO		
XVHSYNC	LCD_HSYNC	O	SYS_CS0	O	VEN_HSYNC	O	GPI	I(L)
XVVSYNC	LCD_VSYNC	O	SYS_CS1	O	VEN_VSYNC	O	GPI	I(L)
XVVDEN	LCD_VDEN	O	SYS_RS	O	VEN_HREF	O	GPI	I(L)
XVVCLK	LCD_VCLK	O	SYS_WE	O	V601_CLK	O	GPI	I(L)
XVVD_0	LCD_VD[0]	O	SYS_VD[0]	IO	VEN_DATA[0]	O	GPI	I(L)
XVVD_1	LCD_VD[1]	O	SYS_VD[1]	IO	VEN_DATA[1]	O	GPI	I(L)
XVVD_2	LCD_VD[2]	O	SYS_VD[2]	IO	VEN_DATA[2]	O	GPI	I(L)
XVVD_3	LCD_VD[3]	O	SYS_VD[3]	IO	VEN_DATA[3]	O	GPI	I(L)
XVVD_4	LCD_VD[4]	O	SYS_VD[4]	IO	VEN_DATA[4]	O	GPI	I(L)
XVVD_5	LCD_VD[5]	O	SYS_VD[5]	IO	VEN_DATA[5]	O	GPI	I(L)
XVVD_6	LCD_VD[6]	O	SYS_VD[6]	IO	VEN_DATA[6]	O	GPI	I(L)
XVVD_7	LCD_VD[7]	O	SYS_VD[7]	IO	VEN_DATA[7]	O	GPI	I(L)
XVVD_8	LCD_VD[8]	O	SYS_VD[8]	IO	V656_DATA[0]	O	GPI	I(L)
XVVD_9	LCD_VD[9]	O	SYS_VD[9]	IO	V656_DATA[1]	O	GPI	I(L)
XVVD_10	LCD_VD[10]	O	SYS_VD[10]	IO	V656_DATA[2]	O	GPI	I(L)
XVVD_11	LCD_VD[11]	O	SYS_VD[11]	IO	V656_DATA[3]	O	GPI	I(L)
XVVD_12	LCD_VD[12]	O	SYS_VD[12]	IO	V656_DATA[4]	O	GPI	I(L)
XVVD_13	LCD_VD[13]	O	SYS_VD[13]	IO	V656_DATA[5]	O	GPI	I(L)
XVVD_14	LCD_VD[14]	O	SYS_VD[14]	IO	V656_DATA[6]	O	GPI	I(L)
XVVD_15	LCD_VD[15]	O	SYS_VD[15]	IO	V656_DATA[7]	O	GPI	I(L)
XVVD_16	LCD_VD[16]	O	SYS_VD[16]	IO			GPI	I(L)
XVVD_17	LCD_VD[17]	O	SYS_VD[17]	IO			GPI	I(L)
XVVD_18	LCD_VD[18]	O	SYS_VD[18]	IO			GPI	I(L)
XVVD_19	LCD_VD[19]	O	SYS_VD[19]	IO			GPI	I(L)
XVVD_20	LCD_VD[20]	O	SYS_VD[20]	IO			GPI	I(L)
XVVD_21	LCD_VD[21]	O	SYS_VD[21]	IO			GPI	I(L)
XVVD_22	LCD_VD[22]	O	SYS_VD[22]	IO			GPI	I(L)
XVVD_23	LCD_VD[23]	O	SYS_VD[23]	IO	V656_CLK	O	GPI	I(L)
XVVSYNC_LDI		O	VSYNC_LDI	O		O	GPI	I(L)
XVSYS_OE		O	SYS_OE	O	VEN_FIELD	O	GPI	I(L)

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Signal	I/O	Description
LCD_HSYNC	O	Horizontal Sync Signal for RGB interface
LCD_VSYNC	O	Vertical Sync Signal for RGB interface
LCD_VDEN	O	Data Enable for RGB interface
LCD_VCLK	O	Video Clock for RGB interface
LCD_VD[23:0]	O	LCD pixel data output for RGB interface
VSYNC_LDI	O	LCD i80 VSYNC Interface
SYS_OE	O	Output Enable for RGB interface
SYS_CS0	O	Chip select LCD0 for LCD Indirect i80 System interface
SYS_CS1	O	Chip select LCD1 for LCD Indirect i80 System interface
SYS_RS	O	Register/ State Select Signal for LCD Indirect i80 System interface
SYS_WE	O	Write Enable for LCD Indirect i80 System interface
SYS_VD[23:0]	IO	Video data input/ output for LCD Indirect i80 System interface
SYS_OE	O	Output Enable for LCD Indirect i80 System interface
VEN_HSYNC	O	Horizontal Sync Signal for 601 interface
VEN_VSYNC	O	Vertical Sync Signal for 601 interface
VEN_HREF	O	Data Enable for 601 interface
V601_CLK	O	Data Clock for 601 interface
VEN_DATA[7:0]	O	YUV422 format data output for 601 interface
V656_DATA[7:0]	O	YUV422 format data output for 656 interface
V656_CLK	O	Data Clock for 656 interface
VEN_FIELD	O	Field Signal for 601 interface

Samsung Confidential

- SDMMC0 / SDMMC1 / SDMMC2 / SDMMC3

Ball Name	Func0		Func1		Func2		Default	Reset
	Signal	IO	Signal	IO	Signal	IO		
XMMC0CLK	SD_0_CLK	O					GPI	I(L)
XMMC0CMD	SD_0_CMD	IO					GPI	I(L)
XMMC0CDN	SD_0_CDn	I					GPI	I(L)
XMMC0DATA_0	SD_0_DATA[0]	IO					GPI	I(L)
XMMC0DATA_1	SD_0_DATA[1]	IO					GPI	I(L)
XMMC0DATA_2	SD_0_DATA[2]	IO					GPI	I(L)
XMMC0DATA_3	SD_0_DATA[3]	IO					GPI	I(L)
XMMC1CLK	SD_1_CLK	O					GPI	I(L)
XMMC1CMD	SD_1_CMD	IO					GPI	I(L)
XMMC1CDN	SD_1_CDn	I					GPI	I(L)
XMMC1DATA_0	SD_1_DATA[0]	IO	SD_0_DATA[4]	IO			GPI	I(L)
XMMC1DATA_1	SD_1_DATA[1]	IO	SD_0_DATA[5]	IO			GPI	I(L)
XMMC1DATA_2	SD_1_DATA[2]	IO	SD_0_DATA[6]	IO			GPI	I(L)
XMMC1DATA_3	SD_1_DATA[3]	IO	SD_0_DATA[7]	IO			GPI	I(L)
XMMC2CLK	SD_2_CLK	O	SPI_2_CLK	IO			GPI	I(L)
XMMC2CMD	SD_2_CMD	IO	SPI_2_nSS	IO			GPI	I(L)
XMMC2CDN	SD_2_CDn	I	SPI_2_MISO	IO			GPI	I(L)
XMMC2DATA_0	SD_2_DATA[0]	IO	SPI_2_MOSI	IO			GPI	I(L)
XMMC2DATA_1	SD_2_DATA[1]	IO					GPI	I(L)
XMMC2DATA_2	SD_2_DATA[2]	IO					GPI	I(L)
XMMC2DATA_3	SD_2_DATA[3]	IO					GPI	I(L)
XMMC3CLK	SD_3_CLK	O					GPI	I(L)
XMMC3CMD	SD_3_CMD	IO					GPI	I(L)
XMMC3CDN	SD_3_CDn	I					GPI	I(L)
XMMC3DATA_0	SD_3_DATA[0]	IO	SD_2_DATA[4]	IO			GPI	I(L)
XMMC3DATA_1	SD_3_DATA[1]	IO	SD_2_DATA[5]	IO			GPI	I(L)
XMMC3DATA_2	SD_3_DATA[2]	IO	SD_2_DATA[6]	IO			GPI	I(L)
XMMC3DATA_3	SD_3_DATA[3]	IO	SD_2_DATA[7]	IO			GPI	I(L)

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Signal	I/O	Description
SD_0_CLK	O	CLOCK (SD/ SDIO/ MMC card interface channel 0)
SD_0_CMD	IO	COMMAND/ RESPONSE (SD/SDIO/ MMC card interface channel 0)
SD_0_CDn	I	CARD DETECT (SD/ SDIO/ MMC card interface channel 0)
SD_0_DATA[3:0]	IO	DATA[3:0] (SD/ SDIO/ MMC card interface channel 0)
SD_1_CLK	O	CLOCK (SD/ SDIO/ MMC card interface channel 1)
SD_1_CMD	IO	COMMAND/RESPONSE (SD/ SDIO/ MMC card interface channel 1)
SD_1_CDn	I	CARD DETECT (SD/ SDIO/ MMC card interface channel 1)
SD_1_DATA[3:0]	IO	DATA[3:0] (SD/ SDIO/ MMC card interface channel 1)
SD_2_CLK	O	CLOCK (SD/ SDIO/ MMC card interface channel 2)
SD_2_CMD	IO	COMMAND/RESPONSE (SD/ SDIO/ MMC card interface channel 2)
SD_2_CDn	I	CARD DETECT (SD/ SDIO/ MMC card interface channel 2)
SD_2_DATA[3:0]	IO	DATA[3:0] (SD/ SDIO/ MMC card interface channel 2)
SD_3_CLK	O	CLOCK (SD/ SDIO/ MMC card interface channel 3)
SD_3_CMD	IO	COMMAND/ RESPONSE (SD/ SDIO/ MMC card interface channel 3)
SD_3_CDn	I	CARD DETECT (SD/ SDIO/ MMC card interface channel 3)
SD_3_DATA[3:0]	IO	DATA[3:0] (SD/ SDIO /MMC card interface channel 3)
SD_0_DATA[7:4]	IO	DATA[7:4] (SD/ SDIO/ MMC card interface channel 0)
SPI_2_CLK	IO	SPI clock for channel 0
SPI_2_nSS	IO	SPI chip select (only for slave mode) for channel 0
SPI_2_MISO	IO	SPI master input / slave output line for channel 0
SPI_2_MOSI	IO	SPI master output / slave input line for channel 0
SD_2_DATA[7:4]	IO	DATA[7:4] (SD/ SDIO/ MMC card interface channel 2)

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- EINT / KEYPAD

Ball Name	Func0		Func1		Func2		Default	Reset
	Signal	IO	Signal	IO	Signal	IO		
XEINT_0		I					GPI	I(L)
XEINT_1		I					GPI	I(L)
XEINT_2		I					GPI	I(L)
XEINT_3		I					GPI	I(L)
XEINT_4		I					GPI	I(L)
XEINT_5		I					GPI	I(L)
XEINT_6		I					GPI	I(L)
XEINT_7		I					GPI	I(L)
XEINT_8		I					GPI	I(L)
XEINT_9		I					GPI	I(L)
XEINT_10		I					GPI	I(L)
XEINT_11		I					GPI	I(L)
XEINT_12		I			HDMI_CEC	IO	GPI	I(L)
XEINT_13		I			HDMI_HPD	I	GPI	I(L)
XEINT_14		I					GPI	I(L)
XEINT_15		I					GPI	I(L)
XEINT_16		I	KP_COL[0]	IO			GPI	I(L)
XEINT_17		I	KP_COL[1]	IO			GPI	I(L)
XEINT_18		I	KP_COL[2]	IO			GPI	I(L)
XEINT_19		I	KP_COL[3]	IO			GPI	I(L)
XEINT_20		I	KP_COL[4]	IO			GPI	I(L)
XEINT_21		I	KP_COL[5]	IO			GPI	I(L)
XEINT_22		I	KP_COL[6]	IO			GPI	I(L)
XEINT_23		I	KP_COL[7]	IO			GPI	I(L)
XEINT_24		I	KP_ROW[0]	I			GPI	I(L)
XEINT_25		I	KP_ROW[1]	I			GPI	I(L)
XEINT_26		I	KP_ROW[2]	I			GPI	I(L)
XEINT_27		I	KP_ROW[3]	I			GPI	I(L)
XEINT_28		I	KP_ROW[4]	I			GPI	I(L)
XEINT_29		I	KP_ROW[5]	I			GPI	I(L)
XEINT_30		I	KP_ROW[6]	I			GPI	I(L)
XEINT_31		I	KP_ROW[7]	I			GPI	I(L)

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Signal	I/O	Description
XEINT[31:0]	I	External interrupts
KP_COL[7:0]	O	KeyIF_Column_data[7:0]
KP_ROW[7:0]	I	KeyIF_Row_data[7:0]
HDMI_CEC	IO	HDMI CEC port
HDMI_HPD	I	HDMI Hot plug

- I2S0 / PCM2

Ball Name	Func0		Func1		Func2		Default	Reset
	Signal	IO	Signal	IO	Signal	IO		
XI2S0SCLK	I2S_0_SCLK	IO	PCM_2_SCLK	O			Func0	O(L)
XI2S0CDCLK	I2S_0_CDCLK	IO	PCM_2_EXTCLK	I			Func0	O(L)
XI2S0LRCK	I2S_0_LRCK	IO	PCM_2_FSYNC	O			Func0	O(L)
XI2S0SDI	I2S_0_SDI	I	PCM_2_SIN	I			Func0	I(L)
XI2S0SDO_0	I2S_0_SDO[0]	O	PCM_2_SOUT	O			Func0	O(L)
XI2S0SDO_1	I2S_0_SDO[1]	O					Func0	O(L)
XI2S0SDO_2	I2S_0_SDO[2]	O					Func0	O(L)

Signal	I/O	Description
I2S_0_SCLK	IO	IIS-bus serial clock for channel 0 (Lower Power Audio)
I2S_0_CDCLK	IO	IIS CODEC system clock for channel 0 (Lower Power Audio)
I2S_0_LRCK	IO	IIS-bus channel select clock for channel 0 (Lower Power Audio)
I2S_0_SDI	I	IIS-bus serial data input for channel 0 (Lower Power Audio)
I2S_0_SDO[2:0]	O	IIS-bus serial data output for channel 0 (Lower Power Audio)
PCM_2_SCLK	O	PCM Serial Shift Clock for channel 2
PCM_2_EXTCLK	I	PCM External Clock for channel 2
PCM_2_FSYNC	O	PCM Sync indicating start of word for channel 2
PCM_2_SIN	I	PCM Serial Data Input for channel 2
PCM_2_SOUT	O	PCM Serial Data Output for channel 2

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- Modem / CAMIF / CFCON / MIPI / KEYPAD / SROM (ADDR16_22)

Pin Name	Func0		Func1		Func2		Func3		Default	Reset
	Signal	IO	Signal	IO	Signal	IO	Signal	IO		
XMSMADDR_0	MSM_ADDR[0]	I	CAM_B_DATA[0]	I	CF_ADDR[0]	O	MIPI_BYTE_CLK	O	GPI	I(L)
XMSMADDR_1	MSM_ADDR[1]	I	CAM_B_DATA[1]	I	CF_ADDR[1]	O	MIPI_ESC_CLK	O	GPI	I(L)
XMSMADDR_2	MSM_ADDR[2]	I	CAM_B_DATA[2]	I	CF_ADDR[2]	O	TS_CLK	I	GPI	I(L)
XMSMADDR_3	MSM_ADDR[3]	I	CAM_B_DATA[3]	I	CF_IORDY	I	TS_SYNC	I	GPI	I(L)
XMSMADDR_4	MSM_ADDR[4]	I	CAM_B_DATA[4]	I	CF_INTRQ	I	TS_VAL	I	GPI	I(L)
XMSMADDR_5	MSM_ADDR[5]	I	CAM_B_DATA[5]	I	CF_DMARQ	I	TS_DATA	I	GPI	I(L)
XMSMADDR_6	MSM_ADDR[6]	I	CAM_B_DATA[6]	I	CF_DRESETN	O	TS_ERROR	I	GPI	I(L)
XMSMADDR_7	MSM_ADDR[7]	I	CAM_B_DATA[7]	I	CF_DMACKN	O			GPI	I(L)
XMSMADDR_8	MSM_ADDR[8]	I	CAM_B_PCLK	I	SROM_ADDR_16to22[0]	O			GPI	I(L)
XMSMADDR_9	MSM_ADDR[9]	I	CAM_B_VSYNC	I	SROM_ADDR_16to22[1]	O			GPI	I(L)
XMSMADDR_10	MSM_ADDR[10]	I	CAM_B_HREF	I	SROM_ADDR_16to22[2]	O			GPI	I(L)
XMSMADDR_11	MSM_ADDR[11]	I	CAM_B_FIELD	I	SROM_ADDR_16to22[3]	O			GPI	I(L)
XMSMADDR_12	MSM_ADDR[12]	I	CAM_B_CLKOUT	O	SROM_ADDR_16to22[4]	O			GPI	I(L)
XMSMADDR_13	MSM_ADDR[13]	I	KP_COL[0]	IO	SROM_ADDR_16to22[5]	O			GPI	I(L)
XMSMDATA_0	MSM_DATA[0]	IO	KP_COL[1]	IO	CF_DATA[0]	IO			GPI	I(L)
XMSMDATA_1	MSM_DATA[1]	IO	KP_COL[2]	IO	CF_DATA[1]	IO			GPI	I(L)
XMSMDATA_2	MSM_DATA[2]	IO	KP_COL[3]	IO	CF_DATA[2]	IO			GPI	I(L)
XMSMDATA_3	MSM_DATA[3]	IO	KP_COL[4]	IO	CF_DATA[3]	IO			GPI	I(L)
XMSMDATA_4	MSM_DATA[4]	IO	KP_COL[5]	IO	CF_DATA[4]	IO			GPI	I(L)

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XMSMDATA_5	MSM_DATA[5]	IO	KP_COL[6]	IO	CF_DATA[5]	IO			GPI	I(L)
XMSMDATA_6	MSM_DATA[6]	IO	KP_COL[7]	IO	CF_DATA[6]	IO			GPI	I(L)
XMSMDATA_7	MSM_DATA[7]	IO	KP_ROW[0]	I	CF_DATA[7]	IO			GPI	I(L)
XMSMDATA_8	MSM_DATA[8]	IO	KP_ROW[1]	I	CF_DATA[8]	IO			GPI	I(L)
XMSMDATA_9	MSM_DATA[9]	IO	KP_ROW[2]	I	CF_DATA[9]	IO			GPI	I(L)
XMSMDATA_10	MSM_DATA[10]	IO	KP_ROW[3]	I	CF_DATA[10]	IO			GPI	I(L)
XMSMDATA_11	MSM_DATA[11]	IO	KP_ROW[4]	I	CF_DATA[11]	IO			GPI	I(L)
XMSMDATA_12	MSM_DATA[12]	IO	KP_ROW[5]	I	CF_DATA[12]	IO			GPI	I(L)
XMSMDATA_13	MSM_DATA[13]	IO	KP_ROW[6]	I	CF_DATA[13]	IO			GPI	I(L)
XMSMDATA_14	MSM_DATA[14]	IO	KP_ROW[7]	I	CF_DATA[14]	IO			GPI	I(L)
XMSMDATA_15	MSM_DATA[15]	IO	KP_ROW[8]	I	CF_DATA[15]	IO			GPI	I(L)
XMSMCSN	MSM_CSn	I	KP_ROW[9]	I	CF_CSn[0]	O			GPI	I(L)
XMSMWEN	MSM_WEn	I	KP_ROW[10]	I	CF_CSn[1]	O			GPI	I(L)
XMSMRN	MSM_Rn	I	KP_ROW[11]	I	CF_IORN	O			GPI	I(L)
XMSMIRQN	MSM_IRQn	O	KP_ROW[12]	I	CF_IOWN	O			GPI	I(L)
XMSMADVN	MSM_ADVN	I	KP_ROW[13]	I	SROM_ADDR_16to22[6]	O			GPI	I(L)

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Signal	I/O	Description
MSM_ADDR[13:0]	I	MODEM (MSM) IF Address (MSM_ADDR[13] should be '0')
MSM_DATA[15:0]	IO	MODEM (MSM) IF Data
MSM_CSn	I	MODEM (MSM) IF Chip Select
MSM_WEn	I	MODEM (MSM) IF Write enable
MSM_Rn	I	MODEM (MSM) IF Read enable
MSM_IRQn	O	MODEM (MSM) IF Interrupt to MODEM
MSM_ADVN	I	MODEM (MSM) IF Address Valid from MODEM Chip
CAM_B_DATA[7:0]	I	Pixel Data driven by the external Video Player
CAM_B_PCLK	I	Pixel Clock, driven by the external Video Player
CAM_B_VSYNC	I	Frame Sync, driven by the external Video Player
CAM_B_HREF	I	Horizontal Sync, driven by the external Video Player
CAM_B_FIELD	I	FIELD signal, driven by the external Video Player
CAM_B_CLKOUT	O	Master Clock to the Camera processor B
KP_COL[7:0]	O	KeyIF_Column_data[7:0]
KP_ROW[13:0]	I	KeyIF_Row_data[13:0]
CF_ADDR[2:0]	O	CF CARD address for ATAPI
CF_IORDY	I	CF Wait signal from CF card
CF_INTRQ	I	CF Interrupt from CF card
CF_DMARQ	I	CF DMA Request
CF_DRESETN	O	CF DMA Reset
CF_DMACKN	O	CF DMA Acknowledge
SROM_ADDR_16to22[6:0]	O	SROM Address bus [22:16]
CF_DATA[15:0]	IO	CF card DATA
CF_CSn[0]	O	CF chip select bank 0
CF_CSn[1]	O	CF chip select bank 1
CF_IORN	O	CF Read strobe for I/O mode
CF_IOWN	O	CF Write strobe for I/O mode
MIPI_BYTE_CLK	O	MIPI BYTE clock for monitoring
MIPI_ESC_CLK	O	MIPI ESC clock for monitoring
TS_CLK	I	TSI system clock, 66MHz
TS_SYNC	I	TSI synchronization control signal
TS_VAL	I	TSI valid signal
TS_DATA	I	TSI input data
TS_ERROR	I	TSI error indicate signal

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- Memory port 0

Pin Name	Func0		Func1		Func2		Func3		Default	Reset
	Signal	IO	Signal	IO	Signal	IO	Signal	IO		
XM0CSN_0	SROM_CSn[0]	O							Func0	O(H)
XM0CSN_1	SROM_CSn[1]	O							Func0	O(H)
XM0CSN_2	SROM_CSn[2]	O	NFCSn[0]	O					Func1	O(H)
XM0CSN_3	SROM_CSn[3]	O	NFCSn[1]	O					Func1	O(H)
XM0CSN_4	SROM_CSn[4]	O	NFCSn[2]	O			ONANDXL_CSn[0]	O	Func3	O(H)
XM0CSN_5	SROM_CSn[5]	O	NFCSn[3]	O			ONANDXL_CSn[1]	O	Func3	O(H)
XM0OEN	EBI_OEn	O							Func0	O(H)
XM0WEN	EBI_WEn	O							Func0	O(H)
XM0BEN_0	EBI_BEn[0]	O							Func0	O(H)
XM0BEN_1	EBI_BEn[1]	O							Func0	O(H)
XM0WAITN	SROM_WAITn	I							Func0	I
XM0DATA_RDN	EBI_DATA_RDn	O							Func0	O(L)
XM0FCLE	NF_CLE	O					ONANDXL_ADDRVALID	O	Func3	O(L)
XM0FALE	NF_ALE	O					ONANDXL_SMCLK	O	Func3	O(L)
XM0FWEN	NF_FWEn	O					ONANDXL_RPn	O	Func3	O(H)
XM0FREN	NF_FREn	O							Func3	O(H)
XM0FRNB_0	NF_RnB[0]	I					ONANDXL_INT[0]	I	Func3	I
XM0FRNB_1	NF_RnB[1]	I					ONANDXL_INT[1]	I	Func3	I
XM0FRNB_2	NF_RnB[2]	I							Func3	I
XM0FRNB_3	NF_RnB[3]	I							Func3	I
XM0ADDR_0	EBI_ADDR[0]	O							Func0	O(L)
XM0ADDR_1	EBI_ADDR[1]	O							Func0	O(L)
XM0ADDR_2	EBI_ADDR[2]	O							Func0	O(L)
XM0ADDR_3	EBI_ADDR[3]	O							Func0	O(L)
XM0ADDR_4	EBI_ADDR[4]	O							Func0	O(L)
XM0ADDR_5	EBI_ADDR[5]	O							Func0	O(L)
XM0ADDR_6	EBI_ADDR[6]	O							Func0	O(L)
XM0ADDR_7	EBI_ADDR[7]	O							Func0	O(L)
XM0ADDR_8	EBI_ADDR[8]	O							Func0	O(L)
XM0ADDR_9	EBI_ADDR[9]	O							Func0	O(L)
XM0ADDR_10	EBI_ADDR[10]	O							Func0	O(L)
XM0ADDR_11	EBI_ADDR[11]	O							Func0	O(L)

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Pin Name	Func0		Func1		Func2		Func3		Default	Reset
	Signal	IO	Signal	IO	Signal	IO	Signal	IO		
XM0ADDR_12	EBI_ADDR[12]	O							Func0	O(L)
XM0ADDR_13	EBI_ADDR[13]	O							Func0	O(L)
XM0ADDR_14	EBI_ADDR[14]	O							Func0	O(L)
XM0ADDR_15	EBI_ADDR[15]	O							Func0	O(L)
XM0DATA_0	EBI_DATA[0]	IO							Func0	O(L)
XM0DATA_1	EBI_DATA[1]	IO							Func0	O(L)
XM0DATA_2	EBI_DATA[2]	IO							Func0	O(L)
XM0DATA_3	EBI_DATA[3]	IO							Func0	O(L)
XM0DATA_4	EBI_DATA[4]	IO							Func0	O(L)
XM0DATA_5	EBI_DATA[5]	IO							Func0	O(L)
XM0DATA_6	EBI_DATA[6]	IO							Func0	O(L)
XM0DATA_7	EBI_DATA[7]	IO							Func0	O(L)
XM0DATA_8	EBI_DATA[8]	IO							Func0	O(L)
XM0DATA_9	EBI_DATA[9]	IO							Func0	O(L)
XM0DATA_10	EBI_DATA[10]	IO							Func0	O(L)
XM0DATA_11	EBI_DATA[11]	IO							Func0	O(L)
XM0DATA_12	EBI_DATA[12]	IO							Func0	O(L)
XM0DATA_13	EBI_DATA[13]	IO							Func0	O(L)
XM0DATA_14	EBI_DATA[14]	IO							Func0	O(L)
XM0DATA_15	EBI_DATA[15]	IO							Func0	O(L)

Signal	I/O	Description
SROM_CSn[5:4]	O	Memory Port 0 SROM Chip select support up to 2 memory bank
SROM_CSn[3:2]	O	Memory Port 0 SROM Chip select support up to 2 memory bank
SROM_CSn[1:0]	O	Memory Port 0 SROM Chip select support up to 2 memory bank
EBI_OEn	O	Memory Port 0 SROM / OneNAND Output Enable
EBI_WEn	O	Memory Port 0 SROM / OneNAND Write Enable
EBI_BEn[1:0]	O	Memory Port 0 SROM Byte Enable
SROM_WAITn	I	Memory Port 0 SROM nWait
EBI_DATA_RDn	O	Memory Port 0 SROM/OneNAND/NAND/CF Output Enable
NF_CLE	O	Memory Port 0 NAND Command Latch Enable
NF_ALE	O	Memory Port 0 NAND Address Latch Enable
NF_FWEn	O	Memory Port 0 NAND Flash Write Enable
NF_FREn	O	Memory Port 0 NAND Flash Read Enalbe
NF_RnB[3:0]	I	Memory Port 0 NAND Flash Ready/Busy

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Signal	I/O	Description
EBI_ADDR[15:0]	O	Memory port 0 Address bus
EBI_DATA[15:0]	IO	Memory port 0 Data bus
NFCSn[0]	O	Memory Port 0 NAND Chip Select bank 0
NFCSn[1]	O	Memory Port 0 NAND Chip Select bank 1
NFCSn[2]	O	Memory Port 0 NAND Chip Select bank 2
NFCSn[3]	O	Memory Port 0 NAND Chip Select bank 3
ONANDXL_ADDRVALID	O	OneNANDXL Flash Address valid
ONANDXL_SMCLK	O	OneNANDXL Flash clock
ONANDXL_RPn	O	OneNANDXL Flash reset
ONANDXL_INT[1:0]	I	OneNANDXL Flash Interrupt signal from OneNAND Device

- Memory port 1 (Dedicated)

Ball Name	I/O	Description
XM1ADDR_0 ~ XM1ADDR_15	O	Memory port 1DRAM Address bus (16bit)
XM1DATA_0 ~XM1DATA_31	IO	Memory port 1DRAM Data bus.(32bit)
XM1DQS_0 ~XM1DQS_3	IO	Memory port 1DRAM Data Strobe (4bit)
XM1DQSn_0 ~XM1DQSn_3	IO	Memory port 1DRAM Data Differential Strobe neg (4bit)
XM1DQM_0 ~XM1DQM_3	O	Memory port 1DRAM Data Mask (4bit)
XM1CKE_0 ~XM1CKE_1	O	Memory port 1DRAM Clock Enable (2bit)
XM1SCLK	O	Memory port 1DRAM Clock
XM1nSCLK	O	Memory port 1DRAM Inverted Clock of Xm1SCLK
XM1CSn_0 ~XM1CSn_1	O	Memory port 1DRAM Chip Select support up to 2 memory bank (2bit)
XM1RASn	O	Memory port 1DRAM Row Address Strobe
XM1CASn	O	Memory port 1DRAM Column Address Strobe
XM1WEn	O	Memory port 1DRAM Write Enable

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- Memory port 2 (Dedicated)

Ball Name	I/O	Description
XM2ADDR_0 ~XM2ADDR_15	O	Memory port 2DRAM Address bus (16bit)
XM2DATA_0 ~XM2DATA_31	IO	Memory port 2DRAM Data bus (32bit)
XM2DQS_0 ~XM2DQS_3	IO	Memory port 2DRAM Data Strobe (4bit)
XM2DQSn_0 ~XM2DQSn_3	IO	Memory port 2DRAM Data Differential Strobe neg (4bit)
XM2DQM_0 ~XM2DQM_3	O	Memory port 2DRAM Data Mask (4bit)
XM2CKE_0 ~XM2CKE_1	O	Memory port 2DRAM Clock Enable (2bit)
XM2SCLK	O	Memory port 2DRAM Clock
XM2nSCLK	O	Memory port 2DRAM Inverted Clock of Xm2SCLK
XM2CSn_0 ~XM2CSn_1	O	Memory port 2DRAM Chip Select support up to 2 memory bank (2bit)
XM2RASn	O	Memory port 2DRAM Row Address Strobe
XM2CASn	O	Memory port 2DRAM Column Address Strobe
XM2WEn	O	Memory port 2DRAM Write Enable

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- JTAG (Dedicated)

Ball Name	I/O	Description
XJTRSTN	I	XjTRSTn (TAP Controller Reset) resets the TAP controller at start. If debugger (black ICE) is not used, XjTRSTn pin must be at L or low active pulse. Pull-down resistor is connected.
XJTMS	I	XjTMS (TAP Controller Mode Select) controls the sequence of the TAP controller's states. Pull-up resistor is connected.
XJTCK	I	XjTCK (TAP Controller Clock) provides the clock input for the JTAG logic. Pull-down resistor is connected.
XJTDI	I	XjTDI (TAP Controller Data Input) is the serial input for test instructions and data. Pull-up resistor is connected.
XJTDO	O	XjTDO (TAP Controller Data Output) is the serial output for test instructions and data.
XJDBGSEL	I	JTAG selection. 0: CORTEXA8 Core JTAG, 1: Peripherals JTAG

- RESET / etc (Dedicated)

Ball Name	I/O	Description
XOM_0 ~ XOM_5	I	Operating Mode control signals (6-bit)
XDDR2SEL	I	Selection DDR type (LPDDR1/2 or DDR2). 0: LPDDR1, 1: LPDDR2/DDR2
XPWRRGTON	O	Power Regulator enable
XNRESET	I	System Reset
XCLKOUT	O	Clock out signal
XNRSTOUT	O	For External device reset control
XNWRESET	I	System Warm Reset.
XRTCCLKO	O	RTC Clock out

- Clock (Dedicated)

Ball Name	I/O	Description
XRTCXTI	I	32 KHz crystal input for RTC
XRTCXTO	O	32 KHz crystal output for RTC
XXTI	I	Crystal Input for internal osc circuit
XXTO	O	Crystal output for internal osc circuit.
XUSBXTI	I	Crystal Input for internal USB circuit
XUSBXTO	O	Crystal output for internal USB circuit

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- ADC/ DAC / HDMI/ MIPI (Dedicated)

Ball Name	I/O	Description
XADCAIN_0 ~XADCAIN_9	I	ADC Analog Input (10-bit)
XDACOUT	O	Analog output of DAC
XDACIREF	I	External resistor connection
XDACVREF	I	Reference voltage input
XDACCOMP	O	External capacitor connection
XHDMITX0P	O	HDMI Phy TX0 P
XHDMITX0N	O	HDMI Phy TX0 N
XHDMITX1P	O	HDMI Phy TX1 P
XHDMITX1N	O	HDMI Phy TX1 N
XHDMITX2P	O	HDMI Phy TX2 P
XHDMITX2N	O	HDMI Phy TX2 N
XHDMITXCP	O	HDMI Phy TX Clock P
XHDMITXCN	O	HDMI Phy TX Clock N
XHDMIREXT	I	HDMI Phy Registance
XHDMIXTI	I	HDMI crystal input
XHDMIXTO	O	HDMI crystal output
XMIPIMDP0	IO	Master DATA LANE0 DP for MIPI-DPHY
XMIPIMDP1	IO	Master DATA LANE1 DP for MIPI-DPHY
XMIPIMDP2	IO	Master DATA LANE2 DP for MIPI-DPHY
XMIPIMDP3	IO	Master DATA LANE3 DP for MIPI-DPHY
XMIPIMDN0	IO	Master DATA LANE0 DN for MIPI-DPHY
XMIPIMDN1	IO	Master DATA LANE1 DN for MIPI-DPHY
XMIPIMDN2	IO	Master DATA LANE2 DN for MIPI-DPHY
XMIPIMDN3	IO	Master DATA LANE3 DN for MIPI-DPHY
XMIPISDP0	IO	Slave DATA LANE0 DP for MIPI-DPHY
XMIPISDP1	IO	Slave DATA LANE1 DP for MIPI-DPHY
XMIPISDP2	IO	Slave DATA LANE2 DP for MIPI-DPHY
XMIPISDP3	IO	Slave DATA LANE3 DP for MIPI-DPHY
XMIPISDN0	IO	Slave DATA LANE0 DN for MIPI-DPHY
XMIPISDN1	IO	Slave DATA LANE1 DN for MIPI-DPHY
XMIPISDN2	IO	Slave DATA LANE2 DN for MIPI-DPHY
XMIPISDN3	IO	Slave DATA LANE3 DN for MIPI-DPHY
XMIPIMDPCLK	IO	Master CLK Lane DP for MIPI-DPHY

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XMIPIMDNCLK	IO	Master CLK Lane DN for MIPI-DPHY
XMIPISDPCLK	IO	Slave CLK Lane DP for MIPI-DPHY
XMIPISDNCLK	IO	Slave CLK Lane DN for MIPI-DPHY
XMIPIVREG_0P4V	IO	Regulator capacitor for MIPI-DPHY

- USB OTG / USB HOST 1.1 (Dedicated)

Ball Name	I/O	Description
XUOTGDRVVUBS	O	USB OTG charge pump enable
XUHOSTPWREN	O	USB HOST charge pump enable
XUHOSTOVERCUR	I	USB HOST over current flag
XUOTGDP	IO	USB OTG Data pin DATA(+)
XUOTGREXT	IO	USB OTG External 44.2ohm (+/- 1%) resistor connection
XUOTGDM	IO	USB OTG Data pin DATA(-)
XUHOSTDP	IO	USB HOST Data pin DATA(+)
XUHOSTREXT	IO	USB HOST External 44.2ohm (+/- 1%) resistor connection
XUHOSTDM	IO	USB HOST Data pin DATA(-)
XUOTGID	IO	USB OTG Mini-Receptacle Identifier
XUOTGVBUS	IO	USB OTG Mini-Receptacle Vbus

- E-fuse (Dedicated)

Ball Name	I/O	Description
XEFFSOURCE_0	I	Power PAD for efuse ROM's FSOURCE

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3.2.1 POWER DOMAIN

- Analog IO Power

Power Domain		Ball Name	Ball No.
Analog IO	ADC	XADCAIN_0	AC11
		XADCAIN_1	AC12
		XADCAIN_2	AB11
		XADCAIN_3	AC10
		XADCAIN_4	Y11
		XADCAIN_5	W12
		XADCAIN_6	Y12
		XADCAIN_7	AA12
		XADCAIN_8	AA11
		XADCAIN_9	AB12
		VDD_ADC	W10
		VSS_ADC	W11
	DAC	XDACCOMP	V4
		XDACIREF	W5
		XDACOUT	U5
		XDACVREF	V5
		VDD_DAC_A	U7
		VSS_DAC_A	U6
		VDD_DAC	V7
		VSS_DAC	V6
	MIPI DPHY	XMIPIMDN0	AD17
		XMIPIMDN1	AD16
		XMIPIMDN2	AD14
		XMIPIMDN3	AD13
		XMIPIMDNCLK	AD15
		XMIPIMDP0	AE17
		XMIPIMDP1	AE16
		XMIPIMDP2	AE14
		XMIPIMDP3	AE13
		XMIPIMDPCLK	AE15
		XMIPISDN0	AE12
		XMIPISDN1	AE11
		XMIPISDN2	AE9
		XMIPISDN3	AE8
		XMIPISDNCLK	AE10

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Power Domain		Ball Name	Ball No.
		XMIPISDP0	AD12
		XMIPISDP1	AD11
		XMIPISDP2	AD9
		XMIPISDP3	AD8
		XMIPISDPCLK	AD10
		XMIPIVREG_0P4V	AC15
		VDD_MIPI_A	Y13
		VDD_MIPI_D	U12, U13
		VDD_MIPI_PLL	W14
		VSS_MIPI	U11, U14
	HDMI PHY	XHDMIREXT	W1
		XHDMITX0N	T1
		XHDMITX0P	T2
		XHDMITX1N	U1
		XHDMITX1P	U2
		XHDMITX2N	V1
		XHDMITX2P	V2
		XHDMITXCN	R1
		XHDMITXCP	R2
		XHDMIXTI	Y2
		XHDMIXTO	Y1
		VDD_HDMI	P6
		VDD_HDMI_PLL	R6
		VDD_HDMI_OSC	T7
		VSS_HDMI	R7
		VSS_HDMI_PLL	P7
		VSS_HDMI_OSC	T6
	USB OTG	XUOTGDM	AE21
		XUOTGDP	AD21
		XUOTGID	AD18
		XUOTGREXT	AE18
		XUOTGVBUS	AC18
		VDD_UOTG_A	W16
		VDD_UOTG_D	U15
		VSS_UOTG_A	Y17
		VSS_UOTG_AC	Y15
		VSS_UOTG_D	W17

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Power Domain		Ball Name	Ball No.
	USB HOST	XUHOSTDM	AD19
		XUHOSTDP	AE19
		XUHOSTREXT	AC17
		VDD_UHOST_A	Y16
		VDD_UHOST_D	W13
		VSS_UHOST_A	AA15
		VSS_UHOST_AC	AA16
		VSS_UHOST_D	Y14
	APLL	VDD_APLL	M20
		VSS_APLL	M19
	MPLL	VDD_MPLL	N20
		VSS_MPLL	N19
	VPLL	VDD_VPLL	P20
		VSS_VPLL	P19
	EPLL	VDD_EPLL	R20
		VSS_EPLL	R19

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- Digital IO Power

Power Domain		Ball Name	Ball No.
Digital IO	MDDR port 2	VDD_M2	J17, K17, L17, M17
	MDDR port 1	VDD_M1	J13, J14, J15, J16
	OneNAND(EBI)	XM0ADDR_0	K5
		XM0ADDR_1	L7
		XM0ADDR_10	J3
		XM0ADDR_11	K7
		XM0ADDR_12	H6
		XM0ADDR_13	G5
		XM0ADDR_14	F4
		XM0ADDR_15	H3
		XM0ADDR_2	J4
		XM0ADDR_3	H5
		XM0ADDR_4	J6
		XM0ADDR_5	K4
		XM0ADDR_6	K6
		XM0ADDR_7	J5
		XM0ADDR_8	H4
		XM0ADDR_9	G4
		XM0BEN_0	T3
		XM0BEN_1	N6
		XM0CSN_0	U3
		XM0CSN_1	T4
		XM0CSN_2	J1
		XM0CSN_3	N9
		XM0CSN_4	N3
		XM0CSN_5	N7
		XM0DATA_0	K3
		XM0DATA_1	L3
		XM0DATA_10	L4
		XM0DATA_11	M1
		XM0DATA_12	M3
		XM0DATA_13	M5
		XM0DATA_14	N5
		XM0DATA_15	P2
		XM0DATA_2	L5

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Power Domain		Ball Name	Ball No.
		XM0DATA_3	M4
		XM0DATA_4	N1
		XM0DATA_5	N2
		XM0DATA_6	P1
		XM0DATA_7	N4
		XM0DATA_8	L1
		XM0DATA_9	L2
		XM0DATA_RDN	M7
		XM0FALE	K2
		XM0FCLE	K1
		XM0FREN	M2
		XM0FRNB_0	R3
		XM0FRNB_1	M6
		XM0FRNB_2	V3
		XM0FRNB_3	L6
		XM0FWEN	J2
		XM0OEN	R4
		XM0WAITN	W2
		XM0WEN	P4
		VDD_M0	K9, M9
	LCD	XVHSYNC	AA13
		XVSYS_OE	AE4
		XVVCLK	AA10
		XVVD_0	AA9
		XVVD_1	AB9
		XVVD_10	AE6
		XVVD_11	AC8
		XVVD_12	Y8
		XVVD_13	AC7
		XVVD_14	AD6
		XVVD_15	AE5
		XVVD_16	AD7
		XVVD_17	AA7
		XVVD_18	AD5
		XVVD_19	AA6
		XVVD_2	AB8
		XVVD_20	AB5

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Power Domain		Ball Name	Ball No.
		XVVD_21	AC5
		XVVD_22	AC6
		XVVD_23	Y7
		XVVD_3	AB7
		XVVD_4	Y9
		XVVD_5	AB6
		XVVD_6	AE7
		XVVD_7	AC9
		XVVD_8	AA8
		XVVD_9	W9
		XVVDEN	AB10
		XVVSYNC	Y10
		XVVSYNC_LDI	W8
		VDD_LCD	U10
	CAMERA	XCICLKENB	AA18
		XCIDATA_0	AB15
		XCIDATA_1	AB16
		XCIDATA_2	AB20
		XCIDATA_3	AA19
		XCIDATA_4	AB21
		XCIDATA_5	Y18
		XCIDATA_6	AB17
		XCIDATA_7	AA17
		XCIFIELD	AB19
		XCIHREF	AB14
		XCIPCLK	AC21
		XCIVSYNC	AA14
		VDD_CAM	V19
	AUDIO	XI2S0CDCLK	AC4
		XI2S0LRCK	AE3
		XI2S0SCLK	AD2
		XI2S0SDI	AE2
		XI2S0SDO_0	AD3
		XI2S0SDO_1	AC3
		XI2S0SDO_2	AA3
		XI2S1CDCLK	AB3
		XI2S1LRCK	AC2

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Power Domain		Ball Name	Ball No.
		XI2S1SCLK	AD1
		XI2S1SDI	AA5
		XI2S1SDO	AB4
		XPCM0EXTCLK	AA1
		XPCM0FSYNC	AB1
		XPCM0SCLK	AA2
		XPCM0SIN	AB2
		XPCM0SOUT	AC1
		XCLKOUT	AE24
		VDD_AUD	U9, U19
	MODEM	XMSMADDR_0	H1
		XMSMADDR_1	G6
		XMSMADDR_10	F1
		XMSMADDR_11	G3
		XMSMADDR_12	E5
		XMSMADDR_13	F2
		XMSMADDR_2	E4
		XMSMADDR_3	H7
		XMSMADDR_4	G1
		XMSMADDR_5	H2
		XMSMADDR_6	F5
		XMSMADDR_7	D5
		XMSMADDR_8	F6
		XMSMADDR_9	G2
		XMSMADVN	A4
		XMSMCSN	G8
		XMSMDATA_0	F3
		XMSMDATA_1	E2
		XMSMDATA_10	B1
		XMSMDATA_11	C3
		XMSMDATA_12	C4
		XMSMDATA_13	B2
		XMSMDATA_14	B3
		XMSMDATA_15	A2
		XMSMDATA_2	E1
		XMSMDATA_3	D3
		XMSMDATA_4	D1

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Power Domain		Ball Name	Ball No.
		XMSMDATA_5	E3
		XMSMDATA_6	D2
		XMSMDATA_7	C1
		XMSMDATA_8	C2
		XMSMDATA_9	D4
		XMSMIRQN	A3
		XMSMRN	G9
		XMSMWEN	B4
		VDD_MODEM	J7
	KEY	XEINT_16	U20
		XEINT_17	Y23
		XEINT_18	V21
		XEINT_19	AB24
		XEINT_20	AA21
		XEINT_21	AA23
		XEINT_22	AC25
		XEINT_23	Y20
		XEINT_24	AC24
		XEINT_25	AB22
		XEINT_26	AD25
		XEINT_27	Y22
		XEINT_28	AD24
		XEINT_29	AA20
		XEINT_30	Y19
		XEINT_31	AB23
		VDD_KEY	T17
	System 0	XXTI	U24
		XXTO	U25
		XOM_0	T23
		XOM_1	T22
		XOM_2	V23
		XOM_3	U21
		XOM_4	V25
		XOM_5	V24
		XPWRRGTON	U22
		XNRESET	U23
		XNRSTOUT	T20

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Power Domain		Ball Name	Ball No.
		XNWRESET	T21
		XEINT_0	Y21
		XEINT_1	W25
		XEINT_2	W23
		XEINT_3	Y25
		XEINT_4	AA22
		XEINT_5	W24
		XEINT_6	W21
		XEINT_7	AA25
		XUOTGDRVVBUS	AC19
		XUHOSTPWREN	AD23
		XUHOSTOVERCUR	AC22
		XDDR2SEL	AB18
		XUSBXTI	AD20
		XUSBXTO	AE20
		XJTRSTN	P5
		XJTMS	R5
		XJTCK	U4
		XJTDI	T5
		XJTDO	W3
		XJDBGSEL	P3
		VDD_SYS0	P9, U16, U17
	System 1	XEINT_8	V20
		XEINT_9	V22
		XEINT_10	Y24
		XEINT_11	W22
		XEINT_12	AA24
		XEINT_13	AC23
		XEINT_14	AB25
		XEINT_15	W20
		VDD_SYS1	T19
	External Peri 0	XMMC0CDN	F7
		XMMC0CLK	B5
		XMMC0CMD	E6
		XMMC0DATA_0	C5
		XMMC0DATA_1	A5
		XMMC0DATA_2	D6

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Power Domain		Ball Name	Ball No.
		XMMC0DATA_3	C6
		XMMC1CDN	C7
		XMMC1CLK	B6
		XMMC1CMD	F8
		XMMC1DATA_0	D7
		XMMC1DATA_1	E7
		XMMC1DATA_2	A6
		XMMC1DATA_3	F9
		XSPICLK_0	B7
		XSPICSN_0	E9
		XSPIMISO_0	J9
		XSPIMOSI_0	J11
		XURXD_0	C8
		XUTXD_0	D8
		XUCTSN_0	D9
		XURTSN_0	A7
		XURXD_1	G10
		XUTXD_1	F10
		XUCTSN_1	B8
		XURTSN_1	E10
		XI2C0SDA	F11
		XI2C0SCL	C9
		XPWMTOUT_0	E8
		XPWMTOUT_1	B9
		XPWMTOUT_2	A8
		XPWMTOUT_3	F12
		VDD_EXT0	J10
	External Peri 1	XMMC2CDN	AA4
		XMMC2CLK	Y6
		XMMC2CMD	W6
		XMMC2DATA_0	Y4
		XMMC2DATA_1	Y5
		XMMC2DATA_2	Y3
		XMMC2DATA_3	W4
		XI2C1SCL	AD22
		XI2C1SDA	AE23
		XI2C2SCL	AE22

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Power Domain		Ball Name	Ball No.
		XI2C2SDA	AC16
		XURXD_2	AC20
		XUTXD_2	AC14
		XURXD_3	AC13
		XUTXD_3	AB13
		VDD_EXT1	T9, W18
	External Peri 2	XMMC3CDN	E11
		XMMC3CLK	A9
		XMMC3CMD	D10
		XMMC3DATA_0	B10
		XMMC3DATA_1	C10
		XMMC3DATA_2	D11
		XMMC3DATA_3	A10
		XSPICLK_1	G12
		XSPICSN_1	B11
		XSPIMISO_1	G13
		XSPIMOSI_1	A11
		VDD_EXT2	G11
	RTC Clock Out	XRTCCLKO	R22
		VDD_CKO	P17
	RTC	XRTCXTI	T24
		XRTCXTO	T25
		VDD_RTC	P21
	EFUSE(Security)	XEFFSOURCE_0	AD4

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- Internal Power

Power Domain		Ball Name	Ball No.
Internal	Internal Logic	VDD_INT	K13, K14, K15, L10, L11, M11, N10, N11, P11, R11, R12, R13, T11
	ARM (Cortex-A8)	VDD_ARM	L13, L14, L15, M13, M14, M15, N14, N15, N16, P14, P15
	Alive	VDD_ALIVE	R17, W15

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- Common GND

Power Domain		Ball Name	Ball No.
Common GND	Internal Logic, Digital IO	VSS	A1, A25, AE1, AE25, G19, G7, J12, K10, K11, K12, K16, K19, L12, L16, L9, M10, M12, M16, M19, N12, N17, N19, P10, P12, P13, P16, P19, R10, R14, R15, R16, R19, R9, T10, T12, T13, T14, T15, T16, W19, W7
	Analog IO	VSS_APLL	M20
		VSS_EPLL	R20
		VSS_MPLL	N20
		VSS_VPLL	P20
		VSS_ADC	W11
		VSS_DAC	V6
		VSS_DAC_A	U6
		VSS_HDMI	R7
		VSS_HDMI_OSC	T6
		VSS_HDMI_PLL	P7
		VSS_MIPI	U11, U14
		VSS_UHOST_A	AA15
		VSS_UHOST_AC	AA16
		VSS_UHOST_D	Y14
		VSS_UOTG_A	Y17
		VSS_UOTG_AC	Y15
		VSS_UOTG_D	W17

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3.2.2 PACKAGE DIMENSION

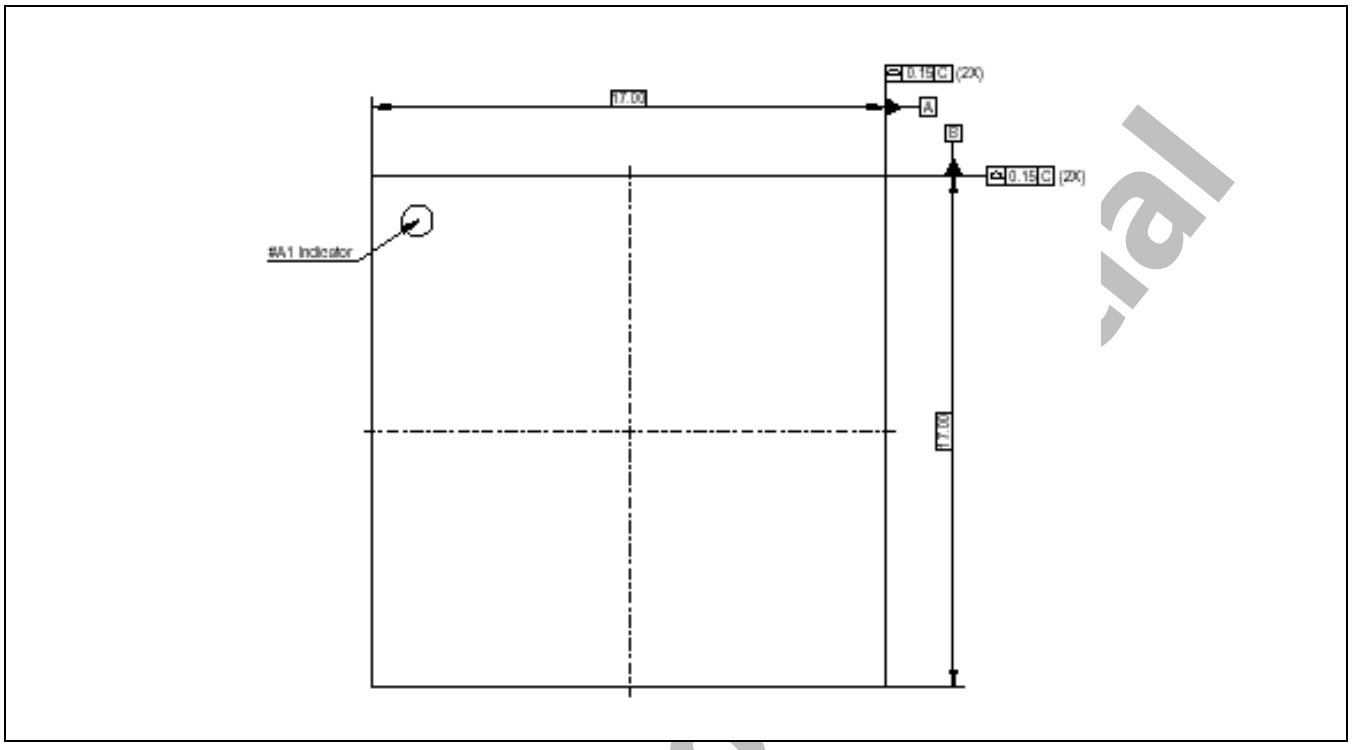

Figure 3-2 S5PV210 Package Dimension (584-FCFBGA) – Top View

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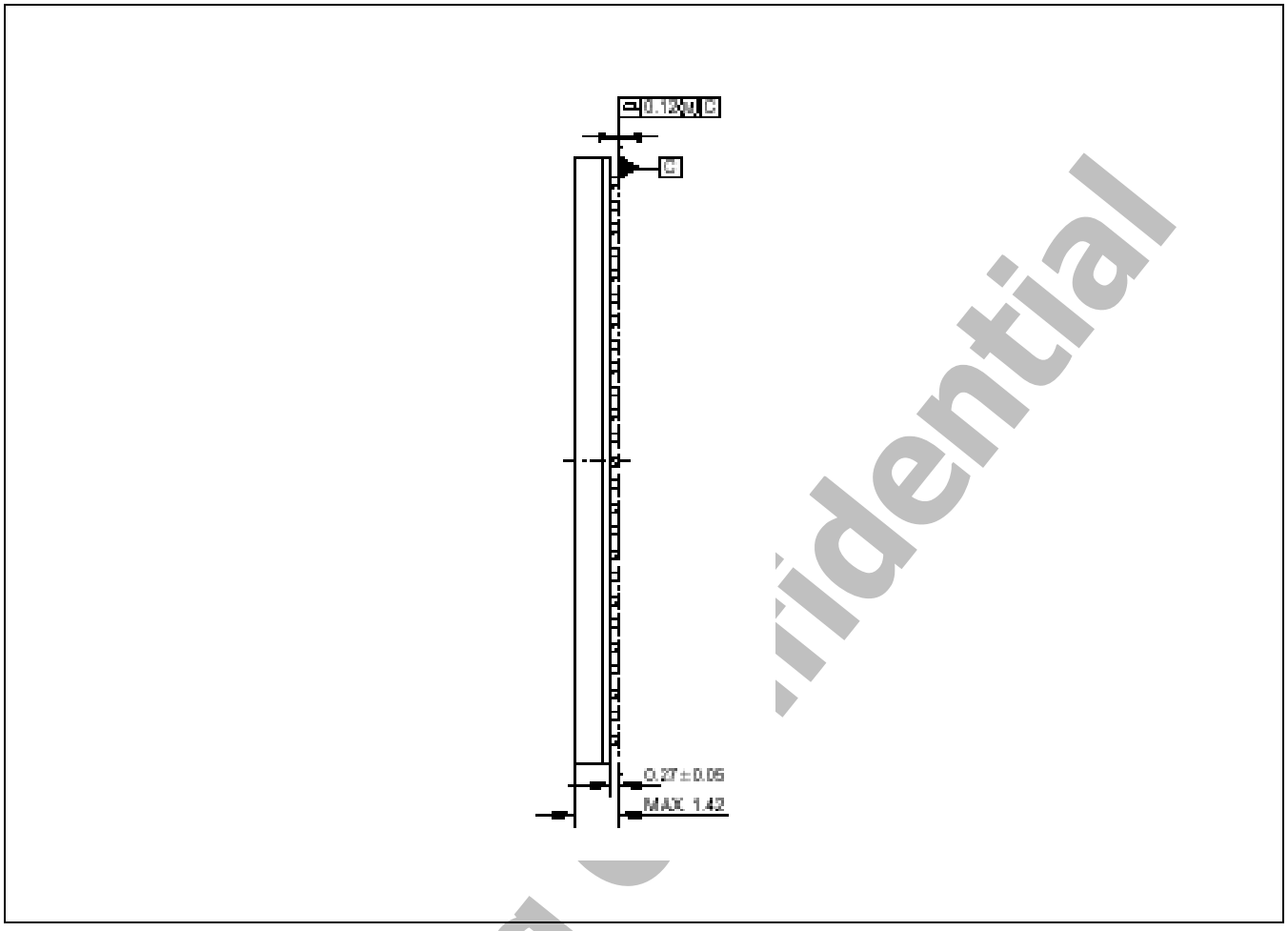

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Section 2

SYSTEM

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1 CHIP ID

1.1 OVERVIEW OF CHIP ID

The S5PV210 includes a Chip ID block for the software (SW) that sends and receives APB interface signals to the bus system. Chip ID is placed on the first address of the SFR region (0xE000_0000).

The product ID register supplies product ID, revision number and device ID.

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1.2 REGISTER DESCRIPTION

1.2.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
PRO_ID	0xE000_0000	R	Product information	0x43110020

1.2.1.1 Product ID Register (PRO_ID, R, Address = 0xE000_0000)

PRO_ID	Bit	Description	Initial State
Product ID	[31:12]	Product ID The product ID allocated to S5PV210 is “0x43110”	0x43110
Reserved	[11:8]	Reserved bits	-
Rev. Number	[7:4]	Revision Number	0x2
Device ID	[3:0]	Device ID 000 = V210 001 = C110 010 = C111 Others = reserved	0x0

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2 GENERAL PURPOSE INPUT/ OUTPUT

This chapter describes the General Purpose Input/ Output (GPIO).

2.1 OVERVIEW

S5PV210 includes 237 multi-functional input/ output port pins and 142 memory port pins. There are 34 general port groups and 2 memory port groups as listed below:

- GPA0: 8 in/out port - 2xUART with flow control
- GPA1: 4 in/out port - 2xUART without flow control or 1xUART with flow control
- GPB: 8 in/out port - 2x SPI
- GPC0: 5 in/out port - I2S, PCM, AC97
- GPC1: 5 in/out port - I2S, SPDIF, LCD_FRM
- GPD0: 4 in/out port - PWM
- GPD1: 6 in/out port - 3xI2C, PWM, IEM
- GPE0,1: 13 in/out port - Camera I/F
- GPF0,1,2,3: 30 in/out port - LCD I/F
- GPG0,1,2,3: 28 in/out port - 4xMMC channel (Channel 0 and 2 support 4-bit and 8-bit mode, but channel 1, and channel 3 support only 4-bit mode)
- GPH0,1,2,3: 32 in/out port - Key pad, External Wake-up (up-to 32-bit). (GPH* groups are in Alive region)
- GPI: Low Power I2S, PCM (in/out port is not used), PDN configuration for power down is controlled by AUDIO_SS PDN Register.
- GPJ0,1,2,3,4: 35 in/out port - Modem IF, CAMIF, CFCON, KEYPAD, SROM ADDR[22:16]
- MP0_1,2,3: 20 in/out port - Control signals of EBI (SROM, NF, OneNAND)
- MP0_4,5,6,7: 32 in/out memory port - EBI (For more information about EBI configuration, refer to Chapter 5, and 6)
- MP1_0~8: 71 DRAM1 ports (in/out port is not used)
- MP2_0~8: 71 DRAM2 ports (in/out port is not used)
- ETC0, ETC1, ETC2, ETC4: 28 in/out ETC ports - JTAG, Operating Mode, RESET, CLOCK (ETC3 is reserved)

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2.1.1 FEATURES

The key features of GPIO include:

- Controls 146 GPIO Interrupts
- Controls 32 External Interrupts
- 237 multi-functional input / output ports
- Controls pin states in Sleep Mode except GPH0, GPH1, GPH2, and GPH3 (GPH* pins are alive-pads)

2.1.2 INPUT/ OUTPUT CONFIGURATION

Configurable Input/ Output (I/O) is subdivided into Type A and Type B.

2.1.3 S5PV210 INPUT/ OUTPUT TYPES

I/O Types	I/O Group	Description
A	GPA0, GPA1, GPC0, GPC1, GPD0, GPD1, GPE0, GPE1, GPF0, GPF1, GPF2, GPF3, GPH0, GPH1, GPH2, GPH3, GPI, GPJ0, GPJ1, GPJ2, GPJ3, GPJ4	Normal I/O (3.3V I/O)
B	GPB, GPG0, GPG1, GPG2, GPG3, MP0	Fast I/O (3.3V I/O)
C	MP1, MP2	DRAM I/O (1.8V IO)

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2.1.4 IO DRIVER STRENGTH

2.1.4.1 Type A IO Driver Strength

(VDD=3.3V±0.3V)

Parameter			Currents		
Driver Type			Worst VDD=3.00V T=125℃ Process=Slow Isink at VDD*0.2V Isource at VDD*0.8V	Typical VDD=3.30V T=25℃ Process=Nominal Isink at VDD*0.2V Isource at VDD*0.8V	Best VDD=3.60V T=-40℃ Process=Fast Isink at VDD*0.2V Isource at VDD*0.8V
3.3V IO	DS0=0,DS1=0	Isink	7.005 mA	11.19 mA	15.92 mA
		Isource	-7.103 mA	-10.88 mA	-15.63 mA
	DS0=0,DS1=1	Isink	11.69 mA	18.67 mA	26.54 mA
		Isource	-11.37 mA	-17.42 mA	-25.02 mA
	DS0=1,DS1=0	Isink	16.35 mA	26.12 mA	37.15 mA
		Isource	-17.06 mA	-26.14 mA	-37.53 mA
	DS0=1,DS1=1	Isink	30.38 mA	48.52 mA	69.01 mA
		Isource	-28.44 mA	-43.56 mA	-62.55 mA

(VDD=2.5V±0.2V)

Parameter			Currents		
Driver Type			Worst VDD=2.30V T=125℃ Process=Slow Isink at VDD*0.2V Isource at VDD*0.8V	Typical VDD=2.50V T=25℃ Process=Nominal Isink at VDD*0.2V Isource at VDD*0.8V	Best VDD=2.70V T=-40℃ Process=Fast Isink at VDD*0.2V Isource at VDD*0.8V
3.3V IO	DS0=0,DS1=0	Isink	4.497 mA	7.461 mA	11.12 mA
		Isource	-4.405 mA	-6.993 mA	-10.42 mA
	DS0=0,DS1=1	Isink	7.501 mA	12.44 mA	18.55 mA
		Isource	-7.053 mA	-11.19 mA	-16.67 mA
	DS0=1,DS1=0	Isink	10.50 mA	17.41 mA	25.96 mA
		Isource	-10.58 mA	-16.79 mA	-24.75 mA
	DS0=1,DS1=1	Isink	19.50 mA	32.35 mA	48.22 mA
		Isource	-17.63 mA	-27.98 mA	-41.68 mA

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(VDD=1.8V±0.15V)

Parameter			Currents		
Driver Type			Worst VDD=1.65V T=12 ℃ Process=Slow Isink at VDD*0.2V Isource at VDD*0.8V	Typical VDD=1.80V T=25℃ Process=Nominal Isink at VDD*0.2V Isource at VDD*0.8V	Best VDD=1.95V T=-40℃ Process=Fast Isink at VDD*0.2V Isource at VDD*0.8V
3.3V IO	DS0=0,DS1=0	Isink	2.263 mA	4.057 mA	6.568 mA
		Isource	-2.272 mA	-3.835 mA	-6.081 mA
	DS0=0,DS1=1	Isink	3.775 mA	6.767 mA	10.95 mA
		Isource	-3.636 mA	-6.136 mA	-9.729 mA
	DS0=1,DS1=0	Isink	5.282 mA	9.469 mA	15.33 mA
		Isource	-5.454 mA	-9.204 mA	-14.59 mA
	DS0=1,DS1=1	Isink	9.813 mA	17.59 mA	28.48 mA
		Isource	-9.091 mA	-15.34 mA	-24.32 mA

NOTE: 1. Isink is measured at 0.2 x VDD

NOTE: 2. Isource is measured at 0.8 X VDD

- Mesured point is different from measurement spec of 65nm IO Driver

2.1.4.2 Type B IO Driver Strength

(VDD=3.3V±0.3V)

Parameter			Currents		
Driver Type			Worst VDD=3.00V T=125℃ Process=Slow Isink at VDD*0.2V Isource at VDD*0.8V	Typical VDD=3.30V T=25℃ Process=Nominal Isink at VDD*0.2V Isource at VDD*0.8V	Best VDD=3.60V T=-40℃ Process=Fast Isink at VDD*0.2V Isource at VDD*0.8V
3.3V IO	DS0=0,DS1=0	Isink	2.79mA	4.49mA	6.47mA
		Isource	-2.78mA	-4.26mA	-6.12mA
	DS0=0,DS1=1	Isink	11.18mA	17.98mA	25.88mA
		Isource	-11.11mA	-17.04mA	-24.49mA
	DS0=1,DS1=0	Isink	19.56mA	31.46mA	45.29mA
		Isource	-19.44mA	-29.81mA	-42.86mA
	DS0=1,DS1=1	Isink	27.95mA	44.94mA	64.7mA
		Isource	-27.77mA	-42.59mA	-61.24mA

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(VDD=2.5V±0.2V)

Parameter			Currents		
Driver Type			Worst VDD=2.30V T=125℃ Process=Slow Isink at VDD*0.2V Isource at VDD*0.8V	Typical VDD=2.50V T=25℃ Process=Nominal Isink at VDD*0.2V Isource at VDD*0.8V	Best VDD=2.70V T=-40℃ Process=Fast Isink at VDD*0.2V Isource at VDD*0.8V
3.3V IO	DS0=0,DS1=0	Isink	1.85mA	3.05mA	4.53mA
		Isource	-1.72mA	-2.73mA	-4.08mA
	DS0=0,DS1=1	Isink	7.41mA	12.22mA	18.11mA
		Isource	-6.88mA	-10.93mA	-16.3mA
	DS0=1,DS1=0	Isink	12.97mA	21.38mA	31.69mA
		Isource	-12.04mA	-19.12mA	-28.52mA
	DS0=1,DS1=1	Isink	18.53mA	30.54mA	45.27mA
		Isource	-17.19mA	-27.32mA	-40.75mA

(VDD=1.8V±0.15V)

Parameter			Currents		
Driver Type			Worst VDD=1.65V T=12 ℃ Process=Slow Isink at VDD*0.2V Isource at VDD*0.8V	Typical VDD=1.80V T=25℃ Process=Nominal Isink at VDD*0.2V Isource at VDD*0.8V	Best VDD=1.95V T=-40℃ Process=Fast Isink at VDD*0.2V Isource at VDD*0.8V
3.3V IO	DS0=0,DS1=0	Isink	0.99mA	1.73mA	2.74mA
		Isource	-0.91mA	-1.53mA	-2.41mA
	DS0=0,DS1=1	Isink	3.96mA	6.93mA	10.94mA
		Isource	-3.63mA	-6.1mA	-9.64mA
	DS0=1,DS1=0	Isink	6.93mA	12.12mA	19.14mA
		Isource	-6.35mA	-10.68mA	-16.88mA
	DS0=1,DS1=1	Isink	9.9mA	17.32mA	27.35mA
		Isource	-9.06mA	-15.26mA	-24.11mA

NOTE: 1. Isink is measured at 0.2 x VDD

NOTE: 2. Isource is measured at 0.8 X VDD

- Mesured point is different from measurement spec of 65nm IO Driver

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2.1.4.3 Type C IO Driver Strength

(VDD=1.8V±VDDx10%)

Parameter			Currents		
Driver Type			Worst VDD=1.65V T=125℃ Process=Slow Isink at VDD*0.2V Isource at VDD*0.8V	Typical VDD=1.80V T=25℃ Process=Nominal Isink at VDD*0.2V Isource at VDD*0.8V	Best VDD=1.95V T=-25℃ Process=Fast Isink at VDD*0.2V Isource at VDD*0.8V
1.8V MDDR IO	DS0=0,DS1=0	Isink	3.37mA	5.60mA	8.36mA
		Isource	-2.62mA	-4.32mA	-6.67mA
	DS0=0,DS1=1	Isink	6.74mA	11.21mA	16.73mA
		Isource	-6.10mA	-10.08mA	-15.58mA
	DS0=1,DS1=0	Isink	10.10mA	16.80mA	25.07mA
		Isource	-6.97mA	-11.51mA	-17.80mA
	DS0=1,DS1=1	Isink	11.77mA	19.59mA	29.24mA
		Isource	-11.32mA	-18.70mA	-28.90mA

(VDD=1.2V±VDDx10%)

Parameter			Currents		
Driver Type			Worst VDD=1.045V T=125℃ Process=Slow Isink at VDD*0.2V Isource at VDD*0.8V	Typical VDD=1.1V T=25℃ Process=Nominal Isink at VDD*0.2V Isource at VDD*0.8V	Best VDD=1.155V T=-25℃ Process=Fast Isink at VDD*0.2V Isource at VDD*0.8V
1.8V MDDR IO	DS0=0,DS1=0	Isink	1.10mA	2.22mA	3.95mA
		Isource	-1.05mA	-1.92mA	-3.30mA
	DS0=0,DS1=1	Isink	2.20mA	4.45mA	7.91mA
		Isource	-2.45mA	-4.49mA	-7.70mA
	DS0=1,DS1=0	Isink	3.30mA	6.67mA	11.86mA
		Isource	-2.80mA	-5.12mA	-8.79mA
	DS0=1,DS1=1	Isink	3.85mA	7.78mA	13.82mA
		Isource	-4.55mA	-8.32mA	-14.29mA

NOTE: 1. Isink is measured at 0.2 x VDD

NOTE: 2. Isource is measured at 0.8 X VDD

- Mesured point is different from measurement spec of 65nm IO Driver

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2.1.5 INPUT/ OUTPUT DESCRIPTION

2.1.5.1 General Purpose Input/Output Block Diagram

GPIO consists of two parts, namely, alive-part and off-part. In Alive-part power is supplied on sleep mode, but in off-part it is not the same. Therefore, the registers in alive-part keep their values during sleep mode.

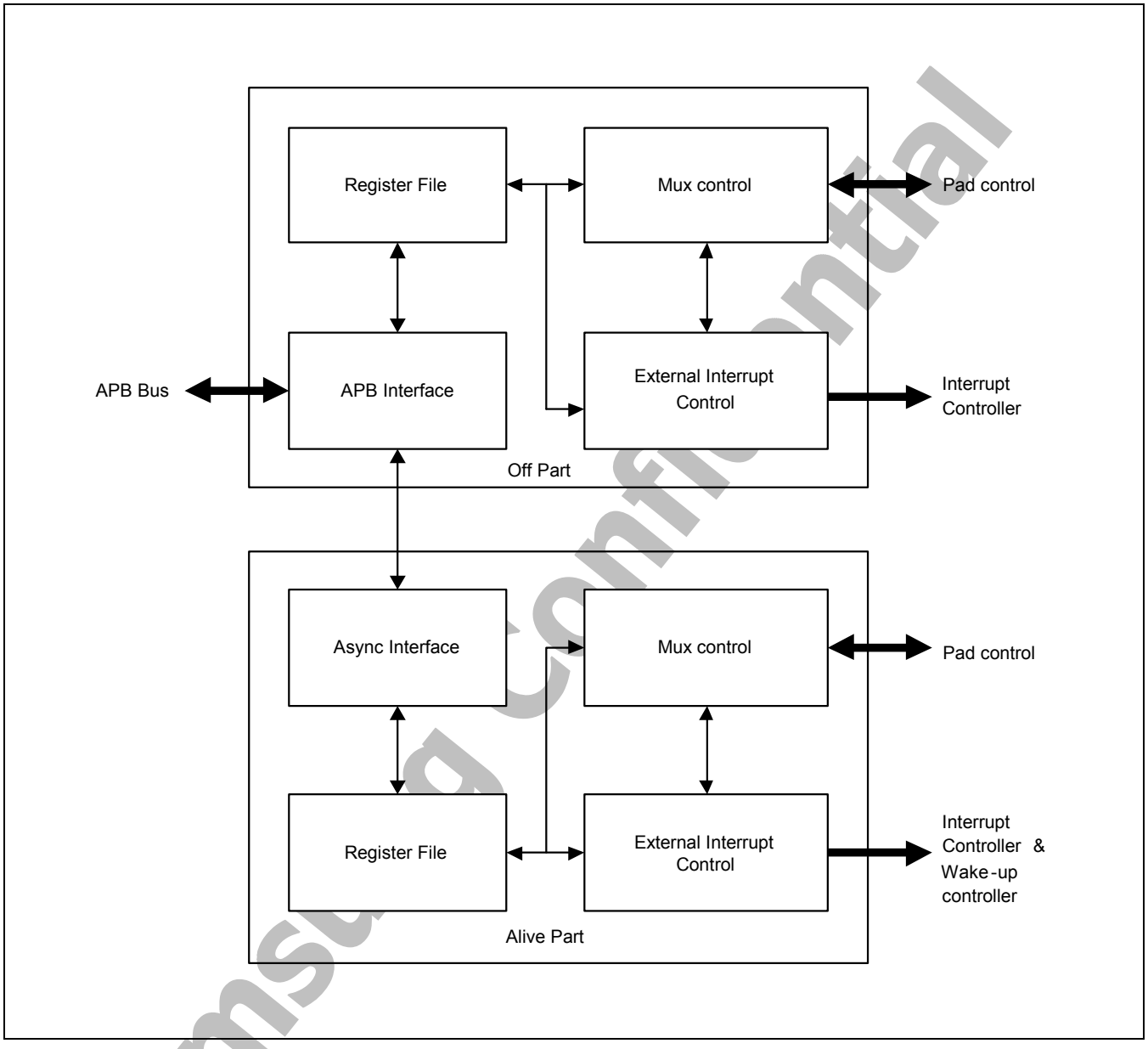

Figure 2-1 GPIO Block Diagram

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2.1.5.2 Pin Summary

I/O Control Type	Function Description
A1	Control at power down mode is possible, power down mode is released by S/W (ENABLE_GPIO bit of OTHERS register at PMU)
A2	Control at power down mode is possible, power down mode is released by S/W (ENABLE_UART_IO bit of OTHERS register at PMU)
A3	Control at power down mode is possible, power down mode is released by S/W (ENABLE_MMC_IO bit of OTHERS register at PMU)
A4	Control at power down mode is possible, power down mode is released by H/W automatically
A5	Control at power down mode is possible, power down mode is released by H/W (ENABLE_CF_IO bit of OTHERS register at PMU)
B1	No Retention (Alive IO)
B2	No Retention (Analog IO)

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2.1.5.3 Pin Mux Description

Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
XuRXD[0]	GPA0[0]	UART_0_RXD				GPI	PD	I(L)	A1	PBIDIRSE_G
XuTXD[0]	GPA0[1]	UART_0_TXD				GPI	PD	I(L)	A1	PBIDIRSE_G
XuCTSn[0]	GPA0[2]	UART_0_CTSn				GPI	PD	I(L)	A1	PBIDIRSE_G
XuRTSn[0]	GPA0[3]	UART_0_RTSn				GPI	PD	I(L)	A1	PBIDIRSE_G
XuRXD[1]	GPA0[4]	UART_1_RXD				GPI	PD	I(L)	A1	PBIDIRSE_G
XuTXD[1]	GPA0[5]	UART_1_TXD				GPI	PD	I(L)	A1	PBIDIRSE_G
XuCTSn[1]	GPA0[6]	UART_1_CTSn				GPI	PD	I(L)	A1	PBIDIRSE_G
XuRTSn[1]	GPA0[7]	UART_1_RTSn				GPI	PD	I(L)	A1	PBIDIRSE_G
XuRXD[2]	GPA1[0]	UART_2_RXD		UART_AUDIO_RXD		GPI	PD	I(L)	A2	PBIDIRSE_G
XuTXD[2]	GPA1[1]	UART_2_TXD		UART_AUDIO_TXD		GPI	PD	I(L)	A2	PBIDIRSE_G
XuRXD[3]	GPA1[2]	UART_3_RXD	UART_2_CTSn			GPI	PD	I(L)	A2	PBIDIRSE_G
XuTXD[3]	GPA1[3]	UART_3_TXD	UART_2_RTSn			GPI	PD	I(L)	A2	PBIDIRSE_G
XspiCLK[0]	GPB[0]	SPI_0_CLK				GPI	PD	I(L)	A1	PBIDIRF_G
XspiCSn[0]	GPB[1]	SPI_0_nSS				GPI	PD	I(L)	A1	PBIDIRF_G
XspiMISO[0]	GPB[2]	SPI_0_MISO				GPI	PD	I(L)	A1	PBIDIRF_G
XspiMOSI[0]	GPB[3]	SPI_0_MOSI				GPI	PD	I(L)	A1	PBIDIRF_G
XspiCLK[1]	GPB[4]	SPI_1_CLK				GPI	PD	I(L)	A1	PBIDIRF_G
XspiCSn[1]	GPB[5]	SPI_1_nSS				GPI	PD	I(L)	A1	PBIDIRF_G
XspiMISO[1]	GPB[6]	SPI_1_MISO				GPI	PD	I(L)	A1	PBIDIRF_G
XspiMOSI[1]	GPB[7]	SPI_1_MOSI				GPI	PD	I(L)	A1	PBIDIRF_G
Xi2s1SCLK	GPC0[0]	I2S_1_SCLK	PCM_1_SCLK	AC97BITCLK		GPI	PD	I(L)	A1	PBIDIRSE_G
Xi2s1CDCLK	GPC0[1]	I2S_1_CDCLK	PCM_1_EXTCLK	AC97RESETn		GPI	PD	I(L)	A1	PBIDIRSE_G
Xi2s1LRCK	GPC0[2]	I2S_1_LRCK	PCM_1_FSYNC	AC97SYNC		GPI	PD	I(L)	A1	PBIDIRSE_G
Xi2s1SDI	GPC0[3]	I2S_1_SDI	PCM_1_SIN	AC97SDI		GPI	PD	I(L)	A1	PBIDIRSE_G
Xi2s1SDO	GPC0[4]	I2S_1_SDO	PCM_1_SOUT	AC97SDO		GPI	PD	I(L)	A1	PBIDIRSE_G
Xpcm2SCLK	GPC1[0]	PCM_2_SCLK	SPDIF_0_OUT	I2S_2_SCLK		GPI	PD	I(L)	A1	PBIDIRSE_G
Xpcm2EXTCLK	GPC1[1]	PCM_2_EXTCLK	SPDIF_EXTCLK	I2S_2_CDCLK		GPI	PD	I(L)	A1	PBIDIRSE_G
Xpcm2FSYNC	GPC1[2]	PCM_2_FSYNC	LCD_FRM	I2S_2_LRCK		GPI	PD	I(L)	A1	PBIDIRSE_G
Xpcm2SIN	GPC1[3]	PCM_2_SIN		I2S_2_SDI		GPI	PD	I(L)	A1	PBIDIRSE_G
Xpcm2SOUT	GPC1[4]	PCM_2_SOUT		I2S_2_SDO		GPI	PD	I(L)	A1	PBIDIRSE_G
XpwmTOUT[0]	GPD0[0]	TOUT_0				GPI	PD	I(L)	A1	PBIDIRSE_G
XpwmTOUT[1]	GPD0[1]	TOUT_1				GPI	PD	I(L)	A1	PBIDIRSE_G
XpwmTOUT[2]	GPD0[2]	TOUT_2				GPI	PD	I(L)	A1	PBIDIRSE_G
XpwmTOUT[3]	GPD0[3]	TOUT_3				GPI	PD	I(L)	A1	PBIDIRSE_G

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Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
Xi2c0SDA	GPD1[0]	I2C0_SDA				GPI	PD	I(L)	A1	PBIDIRSE_G
Xi2c0SCL	GPD1[1]	I2C0_SCL				GPI	PD	I(L)	A1	PBIDIRSE_G
Xi2c1SDA	GPD1[2]	I2C1_SDA				GPI	PD	I(L)	A1	PBIDIRSE_G
Xi2c1SCL	GPD1[3]	I2C1_SCL				GPI	PD	I(L)	A1	PBIDIRSE_G
Xi2c2SDA	GPD1[4]	I2C2_SDA	IEM_SCLK			GPI	PD	I(L)	A1	PBIDIRSE_G
Xi2c2SCL	GPD1[5]	I2C2_SCL	IEM_SPWI			GPI	PD	I(L)	A1	PBIDIRSE_G
XciPCLK	GPE0[0]	CAM_A_PCLK				GPI	PD	I(L)	A1	PBIDIRSE_G
XciVSYNC	GPE0[1]	CAM_A_VSYNC				GPI	PD	I(L)	A1	PBIDIRSE_G
XciHREF	GPE0[2]	CAM_A_HREF				GPI	PD	I(L)	A1	PBIDIRSE_G
XciDATA[0]	GPE0[3]	CAM_A_DATA[0]				GPI	PD	I(L)	A1	PBIDIRSE_G
XciDATA[1]	GPE0[4]	CAM_A_DATA[1]				GPI	PD	I(L)	A1	PBIDIRSE_G
XciDATA[2]	GPE0[5]	CAM_A_DATA[2]				GPI	PD	I(L)	A1	PBIDIRSE_G
XciDATA[3]	GPE0[6]	CAM_A_DATA[3]				GPI	PD	I(L)	A1	PBIDIRSE_G
XciDATA[4]	GPE0[7]	CAM_A_DATA[4]				GPI	PD	I(L)	A1	PBIDIRSE_G
XciDATA[5]	GPE1[0]	CAM_A_DATA[5]				GPI	PD	I(L)	A1	PBIDIRSE_G
XciDATA[6]	GPE1[1]	CAM_A_DATA[6]				GPI	PD	I(L)	A1	PBIDIRSE_G
XciDATA[7]	GPE1[2]	CAM_A_DATA[7]				GPI	PD	I(L)	A1	PBIDIRSE_G
XciCLKenb	GPE1[3]	CAM_A_CLKOUT				GPI	PD	I(L)	A1	PBIDIRSE_G
XciFIELD	GPE1[4]	CAM_A_FIELD				GPI	PD	I(L)	A1	PBIDIRSE_G
XvHSYNC	GPF0[0]	LCD_HSYNC	SYS_CS0	VEN_HSYNC		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVSYNC	GPF0[1]	LCD_VSYNC	SYS_CS1	VEN_VSYNC		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVDEN	GPF0[2]	LCD_VDEN	SYS_RS	VEN_HREF		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVCLK	GPF0[3]	LCD_VCLK	SYS_WE	V601_CLK		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[0]	GPF0[4]	LCD_VD[0]	SYS_VD[0]	VEN_DATA[0]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[1]	GPF0[5]	LCD_VD[1]	SYS_VD[1]	VEN_DATA[1]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[2]	GPF0[6]	LCD_VD[2]	SYS_VD[2]	VEN_DATA[2]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[3]	GPF0[7]	LCD_VD[3]	SYS_VD[3]	VEN_DATA[3]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[4]	GPF1[0]	LCD_VD[4]	SYS_VD[4]	VEN_DATA[4]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[5]	GPF1[1]	LCD_VD[5]	SYS_VD[5]	VEN_DATA[5]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[6]	GPF1[2]	LCD_VD[6]	SYS_VD[6]	VEN_DATA[6]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[7]	GPF1[3]	LCD_VD[7]	SYS_VD[7]	VEN_DATA[7]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[8]	GPF1[4]	LCD_VD[8]	SYS_VD[8]	V656_DATA[0]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[9]	GPF1[5]	LCD_VD[9]	SYS_VD[9]	V656_DATA[1]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[10]	GPF1[6]	LCD_VD[10]	SYS_VD[10]	V656_DATA[2]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[11]	GPF1[7]	LCD_VD[11]	SYS_VD[11]	V656_DATA[3]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[12]	GPF2[0]	LCD_VD[12]	SYS_VD[12]	V656_DATA[4]		GPI	PD	I(L)	A1	PBIDIRSE_G

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Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
XvVD[13]	GPF2[1]	LCD_VD[13]	SYS_VD[13]	V656_DATA[5]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[14]	GPF2[2]	LCD_VD[14]	SYS_VD[14]	V656_DATA[6]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[15]	GPF2[3]	LCD_VD[15]	SYS_VD[15]	V656_DATA[7]		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[16]	GPF2[4]	LCD_VD[16]	SYS_VD[16]			GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[17]	GPF2[5]	LCD_VD[17]	SYS_VD[17]			GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[18]	GPF2[6]	LCD_VD[18]	SYS_VD[18]			GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[19]	GPF2[7]	LCD_VD[19]	SYS_VD[19]			GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[20]	GPF3[0]	LCD_VD[20]	SYS_VD[20]			GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[21]	GPF3[1]	LCD_VD[21]	SYS_VD[21]			GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[22]	GPF3[2]	LCD_VD[22]	SYS_VD[22]			GPI	PD	I(L)	A1	PBIDIRSE_G
XvVD[23]	GPF3[3]	LCD_VD[23]	SYS_VD[23]	V656_CLK		GPI	PD	I(L)	A1	PBIDIRSE_G
XvVSYNC_LDI	GPF3[4]		VSYNC_LDI			GPI	PD	I(L)	A1	PBIDIRSE_G
XvSYS_OE	GPF3[5]		SYS_OE	VEN_FIELD		GPI	PD	I(L)	A1	PBIDIRSE_G
Xmmc0CLK	GPG0[0]	SD_0_CLK				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc0CMD	GPG0[1]	SD_0_CMD				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc0CDn	GPG0[2]	SD_0_CDn				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc0DATA[0]	GPG0[3]	SD_0_DATA[0]				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc0DATA[1]	GPG0[4]	SD_0_DATA[1]				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc0DATA[2]	GPG0[5]	SD_0_DATA[2]				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc0DATA[3]	GPG0[6]	SD_0_DATA[3]				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc1CLK	GPG1[0]	SD_1_CLK				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc1CMD	GPG1[1]	SD_1_CMD				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc1CDn	GPG1[2]	SD_1_CDn				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc1DATA[0]	GPG1[3]	SD_1_DATA[0]	SD_0_DATA[4]			GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc1DATA[1]	GPG1[4]	SD_1_DATA[1]	SD_0_DATA[5]			GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc1DATA[2]	GPG1[5]	SD_1_DATA[2]	SD_0_DATA[6]			GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc1DATA[3]	GPG1[6]	SD_1_DATA[3]	SD_0_DATA[7]			GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc2CLK	GPG2[0]	SD_2_CLK				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc2CMD	GPG2[1]	SD_2_CMD				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc2CDn	GPG2[2]	SD_2_CDn				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc2DATA[0]	GPG2[3]	SD_2_DATA[0]				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc2DATA[1]	GPG2[4]	SD_2_DATA[1]				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc2DATA[2]	GPG2[5]	SD_2_DATA[2]				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc2DATA[3]	GPG2[6]	SD_2_DATA[3]				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc3CLK	GPG3[0]	SD_3_CLK				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc3CMD	GPG3[1]	SD_3_CMD				GPI	PD	I(L)	A3	PBIDIRF_G

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Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
Xmmc3CDn	GPG3[2]	SD_3_CDn				GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc3DATA[0]	GPG3[3]	SD_3_DATA[0]	SD_2_DATA[4]			GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc3DATA[1]	GPG3[4]	SD_3_DATA[1]	SD_2_DATA[5]			GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc3DATA[2]	GPG3[5]	SD_3_DATA[2]	SD_2_DATA[6]			GPI	PD	I(L)	A3	PBIDIRF_G
Xmmc3DATA[3]	GPG3[6]	SD_3_DATA[3]	SD_2_DATA[7]			GPI	PD	I(L)	A3	PBIDIRF_G
XEINT[0]	GPH0[0]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[1]	GPH0[1]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[2]	GPH0[2]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[3]	GPH0[3]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[4]	GPH0[4]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[5]	GPH0[5]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[6]	GPH0[6]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[7]	GPH0[7]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[8]	GPH1[0]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[9]	GPH1[1]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[10]	GPH1[2]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[11]	GPH1[3]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[12]	GPH1[4]			HDMI_CEC		GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[13]	GPH1[5]			HDMI_HPD		GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[14]	GPH1[6]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[15]	GPH1[7]					GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[16]	GPH2[0]		KP_COL[0]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[17]	GPH2[1]		KP_COL[1]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[18]	GPH2[2]		KP_COL[2]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[19]	GPH2[3]		KP_COL[3]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[20]	GPH2[4]		KP_COL[4]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[21]	GPH2[5]		KP_COL[5]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[22]	GPH2[6]		KP_COL[6]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[23]	GPH2[7]		KP_COL[7]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[24]	GPH3[0]		KP_ROW[0]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[25]	GPH3[1]		KP_ROW[1]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[26]	GPH3[2]		KP_ROW[2]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[27]	GPH3[3]		KP_ROW[3]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[28]	GPH3[4]		KP_ROW[4]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[29]	GPH3[5]		KP_ROW[5]			GPI	PD	I(L)	B1	PBIDIR_ALV
XEINT[30]	GPH3[6]		KP_ROW[6]			GPI	PD	I(L)	B1	PBIDIR_ALV

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Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
XEINT[31]	GPH3[7]		KP_ROW[7]			GPI	PD	I(L)	B1	PBIDIR_ALV
Xi2s0SCLK	GPI[0]	I2S_0_SCLK	PCM_0_SCLK			Func0	PD	O(L)	A1	PBIDIRSE_G
Xi2s0CDCLK	GPI[1]	I2S_0_CDCLK	PCM_0_EXTCLK			Func0	PD	O(L)	A1	PBIDIRSE_G
Xi2s0LRCK	GPI[2]	I2S_0_LRCK	PCM_0_FSYNC			Func0	PD	O(L)	A1	PBIDIRSE_G
Xi2s0SDI	GPI[3]	I2S_0_SDI	PCM_0_SIN			Func0	PD	I(L)	A1	PBIDIRSE_G
Xi2s0SDO[0]	GPI[4]	I2S_0_SDO[0]	PCM_0_SOUT			Func0	PD	O(L)	A1	PBIDIRSE_G
Xi2s0SDO[1]	GPI[5]	I2S_0_SDO[1]				Func0	PD	O(L)	A1	PBIDIRSE_G
Xi2s0SDO[2]	GPI[6]	I2S_0_SDO[2]				Func0	PD	O(L)	A1	PBIDIRSE_G
XmsmADDR[0]	GPJ0[0]	MSM_ADDR[0]	CAM_B_DATA[0]	CF_ADDR[0]	MIPI_BYTE_CLK	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADDR[1]	GPJ0[1]	MSM_ADDR[1]	CAM_B_DATA[1]	CF_ADDR[1]	MIPI_ESC_CLK	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADDR[2]	GPJ0[2]	MSM_ADDR[2]	CAM_B_DATA[2]	CF_ADDR[2]	TS_CLK	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADDR[3]	GPJ0[3]	MSM_ADDR[3]	CAM_B_DATA[3]	CF_IORDY	TS_SYNC	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADDR[4]	GPJ0[4]	MSM_ADDR[4]	CAM_B_DATA[4]	CF_INTRQ	TS_VAL	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADDR[5]	GPJ0[5]	MSM_ADDR[5]	CAM_B_DATA[5]	CF_DMARQ	TS_DATA	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADDR[6]	GPJ0[6]	MSM_ADDR[6]	CAM_B_DATA[6]	CF_DRESETN	TS_ERROR	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADDR[7]	GPJ0[7]	MSM_ADDR[7]	CAM_B_DATA[7]	CF_DMACKN	MHL_D0	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADDR[8]	GPJ1[0]	MSM_ADDR[8]	CAM_B_PCLK	SROM_ADDR_16to22[0]	MHL_D1	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADDR[9]	GPJ1[1]	MSM_ADDR[9]	CAM_B_VSYNC	SROM_ADDR_16to22[1]	MHL_D2	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADDR[10]	GPJ1[2]	MSM_ADDR[10]	CAM_B_HREF	SROM_ADDR_16to22[2]	MHL_D3	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADDR[11]	GPJ1[3]	MSM_ADDR[11]	CAM_B_FIELD	SROM_ADDR_16to22[3]	MHL_D4	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADDR[12]	GPJ1[4]	MSM_ADDR[12]	CAM_B_CLKOUT	SROM_ADDR_16to22[4]	MHL_D5	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADDR[13]	GPJ1[5]	MSM_ADDR[13]	KP_COL[0]	SROM_ADDR_16to22[5]	MHL_D6	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[0]	GPJ2[0]	MSM_DATA[0]	KP_COL[1]	CF_DATA[0]	MHL_D7	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[1]	GPJ2[1]	MSM_DATA[1]	KP_COL[2]	CF_DATA[1]	MHL_D8	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[2]	GPJ2[2]	MSM_DATA[2]	KP_COL[3]	CF_DATA[2]	MHL_D9	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[3]	GPJ2[3]	MSM_DATA[3]	KP_COL[4]	CF_DATA[3]	MHL_D10	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[4]	GPJ2[4]	MSM_DATA[4]	KP_COL[5]	CF_DATA[4]	MHL_D11	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[5]	GPJ2[5]	MSM_DATA[5]	KP_COL[6]	CF_DATA[5]	MHL_D12	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[6]	GPJ2[6]	MSM_DATA[6]	KP_COL[7]	CF_DATA[6]	MHL_D13	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[7]	GPJ2[7]	MSM_DATA[7]	KP_ROW[0]	CF_DATA[7]	MHL_D14	GPI	PD	I(L)	A5	PBIDIRSE_G

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Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
XmsmDATA[8]	GPJ3[0]	MSM_DATA[8]	KP_ROW[1]	CF_DATA[8]	MHL_D15	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[9]	GPJ3[1]	MSM_DATA[9]	KP_ROW[2]	CF_DATA[9]	MHL_D16	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[10]	GPJ3[2]	MSM_DATA[10]	KP_ROW[3]	CF_DATA[10]	MHL_D17	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[11]	GPJ3[3]	MSM_DATA[11]	KP_ROW[4]	CF_DATA[11]	MHL_D18	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[12]	GPJ3[4]	MSM_DATA[12]	KP_ROW[5]	CF_DATA[12]	MHL_D19	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[13]	GPJ3[5]	MSM_DATA[13]	KP_ROW[6]	CF_DATA[13]	MHL_D20	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[14]	GPJ3[6]	MSM_DATA[14]	KP_ROW[7]	CF_DATA[14]	MHL_D21	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmDATA[15]	GPJ3[7]	MSM_DATA[15]	KP_ROW[8]	CF_DATA[15]	MHL_D22	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmCSn	GPJ4[0]	MSM_CSn	KP_ROW[9]	CF_CSn[0]	MHL_D23	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmWEn	GPJ4[1]	MSM_WEn	KP_ROW[10]	CF_CSn[1]	MHL_HSYNC	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmRn	GPJ4[2]	MSM_Rn	KP_ROW[11]	CF_IORN	MHL_IDCK	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmIRQn	GPJ4[3]	MSM_IRQn	KP_ROW[12]	CF_IOWN	MHL_VSYNC	GPI	PD	I(L)	A5	PBIDIRSE_G
XmsmADVN	GPJ4[4]	MSM_ADVN	KP_ROW[13]	SROM_ADDR_16to22[6]	MHL_DE	GPI	PD	I(L)	A5	PBIDIRSE_G
Xm0CSn[0]	MP0_1[0]	SROM_CSn[0]				Func0	-	O(H)	A4	PBIDIRF_G
Xm0CSn[1]	MP0_1[1]	SROM_CSn[1]				Func0	-	O(H)	A4	PBIDIRF_G
Xm0CSn[2]	MP0_1[2]	SROM_CSn[2]	NFCSn[0]			Func1	-	O(H)	A4	PBIDIRF_G
Xm0CSn[3]	MP0_1[3]	SROM_CSn[3]	NFCSn[1]			Func1	-	O(H)	A4	PBIDIRF_G
Xm0CSn[4]	MP0_1[4]	SROM_CSn[4]	NFCSn[2]		ONANDXL_CSn[0]	Func3	-	O(H)	A4	PBIDIRF_G
Xm0CSn[5]	MP0_1[5]	SROM_CSn[5]	NFCSn[3]		ONANDXL_CSn[1]	Func3	-	O(H)	A4	PBIDIRF_G
Xm0OEn	MP0_1[6]	EBI_OEn				Func0	-	O(H)	A4	PBIDIRF_G
Xm0WEn	MP0_1[7]	EBI_WEn				Func0	-	O(H)	A4	PBIDIRF_G
Xm0BEn[0]	MP0_2[0]	EBI_BEn[0]				Func0	-	O(H)	A4	PBIDIRF_G
Xm0BEn[1]	MP0_2[1]	EBI_BEn[1]				Func0	-	O(H)	A4	PBIDIRF_G
Xm0WAITn	MP0_2[2]	SROM_WAITn				Func0	-	I	A4	PBIDIRF_G
Xm0DATA_RDn	MP0_2[3]	EBI_DATA_RDn				Func0	-	O(L)	A4	PBIDIRF_G
Xm0FCLE	MP0_3[0]	NF_CLE			ONANDXL_ADDRVALID	Func3	-	O(L)	A4	PBIDIRF_G
Xm0FALE	MP0_3[1]	NF_ALE			ONANDXL_SMCLK	Func3	-	O(L)	A4	PBIDIRF_G
Xm0FWEn	MP0_3[2]	NF_FWEn			ONANDXL_RPn	Func3	-	O(H)	A4	PBIDIRF_G
Xm0FREn	MP0_3[3]	NF_FREn				Func3	-	I	A4	PBIDIRF_G

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Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
Xm0FRnB[0]	MP0_3[4]	NF_RnB[0]			ONANDXL_INT[0]	Func3	-	I	A4	PBIDIRF_G
Xm0FRnB[1]	MP0_3[5]	NF_RnB[1]			ONANDXL_INT[1]	Func3	-	I	A4	PBIDIRF_G
Xm0FRnB[2]	MP0_3[6]	NF_RnB[2]				Func3	-	I	A4	PBIDIRF_G
Xm0FRnB[3]	MP0_3[7]	NF_RnB[3]				Func3	-	I	A4	PBIDIRF_G
Xm0ADDR[0]	MP0_4[0]	EBI_ADDR[0]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[1]	MP0_4[1]	EBI_ADDR[1]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[2]	MP0_4[2]	EBI_ADDR[2]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[3]	MP0_4[3]	EBI_ADDR[3]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[4]	MP0_4[4]	EBI_ADDR[4]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[5]	MP0_4[5]	EBI_ADDR[5]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[6]	MP0_4[6]	EBI_ADDR[6]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[7]	MP0_4[7]	EBI_ADDR[7]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[8]	MP0_5[0]	EBI_ADDR[8]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[9]	MP0_5[1]	EBI_ADDR[9]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[10]	MP0_5[2]	EBI_ADDR[10]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[11]	MP0_5[3]	EBI_ADDR[11]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[12]	MP0_5[4]	EBI_ADDR[12]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[13]	MP0_5[5]	EBI_ADDR[13]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[14]	MP0_5[6]	EBI_ADDR[14]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0ADDR[15]	MP0_5[7]	EBI_ADDR[15]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[0]	MP0_6[0]	EBI_DATA[0]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[1]	MP0_6[1]	EBI_DATA[1]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[2]	MP0_6[2]	EBI_DATA[2]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[3]	MP0_6[3]	EBI_DATA[3]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[4]	MP0_6[4]	EBI_DATA[4]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[5]	MP0_6[5]	EBI_DATA[5]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[6]	MP0_6[6]	EBI_DATA[6]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[7]	MP0_6[7]	EBI_DATA[7]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[8]	MP0_7[0]	EBI_DATA[8]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[9]	MP0_7[1]	EBI_DATA[9]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[10]	MP0_7[2]	EBI_DATA[10]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[11]	MP0_7[3]	EBI_DATA[11]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[12]	MP0_7[4]	EBI_DATA[12]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[13]	MP0_7[5]	EBI_DATA[13]				Func0	-	O(L)	A4	PBIDIRF_G
Xm0DATA[14]	MP0_7[6]	EBI_DATA[14]				Func0	-	O(L)	A4	PBIDIRF_G

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Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
Xm0DATA[15]	MP0_7[7]	EBI_DATA[15]				Func0	-	O(L)	A4	PBIDIRF_G
Xm1ADDR[0]	MP1_0[0]	LD0_ADDR[0]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[1]	MP1_0[1]	LD0_ADDR[1]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[2]	MP1_0[2]	LD0_ADDR[2]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[3]	MP1_0[3]	LD0_ADDR[3]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[4]	MP1_0[4]	LD0_ADDR[4]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[5]	MP1_0[5]	LD0_ADDR[5]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[6]	MP1_0[6]	LD0_ADDR[6]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[7]	MP1_0[7]	LD0_ADDR[7]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[8]	MP1_1[0]	LD0_ADDR[8]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[9]	MP1_1[1]	LD0_ADDR[9]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[10]	MP1_1[2]	LD0_ADDR[10]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[11]	MP1_1[3]	LD0_ADDR[11]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[12]	MP1_1[4]	LD0_ADDR[12]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[13]	MP1_1[5]	LD0_ADDR[13]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[14]	MP1_1[6]	LD0_ADDR[14]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1ADDR[15]	MP1_1[7]	LD0_ADDR[15]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1DATA[0]	MP1_2[0]	LD0_DATA[0]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[1]	MP1_2[1]	LD0_DATA[1]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[2]	MP1_2[2]	LD0_DATA[2]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[3]	MP1_2[3]	LD0_DATA[3]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[4]	MP1_2[4]	LD0_DATA[4]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[5]	MP1_2[5]	LD0_DATA[5]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[6]	MP1_2[6]	LD0_DATA[6]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[7]	MP1_2[7]	LD0_DATA[7]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[8]	MP1_3[0]	LD0_DATA[8]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[9]	MP1_3[1]	LD0_DATA[9]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[10]	MP1_3[2]	LD0_DATA[10]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[11]	MP1_3[3]	LD0_DATA[11]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[12]	MP1_3[4]	LD0_DATA[12]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[13]	MP1_3[5]	LD0_DATA[13]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[14]	MP1_3[6]	LD0_DATA[14]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[15]	MP1_3[7]	LD0_DATA[15]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[16]	MP1_4[0]	LD0_DATA[16]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[17]	MP1_4[1]	LD0_DATA[17]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[18]	MP1_4[2]	LD0_DATA[18]				Func0	-	I	A4	PBIDIR_MDDR

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Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
Xm1DATA[19]	MP1_4[3]	LD0_DATA[19]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[20]	MP1_4[4]	LD0_DATA[20]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[21]	MP1_4[5]	LD0_DATA[21]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[22]	MP1_4[6]	LD0_DATA[22]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[23]	MP1_4[7]	LD0_DATA[23]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[24]	MP1_5[0]	LD0_DATA[24]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[25]	MP1_5[1]	LD0_DATA[25]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[26]	MP1_5[2]	LD0_DATA[26]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[27]	MP1_5[3]	LD0_DATA[27]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[28]	MP1_5[4]	LD0_DATA[28]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[29]	MP1_5[5]	LD0_DATA[29]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[30]	MP1_5[6]	LD0_DATA[30]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DATA[31]	MP1_5[7]	LD0_DATA[31]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DQS[0]	MP1_6[0]	LD0_DQS[0]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DQS[1]	MP1_6[1]	LD0_DQS[1]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DQS[2]	MP1_6[2]	LD0_DQS[2]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DQS[3]	MP1_6[3]	LD0_DQS[3]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DQSn[0]	MP1_6[4]	LD0_DQSn[0]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DQSn[1]	MP1_6[5]	LD0_DQSn[1]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DQSn[2]	MP1_6[6]	LD0_DQSn[2]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DQSn[3]	MP1_6[7]	LD0_DQSn[3]				Func0	-	I	A4	PBIDIR_MDDR
Xm1DQM[0]	MP1_7[0]	LD0_DQM[0]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1DQM[1]	MP1_7[1]	LD0_DQM[1]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1DQM[2]	MP1_7[2]	LD0_DQM[2]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1DQM[3]	MP1_7[3]	LD0_DQM[3]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1CKE[0]	MP1_7[4]	LD0_CKE[0]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1CKE[1]	MP1_7[5]	LD0_CKE[1]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1SCLK	MP1_7[6]	LD0_SCLK				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm1nSCLK	MP1_7[7]	LD0_nSCLK				Func0	-	O(H)	A4	PBIDIR_MDDR
Xm1CSn[0]	MP1_8[0]	LD0_CSn_0				Func0	-	O(H)	A4	PBIDIR_MDDR
Xm1CSn[1]	MP1_8[1]	LD0_CSn_1				Func0	-	O(H)	A4	PBIDIR_MDDR
Xm1RASn	MP1_8[2]	LD0_RASn				Func0	-	O(H)	A4	PBIDIR_MDDR
Xm1CASn	MP1_8[3]	LD0_CASn				Func0	-	O(H)	A4	PBIDIR_MDDR
Xm1WEn	MP1_8[4]	LD0_WEn				Func0	-	O(H)	A4	PBIDIR_MDDR
Xm1GateIn	MP1_8[5]	LD0_IOGATE_IN				Func0	-	I	A4	PBIDIR_MDDR
Xm1GateOut	MP1_8[6]	LD0_IOGATE_OUT				Func0	-	O	A4	PBIDIR_MDDR

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Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
Xm2ADDR[0]	MP2_0[0]	LD1_ADDR[0]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[1]	MP2_0[1]	LD1_ADDR[1]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[2]	MP2_0[2]	LD1_ADDR[2]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[3]	MP2_0[3]	LD1_ADDR[3]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[4]	MP2_0[4]	LD1_ADDR[4]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[5]	MP2_0[5]	LD1_ADDR[5]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[6]	MP2_0[6]	LD1_ADDR[6]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[7]	MP2_0[7]	LD1_ADDR[7]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[8]	MP2_1[0]	LD1_ADDR[8]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[9]	MP2_1[1]	LD1_ADDR[9]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[10]	MP2_1[2]	LD1_ADDR[10]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[11]	MP2_1[3]	LD1_ADDR[11]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[12]	MP2_1[4]	LD1_ADDR[12]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[13]	MP2_1[5]	LD1_ADDR[13]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[14]	MP2_1[6]	LD1_ADDR[14]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2ADDR[15]	MP2_1[7]	LD1_ADDR[15]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2DATA[0]	MP2_2[0]	LD1_DATA[0]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[1]	MP2_2[1]	LD1_DATA[1]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[2]	MP2_2[2]	LD1_DATA[2]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[3]	MP2_2[3]	LD1_DATA[3]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[4]	MP2_2[4]	LD1_DATA[4]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[5]	MP2_2[5]	LD1_DATA[5]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[6]	MP2_2[6]	LD1_DATA[6]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[7]	MP2_2[7]	LD1_DATA[7]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[8]	MP2_3[0]	LD1_DATA[8]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[9]	MP2_3[1]	LD1_DATA[9]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[10]	MP2_3[2]	LD1_DATA[10]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[11]	MP2_3[3]	LD1_DATA[11]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[12]	MP2_3[4]	LD1_DATA[12]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[13]	MP2_3[5]	LD1_DATA[13]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[14]	MP2_3[6]	LD1_DATA[14]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[15]	MP2_3[7]	LD1_DATA[15]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[16]	MP2_4[0]	LD1_DATA[16]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[17]	MP2_4[1]	LD1_DATA[17]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[18]	MP2_4[2]	LD1_DATA[18]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[19]	MP2_4[3]	LD1_DATA[19]				Func0	-	I	A4	PBIDIR_MDDR

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Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
Xm2DATA[20]	MP2_4[4]	LD1_DATA[20]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[21]	MP2_4[5]	LD1_DATA[21]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[22]	MP2_4[6]	LD1_DATA[22]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[23]	MP2_4[7]	LD1_DATA[23]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[24]	MP2_5[0]	LD1_DATA[24]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[25]	MP2_5[1]	LD1_DATA[25]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[26]	MP2_5[2]	LD1_DATA[26]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[27]	MP2_5[3]	LD1_DATA[27]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[28]	MP2_5[4]	LD1_DATA[28]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[29]	MP2_5[5]	LD1_DATA[29]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[30]	MP2_5[6]	LD1_DATA[30]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DATA[31]	MP2_5[7]	LD1_DATA[31]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DQS[0]	MP2_6[0]	LD1_DQS[0]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DQS[1]	MP2_6[1]	LD1_DQS[1]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DQS[2]	MP2_6[2]	LD1_DQS[2]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DQS[3]	MP2_6[3]	LD1_DQS[3]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DQSn[0]	MP2_6[4]	LD1_DQSn[0]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DQSn[1]	MP2_6[5]	LD1_DQSn[1]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DQSn[2]	MP2_6[6]	LD1_DQSn[2]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DQSn[3]	MP2_6[7]	LD1_DQSn[3]				Func0	-	I	A4	PBIDIR_MDDR
Xm2DQM[0]	MP2_7[0]	LD1_DQM[0]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2DQM[1]	MP2_7[1]	LD1_DQM[1]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2DQM[2]	MP2_7[2]	LD1_DQM[2]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2DQM[3]	MP2_7[3]	LD1_DQM[3]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2CKE[0]	MP2_7[4]	LD1_CKE[0]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2CKE[1]	MP2_7[5]	LD1_CKE[1]				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2SCLK	MP2_7[6]	LD1_SCLK				Func0	-	O(L)	A4	PBIDIR_MDDR
Xm2nSCLK	MP2_7[7]	LD1_nSCLK				Func0	-	O(H)	A4	PBIDIR_MDDR
Xm2CSn[0]	MP2_8[0]	LD1_CSn_0				Func0	-	O(H)	A4	PBIDIR_MDDR
Xm2CSn[1]	MP2_8[1]	LD1_CSn_1				Func0	-	O(H)	A4	PBIDIR_MDDR
Xm2RASn	MP2_8[2]	LD1_RASn				Func0	-	O(H)	A4	PBIDIR_MDDR
Xm2CASn	MP2_8[3]	LD1_CASn				Func0	-	O(H)	A4	PBIDIR_MDDR
Xm2WEn	MP2_8[4]	LD1_WEn				Func0	-	O(H)	A4	PBIDIR_MDDR
Xm2GateIn	MP2_8[5]	LD1_IOGATE_IN				Func0	-	I	A4	PBIDIR_MDDR
Xm2GateOut	MP2_8[6]	LD1_IOGATE_OUT				Func0	-	O	A4	PBIDIR_MDDR
XjTRSTn	ETC0[0]	XjTRSTn				Func0	PD	I(L)	A4	PBIDIRSE_G

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Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
XjTMS	ETC0[1]	XjTMS				Func0	PU	I(H)	A4	PBIDIRSE_G
XjTCK	ETC0[2]	XjTCK				Func0	PD	I(L)	A4	PBIDIRSE_G
XjTDI	ETC0[3]	XjTDI				Func0	PU	I(H)	A4	PBIDIRSE_G
XjTDO	ETC0[4]	XjTDO				Func0	-	O(L)	A4	PBIDIRSE_G
XjDBGSEL	ETC0[5]	XjDBGSEL				Func0	-	I	A4	PBIDIRSE_G
XOM[0]	ETC1[0]	XOM[0]				Func0	-	I	B1	PBIDIRSE_G
XOM[1]	ETC1[1]	XOM[1]				Func0	-	I	B1	PBIDIRSE_G
XOM[2]	ETC1[2]	XOM[2]				Func0	-	I	B1	PBIDIRSE_G
XOM[3]	ETC1[3]	XOM[3]				Func0	-	I	B1	PBIDIRSE_G
XOM[4]	ETC1[4]	XOM[4]				Func0	-	I	B1	PBIDIRSE_G
XOM[5]	ETC1[5]	XOM[5]				Func0	-	I	B1	PBIDIRSE_G
XDDR2SEL	ETC1[6]	XDDR2_SEL				Func0	-	I	A1	PBIDIRSE_G
XPWRRGTON	ETC1[7]	XPWRRGTON				Func0	-	O(L)	B1	PBIDIRSE_G
XnRESET	ETC2[0]	XnRESET				Func0	-	I	B1	PBIDIRSE_G
XCLKOUT	ETC2[1]	CLKOUT				Func0	-	O(L)	B1	PBIDIRSE_G
XnRSTOUT	ETC2[2]	XnRSTOUT				Func0	-	O(L)	B1	PBIDIRSE_G
XnWRESET	ETC2[3]	XnWRESET				Func0	PU	I(H)	B1	PBIDIRSE_G
XRTCCLKO	ETC2[4]	RTC_CLKOUT				Func0	-	O(L)	B1	PBIDIRSE_G
XuotgDRVVBUS	ETC2[5]	XuotgDRVVBUS				Func0	-	O(L)	A1	PBIDIRSE_G
XuhostPWREN	ETC2[6]	XuhostPWREN				Func0	-	O(L)	A1	PBIDIRSE_G
XuhostOVERCUR	ETC2[7]	XuhostOVERCUR				Func0	-	I	A1	PBIDIRSE_G
XrtcXTI	ETC4[0]	XrtcXTI				Func0	-	I	B1	POSC1A
XrtcXTO	ETC4[1]	XrtcXTO				Func0	-	O(L)	B1	POSC1A
XXTI	ETC4[2]	XXTI				Func0	-	I	B1	POSCP
XXTO	ETC4[3]	XXTO				Func0	-	O(L)	B1	POSCP
XusbXTI	ETC4[4]	XusbXTI				Func0	-	I	B1	POSCPB
XusbXTO	ETC4[5]	XusbXTO				Func0	-	O(L)	B1	POSCPB
XadcAIN[0]	ANALOG	AIN[0]				Func0	-	I	B2	PANALOGS
XadcAIN[1]	ANALOG	AIN[1]				Func0	-	I	B2	PANALOGS
XadcAIN[2]	ANALOG	AIN[2]				Func0	-	I	B2	PANALOGS
XadcAIN[3]	ANALOG	AIN[3]				Func0	-	I	B2	PANALOGS
XadcAIN[4]	ANALOG	AIN[4]				Func0	-	I	B2	PANALOGS
XadcAIN[5]	ANALOG	AIN[5]				Func0	-	I	B2	PANALOGS
XadcAIN[6]	ANALOG	AIN[6]				Func0	-	I	B2	PANALOGS
XadcAIN[7]	ANALOG	AIN[7]				Func0	-	I	B2	PANALOGS
XadcAIN[8]	ANALOG	AIN[8]				Func0	-	I	B2	PANALOGS

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Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
XadcAIN[9]	ANALOG	AIN[9]				Func0	-	I	B2	PANALOGS
XdacOUT	ANALOG	XdacOUT				Func0	-	O(H)	B2	PANALOGSW
XdacIREF	ANALOG	XdacIREF				Func0	-	I	B2	PANALOGSW
XdacVREF	ANALOG	XdacVREF				Func0	-	I	B2	PANALOGSW
XdacCOMP	ANALOG	XdacCOMP				Func0	-	O(H)	B2	PANALOGSW
XhdmiTX0P	ANALOG	HDMI_TX0P				Func0	-	O(H)	B2	PANALOGS
XhdmiTX0N	ANALOG	HDMI_TX0N				Func0	-	O(H)	B2	PANALOGS
XhdmiTX1P	ANALOG	HDMI_TX1P				Func0	-	O(H)	B2	PANALOGS
XhdmiTX1N	ANALOG	HDMI_TX1N				Func0	-	O(H)	B2	PANALOGS
XhdmiTX2P	ANALOG	HDMI_TX2P				Func0	-	O(H)	B2	PANALOGS
XhdmiTX2N	ANALOG	HDMI_TX2N				Func0	-	O(H)	B2	PANALOGS
XhdmiTXCP	ANALOG	HDMI_TXCP				Func0	-	O(H)	B2	PANALOGS
XhdmiTXCN	ANALOG	HDMI_TXCN				Func0	-	O(H)	B2	PANALOGS
XhdmiREXT	ANALOG	HDMI_REXT				Func0	-	I	B2	PANALOGS
XhdmiXTI	ANALOG	HDMI_XI				Func0	-	I	B2	POSCP
XhdmiXTO	ANALOG	HDMI_XO				Func0	-	O(L)	B2	POSCP
XmipiMDP0	ANALOG	MIPI_MDP_0				Func0	-	I	B2	PANALOGS
XmipiMDP1	ANALOG	MIPI_MDP_1				Func0	-	I	B2	PANALOGS
XmipiMDP2	ANALOG	MIPI_MDP_2				Func0	-	I	B2	PANALOGS
XmipiMDP3	ANALOG	MIPI_MDP_3				Func0	-	I	B2	PANALOGS
XmipiMDN0	ANALOG	MIPI_MDN_0				Func0	-	I	B2	PANALOGS
XmipiMDN1	ANALOG	MIPI_MDN_1				Func0	-	I	B2	PANALOGS
XmipiMDN2	ANALOG	MIPI_MDN_2				Func0	-	I	B2	PANALOGS
XmipiMDN3	ANALOG	MIPI_MDN_3				Func0	-	I	B2	PANALOGS
XmipiSDP0	ANALOG	MIPI_SDP_0				Func0	-	I	B2	PANALOGS
XmipiSDP1	ANALOG	MIPI_SDP_1				Func0	-	I	B2	PANALOGS
XmipiSDP2	ANALOG	MIPI_SDP_2				Func0	-	I	B2	PANALOGS
XmipiSDP3	ANALOG	MIPI_SDP_3				Func0	-	I	B2	PANALOGS
XmipiSDN0	ANALOG	MIPI_SDN_0				Func0	-	I	B2	PANALOGS
XmipiSDN1	ANALOG	MIPI_SDN_1				Func0	-	I	B2	PANALOGS
XmipiSDN2	ANALOG	MIPI_SDN_2				Func0	-	I	B2	PANALOGS
XmipiSDN3	ANALOG	MIPI_SDN_3				Func0	-	I	B2	PANALOGS
XmipiMDPCLK	ANALOG	MIPI_CLK_TX_P				Func0	-	I	B2	PANALOGS
XmipiMDNCLK	ANALOG	MIPI_CLK_TX_N				Func0	-	I	B2	PANALOGS
XmipiSDPCLK	ANALOG	MIPI_CLK_RX_P				Func0	-	I	B2	PANALOGS
XmipiSDNCLK	ANALOG	MIPI_CLK_RX_N				Func0	-	I	B2	PANALOGS

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Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
XmipiVREG_0P4V	ANALOG	MIPI_Reg_cap				Func0	-	I	B2	PANALOGS
XuotgDP	ANALOG	XuotgDP				Func0	-	I	B2	PVHTBR_33_5T
XuotgREXT	ANALOG	XuotgREXT				Func0	-	I	B2	PANALOGS
XuotgDM	ANALOG	XuotgDM				Func0	-	I	B2	PVHTBR_33_5T
XuotgANTEST	ANALOG	XuotgANALOGTEST				Func0	-	O(L)	B2	PANALOGS
XefFSOURCE_0	ANALOG	efrom_fsource_0				Func0	-	I	B2	PV_EFUSE
XefFSOURCE_1	ANALOG	efrom_fsource_1				Func0	-	I	B2	PV_EFUSE
XefFSOURCE_2	ANALOG	efrom_fsource_2				Func0	-	I	B2	PV_EFUSE
XabbNBBG	ANALOG	XabbNBBG				Func0	-	I	B2	PVDRAM
XabbPBBG	ANALOG	XabbPBBG				Func0	-	I	B2	PVDRAM
XuhostDP	ANALOG	XuhostDP				Func0	-	I	B2	PVHTBR_33_5T
XuhostREXT	ANALOG	XuhostREXT				Func0	-	O(L)	B2	PANALOGS
XuhostDM	ANALOG	XuhostDM				Func0	-	O(L)	B2	PVHTBR_33_5T
XuhostANTEST	ANALOG	XuhostANALOGTEST				Func0	-	O(L)	B2	PANALOGS
XuotgID	ANALOG	XuotgID				Func0	-	I	B2	PANALOGS
XuotgVBUS	ANALOG	XuotgVBUS				Func0	-	I	B2	PVHTBR_33_5T

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2.1.5.4 Pad Type Description

Cell Name	Function Description
PBIDIRSE_G	Wide-range I/O supply, programmable bi-direction I/O with cmos / schmitt trigger input, input disable, pull-up/down and 4-step strength output
PBIDIRF_G	Wide-range I/O supply, programmable bi-direction Fast I/O with cmos / schmitt trigger input, input disable, pull-up/down and 4-step strength output
PBIDIR_MDDR	Wide-range I/O supply, programmable bi-direction I/O with cmos / schmitt trigger input, input disable, pull-up/down and 4-step strength output
PVHTBR_33_5T	Wide-range I/O supply, 5V tolerant bi-direction path-through pad with 3 different paths which have no resistor, 50ohm or 200ohm resistor
PANALOGS	Analog input (Note: This cell does not support fail-safe operation)
PANALOGSW	Analog input (Note: This cell does not support fail-safe operation) Pin port wide type
POSCP	Wide-range I/O supply, programmable and retention oscillator for 32kHz~50MHz frequency
POSCPB	Wide-range I/O supply, programmable and retention oscillator for 32kHz~50MHz frequency with 3.3V clock output
POSC1A	Wide-range I/O supply, 32kHz oscillator for RTC interface.
PV_EFUSE	Wide-range I/O supply, bi-direction path-through pad with 2 different paths which have no resistor, 10ohm for EFUSE memory.

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2.2 REGISTER DESCRIPTION

2.2.1 REGISTER MAP

Each Port Group has 2 types of control registers.

One works in normal mode, and the other works in power down mode (STOP, DEEP-STOP, SLEEP mode)

Normal registers (For example, GPA0CON, GPA0DAT, GPA0PUD, and GPA0DRV) are the former, and power down registers (For example, GPA0CONPDN, and GPA0PUDPDN) are the latter.

If, S5PV210 enter the power down mode, all configurations and Pull-down controls are selected by power down registers

Register	Address	R/W	Description	Reset Value
GPA0CON	0xE020_0000	R/W	Port Group GPA0 Configuration Register	0x00000000
GPA0DAT	0xE020_0004	R/W	Port Group GPA0 Data Register	0x00
GPA0PUD	0xE020_0008	R/W	Port Group GPA0 Pull-up/down Register	0x5555
GPA0DRV	0xE020_000C	R/W	Port Group GPA0 Drive Strength Control Register	0x0000
GPA0CONPDN	0xE020_0010	R/W	Port Group GPA0 Power Down Mode Configuration Register	0x00
GPA0PUDPDN	0xE020_0014	R/W	Port Group GPA0 Power Down Mode Pull-up/down Register	0x00
GPA1CON	0xE020_0020	R/W	Port Group GPA1 Configuration Register	0x00000000
GPA1DAT	0xE020_0024	R/W	Port Group GPA1 Data Register	0x00
GPA1PUD	0xE020_0028	R/W	Port Group GPA1 Pull-up/down Register	0x0055
GPA1DRV	0xE020_002C	R/W	Port Group GPA1 Drive Strength Control Register	0x0000
GPA1CONPDN	0xE020_0030	R/W	Port Group GPA1 Power Down Mode Configuration Register	0x00
GPA1PUDPDN	0xE020_0034	R/W	Port Group GPA1 Power Down Mode Pull-up/down Register	0x00
GPBCON	0xE020_0040	R/W	Port Group GPB Configuration Register	0x00000000
GPBDAT	0xE020_0044	R/W	Port Group GPB Data Register	0x00
GPBPUD	0xE020_0048	R/W	Port Group GPB Pull-up/down Register	0x5555
GPBDRV	0xE020_004C	R/W	Port Group GPB Drive Strength Control Register	0x0000
GPBCONPDN	0xE020_0050	R/W	Port Group GPB Power Down Mode Configuration Register	0x00
GPBPUDPDN	0xE020_0054	R/W	Port Group GPB Power Down Mode Pull-up/down Register	0x00
GPC0CON	0xE020_0060	R/W	Port Group GPC0 Configuration Register	0x00000000
GPC0DAT	0xE020_0064	R/W	Port Group GPC0 Data Register	0x00
GPC0PUD	0xE020_0068	R/W	Port Group GPC0 Pull-up/down Register	0x0155

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Register	Address	R/W	Description	Reset Value
GPC0DRV	0xE020_006C	R/W	Port Group GPC0 Drive Strength Control Register	0x0000
GPC0CONPDN	0xE020_0070	R/W	Port Group GPC0 Power Down Mode Configuration Register	0x00
GPC0PUDPDN	0xE020_0074	R/W	Port Group GPC0 Power Down Mode Pull-up/down Register	0x00
GPC1CON	0xE020_0080	R/W	Port Group GPC1 Configuration Register	0x00000000
GPC1DAT	0xE020_0084	R/W	Port Group GPC1 Data Register	0x00
GPC1PUD	0xE020_0088	R/W	Port Group GPC1 Pull-up/down Register	0x0155
GPC1DRV	0xE020_008C	R/W	Port Group GPC1 Drive Strength Control Register	0x0000
GPC1CONPDN	0xE020_0090	R/W	Port Group GPC1 Power Down Mode Configuration Register	0x00
GPC1PUDPDN	0xE020_0094	R/W	Port Group GPC1 Power Down Mode Pull-up/down Register	0x00
GPD0CON	0xE020_00A0	R/W	Port Group GPD0 Configuration Register	0x00000000
GPD0DAT	0xE020_00A4	R/W	Port Group GPD0 Data Register	0x00
GPD0PUD	0xE020_00A8	R/W	Port Group GPD0 Pull-up/down Register	0x0055
GPD0DRV	0xE020_00AC	R/W	Port Group GPD0 Drive Strength Control Register	0x0000
GPD0CONPDN	0xE020_00B0	R/W	Port Group GPD0 Power Down Mode Configuration Register	0x00
GPD0PUDPDN	0xE020_00B4	R/W	Port Group GPD0 Power Down Mode Pull-up/down Register	0x00
GPD1CON	0xE020_00C0	R/W	Port Group GPD1 Configuration Register	0x00000000
GPD1DAT	0xE020_00C4	R/W	Port Group GPD1 Data Register	0x00
GPD1PUD	0xE020_00C8	R/W	Port Group GPD1 Pull-up/down Register	0x0555
GPD1DRV	0xE020_00CC	R/W	Port Group GPD1 Drive Strength Control Register	0x0000
GPD1CONPDN	0xE020_00D0	R/W	Port Group GPD1 Power Down Mode Configuration Register	0x00
GPD1PUDPDN	0xE020_00D4	R/W	Port Group GPD1 Power Down Mode Pull-up/down Register	0x00
GPE0CON	0xE020_00E0	R/W	Port Group GPE0 Configuration Register	0x00000000
GPE0DAT	0xE020_00E4	R/W	Port Group GPE0 Data Register	0x00
GPE0PUD	0xE020_00E8	R/W	Port Group GPE0 Pull-up/down Register	0x5555
GPE0DRV	0xE020_00EC	R/W	Port Group GPE0 Drive Strength Control Register	0x0000
GPE0CONPDN	0xE020_00F0	R/W	Port Group GPE0 Power Down Mode Configuration Register	0x00

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Register	Address	R/W	Description	Reset Value
GPE0PUDPDN	0xE020_00F4	R/W	Port Group GPE0 Power Down Mode Pull-up/down Register	0x00
GPE1CON	0xE020_0100	R/W	Port Group GPE1 Configuration Register	0x00000000
GPE1DAT	0xE020_0104	R/W	Port Group GPE1 Data Register	0x00
GPE1PUD	0xE020_0108	R/W	Port Group GPE1 Pull-up/down Register	0x0155
GPE1DRV	0xE020_010C	R/W	Port Group GPE1 Drive Strength Control Register	0x0000
GPE1CONPDN	0xE020_0110	R/W	Port Group GPE1 Power Down Mode Configuration Register	0x00
GPE1PUDPDN	0xE020_0114	R/W	Port Group GPE1 Power Down Mode Pull-up/down Register	0x00
GPF0CON	0xE020_0120	R/W	Port Group GPF0 Configuration Register	0x00000000
GPF0DAT	0xE020_0124	R/W	Port Group GPF0 Data Register	0x00
GPF0PUD	0xE020_0128	R/W	Port Group GPF0 Pull-up/down Register	0x5555
GPF0DRV	0xE020_012C	R/W	Port Group GPF0 Drive Strength Control Register	0x0000
GPF0CONPDN	0xE020_0130	R/W	Port Group GPF0 Power Down Mode Configuration Register	0x00
GPF0PUDPDN	0xE020_0134	R/W	Port Group GPF0 Power Down Mode Pull-up/down Register	0x00
GPF1CON	0xE020_0140	R/W	Port Group GPF1 Configuration Register	0x00000000
GPF1DAT	0xE020_0144	R/W	Port Group GPF1 Data Register	0x00
GPF1PUD	0xE020_0148	R/W	Port Group GPF1 Pull-up/down Register	0x5555
GPF1DRV	0xE020_014C	R/W	Port Group GPF1 Drive Strength Control Register	0x0000
GPF1CONPDN	0xE020_0150	R/W	Port Group GPF1 Power Down Mode Configuration Register	0x00
GPF1PUDPDN	0xE020_0154	R/W	Port Group GPF1 Power Down Mode Pull-up/down Register	0x00
GPF2CON	0xE020_0160	R/W	Port Group GPF2 Configuration Register	0x00000000
GPF2DAT	0xE020_0164	R/W	Port Group GPF2 Data Register	0x00
GPF2PUD	0xE020_0168	R/W	Port Group GPF2 Pull-up/down Register	0x5555
GPF2DRV	0xE020_016C	R/W	Port Group GPF2 Drive Strength Control Register	0x0000
GPF2CONPDN	0xE020_0170	R/W	Port Group GPF2 Power Down Mode Configuration Register	0x00
GPF2PUDPDN	0xE020_0174	R/W	Port Group GPF2 Power Down Mode Pull-up/down Register	0x00
GPF3CON	0xE020_0180	R/W	Port Group GPF3 Configuration Register	0x00000000
GPF3DAT	0xE020_0184	R/W	Port Group GPF3 Data Register	0x00

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Register	Address	R/W	Description	Reset Value
GPF3PUD	0xE020_0188	R/W	Port Group GPF3 Pull-up/down Register	0x0555
GPF3DRV	0xE020_018C	R/W	Port Group GPF3 Drive Strength Control Register	0x0000
GPF3CONPDN	0xE020_0190	R/W	Port Group GPF3 Power Down Mode Configuration Register	0x00
GPF3PUDPDN	0xE020_0194	R/W	Port Group GPF3 Power Down Mode Pull-up/down Register	0x00
GPG0CON	0xE020_01A0	R/W	Port Group GPG0 Configuration Register	0x00000000
GPG0DAT	0xE020_01A4	R/W	Port Group GPG0 Data Register	0x00
GPG0PUD	0xE020_01A8	R/W	Port Group GPG0 Pull-up/down Register	0x1555
GPG0DRV	0xE020_01AC	R/W	Port Group GPG0 Drive Strength Control Register	0x2AAA
GPG0CONPDN	0xE020_01B0	R/W	Port Group GPG0 Power Down Mode Configuration Register	0x00
GPG0PUDPDN	0xE020_01B4	R/W	Port Group GPG0 Power Down Mode Pull-up/down Register	0x00
GPG1CON	0xE020_01C0	R/W	Port Group GPG1 Configuration Register	0x00000000
GPG1DAT	0xE020_01C4	R/W	Port Group GPG1 Data Register	0x00
GPG1PUD	0xE020_01C8	R/W	Port Group GPG1 Pull-up/down Register	0x1555
GPG1DRV	0xE020_01CC	R/W	Port Group GPG1 Drive Strength Control Register	0x0000
GPG1CONPDN	0xE020_01D0	R/W	Port Group GPG1 Power Down Mode Configuration Register	0x00
GPG1PUDPDN	0xE020_01D4	R/W	Port Group GPG1 Power Down Mode Pull-up/down Register	0x00
GPG2CON	0xE020_01E0	R/W	Port Group GPG2 Configuration Register	0x00000000
GPG2DAT	0xE020_01E4	R/W	Port Group GPG2 Data Register	0x00
GPG2PUD	0xE020_01E8	R/W	Port Group GPG2 Pull-up/down Register	0x1555
GPG2DRV	0xE020_01EC	R/W	Port Group GPG2 Drive Strength Control Register	0x0000
GPG2CONPDN	0xE020_01F0	R/W	Port Group GPG2 Power Down Mode Configuration Register	0x00
GPG2PUDPDN	0xE020_01F4	R/W	Port Group GPG2 Power Down Mode Pull-up/ down Register	0x00
GPG3CON	0xE020_0200	R/W	Port Group GPG3 Configuration Register	0x00000000
GPG3DAT	0xE020_0204	R/W	Port Group GPG3 Data Register	0x00
GPG3PUD	0xE020_0208	R/W	Port Group GPG3 Pull-up/down Register	0x1555
GPG3DRV	0xE020_020C	R/W	Port Group GPG3 Drive Strength Control Register	0x0000
GPG3CONPDN	0xE020_0210	R/W	Port Group GPG3 Power Down Mode Configuration Register	0x00

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Register	Address	R/W	Description	Reset Value
GPG3PUDPDN	0xE020_0214	R/W	Port Group GPG3 Power Down Mode Pull-up/ down Register	0x00
GPICON	0xE020_0220	R/W	Port Group GPI Configuration Register	0x02222222
GPIDAT	0xE020_0224	R/W	Reserved GPI is only used for I2S0 and PCM0	0x00
GPIPUD	0xE020_0228	R/W	Port Group GPI Pull-up/ down Register	0x1555
GPIDRV	0xE020_022C	R/W	Port Group GPI Drive Strength Control Register	0x0000
GPICONPDN	0xE020_0230	R/W	Reserved (Controlled by PAD_PDN_CTRL register at AUDIO_SS)	0x00
GPIPUDPDN	0xE020_0234	R/W	Reserved (Controlled by GPIPUD register)	0x00
GPJ0CON	0xE020_0240	R/W	Port Group GPJ0 Configuration Register	0x00000000
GPJ0DAT	0xE020_0244	R/W	Port Group GPJ0 Data Register	0x00
GPJ0PUD	0xE020_0248	R/W	Port Group GPJ0 Pull-up/ down Register	0x5555
GPJ0DRV	0xE020_024C	R/W	Port Group GPJ0 Drive Strength Control Register	0x0000
GPJ0CONPDN	0xE020_0250	R/W	Port Group GPJ0 Power Down Mode Configuration Register	0x00
GPJ0PUDPDN	0xE020_0254	R/W	Port Group GPJ0 Power Down Mode Pull-up/ down Register	0x00
GPJ1CON	0xE020_0260	R/W	Port Group GPJ1 Configuration Register	0x00000000
GPJ1DAT	0xE020_0264	R/W	Port Group GPJ1 Data Register	0x00
GPJ1PUD	0xE020_0268	R/W	Port Group GPJ1 Pull-up/ down Register	0x0555
GPJ1DRV	0xE020_026C	R/W	Port Group GPJ1 Drive Strength Control Register	0x0000
GPJ1CONPDN	0xE020_0270	R/W	Port Group GPJ1 Power Down Mode Configuration Register	0x00
GPJ1PUDPDN	0xE020_0274	R/W	Port Group GPJ1 Power Down Mode Pull-up/down Register	0x00
GPJ2CON	0xE020_0280	R/W	Port Group GPJ2 Configuration Register	0x00000000
GPJ2DAT	0xE020_0284	R/W	Port Group GPJ2 Data Register	0x00
GPJ2PUD	0xE020_0288	R/W	Port Group GPJ2 Pull-up/ down Register	0x5555
GPJ2DRV	0xE020_028C	R/W	Port Group GPJ2 Drive Strength Control Register	0x0000
GPJ2CONPDN	0xE020_0290	R/W	Port Group GPJ2 Power Down Mode Configuration Register	0x00
GPJ2PUDPDN	0xE020_0294	R/W	Port Group GPJ2 Power Down Mode Pull-up/down Register	0x00
GPJ3CON	0xE020_02A0	R/W	Port Group GPJ3 Configuration Register	0x00000000
GPJ3DAT	0xE020_02A4	R/W	Port Group GPJ3 Data Register	0x00

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Register	Address	R/W	Description	Reset Value
GPJ3PUD	0xE020_02A8	R/W	Port Group GPJ3 Pull-up/ down Register	0x5555
GPJ3DRV	0xE020_02AC	R/W	Port Group GPJ3 Drive Strength Control Register	0x0000
GPJ3CONPDN	0xE020_02B0	R/W	Port Group GPJ3 Power Down Mode Configuration Register	0x00
GPJ3PUDPDN	0xE020_02B4	R/W	Port Group GPJ3 Power Down Mode Pull-up/down Register	0x00
GPJ4CON	0xE020_02C0	R/W	Port Group GPJ4 Configuration Register	0x00000000
GPJ4DAT	0xE020_02C4	R/W	Port Group GPJ4 Data Register	0x00
GPJ4PUD	0xE020_02C8	R/W	Port Group GPJ4 Pull-up/ down Register	0x0155
GPJ4DRV	0xE020_02CC	R/W	Port Group GPJ4 Drive Strength Control Register	0x0000
GPJ4CONPDN	0xE020_02D0	R/W	Port Group GPJ4 Power Down Mode Configuration Register	0x00
GPJ4PUDPDN	0xE020_02D4	R/W	Port Group GPJ4 Power Down Mode Pull-up/down Register	0x00
MP0_1CON	0xE020_02E0	R/W	Port Group MP0_1 Configuration Register	0x22553322
MP0_1DAT	0xE020_02E4	R/W	Port Group MP0_1 Data Register	0x00
MP0_1PUD	0xE020_02E8	R/W	Port Group MP0_1 Pull-up/down Register	0x0000
MP0_1DRV	0xE020_02EC	R/W	Port Group MP0_1 Drive Strength Control Register	0xAAAA
MP0_1CONPDN	0xE020_02F0	R/W	Port Group MP0_1 Power Down Mode Configuration Register	0x00
MP0_1PUDPDN	0xE020_02F4	R/W	Port Group MP0_1 Power Down Mode Pull-up/ down Register	0x00
MP0_2CON	0xE020_0300	R/W	Port Group MP0_2 Configuration Register	0x00002222
MP0_2DAT	0xE020_0304	R/W	Port Group MP0_2 Data Register	0x00
MP0_2PUD	0xE020_0308	R/W	Port Group MP0_2 Pull-up/ down Register	0x0000
MP0_2DRV	0xE020_030C	R/W	Port Group MP0_2 Drive Strength Control Register	0x00AA
MP0_2CONPDN	0xE020_0310	R/W	Port Group MP0_2 Power Down Mode Configuration Register	0x00
MP0_2PUDPDN	0xE020_0314	R/W	Port Group MP0_2 Power Down Mode Pull-up/ down Register	0x00
MP0_3CON	0xE020_0320	R/W	Port Group MP0_3 Configuration Register	0x22552555
MP0_3DAT	0xE020_0324	R/W	Port Group MP0_3 Data Register	0x00
MP0_3PUD	0xE020_0328	R/W	Port Group MP0_3 Pull-up/down Register	0x0000
MP0_3DRV	0xE020_032C	R/W	Port Group MP0_3 Drive Strength Control Register	0xAAAA
MP0_3CONPDN	0xE020_0330	R/W	Port Group MP0_3 Power Down Mode Configuration Register	0x00

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Register	Address	R/W	Description	Reset Value
MP0_3PUDPDN	0xE020_0334	R/W	Port Group MP0_3 Power Down Mode Pull-up/ down Register	0x00
MP0_4CON	0xE020_0340	R/W	Port Group MP0_4 Configuration Register	0x22222222
MP0_4DAT	0xE020_0344	R/W	Port Group MP0_4 Data Register	0x00
MP0_4PUD	0xE020_0348	R/W	Port Group MP0_4 Pull-up/ down Register	0x0000
MP0_4DRV	0xE020_034C	R/W	Port Group MP0_4 Drive Strength Control Register	0xAAAA
MP0_4CONPDN	0xE020_0350	R/W	Port Group MP0_4 Power Down Mode Configuration Register	0x00
MP0_4PUDPDN	0xE020_0354	R/W	Port Group MP0_4 Power Down Mode Pull-up/ down Register	0x00
MP0_5CON	0xE020_0360	R/W	Port Group MP0_5 Configuration Register	0x22222222
MP0_5DAT	0xE020_0364	R/W	Port Group MP0_5 Data Register	0x00
MP0_5PUD	0xE020_0368	R/W	Port Group MP0_5 Pull-up/ down Register	0x0000
MP0_5DRV	0xE020_036C	R/W	Port Group MP0_5 Drive Strength Control Register	0xAAAA
MP0_5CONPDN	0xE020_0370	R/W	Port Group MP0_5 Power Down Mode Configuration Register	0x00
MP0_5PUDPDN	0xE020_0374	R/W	Port Group MP0_5 Power Down Mode Pull-up/ down Register	0x00
MP0_6CON	0xE020_0380	R/W	Port Group MP0_6 Configuration Register	0x22222222
MP0_6DAT	0xE020_0384	R/W	Port Group MP0_6 Data Register	0x00
MP0_6PUD	0xE020_0388	R/W	Port Group MP0_6 Pull-up/ down Register	0x0000
MP0_6DRV	0xE020_038C	R/W	Port Group MP0_6 Drive Strength Control Register	0xAAAA
MP0_6CONPDN	0xE020_0390	R/W	Port Group MP0_6 Power Down Mode Configuration Register	0x00
MP0_6PUDPDN	0xE020_0394	R/W	Port Group MP0_6 Power Down Mode Pull-up/ down Register	0x00
MP0_7CON	0xE020_03A0	R/W	Port Group MP0_7 Configuration Register	0x22222222
MP0_7DAT	0xE020_03A4	R/W	Port Group MP0_7 Data Register	0x00
MP0_7PUD	0xE020_03A8	R/W	Port Group MP0_7 Pull-up/ down Register	0x0000
MP0_7DRV	0xE020_03AC	R/W	Port Group MP0_7 Drive Strength Control Register	0xAAAA
MP0_7CONPDN	0xE020_03B0	R/W	Port Group MP0_7 Power Down Mode Configuration Register	0x00
MP0_7PUDPDN	0xE020_03B4	R/W	Port Group MP0_7 Power Down Mode Pull-up/down Register	0x00
MP1_0CON	0xE020_03C0	R/W	Reserved (Do not use this register)	0x22222222
MP1_0DAT	0xE020_03C4	R/W	Reserved (Do not use this register)	0x00

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Register	Address	R/W	Description	Reset Value
MP1_0PUD	0xE020_03C8	R/W	Reserved (Do not use this register)	0x0000
MP1_0DRV	0xE020_03CC	R/W	Port Group MP1_0 Drive Strength Control Register	0xAAAA
MP1_0CONPDN	0xE020_03D0	R/W	Reserved (Do not use this register)	0x00
MP1_0PUDPDN	0xE020_03D4	R/W	Reserved (Do not use this register)	0x00
MP1_1CON	0xE020_03E0	R/W	Reserved (Do not use this register)	0x22222222
MP1_1DAT	0xE020_03E4	R/W	Reserved (Do not use this register)	0x00
MP1_1PUD	0xE020_03E8	R/W	Reserved (Do not use this register)	0x0000
MP1_1DRV	0xE020_03EC	R/W	Port Group MP1_1 Drive Strength Control Register	0xAAAA
MP1_1CONPDN	0xE020_03F0	R/W	Reserved (Do not use this register)	0x00
MP1_1PUDPDN	0xE020_03F4	R/W	Reserved (Do not use this register)	0x00
MP1_2CON	0xE020_0400	R/W	Reserved (Do not use this register)	0x22222222
MP1_2DAT	0xE020_0404	R/W	Reserved (Do not use this register)	0x00
MP1_2PUD	0xE020_0408	R/W	Reserved (Do not use this register)	0x0000
MP1_2DRV	0xE020_040C	R/W	Port Group MP1_2 Drive Strength Control Register	0xAAAA
MP1_2CONPDN	0xE020_0410	R/W	Reserved (Do not use this register)	0x00
MP1_2PUDPDN	0xE020_0414	R/W	Reserved (Do not use this register)	0x00
MP1_3CON	0xE020_0420	R/W	Reserved (Do not use this register)	0x22222222
MP1_3DAT	0xE020_0424	R/W	Reserved (Do not use this register)	0x00
MP1_3PUD	0xE020_0428	R/W	Reserved (Do not use this register)	0x0000
MP1_3DRV	0xE020_042C	R/W	Port Group MP1_3 Drive Strength Control Register	0xAAAA
MP1_3CONPDN	0xE020_0430	R/W	Reserved (Do not use this register)	0x00
MP1_3PUDPDN	0xE020_0434	R/W	Reserved (Do not use this register)	0x00
MP1_4CON	0xE020_0440	R/W	Reserved (Do not use this register)	0x22222222
MP1_4DAT	0xE020_0444	R/W	Reserved (Do not use this register)	0x00
MP1_4PUD	0xE020_0448	R/W	Reserved (Do not use this register)	0x0000
MP1_4DRV	0xE020_044C	R/W	Port Group MP1_4 Drive Strength Control Register	0xAAAA
MP1_4CONPDN	0xE020_0450	R/W	Reserved (Do not use this register)	0x00
MP1_4PUDPDN	0xE020_0454	R/W	Reserved (Do not use this register)	0x00
MP1_5CON	0xE020_0460	R/W	Reserved (Do not use this register)	0x22222222
MP1_5DAT	0xE020_0464	R/W	Reserved (Do not use this register)	0x00
MP1_5PUD	0xE020_0468	R/W	Reserved (Do not use this register)	0x0000
MP1_5DRV	0xE020_046C	R/W	Port Group MP1_5 Drive Strength Control Register	0xAAAA

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Register	Address	R/W	Description	Reset Value
MP1_5CONPDN	0xE020_0470	R/W	Reserved (Do not use this register)	0x00
MP1_5PUDPDN	0xE020_0474	R/W	Reserved (Do not use this register)	0x00
MP1_6CON	0xE020_0480	R/W	Reserved (Do not use this register)	0x22222222
MP1_6DAT	0xE020_0484	R/W	Reserved (Do not use this register)	0x00
MP1_6PUD	0xE020_0488	R/W	Reserved (Do not use this register)	0x0000
MP1_6DRV	0xE020_048C	R/W	Port Group MP1_6 Drive Strength Control Register	0xAAAA
MP1_6CONPDN	0xE020_0490	R/W	Reserved (Do not use this register)	0x00
MP1_6PUDPDN	0xE020_0494	R/W	Reserved (Do not use this register)	0x00
MP1_7CON	0xE020_04A0	R/W	Reserved (Do not use this register)	0x22222222
MP1_7DAT	0xE020_04A4	R/W	Reserved (Do not use this register)	0x00
MP1_7PUD	0xE020_04A8	R/W	Reserved (Do not use this register)	0x0000
MP1_7DRV	0xE020_04AC	R/W	Port Group MP1_7 Drive Strength Control Register	0xAAAA
MP1_7CONPDN	0xE020_04B0	R/W	Reserved (Do not use this register)	0x00
MP1_7PUDPDN	0xE020_04B4	R/W	Reserved (Do not use this register)	0x00
MP1_8CON	0xE020_04C0	R/W	Reserved (Do not use this register)	0x02222222
MP1_8DAT	0xE020_04C4	R/W	Reserved (Do not use this register)	0x00
MP1_8PUD	0xE020_04C8	R/W	Reserved (Do not use this register)	0x0000
MP1_8DRV	0xE020_04CC	R/W	Port Group MP1_8 Drive Strength Control Register	0x2AAA
MP1_8CONPDN	0xE020_04D0	R/W	Reserved (Do not use this register)	0x00
MP1_8PUDPDN	0xE020_04D4	R/W	Reserved (Do not use this register)	0x00
MP2_0CON	0xE020_04E0	R/W	Reserved (Do not use this register)	0x22222222
MP2_0DAT	0xE020_04E4	R/W	Reserved (Do not use this register)	0x00
MP2_0PUD	0xE020_04E8	R/W	Reserved (Do not use this register)	0x0000
MP2_0DRV	0xE020_04EC	R/W	Port Group MP2_0 Drive Strength Control Register	0xAAAA
MP2_0CONPDN	0xE020_04F0	R/W	Reserved (Do not use this register)	0x00
MP2_0PUDPDN	0xE020_04F4	R/W	Reserved (Do not use this register)	0x00
MP2_1CON	0xE020_0500	R/W	Reserved (Do not use this register)	0x22222222
MP2_1DAT	0xE020_0504	R/W	Reserved (Do not use this register)	0x00
MP2_1PUD	0xE020_0508	R/W	Reserved (Do not use this register)	0x0000
MP2_1DRV	0xE020_050C	R/W	Port Group MP2_1 Drive Strength Control Register	0xAAAA
MP2_1CONPDN	0xE020_0510	R/W	Reserved (Do not use this register)	0x00
MP2_1PUDPDN	0xE020_0514	R/W	Reserved (Do not use this register)	0x00
MP2_2CON	0xE020_0520	R/W	Reserved (Do not use this register)	0x22222222

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Register	Address	R/W	Description	Reset Value
MP2_2DAT	0xE020_0524	R/W	Reserved (Do not use this register)	0x00
MP2_2PUD	0xE020_0528	R/W	Reserved (Do not use this register)	0x0000
MP2_2DRV	0xE020_052C	R/W	Port Group MP2_2 Drive Strength Control Register	0xAAAA
MP2_2CONPDN	0xE020_0530	R/W	Reserved (Do not use this register)	0x00
MP2_2PUDPDN	0xE020_0534	R/W	Reserved (Do not use this register)	0x00
MP2_3CON	0xE020_0540	R/W	Reserved (Do not use this register)	0x22222222
MP2_3DAT	0xE020_0544	R/W	Reserved (Do not use this register)	0x00
MP2_3PUD	0xE020_0548	R/W	Reserved (Do not use this register)	0x0000
MP2_3DRV	0xE020_054C	R/W	Port Group MP2_3 Drive Strength Control Register	0xAAAA
MP2_3CONPDN	0xE020_0550	R/W	Reserved (Do not use this register)	0x00
MP2_3PUDPDN	0xE020_0554	R/W	Reserved (Do not use this register)	0x00
MP2_4CON	0xE020_0560	R/W	Reserved (Do not use this register)	0x22222222
MP2_4DAT	0xE020_0564	R/W	Reserved (Do not use this register)	0x00
MP2_4PUD	0xE020_0568	R/W	Reserved (Do not use this register)	0x0000
MP2_4DRV	0xE020_056C	R/W	Port Group MP2_4 Drive Strength Control Register	0xAAAA
MP2_4CONPDN	0xE020_0570	R/W	Reserved (Do not use this register)	0x00
MP2_4PUDPDN	0xE020_0574	R/W	Reserved (Do not use this register)	0x00
MP2_5CON	0xE020_0580	R/W	Reserved (Do not use this register)	0x22222222
MP2_5DAT	0xE020_0584	R/W	Reserved (Do not use this register)	0x00
MP2_5PUD	0xE020_0588	R/W	Reserved (Do not use this register)	0x0000
MP2_5DRV	0xE020_058C	R/W	Port Group MP2_5 Drive Strength Control Register	0xAAAA
MP2_5CONPDN	0xE020_0590	R/W	Reserved (Do not use this register)	0x00
MP2_5PUDPDN	0xE020_0594	R/W	Reserved (Do not use this register)	0x00
MP2_6CON	0xE020_05A0	R/W	Reserved (Do not use this register)	0x22222222
MP2_6DAT	0xE020_05A4	R/W	Reserved (Do not use this register)	0x00
MP2_6PUD	0xE020_05A8	R/W	Reserved (Do not use this register)	0x0000
MP2_6DRV	0xE020_05AC	R/W	Port Group MP2_6 Drive Strength Control Register	0xAAAA
MP2_6CONPDN	0xE020_05B0	R/W	Reserved (Do not use this register)	0x00
MP2_6PUDPDN	0xE020_05B4	R/W	Reserved (Do not use this register)	0x00
MP2_7CON	0xE020_05C0	R/W	Reserved (Do not use this register)	0x22222222
MP2_7DAT	0xE020_05C4	R/W	Reserved (Do not use this register)	0x00
MP2_7PUD	0xE020_05C8	R/W	Reserved (Do not use this register)	0x0000

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Register	Address	R/W	Description	Reset Value
MP2_7DRV	0xE020_05CC	R/W	Port Group MP2_7 Drive Strength Control Register	0xAAAA
MP2_7CONPDN	0xE020_05D0	R/W	Reserved (Do not use this register)	0x00
MP2_7PUDPDN	0xE020_05D4	R/W	Reserved (Do not use this register)	0x00
MP2_8CON	0xE020_05E0	R/W	Reserved (Do not use this register)	0x02222222
MP2_8DAT	0xE020_05E4	R/W	Reserved (Do not use this register)	0x00
MP2_8PUD	0xE020_05E8	R/W	Reserved (Do not use this register)	0x0000
MP2_8DRV	0xE020_05EC	R/W	Port Group MP2_8 Drive Strength Control Register	0x2AAA
MP2_8CONPDN	0xE020_05F0	R/W	Reserved (Do not use this register)	0x00
MP2_8PUDPDN	0xE020_05F4	R/W	Reserved (Do not use this register)	0x00
ETC0PUD	0xE020_0608	R/W	Port Group ETC0 Pull-up/ down Register	0x0000
ETC0DRV	0xE020_060C	R/W	Port Group ETC0 Drive Strength Control Register	0x0000
ETC1PUD	0xE020_0628	R/W	Port Group ETC1 Pull-up/ down Register	0x0000
ETC1DRV	0xE020_062C	R/W	Port Group ETC1 Drive Strength Control Register	0x0000
ETC2PUD	0xE020_0648	R/W	Port Group ETC2 Pull-up/down Register	0x0000
ETC2DRV	0xE020_064C	R/W	Port Group ETC2 Drive Strength Control Register	0x0202
GPA0_INT_CON	0xE020_0700	R/W	GPIO Interrupt GPA0_INT Configuration Register	0x0
GPA1_INT_CON	0xE020_0704	R/W	GPIO Interrupt GPA1_INT Configuration Register	0x0
GPB_INT_CON	0xE020_0708	R/W	GPIO Interrupt GPB_INT Configuration Register	0x0
GPC0_INT_CON	0xE020_070C	R/W	GPIO Interrupt GPC0_INT Configuration Register	0x0
GPC1_INT_CON	0xE020_0710	R/W	GPIO Interrupt GPC1_INT Configuration Register	0x0
GPD0_INT_CON	0xE020_0714	R/W	GPIO Interrupt GPD0_INT Configuration Register	0x0
GPD1_INT_CON	0xE020_0718	R/W	GPIO Interrupt GPD1_INT Configuration Register	0x0
GPE0_INT_CON	0xE020_071C	R/W	GPIO Interrupt GPE0_INT Configuration Register	0x0
GPE1_INT_CON	0xE020_0720	R/W	GPIO Interrupt GPE1_INT Configuration Register	0x0
GPF0_INT_CON	0xE020_0724	R/W	GPIO Interrupt GPF0_INT Configuration Register	0x0

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Register	Address	R/W	Description	Reset Value
GPF1_INT_CON	0xE020_0728	R/W	GPIO Interrupt GPF1_INT Configuration Register	0x0
GPF2_INT_CON	0xE020_072C	R/W	GPIO Interrupt GPF2_INT Configuration Register	0x0
GPF3_INT_CON	0xE020_0730	R/W	GPIO Interrupt GPF3_INT Configuration Register	0x0
GPG0_INT_CON	0xE020_0734	R/W	GPIO Interrupt GPG0_INT Configuration Register	0x0
GPG1_INT_CON	0xE020_0738	R/W	GPIO Interrupt GPG1_INT Configuration Register	0x0
GPG2_INT_CON	0xE020_073C	R/W	GPIO Interrupt GPG2_INT Configuration Register	0x0
GPG3_INT_CON	0xE020_0740	R/W	GPIO Interrupt GPG3_INT Configuration Register	0x0
GPJ0_INT_CON	0xE020_0744	R/W	GPIO Interrupt GPJ0_INT Configuration Register	0x0
GPJ1_INT_CON	0xE020_0748	R/W	GPIO Interrupt GPJ1_INT Configuration Register	0x0
GPJ2_INT_CON	0xE020_074C	R/W	GPIO Interrupt GPJ2_INT Configuration Register	0x0
GPJ3_INT_CON	0xE020_0750	R/W	GPIO Interrupt GPJ3_INT Configuration Register	0x0
GPJ4_INT_CON	0xE020_0754	R/W	GPIO Interrupt GPJ4_INT Configuration Register	0x0
GPA0_INT_FLTCON0	0xE020_0800	R/W	GPIO Interrupt GPA0_INT Filter Configuration Register 0	0x0
GPA0_INT_FLTCON1	0xE020_0804	R/W	GPIO Interrupt GPA0_INT Filter Configuration Register 1	0x0
GPA1_INT_FLTCON0	0xE020_0808	R/W	GPIO Interrupt GPA1_INT Filter Configuration Register 0	0x0
GPA1_INT_FLTCON1	0xE020_080C	R/W	GPIO Interrupt GPA1_INT Filter Configuration Register 1	0x0
GPB_INT_FLTCON0	0xE020_0810	R/W	GPIO Interrupt GPB_INT Filter Configuration Register 0	0x0
GPB_INT_FLTCON1	0xE020_0814	R/W	GPIO Interrupt GPB_INT Filter Configuration Register 1	0x0
GPC0_INT_FLTCON0	0xE020_0818	R/W	GPIO Interrupt GPC0_INT Filter Configuration Register 0	0x0
GPC0_INT_FLTCON1	0xE020_081C	R/W	GPIO Interrupt GPC0_INT Filter Configuration Register 1	0x0
GPC1_INT_FLTCON0	0xE020_0820	R/W	GPIO Interrupt GPC1_INT Filter Configuration Register 0	0x0

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Register	Address	R/W	Description	Reset Value
GPC1_INT_FLTCON1	0xE020_0824	R/W	GPIO Interrupt GPC1_INT Filter Configuration Register 1	0x0
GPD0_INT_FLTCON0	0xE020_0828	R/W	GPIO Interrupt GPD0_INT Filter Configuration Register 0	0x0
GPD0_INT_FLTCON1	0xE020_082C	R/W	GPIO Interrupt GPD0_INT Filter Configuration Register 1	0x0
GPD1_INT_FLTCON0	0xE020_0830	R/W	GPIO Interrupt GPD1_INT Filter Configuration Register 0	0x0
GPD1_INT_FLTCON1	0xE020_0834	R/W	GPIO Interrupt GPD1_INT Filter Configuration Register 1	0x0
GPE0_INT_FLTCON0	0xE020_0838	R/W	GPIO Interrupt GPE0_INT Filter Configuration Register 0	0x0
GPE0_INT_FLTCON1	0xE020_083C	R/W	GPIO Interrupt GPE0_INT Filter Configuration Register 1	0x0
GPE1_INT_FLTCON0	0xE020_0840	R/W	GPIO Interrupt GPE1_INT Filter Configuration Register 0	0x0
GPE1_INT_FLTCON1	0xE020_0844	R/W	GPIO Interrupt GPE1_INT Filter Configuration Register 1	0x0
GPF0_INT_FLTCON0	0xE020_0848	R/W	GPIO Interrupt GPF0_INT Filter Configuration Register 0	0x0
GPF0_INT_FLTCON1	0xE020_084C	R/W	GPIO Interrupt GPF0_INT Filter Configuration Register 1	0x0
GPF1_INT_FLTCON0	0xE020_0850	R/W	GPIO Interrupt GPF1_INT Filter Configuration Register 0	0x0
GPF1_INT_FLTCON1	0xE020_0854	R/W	GPIO Interrupt GPF1_INT Filter Configuration Register 1	0x0
GPF2_INT_FLTCON0	0xE020_0858	R/W	GPIO Interrupt GPF2_INT Filter Configuration Register 0	0x0
GPF2_INT_FLTCON1	0xE020_085C	R/W	GPIO Interrupt GPF2_INT Filter Configuration Register 1	0x0
GPF3_INT_FLTCON0	0xE020_0860	R/W	GPIO Interrupt GPF3_INT Filter Configuration Register 0	0x0
GPF3_INT_FLTCON1	0xE020_0864	R/W	GPIO Interrupt GPF3_INT Filter Configuration Register 1	0x0
GPG0_INT_FLTCON0	0xE020_0868	R/W	GPIO Interrupt GPG0_INT Filter Configuration Register 0	0x0
GPG0_INT_FLTCON1	0xE020_086C	R/W	GPIO Interrupt GPG0_INT Filter Configuration Register 1	0x0
GPG1_INT_FLTCON0	0xE020_0870	R/W	GPIO Interrupt GPG1_INT Filter Configuration Register 0	0x0
GPG1_INT_FLTCON1	0xE020_0874	R/W	GPIO Interrupt GPG1_INT Filter Configuration Register 1	0x0

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Register	Address	R/W	Description	Reset Value
GPG2_INT_FLTCON0	0xE020_0878	R/W	GPIO Interrupt GPG2_INT Filter Configuration Register 0	0x0
GPG2_INT_FLTCON1	0xE020_087C	R/W	GPIO Interrupt GPG2_INT Filter Configuration Register 1	0x0
GPG3_INT_FLTCON0	0xE020_0880	R/W	GPIO Interrupt GPG3_INT Filter Configuration Register 0	0x0
GPG3_INT_FLTCON1	0xE020_0884	R/W	GPIO Interrupt GPG3_INT Filter Configuration Register 1	0x0
GPJ0_INT_FLTCON0	0xE020_0888	R/W	GPIO Interrupt GPJ0_INT Filter Configuration Register 0	0x0
GPJ0_INT_FLTCON1	0xE020_088C	R/W	GPIO Interrupt GPJ0_INT Filter Configuration Register 1	0x0
GPJ1_INT_FLTCON0	0xE020_0890	R/W	GPIO Interrupt GPJ1_INT Filter Configuration Register 0	0x0
GPJ1_INT_FLTCON1	0xE020_0894	R/W	GPIO Interrupt GPJ1_INT Filter Configuration Register 1	0x0
GPJ2_INT_FLTCON0	0xE020_0898	R/W	GPIO Interrupt GPJ2_INT Filter Configuration Register 0	0x0
GPJ2_INT_FLTCON1	0xE020_089C	R/W	GPIO Interrupt GPJ2_INT Filter Configuration Register 1	0x0
GPJ3_INT_FLTCON0	0xE020_08A0	R/W	GPIO Interrupt GPJ3_INT Filter Configuration Register 0	0x0
GPJ3_INT_FLTCON1	0xE020_08A4	R/W	GPIO Interrupt GPJ3_INT Filter Configuration Register 1	0x0
GPJ4_INT_FLTCON0	0xE020_08A8	R/W	GPIO Interrupt GPJ4_INT Filter Configuration Register 0	0x0
GPJ4_INT_FLTCON1	0xE020_08AC	R/W	GPIO Interrupt GPJ4_INT Filter Configuration Register 1	0x0
GPA0_INT_MASK	0xE020_0900	R/W	GPIO Interrupt GPA0_INT Mask Register	0x000000FF
GPA1_INT_MASK	0xE020_0904	R/W	GPIO Interrupt GPA1_INT Mask Register	0x0000000F
GPB_INT_MASK	0xE020_0908	R/W	GPIO Interrupt GPB_INT Mask Register	0x000000FF
GPC0_INT_MASK	0xE020_090C	R/W	GPIO Interrupt GPC0_INT Mask Register	0x0000001F
GPC1_INT_MASK	0xE020_0910	R/W	GPIO Interrupt GPC1_INT Mask Register	0x0000001F
GPD0_INT_MASK	0xE020_0914	R/W	GPIO Interrupt GPD0_INT Mask Register	0x0000000F
GPD1_INT_MASK	0xE020_0918	R/W	GPIO Interrupt GPD1_INT Mask Register	0x0000003F
GPE0_INT_MASK	0xE020_091C	R/W	GPIO Interrupt GPE0_INT Mask Register	0x000000FF
GPE1_INT_MASK	0xE020_0920	R/W	GPIO Interrupt GPE1_INT Mask Register	0x0000001F
GPF0_INT_MASK	0xE020_0924	R/W	GPIO Interrupt GPF0_INT Mask Register	0x000000FF
GPF1_INT_MASK	0xE020_0928	R/W	GPIO Interrupt GPF1_INT Mask Register	0x000000FF
GPF2_INT_MASK	0xE020_092C	R/W	GPIO Interrupt GPF2_INT Mask Register	0x000000FF
GPF3_INT_MASK	0xE020_0930	R/W	GPIO Interrupt GPF3_INT Mask Register	0x0000003F

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Register	Address	R/W	Description	Reset Value
GPG0_INT_MASK	0xE020_0934	R/W	GPIO Interrupt GPG0_INT Mask Register	0x0000007F
GPG1_INT_MASK	0xE020_0938	R/W	GPIO Interrupt GPG1_INT Mask Register	0x0000007F
GPG2_INT_MASK	0xE020_093C	R/W	GPIO Interrupt GPG2_INT Mask Register	0x0000007F
GPG3_INT_MASK	0xE020_0940	R/W	GPIO Interrupt GPG3_INT Mask Register	0x0000007F
GPJ0_INT_MASK	0xE020_0944	R/W	GPIO Interrupt GPJ0_INT Mask Register	0x000000FF
GPJ1_INT_MASK	0xE020_0948	R/W	GPIO Interrupt GPJ1_INT Mask Register	0x0000003F
GPJ2_INT_MASK	0xE020_094C	R/W	GPIO Interrupt GPJ2_INT Mask Register	0x000000FF
GPJ3_INT_MASK	0xE020_0950	R/W	GPIO Interrupt GPJ3_INT Mask Register	0x000000FF
GPJ4_INT_MASK	0xE020_0954	R/W	GPIO Interrupt GPJ4_INT Mask Register	0x0000001F
GPA0_INT_PEND	0xE020_0A00	R/W	GPIO Interrupt GPA0_INT Pending Register	0x0
GPA1_INT_PEND	0xE020_0A04	R/W	GPIO Interrupt GPA1_INT Pending Register	0x0
GPB_INT_PEND	0xE020_0A08	R/W	GPIO Interrupt GPB_INT Pending Register	0x0
GPC0_INT_PEND	0xE020_0A0C	R/W	GPIO Interrupt GPC0_INT Pending Register	0x0
GPC1_INT_PEND	0xE020_0A10	R/W	GPIO Interrupt GPC1_INT Pending Register	0x0
GPD0_INT_PEND	0xE020_0A14	R/W	GPIO Interrupt GPD0_INT Pending Register	0x0
GPD1_INT_PEND	0xE020_0A18	R/W	GPIO Interrupt GPD1_INT Pending Register	0x0
GPE0_INT_PEND	0xE020_0A1C	R/W	GPIO Interrupt GPE0_INT Pending Register	0x0
GPE1_INT_PEND	0xE020_0A20	R/W	GPIO Interrupt GPE1_INT Pending Register	0x0
GPF0_INT_PEND	0xE020_0A24	R/W	GPIO Interrupt GPF0_INT Pending Register	0x0
GPF1_INT_PEND	0xE020_0A28	R/W	GPIO Interrupt GPF1_INT Pending Register	0x0
GPF2_INT_PEND	0xE020_0A2C	R/W	GPIO Interrupt GPF2_INT Pending Register	0x0
GPF3_INT_PEND	0xE020_0A30	R/W	GPIO Interrupt GPF3_INT Pending Register	0x0
GPG0_INT_PEND	0xE020_0A34	R/W	GPIO Interrupt GPG0_INT Pending Register	0x0
GPG1_INT_PEND	0xE020_0A38	R/W	GPIO Interrupt GPG1_INT Pending Register	0x0
GPG2_INT_PEND	0xE020_0A3C	R/W	GPIO Interrupt GPG2_INT Pending Register	0x0
GPG3_INT_PEND	0xE020_0A40	R/W	GPIO Interrupt GPG3_INT Pending Register	0x0
GPJ0_INT_PEND	0xE020_0A44	R/W	GPIO Interrupt GPJ0_INT Pending Register	0x0
GPJ1_INT_PEND	0xE020_0A48	R/W	GPIO Interrupt GPJ1_INT Pending Register	0x0
GPJ2_INT_PEND	0xE020_0A4C	R/W	GPIO Interrupt GPJ2_INT Pending Register	0x0
GPJ3_INT_PEND	0xE020_0A50	R/W	GPIO Interrupt GPJ3_INT Pending Register	0x0
GPJ4_INT_PEND	0xE020_0A54	R/W	GPIO Interrupt GPJ4_INT Pending Register	0x0

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Register	Address	R/W	Description	Reset Value
GPIO_INT_GRPPRI	0xE020_0B00	R/W	GPIO Interrupt Group Priority Control Register	0x0
GPIO_INT_PRIORITY	0xE020_0B04	R/W	GPIO Interrupt Priority Control Register	0x00
GPIO_INT_SERVICE	0xE020_0B08	R	Current Service Register	0x00
GPIO_INT_SERVICE_PEND	0xE020_0B0C	R	Current Service Pending Register	0x00
GPIO_INT_GRPFIXPRI	0xE020_0B10	R/W	GPIO Interrupt Group Fixed Priority Control Register	0x00
GPA0_INT_FIXPRI	0xE020_0B14	R/W	GPIO Interrupt 1 Fixed Priority Control Register	0x00
GPA1_INT_FIXPRI	0xE020_0B18	R/W	GPIO Interrupt 2 Fixed Priority Control Register	0x00
GPB_INT_FIXPRI	0xE020_0B1C	R/W	GPIO Interrupt 3 Fixed Priority Control Register	0x00
GPC0_INT_FIXPRI	0xE020_0B20	R/W	GPIO Interrupt 4 Fixed Priority Control Register	0x00
GPC1_INT_FIXPRI	0xE020_0B24	R/W	GPIO Interrupt 5 Fixed Priority Control Register	0x00
GPD0_INT_FIXPRI	0xE020_0B28	R/W	GPIO Interrupt 6 Fixed Priority Control Register	0x00
GPD1_INT_FIXPRI	0xE020_0B2C	R/W	GPIO Interrupt 7 Fixed Priority Control Register	0x00
GPE0_INT_FIXPRI	0xE020_0B30	R/W	GPIO Interrupt 8 Fixed Priority Control Register	0x00
GPE1_INT_FIXPRI	0xE020_0B34	R/W	GPIO Interrupt 9 Fixed Priority Control Register	0x00
GPF0_INT_FIXPRI	0xE020_0B38	R/W	GPIO Interrupt 10 Fixed Priority Control Register	0x00
GPF1_INT_FIXPRI	0xE020_0B3C	R/W	GPIO Interrupt 11 Fixed Priority Control Register	0x00
GPF2_INT_FIXPRI	0xE020_0B40	R/W	GPIO Interrupt 12 Fixed Priority Control Register	0x00
GPF3_INT_FIXPRI	0xE020_0B44	R/W	GPIO Interrupt 13 Fixed Priority Control Register	0x00
GPG0_INT_FIXPRI	0xE020_0B48	R/W	GPIO Interrupt 14 Fixed Priority Control Register	0x00
GPG1_INT_FIXPRI	0xE020_0B4C	R/W	GPIO Interrupt 15 Fixed Priority Control Register	0x00
GPG2_INT_FIXPRI	0xE020_0B50	R/W	GPIO Interrupt 16 Fixed Priority Control Register	0x00
GPG3_INT_FIXPRI	0xE020_0B54	R/W	GPIO Interrupt 17 Fixed Priority Control Register	0x00

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Register	Address	R/W	Description	Reset Value
GPJ0_INT_FIXPRI	0xE020_0B58	R/W	GPIO Interrupt 18 Fixed Priority Control Register	0x00
GPJ1_INT_FIXPRI	0xE020_0B5C	R/W	GPIO Interrupt 19 Fixed Priority Control Register	0x00
GPJ2_INT_FIXPRI	0xE020_0B60	R/W	GPIO Interrupt 20 Fixed Priority Control Register	0x00
GPJ3_INT_FIXPRI	0xE020_0B64	R/W	GPIO Interrupt 21 Fixed Priority Control Register	0x00
GPJ4_INT_FIXPRI	0xE020_0B68	R/W	GPIO Interrupt 22 Fixed Priority Control Register	0x00
GPH0CON	0xE020_0C00	R/W	Port Group GPH0 Configuration Register	0x00000000
GPH0DAT	0xE020_0C04	R/W	Port Group GPH0 Data Register	0x00
GPH0PUD	0xE020_0C08	R/W	Port Group GPH0 Pull-up/down Register	0x5555
GPH0DRV	0xE020_0C0C	R/W	Port Group GPH0 Drive Strength Control Register	0x0000
GPH1CON	0xE020_0C20	R/W	Port Group GPH1 Configuration Register	0x00000000
GPH1DAT	0xE020_0C24	R/W	Port Group GPH1 Data Register	0x00
GPH1PUD	0xE020_0C28	R/W	Port Group GPH1 Pull-up/ down Register	0x5555
GPH1DRV	0xE020_0C2C	R/W	Port Group GPH1 Drive Strength Control Register	0x0000
GPH2CON	0xE020_0C40	R/W	Port Group GPH2 Configuration Register	0x00000000
GPH2DAT	0xE020_0C44	R/W	Port Group GPH2 Data Register	0x00
GPH2PUD	0xE020_0C48	R/W	Port Group GPH2 Pull-up/ down Register	0x5555
GPH2DRV	0xE020_0C4C	R/W	Port Group GPH2 Drive Strength Control Register	0x0000
GPH3CON	0xE020_0C60	R/W	Port Group GPH3 Configuration Register	0x00000000
GPH3DAT	0xE020_0C64	R/W	Port Group GPH3 Data Register	0x00
GPH3PUD	0xE020_0C68	R/W	Port Group GPH3 Pull-up/ down Register	0x5555
GPH3DRV	0xE020_0C6C	R/W	Port Group GPH3 Drive Strength Control Register	0x0000
EXT_INT_0_CON	0xE020_0E00	R/W	External Interrupt EXT_INT[0] ~ EXT_INT[7] Configuration Register	0x0
EXT_INT_1_CON	0xE020_0E04	R/W	External Interrupt EXT_INT[8] ~ EXT_INT[15] Configuration Register	0x0
EXT_INT_2_CON	0xE020_0E08	R/W	External Interrupt EXT_INT[16] ~ EXT_INT[23] Configuration Register	0x0
EXT_INT_3_CON	0xE020_0E0C	R/W	External Interrupt EXT_INT[24] ~ EXT_INT[31] Configuration Register	0x0
EXT_INT_0_FLTCON0	0xE020_0E80	R/W	External Interrupt EXT_INT[0] ~ EXT_INT[7] Filter Configuration Register 0	0x80808080

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Register	Address	R/W	Description	Reset Value
EXT_INT_0_FLTCON1	0xE020_0E84	R/W	External Interrupt EXT_INT[0] ~ EXT_INT[7] Filter Configuration Register 1	0x80808080
EXT_INT_1_FLTCON0	0xE020_0E88	R/W	External Interrupt EXT_INT[8] ~ EXT_INT[15] Filter Configuration Register 0	0x80808080
EXT_INT_1_FLTCON1	0xE020_0E8C	R/W	External Interrupt EXT_INT[8] ~ EXT_INT[15] Filter Configuration Register 1	0x80808080
EXT_INT_2_FLTCON0	0xE020_0E90	R/W	External Interrupt EXT_INT[16] ~ EXT_INT[23] Filter Configuration Register 0	0x80808080
EXT_INT_2_FLTCON1	0xE020_0E94	R/W	External Interrupt EXT_INT[16] ~ EXT_INT[23] Filter Configuration Register 1	0x80808080
EXT_INT_3_FLTCON0	0xE020_0E98	R/W	External Interrupt EXT_INT[24] ~ EXT_INT[31] Filter Configuration Register 0	0x80808080
EXT_INT_3_FLTCON1	0xE020_0E9C	R/W	External Interrupt EXT_INT[24] ~ EXT_INT[31] Filter Configuration Register 1	0x80808080
EXT_INT_0_MASK	0xE020_0F00	R/W	External Interrupt EXT_INT[0] ~ EXT_INT[7] Mask Register	0x000000FF
EXT_INT_1_MASK	0xE020_0F04	R/W	External Interrupt EXT_INT[8] ~ EXT_INT[15] Mask Register	0x000000FF
EXT_INT_2_MASK	0xE020_0F08	R/W	External Interrupt EXT_INT[16] ~ EXT_INT[23] Mask Register	0x000000FF
EXT_INT_3_MASK	0xE020_0F0C	R/W	External Interrupt EXT_INT[24] ~ EXT_INT[31] Mask Register	0x000000FF
EXT_INT_0_PEND	0xE020_0F40	R/W	External Interrupt EXT_INT[0] ~ EXT_INT[7] Pending Register	0x0
EXT_INT_1_PEND	0xE020_0F44	R/W	External Interrupt EXT_INT[8] ~ EXT_INT[15] Pending Register	0x0
EXT_INT_2_PEND	0xE020_0F48	R/W	External Interrupt EXT_INT[16] ~ EXT_INT[23] Pending Register	0x0
EXT_INT_3_PEND	0xE020_0F4C	R/W	External Interrupt EXT_INT[24] ~ EXT_INT[31] Pending Register	0x0
PDNEN	0xE020_0F80	R/W	Power down mode Pad Configure Register	0

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2.2.2 PORT GROUP GPA0 CONTROL REGISTER

There are six control registers, namely, GPA0CON, GPA0DAT, GPA0PUD, GPA0DRV, GPA0CONPDN and GPA0PUDPDN in the Port Group GPA0 Control Registers.

2.2.2.1 Port Group GPA0 Control Register (GPA0CON, R/W, Address = 0xE020_0000)

GPA0CON	Bit	Description	Initial State
GPA0CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = UART_1_RTSn 0011 ~ 1110 = Reserved 1111 = GPA0_INT[7]	0000
GPA0CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = UART_1_CTSn 0011 ~ 1110 = Reserved 1111 = GPA0_INT[6]	0000
GPA0CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = UART_1_TXD 0011 ~ 1110 = Reserved 1111 = GPA0_INT[5]	0000
GPA0CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = UART_1_RXD 0011 ~ 1110 = Reserved 1111 = GPA0_INT[4]	0000
GPA0CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = UART_0_RTSn 0011 ~ 1110 = Reserved 1111 = GPA0_INT[3]	0000
GPA0CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = UART_0_CTSn 0011 ~ 1110 = Reserved 1111 = GPA0_INT[2]	0000
GPA0CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = UART_0_TXD 0011 ~ 1110 = Reserved 1111 = GPA0_INT[1]	0000
GPA0CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = UART_0_RXD 0011 ~ 1110 = Reserved 1111 = GPA0_INT[0]	0000

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2.2.2.2 Port Group GPA0 Control Register (GPA0DAT, R/W, Address = 0xE020_0004)

GPA0DAT	Bit	Description	Initial State
GPA0DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.2.3 Port Group GPA0 Control Register (GPA0PUD, R/W, Address = 0xE020_0008)

GPA0PUD	Bit	Description	Initial State
GPA0PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x5555

2.2.2.4 Port Group GPA0 Control Register (GPA0DRV, R/W, Address = 0xE020_000C)

GPA0DRV	Bit	Description	Initial State
GPA0DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.2.5 Port Group GPA0 Control Register (GPA0CONPDN, R/W, Address = 0xE020_0010)

GPA0CONPDN	Bit	Description	Initial State
GPA0[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.2.6 Port Group GPA0 Control Register (GPA0PUDPDN, R/W, Address = 0xE020_0014)

GPA0PUDPDN	Bit	Description	Initial State
GPA0[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.3 PORT GROUP GPA1 CONTROL REGISTER

There are six control registers, namely, GPA1CON, GPA1DAT, GPA1PUD, GPA1DRV, GPA1CONPDN and GPA1PUDPDN in the Port Group GPA1 Control Registers.

2.2.3.1 Port Group GPA1 Control Register (GPA1CON, R/W, Address = 0xE020_0020)

GPA1CON	Bit	Description	Initial State
GPA1CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = UART_3_TXD 0011 = UART_2_RTSn 0100 ~ 1110 = Reserved 1111 = GPA1_INT[3]	0000
GPA1CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = UART_3_RXD 0011 = UART_2_CTSn 0100 ~ 1110 = Reserved 1111 = GPA1_INT[2]	0000
GPA1CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = UART_2_TXD 0011 = Reserved 0100 = UART_AUDIO_TXD 0101 ~ 1110 = Reserved 1111 = GPA1_INT[1]	0000
GPA1CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = UART_2_RXD 0011 = Reserved 0100 = UART_AUDIO_RXD 0101 ~ 1110 = Reserved 1111 = GPA1_INT[0]	0000

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2.2.3.2 Port Group GPA1 Control Register (GPA1DAT, R/W, Address = 0xE020_0024)

GPA1DAT	Bit	Description	Initial State
GPA1DAT[3:0]	[3:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.3.3 Port Group GPA1 Control Register (GPA1PUD, R/W, Address = 0xE020_0028)

GPA1PUD	Bit	Description	Initial State
GPA1PUD[n]	[2n+1:2n] n=0~3	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0055

2.2.3.4 Port Group GPA1 Control Register (GPA1DRV, R/W, Address = 0xE020_002C)

GPA1DRV	Bit	Description	Initial State
GPA1DRV[n]	[2n+1:2n] n=0~3	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.3.5 Port Group GPA1 Control Register (GPA1CONPDN, R/W, Address = 0xE020_0030)

GPA1CONPDN	Bit	Description	Initial State
GPA1[n]	[2n+1:2n] n=0~3	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.3.6 Port Group GPA1 Control Register (GPA1PUDPDN, R/W, Address = 0xE020_0034)

GPA1PUDPDN	Bit	Description	Initial State
GPA1[n]	[2n+1:2n] n=0~3	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.4 PORT GROUP GPB CONTROL REGISTER

There are six control registers, namely, GPBCON, GPBDAT, GPBPUD, GPBDRV, GPBCONPDN and GPBPUDPDN in the Port Group GPB Control Registers.

2.2.4.1 Port Group GPB Control Register (GPBCON, R/W, Address = 0xE020_0040)

GPBCON	Bit	Description	Initial State
GPBCON[7]	[31:28]	0000 = Input 0001 = Output 0010 = SPI_1_MOSI 0011 ~ 1110 = Reserved 1111 = GPB_INT[7]	0000
GPBCON[6]	[27:24]	0000 = Input 0001 = Output 0010 = SPI_1_MISO 0011 ~ 1110 = Reserved 1111 = GPB_INT[6]	0000
GPBCON[5]	[23:20]	0000 = Input 0001 = Output 0010 = SPI_1_nSS 0011 ~ 1110 = Reserved 1111 = GPB_INT[5]	0000
GPBCON[4]	[19:16]	0000 = Input 0001 = Output 0010 = SPI_1_CLK 0011 ~ 1110 = Reserved 1111 = GPB_INT[4]	0000
GPBCON[3]	[15:12]	0000 = Input 0001 = Output 0010 = SPI_0_MOSI 0011 ~ 1110 = Reserved 1111 = GPB_INT[3]	0000
GPBCON[2]	[11:8]	0000 = Input 0001 = Output 0010 = SPI_0_MISO 0011 ~ 1110 = Reserved 1111 = GPB_INT[2]	0000
GPBCON[1]	[7:4]	0000 = Input 0001 = Output 0010 = SPI_0_nSS 0011 ~ 1110 = Reserved 1111 = GPB_INT[1]	0000
GPBCON[0]	[3:0]	0000 = Input 0001 = Output 0010 = SPI_0_CLK 0011 ~ 1110 = Reserved 1111 = GPB_INT[0]	0000

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2.2.4.2 Port Group GPB Control Register (GPBDAT, R/W, Address = 0xE020_0044)

GPBDAT	Bit	Description	Initial State
GPBDAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.4.3 Port Group GPB Control Register (GPBPUD, R/W, Address = 0xE020_0048)

GPBPUD	Bit	Description	Initial State
GPBPUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x5555

2.2.4.4 Port Group GPB Control Register (GPBDRV, R/W, Address = 0xE020_004C)

GPBDRV	Bit	Description	Initial State
GPBDRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.4.5 Port Group GPB Control Register (GPBCONPDN, R/W, Address = 0xE020_0050)

GPBCONPDN	Bit	Description	Initial State
GPB[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.4.6 Port Group GPB Control Register (GPBPUDPDN, R/W, Address = 0xE020_0054)

GPBPUDPDN	Bit	Description	Initial State
GPB[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.5 PORT GROUP GPC0 CONTROL REGISTER

There are six control registers, namely, GPC0CON, GPC0DAT, GPC0PUD, GPC0DRV, GPC0CONPDN and GPC0PUDPDN in the Port Group GPC0 Control Registers.

2.2.5.1 Port Group GPC0 Control Register (GPC0CON, R/W, Address = 0xE020_0060)

GPC0CON	Bit	Description	Initial State
GPC0CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = I2S_1_SDO 0011 = PCM_1_SOUT 0100 = AC97SDO 0101 ~ 1110 = Reserved 1111 = GPC0_INT[4]	0000
GPC0CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = I2S_1_SDI 0011 = PCM_1_SIN 0100 = AC97SDI 0101 ~ 1110 = Reserved 1111 = GPC0_INT[3]	0000
GPC0CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = I2S_1_LRCK 0011 = PCM_1_FSYNC 0100 = AC97SYNC 0101 ~ 1110 = Reserved 1111 = GPC0_INT[2]	0000
GPC0CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = I2S_1_CDCLK 0011 = PCM_1_EXTCLK 0100 = AC97RESETn 0101 ~ 1110 = Reserved 1111 = GPC0_INT[1]	0000
GPC0CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = I2S_1_SCLK 0011 = PCM_1_SCLK 0100 = AC97BITCLK 0101 ~ 1110 = Reserved 1111 = GPC0_INT[0]	0000

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2.2.5.2 Port Group GPC0 Control Register (GPC0DAT, R/W, Address = 0xE020_0064)

GPC0DAT	Bit	Description	Initial State
GPC0DAT[4:0]	[4:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.5.3 Port Group GPC0 Control Register (GPC0PUD, R/W, Address = 0xE020_0068)

GPC0PUD	Bit	Description	Initial State
GPC0PUD[n]	[2n+1:2n] n=0~4	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0155

2.2.5.4 Port Group GPC0 Control Register (GPC0DRV, R/W, Address = 0xE020_006C)

GPC0DRV	Bit	Description	Initial State
GPC0DRV[n]	[2n+1:2n] n=0~4	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.5.5 Port Group GPC0 Control Register (GPC0CONPDN, R/W, Address = 0xE020_0070)

GPC0CONPDN	Bit	Description	Initial State
GPC0[n]	[2n+1:2n] n=0~4	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.5.6 Port Group GPC0 Control Register (GPC0PUDPDN, R/W, Address = 0xE020_0074)

GPC0PUDPDN	Bit	Description	Initial State
GPC0[n]	[2n+1:2n] n=0~4	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.6 PORT GROUP GPC1 CONTROL REGISTER

There are six control registers, namely, GPC1CON, GPC1DAT, GPC1PUD, GPC1DRV, GPC1CONPDN and GPC1PUDPDN in the Port Group GPC1 Control Registers.

2.2.6.1 Port Group GPC1 Control Register (GPC1CON, R/W, Address = 0xE020_0080)

GPC1CON	Bit	Description	Initial State
GPC1CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = PCM_2_SOUT 0011 = Reserved 0100 = I2S_2_SDO 0101 ~ 1110 = Reserved 1111 = GPC1_INT[4]	0000
GPC1CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = PCM_2_SIN 0011 = Reserved 0100 = I2S_2_SDI 0101 ~ 1110 = Reserved 1111 = GPC1_INT[3]	0000
GPC1CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = PCM_2_FSYNC 0011 = LCD_FRM 0100 = I2S_2_LRCK 0101 ~ 1110 = Reserved 1111 = GPC1_INT[2]	0000
GPC1CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = PCM_2_EXTCLK 0011 = SPDIF_EXTCLK 0100 = I2S_2_CDCLK 0101 ~ 1110 = Reserved 1111 = GPC1_INT[1]	0000
GPC1CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = PCM_2_SCLK 0011 = SPDIF_0_OUT 0100 = I2S_2_SCLK 0101 ~ 1110 = Reserved 1111 = GPC1_INT[0]	0000

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2.2.6.2 Port Group GPC1 Control Register (GPC1DAT, R/W, Address = 0xE020_0084)

GPC1DAT	Bit	Description	Initial State
GPC1DAT[4:0]	[4:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.6.3 Port Group GPC1 Control Register (GPC1PUD, R/W, Address = 0xE020_0088)

GPC1PUD	Bit	Description	Initial State
GPC1PUD[n]	[2n+1:2n] n=0~4	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0155

2.2.6.4 Port Group GPC1 Control Register (GPC1DRV, R/W, Address = 0xE020_008C)

GPC1DRV	Bit	Description	Initial State
GPC1DRV[n]	[2n+1:2n] n=0~4	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.6.5 Port Group GPC1 Control Register (GPC1CONPDN, R/W, Address = 0xE020_0090)

GPC1CONPDN	Bit	Description	Initial State
GPC1[n]	[2n+1:2n] n=0~4	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.6.6 Port Group GPC1 Control Register (GPC1PUDPDN, R/W, Address = 0xE020_0094)

GPC1PUDPDN	Bit	Description	Initial State
GPC1[n]	[2n+1:2n] n=0~4	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.7 PORT GROUP GPD0 CONTROL REGISTER

There are six control registers, namely, GPD0CON, GPD0DAT, GPD0PUD, GPD0DRV, GPD0CONPDN and GPD0PUDPDN in the Port Group GPD0 Control Registers.

2.2.7.1 Port Group GPD0 Control Register (GPD0CON, R/W, Address = 0xE020_00A0)

GPD0CON	Bit	Description	Initial State
GPD0CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = TOUT_3 0011 ~ 1110 = Reserved 1111 = GPD0_INT[3]	0000
GPD0CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = TOUT_2 0011 ~ 1110 = Reserved 1111 = GPD0_INT[2]	0000
GPD0CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = TOUT_1 0011 ~ 1110 = Reserved 1111 = GPD0_INT[1]	0000
GPD0CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = TOUT_0 0011 ~ 1110 = Reserved 1111 = GPD0_INT[0]	0000

2.2.7.2 Port Group GPD0 Control Register (GPD0DAT, R/W, Address = 0xE020_00A4)

GPD0DAT	Bit	Description	Initial State
GPD0DAT[3:0]	[3:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.7.3 Port Group GPD0 Control Register (GPD0PUD, R/W, Address = 0xE020_00A8)

GPD0PUD	Bit	Description	Initial State
GPD0PUD[n]	[2n+1:2n] n=0~3	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0055

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2.2.7.4 Port Group GPD0 Control Register (GPD0DRV, R/W, Address = 0xE020_00AC)

GPD0DRV	Bit	Description	Initial State
GPD0DRV[n]	[2n+1:2n] n=0~3	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.7.5 Port Group GPD0 Control Register (GPD0CONPDN, R/W, Address = 0xE020_00B0)

GPD0CONPDN	Bit	Description	Initial State
GPD0[n]	[2n+1:2n] n=0~3	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.7.6 Port Group GPD0 Control Register (GPD0PUDPDN, R/W, Address = 0xE020_00B4)

GPD0PUDPDN	Bit	Description	Initial State
GPD0[n]	[2n+1:2n] n=0~3	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.8 PORT GROUP GPD1 CONTROL REGISTER

There are six control registers, namely, GPD1CON, GPD1DAT, GPD1PUD, GPD1DRV, GPD1CONPDN and GPD1PUDPDN in the Port Group GPD1 Control Registers.

2.2.8.1 Port Group GPD1 Control Register (GPD1CON, R/W, Address = 0xE020_00C0)

GPD1CON	Bit	Description	Initial State
GPD1CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = I2C2_SCL 0011 = IEM_SPWI 0100 ~ 1110 = Reserved 1111 = GPD1_INT[5]	0000
GPD1CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = I2C2_SDA 0011 = IEM_SCLK 0100 ~ 1110 = Reserved 1111 = GPD1_INT[4]	0000
GPD1CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = I2C1_SCL 0011 ~ 1110 = Reserved 1111 = GPD1_INT[3]	0000
GPD1CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = I2C1_SDA 0011 ~ 1110 = Reserved 1111 = GPD1_INT[2]	0000
GPD1CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = I2C0_SCL 0011 ~ 1110 = Reserved 1111 = GPD1_INT[1]	0000
GPD1CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = I2C0_SDA 0011 ~ 1110 = Reserved 1111 = GPD1_INT[0]	0000

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2.2.8.2 Port Group GPD1 Control Register (GPD1DAT, R/W, Address = 0xE020_00C4)

GPD1DAT	Bit	Description	Initial State
GPD1DAT[5:0]	[5:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.8.3 Port Group GPD1 Control Register (GPD1PUD, R/W, Address = 0xE020_00C8)

GPD1PUD	Bit	Description	Initial State
GPD1PUD[n]	[2n+1:2n] n=0~5	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0555

2.2.8.4 Port Group GPD1 Control Register (GPD1DRV, R/W, Address = 0xE020_00CC)

GPD1DRV	Bit	Description	Initial State
GPD1DRV[n]	[2n+1:2n] n=0~5	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.8.5 Port Group GPD1 Control Register (GPD1CONPDN, R/W, Address = 0xE020_00D0)

GPD1CONPDN	Bit	Description	Initial State
GPD1[n]	[2n+1:2n] n=0~5	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.8.6 Port Group GPD1 Control Register (GPD1PUDPDN, R/W, Address = 0xE020_00D4)

GPD1PUDPDN	Bit	Description	Initial State
GPD1[n]	[2n+1:2n] n=0~5	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.9 PORT GROUP GPE0 CONTROL REGISTER

There are six control registers, namely, GPE0CON, GPE0DAT, GPE0PUD, GPE0DRV, GPE0CONPDN and GPE0PUDPDN in the Port Group GPE0 Control Registers.

2.2.9.1 Port Group GPE0 Control Register (GPE0CON, R/W, Address = 0xE020_00E0)

GPE0CON	Bit	Description	Initial State
GPE0CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = CAM_A_DATA[4] 0011 ~ 1110 = Reserved 1111 = GPE0_INT[7]	0000
GPE0CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = CAM_A_DATA[3] 0011 ~ 1110 = Reserved 1111 = GPE0_INT[6]	0000
GPE0CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = CAM_A_DATA[2] 0011 ~ 1110 = Reserved 1111 = GPE0_INT[5]	0000
GPE0CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = CAM_A_DATA[1] 0011 ~ 1110 = Reserved 1111 = GPE0_INT[4]	0000
GPE0CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = CAM_A_DATA[0] 0011 ~ 1110 = Reserved 1111 = GPE0_INT[3]	0000
GPE0CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = CAM_A_HREF 0011 ~ 1110 = Reserved 1111 = GPE0_INT[2]	0000
GPE0CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = CAM_A_VSYNC 0011 ~ 1110 = Reserved 1111 = GPE0_INT[1]	0000
GPE0CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = CAM_A_PCLK 0011 ~ 1110 = Reserved 1111 = GPE0_INT[0]	0000

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2.2.9.2 Port Group GPE0 Control Register (GPE0DAT, R/W, Address = 0xE020_00E4)

GPE0DAT	Bit	Description	Initial State
GPE0DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.9.3 Port Group GPE0 Control Register (GPE0PUD, R/W, Address = 0xE020_00E8)

GPE0PUD	Bit	Description	Initial State
GPE0PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x5555

2.2.9.4 Port Group GPE0 Control Register (GPE0DRV, S/W, Address = 0xE020_00EC)

GPE0DRV	Bit	Description	Initial State
GPE0DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.9.5 Port Group GPE0 Control Register (GPE0CONPDN, S/W, Address = 0xE020_00F0)

GPE0CONPDN	Bit	Description	Initial State
GPE0[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.9.6 Port Group GPE0 Control Register (GPE0PUDPDN, S/W, Address = 0xE020_00F4)

GPE0PUDPDN	Bit	Description	Initial State
GPE0[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.10 PORT GROUP GPE1 CONTROL REGISTER

There are six control registers, namely, GPE1CON, GPE1DAT, GPE1PUD, GPE1DRV, GPE1CONPDN and GPE1PUDPDN in the Port Group GPE1 Control Registers.

2.2.10.1 Port Group GPE1 Control Register (GPE1CON, R/W, Address = 0xE020_0100)

GPE1CON	Bit	Description	Initial State
GPE1CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = CAM_A_FIELD 0011 ~ 1110 = Reserved 1111 = GPE1_INT[4]	0000
GPE1CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = CAM_A_CLKOUT 0011 ~ 1110 = Reserved 1111 = GPE1_INT[3]	0000
GPE1CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = CAM_A_DATA[7] 0011 ~ 1110 = Reserved 1111 = GPE1_INT[2]	0000
GPE1CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = CAM_A_DATA[6] 0011 ~ 1110 = Reserved 1111 = GPE1_INT[1]	0000
GPE1CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = CAM_A_DATA[5] 0011 ~ 1110 = Reserved 1111 = GPE1_INT[0]	0000

2.2.10.2 Port Group GPE1 Control Register (GPE1DAT, R/W, Address = 0xE020_0104)

GPE1DAT	Bit	Description	Initial State
GPE1DAT[4:0]	[4:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

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2.2.10.3 Port Group GPE1 Control Register (GPE1PUD, R/W, Address = 0xE020_0108)

GPE1PUD	Bit	Description	Initial State
GPE1PUD[n]	[2n+1:2n] n=0~4	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0155

2.2.10.4 Port Group GPE1 Control Register (GPE1DRV, R/W, Address = 0xE020_010C)

GPE1DRV	Bit	Description	Initial State
GPE1DRV[n]	[2n+1:2n] n=0~4	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.10.5 Port Group GPE1 Control Register (GPE1CONPDN, R/W, Address = 0xE020_0110)

GPE1CONPDN	Bit	Description	Initial State
GPE1[n]	[2n+1:2n] n=0~4	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.10.6 Port Group GPE1 Control Register (GPE1PUDPDN, R/W, Address = 0xE020_0114)

GPE1PUDPDN	Bit	Description	Initial State
GPE1[n]	[2n+1:2n] n=0~4	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.11 PORT GROUP GPF0 CONTROL REGISTER

There are six control registers, namely, GPF0CON, GPF0DAT, GPF0PUD, GPF0DRV, GPF0CONPDN and GPF0PUDPDN in the Port Group GPF0 Control Registers.

2.2.11.1 Port Group GPF0 Control Register (GPF0CON, R/W, Address = 0xE020_0120)

GPF0CON	Bit	Description	Initial State
GPF0CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = LCD_VD[3] 0011 = SYS_VD[3] 0100 = VEN_DATA[3] 0101 ~ 1110 = Reserved 1111 = GPF0_INT[7]	0000
GPF0CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = LCD_VD[2] 0011 = SYS_VD[2] 0100 = VEN_DATA[2] 0101 ~ 1110 = Reserved 1111 = GPF0_INT[6]	0000
GPF0CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = LCD_VD[1] 0011 = SYS_VD[1] 0100 = VEN_DATA[1] 0101 ~ 1110 = Reserved 1111 = GPF0_INT[5]	0000
GPF0CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = LCD_VD[0] 0011 = SYS_VD[0] 0100 = VEN_DATA[0] 0101 ~ 1110 = Reserved 1111 = GPF0_INT[4]	0000
GPF0CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = LCD_VCLK 0011 = SYS_WE 0100 = V601_CLK 0101 ~ 1110 = Reserved 1111 = GPF0_INT[3]	0000
GPF0CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = LCD_VDEN 0011 = SYS_RS 0100 = VEN_HREF 0101 ~ 1110 = Reserved 1111 = GPF0_INT[2]	0000
GPF0CON[1]	[7:4]	0000 = Input	0000

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GPF0CON	Bit	Description	Initial State
		0001 = Output 0010 = LCD_VSYNC 0011 = SYS_CS1 0100 = VEN_VSYNC 0101 ~ 1110 = Reserved 1111 = GPF0_INT[1]	
GPF0CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = LCD_HSYNC 0011 = SYS_CS0 0100 = VEN_HSYNC 0101 ~ 1110 = Reserved 1111 = GPF0_INT[0]	0000

2.2.11.2 Port Group GPF0 Control Register (GPF0DAT, R/W, Address = 0xE020_0124)

GPF0DAT	Bit	Description	Initial State
GPF0DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.11.3 Port Group GPF0 Control Register (GPF0PUD, R/W, Address = 0xE020_0128)

GPF0PUD	Bit	Description	Initial State
GPF0PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x5555

2.2.11.4 Port Group GPF0 Control Register (GPF0DRV, R/W, Address = 0xE020_012C)

GPF0DRV	Bit	Description	Initial State
GPF0DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

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2.2.11.5 Port Group GPF0 Control Register (GPF0CONPDN, R/W, Address = 0xE020_0130)

GPF0CONPDN	Bit	Description	Initial State
GPF0[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.11.6 Port Group GPF0 Control Register (GPF0PUDPDN, R/W, Address = 0xE020_0134)

GPF0PUDPDN	Bit	Description	Initial State
GPF0[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.12 PORT GROUP GPF1 CONTROL REGISTER

There are six control registers, namely, GPF1CON, GPF1DAT, GPF1PUD, GPF1DRV, GPF1CONPDN and GPF1PUDPDN in the Port Group GPF1 Control Registers.

2.2.12.1 Port Group GPF1 Control Register (GPF1CON, S/W, Address = 0xE020_0140)

GPF1CON	Bit	Description	Initial State
GPF1CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = LCD_VD[11] 0011 = SYS_VD[11] 0100 = V656_DATA[3] 0101 ~ 1110 = Reserved 1111 = GPF1_INT[7]	0000
GPF1CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = LCD_VD[10] 0011 = SYS_VD[10] 0100 = V656_DATA[2] 0101 ~ 1110 = Reserved 1111 = GPF1_INT[6]	0000
GPF1CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = LCD_VD[9] 0011 = SYS_VD[9] 0100 = V656_DATA[1] 0101 ~ 1110 = Reserved 1111 = GPF1_INT[5]	0000
GPF1CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = LCD_VD[8] 0011 = SYS_VD[8] 0100 = V656_DATA[0] 0101 ~ 1110 = Reserved 1111 = GPF1_INT[4]	0000
GPF1CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = LCD_VD[7] 0011 = SYS_VD[7] 0100 = VEN_DATA[7] 0101 ~ 1110 = Reserved 1111 = GPF1_INT[3]	0000
GPF1CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = LCD_VD[6] 0011 = SYS_VD[6] 0100 = VEN_DATA[6] 0101 ~ 1110 = Reserved 1111 = GPF1_INT[2]	0000
GPF1CON[1]	[7:4]	0000 = Input	0000

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GPF1CON	Bit	Description	Initial State
		0001 = Output 0010 = LCD_VD[5] 0011 = SYS_VD[5] 0100 = VEN_DATA[5] 0101 ~ 1110 = Reserved 1111 = GPF1_INT[1]	
GPF1CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = LCD_VD[4] 0011 = SYS_VD[4] 0100 = VEN_DATA[4] 0101 ~ 1110 = Reserved 1111 = GPF1_INT[0]	0000

2.2.12.2 Port Group GPF1 Control Register (GPF1DAT, S/W, Address = 0xE020_0144)

GPF1DAT	Bit	Description	Initial State
GPF1DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.12.3 Port Group GPF1 Control Register (GPF1PUD, S/W, Address = 0xE020_0148)

GPF1PUD	Bit	Description	Initial State
GPF1PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x5555

2.2.12.4 Port Group GPF1 Control Register (GPF1DRV, S/W, Address = 0xE020_014C)

GPF1DRV	Bit	Description	Initial State
GPF1DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

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2.2.12.5 Port Group GPF1 Control Register (GPF1CONPDN, S/W, Address = 0xE020_0150)

GPF1CONPDN	Bit	Description	Initial State
GPF1[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.12.6 Port Group GPF1 Control Register (GPF1PUDPDN, S/W, Address = 0xE020_0154)

GPF1PUDPDN	Bit	Description	Initial State
GPF1[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.13 PORT GROUP GPF2 CONTROL REGISTER

There are six control registers, namely, GPF2CON, GPF2DAT, GPF2PUD, GPF2DRV, GPF2CONPDN and GPF2PUDPDN in the Port Group GPF2 Control Registers.

2.2.13.1 Port Group GPF2 Control Register (GPF2CON, R/W, Address = 0xE020_0160)

GPF2CON	Bit	Description	Initial State
GPF2CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = LCD_VD[19] 0011 = SYS_VD[19] 0100 ~ 1110 = Reserved 1111 = GPF2_INT[7]	0000
GPF2CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = LCD_VD[18] 0011 = SYS_VD[18] 0100 ~ 1110 = Reserved 1111 = GPF2_INT[6]	0000
GPF2CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = LCD_VD[17] 0011 = SYS_VD[17] 0100 ~ 1110 = Reserved 1111 = GPF2_INT[5]	0000
GPF2CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = LCD_VD[16] 0011 = SYS_VD[16] 0100 ~ 1110 = Reserved 1111 = GPF2_INT[4]	0000
GPF2CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = LCD_VD[15] 0011 = SYS_VD[15] 0100 = V656_DATA[7] 0101 ~ 1110 = Reserved 1111 = GPF2_INT[3]	0000
GPF2CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = LCD_VD[14] 0011 = SYS_VD[14] 0100 = V656_DATA[6] 0101 ~ 1110 = Reserved 1111 = GPF2_INT[2]	0000

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GPF2CON	Bit	Description	Initial State
GPF2CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = LCD_VD[13] 0011 = SYS_VD[13] 0100 = V656_DATA[5] 0101 ~ 1110 = Reserved 1111 = GPF2_INT[1]	0000
GPF2CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = LCD_VD[12] 0011 = SYS_VD[12] 0100 = V656_DATA[4] 0101 ~ 1110 = Reserved 1111 = GPF2_INT[0]	0000

2.2.13.2 Port Group GPF2 Control Register (GPF2DAT, R/W, Address = 0xE020_0164)

GPF2DAT	Bit	Description	Initial State
GPF2DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.13.3 Port Group GPF2 Control Register (GPF2PUD, R/W, Address = 0xE020_0168)

GPF2PUD	Bit	Description	Initial State
GPF2PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x5555

2.2.13.4 Port Group GPF2 Control Register (GPF2DRV, S/W, Address = 0xE020_016C)

GPF2DRV	Bit	Description	Initial State
GPF2DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

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2.2.13.5 Port Group GPF2 Control Register (GPF2CONPDN, S/W, Address = 0xE020_0170)

GPF2CONPDN	Bit	Description	Initial State
GPF2[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.13.6 Port Group GPF2 Control Register (GPF2PUDPDN, S/W, Address = 0xE020_0174)

GPF2PUDPDN	Bit	Description	Initial State
GPF2[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.14 PORT GROUP GPF3 CONTROL REGISTER

There are six control registers, namely, GPF3CON, GPF3DAT, GPF3PUD, GPF3DRV, GPF3CONPDN and GPF3PUDPDN in the Port Group GPF3 Control Registers.

2.2.14.1 Port Group GPF3 Control Register (GPF3CON, R/W, Address = 0xE020_0180)

GPF3CON	Bit	Description	Initial State
GPF3CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = Reserved 0011 = SYS_OE 0100 = VEN_FIELD 0101 ~ 1110 = Reserved 1111 = GPF3_INT[5]	0000
GPF3CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = Reserved 0011 = VSYNC_LDI 0100 ~ 1110 = Reserved 1111 = GPF3_INT[4]	0000
GPF3CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = LCD_VD[23] 0011 = SYS_VD[23] 0100 = V656_CLK 0101 ~ 1110 = Reserved 1111 = GPF3_INT[3]	0000
GPF3CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = LCD_VD[22] 0011 = SYS_VD[22] 0100 ~ 1110 = Reserved 1111 = GPF3_INT[2]	0000
GPF3CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = LCD_VD[21] 0011 = SYS_VD[21] 0100 ~ 1110 = Reserved 1111 = GPF3_INT[1]	0000
GPF3CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = LCD_VD[20] 0011 = SYS_VD[20] 0100 ~ 1110 = Reserved 1111 = GPF3_INT[0]	0000

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2.2.14.2 Port Group GPF3 Control Register (GPF3DAT, R/W, Address = 0xE020_0184)

GPF3DAT	Bit	Description	Initial State
GPF3DAT[5:0]	[5:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.14.3 Port Group GPF3 Control Register (GPF3PUD, R/W, Address = 0xE020_0188)

GPF3PUD	Bit	Description	Initial State
GPF3PUD[n]	[2n+1:2n] n=0~5	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0555

2.2.14.4 Port Group GPF3 Control Register (GPF3DRV, R/W, Address = 0xE020_018C)

GPF3DRV	Bit	Description	Initial State
GPF3DRV[n]	[2n+1:2n] n=0~5	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.14.5 Port Group GPF3 Control Register (GPF3CONPDN, R/W, Address = 0xE020_0190)

GPF3CONPDN	Bit	Description	Initial State
GPF3[n]	[2n+1:2n] n=0~5	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.14.6 Port Group GPF3 Control Register (GPF3PUDPDN, R/W, Address = 0xE020_0194)

GPF3PUDPDN	Bit	Description	Initial State
GPF3[n]	[2n+1:2n] n=0~5	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.15 PORT GROUP GPG0 CONTROL REGISTER

There are six control registers, namely, GPG0CON, GPG0DAT, GPG0PUD, GPG0DRV, GPG0CONPDN and GPG0PUDPDN in the Port Group GPG0 Control Registers.

2.2.15.1 Port Group GPG0 Control Register (GPG0CON, R/W, Address = 0xE020_01A0)

GPG0CON	Bit	Description	Initial State
GPG0CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = SD_0_DATA[3] 0011 ~ 1110 = Reserved 1111 = GPG0_INT[6]	0000
GPG0CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = SD_0_DATA[2] 0011 ~ 1110 = Reserved 1111 = GPG0_INT[5]	0000
GPG0CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = SD_0_DATA[1] 0011 ~ 1110 = Reserved 1111 = GPG0_INT[4]	0000
GPG0CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = SD_0_DATA[0] 0011 ~ 1110 = Reserved 1111 = GPG0_INT[3]	0000
GPG0CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = SD_0_CDn 0011 ~ 1110 = Reserved 1111 = GPG0_INT[2]	0000
GPG0CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = SD_0_CMD 0011 ~ 1110 = Reserved 1111 = GPG0_INT[1]	0000
GPG0CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = SD_0_CLK 0011 ~ 1110 = Reserved 1111 = GPG0_INT[0]	0000

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2.2.15.2 Port Group GPG0 Control Register (GPG0DAT, R/W, Address = 0xE020_01A4)

GPG0DAT	Bit	Description	Initial State
GPG0DAT[6:0]	[6:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.15.3 Port Group GPG0 Control Register (GPG0PUD, R/W, Address = 0xE020_01A8)

GPG0PUD	Bit	Description	Initial State
GPG0PUD[n]	[2n+1:2n] n=0~6	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x1555

2.2.15.4 Port Group GPG0 Control Register (GPG0DRV, R/W, Address = 0xE020_01AC)

GPG0DRV	Bit	Description	Initial State
GPG0DRV[n]	[2n+1:2n] n=0~6	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x2AAA

2.2.15.5 Port Group GPG0 Control Register (GPG0CONPDN, R/W, Address = 0xE020_01B0)

GPG0CONPDN	Bit	Description	Initial State
GPG0[n]	[2n+1:2n] n=0~6	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.15.6 Port Group GPG0 Control Register (GPG0PUDPDN, R/W, Address = 0xE020_01B4)

GPG0PUDPDN	Bit	Description	Initial State
GPG0[n]	[2n+1:2n] n=0~6	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.16 PORT GROUP GPG1 CONTROL REGISTER

There are six control registers, namely, GPG1CON, GPG1DAT, GPG1PUD, GPG1DRV, GPG1CONPDN and GPG1PUDPDN in the Port Group GPG1 Control Registers.

2.2.16.1 Port Group GPG1 Control Register (GPG1CON, R/W, Address = 0xE020_01C0)

GPG1CON	Bit	Description	Initial State
GPG1CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = SD_1_DATA[3] 0011 = SD_0_DATA[7] 0100 ~ 1110 = Reserved 1111 = GPG1_INT[6]	0000
GPG1CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = SD_1_DATA[2] 0011 = SD_0_DATA[6] 0100 ~ 1110 = Reserved 1111 = GPG1_INT[5]	0000
GPG1CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = SD_1_DATA[1] 0011 = SD_0_DATA[5] 0100 ~ 1110 = Reserved 1111 = GPG1_INT[4]	0000
GPG1CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = SD_1_DATA[0] 0011 = SD_0_DATA[4] 0100 ~ 1110 = Reserved 1111 = GPG1_INT[3]	0000
GPG1CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = SD_1_CDn 0011 ~ 1110 = Reserved 1111 = GPG1_INT[2]	0000
GPG1CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = SD_1_CMD 0011 ~ 1110 = Reserved 1111 = GPG1_INT[1]	0000
GPG1CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = SD_1_CLK 0011 ~ 1110 = Reserved 1111 = GPG1_INT[0]	0000

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2.2.16.2 Port Group GPG1 Control Register (GPG1DAT, R/W, Address = 0xE020_01C4)

GPG1DAT	Bit	Description	Initial State
GPG1DAT[6:0]	[6:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.16.3 Port Group GPG1 Control Register (GPG1PUD, R/W, Address = 0xE020_01C8)

GPG1PUD	Bit	Description	Initial State
GPG1PUD[n]	[2n+1:2n] n=0~6	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x1555

2.2.16.4 Port Group GPG1 Control Register (GPG1DRV, R/W, Address = 0xE020_01CC)

GPG1DRV	Bit	Description	Initial State
GPG1DRV[n]	[2n+1:2n] n=0~6	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.16.5 Port Group GPG1 Control Register (GPG1CONPDN, R/W, Address = 0xE020_01D0)

GPG1CONPDN	Bit	Description	Initial State
GPG1[n]	[2n+1:2n] n=0~6	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.16.6 Port Group GPG1 Control Register (GPG1PUDPDN, R/W, Address = 0xE020_01D4)

GPG1PUDPDN	Bit	Description	Initial State
GPG1[n]	[2n+1:2n] n=0~6	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.17 PORT GROUP GPG2 CONTROL REGISTER

There are six control registers, namely, GPG2CON, GPG2DAT, GPG2PUD, GPG2DRV, GPG2CONPDN and GPG2PUDPDN in the Port Group GPG2 Control Registers.

2.2.17.1 Port Group GPG2 Control Register (GPG2CON, R/W, Address = 0xE020_01E0)

GPG2CON	Bit	Description	Initial State
GPG2CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = SD_2_DATA[3] 0011 ~ 1110 = Reserved 1111 = GPG2_INT[6]	0000
GPG2CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = SD_2_DATA[2] 0011 ~ 1110 = Reserved 1111 = GPG2_INT[5]	0000
GPG2CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = SD_2_DATA[1] 0011 ~ 1110 = Reserved 1111 = GPG2_INT[4]	0000
GPG2CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = SD_2_DATA[0] 0011 ~ 1110 = Reserved 1111 = GPG2_INT[3]	0000
GPG2CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = SD_2_CDn 0011 ~ 1110 = Reserved 1111 = GPG2_INT[2]	0000
GPG2CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = SD_2_CMD 0011 ~ 1110 = Reserved 1111 = GPG2_INT[1]	0000
GPG2CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = SD_2_CLK 0011 ~ 1110 = Reserved 1111 = GPG2_INT[0]	0000

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2.2.17.2 Port Group GPG2 Control Register (GPG2DAT, R/W, Address = 0xE020_01E4)

GPG2DAT	Bit	Description	Initial State
GPG2DAT[6:0]	[6:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.17.3 Port Group GPG2 Control Register (GPG2PUD, R/W, Address = 0xE020_01E8)

GPG2PUD	Bit	Description	Initial State
GPG2PUD[n]	[2n+1:2n] n=0~6	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x1555

2.2.17.4 Port Group GPG2 Control Register (GPG2DRV, R/W, Address = 0xE020_01EC)

GPG2DRV	Bit	Description	Initial State
GPG2DRV[n]	[2n+1:2n] n=0~6	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.17.5 Port Group GPG2 Control Register (GPG2CONPDN, R/W, Address = 0xE020_01F0)

GPG2CONPDN	Bit	Description	Initial State
GPG2[n]	[2n+1:2n] n=0~6	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.17.6 Port Group GPG2 Control Register (GPG2PUDPDN, R/W, Address = 0xE020_01F4)

GPG2PUDPDN	Bit	Description	Initial State
GPG2[n]	[2n+1:2n] n=0~6	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.18 PORT GROUP GPG3 CONTROL REGISTER

There are six control registers, namely, GPG3CON, GPG3DAT, GPG3PUD, GPG3DRV, GPG3CONPDN and GPG3PUDPDN in the Port Group GPG3 Control Registers.

2.2.18.1 Port Group GPG3 Control Register (GPG3CON, R/W, Address = 0xE020_0200)

GPG3CON	Bit	Description	Initial State
GPG3CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = SD_3_DATA[3] 0011 = SD_2_DATA[7] 0100 ~ 1110 = Reserved 1111 = GPG3_INT[6]	0000
GPG3CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = SD_3_DATA[2] 0011 = SD_2_DATA[6] 0100 ~ 1110 = Reserved 1111 = GPG3_INT[5]	0000
GPG3CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = SD_3_DATA[1] 0011 = SD_2_DATA[5] 0100 ~ 1110 = Reserved 1111 = GPG3_INT[4]	0000
GPG3CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = SD_3_DATA[0] 0011 = SD_2_DATA[4] 0100 ~ 1110 = Reserved 1111 = GPG3_INT[3]	0000
GPG3CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = SD_3_CDn 0011 ~ 1110 = Reserved 1111 = GPG3_INT[2]	0000
GPG3CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = SD_3_CMD 0011 ~ 1110 = Reserved 1111 = GPG3_INT[1]	0000
GPG3CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = SD_3_CLK 0011 ~ 1110 = Reserved 1111 = GPG3_INT[0]	0000

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2.2.18.2 Port Group GPG3 Control Register (GPG3DAT, R/W, Address = 0xE020_0204)

GPG3DAT	Bit	Description	Initial State
GPG3DAT[6:0]	[6:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.18.3 Port Group GPG3 Control Register (GPG3PUD, R/W, Address = 0xE020_0208)

GPG3PUD	Bit	Description	Initial State
GPG3PUD[n]	[2n+1:2n] n=0~6	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x1555

2.2.18.4 Port Group GPG3 Control Register (GPG3DRV, R/W, Address = 0xE020_020C)

GPG3DRV	Bit	Description	Initial State
GPG3DRV[n]	[2n+1:2n] n=0~6	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.18.5 Port Group GPG3 Control Register (GPG3CONPDN, R/W, Address = 0xE020_0210)

GPG3CONPDN	Bit	Description	Initial State
GPG3[n]	[2n+1:2n] n=0~6	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.18.6 Port Group GPG3 Control Register (GPG3PUDPDN, R/W, Address = 0xE020_0214)

GPG3PUDPDN	Bit	Description	Initial State
GPG3[n]	[2n+1:2n] n=0~6	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.19 PORT GROUP GPI CONTROL REGISTER

There are four control registers, namely, GPICON, GPIPUD and GPIDRV in the Port Group GPI Control Registers.

This port group is used to only functional port (I2S_0 and PCM_0), not GPIO and EXT_INT.

2.2.19.1 Port Group GPI Control Register (GPICON, R/W, Address = 0xE020_0220)

GPICON	Bit	Description	Initial State
GPICON[6]	[27:24]	0010 = I2S_0_SDO[2]	0010
GPICON[5]	[23:20]	0010 = I2S_0_SDO[1]	0010
GPICON[4]	[19:16]	0010 = I2S_0_SDO[0] 0011 = PCM_0_SOUT	0010
GPICON[3]	[15:12]	0010 = I2S_0_SDI 0011 = PCM_0_SIN	0010
GPICON[2]	[11:8]	0010 = I2S_0_LRCK 0011 = PCM_0_FSYNC	0010
GPICON[1]	[7:4]	0010 = I2S_0_CDCLK 0011 = PCM_0_EXTCLK	0010
GPICON[0]	[3:0]	0010 = I2S_0_SCLK 0011 = PCM_0_SCLK	0010

2.2.19.2 Port Group GPI Control Register (GPIDAT, R/W, Address = 0xE020_0224)

GPIDAT	Bit	Description	Initial State
GPIDAT[6:0]	[31:0]	Reserved	0x00

2.2.19.3 Port Group GPI Control Register (GPIPUD, R/W, Address = 0xE020_0228)

GPIPUD	Bit	Description	Initial State
GPIPUD[n]	[2n+1:2n] n=0~6	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x1555

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2.2.19.4 Port Group GPI Control Register (GPIDRV, R/W, Address = 0xE020_022C)

GPIDRV	Bit	Description	Initial State
GPIDRV[n]	[2n+1:2n] n=0~6	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.19.5 Port Group GPI Control Register (GPICONPDN, R/W, Address = 0xE020_0230)

GPICONPDN	Bit	Description	Initial State
GPI[n]	[2n+1:2n] n=0~6	Reserved (Controlled by PAD_CON_CTRL register at AUDIO_SS)	0x00

2.2.19.6 Port Group GPI Control Register (GPIPUDPDN, R/W, Address = 0xE020_0234)

GPIPUDPDN	Bit	Description	Initial State
GPI[n]	[2n+1:2n] n=0~6	Reserved (Controlled by GPIPUD register)	0x00

For GPI PDN control in power down mode, PAD_PDN_CTRL Register of GPI is at AUDIO_SS.
For more information, refer to Chapter 10.01, Low Power Audio Subsystem.

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2.2.20 PORT GROUP GPJ0 CONTROL REGISTER

There are six control registers, namely, GPJ0CON, GPJ0DAT, GPJ0PUD, GPJ0DRV, GPJ0CONPDN and GPJ0PUDPDN in the Port Group GPJ0 Control Registers.

2.2.20.1 Port Group GPJ0 Control Register (GPJ0CON, R/W, Address = 0xE020_0240)

GPJ0CON	Bit	Description	Initial State
GPJ0CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = MSM_ADDR[7] 0011 = CAM_B_DATA[7] 0100 = CF_DMACKNs 0101 = MHL_D0 0110 ~ 1110 = Reserved 1111 = GPJ0_INT[7]	0000
GPJ0CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = MSM_ADDR[6] 0011 = CAM_B_DATA[6] 0100 = CF_DRESETN 0101 = TS_ERROR 0110 ~ 1110 = Reserved 1111 = GPJ0_INT[6]	0000
GPJ0CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = MSM_ADDR[5] 0011 = CAM_B_DATA[5] 0100 = CF_DMARQ 0101 = TS_DATA 0110 ~ 1110 = Reserved 1111 = GPJ0_INT[5]	0000
GPJ0CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = MSM_ADDR[4] 0011 = CAM_B_DATA[4] 0100 = CF_INTRQ 0101 = TS_VAL 0110 ~ 1110 = Reserved 1111 = GPJ0_INT[4]	0000
GPJ0CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = MSM_ADDR[3] 0011 = CAM_B_DATA[3] 0100 = CF_IORDY 0101 = TS_SYNC 0110 ~ 1110 = Reserved 1111 = GPJ0_INT[3]	0000
GPJ0CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = MSM_ADDR[2]	0000

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GPJ0CON	Bit	Description	Initial State
		0011 = CAM_B_DATA[2] 0100 = CF_ADDR[2] 0101 = TS_CLK 0110 ~ 1110 = Reserved 1111 = GPJ0_INT[2]	
GPJ0CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = MSM_ADDR[1] 0011 = CAM_B_DATA[1] 0100 = CF_ADDR[1] 0101 = MIPI_ESC_CLK 0110 ~ 1110 = Reserved 1111 = GPJ0_INT[1]	0000
GPJ0CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = MSM_ADDR[0] 0011 = CAM_B_DATA[0] 0100 = CF_ADDR[0] 0101 = MIPI_BYTE_CLK 0110 ~ 1110 = Reserved 1111 = GPJ0_INT[0]	0000

2.2.20.2 Port Group GPJ0 Control Register (GPJ0DAT, R/W, Address = 0xE020_0244)

GPJ0DAT	Bit	Description	Initial State
GPJ0DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.20.3 Port Group GPJ0 Control Register (GPJ0PUD, R/W, Address = 0xE020_0248)

GPJ0PUD	Bit	Description	Initial State
GPJ0PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x5555

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2.2.20.4 Port Group GPJ0 Control Register (GPJ0DRV, R/W, Address = 0xE020_024C)

GPJ0DRV	Bit	Description	Initial State
GPJ0DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.20.5 Port Group GPJ0 Control Register (GPJ0CONPDN, R/W, Address = 0xE020_0250)

GPJ0CONPDN	Bit	Description	Initial State
GPJ0[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.20.6 Port Group GPJ0 Control Register (GPJ0PUDPDN, R/W, Address = 0xE020_0254)

GPJ0PUDPDN	Bit	Description	Initial State
GPJ0[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.21 PORT GROUP GPJ1 CONTROL REGISTER

There are six control registers, namely, GPJ1CON, GPJ1DAT, GPJ1PUD, GPJ1DRV, GPJ1CONPDN and GPJ1PUDPDN in the Port Group GPJ1 Control Registers.

2.2.21.1 Port Group GPJ1 Control Register (GPJ1CON, R/W, Address = 0xE020_0260)

GPJ0CON	Bit	Description	Initial State
GPJ1CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = MSM_ADDR[13] 0011 = KP_COL[0] 0100 = SROM_ADDR_16to22[5] 0101 = MHL_D6 0110 ~ 1110 = Reserved 1111 = GPJ1_INT[5]	0000
GPJ1CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = MSM_ADDR[12] 0011 = CAM_B_CLKOUT 0100 = SROM_ADDR_16to22[4] 0101 = MHL_D5 0110 ~ 1110 = Reserved 1111 = GPJ1_INT[4]	0000
GPJ1CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = MSM_ADDR[11] 0011 = CAM_B_FIELD 0100 = SROM_ADDR_16to22[3] 0101 = MHL_D4 0110 ~ 1110 = Reserved 1111 = GPJ1_INT[3]	0000
GPJ1CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = MSM_ADDR[10] 0011 = CAM_B_HREF 0100 = SROM_ADDR_16to22[2] 0101 = MHL_D3 0110 ~ 1110 = Reserved 1111 = GPJ1_INT[2]	0000
GPJ1CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = MSM_ADDR[9] 0011 = CAM_B_VSYNC 0100 = SROM_ADDR_16to22[1] 0101 = MHL_D2 0110 ~ 1110 = Reserved 1111 = GPJ1_INT[1]	0000
GPJ1CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = MSM_ADDR[8] 0011 = CAM_B_PCLK 0100 = SROM_ADDR_16to22[0] 0101 = MHL_D1 0110 ~ 1110 = Reserved 1111 = GPJ1_INT[0]	0000

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2.2.21.2 Port Group GPJ1 Control Register (GPJ1DAT, R/W, Address = 0xE020_0264)

GPJ1DAT	Bit	Description	Initial State
GPJ1DAT[5:0]	[5:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.21.3 Port Group GPJ1 Control Register (GPJ1PUD, R/W, Address = 0xE020_0268)

GPJ1PUD	Bit	Description	Initial State
GPJ1PUD[n]	[2n+1:2n] n=0~5	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0555

2.2.21.4 Port Group GPJ1 Control Register (GPJ1DRV, R/W, Address = 0xE020_026C)

GPJ1DRV	Bit	Description	Initial State
GPJ1DRV[n]	[2n+1:2n] n=0~5	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.21.5 Port Group GPJ1 Control Register (GPJ1CONPDN, R/W, Address = 0xE020_0270)

GPJ1CONPDN	Bit	Description	Initial State
GPJ1[n]	[2n+1:2n] n=0~5	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.21.6 Port Group GPJ1 Control Register (GPJ1PUDPDN, R/W, Address = 0xE020_0274)

GPJ1PUDPDN	Bit	Description	Initial State
GPJ1[n]	[2n+1:2n] n=0~5	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.22 PORT GROUP GPJ2 CONTROL REGISTER

There are six control registers, namely, GPJ2CON, GPJ2DAT, GPJ2PUD, GPJ2DRV, GPJ2CONPDN and GPJ2PUDPDN in the Port Group GPJ2 Control Registers.

2.2.22.1 Port Group GPJ2 Control Register (GPJ2CON, R/W, Address = 0xE020_0280)

GPJ2CON	Bit	Description	Initial State
GPJ2CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = MSM_DATA[7] 0011 = KP_ROW[0] 0100 = CF_DATA[7] 0101 = MHL_D14 0110 ~ 1110 = Reserved 1111 = GPJ2_INT[7]	0000
GPJ2CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = MSM_DATA[6] 0011 = KP_COL[7] 0100 = CF_DATA[6] 0101 = MHL_D13 0110 ~ 1110 = Reserved 1111 = GPJ2_INT[6]	0000
GPJ2CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = MSM_DATA[5] 0011 = KP_COL[6] 0100 = CF_DATA[5] 0101 = MHL_D12 0110 ~ 1110 = Reserved 1111 = GPJ2_INT[5]	0000
GPJ2CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = MSM_DATA[4] 0011 = KP_COL[5] 0100 = CF_DATA[4] 0101 = MHL_D11 0110 ~ 1110 = Reserved 1111 = GPJ2_INT[4]	0000
GPJ2CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = MSM_DATA[3] 0011 = KP_COL[4] 0100 = CF_DATA[3] 0101 = MHL_D10 0110 ~ 1110 = Reserved 1111 = GPJ2_INT[3]	0000
GPJ2CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = MSM_DATA[2]	0000

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GPJ2CON	Bit	Description	Initial State
		0011 = KP_COL[3] 0100 = CF_DATA[2] 0101 = MHL_D9 0110 ~ 1110 = Reserved 1111 = GPJ2_INT[2]	
GPJ2CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = MSM_DATA[1] 0011 = KP_COL[2] 0100 = CF_DATA[1] 0101 = MHL_D8 0110 ~ 1110 = Reserved 1111 = GPJ2_INT[1]	0000
GPJ2CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = MSM_DATA[0] 0011 = KP_COL[1] 0100 = CF_DATA[0] 0101 = MHL_D7 0110 ~ 1110 = Reserved 1111 = GPJ2_INT[0]	0000

2.2.22.2 Port Group GPJ2 Control Register (GPJ2DAT, R/W, Address = 0xE020_0284)

GPJ2DAT	Bit	Description	Initial State
GPJ2DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.22.3 Port Group GPJ2 Control Register (GPJ2PUD, R/W, Address = 0xE020_0288)

GPJ2PUD	Bit	Description	Initial State
GPJ2PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x5555

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2.2.22.4 Port Group GPJ2 Control Register (GPJ2DRV, R/W, Address = 0xE020_028C)

GPJ2DRV	Bit	Description	Initial State
GPJ2DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.22.5 Port Group GPJ2 Control Register (GPJ2CONPDN, R/W, Address = 0xE020_0290)

GPJ2CONPDN	Bit	Description	Initial State
GPJ2[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.22.6 Port Group GPJ2 Control Register (GPJ2PUDPDN, R/W, Address = 0xE020_0294)

GPJ2PUDPDN	Bit	Description	Initial State
GPJ2[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.23 PORT GROUP GPJ3 CONTROL REGISTER

There are six control registers, namely, GPJ3CON, GPJ3DAT, GPJ3PUD, GPJ3DRV, GPJ3CONPDN and GPJ3PUDPDN in the Port Group GPJ3 Control Registers.

2.2.23.1 Port Group GPJ3 Control Register (GPJ3CON, R/W, Address = 0xE020_02A0)

GPJ3CON	Bit	Description	Initial State
GPJ3CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = MSM_DATA[15] 0011 = KP_ROW[8] 0100 = CF_DATA[15] 0101 = MHL_D22 0110 ~ 1110 = Reserved 1111 = GPJ3_INT[7]	0000
GPJ3CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = MSM_DATA[14] 0011 = KP_ROW[7] 0100 = CF_DATA[14] 0101 = MHL_D21 0110 ~ 1110 = Reserved 1111 = GPJ3_INT[6]	0000
GPJ3CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = MSM_DATA[13] 0011 = KP_ROW[6] 0100 = CF_DATA[13] 0101 = MHL_D20 0110 ~ 1110 = Reserved 1111 = GPJ3_INT[5]	0000
GPJ3CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = MSM_DATA[12] 0011 = KP_ROW[5] 0100 = CF_DATA[12] 0101 = MHL_D19 0110 ~ 1110 = Reserved 1111 = GPJ3_INT[4]	0000
GPJ3CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = MSM_DATA[11] 0011 = KP_ROW[4] 0100 = CF_DATA[11] 0101 = MHL_D18 0110 ~ 1110 = Reserved 1111 = GPJ3_INT[3]	0000
GPJ3CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = MSM_DATA[10]	0000

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GPJ3CON	Bit	Description	Initial State
		0011 = KP_ROW[3] 0100 = CF_DATA[10] 0101 = MHL_D17 0110 ~ 1110 = Reserved 1111 = GPJ3_INT[2]	
GPJ3CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = MSM_DATA[9] 0011 = KP_ROW[2] 0100 = CF_DATA[9] 0101 = MHL_D16 0110 ~ 1110 = Reserved 1111 = GPJ3_INT[1]	0000
GPJ3CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = MSM_DATA[8] 0011 = KP_ROW[1] 0100 = CF_DATA[8] 0101 = MHL_D15 0110 ~ 1110 = Reserved 1111 = GPJ3_INT[0]	0000

2.2.23.2 Port Group GPJ3 Control Register (GPJ3DAT, R/W, Address = 0xE020_02A4)

GPJ3DAT	Bit	Description	Initial State
GPJ3DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.23.3 Port Group GPJ3 Control Register (GPJ3PUD, R/W, Address = 0xE020_02A8)

GPJ3PUD	Bit	Description	Initial State
GPJ3PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x5555

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2.2.23.4 Port Group GPJ3 Control Register (GPJ3DRV, R/W, Address = 0xE020_02AC)

GPJ3DRV	Bit	Description	Initial State
GPJ3DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.23.5 Port Group GPJ3 Control Register (GPJ3CONPDN, R/W, Address = 0xE020_02B0)

GPJ3CONPDN	Bit	Description	Initial State
GPJ3[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.23.6 Port Group GPJ3 Control Register (GPJ3PUDPDN, R/W, Address = 0xE020_02B4)

GPJ3PUDPDN	Bit	Description	Initial State
GPJ3[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.24 PORT GROUP GPJ4 CONTROL REGISTER

There are six control registers, namely, GPJ4CON, GPJ4DAT, GPJ4PUD, GPJ4DRV, GPJ4CONPDN and GPJ4PUDPDN in the Port Group GPJ4 Control Registers.

2.2.24.1 Port Group GPJ4 Control Register (GPJ4CON, R/W, Address = 0xE020_02C0)

GPJ4CON	Bit	Description	Initial State
GPJ4CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = MSM_ADVN 0011 = KP_ROW[13] 0100 = SROM_ADDR_16to22[6] 0101 = MHL_DE 0110 ~ 1110 = Reserved 1111 = GPJ4_INT[4]	0000
GPJ4CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = MSM_IRQn 0011 = KP_ROW[12] 0100 = CF_IOWN 0101 = MHL_VSYNC 0110 ~ 1110 = Reserved 1111 = GPJ4_INT[3]	0000
GPJ4CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = MSM_Rn 0011 = KP_ROW[11] 0100 = CF_IORN 0101 = MHL_IDCK 0110 ~ 1110 = Reserved 1111 = GPJ4_INT[2]	0000
GPJ4CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = MSM_WEn 0011 = KP_ROW[10] 0100 = CF_CSn[1] 0101 = MHL_HSYNC 0110 ~ 1110 = Reserved 1111 = GPJ4_INT[1]	0000
GPJ4CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = MSM_CSn 0011 = KP_ROW[9] 0100 = CF_CSn[0] 0101 = MHL_D23 0110 ~ 1110 = Reserved 1111 = GPJ4_INT[0]	0000

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2.2.24.2 Port Group GPJ4 Control Register (GPJ4DAT, R/W, Address = 0xE020_02C4)

GPJ4DAT	Bit	Description	Initial State
GPJ4DAT[4:0]	[4:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.24.3 Port Group GPJ4 Control Register (GPJ4PUD, R/W, Address = 0xE020_02C8)

GPJ4PUD	Bit	Description	Initial State
GPJ4PUD[n]	[2n+1:2n] n=0~4	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0155

2.2.24.4 Port Group GPJ4 Control Register (GPJ4DRV, R/W, Address = 0xE020_02CC)

GPJ4DRV	Bit	Description	Initial State
GPJ4DRV[n]	[2n+1:2n] n=0~4	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

2.2.24.5 Port Group GPJ4 Control Register (GPJ4CONPDN, R/W, Address = 0xE020_02D0)

GPJ4CONPDN	Bit	Description	Initial State
GPJ4[n]	[2n+1:2n] n=0~4	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.24.6 Port Group GPJ4 Control Register (GPJ4PUDPDN, R/W, Address = 0xE020_02D4)

GPJ4PUDPDN	Bit	Description	Initial State
GPJ4[n]	[2n+1:2n] n=0~4	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.25 PORT GROUP MP0_1 CONTROL REGISTER

There are six control registers, namely, MP0_1CON, MP0_1DAT, MP0_1PUD, MP0_1DRV, MP0_1CONPDN and MP0_1PUDPDN in the Port Group MP0_1 Control Registers.

2.2.25.1 Port Group MP0_1 Control Register (MP0_1CON, R/W, Address = 0xE020_02E0)

MP0_1CON	Bit	Description	Initial State
MP0_1CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = EBI_WEn 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_1CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = EBI_OEn 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_1CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = SROM_CSn[5] 0011 = NFCSn[3] 0100 = Reserved 0101 = ONANDXL_CSn[1] 0110 ~ 1110 = Reserved 1111 = Reserved	0101
MP0_1CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = SROM_CSn[4] 0011 = NFCSn[2] 0100 = Reserved 0101 = ONANDXL_CSn[0] 0110 ~ 1110 = Reserved 1111 = Reserved	0101
MP0_1CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = SROM_CSn[3] 0011 = NFCSn[1] 0100 ~ 1110 = Reserved 1111 = Reserved	0011
MP0_1CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = SROM_CSn[2] 0011 = NFCSn[0] 0100 ~ 1110 = Reserved 1111 = Reserved	0011
MP0_1CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = SROM_CSn[1] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_1CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = SROM_CSn[0] 0011 ~ 1110 = Reserved 1111 = Reserved	0010

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2.2.25.2 Port Group MP0_1 Control Register (MP0_1DAT, R/W, Address = 0xE020_02E4)

MP0_1DAT	Bit	Description	Initial State
MP0_1DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.25.3 Port Group MP0_1 Control Register (MP0_1PUD, R/W, Address = 0xE020_02E8)

MP0_1PUD	Bit	Description	Initial State
MP0_1PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0000

2.2.25.4 Port Group MP0_1 Control Register (MP0_1DRV, R/W, Address = 0xE020_02EC)

MP0_1DRV	Bit	Description	Initial State
MP0_1DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

2.2.25.5 Port Group MP0_1 Control Register (MP0_1CONPDN, R/W, Address = 0xE020_02F0)

MP0_1CONPDN	Bit	Description	Initial State
MP0_1[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.25.6 Port Group MP0_1 Control Register (MP0_1PUDPDN, R/W, Address = 0xE020_02F4)

MP0_1PUDPDN	Bit	Description	Initial State
MP0_1[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.26 PORT GROUP MP0_2 CONTROL REGISTER

There are six control registers, namely, MP0_2CON, MP0_2DAT, MP0_2PUD, MP0_2DRV, MP0_2CONPDN and MP0_2PUDPDN in the Port Group MP0_2 Control Registers.

2.2.26.1 Port Group MP0_2 Control Register (MP0_2CON, R/W, Address = 0xE020_0300)

MP0_2CON	Bit	Description	Initial State
MP0_2CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = EBI_DATA_RDn 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_2CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = SROM_WAITn 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_2CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = EBI_BEn[1] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_2CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = EBI_BEn[0] 0011 ~ 1110 = Reserved 1111 = Reserved	0010

2.2.26.2 Port Group MP0_2 Control Register (MP0_2DAT, R/W, Address = 0xE020_0304)

MP0_2DAT	Bit	Description	Initial State
MP0_2DAT[3:0]	[3:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

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2.2.26.3 Port Group MP0_2 Control Register (MP0_2PUD, R/W, Address = 0xE020_0308)

MP0_2PUD	Bit	Description	Initial State
MP0_2PUD[n]	[2n+1:2n] n=0~3	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0000

2.2.26.4 Port Group MP0_2 Control Register (MP0_2DRV, R/W, Address = 0xE020_030C)

MP0_2DRV	Bit	Description	Initial State
MP0_2DRV[n]	[2n+1:2n] n=0~3	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x00AA

2.2.26.5 Port Group MP0_2 Control Register (MP0_2CONPDN, R/W, Address = 0xE020_0310)

MP0_2CONPDN	Bit	Description	Initial State
MP0_2[n]	[2n+1:2n] n=0~3	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.26.6 Port Group MP0_2 Control Register (MP0_2PUDPDN, R/W, Address = 0xE020_0314)

MP0_2PUDPDN	Bit	Description	Initial State
MP0_2[n]	[2n+1:2n] n=0~3	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.27 PORT GROUP MP0_3 CONTROL REGISTER

There are six control registers, namely, MP0_3CON, MP0_3DAT, MP0_3PUD, MP0_3DRV, MP0_3CONPDN and MP0_3PUDPDN in the Port Group MP0_3 Control Registers.

2.2.27.1 Port Group MP0_3 Control Register (MP0_3CON, R/W, Address = 0xE020_0320)

MP0_3CON	Bit	Description	Initial State
MP0_3CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = NF_RnB[3] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_3CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = NF_RnB[2] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_3CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = NF_RnB[1] 0011 = Reserved 0100 = Reserved 0101 = ONANDXL_INT[1] 0110 ~ 1110 = Reserved 1111 = Reserved	0101
MP0_3CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = NF_RnB[0] 0011 = Reserved 0100 = Reserved 0101 = ONANDXL_INT[0] 0110 ~ 1110 = Reserved 1111 = Reserved	0101
MP0_3CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = NF_FREn 0010 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_3CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = NF_FWEn 0011 = Reserved 0100 = Reserved 0101 = ONANDXL_RPn 0110 ~ 1110 = Reserved 1111 = Reserved	0101
MP0_3CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = NF_ALE 0011 = Reserved	0101

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MP0_3CON	Bit	Description	Initial State
		0100 = Reserved 0101 = ONANDXL_SMCLK 0110 ~ 1110 = Reserved 1111 = Reserved	
MP0_3CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = NF_CLE 0011 = Reserved 0100 = Reserved 0101 = ONANDXL_ADDRVALID 0110 ~ 1110 = Reserved 1111 = Reserved	0101

2.2.27.2 Port Group MP0_3 Control Register (MP0_3DAT, R/W, Address = 0xE020_0324)

MP0_3DAT	Bit	Description	Initial State
MP0_3DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.27.3 Port Group MP0_3 Control Register (MP0_3PUD, R/W, Address = 0xE020_0328)

MP0_3PUD	Bit	Description	Initial State
MP0_3PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0000

2.2.27.4 Port Group MP0_3 Control Register (MP0_3DRV, R/W, Address = 0xE020_032C)

MP0_3DRV	Bit	Description	Initial State
MP0_3DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

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2.2.27.5 Port Group MP0_3 Control Register (MP0_3CONPDN, R/W, Address = 0xE020_0330)

MP0_3CONPDN	Bit	Description	Initial State
MP0_3[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.27.6 Port Group MP0_3 Control Register (MP0_3PUDPDN, R/W, Address = 0xE020_0334)

MP0_3PUDPDN	Bit	Description	Initial State
MP0_3[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.28 PORT GROUP MP0_4 CONTROL REGISTER

There are six control registers, namely, MP0_4CON, MP0_4DAT, MP0_4PUD, MP0_4DRV, MP0_4CONPDN and MP0_4PUDPDN in the Port Group MP0_4 Control Registers.

2.2.28.1 Port Group MP0_4 Control Register (MP0_4CON, R/W, Address = 0xE020_0340)

MP0_4CON	Bit	Description	Initial State
MP0_4CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = EBI_ADDR[0] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_4CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = EBI_ADDR[1] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_4CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = EBI_ADDR[2] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_4CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = EBI_ADDR[3] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_4CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = EBI_ADDR[4] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_4CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = EBI_ADDR[5] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_4CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = EBI_ADDR[6] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_4CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = EBI_ADDR[7] 0011 ~ 1110 = Reserved 1111 = Reserved	0010

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2.2.28.2 Port Group MP0_4 Control Register (MP0_4DAT, R/W, Address = 0xE020_0344)

MP0_4DAT	Bit	Description	Initial State
MP0_4DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.28.3 Port Group MP0_4 Control Register (MP0_4PUD, R/W, Address = 0xE020_0348)

MP0_4PUD	Bit	Description	Initial State
MP0_4PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0000

2.2.28.4 Port Group MP0_4 Control Register (MP0_4DRV, R/W, Address = 0xE020_034C)

MP0_4DRV	Bit	Description	Initial State
MP0_4DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

2.2.28.5 Port Group MP0_4 Control Register (MP0_4CONPDN, R/W, Address = 0xE020_0350)

MP0_4CONPDN	Bit	Description	Initial State
MP0_4[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.28.6 Port Group MP0_4 Control Register (MP0_4PUDPDN, R/W, Address = 0xE020_0354)

MP0_4PUDPDN	Bit	Description	Initial State
MP0_4[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.29 PORT GROUP MP0_5 CONTROL REGISTER

There are six control registers, namely, MP0_5CON, MP0_5DAT, MP0_5PUD, MP0_5DRV, MP0_5CONPDN and MP0_5PUDPDN in the Port Group MP0_5 Control Registers.

2.2.29.1 Port Group MP0_5 Control Register (MP0_5CON, R/W, Address = 0xE020_0360)

MP0_5CON	Bit	Description	Initial State
MP0_5CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = EBI_ADDR[8] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_5CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = EBI_ADDR[9] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_5CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = EBI_ADDR[10] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_5CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = EBI_ADDR[11] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_5CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = EBI_ADDR[12] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_5CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = EBI_ADDR[13] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_5CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = EBI_ADDR[14] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_5CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = EBI_ADDR[15] 0011 ~ 1110 = Reserved 1111 = Reserved	0010

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2.2.29.2 Port Group MP0_5 Control Register (MP0_5DAT, R/W, Address = 0xE020_0364)

MP0_5DAT	Bit	Description	Initial State
MP0_5DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.29.3 Port Group MP0_5 Control Register (MP0_5PUD, R/W, Address = 0xE020_0368)

MP0_5PUD	Bit	Description	Initial State
MP0_5PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0000

2.2.29.4 Port Group MP0_5 Control Register (MP0_5DRV, R/W, Address = 0xE020_036C)

MP0_5DRV	Bit	Description	Initial State
MP0_5DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

2.2.29.5 Port Group MP0_5 Control Register (MP0_5CONPDN, R/W, Address = 0xE020_0370)

MP0_5CONPDN	Bit	Description	Initial State
MP0_5[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.29.6 Port Group MP0_5 Control Register (MP0_5PUDPDN, R/W, Address = 0xE020_0374)

MP0_5PUDPDN	Bit	Description	Initial State
MP0_5[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.30 PORT GROUP MP0_6 CONTROL REGISTER

There are six control registers, namely, MP0_6CON, MP0_6DAT, MP0_6PUD, MP0_6DRV, MP0_6CONPDN and MP0_6PUDPDN in the Port Group MP0_6 Control Registers.

2.2.30.1 Port Group MP0_6 Control Register (MP0_6CON, R/W, Address = 0xE020_0380)

MP0_6CON	Bit	Description	Initial State
MP0_6CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = EBI_DATA[0] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_6CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = EBI_DATA[1] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_6CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = EBI_DATA[2] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_6CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = EBI_DATA[3] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_6CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = EBI_DATA[4] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_6CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = EBI_DATA[5] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_6CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = EBI_DATA[6] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_6CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = EBI_DATA[7] 0011 ~ 1110 = Reserved 1111 = Reserved	0010

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2.2.30.2 Port Group MP0_6 Control Register (MP0_6DAT, R/W, Address = 0xE020_0384)

MP0_6DAT	Bit	Description	Initial State
MP0_6DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.30.3 Port Group MP0_6 Control Register (MP0_6PUD, R/W, Address = 0xE020_0388)

MP0_6PUD	Bit	Description	Initial State
MP0_6PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0000

2.2.30.4 Port Group MP0_6 Control Register (MP0_6DRV, S/W, Address = 0xE020_038C)

MP0_6DRV	Bit	Description	Initial State
MP0_6DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

2.2.30.5 Port Group MP0_6 Control Register (MP0_6CONPDN, S/W, Address = 0xE020_0390)

MP0_6CONPDN	Bit	Description	Initial State
MP0_6[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.30.6 Port Group MP0_6 Control Register (MP0_6PUDPDN, S/W, Address = 0xE020_0394)

MP0_6PUDPDN	Bit	Description	Initial State
MP0_6[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.31 PORT GROUP MP0_7 CONTROL REGISTER

There are six control registers, namely, MP0_7CON, MP0_7DAT, MP0_7PUD, MP0_7DRV, MP0_7CONPDN and MP0_7PUDPDN in the Port Group MP0_7 Control Registers.

2.2.31.1 Port Group MP0_7 Control Register (MP0_7CON, R/W, Address = 0xE020_03A0)

MP0_7CON	Bit	Description	Initial State
MP0_7CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = EBI_DATA[8] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_7CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = EBI_DATA[9] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_7CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = EBI_DATA[10] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_7CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = EBI_DATA[11] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_7CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = EBI_DATA[12] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_7CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = EBI_DATA[13] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_7CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = EBI_DATA[14] 0011 ~ 1110 = Reserved 1111 = Reserved	0010
MP0_7CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = EBI_DATA[15] 0011 ~ 1110 = Reserved 1111 = Reserved	0010

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2.2.31.2 Port Group MP0_7 Control Register (MP0_7DAT, R/W, Address = 0xE020_03A4)

MP0_7DAT	Bit	Description	Initial State
MP0_7DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.31.3 Port Group MP0_7 Control Register (MP0_7PUD, R/W, Address = 0xE020_03A8)

MP0_7PUD	Bit	Description	Initial State
MP0_7PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0000

2.2.31.4 Port Group MP0_7 Control Register (MP0_7DRV, R/W, Address = 0xE020_03AC)

MP0_7DRV	Bit	Description	Initial State
MP0_7DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

2.2.31.5 Port Group MP0_7 Control Register (MP0_7CONPDN, R/W, Address = 0xE020_03B0)

MP0_7CONPDN	Bit	Description	Initial State
MP0_7[n]	[2n+1:2n] n=0~7	00 = Output 0 01 = Output 1 10 = Input 11 = Previous state	0x00

2.2.31.6 Port Group MP0_7 Control Register (MP0_7PUDPDN, R/W, Address = 0xE020_03B4)

MP0_7PUDPDN	Bit	Description	Initial State
MP0_7[n]	[2n+1:2n] n=0~7	00 = Pull-up/down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.32 PORT GROUP MP1_0 CONTROL REGISTER

There are six control registers, namely, MP1_0CON, MP1_0DAT, MP1_0PUD, MP1_0DRV, MP1_0CONPDN and MP1_0PUDPDN in the Port Group MP1_0 Control Registers.

- MP1_0CON, R/W, Address = 0xE020_03C0
- MP1_0DAT, R/W, Address = 0xE020_03C4
- MP1_0PUD, R/W, Address = 0xE020_03C8
- MP1_0DRV, R/W, Address = 0xE020_03CC
- MP1_0CONPDN, R/W, Address = 0xE020_03D0
- MP1_0PUDPDN, R/W, Address = 0xE020_03D4

MP1_0DRV	Bit	Description	Initial State
MP1_0DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

2.2.33 PORT GROUP MP1_1 CONTROL REGISTER

There are six control registers, namely, MP1_1CON, MP1_1DAT, MP1_1PUD, MP1_1DRV, MP1_1CONPDN and MP1_1PUDPDN in the Port Group MP1_1 Control Registers.

- MP1_1CON, R/W, Address = 0xE020_03E0
- MP1_1DAT, R/W, Address = 0xE020_03E4
- MP1_1PUD, R/W, Address = 0xE020_03E8
- MP1_1DRV, R/W, Address = 0xE020_03EC
- MP1_1CONPDN, R/W, Address = 0xE020_03F0
- MP1_1PUDPDN, R/W, Address = 0xE020_03F4

MP1_1DRV	Bit	Description	Initial State
MP1_1DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

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2.2.34 PORT GROUP MP1_2 CONTROL REGISTER

There are six control registers, namely, MP1_2CON, MP1_2DAT, MP1_2PUD, MP1_2DRV, MP1_2CONPDN and MP1_2PUDPDN in the Port Group MP1_2 Control Registers.

- MP1_2CON, R/W, Address = 0xE020_0400
- MP1_2DAT, R/W, Address = 0xE020_0404
- MP1_2PUD, R/W, Address = 0xE020_0408
- MP1_2DRV, R/W, Address = 0xE020_040C
- MP1_2CONPDN, R/W, Address = 0xE020_0410
- MP1_2PUDPDN, R/W, Address = 0xE020_0414

MP1_2DRV	Bit	Description	Initial State
MP1_2DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

2.2.35 PORT GROUP MP1_3 CONTROL REGISTER

There are six control registers, namely, MP1_3CON, MP1_3DAT, MP1_3PUD, MP1_3DRV, MP1_3CONPDN and MP1_3PUDPDN in the Port Group MP1_3 Control Registers.

- MP1_3CON, R/W, Address = 0xE020_0420
- MP1_3DAT, R/W, Address = 0xE020_0424
- MP1_3PUD, R/W, Address = 0xE020_0428
- MP1_3DRV, R/W, Address = 0xE020_042C
- MP1_3CONPDN, R/W, Address = 0xE020_0430
- MP1_3PUDPDN, R/W, Address = 0xE020_0434

MP1_3DRV	Bit	Description	Initial State
MP1_3DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

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2.2.36 PORT GROUP MP1_4 CONTROL REGISTER

There are six control registers, namely, MP1_4CON, MP1_4DAT, MP1_4PUD, MP1_4DRV, MP1_4CONPDN and MP1_4PUDPDN in the Port Group MP1_4 Control Registers.

- MP1_4CON, R/W, Address = 0xE020_0440
- MP1_4DAT, R/W, Address = 0xE020_0444
- MP1_4PUD, R/W, Address = 0xE020_0448
- MP1_4DRV, R/W, Address = 0xE020_044C
- MP1_4CONPDN, R/W, Address = 0xE020_0450
- MP1_4PUDPDN, R/W, Address = 0xE020_0454

MP1_4DRV	Bit	Description	Initial State
MP1_4DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

2.2.37 PORT GROUP MP1_5 CONTROL REGISTER

There are six control registers, namely, MP1_5CON, MP1_5DAT, MP1_5PUD, MP1_5DRV, MP1_5CONPDN and MP1_5PUDPDN in the Port Group MP1_5 Control Registers.

- MP1_5CON, R/W, Address = 0xE020_0460
- MP1_5DAT, R/W, Address = 0xE020_0464
- MP1_5PUD, R/W, Address = 0xE020_0468
- MP1_5DRV, R/W, Address = 0xE020_046C
- MP1_5CONPDN, R/W, Address = 0xE020_0470
- MP1_5PUDPDN, R/W, Address = 0xE020_0474

MP1_5DRV	Bit	Description	Initial State
MP1_5DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

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2.2.38 PORT GROUP MP1_6 CONTROL REGISTER

There are six control registers, namely, MP1_6CON, MP1_6DAT, MP1_6PUD, MP1_6DRV, MP1_6CONPDN and MP1_6PUDPDN in the Port Group MP1_6 Control Registers.

- MP1_6CON, R/W, Address = 0xE020_0480
- MP1_6DAT, R/W, Address = 0xE020_0484
- MP1_6PUD, R/W, Address = 0xE020_0488
- MP1_6DRV, R/W, Address = 0xE020_048C
- MP1_6CONPDN, R/W, Address = 0xE020_0490
- MP1_6PUDPDN, R/W, Address = 0xE020_0494

MP1_6DRV	Bit	Description	Initial State
MP1_6DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

2.2.39 PORT GROUP MP1_7 CONTROL REGISTER

There are six control registers, namely, MP1_7CON, MP1_7DAT, MP1_7PUD, MP1_7DRV, MP1_7CONPDN and MP1_7PUDPDN in the Port Group MP1_7 Control Registers.

- MP1_7CON, R/W, Address = 0xE020_04A0
- MP1_7DAT, R/W, Address = 0xE020_04A4
- MP1_7PUD, R/W, Address = 0xE020_04A8
- MP1_7DRV, R/W, Address = 0xE020_04AC
- MP1_7CONPDN, R/W, Address = 0xE020_04B0
- MP1_7PUDPDN, R/W, Address = 0xE020_04B4

MP1_7DRV	Bit	Description	Initial State
MP1_7DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

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2.2.40 PORT GROUP MP1_8 CONTROL REGISTER

There are six control registers, namely, MP1_8CON, MP1_8DAT, MP1_8PUD, MP1_8DRV, MP1_8CONPDN and MP1_8PUDPDN in the Port Group MP1_8 Control Registers.

- MP1_8CON, R/W, Address = 0xE020_04C0
- MP1_8DAT, R/W, Address = 0xE020_04C4
- MP1_8PUD, R/W, Address = 0xE020_04C8
- MP1_8DRV, R/W, Address = 0xE020_04CC
- MP1_8CONPDN, R/W, Address = 0xE020_04D0
- MP1_8PUDPDN, R/W, Address = 0xE020_04D4

MP1_8DRV	Bit	Description	Initial State
MP1_8DRV[n]	[2n+1:2n] n=0~6	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x2AAA

2.2.41 PORT GROUP MP2_0 CONTROL REGISTER

There are six control registers, namely, MP2_0CON, MP2_0DAT, MP2_0PUD, MP2_0DRV, MP2_0CONPDN and MP2_0PUDPDN in the Port Group MP2_0 Control Registers.

- MP2_0CON, R/W, Address = 0xE020_04E0
- MP2_0DAT, R/W, Address = 0xE020_04E4
- MP2_0PUD, R/W, Address = 0xE020_04E8
- MP2_0DRV, R/W, Address = 0xE020_04EC
- MP2_0CONPDN, R/W, Address = 0xE020_04F0
- MP2_0PUDPDN, R/W, Address = 0xE020_04F4

MP2_0DRV	Bit	Description	Initial State
MP2_0DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

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2.2.42 PORT GROUP MP2_1 CONTROL REGISTER

There are six control registers, namely, MP2_1CON, MP2_1DAT, MP2_1PUD, MP2_1DRV, MP2_1CONPDN and MP2_1PUDPDN in the Port Group MP2_1 Control Registers.

- MP2_1CON, R/W, Address = 0xE020_0500
- MP2_1DAT, R/W, Address = 0xE020_0504
- MP2_1PUD, R/W, Address = 0xE020_0508
- MP2_1DRV, R/W, Address = 0xE020_050C
- MP2_1CONPDN, R/W, Address = 0xE020_0510
- MP2_1PUDPDN, R/W, Address = 0xE020_0514

MP2_1DRV	Bit	Description	Initial State
MP2_1DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

2.2.43 PORT GROUP MP2_2 CONTROL REGISTER

There are six control registers, namely, MP2_2CON, MP2_2DAT, MP2_2PUD, MP2_2DRV, MP2_2CONPDN and MP2_2PUDPDN in the Port Group MP2_2 Control Registers.

- MP2_2CON, R/W, Address = 0xE020_0520
- MP2_2DAT, R/W, Address = 0xE020_0524
- MP2_2PUD, R/W, Address = 0xE020_0528
- MP2_2DRV, R/W, Address = 0xE020_052C
- MP2_2CONPDN, R/W, Address = 0xE020_0530
- MP2_2PUDPDN, R/W, Address = 0xE020_0534

MP2_2DRV	Bit	Description	Initial State
MP2_2DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

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2.2.44 PORT GROUP MP2_3 CONTROL REGISTER

There are six control registers, namely, MP2_3CON, MP2_3DAT, MP2_3PUD, MP2_3DRV, MP2_3CONPDN and MP2_3PUDPDN in the Port Group MP2_3 Control Registers.

- MP2_3CON, R/W, Address = 0xE020_0540
- MP2_3DAT, R/W, Address = 0xE020_0544
- MP2_3PUD, R/W, Address = 0xE020_0548
- MP2_3DRV, R/W, Address = 0xE020_054C
- MP2_3CONPDN, R/W, Address = 0xE020_0550
- MP2_3PUDPDN, R/W, Address = 0xE020_0554

MP2_3DRV	Bit	Description	Initial State
MP2_3DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

2.2.45 PORT GROUP MP2_4 CONTROL REGISTER

There are six control registers, namely, MP2_4CON, MP2_4DAT, MP2_4PUD, MP2_4DRV, MP2_4CONPDN and MP2_4PUDPDN in the Port Group MP2_4 Control Registers.

- MP2_4CON, R/W, Address = 0xE020_0560
- MP2_4DAT, R/W, Address = 0xE020_0564
- MP2_4PUD, R/W, Address = 0xE020_0568
- MP2_4DRV, R/W, Address = 0xE020_056C
- MP2_4CONPDN, R/W, Address = 0xE020_0570
- MP2_4PUDPDN, R/W, Address = 0xE020_0574

MP2_4DRV	Bit	Description	Initial State
MP2_4DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

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2.2.46 PORT GROUP MP2_5 CONTROL REGISTER

There are six control registers, namely, MP2_5CON, MP2_5DAT, MP2_5PUD, MP2_5DRV, MP2_5CONPDN and MP2_5PUDPDN in the Port Group MP2_5 Control Registers.

- MP2_5CON, R/W, Address = 0xE020_0580
- MP2_5DAT, R/W, Address = 0xE020_0584
- MP2_5PUD, R/W, Address = 0xE020_0588
- MP2_5DRV, R/W, Address = 0xE020_058C
- MP2_5CONPDN, R/W, Address = 0xE020_0590
- MP2_5PUDPDN, R/W, Address = 0xE020_0594

MP2_5DRV	Bit	Description	Initial State
MP2_5DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

2.2.47 PORT GROUP MP2_6 CONTROL REGISTER

There are six control registers, namely, MP2_6CON, MP2_6DAT, MP2_6PUD, MP2_6DRV, MP2_6CONPDN and MP2_6PUDPDN in the Port Group MP2_6 Control Registers.

- MP2_6CON, R/W, Address = 0xE020_05A0
- MP2_6DAT, R/W, Address = 0xE020_05A4
- MP2_6PUD, R/W, Address = 0xE020_05A8
- MP2_6DRV, R/W, Address = 0xE020_05AC
- MP2_6CONPDN, R/W, Address = 0xE020_05B0
- MP2_6PUDPDN, R/W, Address = 0xE020_05B4

MP2_6DRV	Bit	Description	Initial State
MP2_6DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

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2.2.48 PORT GROUP MP2_7 CONTROL REGISTER

There are six control registers, namely, MP2_7CON, MP2_7DAT, MP2_7PUD, MP2_7DRV, MP2_7CONPDN and MP2_7PUDPDN in the Port Group MP2_7 Control Registers.

- MP2_7CON, R/W, Address = 0xE020_05C0
- MP2_7DAT, R/W, Address = 0xE020_05C4
- MP2_7PUD, R/W, Address = 0xE020_05C8
- MP2_7DRV, R/W, Address = 0xE020_05CC
- MP2_7CONPDN, R/W, Address = 0xE020_05D0
- MP2_7PUDPDN, R/W, Address = 0xE020_05D4

MP2_7DRV	Bit	Description	Initial State
MP2_7DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0xAAAA

2.2.49 PORT GROUP MP2_8 CONTROL REGISTER

There are six control registers, namely, MP2_8CON, MP2_8DAT, MP2_8PUD, MP2_8DRV, MP2_8CONPDN and MP2_8PUDPDN in the Port Group MP2_8 Control Registers.

- MP2_8CON, R/W, Address = 0xE020_05E0
- MP2_8DAT, R/W, Address = 0xE020_05E4
- MP2_8PUD, R/W, Address = 0xE020_05E8
- MP2_8DRV, R/W, Address = 0xE020_05EC
- MP2_8CONPDN, R/W, Address = 0xE020_05F0
- MP2_8PUDPDN, R/W, Address = 0xE020_05F4

MP2_8DRV	Bit	Description	Initial State
MP2_8DRV[n	[2n+1:2n] n=0~6	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x2AAA

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2.2.50 PORT GROUP ETC0 CONTROL REGISTER

There are two control registers, namely, ETC0PUD and ETC0DRV.

ETC0 ports are dedicated as shown in table below:

ETC0	Pin Name	Description	Initial State
ETC0[0]	XjTRSTn	JTAG TAP Controller Reset	0
ETC0[1]	XjTMS	JTAG TAP Controller Mode Select	0
ETC0[2]	XjTCK	JTAG TAP Controller Clock	0
ETC0[3]	XjTDI	JTAG TAP Controller Data Input	0
ETC0[4]	XjTDI	JTAG TAP Controller Data Input	0
ETC0[5]	XjDBGSEL	JTAG selection(0: CORTEXA8 Core JTAG, 1: Peripherals JTAG)	0

2.2.50.1 Port Group ETC0 Control Register (ETC0PUD, R/W, Address = 0xE020_0608)

ETC0PUD	Bit	Description	Initial State
ETC0PUD	[2n+1:2n] n=4~5	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00
ETC0PUD[m]	[2m+1:2m] m=0~3	Reserved (fixed) ETC0PUD[0] : Pull-down ETC0PUD[1] : Pull-up ETC0PUD[2] : Pull-down ETC0PUD[3] : Pull-up	0x00

2.2.50.2 Port Group ETC0 Control Register (ETC0DRV, R/W, Address = 0xE020_060C)

ETC0DRV	Bit	Description	Initial State
ETC0DRV[n]	[2n+1:2n] n=0~5	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

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2.2.51 PORT GROUP ETC1 CONTROL REGISTER

There are two control registers, namely, ETC1PUD and ETC1DRV.

ETC1 ports are dedicated as shown in table below:

ETC1	Pin Name	Description	Initial State
ETC1[0]	XOM[0]	Operating Mode control signal 0	0
ETC1[1]	XOM[1]	Operating Mode control signal 1	0
ETC1[2]	XOM[2]	Operating Mode control signal 2	0
ETC1[3]	XOM[3]	Operating Mode control signal 3	0
ETC1[4]	XOM[4]	Operating Mode control signal 4	0
ETC1[5]	XOM[5]	Operating Mode control signal 5	0
ETC1[6]	XDDR2_SEL	Selection DDR type (LPDDR1/2 or DDR2)	0
ETC1[7]	XPWRRGTON	Power Regulator enable	0

2.2.51.1 Port Group ETC1 Control Register (ETC1PUD, R/W, Address = 0xE020_0628)

ETC1PUD	Bit	Description	Initial State
ETC1PUD[n]	[2n+1:2n] n=0~5	Reserved(fixed) ETC1PUD[0] : Disable ETC1PUD[1] : Disable ETC1PUD[2] : Disable ETC1PUD[3] : Disable ETC1PUD[4] : Disable ETC1PUD[5] : Disable	0x000
ETC1PUD[6]	[13:12]	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x0
ETC1PUD[7]	[15:14]	Reserved (fixed) ETC1PUD[7] : Disable	0x0

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2.2.51.2 Port Group ETC1 Control Register (ETC1DRV, R/W, Address = 0xE020_062C)

ETC1DRV	Bit	Description	Initial State
ETC1DRV[n]	[2n+1:2n] n=0~5	Reserved(fixed) ETC1DRV[0] : 01 (3x) ETC1DRV[1] : 01 (3x) ETC1DRV[2] : 01 (3x) ETC1DRV[3] : 01 (3x) ETC1DRV[4] : 01 (3x) ETC1DRV[5] : 01 (3x)	-
ETC1DRV[6]	[13:12]	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0
ETC1DRV[7]	[15:14]	Reserved(fixed) ETC1DRV[7] : 11 (4x)	-

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2.2.52 PORT GROUP ETC2 CONTROL REGISTER

There are two control registers, namely, ETC2PUD and ETC2DRV.

ETC2 ports are dedicated as shown in table below:

ETC2	Pin Name	Description	Initial State
ETC2[0]	XnRESET	System Reset	0
ETC2[1]	CLKOUT	Clock out signal	0
ETC2[2]	XnRSTOUT	For External device reset control	0
ETC2[3]	XnWRESET	System Warm Reset	0
ETC2[4]	RTC_CLKOUT	RTC Clock out	0
ETC2[5]	XuotgDRVVBUS	USB OTG charge pump enable	0
ETC2[6]	XuhostPWREN	USB HOST charge pump enable	0
ETC2[7]	XuhostOVERCUR	USB HOST oevercurrent flag	0

2.2.52.1 Port Group ETC2 Control Register (ETC2PUD, R/W, Address = 0xE020_0648)

ETC2PUD	Bit	Description	Initial State
ETC2PUD[n]	[2n+1:2n] n=0~4	Reserved(fixed) ETC2PUD[0] : Disable ETC2PUD[1] : Disable ETC2PUD[2] : Disable ETC2PUD[3] : Pull-up ETC2PUD[4] : Disable	0x00
ETC2PUD[m]	[2m+1:2m] m=5~7	00 = Pull-up/ down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x00

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2.2.52.2 Port Group ETC2 Control Register (ETC2DRV, R/W, Address = 0xE020_064C)

ETC2DRV	Bit	Description	Initial State
ETC2DRV[0]	[1:0]	Reserved(fixed) ETC2DRV[0] : 01 (3x)	-
ETC2DRV[1]	[3:2]	00 = 1x 10 = 2x 01 = 3x 11 = 4x	00
ETC2DRV[n]	[2n+1:2n] n=2~4	Reserved(fixed) ETC2DRV[2] : 11 (4x) ETC2DRV[3] : 01 (3x) ETC2DRV[4] : 10 (2x)	-
ETC2DRV[m]	[2m+1:2m] m=7~5	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0

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2.2.53 PORT GROUP ETC3 IS RESERVED

2.2.54 PORT GROUP ETC4

There is no registers.

ETC4 ports are dedicated as shown in table below:

ETC4	Pin Name	Description	Initial State
ETC4[0]	XrtcXTI	32 KHz crystal input for RTC	0
ETC4[1]	XrtcXTO	32 KHz crystal output for RTC	0
ETC4[2]	XXTI	Crystal input for internal OSC circuit	0
ETC4[3]	XXTO	Crystal output for internal OSC circuit	0
ETC4[4]	XusbXTI	Crystal input for internal USB circuit	0
ETC4[5]	XusbXTO	Crystal output for internal USB circuit	0

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2.2.55 GPIO INTERRUPT CONTROL REGISTERS

GPIO Interrupt comprise of 22 groups, namely, GPA0, GPA1, GPB, GPC0, GPC1, GPD0, GPD1, GPE0, GPE1, GPF0, GPF1, GPF2, GPF3, GPG0, GPG1, GPG2, GPG3, GPJ0, GPJ1, GPJ2, GPJ3 and GPJ4.

In interrupt function, it is important to understand the filter operation.

S5PV210 uses two types of filters to detect interrupt, namely, delay filter and digital filter.

Delay filter uses delay cell.

If clock is not serviced, select the delay filter in alive area.

Delay filter enables to detect interrupt after 35ns from the time when the interrupt occurs.

Digital filter means that all interrupt counts are based on clock.

Therefore, this filter can be used in clock-supported area.(both off area and alive area)

When you select digital filter set the filtering width.

Digital filter can detect interrupt per every clock count as many as filtering width.

Filtering width is 6-bit in alive area and is 7-bit in off area.

When you use interrupt function, set either delay or digital filter enabled in order to detect interrupt.

If filter is disabled, there is strong probability that system detects all interrupt from successive interrupts (Some interrupt detection will be missed).

To detect all interrupts stably, you had better set filter enable.

GPIO Interrupt cannot use for wake-up source. For wake-up interrupt source, you can use External interrupt.

The following table shows the list of GPIO Interrupt control registers.

Register	Address	R/W	Description	Reset Value
GPA0_INT_CON	0xE020_0700	R/W	GPIO Interrupt GPA0_INT Configuration Register	0x0
GPA1_INT_CON	0xE020_0704	R/W	GPIO Interrupt GPA1_INT Configuration Register	0x0
GPB_INT_CON	0xE020_0708	R/W	GPIO Interrupt GPB_INT Configuration Register	0x0
GPC0_INT_CON	0xE020_070C	R/W	GPIO Interrupt GPC0_INT Configuration Register	0x0
GPC1_INT_CON	0xE020_0710	R/W	GPIO Interrupt GPC1_INT Configuration Register	0x0
GPD0_INT_CON	0xE020_0714	R/W	GPIO Interrupt GPD0_INT Configuration Register	0x0
GPD1_INT_CON	0xE020_0718	R/W	GPIO Interrupt GPD1_INT Configuration Register	0x0
GPE0_INT_CON	0xE020_071C	R/W	GPIO Interrupt GPE0_INT Configuration	0x0

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Register	Address	R/W	Description	Reset Value
			Register	
GPE1_INT_CON	0xE020_0720	R/W	GPIO Interrupt GPE1_INT Configuration Register	0x0
GPF0_INT_CON	0xE020_0724	R/W	GPIO Interrupt GPF0_INT Configuration Register	0x0
GPF1_INT_CON	0xE020_0728	R/W	GPIO Interrupt GPF1_INT Configuration Register	0x0
GPF2_INT_CON	0xE020_072C	R/W	GPIO Interrupt GPF2_INT Configuration Register	0x0
GPF3_INT_CON	0xE020_0730	R/W	GPIO Interrupt GPF3_INT Configuration Register	0x0
GPG0_INT_CON	0xE020_0734	R/W	GPIO Interrupt GPG0_INT Configuration Register	0x0
GPG1_INT_CON	0xE020_0738	R/W	GPIO Interrupt GPG1_INT Configuration Register	0x0
GPG2_INT_CON	0xE020_073C	R/W	GPIO Interrupt GPG2_INT Configuration Register	0x0
GPG3_INT_CON	0xE020_0740	R/W	GPIO Interrupt GPG3_INT Configuration Register	0x0
GPJ0_INT_CON	0xE020_0744	R/W	GPIO Interrupt GPJ0_INT Configuration Register	0x0
GPJ1_INT_CON	0xE020_0748	R/W	GPIO Interrupt GPJ1_INT Configuration Register	0x0
GPJ2_INT_CON	0xE020_074C	R/W	GPIO Interrupt GPJ2_INT Configuration Register	0x0
GPJ3_INT_CON	0xE020_0750	R/W	GPIO Interrupt GPJ3_INT Configuration Register	0x0
GPJ4_INT_CON	0xE020_0754	R/W	GPIO Interrupt GPJ4_INT Configuration Register	0x0
GPA0_INT_FLTCON0	0xE020_0800	R/W	GPIO Interrupt GPA0_INT Filter Configuration Register 0	0x0
GPA0_INT_FLTCON1	0xE020_0804	R/W	GPIO Interrupt GPA0_INT Filter Configuration Register 1	0x0
GPA1_INT_FLTCON0	0xE020_0808	R/W	GPIO Interrupt GPA1_INT Filter Configuration Register 0	0x0
GPA1_INT_FLTCON1	0xE020_080C	R/W	GPIO Interrupt GPA1_INT Filter Configuration Register 1	0x0
GPB_INT_FLTCON0	0xE020_0810	R/W	GPIO Interrupt GPB_INT Filter Configuration Register 0	0x0
GPB_INT_FLTCON1	0xE020_0814	R/W	GPIO Interrupt GPB_INT Filter Configuration Register 1	0x0
GPC0_INT_FLTCON0	0xE020_0818	R/W	GPIO Interrupt GPC0_INT Filter Configuration Register 0	0x0

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Register	Address	R/W	Description	Reset Value
GPC0_INT_FLTCON1	0xE020_081C	R/W	GPIO Interrupt GPC0_INT Filter Configuration Register 1	0x0
GPC1_INT_FLTCON0	0xE020_0820	R/W	GPIO Interrupt GPC1_INT Filter Configuration Register 0	0x0
GPC1_INT_FLTCON1	0xE020_0824	R/W	GPIO Interrupt GPC1_INT Filter Configuration Register 1	0x0
GPD0_INT_FLTCON0	0xE020_0828	R/W	GPIO Interrupt GPD0_INT Filter Configuration Register 0	0x0
GPD0_INT_FLTCON1	0xE020_082C	R/W	GPIO Interrupt GPD0_INT Filter Configuration Register 1	0x0
GPD1_INT_FLTCON0	0xE020_0830	R/W	GPIO Interrupt GPD1_INT Filter Configuration Register 0	0x0
GPD1_INT_FLTCON1	0xE020_0834	R/W	GPIO Interrupt GPD1_INT Filter Configuration Register 1	0x0
GPE0_INT_FLTCON0	0xE020_0838	R/W	GPIO Interrupt GPE0_INT Filter Configuration Register 0	0x0
GPE0_INT_FLTCON1	0xE020_083C	R/W	GPIO Interrupt GPE0_INT Filter Configuration Register 1	0x0
GPE1_INT_FLTCON0	0xE020_0840	R/W	GPIO Interrupt GPE1_INT Filter Configuration Register 0	0x0
GPE1_INT_FLTCON1	0xE020_0844	R/W	GPIO Interrupt GPE1_INT Filter Configuration Register 1	0x0
GPF0_INT_FLTCON0	0xE020_0848	R/W	GPIO Interrupt GPF0_INT Filter Configuration Register 0	0x0
GPF0_INT_FLTCON1	0xE020_084C	R/W	GPIO Interrupt GPF0_INT Filter Configuration Register 1	0x0
GPF1_INT_FLTCON0	0xE020_0850	R/W	GPIO Interrupt GPF1_INT Filter Configuration Register 0	0x0
GPF1_INT_FLTCON1	0xE020_0854	R/W	GPIO Interrupt GPF1_INT Filter Configuration Register 1	0x0
GPF2_INT_FLTCON0	0xE020_0858	R/W	GPIO Interrupt GPF2_INT Filter Configuration Register 0	0x0
GPF2_INT_FLTCON1	0xE020_085C	R/W	GPIO Interrupt GPF2_INT Filter Configuration Register 1	0x0
GPF3_INT_FLTCON0	0xE020_0860	R/W	GPIO Interrupt GPF3_INT Filter Configuration Register 0	0x0
GPF3_INT_FLTCON1	0xE020_0864	R/W	GPIO Interrupt GPF3_INT Filter Configuration Register 1	0x0
GPG0_INT_FLTCON0	0xE020_0868	R/W	GPIO Interrupt GPG0_INT Filter Configuration Register 0	0x0
GPG0_INT_FLTCON1	0xE020_086C	R/W	GPIO Interrupt GPG0_INT Filter Configuration Register 1	0x0
GPG1_INT_FLTCON0	0xE020_0870	R/W	GPIO Interrupt GPG1_INT Filter	0x0

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Register	Address	R/W	Description	Reset Value
			Configuration Register 0	
GPG1_INT_FLTCON1	0xE020_0874	R/W	GPIO Interrupt GPG1_INT Filter Configuration Register 1	0x0
GPG2_INT_FLTCON0	0xE020_0878	R/W	GPIO Interrupt GPG2_INT Filter Configuration Register 0	0x0
GPG2_INT_FLTCON1	0xE020_087C	R/W	GPIO Interrupt GPG2_INT Filter Configuration Register 1	0x0
GPG3_INT_FLTCON0	0xE020_0880	R/W	GPIO Interrupt GPG3_INT Filter Configuration Register 0	0x0
GPG3_INT_FLTCON1	0xE020_0884	R/W	GPIO Interrupt GPG3_INT Filter Configuration Register 1	0x0
GPJ0_INT_FLTCON0	0xE020_0888	R/W	GPIO Interrupt GPJ0_INT Filter Configuration Register 0	0x0
GPJ0_INT_FLTCON1	0xE020_088C	R/W	GPIO Interrupt GPJ0_INT Filter Configuration Register 1	0x0
GPJ1_INT_FLTCON0	0xE020_0890	R/W	GPIO Interrupt GPJ1_INT Filter Configuration Register 0	0x0
GPJ1_INT_FLTCON1	0xE020_0894	R/W	GPIO Interrupt GPJ1_INT Filter Configuration Register 1	0x0
GPJ2_INT_FLTCON0	0xE020_0898	R/W	GPIO Interrupt GPJ2_INT Filter Configuration Register 0	0x0
GPJ2_INT_FLTCON1	0xE020_089C	R/W	GPIO Interrupt GPJ2_INT Filter Configuration Register 1	0x0
GPJ3_INT_FLTCON0	0xE020_08A0	R/W	GPIO Interrupt GPJ3_INT Filter Configuration Register 0	0x0
GPJ3_INT_FLTCON1	0xE020_08A4	R/W	GPIO Interrupt GPJ3_INT Filter Configuration Register 1	0x0
GPJ4_INT_FLTCON0	0xE020_08A8	R/W	GPIO Interrupt GPJ4_INT Filter Configuration Register 0	0x0
GPJ4_INT_FLTCON1	0xE020_08AC	R/W	GPIO Interrupt GPJ4_INT Filter Configuration Register 1	0x0
GPA0_INT_MASK	0xE020_0900	R/W	GPIO Interrupt GPA0_INT Mask Register	0x000000FF
GPA1_INT_MASK	0xE020_0904	R/W	GPIO Interrupt GPA1_INT Mask Register	0x0000000F
GPB_INT_MASK	0xE020_0908	R/W	GPIO Interrupt GPB_INT Mask Register	0x000000FF
GPC0_INT_MASK	0xE020_090C	R/W	GPIO Interrupt GPC0_INT Mask Register	0x0000001F
GPC1_INT_MASK	0xE020_0910	R/W	GPIO Interrupt GPC1_INT Mask Register	0x0000001F
GPD0_INT_MASK	0xE020_0914	R/W	GPIO Interrupt GPD0_INT Mask Register	0x0000000F
GPD1_INT_MASK	0xE020_0918	R/W	GPIO Interrupt GPD1_INT Mask Register	0x0000003F
GPE0_INT_MASK	0xE020_091C	R/W	GPIO Interrupt GPE0_INT Mask Register	0x000000FF
GPE1_INT_MASK	0xE020_0920	R/W	GPIO Interrupt GPE1_INT Mask Register	0x0000001F
GPF0_INT_MASK	0xE020_0924	R/W	GPIO Interrupt GPF0_INT Mask Register	0x000000FF

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Register	Address	R/W	Description	Reset Value
GPF1_INT_MASK	0xE020_0928	R/W	GPIO Interrupt GPF1_INT Mask Register	0x000000FF
GPF2_INT_MASK	0xE020_092C	R/W	GPIO Interrupt GPF2_INT Mask Register	0x000000FF
GPF3_INT_MASK	0xE020_0930	R/W	GPIO Interrupt GPF3_INT Mask Register	0x0000003F
GPG0_INT_MASK	0xE020_0934	R/W	GPIO Interrupt GPG0_INT Mask Register	0x0000007F
GPG1_INT_MASK	0xE020_0938	R/W	GPIO Interrupt GPG1_INT Mask Register	0x0000007F
GPG2_INT_MASK	0xE020_093C	R/W	GPIO Interrupt GPG2_INT Mask Register	0x0000007F
GPG3_INT_MASK	0xE020_0940	R/W	GPIO Interrupt GPG3_INT Mask Register	0x0000007F
GPJ0_INT_MASK	0xE020_0944	R/W	GPIO Interrupt GPJ0_INT Mask Register	0x000000FF
GPJ1_INT_MASK	0xE020_0948	R/W	GPIO Interrupt GPJ1_INT Mask Register	0x0000003F
GPJ2_INT_MASK	0xE020_094C	R/W	GPIO Interrupt GPJ2_INT Mask Register	0x000000FF
GPJ3_INT_MASK	0xE020_0950	R/W	GPIO Interrupt GPJ3_INT Mask Register	0x000000FF
GPJ4_INT_MASK	0xE020_0954	R/W	GPIO Interrupt GPJ4_INT Mask Register	0x0000001F
GPA0_INT_PEND	0xE020_0A00	R/W	GPIO Interrupt GPA0_INT Pending Register	0x0
GPA1_INT_PEND	0xE020_0A04	R/W	GPIO Interrupt GPA1_INT Pending Register	0x0
GPB_INT_PEND	0xE020_0A08	R/W	GPIO Interrupt GPB_INT Pending Register	0x0
GPC0_INT_PEND	0xE020_0A0C	R/W	GPIO Interrupt GPC0_INT Pending Register	0x0
GPC1_INT_PEND	0xE020_0A10	R/W	GPIO Interrupt GPC1_INT Pending Register	0x0
GPD0_INT_PEND	0xE020_0A14	R/W	GPIO Interrupt GPD0_INT Pending Register	0x0
GPD1_INT_PEND	0xE020_0A18	R/W	GPIO Interrupt GPD1_INT Pending Register	0x0
GPE0_INT_PEND	0xE020_0A1C	R/W	GPIO Interrupt GPE0_INT Pending Register	0x0
GPE1_INT_PEND	0xE020_0A20	R/W	GPIO Interrupt GPE1_INT Pending Register	0x0
GPF0_INT_PEND	0xE020_0A24	R/W	GPIO Interrupt GPF0_INT Pending Register	0x0
GPF1_INT_PEND	0xE020_0A28	R/W	GPIO Interrupt GPF1_INT Pending Register	0x0
GPF2_INT_PEND	0xE020_0A2C	R/W	GPIO Interrupt GPF2_INT Pending Register	0x0
GPF3_INT_PEND	0xE020_0A30	R/W	GPIO Interrupt GPF3_INT Pending Register	0x0
GPG0_INT_PEND	0xE020_0A34	R/W	GPIO Interrupt GPG0_INT Pending Register	0x0
GPG1_INT_PEND	0xE020_0A38	R/W	GPIO Interrupt GPG1_INT Pending	0x0

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Register	Address	R/W	Description	Reset Value
			Register	
GPG2_INT_PEND	0xE020_0A3C	R/W	GPIO Interrupt GPG2_INT Pending Register	0x0
GPG3_INT_PEND	0xE020_0A40	R/W	GPIO Interrupt GPG3_INT Pending Register	0x0
GPJ0_INT_PEND	0xE020_0A44	R/W	GPIO Interrupt GPJ0_INT Pending Register	0x0
GPJ1_INT_PEND	0xE020_0A48	R/W	GPIO Interrupt GPJ1_INT Pending Register	0x0
GPJ2_INT_PEND	0xE020_0A4C	R/W	GPIO Interrupt GPJ2_INT Pending Register	0x0
GPJ3_INT_PEND	0xE020_0A50	R/W	GPIO Interrupt GPJ3_INT Pending Register	0x0
GPJ4_INT_PEND	0xE020_0A54	R/W	GPIO Interrupt GPJ4_INT Pending Register	0x0
GPIO_INT_GRPPRI	0xE020_0B00	R/W	GPIO Interrupt Group Priority Control Register	0x0
GPIO_INT_PRIORITY	0xE020_0B04	R/W	GPIO Interrupt Priority Control Register	0x00
GPIO_INT_SERVICE	0xE020_0B08	R	Current Service Register	0x00
GPIO_INT_SERVICE_PEND	0xE020_0B0C	R	Current Service Pending Register	0x00
GPIO_INT_GRPFIXPRI	0xE020_0B10	R/W	GPIO Interrupt Group Fixed Priority Control Register	0x00
GPA0_INT_FIXPRI	0xE020_0B14	R/W	GPIO Interrupt 1 Fixed Priority Control Register	0x00
GPA1_INT_FIXPRI	0xE020_0B18	R/W	GPIO Interrupt 2 Fixed Priority Control Register	0x00
GPB_INT_FIXPRI	0xE020_0B1C	R/W	GPIO Interrupt 3 Fixed Priority Control Register	0x00
GPC0_INT_FIXPRI	0xE020_0B20	R/W	GPIO Interrupt 4 Fixed Priority Control Register	0x00
GPC1_INT_FIXPRI	0xE020_0B24	R/W	GPIO Interrupt 5 Fixed Priority Control Register	0x00
GPD0_INT_FIXPRI	0xE020_0B28	R/W	GPIO Interrupt 6 Fixed Priority Control Register	0x00
GPD1_INT_FIXPRI	0xE020_0B2C	R/W	GPIO Interrupt 7 Fixed Priority Control Register	0x00
GPE0_INT_FIXPRI	0xE020_0B30	R/W	GPIO Interrupt 8 Fixed Priority Control Register	0x00
GPE1_INT_FIXPRI	0xE020_0B34	R/W	GPIO Interrupt 9 Fixed Priority Control Register	0x00
GPF0_INT_FIXPRI	0xE020_0B38	R/W	GPIO Interrupt 10 Fixed Priority Control	0x00

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Register	Address	R/W	Description	Reset Value
			Register	
GPF1_INT_FIXPRI	0xE020_0B3C	R/W	GPIO Interrupt 11 Fixed Priority Control Register	0x00
GPF2_INT_FIXPRI	0xE020_0B40	R/W	GPIO Interrupt 12 Fixed Priority Control Register	0x00
GPF3_INT_FIXPRI	0xE020_0B44	R/W	GPIO Interrupt 13 Fixed Priority Control Register	0x00
GPG0_INT_FIXPRI	0xE020_0B48	R/W	GPIO Interrupt 14 Fixed Priority Control Register	0x00
GPG1_INT_FIXPRI	0xE020_0B4C	R/W	GPIO Interrupt 15 Fixed Priority Control Register	0x00
GPG2_INT_FIXPRI	0xE020_0B50	R/W	GPIO Interrupt 16 Fixed Priority Control Register	0x00
GPG3_INT_FIXPRI	0xE020_0B54	R/W	GPIO Interrupt 17 Fixed Priority Control Register	0x00
GPJ0_INT_FIXPRI	0xE020_0B58	R/W	GPIO Interrupt 18 Fixed Priority Control Register	0x00
GPJ1_INT_FIXPRI	0xE020_0B5C	R/W	GPIO Interrupt 19 Fixed Priority Control Register	0x00
GPJ2_INT_FIXPRI	0xE020_0B60	R/W	GPIO Interrupt 20 Fixed Priority Control Register	0x00
GPJ3_INT_FIXPRI	0xE020_0B64	R/W	GPIO Interrupt 21 Fixed Priority Control Register	0x00
GPJ4_INT_FIXPRI	0xE020_0B68	R/W	GPIO Interrupt 22 Fixed Priority Control Register	0x00

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2.2.55.1 GPIO Interrupt Control Registers (GPA0_INT_CON, R/W, Address = 0xE020_0700)

GPA0_INT_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
GPA0_INT_CON[7]	[30:28]	Sets the signaling method of GPA0_INT[7] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
GPA0_INT_CON[6]	[26:24]	Sets the signaling method of GPA0_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
GPA0_INT_CON[5]	[22:20]	Sets the signaling method of GPA0_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPA0_INT_CON[4]	[18:16]	Sets the signaling method of GPA0_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPA0_INT_CON[3]	[14:12]	Sets the signaling method of GPA0_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPA0_INT_CON[2]	[10:8]	Sets the signaling method of GPA0_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered	000

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GPA0_INT_CON	Bit	Description	Initial State
		100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[7]	Reserved	0
GPA0_INT_CON[1]	[6:4]	Sets the signaling method of GPA0_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPA0_INT_CON[0]	[2:0]	Sets the signaling method of GPA0_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.2 GPIO Interrupt Control Registers (GPA1_INT_CON, R/W, Address = 0xE020_0704)

GPA1_INT_CON	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
Reserved	[15]	Reserved	0
GPA1_INT_CON[3]	[14:12]	Sets the signaling method of GPA1_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPA1_INT_CON[2]	[10:8]	Sets the signaling method of GPA1_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
GPA1_INT_CON[1]	[6:4]	Sets the signaling method of GPA1_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPA1_INT_CON[0]	[2:0]	Sets the signaling method of GPA1_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.3 GPIO Interrupt Control Registers (GPB_INT_CON, R/W, Address = 0xE020_0708)

GPB_INT_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
GPB_INT_CON[7]	[30:28]	Sets the signaling method of GPB_INT[7] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
GPB_INT_CON[6]	[26:24]	Sets the signaling method of GPB_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
GPB_INT_CON[5]	[22:20]	Sets the signaling method of GPB_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPB_INT_CON[4]	[18:16]	Sets the signaling method of GPB_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPB_INT_CON[3]	[14:12]	Sets the signaling method of GPB_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPB_INT_CON[2]	[10:8]	Sets the signaling method of GPB_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered	000

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GPB_INT_CON	Bit	Description	Initial State
		100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[7]	Reserved	0
GPB_INT_CON[1]	[6:4]	Sets the signaling method of GPB_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPB_INT_CON[0]	[2:0]	Sets the signaling method of GPB_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.4 GPIO Interrupt Control Registers (GPC0_INT_CON, R/W, Address = 0xE020_070C)

GPC0_INT_CON	Bit	Description	Initial State
Reserved	[31:20]	Reserved	0
Reserved	[19]	Reserved	0
GPC0_INT_CON[4]	[18:16]	Sets the signaling method of GPC0_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPC0_INT_CON[3]	[14:12]	Sets the signaling method of GPC0_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPC0_INT_CON[2]	[10:8]	Sets the signaling method of GPC0_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
GPC0_INT_CON[1]	[6:4]	Sets the signaling method of GPC0_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPC0_INT_CON[0]	[2:0]	Sets the signaling method of GPC0_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.5 GPIO Interrupt Control Registers (GPC1_INT_CON, R/W, Address = 0xE020_0710)

GPC1_INT_CON	Bit	Description	Initial State
Reserved	[31:20]	Reserved	0
Reserved	[19]	Reserved	0
GPC1_INT_CON[4]	[18:16]	Sets the signaling method of GPC1_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPC1_INT_CON[3]	[14:12]	Sets the signaling method of GPC1_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPC1_INT_CON[2]	[10:8]	Sets the signaling method of GPC1_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
GPC1_INT_CON[1]	[6:4]	Sets the signaling method of GPC1_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPC1_INT_CON[0]	[2:0]	Sets the signaling method of GPC1_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.6 GPIO Interrupt Control Registers (GPD0_INT_CON, R/W, Address = 0xE020_0714)

GPD0_INT_CON	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
Reserved	[15]	Reserved	0
GPD0_INT_CON[3]	[14:12]	Sets the signaling method of GPD0_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPD0_INT_CON[2]	[10:8]	Sets the signaling method of GPD0_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
GPD0_INT_CON[1]	[6:4]	Sets the signaling method of GPD0_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPD0_INT_CON[0]	[2:0]	Sets the signaling method of GPD0_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.7 GPIO Interrupt Control Registers (GPD1_INT_CON, R/W, Address = 0xE020_0718)

GPD1_INT_CON	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
Reserved	[23]	Reserved	0
GPD1_INT_CON[5]	[22:20]	Sets the signaling method of GPD1_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPD1_INT_CON[4]	[18:16]	Sets the signaling method of GPD1_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPD1_INT_CON[3]	[14:12]	Sets the signaling method of GPD1_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPD1_INT_CON[2]	[10:8]	Sets the signaling method of GPD1_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
GPD1_INT_CON[1]	[6:4]	Sets the signaling method of GPD1_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPD1_INT_CON[0]	[2:0]	Sets the signaling method of GPD1_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.8 GPIO Interrupt Control Registers (GPE0_INT_CON, R/W, Address = 0xE020_071C)

GPE0_INT_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
GPE0_INT_CON[7]	[30:28]	Sets the signaling method of GPE0_INT[7] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
GPE0_INT_CON[6]	[26:24]	Sets the signaling method of GPE0_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
GPE0_INT_CON[5]	[22:20]	Sets the signaling method of GPE0_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPE0_INT_CON[4]	[18:16]	Sets the signaling method of GPE0_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPE0_INT_CON[3]	[14:12]	Sets the signaling method of GPE0_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPE0_INT_CON[2]	[10:8]	Sets the signaling method of GPE0_INT[2] 000 = Low level 001 = High level	000

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GPE0_INT_CON	Bit	Description	Initial State
		010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[7]	Reserved	0
GPE0_INT_CON[1]	[6:4]	Sets the signaling method of GPE0_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPE0_INT_CON[0]	[2:0]	Sets the signaling method of GPE0_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.9 GPIO Interrupt Control Registers (GPE1_INT_CON, R/W, Address = 0xE020_0720)

GPE1_INT_CON	Bit	Description	Initial State
Reserved	[31:20]	Reserved	0
Reserved	[19]	Reserved	0
GPE1_INT_CON[4]	[18:16]	Sets the signaling method of GPE1_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPE1_INT_CON[3]	[14:12]	Sets the signaling method of GPE1_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPE1_INT_CON[2]	[10:8]	Sets the signaling method of GPE1_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
GPE1_INT_CON[1]	[6:4]	Sets the signaling method of GPE1_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPE1_INT_CON[0]	[2:0]	Sets the signaling method of GPE1_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.10 GPIO Interrupt Control Registers (GPF0_INT_CON, R/W, Address = 0xE020_0724)

GPF0_INT_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
GPF0_INT_CON[7]	[30:28]	Sets the signaling method of GPF0_INT[7] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
GPF0_INT_CON[6]	[26:24]	Sets the signaling method of GPF0_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
GPF0_INT_CON[5]	[22:20]	Sets the signaling method of GPF0_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPF0_INT_CON[4]	[18:16]	Sets the signaling method of GPF0_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPF0_INT_CON[3]	[14:12]	Sets the signaling method of GPF0_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPF0_INT_CON[2]	[10:8]	Sets the signaling method of GPF0_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered	000

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GPF0_INT_CON	Bit	Description	Initial State
		100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[7]	Reserved	0
GPF0_INT_CON[1]	[6:4]	Sets the signaling method of GPF0_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPF0_INT_CON[0]	[2:0]	Sets the signaling method of GPF0_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.11 GPIO Interrupt Control Registers (GPF1_INT_CON, R/W, Address = 0xE020_0728)

GPF1_INT_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
GPF1_INT_CON[7]	[30:28]	Sets the signaling method of GPF1_INT[7] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
GPF1_INT_CON[6]	[26:24]	Sets the signaling method of GPF1_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
GPF1_INT_CON[5]	[22:20]	Sets the signaling method of GPF1_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPF1_INT_CON[4]	[18:16]	Sets the signaling method of GPF1_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPF1_INT_CON[3]	[14:12]	Sets the signaling method of GPF1_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPF1_INT_CON[2]	[10:8]	Sets the signaling method of GPF1_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered	000

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GPF1_INT_CON	Bit	Description	Initial State
		100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[7]	Reserved	0
GPF1_INT_CON[1]	[6:4]	Sets the signaling method of GPF1_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPF1_INT_CON[0]	[2:0]	Sets the signaling method of GPF1_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.12 GPIO Interrupt Control Registers (GPF2_INT_CON, R/W, Address = 0xE020_072C)

GPF2_INT_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
GPF2_INT_CON[7]	[30:28]	Sets the signaling method of GPF2_INT[7] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
GPF2_INT_CON[6]	[26:24]	Sets the signaling method of GPF2_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
GPF2_INT_CON[5]	[22:20]	Sets the signaling method of GPF2_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPF2_INT_CON[4]	[18:16]	Sets the signaling method of GPF2_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPF2_INT_CON[3]	[14:12]	Sets the signaling method of GPF2_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPF2_INT_CON[2]	[10:8]	Sets the signaling method of GPF2_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered	000

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GPF2_INT_CON	Bit	Description	Initial State
		100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[7]	Reserved	0
GPF2_INT_CON[1]	[6:4]	Sets the signaling method of GPF2_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPF2_INT_CON[0]	[2:0]	Sets the signaling method of GPF2_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.13 GPIO Interrupt Control Registers (GPF3_INT_CON, R/W, Address = 0xE020_0730)

GPF3_INT_CON	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
Reserved	[23]	Reserved	0
GPF3_INT_CON[5]	[22:20]	Sets the signaling method of GPF3_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPF3_INT_CON[4]	[18:16]	Sets the signaling method of GPF3_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPF3_INT_CON[3]	[14:12]	Sets the signaling method of GPF3_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPF3_INT_CON[2]	[10:8]	Sets the signaling method of GPF3_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
GPF3_INT_CON[1]	[6:4]	Sets the signaling method of GPF3_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPF3_INT_CON[0]	[2:0]	Sets the signaling method of GPF3_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.14 GPIO Interrupt Control Registers (GPG0_INT_CON, R/W, Address = 0xE020_0734)

GPG0_INT_CON	Bit	Description	Initial State
Reserved	[31:28]	Reserved	0
Reserved	[27]	Reserved	0
GPG0_INT_CON[6]	[26:24]	Sets the signaling method of GPG0_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
GPG0_INT_CON[5]	[22:20]	Sets the signaling method of GPG0_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPG0_INT_CON[4]	[18:16]	Sets the signaling method of GPG0_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPG0_INT_CON[3]	[14:12]	Sets the signaling method of GPG0_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPG0_INT_CON[2]	[10:8]	Sets the signaling method of GPG0_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
GPG0_INT_CON[1]	[6:4]	Sets the signaling method of GPG0_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered	000

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GPG0_INT_CON	Bit	Description	Initial State
		011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[3]	Reserved	0
GPG0_INT_CON[0]	[2:0]	Sets the signaling method of GPG0_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.15 GPIO Interrupt Control Registers (GPG1_INT_CON, R/W, Address = 0xE020_0738)

GPG1_INT_CON	Bit	Description	Initial State
Reserved	[31:28]	Reserved	0
Reserved	[27]	Reserved	0
GPG1_INT_CON[6]	[26:24]	Sets the signaling method of GPG1_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
GPG1_INT_CON[5]	[22:20]	Sets the signaling method of GPG1_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPG1_INT_CON[4]	[18:16]	Sets the signaling method of GPG1_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPG1_INT_CON[3]	[14:12]	Sets the signaling method of GPG1_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPG1_INT_CON[2]	[10:8]	Sets the signaling method of GPG1_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
GPG1_INT_CON[1]	[6:4]	Sets the signaling method of GPG1_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered	000

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GPG1_INT_CON	Bit	Description	Initial State
		011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[3]	Reserved	0
GPG1_INT_CON[0]	[2:0]	Sets the signaling method of GPG1_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.16 GPIO Interrupt Control Registers (GPG2_INT_CON, R/W, Address = 0xE020_073C)

GPG2_INT_CON	Bit	Description	Initial State
Reserved	[31:28]	Reserved	0
Reserved	[27]	Reserved	0
GPG2_INT_CON[6]	[26:24]	Sets the signaling method of GPG2_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
GPG2_INT_CON[5]	[22:20]	Sets the signaling method of GPG2_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPG2_INT_CON[4]	[18:16]	Sets the signaling method of GPG2_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPG2_INT_CON[3]	[14:12]	Sets the signaling method of GPG2_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPG2_INT_CON[2]	[10:8]	Sets the signaling method of GPG2_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
GPG2_INT_CON[1]	[6:4]	Sets the signaling method of GPG2_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered	000

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GPG2_INT_CON	Bit	Description	Initial State
		011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[3]	Reserved	0
GPG2_INT_CON[0]	[2:0]	Sets the signaling method of GPG2_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.17 GPIO Interrupt Control Registers (GPG3_INT_CON, R/W, Address = 0xE020_0740)

GPG3_INT_CON	Bit	Description	Initial State
Reserved	[31:28]	Reserved	0
Reserved	[27]	Reserved	0
GPG3_INT_CON[6]	[26:24]	Sets the signaling method of GPG3_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
GPG3_INT_CON[5]	[22:20]	Sets the signaling method of GPG3_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPG3_INT_CON[4]	[18:16]	Sets the signaling method of GPG3_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPG3_INT_CON[3]	[14:12]	Sets the signaling method of GPG3_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPG3_INT_CON[2]	[10:8]	Sets the signaling method of GPG3_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
GPG3_INT_CON[1]	[6:4]	Sets the signaling method of GPG3_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered	000

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GPG3_INT_CON	Bit	Description	Initial State
		011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[3]	Reserved	0
GPG3_INT_CON[0]	[2:0]	Sets the signaling method of GPG3_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.18 GPIO Interrupt Control Registers (GPJ0_INT_CON, R/W, Address = 0xE020_0744)

GPJ0_INT_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
GPJ0_INT_CON[7]	[30:28]	Sets the signaling method of GPJ0_INT[7] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
GPJ0_INT_CON[6]	[26:24]	Sets the signaling method of GPJ0_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
GPJ0_INT_CON[5]	[22:20]	Sets the signaling method of GPJ0_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPJ0_INT_CON[4]	[18:16]	Sets the signaling method of GPJ0_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPJ0_INT_CON[3]	[14:12]	Sets the signaling method of GPJ0_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPJ0_INT_CON[2]	[10:8]	Sets the signaling method of GPJ0_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered	000

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GPJ0_INT_CON	Bit	Description	Initial State
		100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[7]	Reserved	0
GPJ0_INT_CON[1]	[6:4]	Sets the signaling method of GPJ0_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPJ0_INT_CON[0]	[2:0]	Sets the signaling method of GPJ0_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.19 GPIO Interrupt Control Registers (GPJ1_INT_CON, R/W, Address = 0xE020_0748)

GPJ1_INT_CON	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
Reserved	[23]	Reserved	0
GPJ1_INT_CON[5]	[22:20]	Sets the signaling method of GPJ1_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPJ1_INT_CON[4]	[18:16]	Sets the signaling method of GPJ1_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPJ1_INT_CON[3]	[14:12]	Sets the signaling method of GPJ1_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPJ1_INT_CON[2]	[10:8]	Sets the signaling method of GPJ1_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
GPJ1_INT_CON[1]	[6:4]	Sets the signaling method of GPJ1_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPJ1_INT_CON[0]	[2:0]	Sets the signaling method of GPJ1_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.20 GPIO Interrupt Control Registers (GPJ2_INT_CON, R/W, Address = 0xE020_074C)

GPJ2_INT_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
GPJ2_INT_CON[7]	[30:28]	Sets the signaling method of GPJ2_INT[7] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
GPJ2_INT_CON[6]	[26:24]	Sets the signaling method of GPJ2_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
GPJ2_INT_CON[5]	[22:20]	Sets the signaling method of GPJ2_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPJ2_INT_CON[4]	[18:16]	Sets the signaling method of GPJ2_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPJ2_INT_CON[3]	[14:12]	Sets the signaling method of GPJ2_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPJ2_INT_CON[2]	[10:8]	Sets the signaling method of GPJ2_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered	000

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GPJ2_INT_CON	Bit	Description	Initial State
		100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[7]	Reserved	0
GPJ2_INT_CON[1]	[6:4]	Sets the signaling method of GPJ2_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPJ2_INT_CON[0]	[2:0]	Sets the signaling method of GPJ2_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.21 GPIO Interrupt Control Registers (GPJ3_INT_CON, R/W, Address = 0xE020_0750)

GPJ3_INT_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
GPJ3_INT_CON[7]	[30:28]	Sets the signaling method of GPJ3_INT[7] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
GPJ3_INT_CON[6]	[26:24]	Sets the signaling method of GPJ3_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
GPJ3_INT_CON[5]	[22:20]	Sets the signaling method of GPJ3_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
GPJ3_INT_CON[4]	[18:16]	Sets the signaling method of GPJ3_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPJ3_INT_CON[3]	[14:12]	Sets the signaling method of GPJ3_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPJ3_INT_CON[2]	[10:8]	Sets the signaling method of GPJ3_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered	000

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GPJ3_INT_CON	Bit	Description	Initial State
		100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[7]	Reserved	0
GPJ3_INT_CON[1]	[6:4]	Sets the signaling method of GPJ3_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPJ3_INT_CON[0]	[2:0]	Sets the signaling method of GPJ3_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.22 GPIO Interrupt Control Registers (GPJ4_INT_CON, R/W, Address = 0xE020_0754)

GPJ4_INT_CON	Bit	Description	Initial State
Reserved	[31:20]	Reserved	0
Reserved	[19]	Reserved	0
GPJ4_INT_CON[4]	[18:16]	Sets the signaling method of GPJ4_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
GPJ4_INT_CON[3]	[14:12]	Sets the signaling method of GPJ4_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
GPJ4_INT_CON[2]	[10:8]	Sets the signaling method of GPJ4_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
GPJ4_INT_CON[1]	[6:4]	Sets the signaling method of GPJ4_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
GPJ4_INT_CON[0]	[2:0]	Sets the signaling method of GPJ4_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.55.23 GPIO Interrupt Control Registers (GPA0_INT_FLTCON0, R/W, Address = 0xE020_0800)

GPA0_INT_FLTCON0	Bit	Description	Initial State
FLTEN1[3]	[31]	Filter Enable for GPA0_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH1[3]	[30:24]	Filtering width of GPA0_INT[3] This value is valid when FLTSEL1is 1.	0
FLTEN1[2]	[23]	Filter Enable for GPA0_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH1[2]	[22:16]	Filtering width of GPA0_INT[2] This value is valid when FLTSEL1is 1.	0
FLTEN1[1]	[15]	Filter Enable for GPA0_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH1[1]	[14:8]	Filtering width of GPA0_INT[1] This value is valid when FLTSEL1is 1.	0
FLTEN1[0]	[7]	Filter Enable for GPA0_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH1[0]	[6:0]	Filtering width of GPA0_INT[0] This value is valid when FLTSEL1is 1.	0

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2.2.55.24 GPIO Interrupt Control Registers (GPA0_INT_FLTCON1, R/W, Address = 0xE020_0804)

GPA0_INT_FLTCON1	Bit	Description	Initial State
FLTEN1[7]	[31]	Filter Enable for GPA0_INT[7] 0 = Disables 1 = Enables	0
FLTWIDTH1[7]	[30:24]	Filtering width of GPA0_INT[7] This value is valid when FLTSEL1is 1.	0
FLTEN1[6]	[23]	Filter Enable for GPA0_INT[6] 0 = Disables 1 = Enables	0
FLTWIDTH1[6]	[22:16]	Filtering width of GPA0_INT[6] This value is valid when FLTSEL1is 1.	0
FLTEN1[5]	[15]	Filter Enable for GPA0_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH1[5]	[14:8]	Filtering width of GPA0_INT[5] This value is valid when FLTSEL1is 1.	0
FLTEN1[4]	[7]	Filter Enable for GPA0_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH1[4]	[6:0]	Filtering width of GPA0_INT[4] This value is valid when FLTSEL1is 1.	0

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2.2.55.25 GPIO Interrupt Control Registers (GPA1_INT_FLTCON0, R/W, Address = 0xE020_0808)

GPA1_INT_FLTCON0	Bit	Description	Initial State
FLTEN2[3]	[31]	Filter Enable for GPA1_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH2[3]	[30:24]	Filtering width of GPA1_INT[3] This value is valid when FLTSEL2is 1.	0
FLTEN2[2]	[23]	Filter Enable for GPA1_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH2[2]	[22:16]	Filtering width of GPA1_INT[2] This value is valid when FLTSEL2is 1.	0
FLTEN2[1]	[15]	Filter Enable for GPA1_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH2[1]	[14:8]	Filtering width of GPA1_INT[1] This value is valid when FLTSEL2is 1.	0
FLTEN2[0]	[7]	Filter Enable for GPA1_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH2[0]	[6:0]	Filtering width of GPA1_INT[0] This value is valid when FLTSEL2is 1.	0

2.2.55.26 GPIO Interrupt Control Registers (GPA1_INT_FLTCON1, R/W, Address = 0xE020_080C)

GPA1_INT_FLTCON1	Bit	Description	Initial State
Reserved	[31:0]	Reserved	0

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2.2.55.27 GPIO Interrupt Control Registers (GPB_INT_FLTCON0, R/W, Address = 0xE020_0810)

GPB_INT_FLTCON0	Bit	Description	Initial State
FLTEN3[3]	[31]	Filter Enable for GPB_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH3[3]	[30:24]	Filtering width of GPB_INT[3] This value is valid when FLTSEL3 is 1.	0
FLTEN3[2]	[23]	Filter Enable for GPB_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH3[2]	[22:16]	Filtering width of GPB_INT[2] This value is valid when FLTSEL3 is 1.	0
FLTEN3[1]	[15]	Filter Enable for GPB_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH3[1]	[14:8]	Filtering width of GPB_INT[1] This value is valid when FLTSEL3 is 1.	0
FLTEN3[0]	[7]	Filter Enable for GPB_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH3[0]	[6:0]	Filtering width of GPB_INT[0] This value is valid when FLTSEL3 is 1.	0

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2.2.55.28 GPIO Interrupt Control Registers (GPB_INT_FLTCON1, R/W, Address = 0xE020_0814)

GPB_INT_FLTCON1	Bit	Description	Initial State
FLTEN3[7]	[31]	Filter Enable for GPB_INT[7] 0 = Disables 1 = Enables	0
FLTWIDTH3[7]	[30:24]	Filtering width of GPB_INT[7] This value is valid when FLTSEL3 is 1.	0
FLTEN3[6]	[23]	Filter Enable for GPB_INT[6] 0 = Disables 1 = Enables	0
FLTWIDTH3[6]	[22:16]	Filtering width of GPB_INT[6] This value is valid when FLTSEL3 is 1.	0
FLTEN3[5]	[15]	Filter Enable for GPB_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH3[5]	[14:8]	Filtering width of GPB_INT[5] This value is valid when FLTSEL3 is 1.	0
FLTEN3[4]	[7]	Filter Enable for GPB_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH3[4]	[6:0]	Filtering width of GPB_INT[4] This value is valid when FLTSEL3 is 1.	0

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2.2.55.29 GPIO Interrupt Control Registers (GPC0_INT_FLTCON0, R/W, Address = 0xE020_0818)

GPC0_INT_FLTCON0	Bit	Description	Initial State
FLTEN4[3]	[31]	Filter Enable for GPC0_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH4[3]	[30:24]	Filtering width of GPC0_INT[3] This value is valid when FLTSEL4 is 1.	0
FLTEN4[2]	[23]	Filter Enable for GPC0_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH4[2]	[22:16]	Filtering width of GPC0_INT[2] This value is valid when FLTSEL4 is 1.	0
FLTEN4[1]	[15]	Filter Enable for GPC0_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH4[1]	[14:8]	Filtering width of GPC0_INT[1] This value is valid when FLTSEL4 is 1.	0
FLTEN4[0]	[7]	Filter Enable for GPC0_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH4[0]	[6:0]	Filtering width of GPC0_INT[0] This value is valid when FLTSEL4 is 1.	0

2.2.55.30 GPIO Interrupt Control Registers (GPC0_INT_FLTCON1, R/W, Address = 0xE020_081C)

GPC0_INT_FLTCON1	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
FLTEN4[4]	[7]	Filter Enable for GPC0_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH4[4]	[6:0]	Filtering width of GPC0_INT[4] This value is valid when FLTSEL4 is 1.	0

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2.2.55.31 GPIO Interrupt Control Registers (GPC1_INT_FLTCON0, R/W, Address = 0xE020_0820)

GPC1_INT_FLTCON0	Bit	Description	Initial State
FLTEN5[3]	[31]	Filter Enable for GPC1_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH5[3]	[30:24]	Filtering width of GPC1_INT[3] This value is valid when FLTSEL5 is 1.	0
FLTEN5[2]	[23]	Filter Enable for GPC1_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH5[2]	[22:16]	Filtering width of GPC1_INT[2] This value is valid when FLTSEL5 is 1.	0
FLTEN5[1]	[15]	Filter Enable for GPC1_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH5[1]	[14:8]	Filtering width of GPC1_INT[1] This value is valid when FLTSEL5 is 1.	0
FLTEN5[0]	[7]	Filter Enable for GPC1_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH5[0]	[6:0]	Filtering width of GPC1_INT[0] This value is valid when FLTSEL5 is 1.	0

2.2.55.32 GPIO Interrupt Control Registers (GPC1_INT_FLTCON1, R/W, Address = 0xE020_0824)

GPC1_INT_FLTCON1	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
FLTEN5[4]	[7]	Filter Enable for GPC1_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH5[4]	[6:0]	Filtering width of GPC1_INT[4] This value is valid when FLTSEL5 is 1.	0

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2.2.55.33 GPIO Interrupt Control Registers (GPD0_INT_FLTCON0, R/W, Address = 0xE020_0828)

GPD0_INT_FLTCON0	Bit	Description	Initial State
FLTEN6[3]	[31]	Filter Enable for GPD0_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH6[3]	[30:24]	Filtering width of GPD0_INT[3] This value is valid when FLTSEL6 is 1.	0
FLTEN6[2]	[23]	Filter Enable for GPD0_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH6[2]	[22:16]	Filtering width of GPD0_INT[2] This value is valid when FLTSEL6 is 1.	0
FLTEN6[1]	[15]	Filter Enable for GPD0_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH6[1]	[14:8]	Filtering width of GPD0_INT[1] This value is valid when FLTSEL6 is 1.	0
FLTEN6[0]	[7]	Filter Enable for GPD0_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH6[0]	[6:0]	Filtering width of GPD0_INT[0] This value is valid when FLTSEL6 is 1.	0

2.2.55.34 GPIO Interrupt Control Registers (GPD0_INT_FLTCON1, R/W, Address = 0xE020_082C)

GPD0_INT_FLTCON1	Bit	Description	Initial State
Reserved	[31:0]	Reserved	0

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2.2.55.35 GPIO Interrupt Control Registers (GPD1_INT_FLTCON0, R/W, Address = 0xE020_0830)

GPD1_INT_FLTCON0	Bit	Description	Initial State
FLTEN7[3]	[31]	Filter Enable for GPD1_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH7[3]	[30:24]	Filtering width of GPD1_INT[3] This value is valid when FLTSEL7 is 1.	0
FLTEN7[2]	[23]	Filter Enable for GPD1_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH7[2]	[22:16]	Filtering width of GPD1_INT[2] This value is valid when FLTSEL7 is 1.	0
FLTEN7[1]	[15]	Filter Enable for GPD1_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH7[1]	[14:8]	Filtering width of GPD1_INT[1] This value is valid when FLTSEL7 is 1.	0
FLTEN7[0]	[7]	Filter Enable for GPD1_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH7[0]	[6:0]	Filtering width of GPD1_INT[0] This value is valid when FLTSEL7 is 1.	0

2.2.55.36 GPIO Interrupt Control Registers (GPD1_INT_FLTCON1, R/W, Address = 0xE020_0834)

GPD1_INT_FLTCON1	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
FLTEN7[5]	[15]	Filter Enable for GPD1_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH7[5]	[14:8]	Filtering width of GPD1_INT[5] This value is valid when FLTSEL7is 1.	0
FLTEN7[4]	[7]	Filter Enable for GPD1_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH7[4]	[6:0]	Filtering width of GPD1_INT[4] This value is valid when FLTSEL7 is 1.	0

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2.2.55.37 GPIO Interrupt Control Registers (GPE0_INT_FLTCON0, R/W, Address = 0xE020_0838)

GPE0_INT_FLTCON0	Bit	Description	Initial State
FLTEN8[3]	[31]	Filter Enable for GPE0_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH8[3]	[30:24]	Filtering width of GPE0_INT[3] This value is valid when FLTSEL8 is 1.	0
FLTEN8[2]	[23]	Filter Enable for GPE0_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH8[2]	[22:16]	Filtering width of GPE0_INT[2] This value is valid when FLTSEL8 is 1.	0
FLTEN8[1]	[15]	Filter Enable for GPE0_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH8[1]	[14:8]	Filtering width of GPE0_INT[1] This value is valid when FLTSEL8 is 1.	0
FLTEN8[0]	[7]	Filter Enable for GPE0_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH8[0]	[6:0]	Filtering width of GPE0_INT[0] This value is valid when FLTSEL8 is 1.	0

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2.2.55.38 GPIO Interrupt Control Registers (GPE0_INT_FLTCON1, R/W, Address = 0xE020_083C)

GPE0_INT_FLTCON1	Bit	Description	Initial State
FLTEN8[7]	[31]	Filter Enable for GPE0_INT[7] 0 = Disables 1 = Enables	0
FLTWIDTH8[7]	[30:24]	Filtering width of GPE0_INT[7] This value is valid when FLTSEL8 is 1.	0
FLTEN8[6]	[23]	Filter Enable for GPE0_INT[6] 0 = Disables 1 = Enables	0
FLTWIDTH8[6]	[22:16]	Filtering width of GPE0_INT[6] This value is valid when FLTSEL8 is 1.	0
FLTEN8[5]	[15]	Filter Enable for GPE0_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH8[5]	[14:8]	Filtering width of GPE0_INT[5] This value is valid when FLTSEL8is 1.	0
FLTEN8[4]	[7]	Filter Enable for GPE0_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH8[4]	[6:0]	Filtering width of GPE0_INT[4] This value is valid when FLTSEL8 is 1.	0

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2.2.55.39 GPIO Interrupt Control Registers (GPE1_INT_FLTCON0, R/W, Address = 0xE020_0840)

GPE1_INT_FLTCON0	Bit	Description	Initial State
FLTEN9[3]	[31]	Filter Enable for GPE1_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH9[3]	[30:24]	Filtering width of GPE1_INT[3] This value is valid when FLTSEL9 is 1.	0
FLTEN9[2]	[23]	Filter Enable for GPE1_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH9[2]	[22:16]	Filtering width of GPE1_INT[2] This value is valid when FLTSEL9 is 1.	0
FLTEN9[1]	[15]	Filter Enable for GPE1_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH9[1]	[14:8]	Filtering width of GPE1_INT[1] This value is valid when FLTSEL9 is 1.	0
FLTEN9[0]	[7]	Filter Enable for GPE1_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH9[0]	[6:0]	Filtering width of GPE1_INT[0] This value is valid when FLTSEL9 is 1.	0

2.2.55.40 GPIO Interrupt Control Registers (GPE1_INT_FLTCON1, R/W, Address = 0xE020_0844)

GPE1_INT_FLTCON1	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
FLTEN9[4]	[7]	Filter Enable for GPE1_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH9[4]	[6:0]	Filtering width of GPE1_INT[4] This value is valid when FLTSEL9 is 1.	0

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2.2.55.41 GPIO Interrupt Control Registers (GPF0_INT_FLTCON0, R/W, Address = 0xE020_0848)

GPF0_INT_FLTCON0	Bit	Description	Initial State
FLTEN10[3]	[31]	Filter Enable for GPF0_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH10[3]	[30:24]	Filtering width of GPF0_INT[3] This value is valid when FLTSEL10 is 1.	0
FLTEN10[2]	[23]	Filter Enable for GPF0_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH10[2]	[22:16]	Filtering width of GPF0_INT[2] This value is valid when FLTSEL10 is 1.	0
FLTEN10[1]	[15]	Filter Enable for GPF0_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH10[1]	[14:8]	Filtering width of GPF0_INT[1] This value is valid when FLTSEL10 is 1.	0
FLTEN10[0]	[7]	Filter Enable for GPF0_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH10[0]	[6:0]	Filtering width of GPF0_INT[0] This value is valid when FLTSEL10 is 1.	0

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2.2.55.42 GPIO Interrupt Control Registers (GPF0_INT_FLTCON1, R/W, Address = 0xE020_084C)

GPF0_INT_FLTCON1	Bit	Description	Initial State
FLTEN10[7]	[31]	Filter Enable for GPF0_INT[7] 0 = Disables 1 = Enables	0
FLTWIDTH10[7]	[30:24]	Filtering width of GPF0_INT[7] This value is valid when FLTSEL10 is 1.	0
FLTEN10[6]	[23]	Filter Enable for GPF0_INT[6] 0 = Disables 1 = Enables	0
FLTWIDTH10[6]	[22:16]	Filtering width of GPF0_INT[6] This value is valid when FLTSEL10 is 1.	0
FLTEN10[5]	[15]	Filter Enable for GPF0_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH10[5]	[14:8]	Filtering width of GPF0_INT[5] This value is valid when FLTSEL10 is 1.	0
FLTEN10[4]	[7]	Filter Enable for GPF0_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH10[4]	[6:0]	Filtering width of GPF0_INT[4] This value is valid when FLTSEL10is 1.	0

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2.2.55.43 GPIO Interrupt Control Registers (GPF1_INT_FLTCON0, R/W, Address = 0xE020_0850)

GPF1_INT_FLTCON0	Bit	Description	Initial State
FLTEN11[3]	[31]	Filter Enable for GPF1_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH11[3]	[30:24]	Filtering width of GPF1_INT[3] This value is valid when FLTSEL11 is 1.	0
FLTEN11[2]	[23]	Filter Enable for GPF1_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH11[2]	[22:16]	Filtering width of GPF1_INT[2] This value is valid when FLTSEL11 is 1.	0
FLTEN11[1]	[15]	Filter Enable for GPF1_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH11[1]	[14:8]	Filtering width of GPF1_INT[1] This value is valid when FLTSEL11 is 1.	0
FLTEN11[0]	[7]	Filter Enable for GPF1_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH11[0]	[6:0]	Filtering width of GPF1_INT[0] This value is valid when FLTSEL11 is 1.	0

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2.2.55.44 GPIO Interrupt Control Registers (GPF1_INT_FLTCON1, R/W, Address = 0xE020_0854)

GPF1_INT_FLTCON1	Bit	Description	Initial State
FLTEN11[7]	[31]	Filter Enable for GPF1_INT[7] 0 = Disables 1 = Enables	0
FLTWIDTH11[7]	[30:24]	Filtering width of GPF1_INT[7] This value is valid when FLTSEL11 is 1.	0
FLTEN11[6]	[23]	Filter Enable for GPF1_INT[6] 0 = Disables 1 = Enables	0
FLTWIDTH11[6]	[22:16]	Filtering width of GPF1_INT[6] This value is valid when FLTSEL11 is 1.	0
FLTEN11[5]	[15]	Filter Enable for GPF1_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH11[5]	[14:8]	Filtering width of GPF1_INT[5] This value is valid when FLTSEL11 is 1.	0
FLTEN11[4]	[7]	Filter Enable for GPF1_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH11[4]	[6:0]	Filtering width of GPF1_INT[4] This value is valid when FLTSEL11 is 1.	0

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2.2.55.45 GPIO Interrupt Control Registers (GPF2_INT_FLTCON0, R/W, Address = 0xE020_0858)

GPF2_INT_FLTCON0	Bit	Description	Initial State
FLTEN12[3]	[31]	Filter Enable for GPF2_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH12[3]	[30:24]	Filtering width of GPF2_INT[3] This value is valid when FLTSEL12 is 1.	0
FLTEN12[2]	[23]	Filter Enable for GPF2_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH12[2]	[22:16]	Filtering width of GPF2_INT[2] This value is valid when FLTSEL12 is 1.	0
FLTEN12[1]	[15]	Filter Enable for GPF2_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH12[1]	[14:8]	Filtering width of GPF2_INT[1] This value is valid when FLTSEL12 is 1.	0
FLTEN12[0]	[7]	Filter Enable for GPF2_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH12[0]	[6:0]	Filtering width of GPF2_INT[0] This value is valid when FLTSEL12 is 1.	0

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2.2.55.46 GPIO Interrupt Control Registers (GPF2_INT_FLTCON1, R/W, Address = 0xE020_085C)

GPF2_INT_FLTCON1	Bit	Description	Initial State
FLTEN12[7]	[31]	Filter Enable for GPF2_INT[7] 0 = Disables 1 = Enables	0
FLTWIDTH12[7]	[30:24]	Filtering width of GPF2_INT[7] This value is valid when FLTSEL12 is 1.	0
FLTEN12[6]	[23]	Filter Enable for GPF2_INT[6] 0 = Disables 1 = Enables	0
FLTWIDTH12[6]	[22:16]	Filtering width of GPF2_INT[6] This value is valid when FLTSEL12 is 1.	0
FLTEN12[5]	[15]	Filter Enable for GPF2_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH12[5]	[14:8]	Filtering width of GPF2_INT[5] This value is valid when FLTSEL12 is 1.	0
FLTEN12[4]	[7]	Filter Enable for GPF2_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH12[4]	[6:0]	Filtering width of GPF2_INT[4] This value is valid when FLTSEL12 is 1.	0

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2.2.55.47 GPIO Interrupt Control Registers (GPF3_INT_FLTCON0, R/W, Address = 0xE020_0860)

GPF3_INT_FLTCON0	Bit	Description	Initial State
FLTEN13[3]	[31]	Filter Enable for GPF3_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH13[3]	[30:24]	Filtering width of GPF3_INT[3] This value is valid when FLTSEL13 is 1.	0
FLTEN13[2]	[23]	Filter Enable for GPF3_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH13[2]	[22:16]	Filtering width of GPF3_INT[2] This value is valid when FLTSEL13is 1.	0
FLTEN13[1]	[15]	Filter Enable for GPF3_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH13[1]	[14:8]	Filtering width of GPF3_INT[1] This value is valid when FLTSEL13 is 1.	0
FLTEN13[0]	[7]	Filter Enable for GPF3_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH13[0]	[6:0]	Filtering width of GPF3_INT[0] This value is valid when FLTSEL13 is 1.	0

2.2.55.48 GPIO Interrupt Control Registers (GPF3_INT_FLTCON1, R/W, Address = 0xE020_0864)

GPF3_INT_FLTCON1	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
FLTEN13[5]	[15]	Filter Enable for GPF3_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH13[5]	[14:8]	Filtering width of GPF3_INT[5] This value is valid when FLTSEL13 is 1.	0
FLTEN13[4]	[7]	Filter Enable for GPF3_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH13[4]	[6:0]	Filtering width of GPF3_INT[4] This value is valid when FLTSEL13 is 1.	0

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2.2.55.49 GPIO Interrupt Control Registers (GPG0_INT_FLTCON0, R/W, Address = 0xE020_0868)

GPG0_INT_FLTCON0	Bit	Description	Initial State
FLTEN14[3]	[31]	Filter Enable for GPG0_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH14[3]	[30:24]	Filtering width of GPG0_INT[3] This value is valid when FLTSEL14 is 1.	0
FLTEN14[2]	[23]	Filter Enable for GPG0_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH14[2]	[22:16]	Filtering width of GPG0_INT[2] This value is valid when FLTSEL14 is 1.	0
FLTEN14[1]	[15]	Filter Enable for GPG0_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH14[1]	[14:8]	Filtering width of GPG0_INT[1] This value is valid when FLTSEL14 is 1.	0
FLTEN14[0]	[7]	Filter Enable for GPG0_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH14[0]	[6:0]	Filtering width of GPG0_INT[0] This value is valid when FLTSEL14 is 1.	0

2.2.55.50 GPIO Interrupt Control Registers (GPG0_INT_FLTCON1, R/W, Address = 0xE020_086C)

GPG0_INT_FLTCON1	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
FLTEN14[6]	[23]	Filter Enable for GPG0_INT[6] 0 = Disables 1 = Enables	0
FLTWIDTH14[6]	[22:16]	Filtering width of GPG0_INT[6] This value is valid when FLTSEL14 is 1.	0
FLTEN14[5]	[15]	Filter Enable for GPG0_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH14[5]	[14:8]	Filtering width of GPG0_INT[5] This value is valid when FLTSEL14 is 1.	0
FLTEN14[4]	[7]	Filter Enable for GPG0_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH14[4]	[6:0]	Filtering width of GPG0_INT[4] This value is valid when FLTSEL14 is 1.	0

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2.2.55.51 GPIO Interrupt Control Registers (GPG1_INT_FLTCON0, R/W, Address = 0xE020_0870)

GPG1_INT_FLTCON0	Bit	Description	Initial State
FLTEN15[3]	[31]	Filter Enable for GPG1_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH15[3]	[30:24]	Filtering width of GPG1_INT[3] This value is valid when FLTSEL15 is 1.	0
FLTEN15[2]	[23]	Filter Enable for GPG1_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH15[2]	[22:16]	Filtering width of GPG1_INT[2] This value is valid when FLTSEL15 is 1.	0
FLTEN15[1]	[15]	Filter Enable for GPG1_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH15[1]	[14:8]	Filtering width of GPG1_INT[1] This value is valid when FLTSEL15 is 1.	0
FLTEN15[0]	[7]	Filter Enable for GPG1_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH15[0]	[6:0]	Filtering width of GPG1_INT[0] This value is valid when FLTSEL15is 1.	0

2.2.55.52 GPIO Interrupt Control Registers (GPG1_INT_FLTCON1, R/W, Address = 0xE020_0874)

GPG1_INT_FLTCON1	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
FLTEN15[6]	[23]	Filter Enable for GPG1_INT[6] 0 = Disables 1 = Enables	0
FLTWIDTH15[6]	[22:16]	Filtering width of GPG1_INT[6] This value is valid when FLTSEL15 is 1.	0
FLTEN15[5]	[15]	Filter Enable for GPG1_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH15[5]	[14:8]	Filtering width of GPG1_INT[5] This value is valid when FLTSEL15 is 1.	0
FLTEN15[4]	[7]	Filter Enable for GPG1_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH15[4]	[6:0]	Filtering width of GPG1_INT[4] This value is valid when FLTSEL15 is 1.	0

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2.2.55.53 GPIO Interrupt Control Registers (GPG2_INT_FLTCON0, R/W, Address = 0xE020_0878)

GPG2_INT_FLTCON0	Bit	Description	Initial State
FLTEN16[3]	[31]	Filter Enable for GPG2_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH16[3]	[30:24]	Filtering width of GPG2_INT[3] This value is valid when FLTSEL16 is 1.	0
FLTEN16[2]	[23]	Filter Enable for GPG2_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH16[2]	[22:16]	Filtering width of GPG2_INT[2] This value is valid when FLTSEL16 is 1.	0
FLTEN16[1]	[15]	Filter Enable for GPG2_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH16[1]	[14:8]	Filtering width of GPG2_INT[1] This value is valid when FLTSEL16 is 1.	0
FLTEN16[0]	[7]	Filter Enable for GPG2_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH16[0]	[6:0]	Filtering width of GPG2_INT[0] This value is valid when FLTSEL16 is 1.	0

2.2.55.54 GPIO Interrupt Control Registers (GPG2_INT_FLTCON1, R/W, Address = 0xE020_087C)

GPG2_INT_FLTCON1	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
FLTEN16[6]	[23]	Filter Enable for GPG2_INT[6] 0 = Disables 1 = Enables	0
FLTWIDTH16[6]	[22:16]	Filtering width of GPG2_INT[6] This value is valid when FLTSEL16 is 1.	0
FLTEN16[5]	[15]	Filter Enable for GPG2_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH16[5]	[14:8]	Filtering width of GPG2_INT[5] This value is valid when FLTSEL16 is 1.	0
FLTEN16[4]	[7]	Filter Enable for GPG2_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH16[4]	[6:0]	Filtering width of GPG2_INT[4] This value is valid when FLTSEL16 is 1.	0

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2.2.55.55 GPIO Interrupt Control Registers (GPG3_INT_FLTCON0, R/W, Address = 0xE020_0880)

GPG3_INT_FLTCON0	Bit	Description	Initial State
FLTEN17[3]	[31]	Filter Enable for GPG3_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH17[3]	[30:24]	Filtering width of GPG3_INT[3] This value is valid when FLTSEL17 is 1.	0
FLTEN17[2]	[23]	Filter Enable for GPG3_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH17[2]	[22:16]	Filtering width of GPG3_INT[2] This value is valid when FLTSEL17 is 1.	0
FLTEN17[1]	[15]	Filter Enable for GPG3_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH17[1]	[14:8]	Filtering width of GPG3_INT[1] This value is valid when FLTSEL17 is 1.	0
FLTEN17[0]	[7]	Filter Enable for GPG3_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH17[0]	[6:0]	Filtering width of GPG3_INT[0] This value is valid when FLTSEL17 is 1.	0

2.2.55.56 GPIO Interrupt Control Registers (GPG3_INT_FLTCON1, R/W, Address = 0xE020_0884)

GPG3_INT_FLTCON1	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
FLTEN17[6]	[23]	Filter Enable for GPG3_INT[6] 0 = Disables 1 = Enables	0
FLTWIDTH17[6]	[22:16]	Filtering width of GPG3_INT[6] This value is valid when FLTSEL17 is 1.	0
FLTEN17[5]	[15]	Filter Enable for GPG3_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH17[5]	[14:8]	Filtering width of GPG3_INT[5] This value is valid when FLTSEL17 is 1.	0
FLTEN17[4]	[7]	Filter Enable for GPG3_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH17[4]	[6:0]	Filtering width of GPG3_INT[4] This value is valid when FLTSEL17 is 1.	0

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2.2.55.57 GPIO Interrupt Control Registers (GPJ0_INT_FLTCON0, R/W, Address = 0xE020_0888)

GPJ0_INT_FLTCON0	Bit	Description	Initial State
FLTEN18[3]	[31]	Filter Enable for GPJ0_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH18[3]	[30:24]	Filtering width of GPJ0_INT[3] This value is valid when FLTSEL18 is 1.	0
FLTEN18[2]	[23]	Filter Enable for GPJ0_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH18[2]	[22:16]	Filtering width of GPJ0_INT[2] This value is valid when FLTSEL18 is 1.	0
FLTEN18[1]	[15]	Filter Enable for GPJ0_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH18[1]	[14:8]	Filtering width of GPJ0_INT[1] This value is valid when FLTSEL18 is 1.	0
FLTEN18[0]	[7]	Filter Enable for GPJ0_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH18[0]	[6:0]	Filtering width of GPJ0_INT[0] This value is valid when FLTSEL18 is 1.	0

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2.2.55.58 GPIO Interrupt Control Registers (GPJ0_INT_FLTCON1, R/W, Address = 0xE020_088C)

GPJ0_INT_FLTCON1	Bit	Description	Initial State
FLTEN18[7]	[31]	Filter Enable for GPJ0_INT[7] 0 = Disables 1 = Enables	0
FLTWIDTH18[7]	[30:24]	Filtering width of GPJ0_INT[7] This value is valid when FLTSEL18 is 1.	0
FLTEN18[6]	[23]	Filter Enable for GPJ0_INT[6] 0 = Disables 1 = Enables	0
FLTWIDTH18[6]	[22:16]	Filtering width of GPJ0_INT[6] This value is valid when FLTSEL18 is 1.	0
FLTEN18[5]	[15]	Filter Enable for GPJ0_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH18[5]	[14:8]	Filtering width of GPJ0_INT[5] This value is valid when FLTSEL18 is 1.	0
FLTEN18[4]	[7]	Filter Enable for GPJ0_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH18[4]	[6:0]	Filtering width of GPJ0_INT[4] This value is valid when FLTSEL18 is 1.	0

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2.2.55.59 GPIO Interrupt Control Registers (GPJ1_INT_FLTCON0, R/W, Address = 0xE020_0890)

GPJ1_INT_FLTCON0	Bit	Description	Initial State
FLTEN19[3]	[31]	Filter Enable for GPJ1_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH19[3]	[30:24]	Filtering width of GPJ1_INT[3] This value is valid when FLTSEL19 is 1.	0
FLTEN19[2]	[23]	Filter Enable for GPJ1_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH19[2]	[22:16]	Filtering width of GPJ1_INT[2] This value is valid when FLTSEL19 is 1.	0
FLTEN19[1]	[15]	Filter Enable for GPJ1_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH19[1]	[14:8]	Filtering width of GPJ1_INT[1] This value is valid when FLTSEL19 is 1.	0
FLTEN19[0]	[7]	Filter Enable for GPJ1_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH19[0]	[6:0]	Filtering width of GPJ1_INT[0] This value is valid when FLTSEL19 is 1.	0

2.2.55.60 GPIO Interrupt Control Registers (GPJ1_INT_FLTCON1, R/W, Address = 0xE020_0894)

GPJ1_INT_FLTCON1	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
FLTEN19[5]	[15]	Filter Enable for GPJ1_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH19[5]	[14:8]	Filtering width of GPJ1_INT[5] This value is valid when FLTSEL19 is 1.	000
FLTEN19[4]	[7]	Filter Enable for GPJ1_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH19[4]	[6:0]	Filtering width of GPJ1_INT[4] This value is valid when FLTSEL19 is 1.	000

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2.2.55.61 GPIO Interrupt Control Registers (GPJ2_INT_FLTCON0, R/W, Address = 0xE020_0898)

GPJ2_INT_FLTCON0	Bit	Description	Initial State
FLTEN20[3]	[31]	Filter Enable for GPJ2_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH20[3]	[30:24]	Filtering width of GPJ2_INT[3] This value is valid when FLTSEL20 is 1.	0
FLTEN20[2]	[23]	Filter Enable for GPJ2_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH20[2]	[22:16]	Filtering width of GPJ2_INT[2] This value is valid when FLTSEL20 is 1.	0
FLTEN20[1]	[15]	Filter Enable for GPJ2_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH20[1]	[14:8]	Filtering width of GPJ2_INT[1] This value is valid when FLTSEL20 is 1.	0
FLTEN20[0]	[7]	Filter Enable for GPJ2_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH20[0]	[6:0]	Filtering width of GPJ2_INT[0] This value is valid when FLTSEL20 is 1.	0

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2.2.55.62 GPIO Interrupt Control Registers (GPJ2_INT_FLTCON1, R/W, Address = 0xE020_089C)

GPJ2_INT_FLTCON1	Bit	Description	Initial State
FLTEN20[7]	[31]	Filter Enable for GPJ2_INT[7] 0 = Disables 1 = Enables	0
FLTWIDTH20[7]	[30:24]	Filtering width of GPJ2_INT[7] This value is valid when FLTSEL20 is 1.	0
FLTEN20[6]	[23]	Filter Enable for GPJ2_INT[6] 0 = Disables 1 = Enables	0
FLTWIDTH20[6]	[22:16]	Filtering width of GPJ2_INT[6] This value is valid when FLTSEL20 is 1.	0
FLTEN20[5]	[15]	Filter Enable for GPJ2_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH20[5]	[14:8]	Filtering width of GPJ2_INT[5] This value is valid when FLTSEL20 is 1.	0
FLTEN20[4]	[7]	Filter Enable for GPJ2_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH20[4]	[6:0]	Filtering width of GPJ2_INT[4] This value is valid when FLTSEL20 is 1.	0

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2.2.55.63 GPIO Interrupt Control Registers (GPJ3_INT_FLTCON0, R/W, Address = 0xE020_08A0)

GPJ3_INT_FLTCON0	Bit	Description	Initial State
FLTEN21[3]	[31]	Filter Enable for GPJ3_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH21[3]	[30:24]	Filtering width of GPJ3_INT[3] This value is valid when FLTSEL21 is 1.	0
FLTEN21[2]	[23]	Filter Enable for GPJ3_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH21[2]	[22:16]	Filtering width of GPJ3_INT[2] This value is valid when FLTSEL21 is 1.	0
FLTEN21[1]	[15]	Filter Enable for GPJ3_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH21[1]	[14:8]	Filtering width of GPJ3_INT[1] This value is valid when FLTSEL21 is 1.	0
FLTEN21[0]	[7]	Filter Enable for GPJ3_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH21[0]	[6:0]	Filtering width of GPJ3_INT[0] This value is valid when FLTSEL21 is 1.	0

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2.2.55.64 GPIO Interrupt Control Registers (GPJ3_INT_FLTCON1, R/W, Address = 0xE020_08A4)

GPJ3_INT_FLTCON1	Bit	Description	Initial State
FLTEN21[7]	[31]	Filter Enable for GPJ3_INT[7] 0 = Disables 1 = Enables	0
FLTWIDTH21[7]	[30:24]	Filtering width of GPJ3_INT[7] This value is valid when FLTSEL21 is 1.	0
FLTEN21[6]	[23]	Filter Enable for GPJ3_INT[6] 0 = Disables 1 = Enables	0
FLTWIDTH21[6]	[22:16]	Filtering width of GPJ3_INT[6] This value is valid when FLTSEL21 is 1.	0
FLTEN21[5]	[15]	Filter Enable for GPJ3_INT[5] 0 = Disables 1 = Enables	0
FLTWIDTH21[5]	[14:8]	Filtering width of GPJ3_INT[5] This value is valid when FLTSEL21 is 1.	0
FLTEN21[4]	[7]	Filter Enable for GPJ3_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH21[4]	[6:0]	Filtering width of GPJ3_INT[4] This value is valid when FLTSEL21 is 1.	0

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2.2.55.65 GPIO Interrupt Control Registers (GPJ4_INT_FLTCON0, R/W, Address = 0xE020_08A8)

GPJ4_INT_FLTCON0	Bit	Description	Initial State
FLTEN22[3]	[31]	Filter Enable for GPJ4_INT[3] 0 = Disables 1 = Enables	0
FLTWIDTH22[3]	[30:24]	Filtering width of GPJ4_INT[3] This value is valid when FLTSEL22 is 1.	0
FLTEN22[2]	[23]	Filter Enable for GPJ4_INT[2] 0 = Disables 1 = Enables	0
FLTWIDTH22[2]	[22:16]	Filtering width of GPJ4_INT[2] This value is valid when FLTSEL22 is 1.	0
FLTEN22[1]	[15]	Filter Enable for GPJ4_INT[1] 0 = Disables 1 = Enables	0
FLTWIDTH22[1]	[14:8]	Filtering width of GPJ4_INT[1] This value is valid when FLTSEL22 is 1.	0
FLTEN22[0]	[7]	Filter Enable for GPJ4_INT[0] 0 = Disables 1 = Enables	0
FLTWIDTH22[0]	[6:0]	Filtering width of GPJ4_INT[0] This value is valid when FLTSEL22 is 1.	0

2.2.55.66 GPIO Interrupt Control Registers (GPJ4_INT_FLTCON1, R/W, Address = 0xE020_08AC)

GPJ4_INT_FLTCON1	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
FLTEN22[4]	[7]	Filter Enable for GPJ4_INT[4] 0 = Disables 1 = Enables	0
FLTWIDTH22[4]	[6:0]	Filtering width of GPJ4_INT[4] This value is valid when FLTSEL22 is 1.	0

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2.2.55.67 GPIO Interrupt Control Registers (GPA0_INT_MASK, R/W, Address = 0xE020_0900)

GPA0_INT_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPA0_INT_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
GPA0_INT_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
GPA0_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPA0_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPA0_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPA0_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPA0_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPA0_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

2.2.55.68 GPIO Interrupt Control Registers (GPA1_INT_MASK, R/W, Address = 0xE020_0904)

GPA1_INT_MASK	Bit	Description	Initial State
Reserved	[31:4]	Reserved	0
GPA1_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPA1_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPA1_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPA1_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.55.69 GPIO Interrupt Control Registers (GPB_INT_MASK, R/W, Address = 0xE020_0908)

GPB_INT_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPB_INT_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
GPB_INT_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
GPB_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPB_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPB_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPB_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPB_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPB_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.55.70 GPIO Interrupt Control Registers (GPC0_INT_MASK, R/W, Address = 0xE020_090C)

GPC0_INT_MASK	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
GPC0_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPC0_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPC0_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPC0_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPC0_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

2.2.55.71 GPIO Interrupt Control Registers (GPC1_INT_MASK, R/W, Address = 0xE020_0910)

GPC1_INT_MASK	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
GPC1_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPC1_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPC1_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPC1_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPC1_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.55.72 GPIO Interrupt Control Registers (GPD0_INT_MASK, R/W, Address = 0xE020_0914)

GPD0_INT_MASK	Bit	Description	Initial State
Reserved	[31:4]	Reserved	0
GPD0_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPD0_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPD0_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPD0_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

2.2.55.73 GPIO Interrupt Control Registers (GPD1_INT_MASK, R/W, Address = 0xE020_0918)

GPD1_INT_MASK	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0
GPD1_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPD1_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPD1_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPD1_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPD1_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPD1_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.55.74 GPIO Interrupt Control Registers (GPE0_INT_MASK, R/W, Address = 0xE020_091C)

GPE0_INT_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPE0_INT_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
GPE0_INT_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
GPE0_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPE0_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPE0_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPE0_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPE0_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPE0_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

2.2.55.75 GPIO Interrupt Control Registers (GPE1_INT_MASK, R/W, Address = 0xE020_0920)

GPE1_INT_MASK	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
GPE1_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPE1_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPE1_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPE1_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPE1_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.55.76 GPIO Interrupt Control Registers (GPF0_INT_MASK, R/W, Address = 0xE020_0924)

GPF0_INT_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPF0_INT_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
GPF0_INT_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
GPF0_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPF0_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPF0_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPF0_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPF0_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPF0_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

2.2.55.77 GPIO Interrupt Control Registers (GPF1_INT_MASK, R/W, Address = 0xE020_0928)

GPF1_INT_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPF1_INT_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
GPF1_INT_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
GPF1_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPF1_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPF1_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPF1_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPF1_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPF1_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.55.78 GPIO Interrupt Control Registers (GPF2_INT_MASK, R/W, Address = 0xE020_092C)

GPF2_INT_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPF2_INT_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
GPF2_INT_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
GPF2_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPF2_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPF2_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPF2_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPF2_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPF2_INT_MASK[0]	[0]	0 = Enable Interrupt 1 = Masked	1

2.2.55.79 GPIO Interrupt Control Registers (GPF3_INT_MASK, R/W, Address = 0xE020_0930)

GPF3_INT_MASK	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0
GPF3_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPF3_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPF3_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPF3_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPF3_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPF3_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.55.80 GPIO Interrupt Control Registers (GPG0_INT_MASK, R/W, Address = 0xE020_0934)

GPG0_INT_MASK	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
GPG0_INT_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
GPG0_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPG0_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPG0_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPG0_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPG0_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPG0_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

2.2.55.81 GPIO Interrupt Control Registers (GPG1_INT_MASK, R/W, Address = 0xE020_0938)

GPG1_INT_MASK	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
GPG1_INT_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
GPG1_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPG1_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPG1_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPG1_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPG1_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPG1_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.55.82 GPIO Interrupt Control Registers (GPG2_INT_MASK, R/W, Address = 0xE020_093C)

GPG2_INT_MASK	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
GPG2_INT_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
GPG2_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPG2_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPG2_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPG2_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPG2_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPG2_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

2.2.55.83 GPIO Interrupt Control Registers (GPG3_INT_MASK, R/W, Address = 0xE020_0940)

GPG3_INT_MASK	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
GPG3_INT_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
GPG3_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPG3_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPG3_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPG3_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPG3_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPG3_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.55.84 GPIO Interrupt Control Registers (GPJ0_INT_MASK, R/W, Address = 0xE020_0944)

GPJ0_INT_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPJ0_INT_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
GPJ0_INT_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
GPJ0_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPJ0_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPJ0_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPJ0_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPJ0_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPJ0_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

2.2.55.85 GPIO Interrupt Control Registers (GPJ1_INT_MASK, R/W, Address = 0xE020_0948)

GPJ1_INT_MASK	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0
GPJ1_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPJ1_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPJ1_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPJ1_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPJ1_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPJ1_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.55.86 GPIO Interrupt Control Registers (GPJ2_INT_MASK, R/W, Address = 0xE020_094C)

GPJ2_INT_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPJ2_INT_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
GPJ2_INT_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
GPJ2_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPJ2_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPJ2_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPJ2_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPJ2_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPJ2_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

2.2.55.87 GPIO Interrupt Control Registers (GPJ3_INT_MASK, R/W, Address = 0xE020_0950)

GPJ3_INT_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPJ3_INT_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
GPJ3_INT_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
GPJ3_INT_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
GPJ3_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPJ3_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPJ3_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPJ3_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPJ3_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.55.88 GPIO Interrupt Control Registers (GPJ4_INT_MASK, R/W, Address = 0xE020_0954)

GPJ4_INT_MASK	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
GPJ4_INT_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
GPJ4_INT_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
GPJ4_INT_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
GPJ4_INT_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
GPJ4_INT_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.55.89 GPIO Interrupt Control Registers (GPA0_INT_PEND, R/W, Address = 0xE020_0A00)

GPA0_INT_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPA0_INT_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
GPA0_INT_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
GPA0_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPA0_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPA0_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPA0_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPA0_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPA0_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

2.2.55.90 GPIO Interrupt Control Registers (GPA1_INT_PEND, R/W, Address = 0xE020_0A04)

GPA1_INT_PEND	Bit	Description	Initial State
Reserved	[31:4]	Reserved	0
GPA1_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPA1_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPA1_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPA1_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.55.91 GPIO Interrupt Control Registers (GPB_INT_PEND, R/W, Address = 0xE020_0A08)

GPB_INT_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPB_INT_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
GPB_INT_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
GPB_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPB_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPB_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPB_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPB_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPB_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.55.92 GPIO Interrupt Control Registers (GPC0_INT_PEND, R/W, Address = 0xE020_0A0C)

GPC0_INT_PEND	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
GPC0_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPC0_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPC0_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPC0_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPC0_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

2.2.55.93 GPIO Interrupt Control Registers (GPC1_INT_PEND, R/W, Address = 0xE020_0A10)

GPC1_INT_PEND	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
GPC1_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPC1_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPC1_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPC1_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPC1_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.55.94 GPIO Interrupt Control Registers (GPD0_INT_PEND, R/W, Address = 0xE020_0A14)

GPD0_INT_PEND	Bit	Description	Initial State
Reserved	[31:4]	Reserved	0
GPD0_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPD0_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPD0_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPD0_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

2.2.55.95 GPIO Interrupt Control Registers (GPD1_INT_PEND, R/W, Address = 0xE020_0A18)

GPD1_INT_PEND	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0
GPD1_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPD1_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPD1_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPD1_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPD1_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPD1_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.55.96 GPIO Interrupt Control Registers (GPE0_INT_PEND, R/W, Address = 0xE020_0A1C)

GPE0_INT_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPE0_INT_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
GPE0_INT_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
GPE0_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPE0_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPE0_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPE0_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPE0_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPE0_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

2.2.55.97 GPIO Interrupt Control Registers (GPE1_INT_PEND, R/W, Address = 0xE020_0A20)

GPE1_INT_PEND	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
GPE1_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPE1_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPE1_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPE1_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPE1_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.55.98 GPIO Interrupt Control Registers (GPF0_INT_PEND, R/W, Address = 0xE020_0A24)

GPF0_INT_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPF0_INT_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
GPF0_INT_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
GPF0_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPF0_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPF0_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPF0_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPF0_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPF0_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

2.2.55.99 GPIO Interrupt Control Registers (GPF1_INT_PEND, R/W, Address = 0xE020_0A28)

GPF1_INT_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPF1_INT_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
GPF1_INT_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
GPF1_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPF1_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPF1_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPF1_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPF1_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPF1_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.55.100 GPIO Interrupt Control Registers (GPF2_INT_PEND, R/W, Address = 0xE020_0A2C)

GPF2_INT_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPF2_INT_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
GPF2_INT_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
GPF2_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPF2_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPF2_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPF2_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPF2_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPF2_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

2.2.55.101 GPIO Interrupt Control Registers (GPF3_INT_PEND, R/W, Address = 0xE020_0A30)

GPF3_INT_PEND	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0
GPF3_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPF3_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPF3_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPF3_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPF3_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPF3_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.55.102 GPIO Interrupt Control Registers (GPG0_INT_PEND, R/W, Address = 0xE020_0A34)

GPG0_INT_PEND	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
GPG0_INT_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
GPG0_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPG0_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPG0_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPG0_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPG0_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPG0_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

2.2.55.103 GPIO Interrupt Control Registers (GPG1_INT_PEND, R/W, Address = 0xE020_0A38)

GPG1_INT_PEND	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
GPG1_INT_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
GPG1_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPG1_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPG1_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPG1_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPG1_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPG1_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.55.104 GPIO Interrupt Control Registers (GPG2_INT_PEND, R/W, Address = 0xE020_0A3C)

GPG2_INT_PEND	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
GPG2_INT_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
GPG2_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPG2_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPG2_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPG2_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPG2_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPG2_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

2.2.55.105 GPIO Interrupt Control Registers (GPG3_INT_PEND, R/W, Address = 0xE020_0A40)

GPG3_INT_PEND	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
GPG3_INT_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
GPG3_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPG3_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPG3_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPG3_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPG3_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPG3_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.55.106 GPIO Interrupt Control Registers (GPJ0_INT_PEND, R/W, Address = 0xE020_0A44)

GPJ0_INT_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPJ0_INT_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
GPJ0_INT_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
GPJ0_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPJ0_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPJ0_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPJ0_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPJ0_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPJ0_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

2.2.55.107 GPIO Interrupt Control Registers (GPJ1_INT_PEND, R/W, Address = 0xE020_0A48)

GPJ1_INT_PEND	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0
GPJ1_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPJ1_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPJ1_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPJ1_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPJ1_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPJ1_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.55.108 GPIO Interrupt Control Registers (GPJ2_INT_PEND, R/W, Address = 0xE020_0A4C)

GPJ2_INT_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPJ2_INT_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
GPJ2_INT_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
GPJ2_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPJ2_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPJ2_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPJ2_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPJ2_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPJ2_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

2.2.55.109 GPIO Interrupt Control Registers (GPJ3_INT_PEND, R/W, Address = 0xE020_0A50)

GPJ3_INT_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
GPJ3_INT_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
GPJ3_INT_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
GPJ3_INT_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
GPJ3_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPJ3_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPJ3_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPJ3_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPJ3_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.55.110 GPIO Interrupt Control Registers (GPJ4_INT_PEND, R/W, Address = 0xE020_0A54)

GPJ4_INT_PEND	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
GPJ4_INT_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
GPJ4_INT_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
GPJ4_INT_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
GPJ4_INT_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
GPJ4_INT_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.55.111 GPIO Interrupt Control Registers (GPIO_INT_GRPPRI, R/W, Address = 0xE020_0B00)

GPIO_INT_GRPPRI	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
GPIO_INT_GRPPRI	[0]	GPIO Interrupt groups priority rotate enable 0 = Not rotate (Fixed)	0

2.2.55.112 GPIO Interrupt Control Registers (GPIO_INT_PRIORITY, R/W, Address = 0xE020_0B04)

GPIO_INT_PRIORITY	Bit	Description	Initial State
Reserved	[31:22]	Reserved	0
GPJ4_INT_PRI	[21]	GPJ4_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPJ3_INT_PRI	[20]	GPJ3_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPJ2_INT_PRI	[19]	GPJ2_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPJ1_INT_PRI	[18]	GPJ1_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPJ0_INT_PRI	[17]	GPJ0_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPG3_INT_PRI	[16]	GPG3_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPG2_INT_PRI	[15]	GPG2_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPG1_INT_PRI	[14]	GPG1_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPG0_INT_PRI	[13]	GPG0_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPF3_INT_PRI	[12]	GPF3_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPF2_INT_PRI	[11]	GPF2_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPF1_INT_PRI	[10]	GPF1_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPF0_INT_PRI	[9]	GPF0_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPE1_INT_PRI	[8]	GPE1_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPE0_INT_PRI	[7]	GPE0_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPD1_INT_PRI	[6]	GPD1_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPD0_INT_PRI	[5]	GPD0_INT priority rotate enable 0 = Not rotate(Fixed)	0

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GPIO_INT_PRIORITY	Bit	Description	Initial State
GPC1_INT_PRI	[4]	GPC1_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPC0_INT_PRI	[3]	GPC0_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPB_INT_PRI	[2]	GPB_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPA1_INT_PRI	[1]	GPA1_INT priority rotate enable 0 = Not rotate(Fixed)	0
GPA0_INT_PRI	[0]	GPA0_INT priority rotate enable 0 = Not rotate(Fixed)	0

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2.2.55.113 GPIO Interrupt Control Registers (GPIO_INT_SERVICE, R/W, Address = 0xE020_0B08)

GPIO_INT_SERVICE	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
SVC_Group_Num	[7:3]	GPIO Interrupt Service group number (GPA0_INT ~ GPJ4_INT) Non_INT: 00000 == 0x0 GPA0_INT: 00001 == 0x1 GPA1_INT: 00010 == 0x2 GPB_INT: 00011 == 0x3 GPC0_INT: 00100 == 0x4 GPC1_INT: 00101 == 0x5 GPD0_INT: 00110 == 0x6 GPD1_INT: 00111 == 0x7 GPE0_INT: 01000 == 0x8 GPE1_INT: 01001 == 0x9 GPF0_INT: 01010 == 0xA GPF1_INT: 01011 == 0xB GPF2_INT: 01100 == 0xC GPF3_INT: 01101 == 0xD GPG0_INT: 01110 == 0xE GPG1_INT: 01111 == 0xF GPG2_INT: 10000 == 0x10 GPG3_INT: 10001 == 0x11 GPJ0_INT: 10010 == 0x12 GPJ1_INT: 10011 == 0x13 GPJ2_INT: 10100 == 0x14 GPJ3_INT: 10101 = 0x15 GPJ4_INT: 10110 = 0x16	0
SVC_Num	[2:0]	Interrupt number to be serviced	0

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2.2.55.114 GPIO Interrupt Control Registers (GPIO_INT_SERVICE_PEND, R/W, Address = 0xE020_0B0C)

GPIO_INT_SERVICE_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
SVC_PEND_Num	[7:0]	GPIO Interrupt Service Interrupt number (0 = Not occur , 1 = Occur interrupt) (0 ~ 7bit) 0bit: 0000_0001 == 0x1 1bit: 0000_0010 == 0x2 2bit: 0000_0100 == 0x4 3bit: 0000_1000 == 0x8 4bit: 0001_0000 == 0x10 5bit: 0010_0000 == 0x20 6bit: 0100_0000 == 0x40 7bit: 1000_0000 == 0x80	0

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2.2.55.115 GPIO Interrupt Control Registers (GPIO_INT_GRPFIXPRI, R/W, Address = 0xE020_0B10)

GPIO_INT_GRPFIXPRI	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
Highest_GRP_NUM	[4:0]	Group number of the highest priority when fixed group priority mode: (GPA0_INT ~ GPJ4_INT) Non_INT: 00000 == 0x0 GPA0_INT: 00001 == 0x1 GPA1_INT: 00010 == 0x2 GPB_INT: 00011 == 0x3 GPC0_INT: 00100 == 0x4 GPC1_INT: 00101 == 0x5 GPD0_INT: 00110 == 0x6 GPD1_INT: 00111 == 0x7 GPE0_INT: 01000 == 0x8 GPE1_INT: 01001 == 0x9 GPF0_INT: 01010 == 0xA GPF1_INT: 01011 == 0xB GPF2_INT: 01100 == 0xC GPF3_INT: 01101 == 0xD GPG0_INT: 01110 == 0xE GPG1_INT: 01111 == 0xF GPG2_INT: 10000 == 0x10 GPG3_INT: 10001 == 0x11 GPJ0_INT: 10010 == 0x12 GPJ1_INT: 10011 == 0x13 GPJ2_INT: 10100 == 0x14 GPJ3_INT: 10101 = 0x15 GPJ4_INT: 10110 = 0x16 *For Example, if GPC0_INT is highest priority, next priority group is GPC1_INT, not GPA0_INT.	0

2.2.55.116 GPIO Interrupt Control Registers (GPA0_INT_FIXPRI, R/W, Address = 0xE020_0B14)

GPA0_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPA0_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

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2.2.55.117 GPIO Interrupt Control Registers (GPA1_INT_FIXPRI, R/W, Address = 0xE020_0B18)

GPA1_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPA1_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.118 GPIO Interrupt Control Registers (GPB_INT_FIXPRI, R/W, Address = 0xE020_0B1C)

GPB_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPB_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

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2.2.55.119 GPIO Interrupt Control Registers (GPC0_INT_FIXPRI, R/W, Address = 0xE020_0B20)

GPC0_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPC0_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.120 GPIO Interrupt Control Registers (GPC1_INT_FIXPRI, R/W, Address = 0xE020_0B24)

GPC1_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPC1_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.121 GPIO Interrupt Control Registers (GPD0_INT_FIXPRI, R/W, Address = 0xE020_0B28)

GPD0_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPD0_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

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2.2.55.122 GPIO Interrupt Control Registers (GPD1_INT_FIXPRI, R/W, Address = 0xE020_0B2C)

GPD1_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPD1_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.123 GPIO Interrupt Control Registers (GPE0_INT_FIXPRI, R/W, Address = 0xE020_0B30)

GPE0_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPE0_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.124 GPIO Interrupt Control Registers (GPE1_INT_FIXPRI, R/W, Address = 0xE020_0B34)

GPE1_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPE1_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

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2.2.55.125 GPIO Interrupt Control Registers (GPF0_INT_FIXPRI, R/W, Address = 0xE020_0B38)

GPF0_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPF0_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.126 GPIO Interrupt Control Registers (GPF1_INT_FIXPRI, R/W, Address = 0xE020_0B3C)

GPF1_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPF1_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.127 GPIO Interrupt Control Registers (GPF2_INT_FIXPRI, R/W, Address = 0xE020_0B40)

GPF2_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPF2_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

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2.2.55.128 GPIO Interrupt Control Registers (GPF3_INT_FIXPRI, R/W, Address = 0xE020_0B44)

GPF3_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPF3_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.129 GPIO Interrupt Control Registers (GPG0_INT_FIXPRI, R/W, Address = 0xE020_0B48)

GPG0_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPG0_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.130 GPIO Interrupt Control Registers (GPG1_INT_FIXPRI, R/W, Address = 0xE020_0B4C)

GPG1_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPG1_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

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2.2.55.131 GPIO Interrupt Control Registers (GPG2_INT_FIXPRI, R/W, Address = 0xE020_0B50)

GPG2_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPG2_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.132 GPIO Interrupt Control Registers (GPG3_INT_FIXPRI, R/W, Address = 0xE020_0B54)

GPG3_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPG3_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.133 GPIO Interrupt Control Registers (GPJ0_INT_FIXPRI, R/W, Address = 0xE020_0B58)

GPJ0_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPJ0_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

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2.2.55.134 GPIO Interrupt Control Registers (GPJ1_INT_FIXPRI, R/W, Address = 0xE020_0B5C)

GPJ1_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPJ1_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.135 GPIO Interrupt Control Registers (GPJ2_INT_FIXPRI, R/W, Address = 0xE020_0B60)

GPJ2_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPJ2_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.136 GPIO Interrupt Control Registers (GPJ3_INT_FIXPRI, R/W, Address = 0xE020_0B64)

GPJ3_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPJ3_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

2.2.55.137 GPIO Interrupt Control Registers (GPJ4_INT_FIXPRI, R/W, Address = 0xE020_0B68)

GPJ4_INT_FIXPRI	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Highest_EINT_NUM	[2:0]	Interrupt number of the highest priority in GPJ4_INT when fixed priority mode: 0~7 *For Example, if #3 is high priority, next priority interrupt is #4, not #0.	0

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2.2.56 PORT GROUP GPH0 CONTROL REGISTER

There are four control registers including GPH0CON, GPH0DAT, GPH0PUD and GPH0DRV in the Port Group GPH0 Control Registers.

Group GPH0 is in alive area

2.2.56.1 Port Group GPH0 Control Register (GPH0CON, R/W, Address = 0xE020_0C00)

GPH0CON	Bit	Description	Initial State
GPH0CON[0]	[3:0]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[0]	0000
GPH0CON[1]	[7:4]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[1]	0000
GPH0CON[2]	[11:8]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[2]	0000
GPH0CON[3]	[15:12]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[3]	0000
GPH0CON[4]	[19:16]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[4]	0000
GPH0CON[5]	[23:20]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[5]	0000
GPH0CON[6]	[27:24]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[6]	0000
GPH0CON[7]	[31:28]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[7]	0000

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2.2.56.2 Port Group GPH0 Control Register (GPH0DAT, R/W, Address = 0xE020_0C04)

GPH0DAT	Bit	Description	Initial State
GPH0DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.56.3 Port Group GPH0 Control Register (GPH0PUD, R/W, Address = 0xE020_0C08)

GPH0PUD	Bit	Description	Initial State
GPH0PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x5555

2.2.56.4 Port Group GPH0 Control Register (GPH0DRV, R/W, Address = 0xE020_0C0C)

GPH0DRV	Bit	Description	Initial State
GPH0DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

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2.2.57 PORT GROUP GPH1 CONTROL REGISTER

There are four control registers including GPH1CON, GPH1DAT, GPH1PUD and GPH1DRV in the Port Group GPH1 Control Registers

Group GPH1 is in alive area

2.2.57.1 Port Group GPH1 Control Register (GPH1CON, R/W, Address = 0xE020_0C20)

GPH1CON	Bit	Description	Initial State
GPH1CON[0]	[3:0]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[8]	0000
GPH1CON[1]	[7:4]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[9]	0000
GPH1CON[2]	[11:8]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[10]	0000
GPH1CON[3]	[15:12]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[11]	0000
GPH1CON[4]	[19:16]	0000 = Input 0001 = Output 0010 ~ 0011 = Reserved 0100 = HDMI_CEC 0100 ~ 1110 = Reserved 1111 = EXT_INT[12]	0000
GPH1CON[5]	[23:20]	0000 = Input 0001 = Output 0010 ~ 0011 = Reserved 0100 = HDMI_HPD 0100 ~ 1110 = Reserved 1111 = EXT_INT[13]	0000
GPH1CON[6]	[27:24]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[14]	0000
GPH1CON[7]	[31:28]	0000 = Input 0001 = Output 0010 ~ 1110 = Reserved 1111 = EXT_INT[15]	0000

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2.2.57.2 Port Group GPH1 Control Register (GPH1DAT, R/W, Address = 0xE020_0C24)

GPH1DAT	Bit	Description	Initial State
GPH1DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.57.3 Port Group GPH1 Control Register (GPH1PUD, R/W, Address = 0xE020_0C28)

GPH1PUD	Bit	Description	Initial State
GPH1PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x5555

2.2.57.4 Port Group GPH1 Control Register (GPH1DRV, R/W, Address = 0xE020_0C2C)

GPH1DRV	Bit	Description	Initial State
GPH1DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x0000

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2.2.58 PORT GROUP GPH2 CONTROL REGISTER

There are four control registers, namely, GPH2CON, GPH2DAT, GPH2PUD and GPH2DRV in the Port Group GPH2 Control Registers.

Group GPH2 is in alive area.

2.2.58.1 Port Group GPH2 Control Register (GPH2CON, R/W, Address = 0xE020_0C40)

GPH2CON	Bit	Description	Initial State
GPH2CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_COL[0] 0011 ~ 1110 = Reserved 1111 = EXT_INT[16]	0000
GPH2CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_COL[1] 0011 ~ 1110 = Reserved 1111 = EXT_INT[17]	0000
GPH2CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_COL[2] 0011 ~ 1110 = Reserved 1111 = EXT_INT[18]	0000
GPH2CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_COL[3] 0011 ~ 1110 = Reserved 1111 = EXT_INT[19]	0000
GPH2CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_COL[4] 0011 ~ 1110 = Reserved 1111 = EXT_INT[20]	0000
GPH2CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_COL[5] 0011 ~ 1110 = Reserved 1111 = EXT_INT[21]	0000
GPH2CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_COL[6] 0011 ~ 1110 = Reserved	0000

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GPH2CON	Bit	Description	Initial State
		1111 = EXT_INT[22]	
GPH2CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_COL[7] 0011 ~ 1110 = Reserved 1111 = EXT_INT[23]	0000

2.2.58.2 Port Group GPH2 Control Register (GPH2DAT, R/W, Address = 0xE020_0C44)

GPH2DAT	Bit	Description	Initial State
GPH2DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.58.3 Port Group GPH2 Control Register (GPH2PUD, R/W, Address = 0xE020_0C48)

GPH2PUD	Bit	Description	Initial State
GPH2PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x5555

2.2.58.4 Port Group GPH2 Control Register (GPH2DRV, R/W, Address = 0xE020_0C4C)

GPH2DRV	Bit	Description	Initial State
GPH2DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x00

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2.2.59 PORT GROUP GPH3 CONTROL REGISTER

There are four control registers, namely, GPH3CON, GPH3DAT, GPH3PUD and GPH3DRV in the Port Group GPH3 Control Registers.

Group GPH3 is alive area

2.2.59.1 Port Group GPH3 Control Register (GPH3CON, R/W, Address = 0xE020_0C60)

GPH3CON	Bit	Description	Initial State
GPH3CON[0]	[3:0]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_ROW[0] 0011 ~ 1110 = Reserved 1111 = EXT_INT[24]	0000
GPH3CON[1]	[7:4]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_ROW[1] 0011 ~ 1110 = Reserved 1111 = EXT_INT[25]	0000
GPH3CON[2]	[11:8]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_ROW[2] 0011 ~ 1110 = Reserved 1111 = EXT_INT[26]	0000
GPH3CON[3]	[15:12]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_ROW[3] 0011 ~ 1110 = Reserved 1111 = EXT_INT[27]	0000
GPH3CON[4]	[19:16]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_ROW[4] 0011 ~ 1110 = Reserved 1111 = EXT_INT[28]	0000
GPH3CON[5]	[23:20]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_ROW[5] 0011 ~ 1110 = Reserved 1111 = EXT_INT[29]	0000
GPH3CON[6]	[27:24]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_ROW[6] 0011 ~ 1110 = Reserved	0000

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GPH3CON	Bit	Description	Initial State
		1111 = EXT_INT[30]	
GPH3CON[7]	[31:28]	0000 = Input 0001 = Output 0010 = Reserved 0011 = KP_ROW[7] 0011 ~ 1110 = Reserved 1111 = EXT_INT[31]	0000

2.2.59.2 Port Group GPH3 Control Register (GPH3DAT, R/W, Address = 0xE020_0C64)

GPH3DAT	Bit	Description	Initial State
GPH3DAT[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.	0x00

2.2.59.3 Port Group GPH3 Control Register (GPH3PUD, R/W, Address = 0xE020_0C68)

GPH3PUD	Bit	Description	Initial State
GPH3PUD[n]	[2n+1:2n] n=0~7	00 = Pull-up/down disabled 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	0x5555

2.2.59.4 Port Group GPH3 Control Register (GPH3DRV, R/W, Address = 0xE020_0C6C)

GPH3DRV	Bit	Description	Initial State
GPH3DRV[n]	[2n+1:2n] n=0~7	00 = 1x 10 = 2x 01 = 3x 11 = 4x	0x00

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2.2.60 EXTERNAL INTERRUPT CONTROL REGISTERS

External Interrupt consists of 32 bits. EXT_INT[31:0] are used for wake-up source in Power down mode. In idle mode, all interrupts can be wake-up source; the other groups of external interrupts also can be the wake-up sources.

EXT_INT[0] can be used PS_HOLD_CONTROL. For more information on PS_HOLD_CONTROL Register, refer to Chapter 02.04. PMU.

The table below lists the external interrupt control registers.

2.2.60.1 External Interrupt Control Registers (EXT_INT_0_CON, R/W, Address = 0xE020_0E00)

EXT_INT_0_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
EXT_INT_0_CON[7]	[30:28]	Sets the signaling method of EXT_INT[7] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
EXT_INT_0_CON[6]	[26:24]	Sets the signaling method of EXT_INT[6] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
EXT_INT_0_CON[5]	[22:20]	Sets the signaling method of EXT_INT[5] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
EXT_INT_0_CON[4]	[18:16]	Sets the signaling method of EXT_INT[4] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
EXT_INT_0_CON[3]	[14:12]	Sets the signaling method of EXT_INT[3] 000 = Low level 001 = High level 010 = Falling edge triggered	000

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EXT_INT_0_CON	Bit	Description	Initial State
		011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[11]	Reserved	0
EXT_INT_0_CON[2]	[10:8]	Sets the signaling method of EXT_INT[2] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[7]	Reserved	0
EXT_INT_0_CON[1]	[6:4]	Sets the signaling method of EXT_INT[1] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
EXT_INT_0_CON[0]	[2:0]	Sets the signaling method of EXT_INT[0] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.60.2 External Interrupt Control Registers (EXT_INT_1_CON, R/W, Address = 0xE020_0E04)

EXT_INT_1_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
EXT_INT_1_CON[7]	[30:28]	Sets the signaling method of EXT_INT[15] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
EXT_INT_1_CON[6]	[26:24]	Sets the signaling method of EXT_INT[14] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
EXT_INT_1_CON[5]	[22:20]	Sets the signaling method of EXT_INT[13] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
EXT_INT_1_CON[4]	[18:16]	Sets the signaling method of EXT_INT[12] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
EXT_INT_1_CON[3]	[14:12]	Sets the signaling method of EXT_INT[11] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
EXT_INT_1_CON[2]	[10:8]	Sets the signaling method of EXT_INT[10] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered	000

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EXT_INT_1_CON	Bit	Description	Initial State
		100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[7]	Reserved	0
EXT_INT_1_CON[1]	[6:4]	Sets the signaling method of EXT_INT[9] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
EXT_INT_1_CON[0]	[2:0]	Sets the signaling method of EXT_INT[8] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.60.3 External Interrupt Control Registers (EXT_INT_2_CON, R/W, Address = 0xE020_0E08)

EXT_INT_2_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
EXT_INT_2_CON[7]	[30:28]	Sets the signaling method of EXT_INT[23] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
EXT_INT_2_CON[6]	[26:24]	Sets the signaling method of EXT_INT[22] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
EXT_INT_2_CON[5]	[22:20]	Sets the signaling method of EXT_INT[21] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
EXT_INT_2_CON[4]	[18:16]	Sets the signaling method of EXT_INT[20] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
EXT_INT_2_CON[3]	[14:12]	Sets the signaling method of EXT_INT[19] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
EXT_INT_2_CON[2]	[10:8]	Sets the signaling method of EXT_INT[18] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered	000

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EXT_INT_2_CON	Bit	Description	Initial State
		100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[7]	Reserved	0
EXT_INT_2_CON[1]	[6:4]	Sets the signaling method of EXT_INT[17] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
EXT_INT_2_CON[0]	[2:0]	Sets the signaling method of EXT_INT[16] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.60.4 External Interrupt Control Registers (EXT_INT_3_CON, R/W, Address = 0xE020_0E0C)

EXT_INT_3_CON	Bit	Description	Initial State
Reserved	[31]	Reserved	0
EXT_INT_3_CON[7]	[30:28]	Sets the signaling method of EXT_INT[31] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[27]	Reserved	0
EXT_INT_3_CON[6]	[26:24]	Sets the signaling method of EXT_INT[30] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[23]	Reserved	0
EXT_INT_3_CON[5]	[22:20]	Sets the signaling method of EXT_INT[29] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[19]	Reserved	0
EXT_INT_3_CON[4]	[18:16]	Sets the signaling method of EXT_INT[28] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[15]	Reserved	0
EXT_INT_3_CON[3]	[14:12]	Sets the signaling method of EXT_INT[27] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[11]	Reserved	0
EXT_INT_3_CON[2]	[10:8]	Sets the signaling method of EXT_INT[26] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered	000

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EXT_INT_3_CON	Bit	Description	Initial State
		100 = Both edge triggered 101 ~ 111 = Reserved	
Reserved	[7]	Reserved	0
EXT_INT_3_CON[1]	[6:4]	Sets the signaling method of EXT_INT[25] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000
Reserved	[3]	Reserved	0
EXT_INT_3_CON[0]	[2:0]	Sets the signaling method of EXT_INT[24] 000 = Low level 001 = High level 010 = Falling edge triggered 011 = Rising edge triggered 100 = Both edge triggered 101 ~ 111 = Reserved	000

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2.2.60.5 External Interrupt Control Registers (EXT_INT_0_FLTCON0, R/W, Address = 0xE020_0E80)

EXT_INT_0_FLTCON0	Bit	Description	Initial State
FLTEN_0[3]	[31]	Filter Enable for EXT_INT[3] 0 = Disables 1 = Enables	1
FLTSEL_0[3]	[30]	Filter Selection for EXT_INT[3] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_0[3]	[29:24]	Filtering width of EXT_INT[3] This value is valid when FLTSEL30 is 1.	0
FLTEN_0[2]	[23]	Filter Enable for EXT_INT[2] 0 = Disables 1 = Enables	1
FLTSEL_0[2]	[22]	Filter Selection for EXT_INT[2] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_0[2]	[21:16]	Filtering width of EXT_INT[2] This value is valid when FLTSEL30 is 1.	0
FLTEN_0[1]	[15]	Filter Enable for EXT_INT[1] 0 = Disables 1 = Enables	1
FLTSEL_0[1]	[14]	Filter Selection for EXT_INT[1] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_0[1]	[13:8]	Filtering width of EXT_INT[1] This value is valid when FLTSEL30 is 1.	0
FLTEN_0[0]	[7]	Filter Enable for EXT_INT[0] 0 = Disables 1 = Enables	1
FLTSEL_0[0]	[6]	Filter Selection for EXT_INT[0] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_0[0]	[5:0]	Filtering width of EXT_INT[0] This value is valid when FLTSEL30 is 1.	0

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2.2.60.6 External Interrupt Control Registers (EXT_INT_0_FLTCON1, R/W, Address = 0xE020_0E84)

EXT_INT_0_FLTCON1	Bit	Description	Initial State
FLTEN_0[7]	[31]	Filter Enable for EXT_INT[7] 0 = Disables 1 = Enables	1
FLTSEL_0[7]	[30]	Filter Selection for EXT_INT[7] 0 = Delay filter 1 = Digital filter(clock count)	0
FLTWIDTH_0[7]	[29:24]	Filtering width of EXT_INT[7] This value is valid when FLTSEL30 is 1.	0
FLTEN_0[6]	[23]	Filter Enable for EXT_INT[6] 0 = Disables 1 = Enables	1
FLTSEL_0[6]	[22]	Filter Selection for EXT_INT[6] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_0[6]	[21:16]	Filtering width of EXT_INT[6] This value is valid when FLTSEL30 is 1.	0
FLTEN_0[5]	[15]	Filter Enable for EXT_INT[5] 0 = Disables 1 = Enables	1
FLTSEL_0[5]	[14]	Filter Selection for EXT_INT[5] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_0[5]	[13:8]	Filtering width of EXT_INT[5] This value is valid when FLTSEL30 is 1.	0
FLTEN_0[4]	[7]	Filter Enable for EXT_INT[4] 0 = Disables 1 = Enables	1
FLTSEL_0[4]	[6]	Filter Selection for EXT_INT[4] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_0[4]	[5:0]	Filtering width of EXT_INT[4] This value is valid when FLTSEL30 is 1.	0

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2.2.60.7 External Interrupt Control Registers (EXT_INT_1_FLTCON0, R/W, Address = 0xE020_0E88)

EXT_INT_1_FLTCON0	Bit	Description	Initial State
FLTEN_1[3]	[31]	Filter Enable for EXT_INT[11] 0 = Disables 1 = Enables	1
FLTSEL_1[3]	[30]	Filter Selection for EXT_INT[11] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_1[3]	[29:24]	Filtering width of EXT_INT[11] This value is valid when FLTSEL31 is 1.	0
FLTEN_1[2]	[23]	Filter Enable for EXT_INT[10] 0 = Disables 1 = Enables	1
FLTSEL_1[2]	[22]	Filter Selection for EXT_INT[10] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_1[2]	[21:16]	Filtering width of EXT_INT[10] This value is valid when FLTSEL31 is 1.	0
FLTEN_1[1]	[15]	Filter Enable for EXT_INT[9] 0 = Disables 1 = Enables	1
FLTSEL_1[1]	[14]	Filter Selection for EXT_INT[9] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_1[1]	[13:8]	Filtering width of EXT_INT[9] This value is valid when FLTSEL31 is 1.	0
FLTEN_1[0]	[7]	Filter Enable for EXT_INT[8] 0 = Disables 1 = Enables	1
FLTSEL_1[0]	[6]	Filter Selection for EXT_INT[8] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_1[0]	[5:0]	Filtering width of EXT_INT[8] This value is valid when FLTSEL31 is 1.	0

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2.2.60.8 External Interrupt Control Registers (EXT_INT_1_FLTCON1, R/W, Address = 0xE020_0E8C)

EXT_INT_1_FLTCON1	Bit	Description	Initial State
FLTEN_1[7]	[31]	Filter Enable for EXT_INT[15] 0 = Disables 1 = Enables	1
FLTSEL_1[7]	[30]	Filter Selection for EXT_INT[15] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_1[7]	[29:24]	Filtering width of EXT_INT[15] This value is valid when FLTSEL31 is 1.	0
FLTEN_1[6]	[23]	Filter Enable for EXT_INT[14] 0 = Disables 1 = Enables	1
FLTSEL_1[6]	[22]	Filter Selection for EXT_INT[14] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_1[6]	[21:16]	Filtering width of EXT_INT[14] This value is valid when FLTSEL31 is 1.	0
FLTEN_1[5]	[15]	Filter Enable for EXT_INT[13] 0 = Disables 1 = Enables	1
FLTSEL_1[5]	[14]	Filter Selection for EXT_INT[13] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_1[5]	[13:8]	Filtering width of EXT_INT[13] This value is valid when FLTSEL31 is 1.	0
FLTEN_1[4]	[7]	Filter Enable for EXT_INT[12] 0 = Disables 1 = Enables	1
FLTSEL_1[4]	[6]	Filter Selection for EXT_INT[12] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_1[4]	[5:0]	Filtering width of EXT_INT[12] This value is valid when FLTSEL31 is 1.	0

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2.2.60.9 External Interrupt Control Registers (EXT_INT_2_FLTCON0, R/W, Address = 0xE020_0E90)

EXT_INT_2_FLTCON0	Bit	Description	Initial State
FLTEN_2[3]	[31]	Filter Enable for EXT_INT[19] 0 = Disables 1 = Enables	1
FLTSEL_2[3]	[30]	Filter Selection for EXT_INT[19] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_2[3]	[29:24]	Filtering width of EXT_INT[19] This value is valid when FLTSEL32 is 1.	0
FLTEN_2[2]	[23]	Filter Enable for EXT_INT[18] 0 = Disables 1 = Enables	1
FLTSEL_2[2]	[22]	Filter Selection for EXT_INT[18] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_2[2]	[21:16]	Filtering width of EXT_INT[18] This value is valid when FLTSEL32 is 1.	0
FLTEN_2[1]	[15]	Filter Enable for EXT_INT[17] 0 = Disables 1 = Enables	1
FLTSEL_2[1]	[14]	Filter Selection for EXT_INT[17] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_2[1]	[13:8]	Filtering width of EXT_INT[17] This value is valid when FLTSEL32 is 1.	0
FLTEN_2[0]	[7]	Filter Enable for EXT_INT[16] 0 = Disables 1 = Enables	1
FLTSEL_2[0]	[6]	Filter Selection for EXT_INT[16] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_2[0]	[5:0]	Filtering width of EXT_INT[16] This value is valid when FLTSEL32 is 1.	0

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2.2.60.10 External Interrupt Control Registers (EXT_INT_2_FLTCON1, R/W, Address = 0xE020_0E94)

EXT_INT_2_FLTCON1	Bit	Description	Initial State
FLTEN_2[7]	[31]	Filter Enable for EXT_INT[23] 0 = Disables 1 = Enables	1
FLTSEL_2[7]	[30]	Filter Selection for EXT_INT[23] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_2[7]	[29:24]	Filtering width of EXT_INT[23] This value is valid when FLTSEL32 is 1.	0
FLTEN_2[6]	[23]	Filter Enable for EXT_INT[22] 0 = Disables 1 = Enables	1
FLTSEL_2[6]	[22]	Filter Selection for EXT_INT[22] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_2[6]	[21:16]	Filtering width of EXT_INT[22] This value is valid when FLTSEL32 is 1.	0
FLTEN_2[5]	[15]	Filter Enable for EXT_INT[21] 0 = Disables 1 = Enables	1
FLTSEL_2[5]	[14]	Filter Selection for EXT_INT[21] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_2[5]	[13:8]	Filtering width of EXT_INT[21] This value is valid when FLTSEL32 is 1.	0
FLTEN_2[4]	[7]	Filter Enable for EXT_INT[20] 0 = Disables 1 = Enables	1
FLTSEL_2[4]	[6]	Filter Selection for EXT_INT[20] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_2[4]	[5:0]	Filtering width of EXT_INT[20] This value is valid when FLTSEL32is 1.	0

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2.2.60.11 External Interrupt Control Registers (EXT_INT_3_FLTCON0, R/W, Address = 0xE020_0E98)

EXT_INT_3_FLTCON0	Bit	Description	Initial State
FLTEN_3[3]	[31]	Filter Enable for EXT_INT[27] 0 = Disables 1 = Enables	1
FLTSEL_3[3]	[30]	Filter Selection for EXT_INT[27] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_3[3]	[29:24]	Filtering width of EXT_INT[27] This value is valid when FLTSEL33 is 1.	0
FLTEN_3[2]	[23]	Filter Enable for EXT_INT[26] 0 = Disables 1 = Enables	1
FLTSEL_3[2]	[22]	Filter Selection for EXT_INT[26] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_3[2]	[21:16]	Filtering width of EXT_INT[26] This value is valid when FLTSEL33 is 1.	0
FLTEN_3[1]	[15]	Filter Enable for EXT_INT[25] 0 = Disables 1 = Enables	1
FLTSEL_3[1]	[14]	Filter Selection for EXT_INT[25] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_3[1]	[13:8]	Filtering width of EXT_INT[25] This value is valid when FLTSEL33 is 1.	0
FLTEN_3[0]	[7]	Filter Enable for EXT_INT[24] 0 = Disables 1 = Enables	1
FLTSEL_3[0]	[6]	Filter Selection for EXT_INT[24] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_3[0]	[5:0]	Filtering width of EXT_INT[24] This value is valid when FLTSEL33 is 1.	0

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2.2.60.12 External Interrupt Control Registers (EXT_INT_3_FLTCON1, R/W, Address = 0xE020_0E9C)

EXT_INT_3_FLTCON1	Bit	Description	Initial State
FLTEN_3[7]	[31]	Filter Enable for EXT_INT[31] 0 = Disables 1 = Enables	1
FLTSEL_3[7]	[30]	Filter Selection for EXT_INT[31] 0 = Delay filter 1 = Digital filter(clock count)	0
FLTWIDTH_3[7]	[29:24]	Filtering width of EXT_INT[31] This value is valid when FLTSEL33 is 1.	0
FLTEN_3[6]	[23]	Filter Enable for EXT_INT[30] 0 = Disables 1 = Enables	1
FLTSEL_3[6]	[22]	Filter Selection for EXT_INT[30] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_3[6]	[21:16]	Filtering width of EXT_INT[30] This value is valid when FLTSEL33 is 1.	0
FLTEN_3[5]	[15]	Filter Enable for EXT_INT[29] 0 = Disables 1 = Enables	1
FLTSEL_3[5]	[14]	Filter Selection for EXT_INT[29] 0 = Delay filter 1 = Digital filter (clock count)	0
FLTWIDTH_3[5]	[13:8]	Filtering width of EXT_INT[29] This value is valid when FLTSEL33 is 1.	0
FLTEN_3[4]	[7]	Filter Enable for EXT_INT[28] 0 = Disables 1 = Enables	1
FLTSEL_3[4]	[6]	Filter Selection for EXT_INT[28] 0 = Delay filter 1 = Digital filter(clock count)	0
FLTWIDTH_3[4]	[5:0]	Filtering width of EXT_INT[28] This value is valid when FLTSEL33 is 1.	0

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2.2.60.13 External Interrupt Control Registers (EXT_INT_0_MASK, R/W, Address = 0xE020_0F00)

EXT_INT_0_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
EXT_INT_0_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_0_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_0_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_0_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_0_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_0_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_0_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_0_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

2.2.60.14 External Interrupt Control Registers (EXT_INT_1_MASK, R/W, Address = 0xE020_0F04)

EXT_INT_1_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
EXT_INT_1_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_1_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_1_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_1_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_1_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_1_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_1_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_1_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.60.15 External Interrupt Control Registers (EXT_INT_2_MASK, R/W, Address = 0xE020_0F08)

EXT_INT_2_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
EXT_INT_2_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_2_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_2_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_2_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_2_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_2_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_2_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_2_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

2.2.60.16 External Interrupt Control Registers (EXT_INT_3_MASK, R/W, Address = 0xE020_0F0C)

EXT_INT_3_MASK	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
EXT_INT_3_MASK[7]	[7]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_3_MASK[6]	[6]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_3_MASK[5]	[5]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_3_MASK[4]	[4]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_3_MASK[3]	[3]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_3_MASK[2]	[2]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_3_MASK[1]	[1]	0 = Enables Interrupt 1 = Masked	1
EXT_INT_3_MASK[0]	[0]	0 = Enables Interrupt 1 = Masked	1

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2.2.60.17 External Interrupt Control Registers (EXT_INT_0_PEND, R/W, Address = 0xE020_0F40)

EXT_INT_0_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
EXT_INT_0_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_0_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_0_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_0_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_0_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_0_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_0_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_0_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

2.2.60.18 External Interrupt Control Registers (EXT_INT_1_PEND, R/W, Address = 0xE020_0F44)

EXT_INT_1_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
EXT_INT_1_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_1_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_1_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_1_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_1_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_1_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_1_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_1_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.60.19 External Interrupt Control Registers (EXT_INT_2_PEND, R/W, Address = 0xE020_0F48)

EXT_INT_2_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
EXT_INT_2_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_2_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_2_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_2_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_2_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_2_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_2_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_2_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

2.2.60.20 External Interrupt Control Registers (EXT_INT_3_PEND, R/W, Address = 0xE020_0F4C)

EXT_INT_3_PEND	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
EXT_INT_3_PEND[7]	[7]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_3_PEND[6]	[6]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_3_PEND[5]	[5]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_3_PEND[4]	[4]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_3_PEND[3]	[3]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_3_PEND[2]	[2]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_3_PEND[1]	[1]	0 = Not occur 1 = Occur interrupt	0
EXT_INT_3_PEND[0]	[0]	0 = Not occur 1 = Occur interrupt	0

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2.2.61 EXTERN PIN CONFIGURATION REGISTERS IN POWER DOWN MODE

This registers keep their values during power down mode

2.2.61.1 Extern Pin Configuration Registers in Power down Mode (PDNEN, R/W, Address = 0xE020_0F80)

PDNEN	Bit	Description	Initial State
Reserved	[7:2]	Reserved	0
PDNEN_CFG	[1]	0 = Automatically by power down mode 1 = by PDNEN bit	0
PDNEN	[0]	Power down mode pad state enable register. 1 = PADs Controlled by Power Down mode control registers 0 = PADs Controlled by normal mode This bit is set to '1' automaticially when system enters into Power down mode and can be cleared by writing '0' to this bit or cold reset. After wake up from Power down mode, this bit maintains value '1' until writing '0'	0

3 CLOCK CONTROLLER

This chapter describes the clock management unit (CMU) supported by S5PV210. The system controller (SYSCON) manages CMU and power management unit (PMU) in S5PV210.

3.1 CLOCK DOMAINS

S5PV210 consists of three clock domains, namely, main system (MSYS), display system (DSYS), and peripheral system (PSYS), as shown in *Figure 3-1*.

- MSYS domain comprises Cortex A8 processor, DRAM memory controllers (DMC0 and DMC1), 3D, internal SRAM (IRAM, and IROM), INTC, and configuration interface (SPERI). Cortex A8 supports only synchronous mode, and therefore it must operate synchronously with 200MHz AXI buses.
- DSYS domain comprises display related modules, including FIMC, FIMD, JPEG, and multimedia IPs (all other IPs mentioned in X, L, and T blocks), as shown in *Figure 3-1*.
- PSYS domain is used for security, I/O peripherals, and low power audio play.
- Each bus system operates at 200 MHz (maximum), 166 MHz, and 133 MHz, respectively. There are asynchronous bus bridges (BRG) between two different domains.

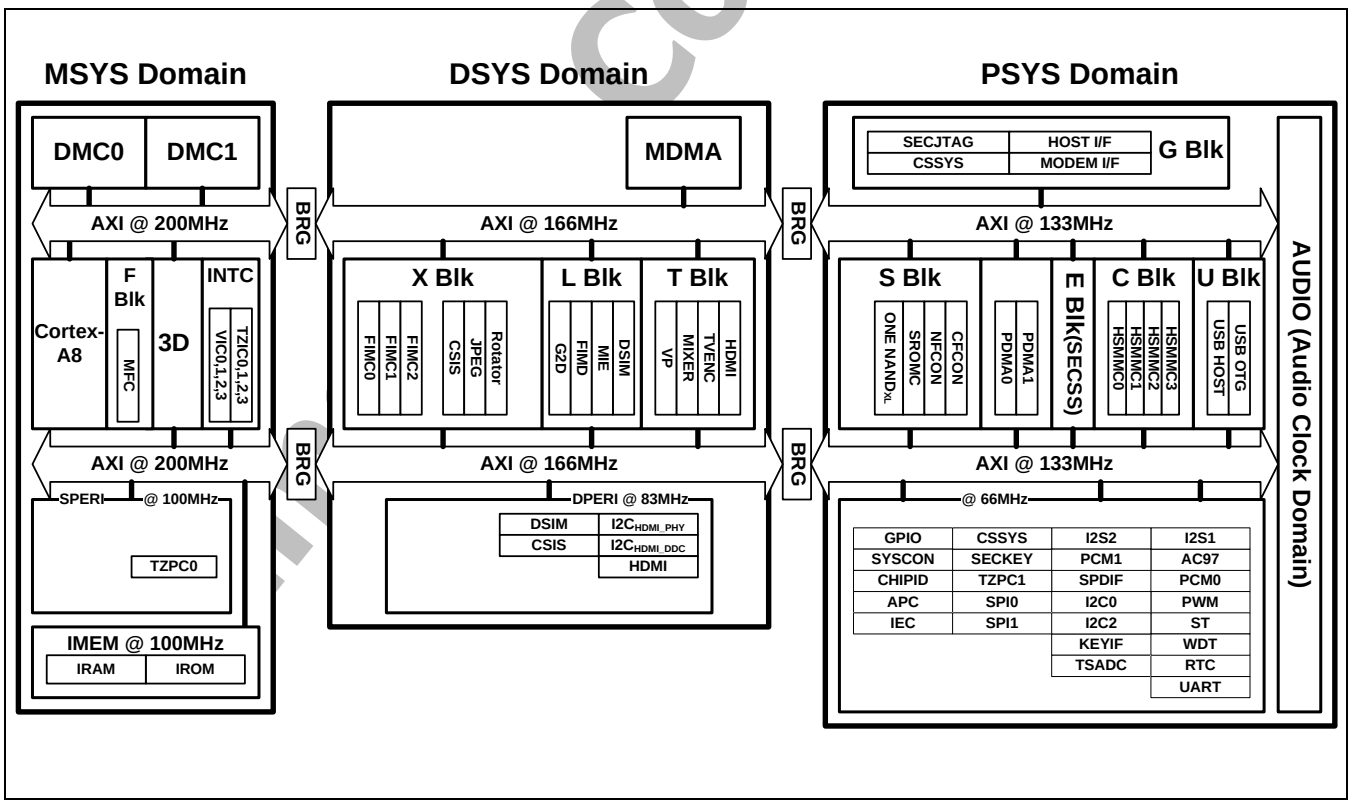

Figure 3-1 S5PV210 Clock Domains

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3.2 CLOCK DECLARATION

Figure 3-2 shows the classification of clocks in S5PV210. The top-level clocks in S5PV210 include:

- Clocks from clock pads, that is, XRTCXTI, XXTI, XUSBXTI, and XHDMIXTI.
- Clocks from CMU (for instance, ARMCLK, HCLK, PCLK, and so on.)
- Clocks from USB PHY
- Clocks from GPIO pads

3.2.1 CLOCKS FROM CLOCK PADS

The following clocks are provided by clock pads. However, you can disable crystal clock pads.

- **XRTCXTI**: Specifies a clock from 32.768 KHz crystal pad with XRTCXTI and XRTCXTO pins. RTC uses this clock as the source of a real-time clock.
- **XXTI**: Specifies a clock from crystal pad with XXTI and XXTO pins. When USB PHY is not used in commercial set, CMU and PLL use this clock to generate other clocks to modules (APLL, MPLL, VPLL, and EPLL.). The input frequency ranges from 12 ~ 50 MHz. It is recommended to use 24MHz crystal because iROM was designed based on the 24MHz input clock.
- **XUSBXTI**: Specifies a clock from a crystal pad with XUSBXTI and XUSBXTO pins. This clock is supplied to APLL, MPLL, VPLL, ELL, and USB PHY. For more information on USB PHY clock, refer to Chapter 8.4 " USB 2.0 HOST Controller " and 8.5 " USB2.0 HS OTG ". It is recommended to use 24MHz crystal because iROM was designed based on the 24MHz input clock.
- **XHDMIXTI**: Specifies a clock from 27MHz crystal pad with XHDMIXTI and XHDMIXTO pins. VPLL or HDMI PHY generates 54MHz clock for TV encoder.

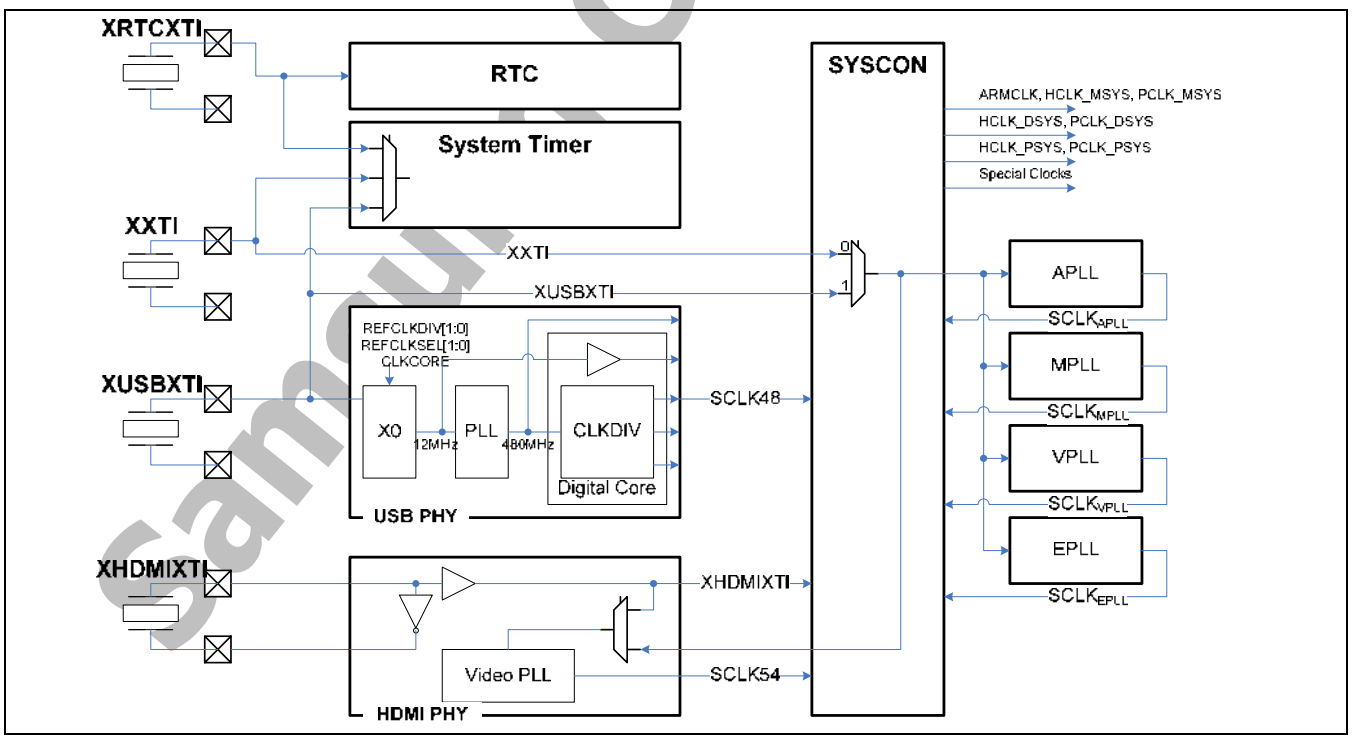

Figure 3-2 S5PV210 Top-Level Clocks

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- XXTI and XXTO use wide-range OSC pads.
- XUSBXTI and XUSBXTO use wide range OSC pads.
- XHDMIXTI and XHDMIXTO use wide range OSC pads.
- XRTCXTI and XRTCXTO use OSC pads for RTC.
- ARMCLK specifies clock for Cortex A8 (up to 1GHz).
- HCLK_MSYS specifies AXI clock for MSYS clock domain, as shown in *Figure 3-1*.
  The maximum operating frequency is up to 200MHz.
- PCLK_MSYS specifies APB clock for MSYS clock domain, as shown in *Figure 3-1*.
  The maximum operating frequency is up to 100MHz.
- HCLK_DSYS specifies AXI/AHB clock for DSYS clock domain, as shown in *Figure 3-1*.
  The maximum operating frequency is up to 166MHz.
- PCLK_DSYS specifies APB clock for DSYS clock domain, as shown in *Figure 3-1*.
  The maximum operating frequency is up to 83 MHz.
- HCLK_PSYS specifies AXI/AHB clock for PSYS clock domain, as shown in *Figure 3-1*.
  The maximum operating frequency is up to 133MHz.
- PCLK_PSYS specifies APB clock for PSYS clock domain, as shown in *Figure 3-1*.
  The maximum operating frequency is up to 66 MHz.
- Special clocks specify all the clocks except bus clock and processor core clock.

3.2.2 CLOCKS FROM CMU

CMU generates internal clocks with intermediate frequencies using clocks from the clock pads (that is, XRTCXTI, XXTI, XUSBXTI, and XHDMIXTI), four PLLs (that is, APLL, MPLL, EPLL, and VPLL), USB PHY and HDMI PHY clock. Some of these clocks can be selected, pre-scaled, and provided to the corresponding modules.

It is recommended to use 24MHz input clock source for APLL, MPLL, EPLL and VPLL.

To generate internal clocks, the following components are used.

- APLL uses FINPLL (refer to *Figure 3-1*) as input to generate 30MHz ~ 1GHz.
- MPLL uses FINPLL as input to generate 50MHz ~ 2GHz.
- EPLL uses FINPLL as input to generate 10MHz ~ 600MHz.
- VPLL uses FINPLL or SCLK_HDMI27M as input to generate 10MHz ~ 600MHz. This PLL generates 54MHz video clock.
- USB OTG PHY uses XUSBXTI to generate 30MHz and 48MHz
- HDMI PHY uses XUSBXTI or XHDMIXTI to generate 54MHz

In typical S5PV210 applications,

- Cortex A8 and MSYS clock domain uses APLL (that is, ARMCLK, HCLK_MSYS, and PCLK_MSYS).
- DSYS and PSYS clock domain (that is, HCLK_DSYS, HCLK_PSYS, PCLK_DSYS, and PCLK_PSYS) and other peripheral clocks (that is, audio IPs, SPI, and so on) use MPLL and EPLL.
- Video clocks uses VPLL.

Clock controller allows bypassing of PLLs for slow clock. It also connects/ disconnects the clock from each block

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(clock gating) using software, resulting in power reduction.

3.3 CLOCK RELATIONSHIP

Clocks have the following relationship:

- MSYS clock domain
  - freq(ARMCLK) = freq(MOUT_MSYS) / n, where n = 1 ~ 8
  - freq(HCLK_MSYS) = freq(ARMCLK) / n, where n = 1 ~ 8
  - freq(PCLK_MSYS) = freq(HCLK_MSYS) / n, where n = 1 ~ 8
  - freq(HCLK_IMEM) = freq(HCLK_MSYS) / 2

- DSYS clock domain
  - freq(HCLK_DSYS) = freq(MOUT_DSYS) / n, where n = 1 ~ 16
  - freq(PCLK_DSYS) = freq(HCLK_DSYS) / n, where n = 1 ~ 8

- PSYS clock domain
  - freq(HCLK_PSYS) = freq(MOUT_PSYS) / n, where n = 1 ~ 16
  - freq(PCLK_PSYS) = freq(HCLK_PSYS) / n, where n = 1 ~ 8
  - freq(SCLK_ONENAND) = freq(HCLK_PSYS) / n, where n = 1 ~ 8

Values for the high-performance operation:

- freq(ARMCLK) = 1000 MHz
- freq(HCLK_MSYS) = 200 MHz
- freq(HCLK_IMEM) = 100 MHz
- freq(PCLK_MSYS) = 100 MHz
- freq(HCLK_DSYS) = 166 MHz
- freq(PCLK_DSYS) = 83 MHz
- freq(HCLK_PSYS) = 133 MHz
- freq(PCLK_PSYS) = 66 MHz
- freq(SCLK_ONENAND) = 133 MHz, 166 MHz

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- PLL
  - APLL can drive MSYS domain and DSYS domain. It can generate up to 1 GHz, 49:51 duty ratio.
  - MPLL can drive MSYS domain and DSYS domain. It supplies clock, up to 2 GHz and 40:60 duty ratio.
  - EPLL is mainly used to generate audio clock.
  - VPLL is mainly used to generate video system operating clock, 54 MHz.
  - Typically, APLL drives MSYS domain and MPLL drives DSYS domain.

NOTE: Although there is the equation for choosing PLL value, we strongly recommend only the values in the PLL value recommendation table. If you have to use other values, please contact us.

3.3.1 RECOMMENDED PLL PMS VALUE FOR APLL

Table 3-1 APLL PMS Value

FIN (MHz)	Target FOUT (MHz)	P	M	S	AFC_ENB	AFC	FVCO (MHz)	FOUT (MHz)
24	800	3	100	1	0	0	1600.000	800.000
24	1000	3	125	1	0	0	2000.000	1000.000

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3.3.2 RECOMMENDED PLL PMS VALUE FOR MPLL

Table 3-2 MPLL PMS Value

FIN (MHz)	Target FOUT (MHz)	VSEL	P	M	S	FVCO (MHz)	FOUT (MHz)
24	133	0	6	266	3	1064.000	133.000
24	166	0	6	332	3	1328.000	166.000
24	266	0	6	266	2	1064.000	266.000
24	333	0	6	333	2	1332.000	333.000
24	667	0	12	667	1	1334.000	667.000

3.3.3 RECOMMENDED PLL PMS VALUE FOR EPLL

Table 3-3 EPLL PMS Value

FIN (MHz)	Target FOUT (MHz)	VSEL	P	M	S	K	FVCO (MHz)	FOUT (MHz)
24	48.0000	0	3	48	3	0	384.000	48.000
24	96.0000	0	3	48	2	0	384.000	96.000
24	144.0000	1	3	72	2	0	576.000	144.000
24	192.0000	0	3	48	1	0	384.000	192.000
24	288.0000	1	3	72	1	0	576.000	288.000
24	84.0000	0	3	42	2	0	336.000	84.000
24	50.0000	0	3	50	3	0	400.000	50.000
24	80.0000	1	3	80	3	0	640.000	80.000
24	32.7680	1	3	65	4	35127	524.28796	32.76800
24	49.1520	0	3	49	3	9961	393.21594	49.15199
24	67.7376	1	3	67	3	48339	541.90076	67.73759
24	73.7280	1	3	73	3	47710	589.82397	73.72800
24	45.1584	0	3	45	3	10381	361.26721	45.15840

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3.3.4 RECOMMENDED PLL PMS VALUE FOR VPLL

Table 3-4 VPLL PMS Value

FIN (MHz)	Target FOUT (MHz)	VSEL	P	M	S	FVCO (MHz)	FOUT (MHz)
24	54.000	0	6	108	3	432.000	54.000
	108.000	0	6	108	2	432.000	108.000
	74.250	1	8	198	3	594.000	74.250
	148.500	1	8	198	2	594.000	148.500
	222.750	0	16	297	1	445.500	222.750
	397.000	0	24	397	0	397.000	397.000
	371.250	0	24	371	0	371.000	371.000
	445.500	0	16	297	0	445.500	445.500
	74.176	1	18	445	3	593.333	74.167
	148.352	1	18	445	2	593.333	148.333
	222.528	0	22	408	1	445.091	222.545
	296.703	1	18	445	1	593.333	296.667
	370.879	0	22	340	0	370.909	370.909
	445.055	0	22	408	0	445.091	445.091
	519.231	1	22	476	0	519.273	519.273
	27.027	0	6	108	4	432.000	27.000
	27.000	0	6	108	4	432.000	27.000
27	54.0000	0	6	96	3	432.000	54.000
	108.000	0	6	96	2	432.000	108.000
	74.2500	1	6	132	3	594.000	74.250
	148.5000	1	6	132	2	594.000	148.500
	222.7500	0	6	99	1	445.500	222.750
	397.0000	0	3	44	0	396.000	396.000
	371.2500	0	4	55	0	371.250	371.250
	445.5000	0	6	99	0	445.500	445.500
	74.1758	1	6	132	3	594.000	74.250
	148.3516	1	6	132	2	594.000	148.500
	222.5275	0	6	99	1	445.500	222.750
	296.7033	1	6	132	1	594.000	297.000
	370.8791	0	11	151	0	370.636	370.636
	445.0549	0	6	99	0	445.500	445.500
	519.2308	1	9	173	0	519.000	519.000

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3.4 CLOCK GENERATION

Figure 3-3 shows block diagram of the clock generation logic. An external crystal clock is connected to the oscillation amplifier. The PLL converts low input frequency to high-frequency clock required by S5PV210. The clock generator block also includes a built-in logic to stabilize the clock frequency after each system reset, since clock takes time before stabilizing.

Figure 3-3 also shows two types of clock mux. Clock mux in grey color represents glitch-free clock mux, which is free of glitches if clock selection is changed. Clock mux in white color represents non-glitch-free clock mux, which can suffer from glitches when changing clock sources. Care must be taken in using each of clock muxes. For glitch-free mux, it should be guaranteed that both of clock sources are running when clock selection is changed from one to the other. If that's not the case, clock changing is not finished fully and resulting clock output can have unknown states. For non-glitch-free clock mux, it is possible to have a glitch when clock selections are changed. To prevent the glitch signals, it is recommended to disable output of non-glitch-free muxes before trying to change clock sources. After clock changing is completed, users can re-enable output of the non-glitch-free clock mux so that there will be no glitches resulting from clock changes. Masking output of non-glitch-free muxes are handled by clock source control registers.

Clock dividers shown in *Figure 3-3* indicates possible dividing value in parentheses. Those diving values can be decided by clock divider registers on run-time. Some clock dividers can only have one dividing value and user cannot change them and does not have corresponding fields in clock divider registers.

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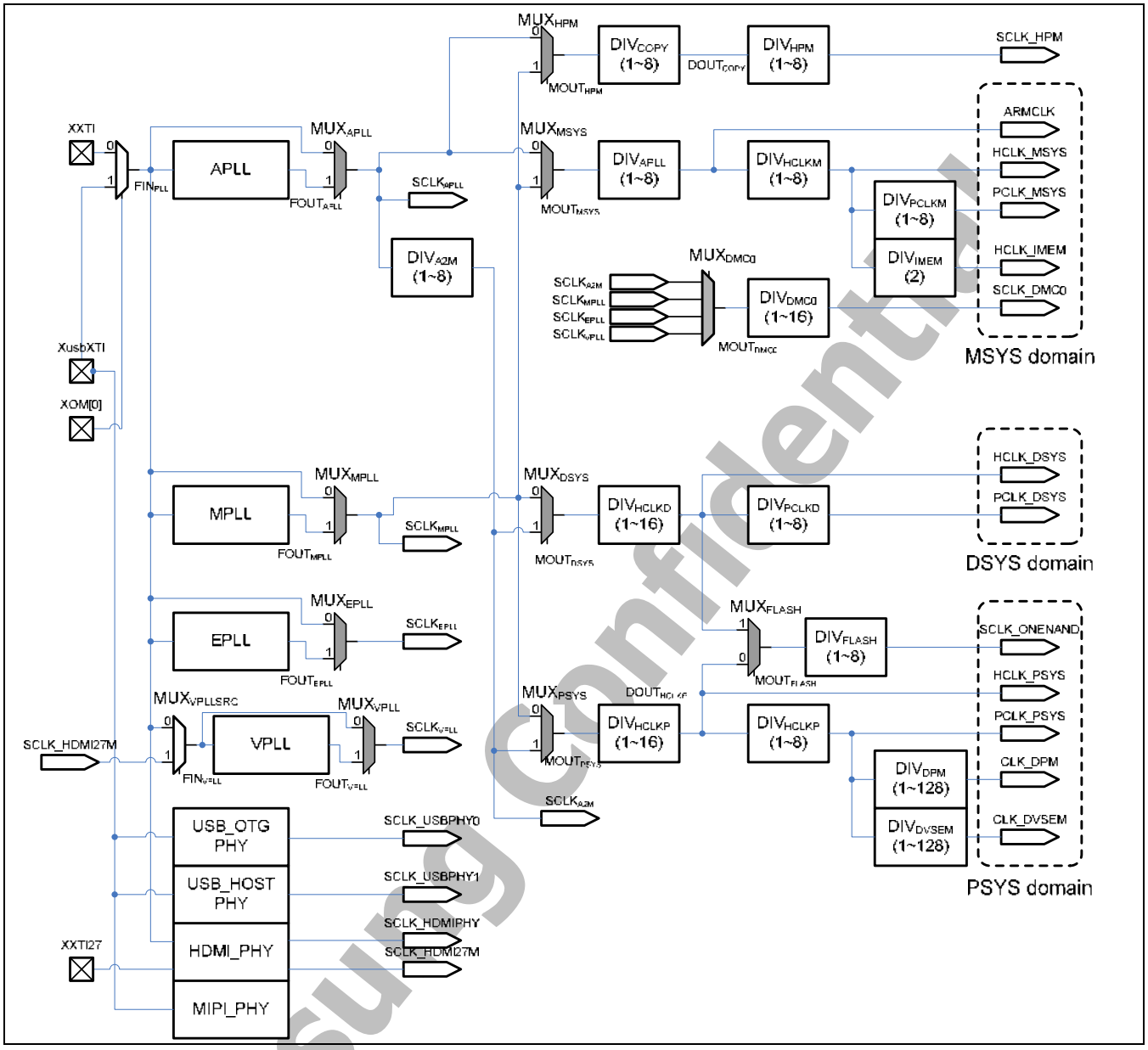

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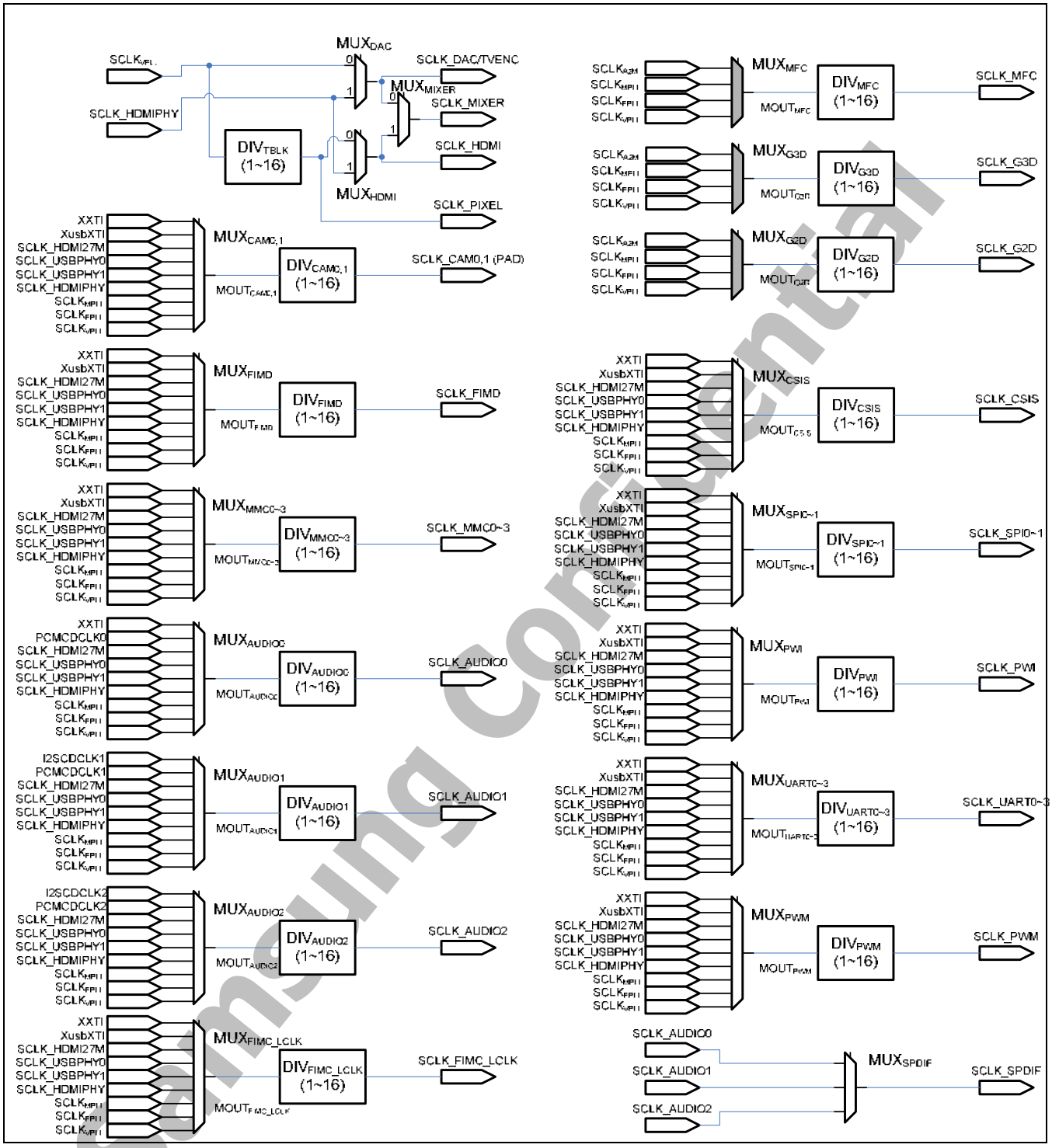

Figure 3-3 S5PV210 Clock Generation Circuit 1

Caution: For glitch-free mux, it should be guaranteed that all of clock sources are running when clock selection is changed from one to the others.

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Table 3-5 Maximum Operating Frequency for Each Sub-block

Clock Domain	Max. Freq.	Module
MSYS	200 MHz	MFC, G3D TZIC0, TZIC1, TZIC2, TZIC3, VIC0, VIC1, VIC2, VIC3 DMC0, DMC1 AXI_MSYS, AXI_MSFR, AXI_MEM
	100 MHz	IRAM, IROM, TZPC0
DSYS	166 MHz	FIMC0, FIMC1, FIMC2, FIMD, DSIM, CSIS, JPEG, Rotator, VP, MIXER, TVENC, HDMI, MDMA, G2D
	83 MHz	DSIM, CSIS, I2C_HDMI_PHY, I2C_HDMI_DDC
PSYS	133 MHz	CSSYS, JTAG, MODEM I/F CFCON, NFCON, SROMC, ONENAND PDMA0, PDMA1 SECSS HSMMC0, HSMMC1, HSMMC2, HSMMC3 USB OTG, USB HOST
	66MHz	SYSCON, GPIO, CHIPID, APC, IEC, TZPC1, SPI0, SPI1, I2S1, I2S2, PCM0, PCM1, PCM2, AC97, SPDIF, I2C0, I2C2, KEYIF, TSADC, PWM, ST, WDT, RTC, UART

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3.5 CLOCK CONFIGURATION PROCEDURE

Rules to follow when the clock configuration changes:

- All inputs of a glitch-free mux must run.
- When a PLL is power-off, you should not select the output of PLL.

Basic SFR configuration flows:

Turn on a PLL

(A,M,E,V)PLL_CON[31] = 1; // Power on a PLL (Refer to (A, M, E, V) PLL_CON SFR)

wait_lock_time; // Wait until the PLL is locked

(A, M, E, V)PLL_SEL = 1; // Select the PLL output clock instead of input reference clock, after PLL output clock is stabilized. (Refer to 0, 4, 8, 12th bit of CLK_SRC0 SFR)

Once you turned on any PLL, do not turn off that.

Change PLL's PMS values

Set PMS values; // Set PDIV, MDIV, and SDIV values (Refer to (A, M, E, V) PLL_CON SFR)

Change the system clock divider values

CLK_DIV0 [31:0] = target value0;

Change the divider values for special clocks

CLK_DIV1 [31:0] = target value1;

CLK_DIV2 [31:0] = target value2;

3.5.1 CLOCK GATING

S5PV210 can disable the clock operation of each IP if it is not required. This reduces dynamic power.

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3.6 SPECIAL CLOCK DESCRIPTION

3.6.1 SPECIAL CLOCK TABLE

Table 3-6 Special Clocks in S5PV210

Name	Description	Range	Source
SCLK_ONENAND	ONENAND operating clock	~166 MHz (SCLK_ONENAND)	HCLK_DSYS, HCLK_PSYS
SCLK_G3D	G3D core operating clock	~200 MHz	SCLKA2M, SCLKMPLL, SCLKEPLL, SCLKVPLL
SCLK_G2D	G2D core operating clock	~223 MHz	SCLKA2M, SCLKMPLL, SCLKEPLL, SCLKVPLL
SCLK_MFC	MFC core operating clock	~200 MHz	SCLKA2M, SCLKMPLL, SCLKEPLL, SCLKVPLL
SCLK_CAM0,1	Reference clock for external CAM device	CAM spec	All possible clock sources
SCLK_FIMD	FIMD operating clock	~166MHz	All possible clock sources
SCLK_TVENC	TVENC/ DAC clock	54 MHz	SCLKVPLL, HDMI PHY output
SCLK_DAC	DAC clock	54 MHz	SCLKVPLL, HDMI PHY output
SCLK_MIXER	MIXER clock	54MHz (TV) ~148.5MHz (HDMI)	SCLKVPLL, HDMI PHY output
SCLK_HDMI	HDMI LINK clock	~148.5MHz	All possible clock sources
SCLK_PIXEL	HDMI PIXEL clock	~148.5MHz	All possible clock sources
SCLK_SPDIF	SPDIF operating clock	~83MHz	SCLK_AUDIO0~2
SCLK_MMC0,1,2,3	HSMMC operating clock	~52MHz	All possible clock sources
SCLK_USBPHY0	USB OTG clock	48MHz	USB OTG PHY clock out
SCLK_USBPHY1	USB HOST clock	48MHz	USB HOST PHY clock out
SCLK_AUDIO0,1,2	AUDIO operating clock (PCM, I2S)	~83MHz	All possible clock sources
SCLK_PWI	IEM APC operating clock	6~30MHz	All possible clock sources
SCLK_SRCLK	KEY I/F or TSADC filter clock	~24MHz	XXTI, XUSBXTI
SCLK_SPI0,1	SPI operating clock	~100MHz	All possible clock sources
SCLK_UART0,1,2,3	UART operating clock	~200MHz	All possible clock sources

All possible clock sources include XXTI, XUSBXTI, SCLK_HDMI27M, SCLK_USBPHY, SCLK_HDMIPHY, SCLKMPLL, SCLKEPLL, and SCLKVPLL.

XXTI and XUSBXTI mean external crystal, respectively.

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SCLK_USBPHY means USB PHY 48 MHz output clock.

SCLK_HDMI27M means HDMI PHY (27 MHz reference clock for HDMI) output.

SCLK_HDMIPHY means HDMI PHY (PIXEL_CLKO) output clock.

SCLKMPLL, SCLKEPLL, and SCLKVPLL mean output clock of MPLL, EPLL and VPLL, respectively.

Table 3-7 I/O Clocks in S5PV210

Name	I/O	Pin name	GPIO function	Range	Description
IOCLK_AC97	IN	Xi2s1SCLK	Func2 : AC97BITCLK	12.288MHz	AC97 bit clock
IOCLK_I2S0,1,2	IN	Xi2s0CDCLK Xi2s1CDCLK Xpcm2EXTCLK	Func0 : I2S_0_CDCLK Func0 : I2S_1_CDCLK Func2 : I2S_2_CDCLK	~83.4MHz	I2S CODEC clock
IOCLK_PCM0,1,2	IN	Xi2s0CDCLK Xi2s1CDCLK Xpcm2EXTCLK	Func1 : PCM_0_EXTCLK Func1 : PCM_1_EXTCLK Func0 : PCM_2_EXTCLK	~83.4MHz	PCM CODEC clock
IOCLK_SPDIF	IN	Xpcm2EXTCLK	Func1 : SPDIF_EXTCLK	36.864MHz	SPDIF input clock

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3.7 REGISTER DESCRIPTION

System controller controls PLL, clock generator, the power management unit (PMU), and other system dependent units. This section describes how to control these parts using Special Functional Register (SFR) within the system controller. Do not change any reserved area. Changing value of Reserved area can lead to undefined behavior.

3.7.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
APLL_LOCK	0xE010_0000	R/W	Control PLL locking period for APLL.	0x0000_0FFF
Reserved	0xE010_0004	-	Reserved	-
MPLL_LOCK	0xE010_0008	R/W	Control PLL locking period for MPLL.	0x0000_0FFF
Reserved	0xE010_000C	-	Reserved	-
EPLL_LOCK	0xE010_0010	R/W	Control PLL locking period for EPLL.	0x0000_0FFF
Reserved	0xE010_0014~ 0xE010_001C	-	Reserved	-
VPLL_LOCK	0xE010_0020	R/W	Control PLL locking period for VPLL.	0x0000_0FFF
Reserved	0xE010_0024~ 0xE010_00FC	-	Reserved	-
APLL_CON0	0xE010_0100	R/W	Control PLL output frequency for APLL.	0x00C8_0301
APLL_CON1	0xE010_0104	R/W	Control PLL AFC (Adaptive Frequency Calibrator)	0x0000_0000
MPLL_CON	0xE010_0108	R/W	Control PLL output frequency for MPLL.	0x014D_0301
Reserved	0xE010_010C	-	Reserved	-
EPLL_CON0	0xE010_0110	R/W	Control PLL output frequency for EPLL.	0x0885_0302
EPLL_CON1	0xE010_0114	R/W	Control PLL output frequency for EPLL.	0x0000_0000
Reserved	0xE010_0118~ 0xE010_011C	-	Reserved	-
VPLL_CON	0xE010_0120	R/W	Control PLL output frequency for VPLL.	0x006C_0303
Reserved	0xE010_0124~ 0xE010_01FC	-	Reserved	-
CLK_SRC0	0xE010_0200	R/W	Select clock source 0 (Main)	0x0000_0000
CLK_SRC1	0xE010_0204	R/W	Select clock source 1 (Multimedia)	0x0000_0000
CLK_SRC2	0xE010_0208	R/W	Select clock source 2 (Multimedia)	0x0000_0000
CLK_SRC3	0xE010_020C	R/W	Select clock source 3 (Multimedia)	0x0000_0000
CLK_SRC4	0xE010_0210	R/W	Select clock source 4 (Connectivity)	0x0000_0000
CLK_SRC5	0xE010_0214	R/W	Select clock source 5 (Connectivity)	0x0000_0000
CLK_SRC6	0xE010_0218	R/W	Select clock source 6 (Audio)	0x0000_0000
Reserved	0xE010_021C~ 0xE010_027C	-	Reserved	-
CLK_SRC_MASK0	0xE010_0280	R/W	Clock source mask 0	0xFFFF_FFFF

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Register	Address	R/W	Description	Reset Value
CLK_SRC_MASK1	0xE010_0284	R/W	Clock source mask 1	0xFFFF_FFFF
Reserved	0xE010_0288~ 0xE010_02FC	-	Reserved	-
CLK_DIV0	0xE010_0300	R/W	Set clock divider ratio 0 (System Clocks)	0x0000_0000
CLK_DIV1	0xE010_0304	R/W	Set clock divider ratio 1 (Multimedia)	0x0000_0000
CLK_DIV2	0xE010_0308	R/W	Set clock divider ratio 2 (Multimedia)	0x0000_0000
CLK_DIV3	0xE010_030C	R/W	Set clock divider ratio 3 (Multimedia)	0x0000_0000
CLK_DIV4	0xE010_0310	R/W	Set clock divider ratio 4 (Connectivity)	0x0000_0000
CLK_DIV5	0xE010_0314	R/W	Set clock divider ratio 5 (Connectivity)	0x0000_0000
CLK_DIV6	0xE010_0318	R/W	Set clock divider ratio 6 (Audio & Others)	0x0000_0000
CLK_DIV7	0xE010_031C	R/W	Set clock divider ratio 7 (IEM_IEC)	0x0000_0000
Reserved	0xE010_0320~ 0xE010_0440	-	Reserved	-
CLK_GATE_SCLK	0xE010_0444	R/W	Control special clock gating	0xFFFF_FFFF
Reserved	0xE010_0448~ 0xE010_045C	-	Reserved	-
CLK_GATE_IP0	0xE010_0460	R/W	Control IP clock gating	0xFFFF_FFFF
CLK_GATE_IP1	0xE010_0464	R/W	Control IP clock gating	0xFFFF_FFFF
CLK_GATE_IP2	0xE010_0468	R/W	Control IP clock gating	0xFFFF_FFFF
CLK_GATE_IP3	0xE010_046C	R/W	Control IP clock gating	0xFFFF_FFFF
CLK_GATE_IP4	0xE010_0470	R/W	Control IP clock gating	0xFFFF_FFFF
Reserved	0xE010_0474~ 0xE010_047C	-	Reserved	-
CLK_GATE_BLOCK	0xE010_0480	R/W	Control block clock gating	0xFFFF_FFFF
CLK_GATE_IP5	0xE010_0484	R/W	Control IP clock gating	0xFFFF_FFFF
Reserved	0xE010_0488~ 0xE010_04FC	-	Reserved	-
CLK_OUT	0xE010_0500	R/W	Select clock output	0x0000_0000
Reserved	0xE010_0504~ 0xE010_0FFC	-	Reserved	-
CLK_DIV_STAT0	0xE010_1000	R	Clock divider status (CLK_DIV0~3)	0x0000_0000
CLK_DIV_STAT1	0xE010_1004	R	Clock divider status 1 (CLK_DIV4~5)	0x0000_0000
Reserved	0xE010_1008~ 0xE010_10FC	-	Reserved	-
CLK_MUX_STAT0	0xE010_1100	R	Clock MUX status 0	0x1111_1111
CLK_MUX_STAT1	0xE010_1104	R	Clock MUX status 1	0x0001_0000
Reserved	0xE010_1108~ 0xE010_1FFC	-	Reserved	-
SWRESET	0xE010_2000	R/W	Generate software reset	0x0000_0000

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Register	Address	R/W	Description	Reset Value
Reserved	0xE010_2004~ 0xE010_2FFC	-	Reserved	-
DCGIDX_MAP0	0xE010_3000	R/W	DCG index map 0	0xFFFF_FFFF
DCGIDX_MAP1	0xE010_3004	R/W	DCG index map 1	0xFFFF_FFFF
DCGIDX_MAP2	0xE010_3008	R/W	DCG index map 2	0xFFFF_FFFF
Reserved	0xE010_300C~ 0xE010_301C	-	Reserved	-
DCGPERF_MAP0	0xE010_3020	R/W	DCG performance map 0	0xFFFF_FFFF
DCGPERF_MAP1	0xE010_3024	R/W	DCG performance map 1	0xFFFF_FFFF
Reserved	0xE010_3028~ 0xE010_303C	-	Reserved	-
DVCIDX_MAP	0xE010_3040	R/W	DVC index map	0x00FF_FFFF
Reserved	0xE010_3044~ 0xE010_305C	-	Reserved	-
FREQ_CPU	0xE010_3060	R/W	Maximum frequence of CPU	0x0000_0000
FREQ_DPM	0xE010_3064	R/W	Frequency of DPM accumulators	0x0000_0000
Reserved	0xE010_3068~ 0xE010_307C	-	Reserved	-
DVSEMCLK_EN	0xE010_3080	R/W	DVS emulation clock enable	0x0000_0000
MAXPERF	0xE010_3084	R/W	MAX performance enable	0x0000_0000
Reserved	0xE010_3088~ 0xE010_30FC	-	Reserved	-
APLL_CON0_L8	0xE010_3100	R/W	APLL control (performance level-8)	0x00C8_0301
APLL_CON0_L7	0xE010_3104	R/W	APLL control (performance level-7)	0x00C8_0301
APLL_CON0_L6	0xE010_3108	R/W	APLL control (performance level-6)	0x00C8_0301
APLL_CON0_L5	0xE010_310C	R/W	APLL control (performance level-5)	0x00C8_0301
APLL_CON0_L4	0xE010_3110	R/W	APLL control (performance level-4)	0x00C8_0301
APLL_CON0_L3	0xE010_3114	R/W	APLL control (performance level-3)	0x00C8_0301
APLL_CON0_L2	0xE010_3118	R/W	APLL control (performance level-2)	0x00C8_0301
APLL_CON0_L1	0xE010_311C	R/W	APLL control (performance level-1)	0x00C8_0301
Reserved	0xE010_3120~ 0xE010_31FC	-	Reserved	-
CLKDIV_IEM_L8	0xE010_3200	R/W	Clock divider for IEM (performance level-8)	0x0000_0000
CLKDIV_IEM_L7	0xE010_3204	R/W	Clock divider for IEM (performance level-7)	0x0000_0000
CLKDIV_IEM_L6	0xE010_3208	R/W	Clock divider for IEM (performance level-6)	0x0000_0000
CLKDIV_IEM_L5	0xE010_320C	R/W	Clock divider for IEM (performance level-5)	0x0000_0000

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Register	Address	R/W	Description	Reset Value
CLKDIV_IEM_L4	0xE010_3210	R/W	Clock divider for IEM (performance level-4)	0x0000_0000
CLKDIV_IEM_L3	0xE010_3214	R/W	Clock divider for IEM (performance level-3)	0x0000_0000
CLKDIV_IEM_L2	0xE010_3218	R/W	Clock divider for IEM (performance level-2)	0x0000_0000
CLKDIV_IEM_L1	0xE010_321C	R/W	Clock divider for IEM (performance level-1)	0x0000_0000
Reserved	0xE010_3220~ 0xE010_32FC	-	Reserved	-
APLL_CON1_L8	0xE010_3300	R/W	Control PLL AFC (performance level-1)	0x0000_0000
APLL_CON1_L7	0xE010_3304	R/W	Control PLL AFC (performance level-7)	0x0000_0000
APLL_CON1_L6	0xE010_3308	R/W	Control PLL AFC (performance level-6)	0x0000_0000
APLL_CON1_L5	0xE010_330C	R/W	Control PLL AFC (performance level-5)	0x0000_0000
APLL_CON1_L4	0xE010_3310	R/W	Control PLL AFC (performance level-4)	0x0000_0000
APLL_CON1_L3	0xE010_3314	R/W	Control PLL AFC (performance level-3)	0x0000_0000
APLL_CON1_L2	0xE010_3318	R/W	Control PLL AFC (performance level-2)	0x0000_0000
APLL_CON1_L1	0xE010_331C	R/W	Control PLL AFC (performance level-1)	0x0000_0000
Reserved	0xE010_3320~ 0xE010_60FC	-	Reserved	-
GENERAL_CTRL	0xE010_6100		General Control Register	0x0000_0001
Reserved	0xE010_6104~ 0xE010_7004		Reserved	-
DISPLAY_CONTROL	0xE010_7008	R/W	Display output path selection.	0x0000_0000
AUDIO_ENDIAN	0xE010_700C	R/W	Endian selection for audio subsystem	0x0000_0000

SFRs consist of several parts.

The SFRs with address 0xE010_0XXX controls clock-related logics. They control the output frequency of three PLLs, clock source selection, clock divider ratio, and clock gating.

The SFRs with address 0xE010_2XXX controls SW reset.

The SFRs with address 0xE010_3XXX controls IEM block.

The SFRs with address 0xE010_6XXX controls S5PV210 system.

The SFRs with address 0xE010_7XXX include miscellaneous registers.

The SFRs with address 0xE010_8XXX controls the power management block.

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S5PV210 has four internal PLLs, namely, APLL, MPLL, EPLL, and VPLL. The four internal PLLs are controlled by the following eight special registers:

3.7.2 PLL CONTROL REGISTERS

3.7.2.1 PLL Control Registers (APLL_LOCK / MPLL_LOCK / EPLL_LOCK / VPLL_LOCK)

- (APLL_LOCK, R/W, Address = 0xE010_0000)
- (MPLL_LOCK, R/W, Address = 0xE010_0008)
- (EPLL_LOCK, R/W, Address = 0xE010_0010)
- (VPLL_LOCK, R/W, Address = 0xE010_0020)

A PLL requires locking period when input frequency is changed or frequency division (multiplication) values are changed. PLL_LOCK register specifies this locking period, which is based on PLL's source clock. During this period, output will be low state.

APLL_LOCK / MPLL_LOCK / EPLL_LOCK / VPLL_LOCK	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0000
PLL_LOCKTIME	[15:0]	Required period to generate a stable clock output This count is based on PLL's source clock. - FINPLL for APLL, MPLL, EPLL - FINVPLL for VPLL Refer to *Figure 3-3*	0x0FFF

Lock time of PLL is related Fref which is FIN / PDIV.

1) Lock time of APLL is changed as the frequency of Fref. :
   <30us @ Fref=6MHz/8MHz, <40us @ Fref=4MHz, <60us @ Fref=2MHz, <100us @ Fref=1MHz
2) Lock time of MPLL and VPLL is maximum 400 cycles of Fref.
   100us @ Fref=4Mhz, 200us @ Fref=2MHz, 400us @ Fref=1MHz
3) Lock time of EPLL is maximum 3000 cycles of Fref.
   125us @ Fref=24Mhz, 375us @ Fref=8MHz, 750us @ Fref=4MHz

The following example shows the lock time setting for recommended PMS value of each PLL.

FIN (MHz)	Target FOUT (MHz)	PLL	P	M	S	K	Fref (MHz)	Lock time (us)
24	1000.0000	APLL	3	125	1	-	8	30
24	667.0000	MPLL	12	667	1	-	2	200
24	96.0000	EPLL	3	48	2	0	8	375
24	54.0000	VPLL	6	108	3	-	4	100

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PLL_CON register controls the operation of each PLL. If ENABLE bit is set, the corresponding PLL generates output after PLL locking period. The MDIV, PDIV, and SDIV values control the output frequency of PLL. The PLL also generates the output frequency when MDIV, PDIV, and VSEL are changed. However, the PLL locking period is not applied if only SDIV is changed. PLL Control Registers (APLL_CON0/APLL_CON1, R/W, Address = 0xE010_0100/0xE010_0104)

APLL_CON0	Bit	Description	Initial State
ENABLE	[31]	PLL enable control (0: disable, 1: enable)	0
Reserved	[30]	Reserved	0
LOCKED	[29]	PLL locking indication 0 = Unlocked 1 = Locked Read Only	0
Reserved	[28:26]	Reserved	0x0
MDIV	[25:16]	PLL M divide value	0xC8
Reserved	[15:14]	Reserved	0
PDIV	[13:8]	PLL P divide value	0x3
Reserved	[7:3]	Reserved	0
SDIV	[2:0]	PLL S divide value	0x1

The reset value of APLL_CON0 generates 800 MHz output clock, if the input clock frequency is 24 MHz.

Equation to calculate the output frequency:

FOUT = MDIV X FIN / (PDIV $\times$ 2^{SDIV-1})

where, MDIV, PDIV, SDIV for APLL and MPLL must meet the following conditions :

PDIV: 1 $\leq$ PDIV $\leq$ 63
MDIV: 64 $\leq$ MDIV $\leq$ 1023
SDIV: 1 $\leq$ SDIV $\leq$ 5
Fref (=FIN / PDIV): 1MHz $\leq$ Fref $\leq$ 12MHz

FVCO (=2 $\times$ MDIV $\times$ FIN / PDIV): 1000MHz $\leq$ FVCO $\leq$ 2060MHz

Refer to *3.3.1 Recommended PLL PMS Value for APLL* for recommended PMS values.

Caution: APLL should be turned on before entering following low-power modes. Deep idle, stop, deep stop, sleep mode. APLL will be automatically turned off while entering those low-power modes.

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APLL_CON1	Bit	Description	Initial State
AFC_ENB	[31]	Decides whether AFC is enabled or not. Active low. 0 : Enable 1 : Disable AFC selects adaptive frequency curve of VCO for wide range, high phase noise (or jitter) and fast lock time. Users should refer to *3.3.1* on whether to use AFC for a given P/M/S values.	0x0
Reserved	[30:5]	Reserved	0x0
AFC	[4:0]	AFC value. If user disable the AFC, this value should be set manually. Users should refer to *3.3.1* on the recommended AFC value for a given scenario.	0x0

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3.7.2.2 PLL Control Registers (MPLL_CON, R/W, Address = 0xE010_0108)

MPLL_CON	Bit	Description	Initial State
ENABLE	[31]	PLL enable control (0: disable, 1: enable)	0
Reserved	[30]	Reserved	0
LOCKED	[29]	PLL locking indication 0 = Unlocked 1 = Locked Read Only	0
Reserved	[28]	Reserved	0
VSEL	[27]	VCO frequency range selection	0x0
Reserved	[26]	Reserved	0
MDIV	[25:16]	PLL M divide value	0x14D
Reserved	[15:14]	Reserved	0
PDIV	[13:8]	PLL P divide value	0x3
Reserved	[7:3]	Reserved	0
SDIV	[2:0]	PLL S divide value	0x1

The reset value of MPLL_CON generates 667 MHz output clock respectively, if the input clock frequency is 24 MHz.

Equation to calculate the output frequency:

FOUT = MDIV X FIN / (PDIV X 2^{SDIV})

where, MDIV, PDIV, SDIV for APLL and MPLL must meet the following conditions :

PDIV: $1 \leq PDIV \leq 63$

MDIV: $16 \leq MDIV \leq 1023$

SDIV: $0 \leq SDIV \leq 5$

Fref (=FIN / PDIV): $1MHz \leq Fref \leq 10MHz$

FVCO (=MDIV X FIN / PDIV):

$1000MHz \leq FVCO \leq 1400MHz$ when VSEL=LOW.

$1400MHz \leq FVCO \leq 2000MHz$ when VSEL=HIGH.

FOUT: $32MHz \leq FOUT \leq 2000MHz$

Refer to *3.3.2 Recommended PLL PMS Value for MPLL* for recommended PMS values.

Caution: MPLL should be turned on before entering following low-power modes. Deep idle, stop, deep stop, sleep mode. MPLL will be automatically turned off while entering those low-power modes.

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3.7.2.3 PLL Control Registers (EPLL_CON0/ EPLL_CON1, R/W, Address = 0xE010_0110/0xE010_0114)

EPLL_CON0	Bit	Description	Initial State
ENABLE	[31]	PLL enable control (0: disable, 1: enable)	0x0
Reserved	[30]	Reserved	0x0
LOCKED	[29]	PLL locking indication 0 = Unlocked 1 = Locked Read Only	0x0
Reserved	[28]	Reserved	0x0
VSEL	[27]	VCO frequency range selection	0x1
Reserved	[26:25]	Reserved	0x0
MDIV	[24:16]	PLL M divide value	0x85
Reserved	[15:14]	Reserved	0x0
PDIV	[13:8]	PLL P divide value	0x3
Reserved	[7:3]	Reserved	0x0
SDIV	[2:0]	PLL S divide value	0x2

EPLL_CON1	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0
K	[15:0]	PLL K value. K value is used to fine-tune M divider value to meet FOUT requirement exactly. For this purpose, MDIV+K/65536 is used for M divider value. Also called as DSM (Delta-Sigma Modulator).	0x0

The reset value of EPLL_CON generates 133 MHz output clock respectively, if the input clock frequency is 24 MHz.

Equation to calculate the output frequency:

FOUT = (MDIV+K/65536) X FIN / (PDIV X 2^{SDIV})

where, MDIV, PDIV, SDIV for PLLs must meet the following conditions :

PDIV: $1 \leq PDIV \leq 63$
MDIV: $16 \leq MDIV \leq 511$
SDIV: $0 \leq SDIV \leq 5$
K: $0 \leq SDIV \leq 65535$
Fref (=FIN / PDIV): $4MHz \leq Fref \leq 30MHz$

FVCO (=MDIV X FIN / PDIV):
$330MHz \leq FVCO \leq 460MHz$ when VSEL=LOW.

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460MHz ≤ FVCO ≤ 660MHz when VSEL=HIGH.

FOUT: 12MHz ≤ FOUT ≤ 660MHz

Don't set the value PDIV or MDIV to all zeros.

Refer to *3.3.3 Recommended PLL PMS Value for EPLL* for recommended PMS values.

Caution: EPLL should be turned on before entering following low-power modes. Deep idle, stop, deep stop, sleep mode. EPLL will be automatically turned off while entering those low-power modes.

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3.7.2.4 PLL Control Registers (VPLL_CON, R/W, Address = 0xE010_0120)

VPLL_CON	Bit	Description	Initial State
ENABLE	[31]	PLL enable control (0: disable, 1: enable)	0
Reserved	[30]	Reserved	0
LOCKED	[29]	PLL locking indication 0 = Unlocked 1 = Locked Read Only	0
Reserved	[28]	Reserved	0
VSEL	[27]	VCO frequency range selection	0x0
Reserved	[26:25]	Do not change	0
MDIV	[24:16]	PLL M divide value	0x6C
Reserved	[15:14]	Reserved	0
PDIV	[13:8]	PLL P divide value	0x3
Reserved	[7:3]	Reserved	0
SDIV	[2:0]	PLL S divide value	0x3

The reset value of VPLL_CON generates 54 MHz output clock respectively, if the input clock frequency is 24 MHz.

Equation to calculate the output frequency:

FOUT = MDIV X FIN / (PDIV X 2^{SDIV})

where, MDIV, PDIV, SDIV for PLLs must meet the following conditions :

PDIV: $1 \leq PDIV \leq 63$

MDIV: $16 \leq MDIV \leq 511$

SDIV: $0 \leq SDIV \leq 5$

Fref (=FIN / PDIV): $1MHz \leq Fref \leq 10MHz$

FVCO (=MDIV X FIN / PDIV):

$330MHz \leq FVCO \leq 460MHz$ when VSEL=LOW.

$460MHz \leq FVCO \leq 660MHz$ when VSEL=HIGH.

FOUT : $12MHz \leq FOUT \leq 660MHz$

Refer to *3.3.4 Recommended PLL PMS Value for VPLL* for recommended PMS values.

Caution: VPLL should be turned on before entering following low-power modes. Deep idle, stop, deep stop, sleep mode. VPLL will be automatically turned off while entering those low-power modes.

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3.7.3 CLOCK SOURCE CONTROL REGISTERS

S5PV210 has many clock sources, which include four PLL outputs, the external oscillator, the external clock, and other clock sources from GPIO. CLK_SRCn registers control the source clock of each clock divider.

3.7.3.1 Clock Source Control Registers (CLK_SRC0, R/W, Address = 0xE010_0200)

CLK_SRC0	Bit	Description	Initial State
Reserved	[31:29]	Reserved	0x0
ONENAND_SEL	[28]	Control MUXFLASH (0:HCLK_PSYS, 1:HCLK_DSYS)	0
Reserved	[27:25]	Reserved	0x0
MUX_PSYS_SEL	[24]	Control MUX_PSYS (0:SCLKMPLL, 1:SCLKA2M)	0
Reserved	[23:21]	Reserved	0x0
MUX_DSYS_SEL	[20]	Control MUX_DSYS (0:SCLKMPLL, 1:SCLKA2M)	0
Reserved	[19:17]	Reserved	0x0
MUX_MSYS_SEL	[16]	Control MUX_MSYS (0:SCLKAPLL, 1:SCLKMPLL)	0
Reserved	[15:13]	Reserved	0x0
VPLL_SEL	[12]	Control MUXVPLL (0: FINVPLL, 1: FOUTVPLL)	0
Reserved	[11:9]	Reserved	0x0
EPLL_SEL	[8]	Control MUXEPLL (0:FINPLL, 1:FOUTEPLL)	0
Reserved	[7:5]	Reserved	0x0
MPLL_SEL	[4]	Control MUXMPLL (0:FINPLL, 1:FOUTMPLL)	0
Reserved	[3:1]	Reserved	0x0
APLL_SEL	[0]	Control MUXAPLL (0:FINPLL, 1:FOUTAPLL)	0

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3.7.3.2 Clock Source Control Registers (CLK_SRC1, R/W, Address = 0xE010_0204)

CLK_SRC1	Bit	Description	Initial State
Reserved	[31:29]	Reserved	0x0
VPLLSRC_SEL	[28]	Control MUXVPLLSRC, which is the source clock of VPLL (0: FINPLL, 1: SCLK_HDMI27M)	0x0
CSIS_SEL	[27:24]	Control MUXCSIS, which is the source clock of CSIS (0000: XXTI, 0001: XusbXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
FIMD_SEL	[23:20]	Control MUXFIMD, which is the source clock of FIMD (0000: XXTI, 0001: XusbXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
CAM1_SEL	[19:16]	Control MUXCAM1, which is the source clock of CAM0 (0000: XXTI, 0001: XusbXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
CAM0_SEL	[15:12]	Control MUXCAM0, which is the source clock of CAM0 (0000: XXTI, 0001: XusbXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
Reserved	[11:9]	Reserved	0x0
DAC_SEL	[8]	Control MUXDAC, which is the source clock of TVENC and DAC (0:SCLKVPLL, 1: SCLK_HDMIPHY)	0x0
Reserved	[7:5]	Reserved	0x0
MIXER_SEL	[4]	Control MUXMIXER, which is the source clock of MIXER (0:SCLK_DAC, 1: SCLK_HDMI)	0x0
Reserved	[3:1]	Reserved	0x0
HDMI_SEL	[0]	Control MUXHDMI, which is the source clock of HDMI link (0:SCLK_PIXEL, 1: SCLK_HDMIPHY)	0x0

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3.7.3.3 Clock Source Control Registers (CLK_SRC2, R/W, Address = 0xE010_0208)

CLK_SRC2	Bit	Description	Initial State
Reserved	[31:10]	Reserved	0x0
G2D_SEL	[9:8]	Control MUXG2D, which is the source clock of G2D core (00:SCLKA2M, 01:SCLKMPLL, 10:SCLKEPLL, 11:SCLKVPLL)	0x0
Reserved	[7:6]	Reserved	0x0
MFC_SEL	[5:4]	Control MUXMFC, which is the source clock of MFC core (00:SCLKA2M, 01:SCLKMPLL, 10:SCLKEPLL, 11:SCLKVPLL)	0x0
Reserved	[3:2]	Reserved	0x0
G3D_SEL	[1:0]	Control MUXG3D, which is the source clock of G3D core (00:SCLKA2M, 01:SCLKMPLL, 10:SCLKEPLL, 11:SCLKVPLL)	0x0

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3.7.3.4 Clock Source Control Registers (CLK_SRC3, R/W, Address = 0xE010_020C)

CLK_SRC3	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
FIMC_LCLK_SEL	[23:20]	Control MUXFIMC_LCLK, which is the source clock of FIMC2 local clock (0000: XXTI, 0001: XUSBXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
F1	[19:16]	Should have same value as FIMC_LCLK_SEL	0x0
F0	[15:12]	Should have same value as FIMC_LCLK_SEL	0x0
Reserved	[11:0]	Reserved	0x0

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3.7.3.5 Clock Source Control Registers (CLK_SRC4, R/W, Address = 0xE010_0210)

CLK_SRC4	Bit	Description	Initial State
UART3_SEL	[31:28]	Control MUXUART3, which is the source clock of UART3 (0000: XXTI, 0001: XUSBXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
UART2_SEL	[27:24]	Control MUXUART2, which is the source clock of UART2 (0000: XXTI, 0001: XUSBXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
UART1_SEL	[23:20]	Control MUXUART1, which is the source clock of UART1 (0000: XXTI, 0001: XUSBXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
UART0_SEL	[19:16]	Control MUXUART0, which is the source clock of UART0 (0000: XXTI, 0001: XUSBXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
MMC3_SEL	[15:12]	Control MUXMMC3, which is the source clock of MMC3 (0000: XXTI, 0001: XUSBXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
MMC2_SEL	[11:8]	Control MUXMMC2, which is the source clock of MMC2 (0000: XXTI, 0001: XUSBXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
MMC1_SEL	[7:4]	Control MUXMMC1, which is the source clock of MMC1 (0000: XXTI, 0001: XUSBXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
MMC0_SEL	[3:0]	Control MUXMMC0, which is the source clock of MMC0 (0000: XXTI, 0001: XUSBXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0

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3.7.3.6 Clock Source Control Registers (CLK_SRC5, R/W, Address = 0xE010_0214)

CLK_SRC5	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0
PWM_SEL	[15:12]	Control MUXPWM, which is the source clock of PWM (0000: XXTI, 0001: XUSBXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
Reserved	[11:8]	Reserved	0x0
SPI1_SEL	[7:4]	Control MUXSPI1, which is the source clock of SPI1 (0000: XXTI, 0001: XUSBXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
SPI0_SEL	[3:0]	Control MUXSPI0, which is the source clock of SPI0 (0000: XXTI, 0001: XUSBXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0

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3.7.3.7 Clock Source Control Registers (CLK_SRC6, R/W, Address = 0xE010_0218)

CLK_SRC6	Bit	Description	Initial State
Reserved	[31:26]	Reserved	0x00
DMC0_SEL	[25:24]	Control MUXDMC0, which is the source clock of DMC0 (00:SCLKA2M, 01:SCLKMPLL, 10:SCLKEPLL, 11:SCLKVPLL)	0x0
PWI_SEL	[23:20]	Control MUXPWI, which is the source clock of PWI (0000: XXTI, 0001: XUSBXTI, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
Reserved	[19:17]	Reserved	0
HPM_SEL	[16]	Control MUXHPM, which is the source clock of HPM (0: SCLKAPLL, 1: SCLKMPLL)	0x0
Reserved	[15:14]	Reserved	0x0
SPDIF_SEL	[13:12]	Control MUXSPDIF, which is the source clock of SPDIF (00:SCLK_AUDIO0, 01:SCLK_AUDIO1, 1x:SCLK_AUDIO2)	0x0
AUDIO2_SEL	[11:8]	Control MUXAUDIO2, which is the source clock of AUDIO2 (0000: I2SCDCLK2, 0001: PCMCDCLK2, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: rerved)	0x0
AUDIO1_SEL	[7:4]	Control MUXAUDIO1, which is the source clock of AUDIO1 (0000: I2SCDCLK1, 0001: PCMCDCLK1, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 1000: SCLKVPLL, OTHERS: reserved)	0x0
AUDIO0_SEL	[3:0]	Control MUXAUDIO0, which is the source clock of AUDIO0 (0000: XXTI, 0001: PCMCDCLK0, 0010: SCLK_HDMI27M, 0011: SCLK_USBPHY0, 0100: SCLK_USBPHY1, 0101: SCLK_HDMIPHY, 0110: SCLKMPLL, 0111: SCLKEPLL, 100: SCLKVPLL, OTHERS: reserved)	0x0

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3.7.3.8 Clock Source Control Registers (CLK_SRC_MASK0, R/W, Address = 0xE010_0280)

CLK_SRC_MASK0	Bit	Description	Initial State
Reserved	[31:30]	Reserved	0x3
PWI_MASK	[29]	Mask output clock of MUXPWI (0: disable, 1: enable)	1
Reserved	[28]	Reserved	1
SPDIF_MASK	[27]	Mask output clock of MUXSPDIF (0: disable, 1: enable)	1
AUDIO2_MASK	[26]	Mask output clock of MUXAUDIO2 (0: disable, 1: enable)	1
AUDIO1_MASK	[25]	Mask output clock of MUXAUDIO1 (0: disable, 1: enable)	1
AUDIO0_MASK	[24]	Mask output clock of MUXAUDIO0 (0: disable, 1: enable)	1
Reserved	[23:20]	Reserved	0xF
PWM_MASK	[19]	Mask output clock of MUXPWM (0: disable, 1: enable)	1
Reserved	[18]	Reserved	1
SPI1_MASK	[17]	Mask output clock of MUXSPI1 (0: disable, 1: enable)	1
SPI0_MASK	[16]	Mask output clock of MUXSPI0 (0: disable, 1: enable)	1
UART3_MASK	[15]	Mask output clock of MUXUART3 (0: disable, 1: enable)	1
UART2_MASK	[14]	Mask output clock of MUXUART2 (0: disable, 1: enable)	1
UART1_MASK	[13]	Mask output clock of MUXUART1 (0: disable, 1: enable)	1
UART0_MASK	[12]	Mask output clock of MUXUART0 (0: disable, 1: enable)	1
MMC3_MASK	[11]	Mask output clock of MUXMMC3 (0: disable, 1: enable)	1
MMC2_MASK	[10]	Mask output clock of MUXMMC2 (0: disable, 1: enable)	1
MMC1_MASK	[9]	Mask output clock of MUXMMC1 (0: disable, 1: enable)	1
MMC0_MASK	[8]	Mask output clock of MUXMMC0 (0: disable, 1: enable)	1
FINVPLL_MASK	[7]	Mask output clock of MUXVPLLSRC (0: disable, 1: enable)	1
CSIS_MASK	[6]	Mask output clock of MUXCSIS (0: disable, 1: enable)	1
FIMD_MASK	[5]	Mask output clock of MUXFIMD (0: disable, 1: enable)	1
CAM1_MASK	[4]	Mask output clock of MUXCAM1 (0: disable, 1: enable)	1
CAM0_MASK	[3]	Mask output clock of MUXCAM0 (0: disable, 1: enable)	1
DAC_MASK	[2]	Mask output clock of MUXDAC (0: disable, 1: enable)	1
MIXER_MASK	[1]	Mask output clock of MUXMIXER (0: disable, 1: enable)	1
HDMI_MASK	[0]	Mask output clock of MUXHDMI (0: disable, 1: enable)	1

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3.7.3.9 Clock Source Control Registers (CLK_SRC_MASK1, Address = R/W, 0xE010_0284)

CLK_SRC_MASK1	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0x7FF_FFFF
FIMC_LCLK_MASK	[4]	Mask output clock of MUXFIMC_LCLK (0: disable, 1: enable)	1
F1	[3]	Should have same value as FIMC_LCLK_MASK	1
F0	[2]	Should have same value as FIMC_LCLK_MASK	1
Reserved	[1:0]	Reserved	0x3

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3.7.4 CLOCK DIVIDER CONTROL REGISTER

S5PV210 has several clock dividers to support various operating clock frequency. The clock divider ratio can be controlled by CLK_DIV0, CLK_DIV1, 2, 3, 4, and 5.

There are operating frequency limitations. The maximum operating frequency of SCLKAPLL, SCLKMPLL, SCLKA2M, HCLK_MSYS, and PCLK_MSYS are 1GHz, 667 MHz, 400 MHz, 200 MHz, and 100 MHz, respectively. These operating clock conditions must be met through CLK_DIVX configuration.
Divider for internal memory shown as DIV_{IMEM} in *Figure 3-3* does not have corresponding fields in clock divider control registers since the divider value is fixed to two.

Whenever clock divider control register is changed, it is recommended to check clock divider status registers before using the new clock output. This guarantees corresponding divider finishes changing to a new dividing value before it's output is used by other modules.

3.7.4.1 Clock Divider Control Register (CLK_DIV0, R/W, Address = 0xE010_0300)

CLK_DIV0	Bit	Description	Initial State
Reserved	[31]	Reserved	0
PCLK_PSYS_RATIO	[30:28]	DIVPCLKP clock divider ratio, PCLK_PSYS = HCLK_PSYS / (PCLK_PSYS_RATIO + 1)	0x0
HCLK_PSYS_RATIO	[27:24]	DIVHCLKP clock divider ratio, HCLK_PSYS = MOUT_PSYS / (HCLK_PSYS_RATIO + 1)	0x0
Reserved	[23]	Reserved	0
PCLK_DSYS_RATIO	[22:20]	DIVPCLKD clock divider ratio, PCLK_DSYS = HCLK_DSYS / (PCLK_DSYS_RATIO + 1)	0x0
HCLK_DSYS_RATIO	[19:16]	DIVHCLKD clock divider ratio, HCLK_DSYS = MOUT_DSYS / (HCLK_DSYS_RATIO + 1)	0x0
Reserved	[15]	Reserved	0
PCLK_MSYS_RATIO	[14:12]	DIVPCLKM clock divider ratio, PCLK_MSYS = HCLK_MSYS / (PCLK_MSYS_RATIO + 1)	0x0
Reserved	[11]	Reserved	0
HCLK_MSYS_RATIO	[10:8]	DIVHCLKM clock divider ratio, HCLK_MSYS = ARMCLK / (HCLK_MSYS_RATIO + 1)	0x0
Reserved	[7]	Reserved	0
A2M_RATIO	[6:4]	DIVA2M clock divider ratio, SCLKA2M = SCLKAPLL / (A2M_RATIO + 1)	0x0
Reserved	[3]	Reserved	0
APLL_RATIO	[2:0]	DIVAPLL clock divider ratio, ARMCLK = MOUT_MSYS / (APLL_RATIO + 1)	0x0

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3.7.4.2 Clock Divider Control Register (CLK_DIV1, R/W, Address = 0xE010_0304)

CLK_DIV1	Bit	Description	Initial State
CSIS_RATIO	[31:28]	DIVCSIS clock divider ratio, SCLK_CSIS = MOUTCSIS / (CSIS_RATIO + 1)	0x0
Reserved	[27:24]	Reserved	0x0
FIMD_RATIO	[23:20]	DIVFIMD clock divider ratio, SCLK_FIMD = MOUTFIMD / (FIMD_RATIO + 1)	0x0
CAM1_RATIO	[19:16]	DIVCAM1 clock divider ratio, SCLK_CAM1 = MOUTCAM1 / (CAM1_RATIO + 1)	0x0
CAM0_RATIO	[15:12]	DIVCAM0 clock divider ratio, SCLK_CAM0 = MOUTCAM0 / (CAM0_RATIO + 1)	0x0
Reserved	[11:4]	Reserved	0x0
TBLK_RATIO	[3:0]	DIVTBLK clock divider ratio, SCLK_PIXEL= SCLKVPLL/ (TBLK_RATIO + 1)	0x0

3.7.4.3 Clock Divider Control Register (CLK_DIV2, R/W, Address = 0xE010_0308)

CLK_DIV2	Bit	Description	Initial State
Reserved	[31:12]	Reserved	0x00_0000
G2D_RATIO	[11:8]	DIVG2D clock divider ratio, SCLKG2D= MOUTG2D / (G2D_RATIO + 1)	0x0
MFC_RATIO	[7:4]	DIVMFC clock divider ratio, SCLKMFC= MOUTMFC / (MFC_RATIO + 1)	0x0
G3D_RATIO	[3:0]	DIVG3D clock divider ratio, SCLKG3D= MOUTG3D / (G3D_RATIO + 1)	0x0

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3.7.4.4 Clock Divider Control Register (CLK_DIV3, R/W, Address = 0xE010_030C)

CLK_DIV3	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
FIMC_LCLK_RATIO	[23:20]	DIVFIMC_LCLK clock divider ratio, SCLKFIMC_LCLK= MOUTFIMC_LCLK / (FIMC_LCLK_RATIO + 1)	0x0
F1	[19:16]	Should have same value as FIMC_LCLK_RATIO	0x0
F0	[15:12]	Should have same value as FIMC_LCLK_RATIO	0x0
Reserved	[11:0]	Reserved	0

3.7.4.5 Clock Divider Control Register (CLK_DIV4, R/W, Address = 0xE010_0310)

CLK_DIV4	Bit	Description	Initial State
UART3_RATIO	[31:28]	DIVUART3 clock divider ratio, SCLK_UART3 = MOUTUART3 / (UART3_RATIO + 1)	0x0
UART2_RATIO	[27:24]	DIVUART2 clock divider ratio, SCLK_UART2 = MOUTUART2 / (UART2_RATIO + 1)	0x0
UART1_RATIO	[23:20]	DIVUART1 clock divider ratio, SCLK_UART1 = MOUTUART1 / (UART1_RATIO + 1)	0x0
UART0_RATIO	[19:16]	DIVUART0 clock divider ratio, SCLK_UART0 = MOUTUART0 / (UART0_RATIO + 1)	0x0
MMC3_RATIO	[15:12]	DIVMMC3 clock divider ratio, SCLK_MMC3 = MOUTMMC3 / (MMC3_RATIO + 1)	0x0
MMC2_RATIO	[11:8]	DIVMMC2 clock divider ratio, SCLK_MMC2 = MOUTMMC2 / (MMC2_RATIO + 1)	0x0
MMC1_RATIO	[7:4]	DIVMMC1 clock divider ratio, SCLK_MMC1 = MOUTMMC1 / (MMC1_RATIO + 1)	0x0
MMC0_RATIO	[3:0]	DIVMMC0 clock divider ratio, SCLK_MMC0 = MOUTMMC0 / (MMC0_RATIO + 1)	0x0

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3.7.4.6 Clock Divider Control Register (CLK_DIV5, R/W, Address = 0xE010_0314)

CLK_DIV5	Bit	Description	Initial State
Reserved	[31:12]	Reserved	0x0
PWM_RATIO	[15:12]	DIVPWM clock divider ratio, SCLK_PWM = MOUTPWM / (PWM_RATIO + 1)	0x0
Reserved	[11:8]	Reserved	0x0
SPI1_RATIO	[7:4]	DIVSPI1 clock divider ratio, SCLK_SPI1 = MOUTSPI1 / (SPI1_RATIO + 1)	0x0
SPI0_RATIO	[3:0]	DIVSPI0 clock divider ratio, SCLK_SPI0 = MOUTSPI0 / (SPI0_RATIO + 1)	0x0

3.7.4.7 Clock Divider Control Register (CLK_DIV6, R/W, Address = 0xE010_0318)

CLK_DIV6	Bit	Description	Initial State
DMC0_RATIO	[31:28]	DIVDMC0 clock divider ratio, SCLK_DMC0 = MOUTDMC0 / (DMC0_RATIO + 1)	0x0
PWI_RATIO	[27:24]	DIVPWI clock divider ratio, SCLK_PWI = MOUTPWI / (PWI_RATIO + 1)	0x0
Reserved	[23]	Reserved	0
HPM_RATIO	[22:20]	DIVHPM clock divider ratio, SCLK_HPM = DOUTCOPY / (IEM_RATIO + 1)	0x0
Reserved	[19]	Reserved	0
COPY_RATIO	[18:16]	DIVCOPY clock divider ratio, DOUTCOPY = MOUTHPM / (COPY_RATIO + 1)	0x0
Reserved	[15]	Reserved	0x0
ONENAND_RATIO	[14:12]	DIVFLASH clock divider ratio, SCLK_ONENAND = MOUTFLASH / (ONENAND_RATIO + 1)	0x0
AUDIO2_RATIO	[11:8]	DIVAUDIO2 clock divider ratio, SCLK_AUDIO2 = MOUTAUDIO2 / (AUDIO2_RATIO + 1)	0x0
AUDIO1_RATIO	[7:4]	DIVAUDIO1 clock divider ratio, SCLK_AUDIO1 = MOUTAUDIO1 / (AUDIO1_RATIO + 1)	0x0
AUDIO0_RATIO	[3:0]	DIVAUDIO0 clock divider ratio, SCLK_AUDIO0 = MOUTAUDIO0 / (AUDIO0_RATIO + 1)	0x0

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3.7.4.8 Clock Divider Control Register (CLK_DIV7, R/W, Address = 0xE010_031C)

CLK_DIV7	Bit	Description	Initial State
Reserved	[31:15]	Reserved	0x0
DPM_RATIO	[14:8]	CLK_DPM clock divider ratio. Source of DIVDPM clock divider is PCLK for IEM_IEC. DPM_RATIO decides how often DPM channel increments for IEM_IEC. Refer to *Figure 3-3*.	0x0
Reserved	[7]	Reserved	0
DVSEM_RATIO	[6:0]	CLK_DVSEM clock divider ratio Source of DIVDVSEM clock divider is PCLK for IEM_IEC. DVSEM_RATIO decides how often PWM frame time slot is advanced when IEM_IEC is in DVS emulation mode. It should be guaranteed DIVDVSEM clock runs at 1MHz. Refer to *Figure 3-3*.	0x0

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3.7.5 CLOCK GATING CONTROL REGISTER

There are two types of clock gating control registers for disable/enable operation, namely:

- Clock gating control register by block
- Clock gating register for by IP

The above two registers are ANDed together to generate a final clock gating enable signal. As a result, if either of the two register field is turned OFF, the resulting clock is stopped.

3.7.5.1 Clock Gating Control Register (CLK_GATE_SCLK, R/W, Address = 0xE010_0444)

CLK_GATE_SCLK	Bit	Description	Gated Clock Name	Initial State
Reserved	[31:6]	Reserved	Reserved	0x3FF_FFFF
SCLK_FIMC_LCLK	[5]	Gating special clock for FIMC local clock (0: mask, 1: pass)	SCLK_FIMC_LCLK	1
Reserved	[4:0]	Should be one for all bit	Reserved	0x1F

3.7.5.2 Clock Gating Control Register (CLK_GATE_IP0, R/W, Address = 0xE010_0460)

CLK_GATE_IP0	Bit	Description	Gated Clock Name	Initial State
CLK_CSIS	[31]	Gating all clocks for CSIS	PCLK_CSIS SCLK_CSIS	1
Reserved	[30]	Reserved	Reserved	1
CLK_ROTATOR	[29]	Gating all clocks for ROTATOR (0: mask, 1: pass)	ACLK_ROTATOR	1
Reserved	[28:27]	Reserved	Reserved	0x3
CLK_FIMC2	[26]	Gating all clocks for FIMC2 (0: mask, 1: pass)	ACLK_FIMC2 SCLK_FIMC_LCLK SCLK_CAM0, 1	1
CLK_FIMC1	[25]	Gating all clocks for FIMC1 (0: mask, 1: pass)	ACLK_FIMC1 SCLK_CAM0, 1	1
CLK_FIMC0	[24]	Gating all clocks for FIMC0 (0: mask, 1: pass)	ACLK_FIMC0 SCLK_CAM0, 1	1
Reserved	[23:17]	Reserved	Reserved	0x7F
CLK_MFC	[16]	Gating all clocks for MFC (0: mask, 1: pass)	PCLK_MFC SCLK_MFC	1
Reserved	[15:13]	Reserved	Reserved	0x7
CLK_G2D	[12]	Gating all clocks for G2D	ACLK_G2D SCLK_G2D PCLK_G2D	0x1
Reserved	[11:9]	Reserved	Reserved	0x7

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CLK_GATE_IP0	Bit	Description	Gated Clock Name	Initial State
CLK_G3D	[8]	Gating all clocks for G3D (0: mask, 1: pass)	ACLK_G3D SCLK_G3D	1
Reserved	[7:6]	Reserved	Reserved	0x3
CLK_IMEM	[5]	Gating all clocks for IMEM (0: mask, 1: pass)	ACLK_IMEM	1
CLK_PDMA1	[4]	Gating all clocks for PDMA1 (0: mask, 1: pass)	ACLK_PDMA1 PCLK_PDMA1	1
CLK_PDMA0	[3]	Gating all clocks for PDMA0 (0: mask, 1: pass)	ACLK_PDMA0 PCLK_PDMA0	1
CLK_MDMA	[2]	Gating all clocks for MDMA (0: mask, 1: pass)	ACLK_MDMA PCLK_MDMA	1
CLK_DMC1	[1]	Gating all clocks for DMC1 (0: mask, 1: pass)	ACLK_DMC1 PCLK_DMC1	1
CLK_DMC0	[0]	Gating all clocks for DMC0 (0: mask, 1: pass)	SCLK_DMC0 ACLK_DMC0 PCLK_DMC0	1

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3.7.5.3 Clock Gating Control Register (CLK_GATE_IP1, R/W, Address = 0xE010_0464)

CLK_GATE_IP1	Bit	Description	Gated Clock Name	Initial State
Reserved	[31:29]	Reserved		0x7
CLK_NFCON	[28]	Gating all clocks for NFCON (0: mask, 1: pass)	ACLK_NFCON	1
Reserved	[27]	Reserved		1
CLK_SROMC	[26]	Gating all clocks for SROM (0: mask, 1: pass)	ACLK_SROMC	1
CLK_CFCON	[25]	Gating all clocks for CFCON (0: mask, 1:pass)	ACLK_CFCON	1
CLK_NANDXL	[24]	Gating all clocks for One NAND-XL (0:mask, 1:pass)	ACLK_NANDXL SCLK_NANDXL	1
Reserved	[23:18]	Reserved		0x3F
CLK_USBHOST	[17]	Gating all clocks for USB HOST (0: mask, 1: pass)	ACLK_USBHOST	1
CLK_USBOTG	[16]	Gating all clocks for USB OTG (0: mask, 1: pass)	ACLK_USBOTG	1
Reserved	[15:12]	Reserved		0xF
CLK_HDMI	[11]	Gating all clocks for HDMI link (0: mask, 1: pass)	PCLK_HDMI SCLK_HDMI	1
CLK_TVENC	[10]	Gating all clocks for TVENC (0: mask, 1: pass)	ACLK_TVENC SCLK_TVENC SCLK_DAC	1
CLK_MIXER	[9]	Gating all clocks for MIXER (0: mask, 1: pass)	ACLK_MIXER SCLK_MIXER	1
CLK_VP	[8]	Gating all clocks for VP (0: mask, 1: pass)	ACLK_VP	1
Reserved	[7:3]	Reserved		0x1F
CLK_DSIM	[2]	Gating all clocks for DSIM (0: mask, 1: pass)	PCLK_DSIM	1
Reserved	[1]	Reserved		1
CLK_FIMD	[0]	Gating all clocks for FIMD (0: mask, 1: pass)	ACLK_FIMD SCLK_FIMD	1

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3.7.5.4 Clock Gating Control Register (CLK_GATE_IP2, R/W, Address = 0xE010_0468)

CLK_GATE_IP2	Bit	Description	Gated Clock Name	Initial State
CLK_TZIC3	[31]	Gating all clocks for TZIC3 (0: mask, 1: pass)	ACLK_TZIC3	1
CLK_TZIC2	[30]	Gating all clocks for TZIC2 (0: mask, 1: pass)	ACLK_TZIC2	1
CLK_TZIC1	[29]	Gating all clocks for TZIC1 (0: mask, 1: pass)	ACLK_TZIC1	1
CLK_TZIC0	[28]	Gating all clocks for TZIC0 (0: mask, 1: pass)	ACLK_TZIC0	1
CLK_VIC3	[27]	Gating all clocks for VIC3 (0: mask, 1: pass)	ACLK_VIC3	1
CLK_VIC2	[26]	Gating all clocks for VIC2 (0: mask, 1: pass)	ACLK_VIC2	1
CLK_VIC1	[25]	Gating all clocks for VIC1 (0: mask, 1: pass)	ACLK_VIC1	1
CLK_VIC0	[24]	Gating all clocks for VIC0 (0: mask, 1: pass)	ACLK_VIC0	1
Reserved	[23:21]	Reserved		0x7
CLK_TSI	[20]	Gating all clocks for TSI (0: mask, 1: pass)	ACLK_TSI	1
CLK_HSMMC3	[19]	Gating all clocks for HSMMC3 (0: mask, 1: pass)	ACLK_HSMMC3 SCLK_MMC3	1
CLK_HSMMC2	[18]	Gating all clocks for HSMMC2 (0: mask, 1: pass)	ACLK_HSMMC2 SCLK_MMC2	1
CLK_HSMMC1	[17]	Gating all clocks for HSMMC1 (0: mask, 1: pass)	ACLK_HSMMC1 SCLK_MMC1	1
CLK_HSMMC0	[16]	Gating all clocks for HSMMC0 (0: mask, 1: pass)	ACLK_HSMMC0 SCLK_MMC0	1
Reserved	[15:12]	Reserved		0xF
CLK_JTAG	[11]	Gating all clocks for JTAG (0: mask, 1: pass)	PCLK_JTAG	1
Reserved	[10]	Reserved		1
CLK_MODEM	[9]	Gating all clocks for MODEM I/F (0: mask, 1: pass)	ACLK_MODEM	1
CLK_CORESIGHT	[8]	Gating all clocks for CORESIGHT (0: mask, 1: pass)	ACLK_CSSYS PCLK_CSSYS	1
Reserved	[7:2]	Reserved		0x3F

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CLK_GATE_IP2	Bit	Description	Gated Clock Name	Initial State
CLK_SDM	[1]	Gating all clocks for SDM (0: mask, 1: pass)	ACLK_SDM PCLK_SDM	1
CLK_SECSS	[0]	Gating all clocks for SECSS (0: mask, 1: pass)	ACLK_SECSS	1

Caution: It should be guaranteed that S/W does not access IPs whose clock is gated. This can cause system failure.

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3.7.5.5 Clock Gating Control Register (CLK_GATE_IP3, R/W, Address = 0xE010_046C)

CLK_GATE_IP3	Bit	Description	Gated Clock Name	Initial State
Reserved	[31]	Reserved	-	1
CLK_PCM2	[30]	Gating all clocks for PCM2 (0: mask, 1: pass)	PCLK_PCM2 SCLK_AUDIO2	1
CLK_PCM1	[29]	Gating all clocks for PCM1 (0: mask, 1: pass) (DO NOT mask when I2S1 or SPDIF is used)	PCLK_PCM1 SCLK_AUDIO1	1
CLK_PCM0	[28]	Gating all clocks for PCM0 (0: mask, 1: pass) (DO NOT mask when I2S0 or SPDIF is used)	PCLK_PCM0 SCLK_AUDIO0	1
CLK_SYSCON	[27]	Gating all clocks for SYSCON (0: mask, 1: pass)	PCLK_SYSCON	1
CLK_GPIO	[26]	Gating all clocks for GPIO (0: mask, 1: pass)	PCLK_GPIO	1
Reserved	[25]	Reserved		1
CLK_TSADC	[24]	Gating all clocks for TSADC (0: mask, 1: pass)	PCLK_TSADC	1
CLK_PWM	[23]	Gating all clocks for PWM (0: mask, 1: pass)	PCLK_PWM SCLK_PWM	1
CLK_WDT	[22]	Gating all clocks for WDT (0: mask, 1: pass)	PCLK_WDT	1
CLK_KEYIF	[21]	Gating all clocks for KEYIF (0: mask, 1: pass)	PCLK_KEYIF	1
CLK_UART3	[20]	Gating all clocks for UART3 (0: mask, 1: pass)	PCLK_UART3 SCLK_UART3	1
CLK_UART2	[19]	Gating all clocks for UART2 (0: mask, 1: pass)	PCLK_UART2 SCLK_UART2	1
CLK_UART1	[18]	Gating all clocks for UART1 (0: mask, 1: pass)	PCLK_UART1 SCLK_UART1	1
CLK_UART0	[17]	Gating all clocks for UART0 (0: mask, 1: pass)	PCLK_UART0 SCLK_UART0	1
CLK_SYSTIMER	[16]	Gating all clocks for System Timer (0: mask, 1: pass)	PCLK_ST	1
CLK_RTC	[15]	Gating all clocks for RTC (0: mask, 1: pass)	PCLK_RTC	1
Reserved	[14]	Reserved		1
CLK_SPI1	[13]	Gating all clocks for SPI1 (0: mask, 1: pass)	PCLK_SPI1 SCLK_SPI1	1

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CLK_GATE_IP3	Bit	Description	Gated Clock Name	Initial State
CLK_SPI0	[12]	Gating all clocks for SPI0 (0: mask, 1: pass)	PCLK_SPI0 SCLK_SPI0	1
CLK_I2C_HDMI_PHY	[11]	Gating all clocks for I2C_HDMI_PHY (0: mask, 1: pass)	PCLK_I2C_HDMI_PHY	1
CLK_I2C_HDMI_DDC	[10]	Gating all clocks for I2C_HDMI_DDC (0: mask, 1: pass)	PCLK_I2C_HDMI_DDC	1
CLK_I2C2	[9]	Gating all clocks for I2C2 (0: mask, 1: pass)	PCLK_I2C2	1
Reserved	[8]	Reserved		1
CLK_I2C0	[7]	Gating all clocks for I2C0 (0: mask, 1: pass)	PCLK_I2C0	1
CLK_I2S2	[6]	Gating all clocks for I2S2 (0: mask, 1: pass) (DO NOT mask when SPDIF is used)	PCLK_I2S2 SCLK_AUDIO2	1
CLK_I2S1	[5]	Gating all clocks for I2S1 (0: mask, 1: pass) (DO NOT mask when PCM1 or SPDIF is used)	PCLK_I2S1 SCLK_AUDIO1	1
CLK_I2S0	[4]	Gating all clocks for I2S0 (0: mask, 1: pass) (DO NOT mask when PCM0 or SPDIF is used)	SCLK_AUDIO0	1
Reserved	[3:2]	Reserved		0x3
CLK_AC97	[1]	Gating all clocks for AC97 (0: mask, 1: pass)	PCLK_AC97	1
CLK_SPDIF	[0]	Gating all clocks for SPDIF (0: mask, 1: pass)	PCLK_SPDIF SCLK_SPDIF SCLK_AUDIO0 SCLK_AUDIO1 SCLK_AUDIO2	1

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3.7.5.6 Clock Gating Control Register (CLK_GATE_IP4, R/W, Address = 0xE010_0470)

CLK_GATE_IP4	Bit	Description	Gated Clock Name	Initial State
Reserved	[31:9]	Reserved		0x7F_FFFF
CLK_TZPC3	[8]	Gating all clocks for TZPC3 (0: mask, 1: pass)	PCLK_TZPC3	1
CLK_TZPC2	[7]	Gating all clocks for TZPC2 (0: mask, 1: pass)	PCLK_TZPC2	1
CLK_TZPC1	[6]	Gating all clocks for TZPC1 (0: mask, 1: pass)	PCLK_TZPC1	1
CLK_TZPC0	[5]	Gating all clocks for TZPC0 (0: mask, 1: pass)	PCLK_TZPC0	1
Reserved	[4]	Reserved		1
CLK_SECKEY	[3]	Gating all clocks for SECKEY (0: mask, 1: pass)	PCLK_SECKEY	1
CLK_IEM_APC	[2]	Gating all clocks for IEM APC (0: mask, 1: pass)	PCLK_IEM_APC SCLK_PWI	1
CLK_IEM_IEC	[1]	Gating all clocks for IEM IEC (0: mask, 1: pass)	PCLK_IEM_IEC SCLK_PWI SCLK_HPM	1
CLK_CHIP_ID	[0]	Gating all clocks for CHIP ID (0: mask, 1: pass)	PCLK_CHIP_ID	1

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3.7.5.7 Clock Gating Control Register (CLK_GATE_BLOCK, R/W, Address = 0xE010_0480)

CLK_GATE_BLOCK	Bit	Description	Gated Clock Name	Initial State
Reserved	[31:11]	Reserved		0x1F_FFFF
CLK_INTC	[10]	Gating all clocks for block-INTC (VIC0,1,2, TZIC0,1,2) (0: mask, 1: pass)	ACLK_VIC0,1,2,3 ACLK_TZIC0,1,2,3 ACLK_AHB_ISFR	1
CLK_HSMMC	[9]	Gating all clocks for block-HSMMC (HSMMC0,1,2,3) (0: mask, 1: pass)	ACLK_HSMMC0,1,2,3 ACLK_TSI ACLK_AHB_CSFR ACLK_AHB_CSYS SCLK_HSMMC0,1,2,3	1
CLK_DEBUG	[8]	Gating all clocks for block-DEBUG (MODEM I/F, HOST I/F, CSSYS, JTAG) (0: mask, 1: pass)	ACLK_CSSYS ACLK_MODEM ACLK_AHB_GSFR ACLK_AHB_GSYS PCLK_CSSYS PCLK_JTAG	1
CLK_SECURITY	[7]	Gating all clocks for block-SECURITY (Security Subsystem) (0: mask, 1: pass)	ACLK_SECSS ACLK_AHB_ESYS0,1 ACLK_AHB_ESFR	1
CLK_MEMORY	[6]	Gating all clocks for block-MEMORY (OneNAND XL, CFCON, SROMC, OneNAND, EBI) (0: mask, 1: pass)	ACLK_ONENANDXL ACLK_CFCON ACLK_SROMC ACLK_NFCON ACLK_AHB_SSFR ACLK_AHB_SSYS ACLK_AHB_SMEM SCLK_NANDXL SCLK_ONENAND SCLK_EBI	1
CLK_USB	[5]	Gating all clocks for block-USB (USB OTG) (0: mask, 1: pass)	ACLK_USBOTG ACLK_USBHOST ACLK_AHB_USFR ACLK_AHB_USYS	1

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CLK_GATE_BLOCK	Bit	Description	Gated Clock Name	Initial State
CLK_TV	[4]	Gating all clocks for block-TV (VP, MIXER, TVENC) (0: mask, 1: pass)	ACLK_VP ACLK_MIXER ACLK_TVENC ACLK_AHB_TSFR ACLK_AXI_TSYS PCLK_HDMI PCLK_AXI_TSYS SCLK_MIXER SCLK_TVENC SCLK_DAC SCLK_PIXEL	1
CLK_LCD	[3]	Gating all clocks for block-LCD (FIMD, G2D) (0: mask, 1: pass)	ACLK_FIMD ACLK_AHB_LSFR ACLK_AXI_LSYS PCLK_DSIM PCLK_AXI_LSYS SCLK_FIMD SCLK_FIMC_LCLK[1] ACLK_G2D SCLK_G2D	1
CLK_IMG	[2]	Gating all clocks for block-IMG (FIMC0,1,2, JPEG, ROTATOR) (0: mask, 1: pass)	ACLK_FIMC0,1,2 ACLK_JPEG ACLK_ROTATOR ACLK_AHB_XSFR ACLK_AXI_XSYS PCLK_CSIS PCLK_AXI_XSYS SCLK_CAM0,1 SCLK_CSIS SCLK_FIMC_LCLK	1
CLK_MFC	[1]	Gating all clocks for block-MFC (MFC) (0: mask, 1: pass)	PCLK_MFC SCLK_MFC	1
CLK_G3D	[0]	Gating all clocks for block-G3D (G3D) (0: mask, 1: pass)	ACLK_G3D SCLK_G3D	1

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1 SCLK_FIMC_LCLK will be automatically turned OFF when any of block clock CLK_LCD and CLK_IMG is turned OFF.

3.7.5.8 Clock Gating Control Register (CLK_GATE_IP5, R/W, Address = 0xE010_0484)

CLK_GATE_IP5	Bit	Description	Gated Clock Name	Initial State
Reserved	[31:30]	Should be one for all bit		0x3
CLK_JPEG	[29]	Gating all clocks for JPEG (0: mask, 1: pass)	ACLK_JPEG	1
Reserved	[28:0]	Should be one for all bit		0x1FFFFFFF

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3.7.5.9 Clock Gating Exceptions

Some clock gating cells have exceptional conditions for gating clocks. This section summarizes this.

SCLK_AUDIO0 is gated when all of the following register fields are cleared to LOW. This guarantees SCLK_AUDIO0 is running when any of the load is running.

- CLK_GATE_IP3[0] for SPDIF
- CLK_GATE_IP3[4] for I2S0
- CLK_GATE_IP3[28] for PCM0

SCLK_AUDIO1 is gated when all of the following register fields are cleared to LOW. This guarantees SCLK_AUDIO1 is running when any of the load is running.

- CLK_GATE_IP3[0] for SPDIF
- CLK_GATE_IP3[5] for I2S1
- CLK_GATE_IP3[29] for PCM1

SCLK_AUDIO2 is gated when all of the following register fields are cleared to LOW. This guarantees SCLK_AUDIO2 is running when any of the load is running.

- CLK_GATE_IP3[0] for SPDIF
- CLK_GATE_IP3[6] for I2S2
- CLK_GATE_IP3[30] for PCM2

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3.7.6 CLOCK OUTPUT CONFIGURATION REGISTER

Internal clocks can be monitored through XCLKOUT PAD. CLK_OUT register selects an internal clock among PLL outputs, USBPHY output, HDMIPHY output, RTC, TICK, system bus clocks, ARMCLK, HPM clock and external OSCs. It also divides the selected clock. This is just for debugging. Do not supply this to other components as clock.

CLKOUT frequency = CLKIN (selected by CLKSEL) frequency / (DIVVAL+1)

3.7.6.1 Clock Output Configuration Register (CLK_OUT, R/W, Address = 0xE010_0500)

CLK_OUT	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x000
DIVVAL	[23:20]	Divide ratio (Divide ratio = DIVVAL + 1)	0x0
Reserved	[19:17]	Reserved	0x000
CLKSEL	[16:12]	00000 = FOUTAPLL/4	0x0
		00001 = FOUTMPLL/2	
		00010 = FOUTEPLL	
		00011 = FOUTVPLL	
		00100 = SCLK_USBPHY0	
		00101 = SCLK_USBPHY1	
		00110 = SCLK_HDMIPHY	
		00111 = RTC	
		01000 = RTC_TICK_SRC	
		01001 = HCLK_MSYS	
		01010 = PCLK_MSYS	
		01011 = HCLK_DSYS	
		01100 = PCLK_DSYS	
		01101 = HCLK_PSYS	
		01110 = PCLK_PSYS	
		01111 = ARMCLK/4	
		10000 = SCLK_HPM	
		10001 = XXTI	
		10010 = XUSBXTI	
		10011 = DCLK DCLKCMP, DCLKDIV, DCLKSEL, and DCLKEN fields define DCLK. These bit fields are valid only when CLKSEL is DCLK	
DCLKCMP	[11:8]	This field changes the clock duty of DCLK. Thus, it must be smaller than DCLKDIV. If the DCLKDIV is n, low level duration is (n+1). High level duration is ((DCLKDIV + 1) - (n+1))	0x0

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CLK_OUT	Bit	Description	Initial State
DCLKDIV	[7:4]	DCLK divide value DCLK frequency = DCLKIN / (DCLKDIV + 1)	0x0
DCLKSEL	[3:1]	Select DCLK source clock (000: XXTI, 001: XUSBXTI, 010: SCLK_HDMI27M, 011: SCLK_USBPHY0, 100: SCLK_USBPHY1, 101: SCLK_HDMIPHY, 110: FOUTMPLL/2, 111: SCLKEPLL)	0
DCLKEN	[0]	Enable DCLK (0:disable, 1:enable)	0

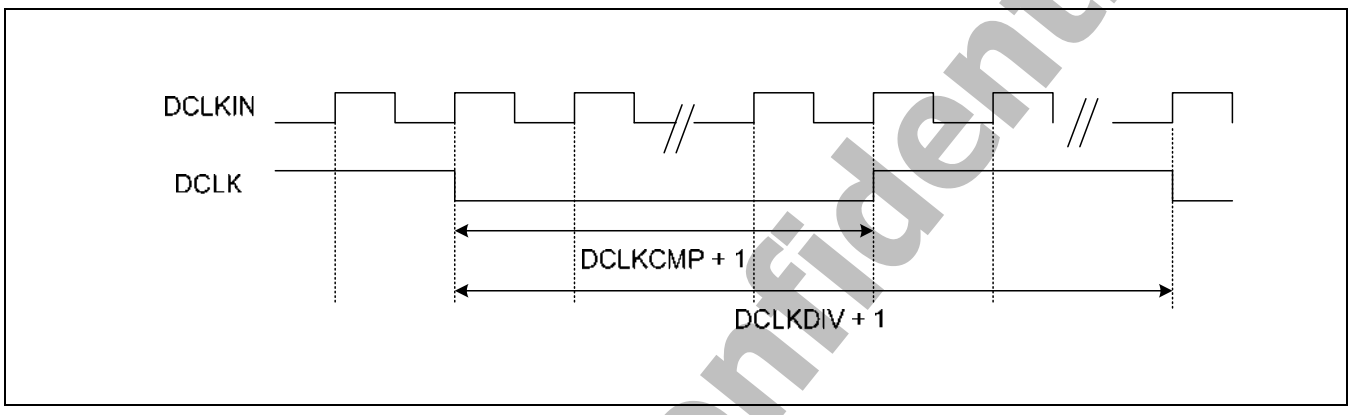

Figure 3-4 CLKOUT Waveform with DCLK Divider

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3.7.7 CLOCK DIVIDER STATUS SFRS

3.7.7.1 Clock Divider Status SFRs (CLK_DIV_STAT0, R, Address = 0xE010_1000)

CLK_DIV_STAT0	Bit	Description	Initial State
DIV_UART3	[31]	DIVUART3 status (0: stable, 1: divider is changing)	0
DIV_UART2	[30]	DIVUART2 status (0: stable, 1: divider is changing)	0
DIV_UART1	[29]	DIVUART1 status (0: stable, 1: divider is changing)	0
DIV_UART0	[28]	DIVUART0 status (0: stable, 1: divider is changing)	0
DIV_MMC3	[27]	DIVMMC3 status (0: stable, 1: divider is changing)	0
DIV_MMC2	[26]	DIVMMC2 status (0: stable, 1: divider is changing)	0
DIV_MMC1	[25]	DIVMMC1 status (0: stable, 1: divider is changing)	0
DIV_MMC0	[24]	DIVMMC0 status (0: stable, 1: divider is changing)	0
Reserved	[23]	Reserved	0
DIV_FIMC_LCLK	[22]	DIVFIMC_LCLK status (0: stable, 1: divider is changing)	0
Reserved	[21:18]	Reserved	0
DIV_MFC	[17]	DIVMFC status (0: stable, 1: divider is changing)	0
DIV_G3D	[16]	DIVG3D status (0: stable, 1: divider is changing)	0
DIV_CSIS	[15]	DIVCSIS status (0: stable, 1: divider is changing)	0
Reserved	[14]	Reserved	0
DIV_FIMD	[13]	DIVFIMD status (0: stable, 1: divider is changing)	0
DIV_CAM1	[12]	DIVCAM1 status (0: stable, 1: divider is changing)	0
DIV_CAM0	[11]	DIVCAM0 status (0: stable, 1: divider is changing)	0
DIV_FIMC	[10]	DIVFIMC status (0: stable, 1: divider is changing)	0
Reserved	[9]	Reserved	0
DIV_TBLK	[8]	DIVTBLK status (0: stable, 1: divider is changing)	0
DIV_PCLK_PSYS	[7]	DIVPCLKP status (0: stable, 1: divider is changing)	0
DIV_HCLK_PSYS	[6]	DIVHCLKP status (0: stable, 1: divider is changing)	0
DIV_PCLK_DSYS	[5]	DIVPCLKD status (0: stable, 1: divider is changing)	0
DIV_HCLK_DSYS	[4]	DIVHCLKD status (0: stable, 1: divider is changing)	0
DIV_PCLK_MSYS	[3]	DIVPCLKM status (0: stable, 1: divider is changing)	0
DIV_HCLK_MSYS	[2]	DIVHCLKM status (0: stable, 1: divider is changing)	0
DIV_A2M	[1]	DIVA2M status (0: stable, 1: divider is changing)	0
DIV_APLL	[0]	DIVAPLL status (0: stable, 1: divider is changing)	0

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3.7.7.2 Clock Divider Status SFRs (CLK_DIV_STAT1, R, Address = 0xE010_1004)

CLK_DIV_STAT1	Bit	Description	Initial State
Reserved	[31:21]	Reserved	0x0
DIV_G2D	[20]	DIVG2D status (0: stable, 1: divider is changing)	0
Reserved	[19:18]	Reserved	0x0
DIV_DPM	[17]	DIVDPM status (0: stable, 1: divider is changing)	0
DIV_DVSEM	[16]	DIVDVSEM status (0: stable, 1: divider is changing)	0
DIV_DMC0	[15]	DIVDMC0 status (0: stable, 1: divider is changing)	0
DIV_PWI	[14]	DIVPWI status (0: stable, 1: divider is changing)	0
DIV_HPM	[13]	DIVHPM status (0: stable, 1: divider is changing)	0
DIV_COPY	[12]	DIVCOPY status (0: stable, 1: divider is changing)	0
DIV_ONENAND	[11]	DIVFLASH status (0: stable, 1: divider is changing)	0
DIV_AUDIO2	[10]	DIVAUDIO2 status (0: stable, 1: divider is changing)	0
DIV_AUDIO1	[9]	DIVAUDIO1 status (0: stable, 1: divider is changing)	0
DIV_AUDIO0	[8]	DIVAUDIO0 status (0: stable, 1: divider is changing)	0
Reserved	[7:4]	Reserved	0
DIV_PWM	[3]	DIVPWM status (0: stable, 1: divider is changing)	0
Reserved	[2]	Reserved	0
DIV_SPI1	[1]	DIVSPI1 status (0: stable, 1: divider is changing)	0
DIV_SPI0	[0]	DIVSPI0 status (0: stable, 1: divider is changing)	0

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3.7.8 CLOCK MUX STATUS SFRS

3.7.8.1 Clock MUX Status SFRs (CLK_MUX_STAT0, R, Address = 0xE010_1100)

Clock MUX status registers show the status of glitch-free MUX logic. When CLK_SRCx SFR has been changed, it takes several clock cycles. Therefore, S/W should check the status of glitch-free MUX if the SFR values are applied.

CLK_MUX_STAT0	Bit	Description	Initial State
Reserved	[31]	Reserved	0
ONENAND_SEL	[30:28]	Selection signal status of MUXFLASH (001:HCLK_PSYS, 010:HCLK_DSYS, 1xx: On changing)	0x1
Reserved	[27]	Reserved	0
MUX_PSYS_SEL	[26:24]	Selection signal status of MUX_PSYS (001:SCLKMPLL, 010:SCLKA2M, 1xx: On changing)	0x1
Reserved	[23]	Reserved	0
MUX_DSYS_SEL	[22:20]	Selection signal status of MUX_DSYS (001:SCLKMPLL, 010:SCLKA2M, 1xx: On changing)	0x1
Reserved	[19]	Reserved	0
MUX_MSYS_SEL	[18:16]	Selection signal status of MUX_MSYS (001:SCLKAPLL, 010:SCLKMPLL, 1xx: On changing)	0x1
Reserved	[15]	Reserved	0
VPLL_SEL	[14:12]	Selection signal status of MUXVPLL (001: FINVPLL, 010: FOUTVPLL, 1xx: On changing)	0x1
Reserved	[11]	Reserved	0
EPLL_SEL	[10:8]	Selection signal status of MUXEPLL (001:FINPLL, 010:FOUTEPLL, 1xx: On changing)	0x1
Reserved	[7]	Reserved	0
MPLL_SEL	[6:4]	Selection signal status of MUXMPLL (001:FINPLL, 010:FOUTMPLL, 1xx: On changing)	0x1
Reserved	[3]	Reserved	0
APLL_SEL	[2:0]	Selection signal status of MUXAPLL (001:FINPLL, 010:FOUTAPLL, 1xx: On changing)	0x1

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3.7.8.2 Clock MUX Status SFRs (CLK_MUX_STAT1, R, Address = 0xE010_1104)

CLK_MUX_STAT1	Bit	Description	Initial State
DMC0_SEL	[31:28]	Selection signal status of MUXDMC0 (00x0:SCLKA2M, 00x1:SCLKMPLL, 010x:SCLKEPLL, 011x:SCLKVPLL, 1xxx: On changing)	0x0
G2D_SEL	[27:24]	Selection signal status of MUXG2D (00x0:SCLKA2M, 00x1:SCLKMPLL, 010x:SCLKEPLL, 011x:SCLKVPLL, 1xxx: On changing)	0x0
Reserved	[23:19]	Reserved	0x0
HPM_SEL	[18:16]	Selection signal status of MUXHPM (001: SCLKAPLL, 010: SCLKMPLL, 1xx: On changing)	0x1
Reserved	[15:8]	Reserved	0x0
MFC_SEL	[7:4]	Selection signal status of MUXMFC (00x0:SCLKA2M, 00x1:SCLKMPLL, 010x:SCLKEPLL, 011x:SCLKVPLL, 1xxx: On changing)	0x0
G3D_SEL	[3:0]	Selection signal status of MUXG3D (00x0:SCLKA2M, 00x1:SCLKMPLL, 010x:SCLKEPLL, 011x:SCLKVPLL, 1xxx: On changing)	0x0

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3.7.9 OTHER SFRS

3.7.9.1 Other SFRs (SWRESET, R/W, Address = 0xE010_2000)

SWRESET	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0x0
SWRESET	[0]	Software reset (0: no effect, 1: reset)	0

3.7.10 IEM CONTROL SFRS

3.7.10.1 IEM Control SFRs (DCGIDX_MAP0, R/W, Address = 0xE010_3000)

DCGIDX_MAP0	Bit	Description	Initial State
DCGIDX_MAP0	[31:0]	IEC configuration for DCG index map[31:0]	0xFFFF_FFFF

3.7.10.2 IEM Control SFRs (DCGIDX_MAP1, R/W, Address = 0xE010_3004)

DCGIDX_MAP1	Bit	Description	Initial State
DCGIDX_MAP1	[31:0]	IEC configuration for DCG index map[63:32]	0xFFFF_FFFF

3.7.10.3 IEM Control SFRs (DCGIDX_MAP2, R/W, Address = 0xE010_3008)

DCGIDX_MAP2	Bit	Description	Initial State
DCGIDX_MAP2	[31:0]	IEC configuration for DCG index map[95:64]	0xFFFF_FFFF

DCGIDX_MAP0~3 are mapped to IECCFGDCGIDXMAP[95:0] of IEM_IEC input port.

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3.7.10.4 IEM Control SFRs (DCGPERF_MAP0, R/W, Address = 0xE010_3020)

DCGPERF_MAP0	Bit	Description	Initial State
DCGPERF_MAP0	[31:0]	DCG performance map[31:0]	0xFFFF_FFFF

3.7.10.5 IEM Control SFRs (DCGPERF_MAP1, R/W, Address = 0xE010_3024)

DCGPERF_MAP1	Bit	Description	Initial State
DCGPERF_MAP1	[31:0]	DCG performance map[63:32]	0xFFFF_FFFF

DCGPERF_MAP0~1 are mapped to IECCFGDCGPERFMAP[63:0] of IEM_IEC input port.

3.7.10.6 IEM Control SFRs (DVCIDX_MAP_MAP0, R/W, Address = 0xE010_3040)

DVCIDX_MAP	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
DCGPERF_MAP0	[23:0]	IEC configuration for DVC index map[23:0]	0xFF_FFFF

DVCIDX_MAP is mapped to IECCFGDVCIDXMAP[23:0] of IEM_IEC input port.

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3.7.10.7 IEM Control SFRs (FREQ_CPU, R/W, Address = 0xE010_3060)

FREQ_CPU	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
FREQ_CPU	[23:0]	Maximum frequency of CPU in kHz	0x00_0000

The register is related to IECCFGFREQCPU[23:0] of IEM_IEC input port. FREQ_CPU[23:0] is the maximum processor of frequency in KHz, and gives the clock frequency of the processor in KHz. Examples values are shown in the following table.

FREQ_CPU[23:0]	Verilog Expression	Processor Frequency
0x00_4E20	24'MSYS20_000	200,000KHz = 20MHz
0x03_A980	24'PSYS40_000	240,000KHz = 240MHz
0x00_03E8	24'MSYS01_000	1,000KHz = 1MHz

3.7.10.8 IEM Control SFRs (FREQ_DPM, R/W, Address = 0xE010_3064)

FREQ_DPM	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
FREQ_DPM	[23:0]	Maximum frequency of DPM accumulators	0x00_0000

The register is related to IECCFGFREQDPM[23:0] of IEM_IEC input port. FREQ_DPM[23:0] is the DPM frequency in KHz, and gives the rate that the DPM is accumulating in KHz. Examples values are shown in the following table.

FREQ_DPM[23:0]	Verilog Expression	Processor Frequency
0x00_4E20	24'MSYS20_000	200,000KHz = 20MHz
0x00_2710	24'MSYS10_000	100,000KHz = 10MHz
0x00_03E8	24'MSYS01_000	1,000KHz = 1MHz

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3.7.10.9 IEM Control SFRs (DVSEMCLK_EN, R/W, Address = 0xE010_3080)

DVSEMCLK_EN	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0x0000_0000
DVSEMCLK_EN	[0]	DVS emulation clock enable	0

The register is related to IECDVSEMCLKEN of IEM_IEC input port. DVSEMCLK_EN means the enable for advancing the PWM frame time slots when in DVS emulation mode. The signal must be pulsed at a frequency of 1 MHz.

3.7.10.10 IEM Control SFRs (MAXPERF, R/W, Address = 0xE010_3084)

MAXPERF	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0x0000_0000
MAXPERF_EN	[0]	MAX performance enable (0: disable, 1: enable)	0

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3.7.10.11 IEM Control SFRs

- APLL_CON0_L8, R/W, Address = 0xE010_3100
- APLL_CON0_L7, R/W, Address = 0xE010_3104
- APLL_CON0_L6, R/W, Address = 0xE010_3108
- APLL_CON0_L5, R/W, Address = 0xE010_310C
- APLL_CON0_L4, R/W, Address = 0xE010_3110
- APLL_CON0_L3, R/W, Address = 0xE010_3114
- APLL_CON0_L2, R/W, Address = 0xE010_3118
- APLL_CON0_L1, R/W, Address = 0xE010_311C

- APLL_CON1_L8, R/W, Address = 0xE010_3300
- APLL_CON1_L7, R/W, Address = 0xE010_3304
- APLL_CON1_L6, R/W, Address = 0xE010_3308
- APLL_CON1_L5, R/W, Address = 0xE010_330C
- APLL_CON1_L4, R/W, Address = 0xE010_3310
- APLL_CON1_L3, R/W, Address = 0xE010_3314
- APLL_CON1_L2, R/W, Address = 0xE010_3318
- APLL_CON1_L1, R/W, Address = 0xE010_331C

APLL_CON0_L1 ~ 8	Bit	Description	Initial State
Reserved	[31:26]	Reserved	0x00
MDIV	[25:16]	APLL M divide value	0x0C8
Reserved	[15:14]	Reserved	0
PDIV	[13:8]	APLL P divide value	0x3
Reserved	[7:3]	Reserved	0
SDIV	[2:0]	APLL S divide value	0x1

Each register of APLL_CON0_L1 ~ 7 configures P/M/S/VCO_FREQ values for ARM PLL at IEM performance level-1 to 8.

APLL_CON1_L1 ~ 8	Bit	Description	Initial State
AFC_ENB	[31]	Decides whether AFC is enabled or not. Active low. AFC selects adaptive frequency curve of VCO for wide range, high phase noise (or jitter) and fast lock time. (LOW: AFC is enabled, HIGH: AFC is disabled)	0x0
Reserved	[30:5]	Reserved	0x0
AFC	[4:0]	AFC value	0x0

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3.7.10.12 IEM Control SFRs

- CLKDIV_IEM_L8, R/W, 0xE010_3200
- CLKDIV_IEM_L7, R/W, 0xE010_3204
- CLKDIV_IEM_L6, R/W, 0xE010_3208
- CLKDIV_IEM_L5, R/W, 0xE010_320C
- CLKDIV_IEM_L4, R/W, 0xE010_3210
- CLKDIV_IEM_L3, R/W, 0xE010_3214
- CLKDIV_IEM_L2, R/W, 0xE010_3218
- CLKDIV_IEM_L1, R/W, 0xE010_321C

CLKDIV_IEM_L1 ~ 8	Bit	Description	Initial State
Reserved	[31:23]	Reserved	0x000
HPM_RATIO	[22:20]	DIVIEM clock divider ratio, DIVIEM = DIVCOPY / RATIO (RATIO = IEM_RATIO + 1)	0x0
Reserved	[19]	Reserved	0
COPY_RATIO	[18:16]	DIVCOPY clock divider ratio, DIVCOPY = MUXIEM / RATIO (RATIO = COPY_RATIO + 1)	0x0
Reserved	[15:11]	Reserved	0x00
HCLK_MSYS_RATIO	[10:8]	DIVHCLKM clock divider ratio, HCLK_MSYS = ARMCLK / RATIO (RATIO = HCLK_MSYS_RATIO + 1)	0x0
Reserved	[7:3]	Reserved	0x0
APLL_RATIO	[2:0]	DIVAPLL clock divider ratio, ARMCLK = MUX_MSYS / RATIO (RATIO = APLL_RATIO + 1)	0x0

Each register of CLKDIV_IEM_L1~8 configures clock divider values for ARM and HPM clocks at IEM performance level-1 to 8.

3.7.11 MISCELLANEOUS SFRS

3.7.11.1 Miscellaneous SFRs (DISPLAY_CONTROL, R/W, Address = 0xE010_7008)

DISPLAY_CONTROL	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0x0000_0000
DISPLAY_PATH_SEL	[1:0]	Display path selection	0
		00: RGB=--- I80=FIMD ITU=FIMD 01: RGB=--- I80=--- ITU=FIMD 10: RGB=FIMD I80=FIMD ITU=FIMD 11: RGB=FIMD I80=FIMD ITU=FIMD	

3.7.11.2 Miscellaneous SFRs (AUDIO_ENDIAN, R/W, Address = 0xE010_700C)

AUDIO_ENDIAN	Bit	Description	Initial State
Reserved	[31:4]	Reserved	0x0000_0000
RP_R_ENDIAN	[3]	Endian selection for RP read channel (0: little endian, 1: big endian)	0
RP_W_ENDIAN	[2]	Endian selection for RP write channel channel (0: little endian, 1: big endian)	0
ARM_R_ENDIAN	[1]	Endian selection for ARM read channel channel (0: little endian, 1: big endian)	0
ARM_W_ENDIAN	[0]	Endian selection for ARM write channel channel (0: little endian, 1: big endian)	0

4 POWER MANAGEMENT

This chapter describes the Power Management Unit (PMU) in S5PV210. SYSCON manages clock management unit (CMU) and PMU in S5PV210.

4.1 OVERVIEW OF PMU

Mobile application processors such as the S5PV210 should consume less power, since mobile products have a small battery with limited power capacity. The purpose of PMU is to provide various methods in S5PV210 to consume less power under specific application scenarios.

The power management scheme in S5PV210 provides six system power modes, namely, *Normal, Idle, Deep-idle, Stop, Deep-stop,* and *Sleep* modes.

The description of each power mode is given as follows:

- **Normal**: In this mode, the CPU core is running, that is, the software is running.
- **Idle**: In this mode, the CPU core is idle, that is, the CPU core clock is disabled but the remaining parts of the S5PV210 are running.
- **Deep-idle**: In this mode, the CPU core is power-gated, that is, the CPU core power is supplied, but is powered off by the internal power switch. The remaining parts of the chip remain the same as those in the *Normal* mode, or become power-gated (except Audio power domain for application of low power MP3 playback).
- **Stop**: In this mode, the S5PV210 is clock-gated (except RTC module). Therefore, application programming stops and waits for wakeup event to resume its operation. Also, the CPU core clock is disabled. (**Note**: The power-gated block in *Normal* mode is still power-gated in *Stop* mode.)
- **Deep-stop**: In this mode, the CPU core and remaining parts of the chip are power-gated (except TOP, RTC, and ALIVE modules). The TOP module can be power-gated or powered-on.
- **Sleep**: In this mode, the internal power(VDD_ARM, VDD_INT, VDD_PLL) of the S5PV210 is externally turned off using regulator or power management IC (PMIC). Therefore, the internal power to S5PV210 is powered “off” except ALIVE block. (**Note**: RTC power to RTC and external power to I/O pad is still "on". If wakeup event occurs, S5PV210 is initialized by wakeup reset, as though power-on reset was asserted.)

‘*Deep*’ means CPU core is power-gated. Therefore, leakage power of CPU core is minimized in *Deep-idle* and *Deep-stop* power modes.

The above description about power mode is given in view of internal digital logic. For more information on non-digital logic, refer to *4.5 "Cortex-A8 Power Mode"*, *4.7 "External Power Control"*, and *4.8 "Internal memory control"*.

PMU controls the power mode of SRAM and PLL. However, the power mode of analog IP (except SRAM and PLL) should be controlled by its corresponding control module.

In addition to the PMU, clock management unit (CMU) also controls the PLL.

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4.2 FUNCTIONAL DESCRIPTION OF PMU

The total power consumption consists of static and dynamic power consumptions. Static power is consumed when power to a circuit is supplied and there is no active operation in the circuit. On the other hand, dynamic power is consumed when the signal to a circuit is changing and there are some active operations in the circuit. The static power consumption is due to leakage current in the process, while dynamic power consumption is due to the transition of gate state. The dynamic power consumption depends on the operating voltage, operating frequency, and toggling ratios of the logic gate.

Various power-saving techniques have been developed, and some of them are shown and compared in *Table 4-1*.

Table 4-1 Comparison of Power Saving Techniques

Power saving techniques	Result	Clock	Power	State Retention	
				Normal F/F	Retention F/F
Frequency scaling	Reduce dynamic power	Enable	Supplied	Keep state	
Clock gating	Minimize dynamic power	Disable	Supplied	Keep state	
Power gating	Minimize leakage power	Disable	External power supplied, while internally gated	Lose state	Keep state
Power off	Nearly zero power	Disable	Externally off	Lose state	

Frequency scaling means that the frequency of clock to a specific module is lowered when the module is not required to run fast. Dynamic power can be reduced by frequency scaling.

Clock gating means that the clock to a specific Intellectual Property (IP) module is disabled using clock gating cells in SYSCON. To control these clock gating cells, set registers CLK_GATE_IP0-4 and CLK_GATE_BLOCK in SYSCON. Clock gating technique is also applied in synthesis phase of chip development flow, where gate-level netlist is generated from RTL code by synthesis tool. The clock gating cells inserted by synthesis tool are controlled not by software, but by hardware automatically. When clock gating is applied, power to logic gate is still supplied. Therefore, the states of Normal Flip-Flop (F/F) and Retention F/F are kept. Retention F/F is developed to keep its state, even though power is not supplied due to power gating.

Power gating means that a current path to a specific power domain (a group of IP modules) is internally disconnected using switch cells in that power domain. Therefore, power to that domain is not supplied. The switch cell can be located between real power and virtual power (HEADER), or between real ground and virtual ground (FOOTER).

To control the switch cells, set registers NORMAL_CFG, IDLE_CFG, and STOP_CFG in SYSCON. Note that external power to S5PV210 is not "OFF". When power gating is applied, the states of normal F/Fs are lost, but the states of retention F/Fs are kept. Therefore, there can be two power-gating techniques, as listed below:

- Power gating without state retention
  - Normal F/F is used.
- Wakeup reset is required. Power gating with state retention
  - Retention F/F is used.

Power “OFF” means that the power to S5PV210 is externally “OFF” using regulator or Power Management IC (PMIC). In S5PV210, SYSCON generates power control signal to regulator or PMIC. When power “OFF” is applied, the states of normal F/Fs and retention F/Fs are lost. Therefore, if you want to save some important data, you should move the data to external memory and restore it when wakeup event occurs.

To reduce the dynamic power consumption, S5PV210 uses clock gating and frequency scaling. Clocks in S5PV210 can be disabled in module-by-module basis. Clock frequency can be lowered when the system is not required to operate at the maximum frequency.

To reduce power consumption further in the system level, S5PV210 makes the DRAM enter into self-refresh mode and deep power-down mode (refer to Chapter 5.1, "DRAM Controller").

To reduce the static current, S5PV210 supports block-based power gating. In specific applications, a certain group of modules are not required to run, and therefore do not need to be powered "ON". For example, MP3 playback, Multi-Format Codec (MFC), Video modules (Camera interface, JPEG, Video Processor, Mixer, and so on), and 3D graphics core, do not need to operate and can be power-gated for minimum static power consumption. S5PV210 internal modules are grouped into 11 power domains based on their functions, as shown in *Table 4-2* S5PV210 Power Domains of Internal Logic and eight power domains except System Timer, ALIVE and RTC can be power-gated by turning “OFF” the Current Cut-off Switch (CCS), which connects the current path between real VDD and virtual VDD.

Table 4-2 S5PV210 Power Domains of Internal Logic

	Power Domain	Included Modules	Power Gating Methods
1	CPU	Cortex-A8, L1/L2 Cache, ETM, NEON	PMOS (inside CPU)
2	MFC	MFC	PMOS (header)
3	G3D	G3D	PMOS (header)
4	Audio Sub-system	Audio related modules: I2S channel 0 only, Audio buffer RAM	PMOS (header)
5	LCD	LCD controller(FIMD), DSIM, G2D	PMOS (header)
6	TV	VP, MIXER, TV Encoder, HDMI	PMOS (header)
7	CAM	Camera interface(FIMC), CSIS, JPEG, Rotator	PMOS (header)
8	System Timer	System Timer	PMOS but, switch is not off (always on)
9	TOP	Clock Management Unit (CMU), GPIO(OFF), Bus components, VIC, TZIC, Internal memory (IROM and IRAM), NAND controller, OneNAND controller, CF controller, SRAM controller, Peripheral DMA, Memory DMA, CoreSight, JTAG, Modem interface, Security sub-system, TSI, HSMMC, USB HOST, USB OTG, DRAM controller, CHIPID, IEM_IEC, Security key, SPDIF, PCM, SPI, KEYIF, TSADC, I2C, I2S channel 1 and 2, AC97, PCM, System timer, Watchdog timer, UART	PMOS (header)
10	ALIVE	Power Management Unit(PMU), GPIO(ALIVE), Wakeup logic	NO
11	RTC	RTC	NO

4.3 SYSTEM POWER MODE

4.3.1 OVERVIEW

According to the power saving schemes and features explained in *Section 4.3* , S5PV210 provides six power modes, namely, NORMAL, IDLE, DEEP-IDLE, STOP, DEEP-STOP, and SLEEP.

Power modes are summarized in *Table 4-3*.

In NORMAL mode, use module-based clock gating, block-based power gating, and frequency scaling to reduce power consumption. To reduce dynamic power consumption, clock gating disables clock input to specific module according to the operating scenario. Clock gating can be done in module-by-module basis.

To reduce static power consumption of a block or power domain (a group of modules), power gating disconnects a leakage current path. Power gating can be done in block-by-block basis.

Frequency scaling lowers the operating frequency to reduce dynamic power consumption.

In IDLE mode, the CPU clock is disabled internally by entering Standby mode of Cortex-A8. CPU performs WFI instruction to enter Standby mode. In this mode, Cortex-A8 core is not running, therefore dynamic power of CPU is reduced. The remaining parts of the chip keep their states in NORMAL mode, that is, clock-gated modules are still clock-gated and power-gated blocks are still power-gated.

In DEEP-IDLE mode, Cortex-A8 core is power-gated rather than clock-gated. In DEEP-IDLE mode, the leakage power of CPU core is minimized. There are three options in DEEP-IDLE mode. The first option is that the remaining parts of the chip keep their operations in NORMAL mode. The second option is that the remaining parts of the chip keep their states in NORMAL mode. The third option is that for low-power MP3 playback, that is, TOP and SUB blocks are also power-gated, but only Audio block is still power on. These three options can be selected by setting TOP_LOGIC field of IDLE_CFG register in SYSCON, that is, TOP domain can either be power-on or power-gated by setting TOP_LOGIC field of IDLE_CFG register before entry into IDLE mode.

- TOP_LOGIC = 2’b01: TOP block and sub-blocks keep their states in NORMAL mode. Audio block is running the operation.
- TOP_LOGIC = 2’b10: TOP block, sub-blocks, and Audio block is running the operation.

‘DEEP’ means that Cortex-A8 Core is power-gated.

In STOP mode, the clock to modules (except RTC module), PLLs, and unnecessary oscillators are selectively disabled in order to minimize dynamic power consumption. In this mode, Cortex-A8 Core enters into Standby mode.

In DEEP-STOP mode, Cortex-A8 Core is power-gated rather than clock-gated as in STOP mode, and the remaining parts of the chip are power-gated (except TOP, RTC, and ALIVE modules). However, TOP domain can either be power-on or power-gated. To do so, set TOP_LOGIC field of STOP_CFG register before entry into DEEP-STOP mode. Cortex-A8 L2 cache can be powered “ON” for memory retention or power-gated to save power.

- TOP_LOGIC = 2’b01, TOP block is power-gated.
- TOP_LOGIC = 2’b10, TOP block is power “ON”.

Table 4-3 Power Mode Summary

		Power Mode					
		NORMAL	**IDLE**	**DEEP-IDLE**	**STOP**	**DEEP-STOP**	**SLEEP**
Cortex-A8	Core	Run with IEM[1)]	Standby	Power gating off	Standby	Power gating off	External Power off
	L2 Cache	Run with IEM	Power on	Retention/ Power gating off	Power on	Retention/ Power gating off	External Power off
Internal Logic	SUB[2)]	Power gating on/off Clock gating on/off	KEEP power state in NORMAL mode	Power gating off	Power gating off	Power gating off	External Power off
	Audio block[3)]	Power gating on/off Clock gating on/off	KEEP power state in NORMAL mode	KEEP power state in NORMAL mode[5)]	Clock gating off	Power gating off	External Power off
	TOP[4)]	Power on Clock gating on/off	KEEP power state in NORMAL mode	Power gating on/off	Clock gating off	Power gating on/off	External Power off
ALIVE		Power on					
PLL		All PLLs on		EPLL on A/M/VPLL off	All PLLs off		External Power off
OSC		XXTI, XUSBXTI on/off			XXTI, XUSBXTI on/off		Selectively Disabled
Typical Wakeup time[6)]	OSC enabled	< 1us[7)]	< 1us	< 1us[8)] or < 410us[9)]	< 410us[10)]	< 410us[10)]	< 1.9ms[12)]
	OSC disabled	N.A	N.A	N.A	< 2.41 ms[11)]	< 2.41ms[11)]	< 4.4 ms[13)]

1) IEM refers to Intelligent Energy Management introduced by ARM. IEM is explained in detail separately in IEM related TRM.

2) SUB refers to power domain of Row 2, 3, 5, 6, 7, and 8 in *Table 4-2*.

3) Audio block refers to power domain of Row 4 in *Table 4-2*.

4) TOP refers to power domain of Row 10 in *Table 4-2*.

5) There is second option in DEEP-IDLE mode for low-power MP3 playback, i.e., TOP block and SUB block is power-gated, but Audio block is still power ”ON”.

6) This time is measured from wakeup event assertion to ARM reset de-assertion or ARM clock supply. That is, ARM runs the next instruction this time after wakeup event is asserted. Restored time is not included. Those saved data in external memory should be restored after this time. All values are measured assuming 24 MHz clock as OSC source.

7) Wake-up time in this case refers to time to power-up a controllable power domain.

8) For TOP block ”ON”, about 300ns for ARM clock supply

9) For TOP block ”OFF”, the highest lock time of PLLs + about under 30us for state recovery time

10) The highest lock time of PLLs + about under 30us for state recovery time

11) OSC_STABLE (set about 2ms in this case. While, default 44.8ms in cold booting) + the highest lock time of PLLs + about under 30us for state recovery time

12) External power supplied time (set 500us in this case, dominated by used power regulator) + PWR_STABLE (set about 1ms in this case. While, default 44.8ms in cold booting) + the highest lock time of PLLs + about under 30us for state recovery time

13) External power supplied time (set 500us in this case, dominated by used power regulator) + The highest of OSC_STABLE and PWR_STABLE (set about 2ms in this case. While, default 44.8ms in cold booting) + the highest lock time of PLLs + about under 30us for state recovery time

In SLEEP mode, power for all blocks except ALIVE block is not supplied since regulator or PMIC turn “OFF” the external power source, and all PLLs and unnecessary oscillators are disabled. Static power consumption is very small in SLEEP mode. The only leakage power source is due to power supplied to ALIVE block.

Hardware disables the PLL in STOP and SLEEP mode, and OSCs are selectively disabled by setting OSC_EN field of STOP_CFG and SLEEP_CFG register in SYSCON.

4.3.2 NORMAL MODE

In NORMAL mode, clock gating, power gating, and frequency scaling can be used for power saving.

Clock gating can be done on the basis of module-by-module. In other words, you can decide which modules to turn on or off. To disable the clock of one or more modules, set the corresponding bits in clock gating control registers CLK_GATE_IP0-4 and CLK_GATE_BLOCK in SYSCON module. Changing these bits (except some bits related AXI modules) will enable/ disable the clock to corresponding modules immediately.

Some bits related to AXI modules will disable the clock input after some time, but will enable the clock input almost immediately. The delay to disable the clock input is due to handshaking procedure of Low power interface. If you want to disable the AXI module, set the bit related to that module to 1'b0, then SYSCON asserts CSYSREQ to 1'b0 to request the AXI module to enter the low power state. If the module asserts CSYSACK to 1'b0, then SYSCON will disable the clock to that module.

NOTE: Use Standby mode to disable CPU clock internally. The Standby mode is one of the power modes of ARM Cortex-A8. The clock to CPU is disabled to reduce switching current in ARM Cortex-A8. When S5PV210 enters IDLE mode, CPU clock is disabled using Standby mode, where application program is not running until wakeup event occurs.

Frequency scaling is done in PLL-by-PLL basis. Change the PLL P/M/S values to lower the operating frequency of the modules. Changing a P/M/S value results in PLL lock operation. S5PV210 stops its operation during the PLL lock period, since the PLL output clock is masked. For more information on how to change P/M/S value and related clock divider value, refer to Chapter 2.10, "Clock Strategy".

Power gating is done on the basis of block-by-block. Set the corresponding bits in NORMAL_CFG register to perform power gating in one or more blocks. The IP blocks that can be power-gated in NORMAL mode are MFC, G3D, IMG sub-system, LCD sub-system, and TV sub-system (Refer to *Table 4-2*).

Power gating of a block will disconnect the current path to the logic gates.

The power domain can also be powered "ON" by setting the corresponding bit in NORMAL_CFG register. Change the multiple bits in the NORMAL_CFG registers to power "ON" or power-gate multiple power domains at the same time. However, you should not initiate power "ON" (or power-gate) before power gating (or power on) is complete.

Power gating status of each power domain is found in the BLK_PWR_STAT register. BLK_PWR_STAT is not updated until the power-up or power-down process is completed. NORMAL_CFG and BLK_PWR_STAT will have different values while the power-up or power-down procedure is in progress, and will have the same value after the power state change is completed. Look up BLK_PWR_STAT register value to know whether power gating is complete or not.

The power gating does not preserve the state of normal flip-flops in the power-down domain. A power domain (except TOP domain) has only normal F/Fs and is not implemented with retention F/Fs. Therefore, a power domain (except TOP domain) namely sub-domain does not preserve the state of F/Fs when the sub-domain is power-gated. When a sub-domain is powered up again, a wakeup reset is asserted for the modules in the sub-domain. However, top domain has retention F/Fs instead of normal F/Fs, therefore top domain keeps the state of F/Fs when the top domain is power-gated. When top domain is powered up again, a wakeup reset is not asserted for the modules in the top domain.

The power-up takes time to stabilize the internal logic gates and memory after power is supplied again. The power-up time is required because a simultaneous power-up of all logic gates and memories is not allowed since it will drain a large amount of current in a very short period and cause system malfunction consequently.

There are two wakeup techniques. First technique is applied to TOP domain and System Timer domain, whereas the other is applied to SUB domains (except System Timer domain).

The first technique is as follows:

The logic gates in TOP and System Timer domains are turned “ON” in two steps, and then memories are turned “ON” one-by-one in memory group. Two steps means that about 10% of all switches are supplied power first, and the remaining 90% switches are supplied power after some time. The power-up time is composed of the logic power-up time and the memory power-up time. These are determined by the oscillator frequency, number of memories and count values given in the OSC_FREQ registers. The count value depends on the size of the logic gates and number of memories. System Timer domain has no memory, and therefore memory power-up time is not necessary.

The second technique is as follows:

The logic gates and memory in SUB domains (except System Timer domain) are turned “ON” at the same time. However, to prevent wakeup noise from occurring, the power to switches is supplied in two steps similar with first technique. About 10% switches are supplied power first, and remaining 90% switches are supplied power after some time.

4.3.3 IDLE MODE

If Cortex-A8 is not required to operate, the clock for Cortex-A8 can be disabled internally. This saves the dynamic power consumption. To disable clock to Cortex-A8, execute a Wait-For-Interrupt instruction. The remaining parts of the chip (except state of Cortex-A8 core) keep their operating states in NORMAL, that is, the running modules are still running, clock-gated modules are still clock-gated, and power-gated modules are still power-gated.

To enter the IDLE mode,

1. Set CFG_STANDBYWFI field of PWR_CFG to 2'b00.
2. Execute Wait-For-Interrupt instruction (WFI).

To exit the IDLE mode, wake up sources (For more information, refer to Section 4.6 "Wakeup Sources").

4.3.4 DEEP-IDLE MODE

If Cortex-A8 is not required to operate and to reduce CPU power, the power to Cortex-A8 core can be gated internally. This saves the static leakage consumption.

To save the static leakage consumption, set the register IDLE_CFG in SYSCON, and execute a Wait-For-Interrupt instruction.

There are three options in DEEP-IDLE mode, namely:

1. The remaining parts of the chip keep their operations in NORMAL mode.
2. The remaining parts of the chip keep their states in NORMAL mode.
3. For low power MP3 playback, TOP block and SUB block is also power-gated, but only Audio block is still power "ON".

To select the above options, set TOP_LOGIC field of IDLE_CFG register in SYSCON, that is, TOP domain can either be power-on or power-gated by the setting of TOP_LOGIC field of IDLE_CFG register, before entry into IDLE mode.

- TOP_LOGIC = 2'b01: TOP block and sub-blocks keep their states in NORMAL mode. Audio block is running the operation.
- TOP_LOGIC = 2'b10: TOP block, sub-blocks, and Audio block is running the operation.

To enter the DEEP-IDLE mode,

1. Make sure all PLLs are running before entering low-power mode.
   This can be done by checking APLL_CON0, MPLL_CON, EPLL_CON0, VPLL_CON register.
   This step is required only when TOP_LOGIC field is set to 2'b01.
2. Set CFG_DIDLE field of IDLE_CFG to 2’b1.
3. Set other fields of IDLE_CFG based on the users' requirements.
4. Set CFG_STANDBYWFI field of PWR_CFG to 2’b01.
5. Set SYSCON_INT_DISABLE field of OTHERS to 1’b1
6. Execute Wait-For-Interrupt instruction (WFI). If SYSCON_INT_DISABLE field of OTHERS is still 1'b1 after calling wfi instruction, this indicates wfi instruction is ignored by the processor
   and user should call wfi instruction again.

The SYSCON performs the following sequence to enter DEEP-IDLE mode (TOP_LOGIC = 2’b01).

1. Complete all active bus transactions.
2. Complete all active memory controller transactions.
3. Allow external DRAM to enter self-refresh mode (to preserve DRAM contents).
4. Mask clock input using internal signal in SYSCON.
5. Disable all PLLs except for EPLL.
6. Selectively disable OSCs except 32.768 KHz.

To exit the DEEP-IDLE mode, wake up sources (For more information, refer to Section 4.6). Then SYSCON performs the following sequence to exit from DEEP-IDLE mode (TOP_LOGIC = 2’b01).

1. Enable the OSC pads if disabled and wait for the OSC stabilization (around 1ms).
2. Unmask clock input to clock-on blocks.
3. Enable the PLLs and wait for locking (about 300us).
4. Let DRAMs exit from self-refresh mode.

4.3.5 STOP MODE

In STOP mode, clock to modules (except RTC module), PLLs, and unnecessary oscillators are selectively disabled to minimize dynamic power consumption. In this mode, Cortex-A8 Core enters into Standby mode. Therefore, current application program that is running in NORMAL mode stops in STOP mode and waits for wakeup event to resume.

To enter the STOP mode,

1. Make sure all PLLs are running before entering low-power mode.
   This can be done by checking APLL_CON0, MPLL_CON, EPLL_CON0, VPLL_CON register.
2. Cut power off for all sub-blocks (LCD, CAM, TV, 3D, MFC) and verifies it is finised.
3. Set ARM_LOGIC field of STOP_CFG register to 2’b10. Set TOP_LOGIC field of STOP_CFG register to 2'b10.
4. Set other fields of STOP_CFG based on the users' requirements.
5. Set CFG_STANDBYWFI field of PWR_CFG to 2’b10.
6. Set SYSCON_INT_DISABLE field of OTHERS to 1’b1
7. Execute Wait-For-Interrupt instruction (WFI). If SYSCON_INT_DISABLE field of OTHERS is still 1'b1 after calling wfi instruction, this indicates wfi instruction is ignored by the processor and user should call wfi instruction again.

The SYSCON performs the following sequence to enter STOP mode.

1. Complete all active bus transactions.
2. Complete all active memory controller transactions.
3. Allow external DRAM to enter self-refresh mode (to preserve DRAM contents).
4. Mask clock input using internal signal in SYSCON.
5. Disable all PLLs.
6. Selectively disable OSCs except 32.768KHz.

In the above procedure, to finish all active bus transactions, SYSCON asserts CSYSREQs for AXI interface components (AXI masters). If SYSCON confirms that all CSYSACKs and CACTIVEs from all AXI masters become low, then it will check that CSYSACK and CACTIVE from external memory controller become low after it asserts CSYSREQ to external memory controller to low. Then it confirms that CSYSACK and CACTIVE from external memory controller become low and proceeds to next step.

To exit STOP mode, wake up sources (For more information, refer to *Section 4.6 "Wakeup Sources").* Then SYSCON performs the following sequence to exit from STOP mode.

1. Enable the OSC pads if disabled and wait for the OSC stabilization (around 1ms).
2. Enable the PLLs and wait for locking (about 300us).
3. Unmask clock input to clock-on blocks.
4. Let DRAMs exit from self-refresh mode.

OSC stabilization time is determined by the external clock frequency and counter value specified in the OSC_STABLE register. PLL locking time is set in PLL_LOCK registers.

4.3.6 DEEP-STOP MODE

In DEEP-STOP mode, Cortex-A8 Core is power-gated rather than clock-gated, and the remaining parts of the chip are power-gated (except RTC module). However, TOP domain can either be power-on or power-gated by setting TOP_LOGIC field of STOP_CFG register before entry into DEEP-STOP mode. Cortex-A8 L2 cache can be powered on for memory retention or power-gated to save power.

- TOP_LOGIC = 2'b01, TOP block is power-gated.
- TOP_LOGIC = 2'b10, TOP block is power "ON".

To enter the DEEP-STOP mode,

1. Make sure all PLLs are running before entering low-power mode.
   This can be done by checking APLL_CON0, MPLL_CON, EPLL_CON0, VPLL_CON register.
2. Cut power off for all sub-blocks (LCD, CAM, TV, 3D, MFC) and verifies it is finised.
3. Set ARM_LOGIC field of STOP_CFG register to 2'b00.
4. Set other fields of STOP_CFG based on the users' requirements.
5. Set CFG_STANDBYWFI field of PWR_CFG to 2'b10
6. Set SYSCON_INT_DISABLE field of OTHERS to 1'b1
7. Execute Wait-For-Interrupt instruction (WFI). If SYSCON_INT_DISABLE field of OTHERS is still 1'b1 after calling wfi instruction, this indicates wfi instruction is ignored by the processor and user should call wfi instruction again.

The SYSCON performs the following sequence to enter DEEP-STOP mode.

1. Complete all active bus transactions.
2. Complete all active memory controller transactions.
3. Allow external DRAM to enter self-refresh mode (to preserve DRAM contents).
4. Mask clock input using internal signal in SYSCON.
5. Disable all PLLs.
6. Selectively disable OSCs except 32.768KHz.

To exit the DEEP-STOP mode, wake up sources (For more information, refer to *Section 4.6 "Wakeup Sources").*
Then SYSCON performs the following sequence to exit from DEEP-STOP mode.

1. Enable the OSC pads if disabled and wait for the OSC stabilization (around 1ms).
2. Enable the PLLs and wait for locking (about 300us).
3. Unmask clock input to clock-on blocks.

4. Let DRAMs exit from self-refresh mode.

4.3.7 SLEEP MODE

In SLEEP mode, all power domains are powered down (except ALIVE and RTC), all PLLs are disabled, and the oscillators (except RTC) are selectively disabled.

To enter the SLEEP mode,

1. Set SLEEP_CFG based on the users' requirements.
2. Set CFG_STANDBYWFI field of PWR_CFG to 2'b11.
3. Set SYSCON_INT_DISABLE field of OTHERS to 1'b1
4. Execute Wait-For-Interrupt instruction (WFI). If SYSCON_INT_DISABLE field of OTHERS is still 1'b1 after calling wfi instruction, this indicates wfi instruction is ignored by the processor and user should call wfi instruction again.

Then the SYSCON performs the following sequence to enter SLEEP mode.

1. Complete all active bus transactions.
2. Complete all active memory controller transactions.
3. Allow the external DRAM enter self-refresh mode (to preserve DRAM contents).
4. Disable all PLLs.
5. Selectively disable OSCs except 32.768 KHz.
6. XPWRRGTON becomes low to power off external voltage regulator.

To exit the SLEEP mode, wake up sources referred in section <TODO> Wakeup Sources.

Then the SYSCON performs the following sequence to exit from SLEEP mode.

1. Assert wake-up reset to low.
2. XPWRRGTON becomes high to power on external voltage regulator.
3. Wait for voltage regulator to be stable (around 6ms).
4. Enable the OSC pads if disabled and wait for the OSC stabilization (around 1ms.)
5. Power up all power domains except power domains, which was power-down state before entering the SLEEP Mode.
6. Release wake-up reset.

Since all modules are powered "OFF" and their states are not preserved in SLEEP mode, you must save and

restore necessary state information before and after SLEEP mode. An example procedure of state saving and recovery is described in *Section 4.5.3 "State Save and Restore"* on *page 4-22.*

Caution: Executing wfi instruction is a mandatory step when entering low-power mode. To make sure the processor does not ignore wfi instruction, it is recommended to make a loop statement around the wfi instruction. The loop repeatedly calls wfi instruciton until SYSCON_INT_DISABLE field of OTHERS register to become LOW, which indicates low-power mode entering sequence is completed.

4.4 SYSTEM POWER MODE TRANSITION

Figure 4-1 shows the state transition diagram of power mode.

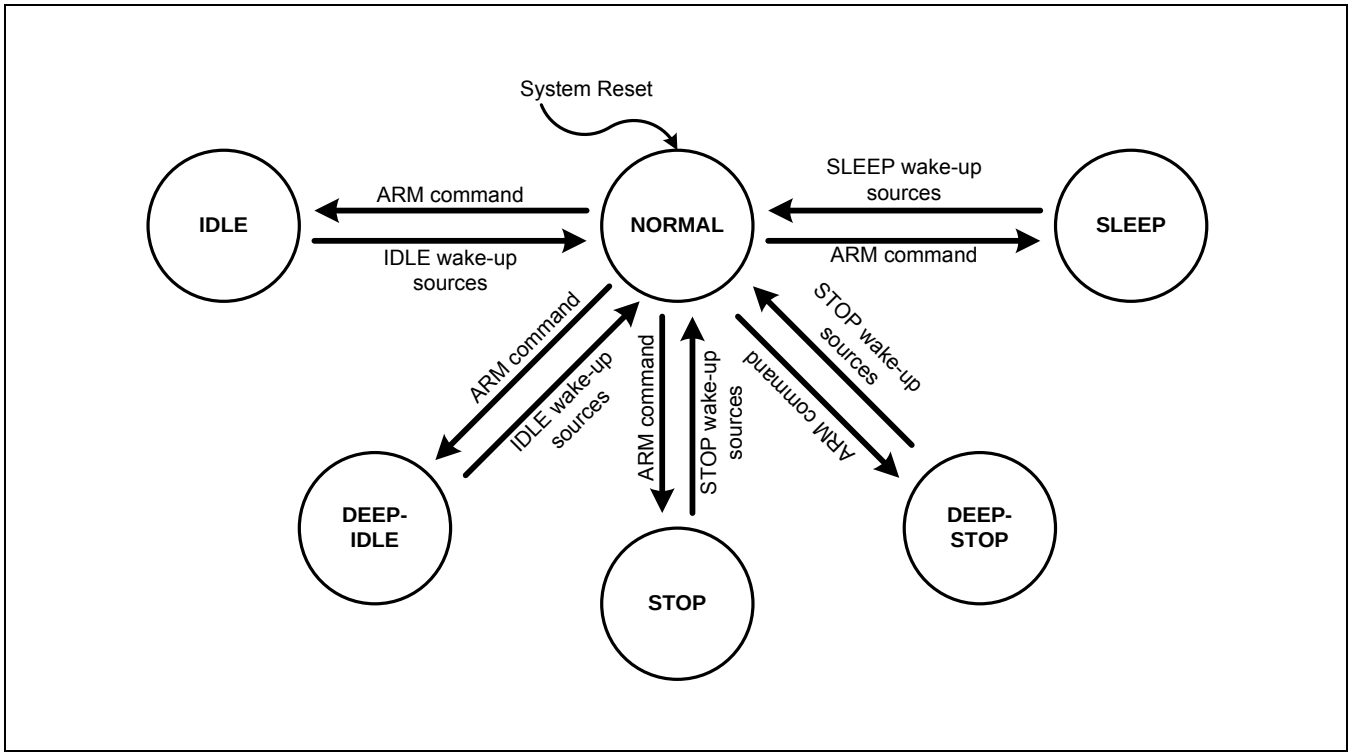


Figure 4-1 State Transition Diagram of Power Mode

The wakeup sources described in *Figure 4-1* are summarized in *Table 4-4*.

4.4.1 TRANSITION ENTERING/ EXITING CONDITION

Table 4-4 shows the Power Saving mode state and Entering or Exiting condition. As you can see, the entering conditions are set by the main ARM CPU.

Table 4-4 Power Saving Mode Entering/Exiting Condition

Power Mode	Enter	Exit
General Clock Gating	Use S/W to set the Clock-disable Bit for each IP block	Use S/W to clear the Clock-disable Bit for each IP block
IDLE	Set CFG_STANDBYWFI field of PWR_CFG to 2'b00. Execute Wait-For-Interrupt instruction (WFI).	1) All interrupt sources[1]
DEEP-IDLE (TOP block on)	Set CFG_DIDLE field of IDLE_CFG to 0x1. Set TOP_LOGIC field of IDLE_CFG to 0x2. Set other fields of IDLE_CFG for users' need. Set CFG_STANDBYWFI field of PWR_CFG to 2'b01. Set SYSCON_INT_DISABLE field of OTHERS to 1'b1 Execute WFI.	1) All interrupt sources[1]
DEEP-IDLE (TOP block off)	Set CFG_DIDLE field of IDLE_CFG to 0x1. Set TOP_LOGIC field of IDLE_CFG to 0x1. Set other fields of IDLE_CFG for users' need. Set CFG_STANDBYWFI field of PWR_CFG to 2'b01. Set SYSCON_INT_DISABLE field of OTHERS to 1'b1 Execute WFI.	1) External Interrupt 2) RTC Alarm 3) RTC TICK 4) Key Pad Press event 5) MMC0~3 6) Touch Screen Pen-down event 7) I2S in audio sub-block wake-up event 8) System Timer event 9) CEC wake-up event
(DEEP) STOP	Set ARM_LOGIC field of STOP_CFG register. (0x2 for STOP and 0x0 for DEEP-STOP) Set other fields of STOP_CFG for users' need. Set CFG_STANDBYWFI field of PWR_CFG to 2'b10. Set SYSCON_INT_DISABLE field of OTHERS to 1'b1 Execute WFI.	1) External Interrupt 2) RTC Alarm 3) RTC TICK 4) Key Pad Press event 5) MMC0~3 6) Touch Screen Pen-down event 7) System Timer event 8) CEC wake-up event
SLEEP	Set SLEEP_CFG for users' need. Set CFG_STANDBYWFI field of PWR_CFG to 2'b11. Set SYSCON_INT_DISABLE field of OTHERS to 1'b1 Execute WFI.	1) External Interrupt 2) RTC Alarm 3) RTC TICK 4) Key Pad Press event 5) CEC wake-up event

1. Depends on their interrupt mask bits.

Power mode exit condition is met when one of various wakeup sources occurs. For more information on wakeup sources, refer to *4.6 "Wakeup Sources"*.

4.5 CORTEX-A8 POWER MODE

4.5.1 OVERVIEW

Cortex-A8 has its own four power modes, namely, RUN, STANDBY, L2RETENTION, and POWER-OFF.

In each power mode, power control of Cortex-A8 is done as follows:

- In RUN mode, Core logic of Cortex-A8 is powered "ON" and clocked. The L2 cache of Cortex-A8 is power-on.
- In STANDBY mode, Core logic of Cortex-A8 is powered "ON" and only wake-up logic is clocked. The L2 cache of Cortex-A8 is power-on.
- In L2RETENTION mode, Core logic of Cortex-A8 is power-gated and L2 cache of Cortex-A8 enters retention mode for data retention. Therefore, the data of L2 cache can be kept in this mode.
- In POWER-OFF mode, all components of Cortex-A8 (that is, Core logic, L2 cache, ETM, and NEON) are all power-gated.

4.5.2 CORTEX-A8 POWER MODE TRANSITION

For information on entry to and exit from STANDBY mode in IDLE mode, refer to *4.3.3 "IDLE Mode"*.

For information on entry to and exit from L2RETENTION and POWER-OFF in DEEP-IDLE mode, refer to *4.3.4 "DEEP-IDLE Mode"*.

In IDLE and STOP mode, Cortex-A8 enters STANDBY mode.

In DEEP-IDLE and DEEP-STOP mode, Cortex-A8 enters L2RETENTION or POWER-OFF mode depending on the selection of L2 retention mode, that is, IDLE_CFG[27:26] for DEEP-IDLE mode, and STOP_CFG[27:26] for DEEP-STOP mode.

In SLEEP mode, Cortex-A8 automatically enters POWER-OFF mode. Before entry into SLEEP mode, state of Cortex-A8 must be saved in external memory.

Figure 4-2 shows the state transition diagram of Cortex-A8 power mode, and the relationship between System power mode and Cortex-A8 power mode transition is summarized in *Table 4-5*.

STANDBY, L2RETENTION, and POWER-OFF modes transition from RUN mode can be done in NORMAL system power mode. STANDBY mode of Cortex-A8 can exist in IDLE and STOP system power modes. L2RETENTION mode of Cortex-A8 can exist in DEEP-IDLE and DEEP-STOP system power mode. POWER-OFF mode of Cortex-A8 can exist in DEEP-IDLE, DEEP-STOP, and SLEEP system power mode.

RUN mode transitions from STANDBY, L2RETENTION, and POWER-OFF can be done by wakeup sources. In IDLE mode, internal interrupts, external interrupts, and RTC alarm can be wakeup sources. In DEEP-IDLE mode, external interrupts, wakeup event, and RTC alarm can be wakeup sources. In STOP, and DEEP-STOP, external interrupts, wakeup event, and RTC alarm can be wakeup sources.

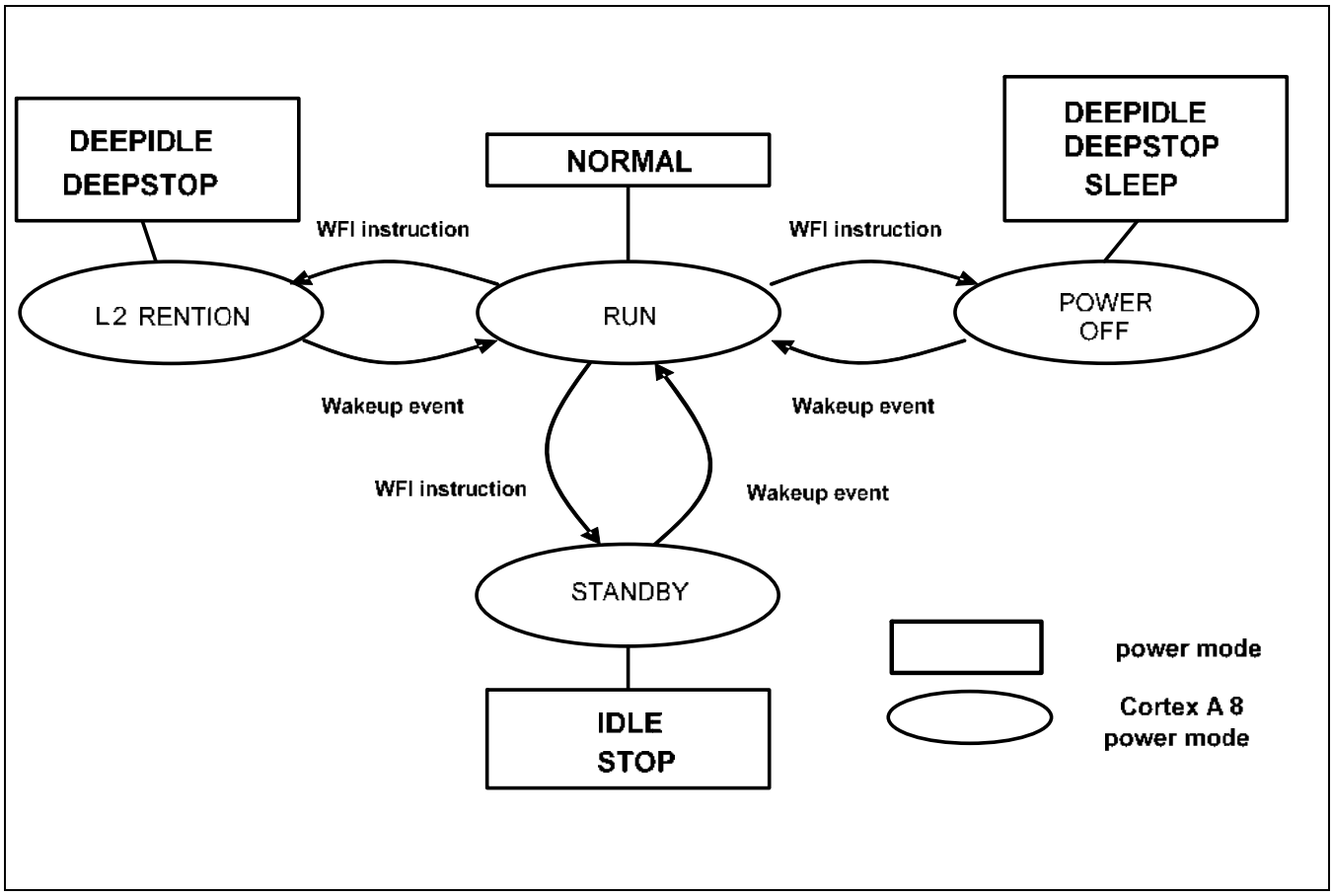


Figure 4-2 Cortex-A8 Power Mode Transition Diagram

Table 4-5 Cortex-A8 Power Control

Cortex-A8 power mode transition	System Power Mode					
	NORMAL	IDLE	DEEP-IDLE	STOP	DEEP-STOP	SLEEP
Cortex-A8	Core	Run with IEM1)	Standby	Power gating	Standby	Power gating
RUN → STANDBY	By WFI command	Standby	N.A	Standby	N.A.	N.A.
RUN → L2RETENTION	By register setting and WFI command (SYSCON)	N.A.	L2RETENTION	N.A.	L2RETENTION	N.A.
RUN → POWER-OFF	By register setting and WFI command (SYSCON)	N.A.	POWER-OFF	N.A.	POWER-OFF	POWER-OFF
STANDBY → RUN	N.A	Wakeup by interrupt	N.A	Wakeup by interrupt	N.A.	N.A.
L2RETENTION → RUN	N.A	N.A.	Wakeup by interrupt	N.A	Wakeup by interrupt	N.A.
POWER-OFF → RUN	N.A	N.A.	Wakeup by interrupt	N.A.	Wakeup by interrupt	Wakeup by interrupt

N.A: Not Available

4.5.3 STATE SAVE AND RESTORE

The current state of power-gated modules will be lost when their power turns ”OFF”. Therefore, before the modules are power-gated, their state should be saved, and restored after wakeup reset is asserted. In case of Cortex-A8, in DEEP-IDLE, DEEP-STOP, and SLEEP mode, the state of Cortex-A8 core will be lost, therefore the current states must be saved. Cortex-A8 will start running from the reset handler as it does when hardware reset occurs. To continue execution from the point where it entered SLEEP mode, users must save and restore the current states before and after those modes. An example of state save and restore is described below.

Before entering SLEEP mode,

1. Save the status of necessary modules.
2. Save resume address, MMU (Memory Management Unit), and registers for each Cortex-A8 mode (SVC, FIQ, IRQ, ABT, etc.).
3. Create and save checksum for security.
4. Flush cache if L2 cache is power-gated.

After wake-up,

1. Proceed to normal system initialization sequence including PLL locking.
2. Look up the RST_STAT register to check if it is the wake-up from SLEEP mode.
3. Let external DRAM exit from self-refresh mode.
4. Restore all registers and MMU information.
5. Jump to the saved resume address to resume execution.

The SYSCON has eight 32-bit SFRs, namely, INFORM0-6 for quick saving and recovery of the state information, or you can save information to external DRAM.

4.6 WAKEUP SOURCES

Table 4-6 Relationship Among Power Mode Wakeup Sources

Power Mode				Wakeup Sources
IDLE DEEP-IDLE (1)				All interrupt sources
	DEEP-IDLE (2)			I2S (in audio block)
		STOP or DEEP-STOP		MMC0, MM1, MMC2, MMC3
				TSADC
				System Timer
			SLEEP	External interrupt sources (EINT)
				RTC Alarm
				RTC TICK
				KEYIF
				HDMI CEC

NOTE:

1. If TOP block on
2. If TOP block off

4.6.1 EXTERNAL INTERRUPTS

External interrupts are the common wake-up source of IDLE (including DEEP-IDLE), STOP (including DEEP-STOP), and SLEEP modes. The logic for external interrupt configuration such as polarity, edge/level sensitivity, and masking resides in the GPIO. It can be modified through GPIO register setting before entering power down modes. The external interrupt handling logic holds the external interrupt information until Cortex-A8 clears the information. It allows Cortex-A8 to handle the external interrupt after wake-up.

4.6.2 RTC ALARM

The Real Time Clock (RTC) has 32-bit counter to wake up the system after specified time. If the timer alarm triggers, the SYSCON wakes up the system and sets the RTL_ALARM field of WAKEUP_STAT register to 1. After the wake-up, Cortex-A8 can refer the WAKEUP_STAT register to find out the cause of wake up.

4.6.3 SYSTEM TIMER

System Timer is newly introduced module in S5PV210. It supplements PWM timer, which suffers from accumulation of time deviation when operated in variable tick mode. On the contrary, System Timer is free from such deviation and can be a preferrable choice for variable tick generation.

In DEEP-IDLE, STOP, and DEEP-STOP mode, there can be no system clock when TOP block is power-gated. Therefore, RTC is used to generate timing tick instead of PWM timer, but by using this clock, timing count is not controlled to meet exact 1ms OS time tick since RTC clock does not have high resolution. On the other hand, System timer has the function to generate interrupts at various interval, and do not require manual setting. Thus, it does not wake up the chip too often, and provides accurate 1ms timing ticks. It uses an external crystal clock, RTC clock and the generated clock from SYSCON as clock input.

For System Timer to operate in DEEP-IDLE, STOP, and DEEP-STOP mode, power to System Timer is not gated. The wakeup event from System Timer will wake up S5PV210 from DEEP-IDLE, STOP, and DEEP-STOP mode.

4.7 EXTERNAL POWER CONTROL

Table 4-7 shows the external power control summary.

Table 4-7 S5PV210 External Power Control

	Block	Controlled by	NORMAL	IDLE/ DEEP-IDLE (1)	DEEP-IDLE (2) / STOP / DEEP-STOP	SLEEP
1	USB PHY	USB link	Run / IDLE / Suspend / externally powered-off	Keep operation or power state in NORMAL	Suspend / externally powered-off	Should be externally powered-off.
2	HDMI PHY	HDMI link	Run / Power-down / externally powered-off	Keep operation or power state in NORMAL	Power-down / externally powered-off	Should be externally powered-off.
3	MIPI D-PHY	MIPI link	Run / LP / ULPS / externally powered-off	Keep operation or power state in NORMAL	LP / ULPS / externally powered-off	Should be externally powered-off.
4	PLL	SYSCON	Run / Power-down	Keep operation or power state in NORMAL	Power-down	Should be externally powered-off.
5	DAC	TV Encoder logic	Run / Power-down / externally powered-off	Keep operation or power state in NORMAL	Power-down / externally powered-off	Should be externally powered-off.
6	TSADC	TSADC logic	Run / Power-down	Keep operation or power state in NORMAL	Standby / Power-down	Power-on
7	Digital I/O	SYSCON	Power-on	Power-on	Power-on	Power-on

NOTE:

1. TOP block on
2. TOP block off

4.7.1 USB PHY (OTG AND HOST)

USB PHY has three power modes, namely, Run, IDLE, and Suspend mode.

- In Run mode, USB PHY sends and receives data normally.
- In IDLE mode, there is no data transaction to and from USB PHY. However, the clock is still supplied to USB PHY.
- In Suspend mode, USB PHY clock is “OFF” to save power.

In NORMAL mode, all the three power modes can be used.

If USB PHY is in use, then it is in Run mode when there is data transaction, and in IDLE mode when there is no data transaction. The USB link performs the change between these two modes.

If USB PHY is not in use, then it can enter into Suspend mode. Set register in USB for Entry to, and Exit from Suspend mode.

In IDLE mode and DEEP-IDLE mode where TOP block is ”ON”, USB PHY keeps its operation or power state in NORMAL.

Before entry to DEEP-IDLE mode where TOP block is ”OFF”, STOP, DEEP-STOP, and SLEEP mode, it is recommended that USB PHY enter into Suspend mode.

4.7.2 HDMI PHY

HDMI PHY has two power modes, namely, Run and Power-down mode

- In Run mode, HDMI PHY sends and receives data normally.
- In Power-down mode, all power to HDMI PHY is “OFF” internally.

In NORMAL mode, both the power modes can be used.

If you want to use HDMI PHY, then set it in the Run mode. Otherwise, it can enter into Power-down mode to save static power by setting register in HDMI link. I2C I/F can control the mode transition from normal mode to power-down mode. The hardware signal, PWR_OFF, is not used for this purpose.

In IDLE mode, and DEEP-IDLE mode where TOP block is ”ON”, HDMI PHY keeps its operation or power state in NORMAL.

Before entry to DEEP-IDLE mode where TOP block is ”OFF”, STOP, DEEP-STOP, and SLEEP mode, it is recommended that HDMI PHY enter into Power-down mode.

4.7.3 MIPI D-PHY

MIPI D-PHY has three power modes, namely, Run, LP, and ULPS mode

- In Run mode, MIPI D-PHY sends and receives data normally.
- In LP and ULPS mode, all power MIPI D-PHY is off internally.

In NORMAL mode, all three power modes can be used.

If you want to use MIPI D-PHY, then you should set it in the Run mode. Otherwise, it can enter into LP or ULPS mode to save static power by setting register in MIPI link.

In IDLE mode, and DEEP-IDLE mode where TOP block is ”ON”, MIPI D-PHY keeps its operation or power state in NORMAL.

Before entry to DEEP-IDLE mode where TOP block is ”OFF”, STOP, and DEEP-STOP mode, it is recommended that MIPI D-PHY enter into LP or ULPS mode. Before entry to SLEEP, it is recommended that MIPI D-PHY enter into ULPS mode. For more details about LP and ULPS mode, refer to MIPI D-PHY user’s manual.

4.7.4 PLL

PLL has two power modes, namely, Run and Power-down mode

- In Run mode, PLL operate normally. (PLL Enable)
- In Power-down mode, all power to PLL is “OFF” internally. (PLL Disable)

In NORMAL mode, both power modes can be used.

If you want to use PLL, then you should set it in the Run mode. Otherwise, it can enter into Power-down mode to save static power by setting register (APLLCON, MPLLCON, EPLLCON, VPLLCON) in SYSCON.

In IDLE mode, and DEEP-IDLE mode where TOP block is ”ON”, PLL keeps its operation or power state in NORMAL.

In DEEP-IDLE mode where TOP block is “OFF”, APLL, MPLL, and VPLL are powered down automatically by SYSCON. Note that EPLL is still powered on in this mode to provide proper operating clock to Audio sub-block.

In STOP and SLEEP mode, all PLLs are powered down automatically by SYSCON.

4.7.4.1 Status of PLL after Wake-Up Event

When the S5PV210 wakes up from STOP mode or SLEEP mode by an External Interrupt, a RTC alarm wakeup and other wakeup events, the PLL is turned “ON” automatically. However, the clock supply scheme is quite different. The initial-state of the S5PV210 after wake-up from the SLEEP mode is almost the same as the Power-On-Reset state except that the contents of the external DRAM is preserved. On the other hand, the S5PV210 automatically recovers the previous working state after wake-up from the STOP mode. The following *Table 4-8* shows the states of PLLs and internal clocks after wake-ups from the power-saving modes.

Table 4-8 The Status of PLL and SYSCLK After Wake-Up

Mode before wake-up	PLL on/off after wake up	SYSCLK after low power mode wake-up
IDLE	unchanged	PLL Output
DEEP-IDLE	off → on	PLL Output
STOP	off → on	PLL Output
DEEP-STOP	off → on	PLL Output
SLEEP	off → off	PLL reference clock

4.7.5 DAC

DAC has two power modes, namely, Run and Power-down mode

- In Run mode, DAC sends and receives data normally.
- In Power-down mode, all power to DAC is off internally.

In NORMAL mode, both power modes can be used. If DAC is in use, then it is in Run mode. Otherwise, it can enter into Power-down mode to save static power by setting register in TVOUT logic.

In IDLE mode, and DEEP-IDLE mode where TOP block is on, DAC keeps its operation or power state in NORMAL.

Before entry to DEEP-IDLE mode where TOP block is ”OFF”, STOP and SLEEP mode, it is recommended that DAC enter into Power-down mode.

4.7.6 ADC I/O

In DEEP-IDLE mode where TOP block is off, and DEEP-STOP mode where TOP block is off, the output port of normal I/O keeps its driving value before entering DEEP-IDLE/ DEEP-STOP mode. Normal I/O has output retention function, and it uses latch to keep its driving value. The retention control signal to input port (RTO, CPGI) of normal I/O is generated by SYSCON when entering DEEP-IDLE/ DEEP-STOP mode. RTO is first asserted to 1'b0 to latch the output value, and then CPGI is asserted to 1'b0 to prevent leakage path from power-off block. Finally, power-gating signal (nSCPRE, nSCALL) is asserted to 1'b0 to power off the block. RTO is 3.3V signal, and becomes 3.3V via level-shifter.

Alive I/O also keeps its driving value from power-off region before entering DEEP-IDLE/DEEP-STOP mode. SYSCON generates the retention control signal (CPGI).

In SLEEP mode, internal power to normal I/O is "OFF", and I/O power to normal I/O is still "ON". SYSCON generates the retention control signal (RTO and CPGI) while entering SLEEP mode. Alive I/O changes its output path from Normal path (power-off region) to ALIVE path (ALIVE module). RTO is asserted to 1'b0 to latch the output value. ALIVE module drives output value of alive I/O in SLEEP mode. Read value from alive I/O goes to ALIVE module. This read values acts as wakeup source in SLEEP mode.

4.7.7 POR

Power-On-Reset (POR) uses alive power. Thus, there is no power-down mode. The maximum current is up-to 10uA.

4.8 INTERNAL MEMORY CONTROL

Table 4-9 shows the internal memory power control summary.

Table 4-9 S5PV210 Internal Memory Control

	Block	Controlled by	NORMAL	IDLE/ DEEP-IDLE(1)	DEEP-IDLE(2) / STOP / DEEP-STOP	SLEEP
1	SRAM	SYSCON	Run / Stand-by	Keep operation or power state in NORMAL	Stand-by Retention / Power-down	(Power off)
2	ROM	SYSCON	Run / Stand-by / Power-down	Keep operation or power state in NORMAL	Stand-by / Power-down	(Power off)

4.8.1 SRAM

SRAM in TOP block has four power modes, namely, Run, Stand-by, Retention, and Power-down mode.

- In Run mode, read and write access to SRAM can be performed normally.
- In Stand-by mode, SRAM chip select is deactivated, so that there is no read and write access.
- In Retention mode, power is provided to only core of SRAM, and power to peripheral circuitry is ”OFF” internally.
- In Power-down mode, all power to core and peripheral circuitry is ”OFF”.

In NORMAL mode, run, or stand-by mode can be used.

Run mode is used when there is read and write access, while stand-by mode is used when there is no read and write access. The change between these two modes can be done by module that has SRAM.

In IDLE mode, and DEEP-IDLE mode where TOP block is ”ON”, SRAM keeps its operation or power state in NORMAL.

In DEEP-IDLE mode where TOP block is ”OFF”, SRAM in TOP module can enter stand-by, retention, or power-down mode. Before entering this mode, you must set the TOP_MEMORY field IDLE_CFG in SYSCON.

In STOP mode and DEEP-STOP mode, stand-by, retention, and power-down mode can be entered.

Before entry to STOP mode, you must set the TOP_MEMORY field of STOP_CFG register in SYSCON to determine which power mode SRAM will enter during STOP mode.

In SLEEP mode, power to SRAM is off, so the data in SRAM will be lost. Power mode in SLEEP mode has no meaning.

4.8.2 ROM

ROM has three power modes, namely, Run, Stand-by, and Power-down mode.

- In Run mode, read access to ROM can be performed normally.
- In Stand-by mode, chip selection to ROM is deactivated, so that there is no read access.
- In Power-down mode, all power to core and peripheral circuitry is off internally.

In NORMAL mode, all three power modes can be used.

When ROM is in use, two power modes are available. Run mode is used when there is read access, while Standby mode is used when there is no read access. The decision to move from one mode to another is made by the internal ROM controller.

If ROM is not in use, then it can enter into Power-down mode. Set the IROM field of NORMAL_CFG register in SYSCON for Entry to, and exit from Power-down mode.

In IDLE mode, and DEEP-IDLE mode where TOP block is ”ON”, ROM keeps its operation or power state in NORMAL.

In DEEP-IDLE mode where TOP block is ”OFF”, STOP mode and DEEP-STOP mode, ROM can have two power states. If IROM bit of NORMAL_CFG is 1’b1, then ROM keeps stand-by mode. Otherwise, ROM keeps power down mode.

In SLEEP mode, power to ROM is ”OFF”, so the data in ROM will be lost. Power mode in SLEEP mode has no meaning.

4.9 RESET CONTROL

4.9.1 RESET TYPES

S5PV210 has four types of resets and reset generator can place the system into one of five reset states.

There are five reset states, namely:

- Hardware Reset - The hardware reset is generated when XnRESET is driven to low. It is an uncompromised, ungated, and total reset that is used to drive S5PV210 to a known initial state.
- Watchdog Reset - Reset signal by watchdog timer
- Software Reset - Reset signal by setting special control register
- Warm reset - Reset signal by XnWRESET pin.
- Wakeup Reset - Reset signal generated when a module that has normal F/Fs is powered down, and the module is powered up again by wakeup events; but in sleep mode, wakeup reset is generated to all modules that were powered off regardless of normal F/F or retention F/F.

Five resets have the following priorities:

Hardware Reset > Watchdog Reset > Warm Reset > Software Reset > Wakeup Reset

4.9.2 HARDWARE RESET

Hardware reset is asserted when the XnRESET pin is driven to low, and all units in the system (except RTC function module) are reset to known states.

During the hardware reset, the following actions take place:

- All internal registers and Cortex-A8 go into their pre-defined reset state.
- All pins get their reset state.
- The XnRSTOUT pin is asserted when XnRESET is driven.

Hardware reset is asserted when an external source drives the XnRESET input pin low. XnRESET is non-maskable, and therefore is always applicable. Upon assertion of XnRESET, S5PV210 enters into reset state regardless of the previous state. For hardware reset to be asserted actually, XnRESET must be held long enough to allow internal stabilization and propagation of the reset state.

Caution: Power regulator for system must be stable prior to the deassertion of XnRESET. If power regulator for system is not stable, it damages to S5PV210 and its operation is not guaranteed.

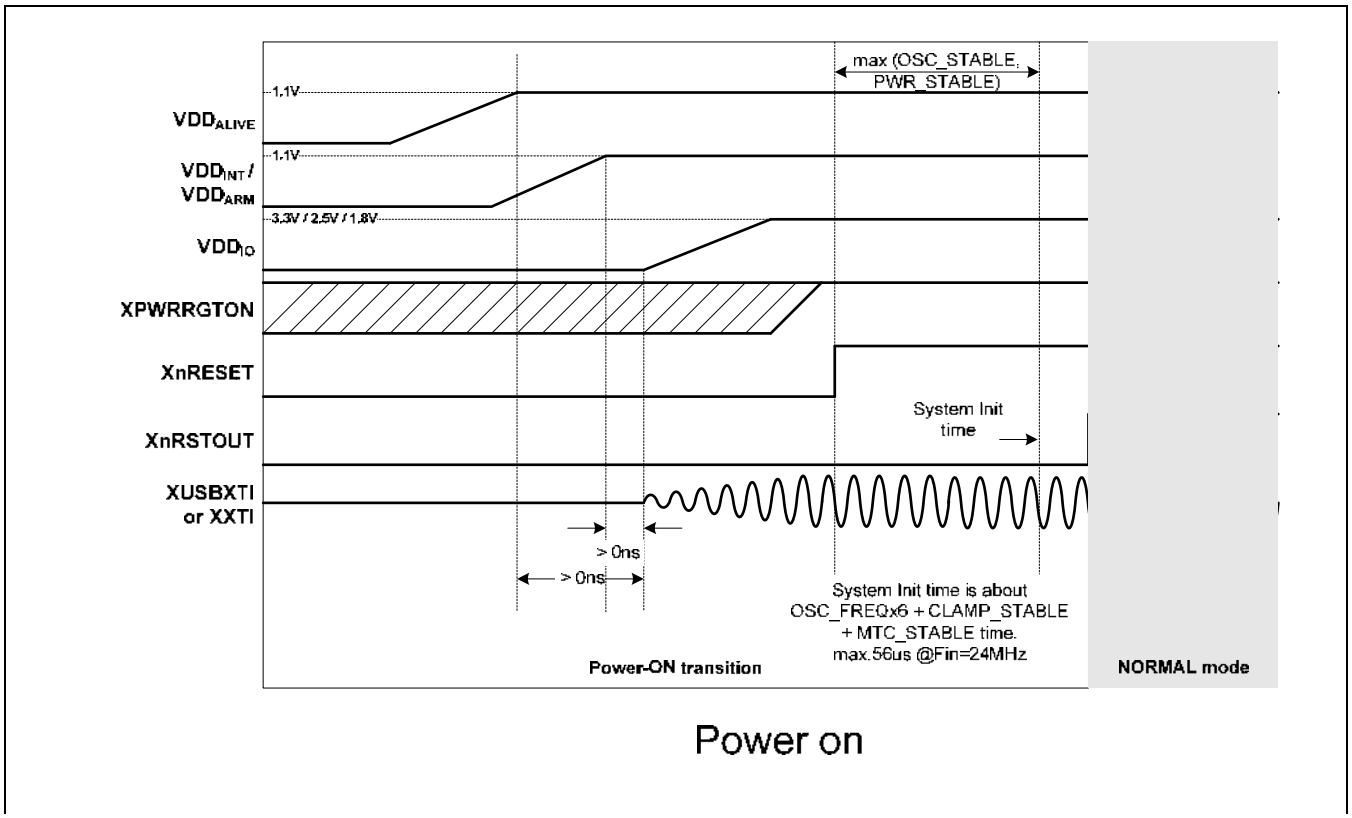
Figure 4-3 shows the clock behaviour during the power-on reset sequence. The crystal oscillator begins oscillation within several milliseconds after the power supply supplies enough power-level to the S5PV210. Internal PLLs are disabled after power-on reset is asserted. XnRESET signal should be released after the fully settle-down of the power supply-level. For the proper system operation, the S5PV210 requires a hazard-free system clock (SYSCLK, ARMCLK, HCLK and PCLK) when the system reset is released (XnRESET). However, since PLLs are disabled, Fin (the direct external oscillator clock) is fed directly to SYSCLK instead of the MPLL_CLK (PLL output) before the S/W configures the MPLLCON register to enable the operation of PLLs. If new P/M/S values are required, the S/W configures P/M/S field.

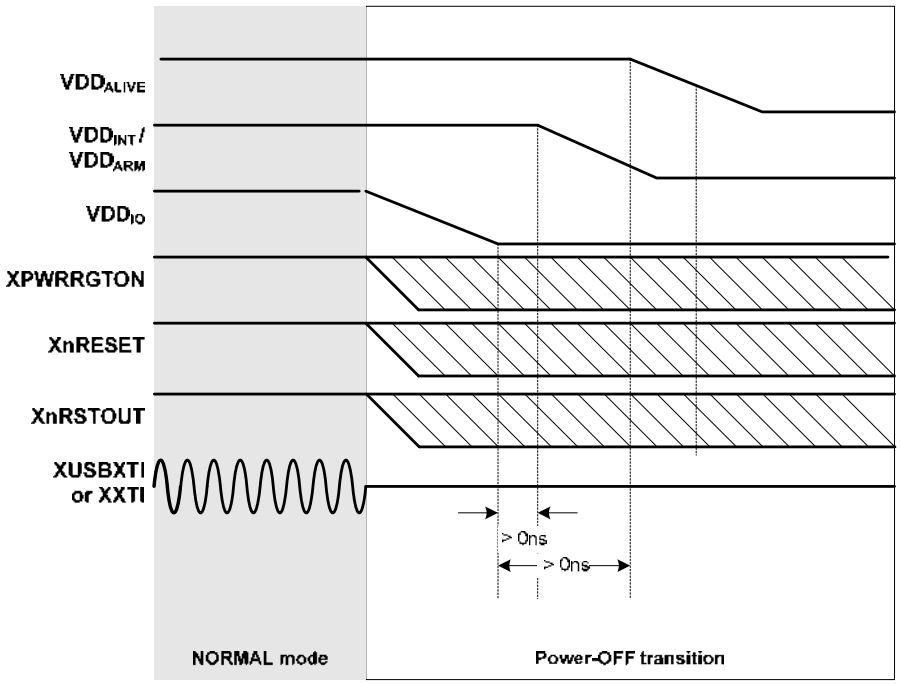
The PLL begins the lockup sequence toward the new frequency only after the S/W configures the PLL with a new frequency-value. SYSCLK is configured to be PLL output (MPLL_CLK) immediately after lock time.

The user should be aware that the crystal oscillator settle-down time is not explicitly added by the hardware during the power-up sequence. The S5PV210 assumes that the crystal oscillation is settled during the power-supply settle-down period. However, to ensure the proper operation during wake-up from the STOP mode, the S5PV210 explicitly adds the crystal oscillator settle-down time (the wait-time can be programmed using the OSC_STABLE registers) after wake-up from the STOP mode.

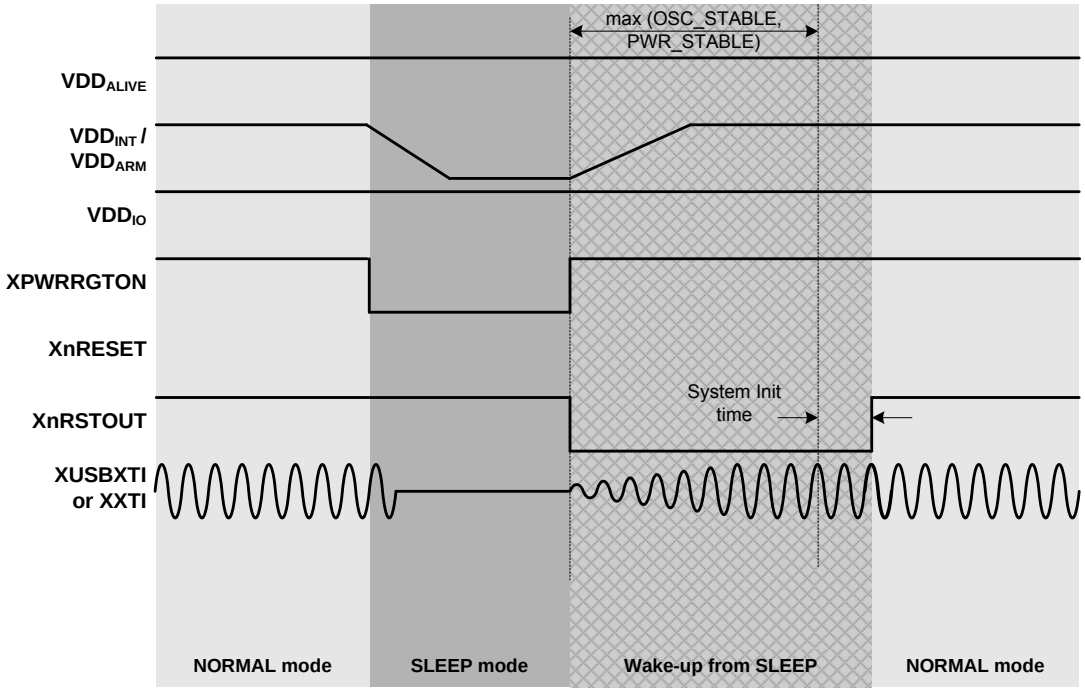
S5PV210 has four PLLs, namely, APLL, MPLL, EPLL, and VPLL.

- APLL: used to generate ARM clock
- MPLL: used to generate system bus clock and several special clocks
- EPLL: used to generate several special clocks
- VPLL: used to generate Video clocks. Usually, generates 54 MHz.





Power off



Sleep wakeup

Figure 4-3 Power ON/OFF & Sleep mode Enter/Exit Sequence

4.9.2.1 Watchdog Reset

Watchdog reset is asserted when software fails to prevent the watchdog timer from timing out. In watchdog reset all units in S5PV210 (except some blocks listed in *Table 4-10*) are reset to their predefined reset states. The behavior after Watchdog reset is asserted, is the same as Hardware reset case. (Refer to *4.9 "Reset Control*")

During the watchdog reset, the following actions occur:

- All units (except some blocks listed in *Table 4-10*) go into their pre-defined reset state.
- All pins get their reset state.
- The XnRSTOUT pin is asserted during watchdog reset.

Watchdog reset can be activated in NORMAL and IDLE (DEEP-IDLE) mode because watchdog timer can expire with clock.

Watchdog reset is asserted when watchdog timer and reset are enabled (WTCON[5] = 1, WTCON[0]=1) and watchdog timer is expired.

Watchdog reset is asserted then, the following sequence occurs:

1. WDT generate time-out signal.
2. SYSCON invokes reset signals and initialize internal IPs.
3. The reset including nRSTOUT will be asserted until the reset counter, RST_STABLE, is expired.

4.9.2.2 Software Reset

Software reset is asserted when CPU write “1” to SWRESET register in NORMAL mode.

During the software reset, the following actions occur:

- All units (except some blocks listed in *Table 4-10*) go into their pre-defined reset state.
- All pins get their reset state.
- The XnRSTOUT pin is asserted during software reset.

When Software reset is asserted the following sequence occurs.

1. SYSCON requests bus controller to finish current transactions.
2. Bus controller send acknowledge to SYSCON after completed bus transactions.
3. SYSCON request memory controller to enter into self refresh mode.
4. SYSCON wait for self refresh acknowledge from memory controller.
5. Internal reset signals and XnRSTOUT are asserted and reset counter is activated.
6. Reset counter is expired, then internal reset signals and XnRSTOUT are deasserted.

4.9.2.3 Warm Reset

Warm reset is asserted when XnWRESET is asserted to '0'.

During the warm reset, the following actions occur:

- All units (except some blocks listed in *Table 4-10*) go into their pre-defined reset state.
- All pins get their reset state.
- The XnRSTOUT pin is asserted during software reset.

When warm reset is asserted the following sequence occurs.

1. SYSCON requests bus controller to finish current transactions.
2. Bus controller send acknowledge to SYSCON after completed bus transactions.
3. SYSCON request memory controller to enter into self refresh mode.
4. SYSCON wait for self refresh acknowledge from memory controller.
5. Internal reset signals and XnRSTOUT are asserted and reset counter is activated.
6. Reset counter is expired, then internal reset signals and XnRSTOUT are deasserted.

4.9.2.4 Wakeup Reset

Wakeup reset is asserted when a module that has normal F/Fs is powered down, and the module is powered up again by wakeup events. Note that if the module has only retention F/Fs, wakeup reset is not asserted. However, in sleep mode, wakeup reset is generated to all modules that were powered off regardless of normal F/F or retention F/F.

Therefore, wakeup reset can be asserted in NORMAL, DEEP-IDLE, DEEP-STOP, and SLEEP mode.

In NORMAL mode, when a sub-domain is powered down, and the sub-domain is powered up again, wakeup reset is asserted to the sub-domain.

In DEEP-IDLE and DEEP-STOP mode, wakeup reset is asserted to Cortex-A8, since Cortex-A8 is powered up again when wakeup event occurs in these power modes. Wakeup reset is also asserted to a sub-block that becomes power on after exiting from DEEP-IDLE and DEEP-STOP mode.

Finally, wakeup reset is asserted when the system is waked up from sleep mode by wakeup event.

Register initialization due to various resets, is shown in *Table 4-10*.

Table 4-10 Register Initialization Due to Various Resets

Block	Register	Software Reset Warm Reset Wakeup from SLEEP	Watchdog	XnRESET	ALIVE Power On Reset
SYSCON (PMU)	INFORM4~6, OM_STAT	X	X	X	O
SYSCON (PMU)	RST_STAT, PS_HOLD_CONTROL	X	X	O	O
SYSCON (PMU)	OSC_CON, PWR_CFG, EINT_WAKEUP_MASK, WAKEUP_MASK, PWR_MODE, NORMAL_CFG, IDLE_CFG, STOP_CFG, STOP_MEM_CFG, SLEEP_CFG, OSC_FREQ, OSC_STABLE, PWR_STABLE, MTC_STABLE, CLAMP_STABLE, WAKEUP_STAT, BLK_PWR_STAT, OTHERS, HDMI_CONTROL, USB_PHY_CONTROL, MIPI_DPHY_CONTROL, ADC_CONTROL, DAC_CONTROL, INFORM0~3	X	O	O	O
RTC	RTCCON, TICCNT, RTCALM, ALMSEC, ALMMIN, ALMHOUR, ALMDAY, ALMMON, ALMYEAR, RTCRST	X	O	O	O
Others	-	O	O	O	O

4.10 REGISTER DESCRIPTION

Do not change any reserved area. Changing value of Reserved area can lead to undefined behavior.

4.10.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
OSC_CON	0xE010_8000	R/W	Crystal oscillator control register	0x0000_0003
Reserved	0xE010_8004 ~ 0xE010_9FFC		Reserved	0x0000_0000
RST_STAT	0xE010_A000	R	Reset status register	0x0000_0001
Reserved	0xE010_A004 ~ 0xE010_BFFC	R/W	Reserved	0x0000_0000
PWR_CFG	0xE010_C000	R/W	Configure power manager	0x0000_0000
EINT_WAKEUP_MASK	0xE010_C004	R/W	Configure EINT(external interrupt) mask	0x0000_0000
WAKEUP_MASK	0xE010_C008	R/W	Configure wakeup source mask	0x0000_0000
PWR_MODE	0xE010_C00C	R/W	Secondary entering method to power down mode	0x0000_0000
NORMAL_CFG	0xE010_C010	R/W	Configure power manager at NORMAL mode	0xFFFF_FFBF
Reserved	0xE010_C014 ~ 0xE010_C01C		Reserved	0x0000_0000
IDLE_CFG	0xE010_C020	R/W	Configure power manager at IDLE mode	0x6000_0000
Reserved	0xE010_C024 ~ 0xE010_C02C		Reserved	0x0000_0000
STOP_CFG	0xE010_C030	R/W	Configure power manager at STOP mode	0x9600_0000
STOP_MEM_CFG	0xE010_C034	R/W	Configure memory power at STOP mode	0x0000_00FF
Reserved	0xE010_C038 ~ 0xE010_C03C		Reserved	0x0000_0000
SLEEP_CFG	0xE010_C040	R/W	Configure power manager at SLEEP mode	0x0000_0000
Reserved	0xE010_C044 ~ 0xE010_C0FC		Reserved	0x0000_0000
OSC_FREQ	0xE010_C100	R/W	Oscillator frequency scale counter	0x0000_000F
OSC_STABLE	0xE010_C104	R/W	Oscillator pad stable counter	0x0000_FFFF
PWR_STABLE	0xE010_C108	R/W	Power stable counter	0x0000_FFFF
Reserved	0xE010_C10C		Reserved	0x0000_0000
MTC_STABLE	0xE010_C110	R/W	MTC stable counter	0xFFFF_FFFF
CLAMP_STABLE	0xE010_C114	R/W	Cortex-A8 CLAMP stable counter	0x03FF_03FF
Reserved	0xE010_C118 ~		Reserved	0x0000_0000

Register	Address	R/W	Description	Reset Value
	0xE010_C1FC			
WAKEUP_STAT	0xE010_C200	R/W	Wakeup status registers	0x0000_0000
BLK_PWR_STAT	0xE010_C204	R	Block power status register	0x0000_00BF
Reserved	0xE010_C208 ~ 0xE010_DFFC		Reserved	0x0000_0000
OTHERS	0xE010_E000	R/W	Others control register	0x0000_0000
Reserved	0xE010_E00C ~ 0xE010_E0FC	R/W	Reserved	0x0000_0000
OM_STAT	0xE010_E100	R	OM status register	0x0000_0000
Reserved	0xE010_E104 ~ 0xE010_E7FC		Reserved	0x0000_0000
Reserved	0xE010_E800	R/W	Reserved	0x0000_0001
HDMI_CONTROL	0xE010_E804	R/W	HDMI control register	0x0096_0000
Reserved	0xE010_E808		Reserved	0x0000_0000
USB_PHY_CONTROL	0xE010_E80C	R/W	USB PHY control register	0x0000_0000
DAC_CONTROL	0xE010_E810	R/W	DAC control register	0x0000_0001
MIPI_DPHY_CONTROL	0xE010_E814	R/W	MIPI DPHY control register	0x0000_0000
ADC_CONTROL	0xE010_E818	R/W	TS-ADC control register	0x0000_0000
PS_HOLD_CONTROL	0xE010_E81C	R/W	PS_HOLD control register	0x0000_5200
Reserved	0xE010_E81C ~ 0xE010_EFFC		Reserved	0x0000_0000
INFORM0	0xE010_F000	R/W	Information register0	0x0000_0000
INFORM1	0xE010_F004	R/W	Information register1	0x0000_0000
INFORM2	0xE010_F008	R/W	Information register2	0x0000_0000
INFORM3	0xE010_F00C	R/W	Information register3	0x0000_0000
INFORM4	0xE010_F010	R/W	Information register4	0x0000_0000
INFORM5	0xE010_F014	R/W	Information register5	0x0000_0000
INFORM6	0xE010_F018	R/W	Information register6	0x0000_0000
Reserved	0xE010_F020 ~ 0xE010_FFFC		Reserved	0x0000_0000

PMU SFRs consists of four parts. The first part, OSC_CON, controls the operation of external oscillators. The second part, RST_STAT, shows the reset status. Before entering into low power mode, S/W must set appropriate values for the third part. The final part has system control registers and user specific information registers.

4.10.2 CLOCK CONTROL REGISTER

Clock control register enables and disables all oscillators for S5PV210.

OSC_CON register control all oscillators for S5PV210. Each oscillator can be controlled independently. When oscillator pad is disabled, oscillation stops and no clock is generated further.

4.10.2.1 Clock Control Register (OSC_CON, R/W, Address = 0xE010_8000)

OSC_CON	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0x0000_0000
OSCUSB_EN	[1]	Control X-tal oscillator pad for USB (0: disable, 1: enable)	1
OSC_EN	[0]	Control X-tal oscillator pad for main oscillator (0: disable, 1: enable)	1

4.10.3 RESET CONTROL REGISTER

4.10.3.1 Reset Control Register (RST_STAT, R/W, Address = 0xE010_A000)

RST_STAT	Bit	Description	Initial State
Reserved	[31:20]	Reserved	0x000
DIDLE_WAKEUP	[19]	ARM reset from DEEP-IDLE	0
DSTOP_WAKEUP	[18]	ARM reset from DEEP-STOP	0
Reserved	[17]	Reserved	0
SLEEP_WAKEUP	[16]	Reset by SLEEP mode wake-up	0
Reserved	[15:4]	Reserved	0x000
SWRESET	[3]	Software reset by SWRESET	0
nWDTRESET	[2]	Watch dog timer reset by WDTRST	0
nWRESET	[1]	Warm reset by XnWRESET	0
nRESET	[0]	External reset by XnRESET	1

4.10.4 POWER MANAGEMENT REGISTER

4.10.4.1 Power Management Register (PWR_CFG, R/W, Address = 0xE010_C000)

PWR_CFG	Bit	Description	Initial State
Reserved	[31:10]	Reserved	0x00_0000
CFG_STANDBYWFI	[9:8]	Configure Cortex-A8 STANDBYWFI Determines what action is taken when the STANDBYWFI signal is activated by the Cortex-A8 00 = Enter IDLE mode 01 = Enter DEEPIDLE mode 10 = Enter STOP / DEEPSTOP mode 11 = Enter SLEEP mode	0x0
Reserved	[7:0]	Reserved	0x00

4.10.4.2 Power Management Register (EINT_WAKEUP_MASK, R/W, Address = 0xE010_C004)

EINT_WAKEUP_MASK	Bit	Description	Initial State
EINT_WAKEUP_MASK	[31:0]	External interrupt wake-up mask EINT[31:0] . The field affects on NORMAL mode. Therefore, this field must clear when EINT is used as a normal external interrupt source. 0 = Use as a wake-up source 1 = Disable	0x0000_0000

4.10.4.3 Power Management Register (WAKEUP_MASK, R/W, Address = 0xE010_C008)

WAKEUP_MASK	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0000
CEC	[15]	Wake-up mask for HDMI-CEC (0: pass, 1: mask)	0
ST	[14]	Wake-up mask for system timer (0: pass, 1: mask)	0
I2S	[13]	Wake-up mask for I2S within Audio sub-system (0: pass, 1: mask)	0
MMC3	[12]	Wake-up mask for MMC3 (0: pass, 1: mask)	0
MMC2	[11]	Wake-up mask for MMC2 (0: pass, 1: mask)	0
MMC1	[10]	Wake-up mask for MMC1 (0: pass, 1: mask)	0
MMC0	[9]	Wake-up mask for MMC0 (0: pass, 1: mask)	0
Reserved	[8]	Reserved	0
Reserved	[7]	Reserved	0
Reserved	[6]	Reserved	0
KEY	[5]	Wake-up mask for KEY I/F (0: pass, 1: mask)	0
TS1	[4]	Wake-up mask for TSADC1 (0: pass, 1: mask)	0
TS0	[3]	Wake-up mask for TSADC0 (0: pass, 1: mask)	0
RTC_TICK	[2]	Wake-up mask for RTC-TICK (0: pass, 1: mask)	0
RTC_ALARM	[1]	Wake-up mask for RTC-Alarm (0: pass, 1: mask)	0
Reserved	[0]	Reserved	0

4.10.4.4 Power Management Register (NORMAL_CFG, R/W, Address = 0xE010_C010)

NORMAL_CFG	Bit	Description	Initial State
Reserved	[31:21]	Reserved	0x7FF
IROM	[20]	Power gating control for I-ROM (0: LP mode (OFF), 1: Active mode (ON))	1
Reserved	[19:8]	Reserved	0xFFF
AUDIO	[7]	Power gating control for Audio sub-block (0: LP mode (OFF), 1: Active mode (ON))	1
Reserved	[6]	Reserved	1
CAM	[5]	Power gating control for X-block (0: LP mode (OFF), 1: Active mode (ON))	1
TV	[4]	Power gating control for T-block (0: LP mode (OFF), 1: Active mode (ON))	1
LCD	[3]	Power gating control for L-block (0: LP mode (OFF), 1: Active mode (ON))	1
G3D	[2]	Power gating control for G3D block (0: LP mode (OFF), 1: Active mode (ON))	1
MFC	[1]	Power gating control for F-block	1

		(0: LP mode (OFF), 1: Active mode (ON))	
Reserved	[0]	Reserved	1

Warning: Don't access SFR of modules whose block power is gated.

Warning: When block power is turned on, be sure to keep the clock running for the corresponding modules.

4.10.4.5 Power Management Register (IDLE_CFG, R/W, Address = 0xE010_C020)

IDLE_CFG	Bit	Description	Initial State
TOP_LOGIC	[31:30]	Configure TOP logic state 01 = Retention 10 = ON Other: Reserved	0x1
TOP_MEMORY	[29:28]	Configure TOP memory state 01 = Retention 10 = ON Other: Reserved	0x1
ARM_L2CACHE	[27:26]	Configure ARM L2 cache state in DEEP-IDLE mode 00 = OFF 01 = Retention Other: Reserved	0x0
Reserved	[25:1]	Reserved	0x000_0000
CFG_DIDLE	[0]	Configure DEEP-IDLE setting for Cortex-A8 core 0 = No DEEP (Cortex-A8 core power on) 1 = DEEP (Cortex-A8 core power off)	0

4.10.4.6 Power Management Register (STOP_CFG, R/W, Address = 0xE010_C030)

STOP_CFG	Bit	Description	Initial State
TOP_LOGIC	[31:30]	Configure TOP logic state 01 = Retention 10 = ON Other: Reserved. Writing reserved values to registers can lead to unexpected behavior. When ARM_LOGIC is set to 2'b10 (STOP mode), this field should be 2'b10.	0x2
TOP_MEMORY	[29:28]	Configure TOP memory state (DO NOT CHANGE) 01 = OFF/ Retention (According to STOP_MFM_CFG) Other: Reserved	0x1
ARM_L2CACHE	[27:26]	Configure ARM L2 cache state in STOP mode. When ARM_LOGIC is ON, L2CACHE is always ON regardless of this field setting. 00 = OFF 01 = Retention Other: Reserved	0x1
ARM_LOGIC	[25:24]	Configure ARM logic state in STOP/D-STOP mode 00 = OFF (D-STOP mode) 10 = ON (STOP mode) Other: Reserved	0x2
Reserved	[23:2]	Reserved	0x00_0000
OSCUSB_EN	[1]	Control XUSBXTI X-tal Oscillator pad in STOP mode (0: disable, 1: enable)	0
OSC_EN	[0]	Control XXTI X-tal Oscillator pad in STOP mode (0: disable, 1: enable)	0

4.10.4.7 Power Management Register (STOP_MEM_CFG, R/W, Address = 0xE010_C034)

STOP_MEM_CFG	Bit	Description	Initial State
Reserved	[31:9]	Reserved	0x00_0000
ONENAND	[8]	Memory retention control for ONENAND I/F (0: OFF, 1: Retention)	1
MODEMIF	[7]	Memory retention control for MODEM I/F (0: OFF, 1: Retention)	1
Reserved	[6]	Reserved	1
USBOTG	[5]	Memory retention control for USB-OTG (0: OFF, 1: Retention)	1
HSMMC	[4]	Memory retention control for HSMMC (0: OFF, 1: Retention)	1
CSSYS	[3]	Memory retention control for CoreSight (0: OFF, 1: Retention)	1
SECSS	[2]	Memory retention control for security sub-system (0: OFF, 1: Retention)	1
IRAM	[1]	Memory retention control for internal RAM This field should be 0x1.	0x1
Reserved	[0]	Reserved	0x0

4.10.4.8 Power Management Register (SLEEP_CFG, R/W, Address = 0xE010_C040)

SLEEP_CFG	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0x0000_0000
OSCUSB_EN	[1]	Control XUSBXTI X-tal Oscillator pad in SLEEP mode (0: disable, 1: enable)	0
OSC_EN	[0]	Control XXTI X-tal oscillator pad in SLEEP mode (0: disable, 1: enable)	0

4.10.4.9 Power Management Register (OSC_FREQ, R/W, Address = 0xE010_C100)

OSC_FREQ	Bit	Description	Initial State
Reserved	[31:4]	Reserved	0x000_0000
OSC_FREQ_VALUE	[3:0]	Oscillator frequency scale counter. Clock count is based on FINPLL. (OSC_FREQ_VALUE / oscillator_frequency > 200ns) Recommended to use defualt value Ex) 1 count time = 1/24Mhz = 41.7ns	0xF

4.10.4.10 Power Management Register (OSC_STABLE, R/W, Address = 0xE010_C104)

OSC_STABLE	Bit	Description	Initial State
Reserved	[31:20]	Reserved	0x000
OSC_CNT_VALUE	[19:0]	20-bit oscillator stable counter value. It sets required period of time for oscillator to be stabilized. Whenever oscillator is turned on, corresponding counter increments from zero until it gets 16 times as big as this field value. The reference clock for the counter is external oscillator clock input (FINPLL). Ex) If stable oscillation time of used 24Mhz crystal is 2ms, 1 count time = 1/24Mhz x 16 = 666.7ns Counts for 2 ms = 2ms / 666.7ns = 3000 (0xBB8)	0x0_FFFF

4.10.4.11 Power Management Register (PWR_STABLE, R/W, Address = 0xE010_C108)

PWR_STABLE	Bit	Description	Initial State
Reserved	[31:20]	Reserved	0x000
PWR_CNT_VALUE	[19:0]	20-bit power stable counter value. It sets required period of time for external power regulator to be stabilized. Whenever external power regulator is turned on, corresponding counter increments from zero until it gets 16 times as big as this field value. The reference clock for the counter is external oscillator clock input (FINPLL). Ex) If max. stable power-up time of VDD_ARM and VDD_INT is 50us, @FINPLL=24MHz 1 count time = 1/24Mhz x 16 = 666.7ns Counts for 50us = 50us / 666.7ns = 75 (0x4B)	0x0_FFFF

4.10.4.12 Power Management Register (MTC_STABLE, R/W, Address = 0xE010_C110)

MTC_STABLE	Bit	Description	Initial State
AUDIO	[31:28]	Memory power stabilization counter for Audio sub-block Corresponding counter increments from zero until it gets 64 times as big as this field value. The reference clock for the counter is external oscillator clock input (FINPLL). Ex) 1 count time = 1/24Mhz x 64 = 2.6us The following bit fields(CAM, TV, …) are applied just as well.	0xF
Reserved	[27:24]	Reserved	0x0
CAM	[23:20]	Memory power stabilization counter for CAM-block	0xF
TV	[19:16]	Memory power stabilization counter for TV-block	0xF
LCD	[15:12]	Memory power stabilization counter for LCD-block	0xF
G3D	[11:8]	Memory power stabilization counter for G3D block	0xF
MFC	[7:4]	Memory power stabilization counter for MFC-block	0xF
TOP	[3:0]	Memory power stabilization counter for TOP block	0xF

MTC_STABLE counter indicates time required for power supplies to be stabilized when sub-block power is turned “ON”. Unless commented, use the default values.

4.10.4.13 Power Management Register (CLAMP_STABLE, R/W, Address = 0xE010_C114)

CLAMP_STABLE	Bit	Description	Initial State
Reserved	[31:26]	Reserved	0x00
CLAMP_OFF_VALUE	[25:16]	Clamp OFF counter value Clock count is based on FINPLL. Ex) 1 count time = 1/24Mhz = 41.7ns	0x3FF
Reserved	[15:10]	Reserved	0x00
CLAMP_ON_VALUE	[9:0]	Clamp ON counter value Clock count is based on FINPLL. Ex) 1 count time = 1/24Mhz = 41.7ns	0x3FF

CLAMP_STABLE counter indicates time required for power supplies to be stabilized when Cortex processor power is turned “ON” or turned “OFF”. Unless commented, use the default values.

4.10.4.14 Power Management Register (WAKEUP_STAT, Address = R/W, 0xE010_C200)

WAKEUP_STAT	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0000
CEC	[15]	Wake-up by HDMI-CEC. This is cleared by writing 1.	0
ST	[14]	Wake-up by system timer. This is cleared by writing 1.	0
I2S	[13]	Wake-up by I2S within Audio sub-system. This is cleared by writing 1.	0
MMC3	[12]	Wake-up by MMC3. This is cleared by writing 1.	0
MMC2	[11]	Wake-up by MMC2. This is cleared by writing 1.	0
MMC1	[10]	Wake-up by MMC1. This is cleared by writing 1.	0
MMC0	[9]	Wake-up by MMC2. This is cleared by writing 1.	0
Reserved	[8]	Reserved	0
Reserved	[7]	Reserved	0
Reserved	[6]	Reserved	0
KEY	[5]	Wake-up by KEY I/F. This is cleared by writing 1.	0
TS0	[4]	Wake-up by TSADC1. This is cleared by writing 1.	0
TS1	[3]	Wake-up by TSADC0. This is cleared by writing 1.	0
RTC_TICK	[2]	Wake-up by RTC-TICK. This is cleared by writing 1.	0
RTC_ALARM	[1]	Wake-up by RTC-Alarm. This is cleared by writing 1.	0
EINT	[0]	Wake-up by EINT. This is cleared by writing 1.	0

4.10.4.15 Power Management Register (BLK_PWR_STAT, R, 0xE010_C204)

BLK_PWR_STAT	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0x0
AUDIO	[7]	Audio block power ready (0: OFF, 1: ON)	1
Reserved	[6]	Reserved	0
CAM	[5]	X-block power ready (0: OFF, 1: ON)	1
TV	[4]	T-block power ready (0: OFF, 1: ON)	1
LCD	[3]	L-block power ready (0: OFF, 1: ON)	1
G3D	[2]	G3D block power ready (0: OFF, 1: ON)	1
MFC	[1]	F-block power ready (0: OFF, 1: ON)	1
TOP	[0]	TOP power ready (0: OFF, 1: ON)	1

4.10.5 MISC REGISTER

4.10.5.1 MISC Register (OTHERS, R/W, Address = 0xE010_E000)

OTHERS	Bit	Description	Initial State
RELEASE_RET_GPIO	[31]	RELEASE_RET_GPIO is retention control signal to normal I/O pad. If you want to disable RELEASE_RET_GPIO, set to 1. After RELEASE_RET_GPIO becomes OFF, this bit will be cleared to 0. Usage1: Wakeup from IDLE, DEEP-IDLE, STOP, or DEEP-STOP with top-level logic ON -> No need to set this register field. Usage2: Wakeup from DEEP-IDLE, STOP, or DEEP-STOP with top-level logic OFF. -> Set HIGH on this register field to that corresponding PAD starts to work. Usage3: Wakeup from SLEEP. -> First restore GPIO configuration options to those values before entering SLEEP mode. And then set HIGH on this register field to that corresponding PAD starts to work. 0 = Auto clear 1 = RELEASE_RET_GPIO For more information on list of PADs belonging to normal I/O pad, refer to Section 4.2 PIN SUMMARY of GPIO manual.	0
RELEASE_RET_CF_IO	[30]	RELEASE_RET_CF_IO_IO is retention control signal to CF I/O pad. If you want to disable RELEASE_RET_CF_IO_IO, set to 1. After RELEASE_RET_CF_IO_IO becomes OFF, this bit will be cleared to 0. Usage1: Wakeup from IDLE, DEEP-IDLE, STOP, or DEEP-STOP with top-level logic ON -> No need to set this register field. Usage2: Wakeup from DEEP-IDLE, STOP, or DEEP-STOP with top-level logic OFF. -> Set HIGH on this register field to that corresponding PAD starts to work. Usage3: Wakeup from SLEEP. -> First restore GPIO configuration options to those values before entering SLEEP mode. And then set HIGH on this register field to that corresponding PAD starts to work. 0 = Auto clear 1 = RELEASE_RET_CF_IO_IO	0

OTHERS	Bit	Description	Initial State
		For more information on list of PADs belonging to MMC I/O pad, refer to Section 4.2 PIN SUMMARY of GPIO manual.	
RELEASE_RET_MMC_IO	[29]	RELEASE_RET_MMC_IO is retention control signal to MMC I/O pad. If you want to disable RELEASE_RET_MMC_IO, set to 1. After RELEASE_RET_MMC_IO becomes OFF, this bit will be cleared to 0. Usage1: Wakeup from IDLE, DEEP-IDLE, STOP, or DEEP-STOP with top-level logic ON -> No need to set this register field. Usage2: Wakeup from DEEP-IDLE, STOP, or DEEP-STOP with top-level logic OFF. -> Set HIGH on this register field to that corresponding PAD starts to work. Usage3: Wakeup from SLEEP. -> First restore GPIO configuration options to those values before entering SLEEP mode. And then set HIGH on this register field to that corresponding PAD starts to work. 0 = Auto clear 1 = RELEASE_RET_MMC_IO For more information on list of PADs belonging to MMC I/O pad, refer to Section 4.2 PIN SUMMARY of GPIO manual.	0
RELEASE_RET_UART_IO	[28]	RELEASE_RET_UART_IO is retention control signal to UART I/O pad. If you want to disable RELEASE_RET_UART_IO, set to 1. After RELEASE_RET_UART_IO becomes OFF, this bit will be cleared to 0. Usage1: Wakeup from IDLE, DEEP-IDLE, STOP, or DEEP-STOP with top-level logic ON -> No need to set this register field. Usage2: Wakeup from DEEP-IDLE, STOP, or DEEP-STOP with top-level logic OFF. -> Set HIGH on this register field to that corresponding PAD starts to work. Usage3: Wakeup from SLEEP. -> First restore GPIO configuration options to those values before entering SLEEP mode. And then set HIGH on this register field to that corresponding PAD starts to work. 0 = Auto clear	0

OTHERS	Bit	Description	Initial State
		1 = RELEASE_RET_UART_IO For more information on list of PADs belonging to UART I/O pad, refer to Section 4.2 PIN SUMMARY of GPIO manual.	
Reserved	[27:18]	Reserved	0x000
ARM_PRESETn_TYPE	[17]	ARM_PRESETn type selection 0 = Asserted when software reset is generated. 1 = Not asserted when software reset is generated.	0
Reserved	[16:10]	Reserved	0x00
CLKOUT	[9:8]	Control the XCLKOUT signal output. This bit is prior to CLK_OUT register value. When this bit is '10' or '11', XCLKOUT output selected clock is not only normal mode but also Top block off status and sleep mode. 00 = Clock out signal from SYSCON (by CLK_OUT SFR of CMU) 01 = Reserved 10 = XXTI (Main X-tal input) 11 = XUSBXTI (USB X-tal input)	0x0
Reserved	[7:2]	Reserved	0x00
CLEAR_DBGACK	[1]	Clear DBGACK signal when this field has value 1. Cortex-A8 asserts DBGACK signal to indicate the system has entered DEBUG state. If DBGACK is asserted, this state is stored in PMU until software clears it using this field.	0
SYSCON_INT_DISABLE	[0]	Disables new interrupt to reach processor core. Active HIGH. Setting this field to HIGH is a mandatory step when entering low-power mode. This field is automatically cleared when low-power mode entering sequence is completed.	0

4.10.5.2 MISC Register (OM_STAT, R, Address = 0xE010_E100)

OM_STAT	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0x000_0000
OM	[5:0]	Operation mode value	0x00

4.10.5.3 MISC Register (HDMI_CONTROL, R/W, Address = 0xE010_E804)

HDMI_CONTROL	Bit	Description	Initial State
Reserved	[31:26]	Reserved	0x00
DIV_RATIO	[25:16]	Clock divider ratio for HDMI	0x96
Reserved	[15:1]	Reserved	0x0000
ENABLE	[0]	HDMI PHY enable (0: disable, 1: enable)	0

4.10.5.4 MISC Register (USB_PHY_CONTROL, R/W, Address = 0xE010_E80C)

USB_PHY_CONTROL	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0x0000_0000
ENABLE1	[1]	USB PHY1(HOST) Enable selection (0: disable, 1: enable)	0
ENABLE0	[0]	USB PHY0(OTG device) Enable selection (0: disable, 1: enable)	0

4.10.5.5 MISC Register (DAC_CONTROL, R/W, Address = 0xE010_E810)

DAC_CONTROL	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0x0000_0000
ENABLE	[0]	DAC IP enable selection. This bit must be set to 1 at the system initialization step before data access from/to DAC begins. Caution: If DAC is not used in your system, do not touch this field. (0: disable, 1: enable)	0

4.10.5.6 MISC Register (MIPI_DPHY_CONTROL, R/W, Address = 0xE010_E814)

MIPI_DPHY_CONTROL	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0x0000_0000
M_RESETN	[2]	Isolate/Connect MIPI_PHY Master Logic from/to Link 0 : Isolate MIPI D-PHY Master Logic from DSI Link 1: Connect MIPI D-PHY Master Logic to DSI Link	0
S_RESETN	[1]	Isolate/Connect MIPI_PHY Slave Logic from/to Link 0 : Isolate MIPI D-PHY Slave Logic from CSI Link 1: Connect MIPI D-PHY Slave Logic to CSI Link	0
ENABLE	[0]	MIPI_DPHY enable selection. This bit must be set to 1 at the system initialization step before data access from/to MIPI_DPHY begins. Caution: If MIPI_DPHY is not used in your system, do not touch this bit. (0: disable, 1: enable)	0

4.10.5.7 MISC Register (ADC_CONTROL, R/W, Address = 0xE010_E818)

ADC_CONTROL	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0x0000_0000
DISABLE	[0]	TS-ADC enable control (0: disable, 1: enable)	1

4.10.5.8 MISC Register (PS_HOLD_CONTROL, R/W, Address = 0xE010_E81C)

PS_HOLD_CONTROL	Bit	Description	Initial State
Reserved	[31:12]	Reserved	0x00005
Reserved	[11:10]	Reserved	0
DIR	[9]	Direction (0: input, 1: output)	1
DATA	[8]	Driving value (0:low, 1:high)	0
Reserved	[7:1]	Reserved	0x00
PS_HOLD_OUT_EN	[0]	XEINT[0] pad is controlled by this register values and values of control registers for XEINT[0] of GPIO chapter is ignored when this field is '1'. (0: disable, 1: enable)	0

PS_HOLD (muxed with XEINT[0]) pin value is kept up in any power mode. This register is in alive region and reset by XnRESET or power off only.

4.10.5.9 MISC Register

- INFORM0, R/W, 0xE010_F000
- INFORM1, R/W, 0xE010_F004
- INFORM2, R/W, 0xE010_F008
- INFORM3, R/W, 0xE010_F00C
- INFORM4, R/W, 0xE010_F010
- INFORM5, R/W, 0xE010_F014
- INFORM6, R/W, 0xE010_F018

INFORMn	Bit	Description	Initial State
INFORM	[31:0]	User defined information register. INFORM0~3 registers are cleared by asserting XnRESET pin. INFORM4~6 registers are cleared by power off only.	0x0000_0000

5 INTELLIGENT ENERGY MANAGEMENT

5.1 OVERVIEW OF INTELLIGENT ENERGY MANAGEMENT

The Intelligent Energy Management (IEM) solution is designed primarily for battery-powered equipment, where the major requirement is to have long battery life. The IEM solution is ideal for portable applications, for example, smartphones, feature phones, Personal Digital Assistants (PDA), hand held games consoles and portable media players.

Figure 5-1 shows a high-level block diagram of a complete IEM solution.

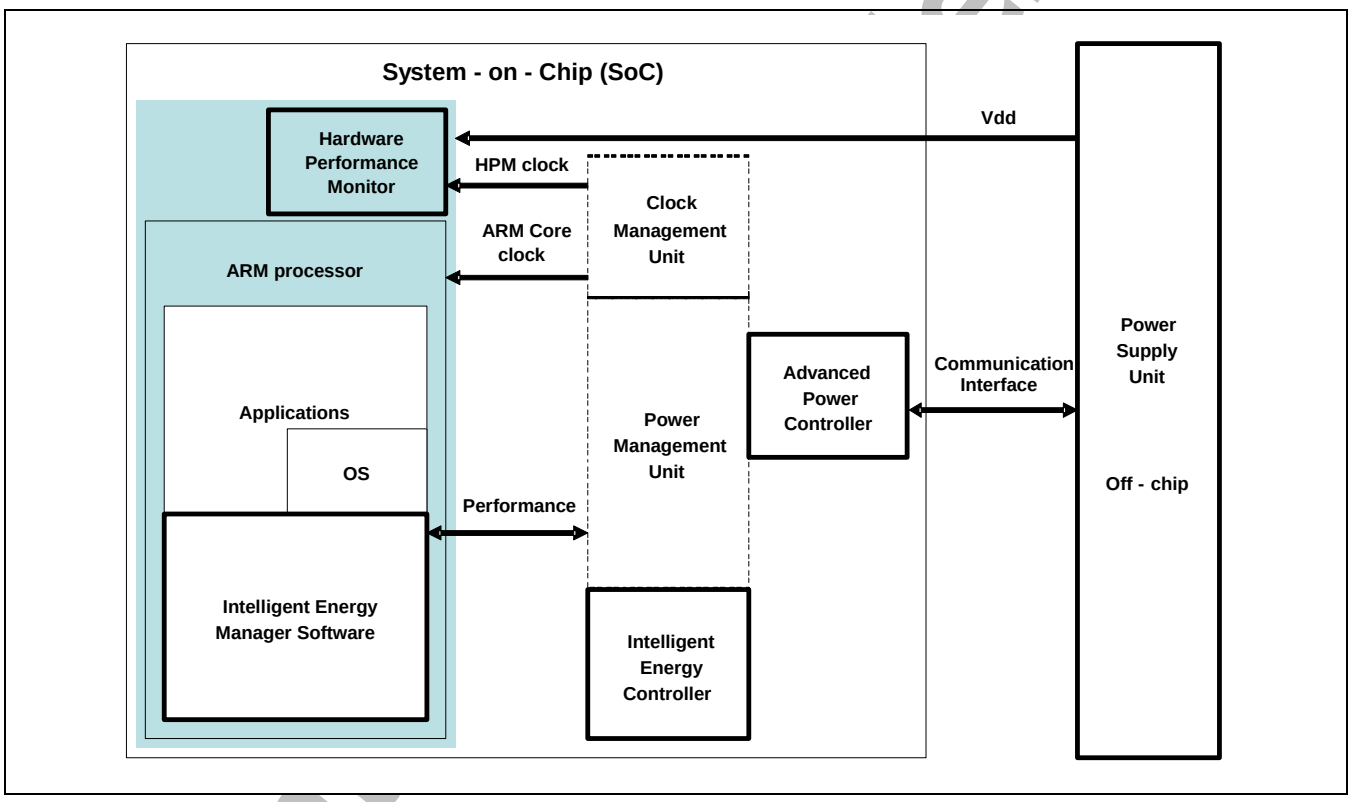


Figure 5-1 Intelligent Energy Manager Solution

An IEM system consists of the following components:

- An operating system (OS) modified to co-operate with the IEM software (An IEM-enabled OS).
- The IEM software, ported to the platform that you are using.
- Performance scaling hardware and appropriate drivers for that hardware.

The above listed components, which are part of the IEM system, co-operate with each other to optimize power consumption, without compromising on performance or responsiveness.

Work flow of IEM system:

- When the IEM software starts, software registers some kernel hooks with the OS.
- The OS uses these kernel hooks to invoke the IEM software. It does so whenever a system event occurs that might influence the optimum performance level.
- The IEM software records information about the events that occur, and the related tasks.
- The policies that are a part of the IEM software analyze this information to determine the optimum performance level.
- Whenever the optimum performance level changes, the IEM software uses the performance scaling hardware to set the new level.

5.1.1 KEY FEATURES OF INTELLIGENT ENERGY MANAGEMENT

The key features of IEM include:

- Up to eight energy level control
- Up to eight frequency level control
- Up to eight voltage level control
- Supports low power mode

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5.1.2 BLOCK DIAGRAM

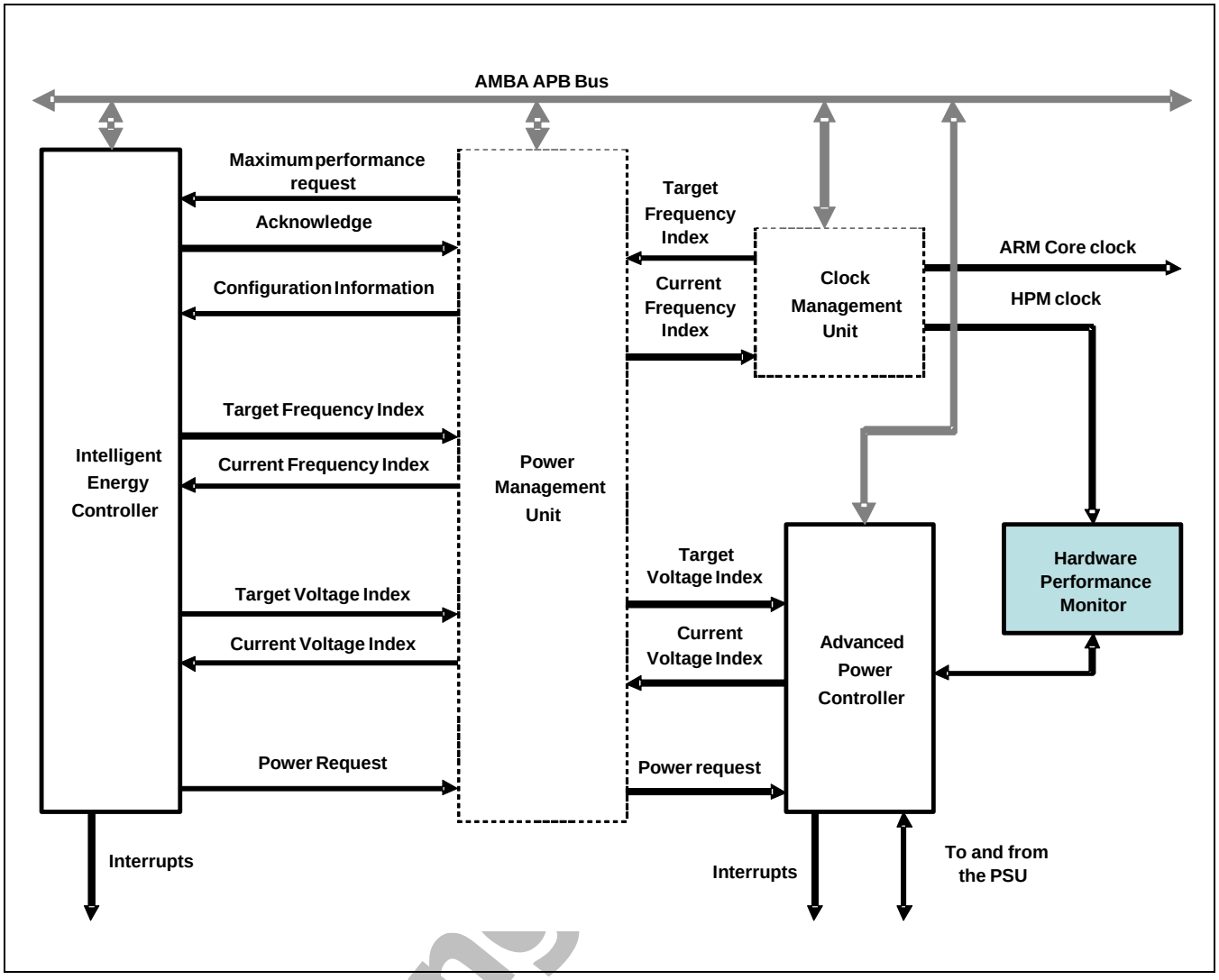

Figure 5-2 IEM Block Diagram

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5.2 FUNCTIONAL DESCRIPTION OF INTELLIGENT ENERGY MANAGEMENT

To support IEM, S5PV210 includes special IPs, namely:

- Intelligent Energy Controller
- Power Management Unit supporting IEM
- Clock Management Unit (CMU) supporting Dynamic Clock Generation
  - Clock Management Unit in System Controller acts as Dynamic Clock Generator
- Advanced Power Controller (APC1) supporting Dynamic Voltage Control
  - APC1 acts as Dynamic Voltage Controller
- Power Supply Unit supporting Dynamic Voltage Scaling
  - Power Supply Unit is the only off-chip component.
- Hardware Performance Monitor (HPM)
  - This is optional and required only for a closed loop system

Figure 5-2 shows the on-chip IEM components required for a complete solution of IEM and how each component are connected.

5.2.1 IEM SYSTEM COMPONENTS

5.2.1.1 Intelligent Energy Controller

The Intelligent Energy Controller (IEC) from ARM is designed to reuse in a wide variety of AMBA based designs and has a standard APB slave interface to program the registers. The IEC provides an Applications Programming Interface (API) for the IEM software. The IEC connects via defined interfaces to SoC-specific components such as the APC1.

The IEC uses prediction performance level requests from the IEM software. The performance setting is communicated to the IEC in order to control the System-on-Chip specific and product platform scaling hardware and to achieve desired system performance. Battery life is extended by lowering the operating frequency and voltage of SoC components, such as the processor, and consequently reducing energy consumption.

The IEC provides an abstracted view of the SoC-specific performance scaling hardware. It is responsible for translating the performance prediction made by the IEM software (0-100% of maximum performance) to an appropriate performance point at which the system runs and then controlling the scaling hardware to achieve operation at that target point. To achieve this, IEC sends a target performance request to the CMU and APC1.

The IEC also measures the work done in the system to ensure that the software deadlines are not missed. Additionally, the IEC supports a maximum performance hardware request feature. The IEC is designed to map to an implementation-defined set of index levels. You must configure the IEC to define the CMU frequencies and APC1 voltage levels that can be selected. These frequencies and voltages depend on the capabilities of the dynamic or adaptive power supply technology to support multiple operating performance points.

The IEC interfaces to the CMU and APC1 blocks via PMU through a thermometer encoded interface protocol, which indicates to the IEC the current performance level. This protocol is specified to support interfacing across asynchronous clock domains between high-speed PLL and clock-generator and low-speed voltage scaling hardware. The IEC provides an encoded performance index to S5PV210's CMU and APC1 blocks.

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The IEC also includes a Design for Test (DFT) interface. This enables easier control over the scaling hardware during production testing of the SoC device.

The IEC is an AMBA compliant, SoC peripheral that is developed, tested, and licensed by ARM Limited. The IEC features are as follows:

- AMBA APB compliant.
- Defined interfaces between the IEC and CMU/APC1 via PMU that is necessary for a complete energy management solution.
- An abstract interface to the underlying system-specific clock multiplexing and dynamic voltage or power control. This is through mapping to an implementation-defined set of index levels:
  - That correspond with the CMU frequencies that can be selected, and
  - That enables the voltage steps for the corresponding dynamic or adaptive power supply technology and consequently supports multiple operating performance points.
- An encoded interface protocol that provides a performance index to S5PV210x's CMU and APC1 blocks.
- Dynamic Voltage Scaling (DVS) emulation support enables a run fast then idle mode of operation.
- An API interface for efficient control and monitoring:
  - Implementation-independent fractional performance setting interface to support performance prediction algorithms without hard-coded frequencies.
  - Implementation-independent interrogation of performance-level quantization mapping levels to enable performance prediction software to adapt to the processor clock frequencies provided.
  - SoC-specific configuration interrogation, consisting of processor and IEC clock frequencies in kHz, and performance level mapping provided by the S5PV210x's CMU.
- Supports maximum performance signaling for real time subsystems that enables:
  - The maximum performance level to be requested regardless of the current programmed target performance level.
  - You to decide the events that activate this mode.
- Monitoring for IEM-specific algorithms, through a multi-channel interface designed to support automatic accumulation of system metrics.
- Supports synchronization handshaking with synchronous and asynchronous bridges to control entry and exit from maximum performance mode.
- Test registers for use in block and system level integration testing.
- System level integration testing using externally applied integration vectors.
- Debug mode to test clock generation with maximum voltage.
- ID support registers to port software driver compliance.

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5.2.1.2 DFT interface to control the target index outputs during SoC DFT. Advanced Power Controller

S5PV210 uses Advanced Power Controller (APC1) from National Semiconductor for Dynamic Voltage Control.

The APC1 is an advanced power controller designed for reuse in the AMBA-based designs with a standard APB slave interface to program registers. Based on the requested performance requirements from the CMU, the APC1 dynamically controls the EMU to provide sufficient voltage level to the SoC in order to achieve the performance level. This is the minimum voltage for the best power saving. APC1 uses a thermometer-encoded interface to receive target performance level requirements, and to send out current performance level updates indicating voltage readiness.

Together with the HPM, the APC1 tracks the system timing in real time, and sends voltage commands to the EMU to request the adjustment of voltage level. The flowchart in *Figure 5-3* shows how the adaptive voltage control is processed to find optimum voltage level.

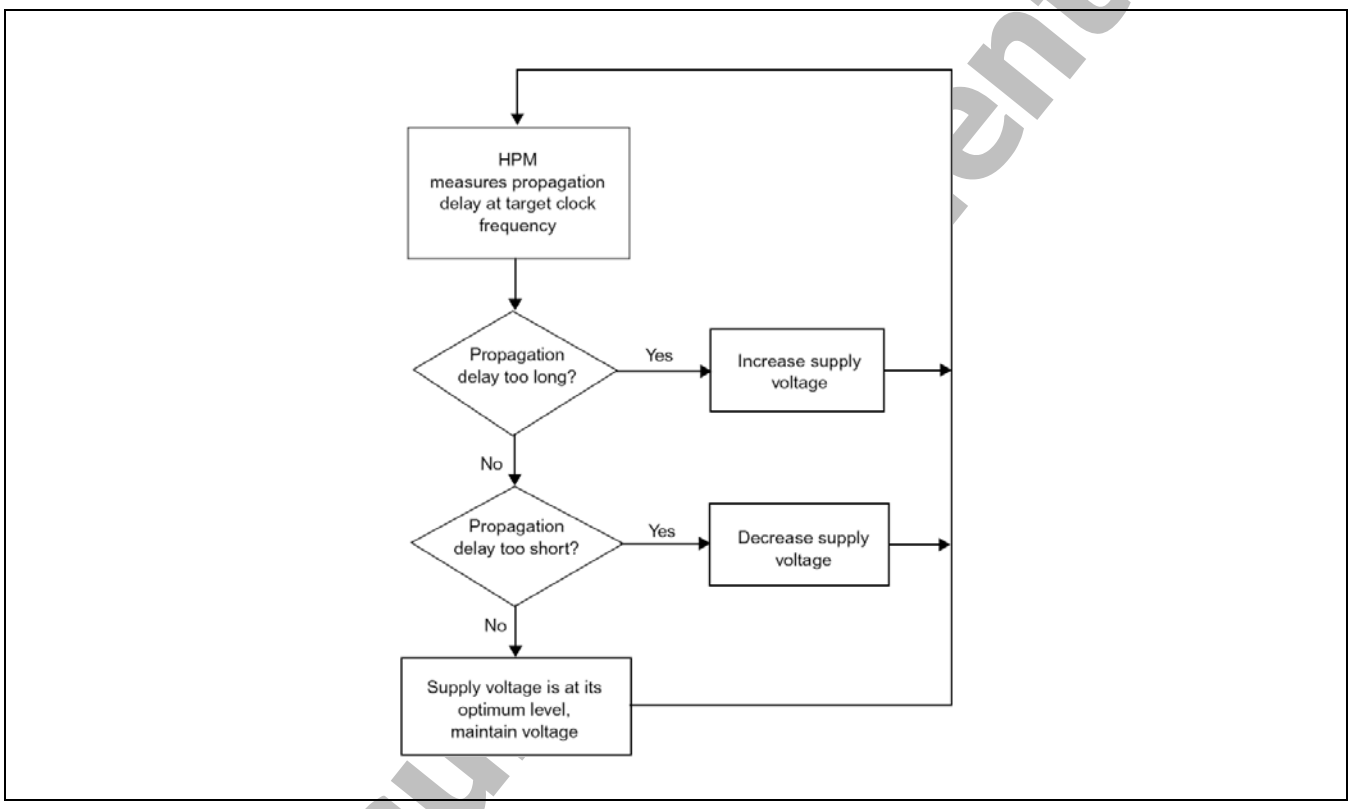

Figure 5-3 PowerWise Performance Tracking and Voltage Adjustment

If you require the open-loop Dynamic Voltage Scaling (DVS) voltage control you can use a built-in voltage table to request the EMU voltage level corresponding to the target performance level.

The APC1 is an AMBA APB-based SoC peripheral. The features are as follows:

- AMBA APB interface to program the registers
- PowerWise Interface™ (PWI) Rev 1.0 compliant master to control an external PWI-compliant power supply
- Supports the closed-loop AVS voltage control in conjunction with the HPM
- Voltage table to support the open-loop DVS

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- Supports thermometer-encoded interface for a target performance level request and a current performance level update
- Parameterized design supports up to eight performance levels
- Supports sleep mode (retention level) power-down
- Revision identification register to port software driver compliance
- DFT-ready for SCAN-based ATPG.

The APC1 receives the required target performance request from the IEC via PMU. This performance request is then translated to a voltage level that is communicated to the PSU through an interface such as the. The ARM and National Semiconductor jointly developed PWI to provide a high-speed and low-power control interface between an IEM-enabled SoC and an external power supply unit.

For an open loop system, the APC1 can either:

- Wait a programmed time that is dependent on the response time of the PSU, before signaling to the CMU that the target performance can be achieved
- Interrogate the PSU through the PWI for a VDD_OK signal indication.

If the PSU provides intermediate stable voltage level indication, then the APC1 can also determine this via the PWI.

5.2.1.3 Hardware Performance Monitor

The Hardware Performance Monitor (HPM) is designed for reuse and easy implementation. Although it is a separate entity in physical partition, the HPM is an integral part of the APC1 for an AVS power management system. The HPM is not a memory mapped device. An HPM is required for closed loop control, but not for an open loop control system.

The HPM tracks the system delay. The output of the HPM is a function of voltage level and the HPM clock. As shown in *Figure 5-3*, the HPM is embedded in the ARM Core voltage domain that is AVS controlled. It receives the clock from the CMU, and outputs are connected to the APC1. It translates voltage level into system delay information. APC1 uses the system delay information to determine the optimum voltage level for the target performance requirement.

To be short, the CMU supplies the target frequency required by the IEM software for that voltage domain, and the HPM informs the APC1 when this target frequency is detected.

The HPM design is structurally coded in the synthesizable RTL to facilitate ease of place and route. This is required to optimize the accuracy of the system delay tracking.

The HPM features are as follows:

- Configurable for a different target frequency
- Low power consumption overhead
- Low area overhead
- DFT-ready for SCAN based ATPG

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5.2.1.4 Power Management Unit

The Power Management Unit (PMU) in S5PV210X supports IEM features. The PMU provides configuration information to IEC, for example:

- Fractional index map, indicating the fractional levels supported
- Performance map, providing the mapping of the performance levels onto the clock frequencies supported by the CMU
- Maximum processor performance.

5.2.1.5 Clock Management Unit

In S5PV210X, Clock Management Unit (CMU) in System Controller supports Dynamic Clock Generation.

The CMU receives target performance requests from the IEC, via Power Management Unit (PMU). It generates the necessary clocks for the CPU, for example:

- Processor clock
- Peripheral clocks
- AMBA clock.

Additionally, for a more efficient design, the CMU must be capable to generate the different performance levels as indicated by the IEC. The CMU can also be a memory mapped AMBA peripheral and can contain both control and status registers.

The design of the CMU must meet the requirements set by the IEC and the Advanced Power Controller (APC1). These constraints are necessary to ensure optimum and correct performance of the Hardware Performance Monitor (HPM).

5.2.1.6 Power Supply Unit Supporting Dynamic Voltage Scaling

The Power Supply Unit (PSU) is the only off-chip component. The PSU provides the requested voltage to the SoC. It interfaces to the DVC through an interface such as the PWI. It ensures that the voltage targets specified by the DVC are provided to the SoC.

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5.2.2 IEM SYSTEM OPERATION

Loading and starting the software

At an appropriate stage of system boot-up, the OS loads and initializes the modules that contain the IEM software:

- On most platforms, the module loader automatically runs the initialization code for a module (if any)
- Else, the OS (or a driver) must call the initialization codlmee itself.

This initialization code performs most of the set up for the IEM software. For example:

- The code in the IEM HAL sets up and configures the performance scaling hardware
- The code in the control component loads the Comms driver that it uses to communicate with the IEM kernel.

The OS then configures the IEM kernel by issuing commands to the control component. The control component encodes these commands as messages, and uses the Comms driver to send them to the IEM kernel. These control messages:

- Start the policies, so that they are ready to use
- Optionally:
  - Configure the IEM activities that are traced
  - Enables tracing.

Finally, the OS issues a command to start the IEM kernel. When the IEM kernel receives the corresponding control message, it:

1. Allocates memory for the event queue, and initializes it.
2. Allocates memory for the IEM blocks, and initializes them.
3. Registers the kernel hooks that the OS calls whenever a system event occurs.

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5.2.2.1 Handling System Events

When an event occurs that might influence the optimum performance level, the OS calls the appropriate kernel hook in the IEM kernel:

- The New Task hook is called whenever a new task is created. This hook generates a New Task system event for the new task that has just been created.
- The Exit hook is called whenever a task is about to exit. This hook generates a Task Exit system event for the exiting task.
- The Task Switch hook is called whenever the OS switches from one task to another. This hook generates two system events:
  - A Task Schedule Out system event for the previous task that has just been switched out
  - A Task Schedule In system event for the next task that is being switched in.
- The User Input hook is called whenever a task receives user input. This hook generates a User Input system event for the task that is receiving input.

When a kernel hook generates an system event, it determines whether any event handlers recognize the system event. If so, it:

- Creates a structure describing the system event
- Ensures that there is an IEM block describing the corresponding task
- Runs the fast event handlers to process the system event.

The kernel hook then determines whether any standard event handlers recognize the system event. If so, the kernel hook adds the event to the event queue, for subsequent processing by the standard event handlers.

The kernel hook finally ensures that, if there are any system events in the event queue, the standard event handlers run within a given period.

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5.2.2.2 Running the Fast Event Handlers

The fast event handlers are run from the kernel hooks whenever a system event occurs.

For each policy, the IEM kernel determines whether its fast event handler recognizes the system event. If so, the IEM kernel runs the fast event handler, passing it pointers to the IEM kernel data structures that include:

- The system event structure describing the event
- The IEM block describing the task that triggered the system event.

The fast event handler then processes the event. Typical uses of the fast event handler include:

- Recognizing a task that requires an immediate change in performance level, and requesting that performance level. The fast event handler might recognize:
  - A specific task, such as a movie player
  - A type of task, such as real-time tasks, or tasks that are receiving user input.

If necessary, the fast event handler can get further information about the task by making calls to the OS layer API.

- Storing policy-specific information about the current state of the task or the system, for later processing by the standard event handler of the same policy. The fast event handler might get this information by making calls to the IEM HAL or OS layer APIs. It typically stores this information in arrays of memory that are allocated by the initialization function of the policy.

When the fast event handlers have been run, the IEM kernel then combines any performance requests that the fast event handlers are making, and sets the resulting performance level using the IEM HAL.

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5.2.2.3 Running the Standard Event Handlers

The standard event handlers are run periodically by the IEM kernel.

When the IEM kernel determines that it must run the standard event handlers, there are typically a number of outstanding system events in the event queue, that have not yet been processed by the standard event handlers. Starting with the oldest event, the IEM kernel processes each event in turn by enabling pre-emption, and then running the standard event handlers.

The standard event handlers are run in a very similar way to the fast event handlers. For each policy, the IEM kernel determines whether its standard event handler recognizes the system event. If so, the IEM kernel runs the standard event handler, passing it pointers to the IEM kernel data structures that include:

- The system event structure describing the event
- The IEM block describing the task that triggered the system event.

The standard event handler then processes the event, analyzing the data in the IEM kernel data structures and any data that was stored by the fast event handler to determine the optimum performance level. The analysis that the standard event handler performs is usually very different to that performed by the fast event handler of the same policy. This is because the standard event handler is working on historical data. Also, the standard event handler is pre-emptable, and so can spend longer analyzing the data without impacting system responsiveness. It can therefore use more complex algorithms, such as decaying weighted averages.

When the final outstanding event in the queue is processed, the standard event handlers can request a performance level. The IEM kernel then combines any performance requests that the standard event handlers are making, and sets the resulting performance level using the IEM HAL.

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5.3 IEM IMPLEMENTATION AND DRIVER SETTING

5.3.1 DEFINITION OF PERFORMANCE

The maximum frequency of APLL is 2GHz. The expected frequency range of ARM Core is from 166MHz to 800MHz. AXI_MSYS bus, which is connected to ARM Core, works at 166MHz.

In S5PV210X, CMU only uses clock divider to change performance. If you want to use PLL clock change, you should change PLL setting. With this specification, we should consider about number of the frequency levels as well as the resolution of each frequency level.

There are divider values for ARM Core clock, AXI_MSYS bus AXI clock and HPM clock when PLL output is 1600MHz as shown in table below.

Table 5-1 Example Divider Values for 1600MHz PLL Output

PLL Output (MHz)	ARM Core Clock Frequency (MHz)	HPM Clock Frequency (MHz)	AXI Bus Clock Frequency (MHz)	ARM Clock Ratio (f_{PLL}/f_{ARM})	HPM Clock Ratio (f_{ARM}/f_{HPM})	AXI Bus Clock Ratio (f_{PLL}/f_{AXI})	Performance mapping (%)
1600	800.0	100.0	160.0	2	8	10	100.0
	533.3	66.7		3			66.7
	400.0	50.0		4			50.0
	320.0	40.0		5			40.0
	266.7	33.3		6			33.3
	228.6	28.6		7			28.6
	200.0	25.0		8			25.0
	177.8	22.2		9			22.2
	160.0	20.0		10			20.0

There are divider values for ARM Core clock, AXI_MSYS bus AXI clock and HPM clock when PLL output is 833MHz as shown table below.

Table 5-2 Example Divider Values for 833MHz PLL Output

PLL Output (MHz)	ARM Core Clock Frequency (MHz)	HPM Clock Frequency (MHz)	AXI Bus Clock Frequency (MHz)	ARM Clock Ratio (f_{PLL}/f_{ARM})	HPM Clock Ratio (f_{ARM}/f_{HPM})	AXI Bus Clock Ratio (f_{PLL}/f_{AXI})	Performance mapping (%)
833	833.0	104.1	166.6	2	8	5	100.0
	416.5	52.1		3			50.0
	277.7	34.7		4			33.3
	208.3	26.0		5			25.0
	166.6	20.8		6			20.0

If you want to add more performance level above 50%, you should put PLL change scheme to CMU.

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5.3.2 HPM STRUCTURE AND CLOSED-LOOP BEHAVIOR

When IEM works with closed-loop, HPM and APC1 work as shown in *Figure 5-4* and *Figure 5-5*.

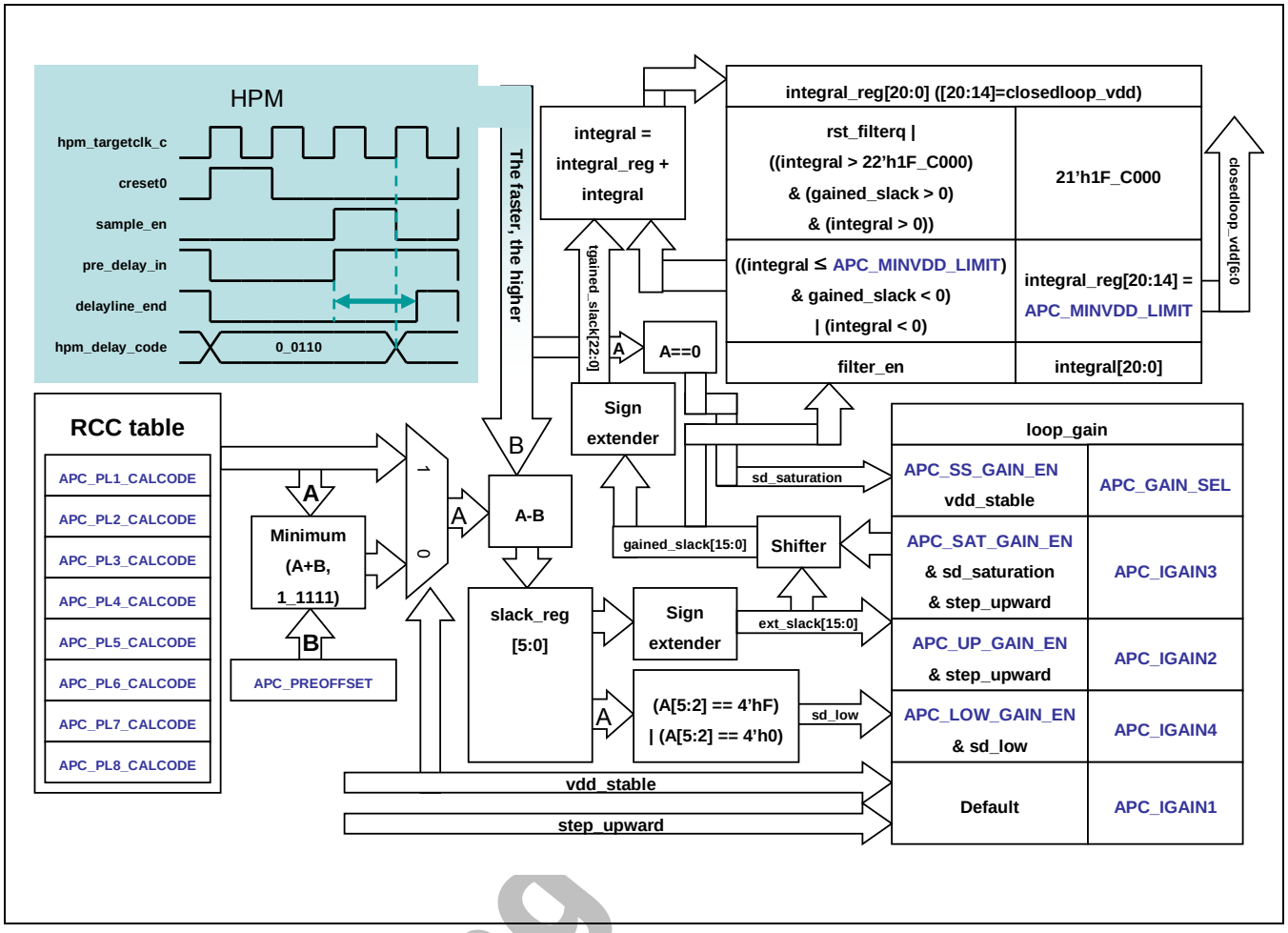

Figure 5-4 IEM Closed-Loop Voltage Generation Flow in HPM and APC1

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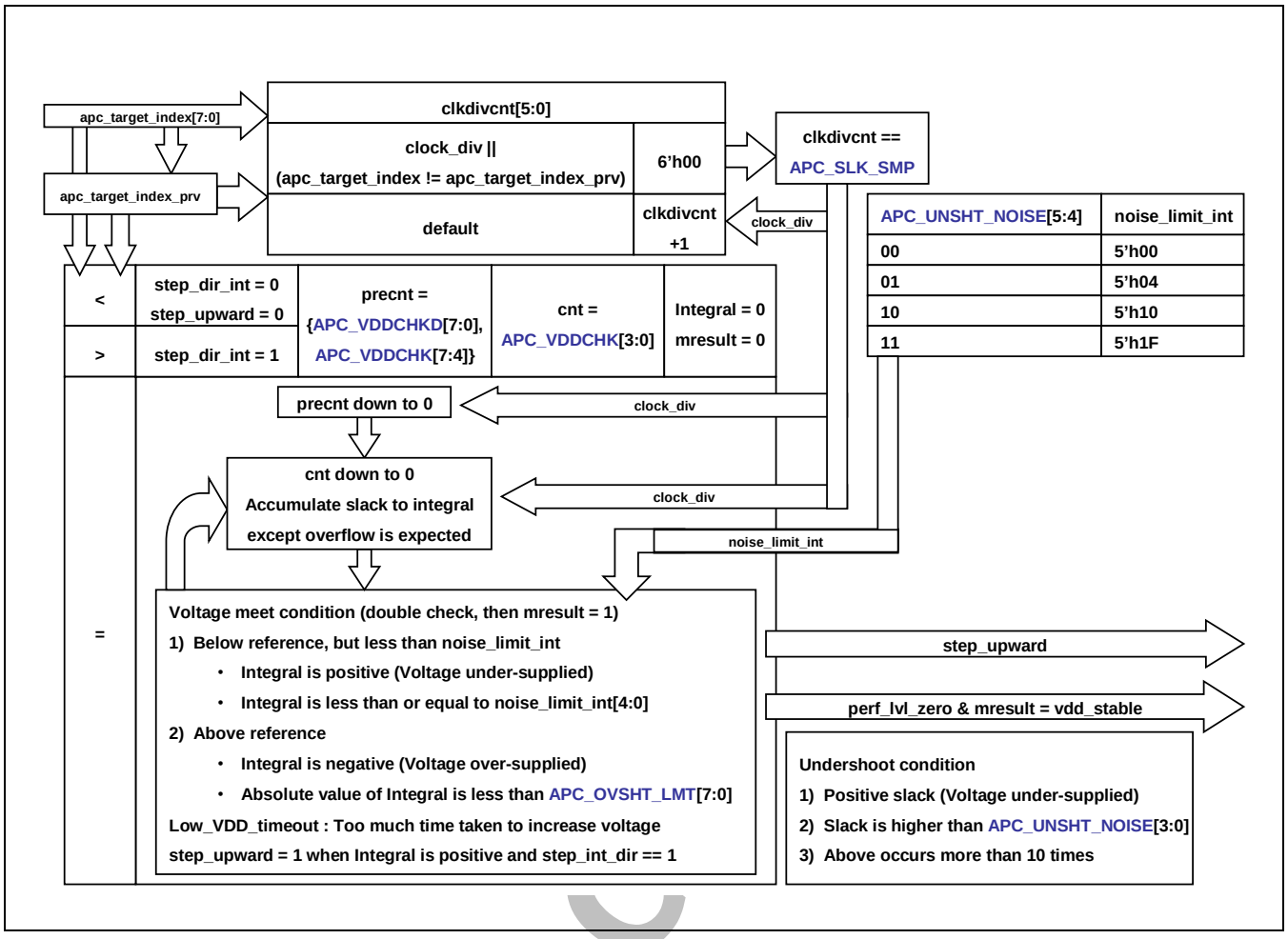

Figure 5-5 IEM Closed-Loop Control Flow in APC1 HPM Delay

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Critical path delay of ARM Core in S5PV210X is about 1.70ns in the worst condition. Delay of NOR2X1 cell is about 0.04609ns. One delay tap has four NOR2X1 cells and each delay tap gives 0.184ns delay. Delay tap structure is as shown in *Figure 5-6*.

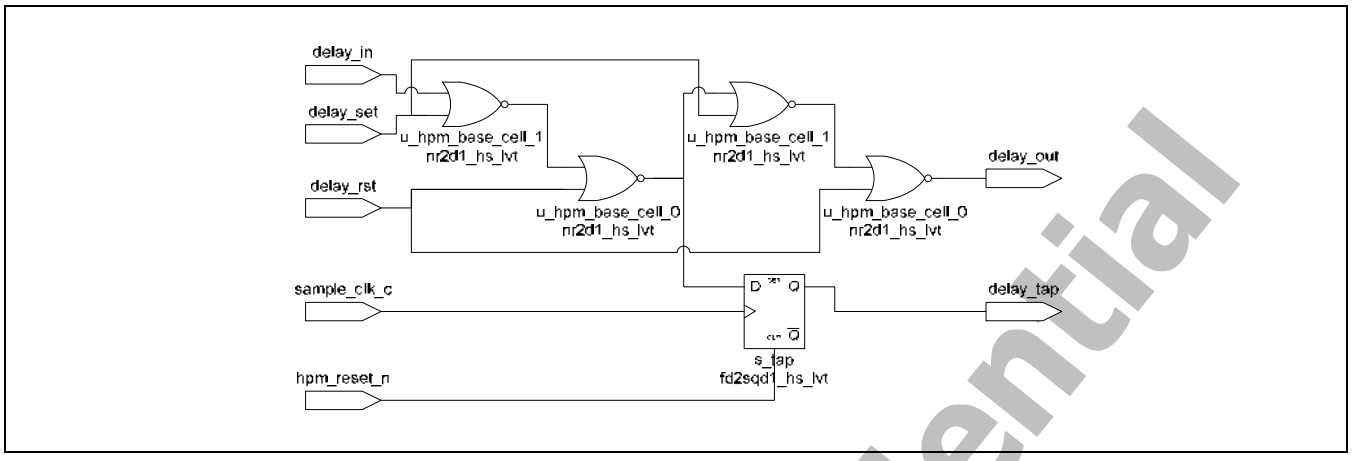

Figure 5-6 HPM Delay Tap structure in S5PV210

HPM has a predelay module that includes 32 delay tap-like delay elements and a delayline module that includes 32 delay taps. To correlate with ARM core, 14-th tap should be selected with setting predelay_sel[2:0] of HPM 3'b000 when HPM clock ratio is equal to 1.

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5.3.2.1 Calibration Code for Closed-loop

In closed-loop mode, Calibration codes are used to control voltage level, while voltage values in open-loop mode. Calibration code stands for critical path delay of ARM core. In S5PV210X, 14-th tap output of HPM has the nearly same delay to the critical path of ARM core (when HPM clock ratio is equal to 1), which can be encoded to the delay code 5'hE.

5.3.3 INITIALIZATION SEQUENCE

1. Initialize the index map & all other IEM & APC mapping values.
2. If IEM will use 'overdrive' level, then programs 'Max performance mapping index value' in IECDPCCR register with proper values (smaller than 3'b111)
3. Enables voltage scaling feature in the APC by setting 'APC_VDD_UD' bit in APC_CONTROL register as "1"
4. If IEM will use closed loop mode, then programs 'APC_HPM_EN' bit & 'APC_LOOP_MODE' bit in APC_CONTROL register as "1"
5. Start IEM HW by setting 'iem_enable' bit in IEM_CONTROL register in power management unit as "1"
6. Start IEM control by setting "iec_enable" bit in IECDPCCR register as "1"
7. Now, the system is under the IEM control.

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5.4 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
IEM_SCLK	Bidirectional	PWI clock	IEM_SCLK	dedicated
IEM_SPWI	Bidirectional	PWI serial data	IEM_SPWI	dedicated

NOTE: Type field indicates whether pads are dedicated to the signal or pads are connected to the multiplexed signals.

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5.5 REGISTER DESCRIPTION

5.5.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
IEC				
IECDPCCR	0xE080_0000	R/W	DPC Control Register	0x000000E0
IECDVSEMSTR	0xE080_0004	R/W	DVS Emulation Slot Time Register	0x63
IECDPCTGTPERF	0xE080_0008	W	DPC Target Performance Register	0x80
IECDPCCRNTPERF	0xE080_000C	R	DPC Current Performance Register	System Dependent
IECIMSC	0xE080_0010	R/W	Interrupt Mask Set and Clear Register	0x3
IECRIS	0xE080_0014	R	Raw Interrupt Status Register	0x0
IECMIS	0xE080_0018	R	Masked Interrupt Status Register	0x0
IECICR	0xE080_001C	W	Interrupt Clear Register	0x0
IECCFGCPUFREQ	0xE080_0020	R	Configured CPU Frequency Register	From PMU
IECDPMFREQ	0xE080_0024	R	DPM Frequency Register	From PMU
IECCFGDCGIDXMAP00	0xE080_0040	R	Configuration Fractional Index Map0	From PMU
IECCFGDCGIDXMAP32	0xE080_0044	R	Configuration Fractional Index Map32	From PMU
IECCFGDCGIDXMAP64	0xE080_0048	R	Configuration Fractional Index Map64	From PMU
IECCFGDVCIDXMAP	0xE080_004C	R	Configuration DVC Index Map Register	From PMU
IECCFGDCGPERFMAP0	0xE080_0060	R	Configuration Performance Map 0	From PMU
IECCFGDCGPERFMAP4	0xE080_0064	R	Configuration Performance Map 4	From PMU
IECDPMCR	0xE080_0100	R/W	DPM Command Register	0x000
IECDPM2RATE	0xE080_0108	R/W	DPM Channel 2 Rate Register	0x80
IECDPM3RATE	0xE080_010C	R/W	DPM Channel 3 Rate Register	0x80
IECDPMILO	0xE080_0180	R	DPM Channel 1 Low Register	0x00000000
IECDPM1H1	0xE080_0184	R	DPM Channel 1 High Register	0x00000000
IECDPM2LO	0xE080_0188	R	DPM Channel 2 Low Register	0x00000000
IECDPM2HI	0xE080_018C	R	DPM Channel 2 High Register	0x00000000
IECDPM3LO	0xE080_0190	R	DPM Channel 3 Low Register	0x00000000
IECDPM3HI	0xE080_0194	R	DPM Channel 3 High Register	0x00000000
IECITCR	0xE080_0F00	R/W	Integration Test Control Register	0x0
IECITIP1	0xE080_0F10	R/W	Integration Test Input Read or Set Register 1	0x00
IECITIP2	0xE080_0F14	R/W	Integration Test Input Read or Set Register 2	0x0
IECITIP3	0xE080_0F18	R/W	Integration Test Input Read or Set Register 3	0x00
IECITOP1	0xE080_0F20	R/W	Integration Test Output Read or Set Register 1	0x0

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Register	Address	R/W	Description	Reset Value
IECITOP2	0xE080_0F24	R/W	Integration Test Output Read or Set Register 2	0x00
IECITOP3	0xE080_0F28	R/W	Integration Test Output Read or Set Register 3	0x00
IECITCR	0xE080_0F00	R/W	Integration Test Control Register	0x0
IECPeriphID4	0xE080_0FD0	R	Peripheral Identification Register 4	0x03
IECPeriphID5	0xE080_0FD4	R	Peripheral Identification Register 5	0x08
IECPeriphID6	0xE080_0FD8	R	Peripheral Identification Register 6	Reserved
IECPeriphID7	0xE080_0FDC	R	Peripheral Identification Register 7	Reserved
IECPeriphID0	0xE080_0FE0	R	Peripheral Identification Register 0	0x50
IECPeriphID1	0xE080_0FE4	R	Peripheral Identification Register 1	0x17
IECPeriphID2	0xE080_0FE8	R	Peripheral Identification Register 2	0x04
IECPeriphID3	0xE080_0FEC	R	Peripheral Identification Register 3	0x08
IECID0	0xE080_0FF0	R	IEC Identification Register 0	0x0D
IECID1	0xE080_0FF4	R	IEC Identification Register 1	0xF0
IECID2	0xE080_0FF8	R	IEC Identification Register 2	0x05
IECID3	0xE080_0FFC	R	IEC Identification Register 3	0xB1
APC				
APC_PWICMD	0xE070_0000	R/W	PWI Command Register	0x00
APC_PWIDATAWR	0xE070_0004	R/W	PWI Write Data Register	0x00
APC_PWIDATARD	0xE070_0008	R	PWI Read Data Register	0x00
APC_CONTROL	0xE070_0010	R/W	APC Control Register	0x00
APC_STATUS	0xE070_0014	R	APC Status Register	0x00
APC_MINVDD_LIMIT	0xE070_0018	R/W	Minimum Limit Register	0x00
APC_VDDCHK	0xE070_001C	R/W	VDD Check Register	0x00
APC_VDDCHKD	0xE070_0020	R/W	VDD Delay Time Register	0x00
APC_PREDLYSEL	0xE070_0024	R/W	VDD Pre-delay Select Register	0x07
APC_IMASK	0xE070_0028	R/W	APC Interrupt Mask Register	0x00
APC_ISTATUS	0xE070_002C	R	APC Interrupt Status Register	0x00
APC_ICLEAR	0xE070_0030	W	APC Interrupt Clear Register	0x00
APC_UNSH_NOISE	0xE070_0034	R/W	APC Undershoot Threshold and Noise Limit Register	0x00
APC_WKUP_DLY	0xE070_0038	R/W	Wakeup Delay Register	0x00
APC_SLK_SMP	0xE070_003C	R/W	Slack Sample Count Register	0x00
APC_CLKDIV_PWICLK	0xE070_0040	R/W	PWI Clock Division Register	0x00
APC_OVSHT_LMT	0xE070_0050	R/W	APC Overshoot Limit Register	0x00
APC_CLP_CTRL	0xE070_0054	R/W	APC Closed-loop Control	0x00
APC_SS_SRATE	0xE070_0058	R/W	APC Steady State Slew Rate Register	0x00

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Register	Address	R/W	Description	Reset Value
APC_IGAIN4	0xE070_005C	R/W	Integrator's Gain 4 Register	0x00
APC_IGAIN1	0xE070_0060	R/W	Integrator's Gain 1 Register	0x00
APC_IGAIN2	0xE070_0064	R/W	Integrator's Gain 2 Register	0x00
APC_IGAIN3	0xE070_0068	R/W	Integrator's Gain 3 Register	0x00
APC_ITSTCTRL	0xE070_006C	R/W	Integration Test Control Register	0x00
APC_ITSTIP1	0xE070_0070	R/W	Integration Test Input Read or Set Register 1	0x00
APC_ITSTIP2	0xE070_0074	R/W	Integration Test Input Read or Set Register 2	0x00
APC_ITSTOP1	0xE070_0078	R/W	Integration Test Output Read or Set Register 1	0x00
APC_ITSTOP2	0xE070_007C	R/W	Integration Test Output Read or Set Register 2	0x00
APC_PL1_CALCODE	0xE070_0080	R/W	Calibration Code 1 Register	0x1F
APC_PL2_CALCODE	0xE070_0084	R/W	Calibration Code 2 Register	0x1F
APC_PL3_CALCODE	0xE070_0088	R/W	Calibration Code 3 Register	0x1F
APC_PL4_CALCODE	0xE070_008C	R/W	Calibration Code 4 Register	0x1F
APC_PL5_CALCODE	0xE070_0090	R/W	Calibration Code 5 Register	0x1F
APC_PL6_CALCODE	0xE070_0094	R/W	Calibration Code 6 Register	0x1F
APC_PL7_CALCODE	0xE070_0098	R/W	Calibration Code 7 Register	0x1F
APC_PL8_CALCODE	0xE070_009C	R/W	Calibration Code 8 Register	0x1F
APC_PL1_COREVDD	0xE070_00A0	R/W	Open-loop VDD Core Register 1	0x7F
APC_PL2_COREVDD	0xE070_00A4	R/W	Open-loop VDD Core Register 2	0x7F
APC_PL3_COREVDD	0xE070_00A8	R/W	Open-loop VDD Core Register 3	0x7F
APC_PL4_COREVDD	0xE070_00AC	R/W	Open-loop VDD Core Register 4	0x7F
APC_PL5_COREVDD	0xE070_00B0	R/W	Open-loop VDD Core Register 5	0x7F
APC_PL6_COREVDD	0xE070_00B4	R/W	Open-loop VDD Core Register 6	0x7F
APC_PL7_COREVDD	0xE070_00B8	R/W	Open-loop VDD Core Register 7	0x7F
APC_PL8_COREVDD	0xE070_00BC	R/W	Open-loop VDD Core Register 8	0x7F
APC_RET_VDD	0xE070_00C0	R/W	Retention VDD Register	0x00
APC_ITSTOP3	0xE070_00C4	R/W	Integration Test Output Read or Set Register 3	0x00
APC_DBG_DLYCODE	0xE070_00E0	R	Debug Performance Register	0x00
APC_REV	0xE070_00FC	R	Revision Number Register	0x01

NOTE: All registers of IEM interface are accessible by word unit with STR/LDR instructions.

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5.5.2 IEC RELATED REGISTERS

5.5.2.1 DPC Control Register (IECDPCCR, R/W, Address = 0xE080_0000)

IECDPCCR	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read undefined, do not modify.	0
Max Performance mapping index value	[7:5]	When IECMAXPERF goes high, the IEC requests maximum performance level which is decided by this register value. The reset value is 3'b111 which is literally max performance. However, if 3'b111 performance level needs overdrive, it is not desirable to overdrive SoC on every interrupt (MAXPERF case). In that case, software programs this register as lower value than the value needs overdrive.	0x7
Synchronous Mode Handshaking Enable	[4]	Enable/disable the use of the synchronous mode handshaking control signals. 0 = Synchronous mode handshaking disabled, also the reset value 1 = Synchronous mode handshaking enabled. When this bit is set, the synchronous mode handshaking signals are used to control entry and exit from the maximum performance mode. When this bit is cleared, the handshaking signals are not used.	0
IEC Software Debug Emulation	[3]	Control to debug performance scaling. 0 = IEC performance scaling software debug disabled, also the reset value 1 = IEC performance scaling software debug enabled. When this bit is seta, the performance level driven out of the IECTGTDVCIDX is set to maximum regardless of the software request. The performance level changes are only visible on IECTGTDCGIDX.	0
IEC Max Perf Enable	[2]	Enable/disable maximum performance mode override. 0 = IEC maximum performance mode disabled, also the reset value 1 = IEC maximum performance mode enabled. When this bit is set, the maximum performance mode is enabled and therefore whenever IECMAXPERF goes high, the IEC requests maximum performance level regardless of the current software request.	0
IEC PWM DVS En	[1]	Enable/disable the IEC PWM DVS mode. 0 = IEC PWM DVS mode disabled, also the reset value 1 = IEC PWM DVS mode enabled. When this bit is set, the IEC requests power through the IECPWRREQ output. The target performance index outputs are set to either maximum or minimum depending on the PWM state.	0
IEC Enable	[0]	Controls enabling and disabling of the IEC. 0 = IEC Disabled, also the reset value 1 = IEC Enabled When this bit is set, the IEC is enabled for performance scaling. When the bit is cleared, the IEC always requests maximum performance.	0

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5.5.2.2 DVS Emulation Slot Time Register (IECDVSEMSTR, R/W, Address = 0xE080_0004)

IECDVSEMSTR	Bit	Description	Initial State
Reserved	[31:10]	Reserved, read undefined, do not modify.	0
Slot time	[9:0]	The time in µs for each slot of a PWM frame. This is reset to 0x63. For example, if you want each time slot to be 100µs in length, then the slot time bits must be programmed with 0x63. Similarly, if you want each time slot to be 200µs in length, then the slot time bits must be programmed with 0xC7a.	0x63

5.5.2.3 DPC Target Performance Register (IECDPCTGTPERF, W, Address = 0xE080_0008)

IECDPCTGTPERF	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read undefined, do not modify.	0
IECDPCTGTPERF	[7:0]	Sets the target fractional performance level. At system reset, the value 0x80 (100%).	0x80

5.5.2.4 DPC Current Performance Register (IECDPCCRNTPERF, R, Address = 0xE080_000C)

IECDPCCRNTPERF	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read undefined, do not modify.	0
IECDPCCRNTPERF	[7:0]	Returns the current performance level as indicated to the IEC by the DCG on the IECCRNTDCGIDX inputs.	System Dependent

5.5.2.5 Interrupt Mask Set and Clear Register (IECIMSC, R/W, Address = 0xE080_0010)

IECIMSC	Bit	Description	Initial State
Reserved	[31:2]	Reserved, read undefined, do not modify.	0
CPU Sleep Interrupt Mask (CSIM)	[1]	On a read, the current mask of the CSIM is returned. On a write of 1, the mask of CSIM interrupt is set. A write of 0 clears the mask. The reset value is 1.	1
CPU Wake-up Interrupt Mask (CWIM)	[0]	On a read, the current mask of the CWIM is returned. On a write of 1, the mask of CWIM interrupt is set. A write of 0 clears the mask. The reset value is 1.	1

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5.5.2.6 Raw Interrupt Status Register (IECRIS, R, Address = 0xE080_0014)

IECRIS	Bit	Description	Initial State
Reserved	[31:2]	Reserved, read undefined, do not modify.	0
CPU Sleep Interrupt Status (CSRIS)	[1]	Returns the raw interrupt state prior to masking of the IECCPUSLPINT interrupt. The reset value is 0.	0
CPU Wake-up Interrupt Status (CWRIS)	[0]	Returns the raw interrupt state prior to masking of the IECCPUWUINT interrupt. The reset value is 0.	0

5.5.2.7 Interrupt Masked Interrupt Status Register (IECMIS, R, Address = 0xE080_0018)

IECMIS	Bit	Description	Initial State
Reserved	[31:2]	Reserved, read undefined, do not modify.	0
CPU Sleep Masked Interrupt Status (CSMIS)	[1]	Gives the masked interrupt state (after masking) of the IECCPUSLPINT interrupt. The reset value is 0.	0
CPU Wake-up Masked Interrupt Status (CWMIS)	[0]	Gives the masked interrupt state (after masking) of the IECCPUWUINT interrupt. The reset value is 0.	0

5.5.2.8 Interrupt Clear Register (IECICR, W, Address = 0xE080_001C)

IECICR	Bit	Description	Initial State
Reserved	[31:2]	Reserved, read undefined, do not modify.	0
CPU Sleep Interrupt Clear (CSIC)	[1]	Clears the IECCPUSLPINT interrupt. The reset value is 0.	0
CPU Wake-up Interrupt Clear (CWIC)	[0]	Clears the IECCPUWUINT interrupt. The reset value is 0.	0

5.5.2.9 Configured CPU Frequency Register (IECCFGCPUFREQ, R, Address = 0xE080_0020)

IECCFGCPUFREQ	Bit	Description	Initial State
Reserved	[31:24]	Reserved, read undefined, do not modify.	0
Configured CPU Frequency (CFGCPUF)	[23:0]	The configured CPU frequency in kHz.	From PMU

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5.5.2.10 DPM Frequency Register (IECDPMFREQ, R, Address = 0xE080_0024)

IECDPMFREQ	Bit	Description	Initial State
Reserved	[31:24]	Reserved, read undefined, do not modify.	0
DPM Frequency (DPMF)	[23:0]	The DPM frequency in kHz.	From PMU

5.5.2.11 Configuration Fractional Index Map00 Register (IECCFGDCGIDXMAP00, R, Address = 0xE080_0040)

IECCFGDCGIDXMAP00	Bit	Description	Initial State
IECCFGDCGIDXMAP00	[31:0]	State of IECCFGDCGIDXMAP [31:0]	From PMU

5.5.2.12 Configuration Fractional Index Map32 Register (IECCFGDCGIDXMAP32, R, Address = 0xE080_0044)

IECCFGDCGIDXMAP32	Bit	Description	Initial State
IECCFGDCGIDXMAP32	[31:0]	State of IECCFGDCGIDXMAP [63:32]	From PMU

5.5.2.13 Configuration Fractional Index Map32 Register (IECCFGDCGIDXMAP64, R, Address = 0xE080_0048)

IECCFGDCGIDXMAP64	Bit	Description	Initial State
IECCFGDCGIDXMAP64	[31:0]	State of IECCFGDCGIDXMAP [95:64]	From PMU

5.5.2.14 Configuration DVC Index Map Register (IECCFRDVCIDXMAP, R, Address = 0xE080_004C)

IECCFGDVCIDXMAP	Bit	Description	Initial State
-	[31:24]	Reserved, read undefined, do not modify.	0
IECCFGDVCIDXMAP	[23:0]	State of IECCFGDVCIDXMAP [23:0]	From PMU

5.5.2.15 Configuration Performance Map Register0 (IECCFGDCGPERFMAP0, R, Address = 0xE080_0060)

IECCFGDCGPERFMAP0	Bit	Description	Initial State
IECCFGDCGPERFMAP0	[31:0]	State of IECCFGDCGPERFMAP [31:0]	From PMU

5.5.2.16 Configuration Performance Map Register4 (IECCFGDCGPERFMAP4, R, Address = 0xE080_0064)

IECCFGDCGPERFMAP4	Bit	Description	Initial State
IECCFGDCGPERFMAP4	[31:0]	State of IECCFGDCGPERFMAP [63:32]	From PMU

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5.5.2.17 DPM Command Register (IECDPMCR, R/W, Address = 0xE080_0100)

IECDPMCR	Bit	Description	Initial State
Reserved	[31:12]	Reserved, read undefined, do not modify.	0
DPMCH3CMD	[11:8]	DPM Channel 3 command.	0
DPMCH2CMD	[7:4]	DPM Channel 2 command.	0
DPMCH1CMD	[3:0]	DPM Channel 1 command.	0

DPMCHxCMD	Command	Description	Initial State
b'0000	Freeze	The channel is frozen and stops accumulating. This is also the reset value.	0
b'0001	Reset	The channel is reset to zero.	0
b'0010	Accumulate	The channel starts accumulating.	0

5.5.2.18 DPM Channel Rate Registers (IECDPM2RATE, R/W, Address = 0xE080_0108)

IECDPM2RATE	Bit	Description	Initial State
-	[31:8]	Reserved, read undefined, do not modify.	0
IECDPM2RATE	[7:0]	The fractional rate that DPM channel 2 counts. The reset value of this register is 0x80, that is, 100%.	0x80

5.5.2.19 DPM Channel Rate Registers (IECDPM3RATE, R/W, Address = 0xE080_010C)

IECDPM3RATE	Bit	Description	Initial State
-	[31:8]	Reserved, read undefined, do not modify.	0
IECDPM3RATE	[7:0]	The fractional rate that DPM channel 3 counts. The reset value of this register is 0x80, that is, 100%.	0x80

5.5.2.20 DPM Channel Registers (IECDPM1LO, R, Address = 0xE080_0180)

IECDPM1LO	Bit	Description	Initial State
IECDPM1LO	[31:0]	Low 32-bit of DPM channel 1. The reset value is 0x00000000.	0x00000000.

5.5.2.21 DPM Channel Registers (IECDPM1HI, R, Address = 0xE080_0184)

IECDPM1HI	Bit	Description	Initial State
IECDPM1HI	[31:0]	High 32-bit of DPM channel 1. The reset value is 0x00000000.	0x00000000

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5.5.2.22 DPM Channel Registers (IECDPM2LO, R, Address = 0xE080_0188)

IECDPM2LO	Bit	Description	Initial State
IECDPM2LO	[31:0]	Low 32-bit of DPM channel 2. The reset value is 0x00000000.	0x00000000

5.5.2.23 DPM Channel Registers (IECDPM2HI, R, Address = 0xE080_018C)

IECDPM2HI	Bit	Description	Initial State
IECDPM2HI	[31:0]	High 32-bits of DPM channel 2. The reset value is 0x00000000.	0x00000000

5.5.2.24 DPM Channel Registers (IECDPM3LO, R, Address = 0xE080_0190)

IECDPM3LO	Bit	Description	Initial State
IECDPM3LO	[31:0]	Low 32-bits of DPM channel 3. The reset value is 0x00000000.	0x00000000.

5.5.2.25 DPM Channel Registers (IECDPM3HI, R, Address = 0xE080_0194)

IECDPM3HI	Bit	Description	Initial State
IECDPM3HI	[31:0]	High 32-bits of DPM channel 3. The reset value is 0x00000000.	0x00000000

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5.5.2.26 IEC Integration Test Control Register (IECITCR, R/W, Address = 0xE080_0F00)

IECITCR	Bit	Description	Initial State
-	[31:3]	Reserved. Unpredictable when read. Should be written as zero.	0
DPM Counter Test	[2]	Enable or disable test mode for all DPM counters. 0 = DPM counter test mode disabled, also the reset value. 1 = DPM counter test mode enabled. When this bit is set, the 64-bit DPM counters are split up into eight separate 8-bit counters, each accumulate by the CPU or programmed rate. This reduces the testing time required to ensure that all bits of the counters toggle correctly.	0
DVS Emulation Slot Counter Test	[1]	Enable or disable test mode for the bus V slotcounter. 0 = DVS emulation slot counter test mode disabled, also reset value. 1 = DVS emulation slot counter test mode enabled. When this bit is set, the 10-bit DVS emulation slot timing counter is split up into two 5-bit counters, each decrement separately. This reduces the testing time required to ensure that all bits of the counters toggle correctly.	0
ITEN	[0]	Integration test enable. When this bit is set to 1, the IEC is put into integration test mode. When 0, the IEC is in normal operating mode. The reset value is 0.	0

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5.5.2.27 IEC Integration Test Input Read or Set Registers (IECITIP1, R/W, Address = 0xE080_0F10)

IECITIP1	Bit	Description	Initial State
-	[31:5]	Reserved. Unpredictable when read. Should be written as zero.	0
IECSYNCMODEACK	[4]	Intra-chip input. Writes to this bit, set the value to be driven onto the input IECSYNCMODEACK, in the integration test mode. Reads return the value of the IECSYNCMODEACK input at the output of the test multiplexer. The reset value is 0.	0
IECDPMCLKEN	[3]	Intra-chip input. Writes to this bit, set the value to be driven onto the input IECDPMCLKEN, in the integration test mode. Reads return the value of the IECDPMCLKEN input at the output of the test multiplexer. The reset value is 0.	0
IECDVSEMCLKEN	[2]	Intra-chip input. Writes to this bit set the value to be driven onto the input IECDVSEMCLKEN, in the integration test mode. Reads return the value of the IECDVSEMCLKEN input at the output of the test multiplexer. The reset value is 0.	0
IECCPUWFIACK	[1]	Intra-chip input. Writes to this bit set the value to be driven onto the input IECCPUWFIACK, in the integration test mode. Reads return the value of the IECCPUWFIACK input at the output of the test multiplexer. The reset value is 0.	0
IECMAXPERF	[0]	Intra-chip input. Writes to this bit set the value to be driven onto the input IECMAXPERF, in the integration test mode. Reads return the value of the IECMAXPERF input at the output of the test multiplexer. The reset value is 0.	0

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5.5.2.28 IEC Integration Test Input Read or Set Registers (IECITIP1, R/W, Address = 0xE080_0F14)

IECITIP2	Bit	Description	Initial State
-	[31:8]	Reserved, read undefined, do not modify.	0
IECCRNTDCGIDX	[7:0]	Intra-chip input. Writes to these bits set the value to be driven onto the inputs IECCRNTDCGIDX[7:0], in the integration test mode. Reads return the value of the IECCRNTDCGIDX[7:0] inputs at the output of the test multiplexer. The reset value is 0x00.	0x00

5.5.2.29 IEC Integration Test Input Read or Set Registers (IECITIP1, R/W, Address = 0xE080_0F18)

IECITIP3	Bit	Description	Initial State
-	[31:8]	Reserved, read undefined, do not modify.	0
IECCRNTDVGIDX	[7:0]	Intra-chip input. Writes to these bits set the value to be driven onto the inputs IECCRNTDVCIDX[7:0], in the integration test mode. Reads return the value of theIECCRNTDVCIDX[7:0] inputs at the output of the test multiplexer. The reset value is 0x00.	0x00

5.5.2.30 Integration Test Output Read or Set Registers (IECITOP1, R/W, Address = 0xE080_0F20)

IECITOP1	Bit	Description	Initial State
-	[31:4]	Reserved, read undefined, do not modify.	0
IECSYNCMODEREQ	[3]	Intra-chip output. Writes to this bit set the value to be driven onto the IECSYNCMODEREQ output in integration test mode. Reads return the value of IECSYNCMODEREQ at the output of the test multiplexer. The reset value is 0.	0
IECPWRREQ	[2]	Intra-chip output. Writes to this bit set the value to be driven onto the IECPWRREQ output in integration test mode. Reads return the value of IECPWRREQ at the output of the test multiplexer. The reset value is 0.	0
IECCPUSLPINT	[1]	Intra-chip output. Writes to this bit set the value to be driven onto the IECCPUSLPINT output in integration test mode. Reads return the value of IECCPUSLPINT at the output of the test multiplexer. The reset value is 0.	0
IECCPUWUINT	[0]	Intra-chip output. Writes to this bit set the value to be driven onto the IECCPUWUINT output in integration test mode. Reads return the value of IECCPUWUINT at the output of the test multiplexer. The reset value is 0.	0

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5.5.2.31 Integration Test Output Read or Set Registers (IECITOP2, R/W, Address = 0xE080_0F24)

IECITOP2	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read undefined, do not modify.	0
IECTGTDCGIDX	[7:0]	Intra-chip outputs. Writes to these bits set the value to be driven onto the IECTGTDCGIDX [7:0] outputs in integration test mode. Reads return the value of IECTGTDCGIDX[7:0] at the output of the test multiplexer. The reset value is 0x00.	0x00

5.5.2.32 Integration Test Output Read or Set Registers (IECITOP3, R/W, Address = 0xE080_0F28)

IECITOP3	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read undefined, do not modify.	0
IECTGTDVCIDX	[7:0]	Intra-chip outputs. Writes to these bits set the value to be driven onto the IECTGTDVCIDX[7:0] outputs in integration test mode. Reads return the value of IECTGTDVCIDX[7:0] at the output of the test multiplexer. The reset value is 0x00.	0x00

5.5.2.33 Peripheral Identification Register 0 (IECPeriphID0, R, Address = 0xE080_0FE0)

IECPeriphID0	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read undefined, do not modify.	X
Partnumber0	[7:0]	These bits read back as 0x50	0x50

5.5.2.34 Peripheral Identification Register 1 (IECPeriphID1, R, Address = 0xE080_0FE4)

IECPeriphID1	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read undefined, do not modify.	X
Partnumber1	[7:0]	These bits read back as 0x07	0x07

5.5.2.35 Peripheral Identification Register 2 (IECPeriphID2, R, Address = 0xE080_0FE8)

IECPeriphID2	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read undefined, do not modify.	X
Revision	[7:4]	These bits read back as 0x0	0x0
Designer1	[3:0]	These bits read back as 0x04	0x04

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5.5.2.36 Peripheral Identification Register 3 (IECPeriphID3, R, Address = 0xE080_0FEC)

IECPeriphID3	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read undefined, do not modify.	X
Configuration 1	[7:0]	Number of DPC levels. These bits read back as 0x08.	0x08

5.5.2.37 Peripheral Identification Register 4 (IECPeriphID4, R, Address = 0xE080_0FD0)

IECPeriphID4	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read undefined, do not modify.	X
Reserved	[7:3]	Reserved	X
Configuration 2	[2:0]	Number of DPM channels. These bits are read back as 0x3.	0x3

5.5.2.38 Peripheral Identification Register 5 (IECPeriphID5, R, Address = 0xE080_0FD4)

IECPeriphID5	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read undefined, do not modify.	X
Configuration 3	[7:0]	Number of DVS slots in a frame. These bits read back as 0x08.	0x08

5.5.2.39 Peripheral Identification Register 6 (IECPeriphID6, R, Address = 0xE080_0FD8)

IECPeriphID6	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read undefined, do not modify.	X
Configuration 4	[7:0]	These bits are all reserved	Reserved

5.5.2.40 Peripheral Identification Register 7 (IECPeriphID7, R, Address = 0xE080_0FDC)

IECPeriphID7	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read undefined, do not modify.	X
Configuration 5	[7:0]	These bits are all reserved	Reserved

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5.5.2.41 IEC Identification Register 0 (IECID0, R, Address = 0xE080_0FF0)

IECID0	Bit	Description	Initial State
-	[31:8]	Reserved, read undefined, do not modify.	X
IECID0	[7:0]	These bits read back as 0x0D	0x0D

5.5.2.42 IEC Identification Register 1 (IECID1, R, Address = 0xE080_0FF4)

IECID1	Bit	Description	Initial State
-	[31:8]	Reserved, read undefined, do not modify.	X
IECID1	[7:0]	These bits read back as 0xF0	0xF0

5.5.2.43 IEC Identification Register 2 (IECID2, R, Address = 0xE080_0FF8)

IECID2	Bit	Description	Initial State
-	[31:8]	Reserved, read undefined, do not modify.	X
IECID2	[7:0]	These bits read back as 0x05	0x05

5.5.2.44 IEC Identification Register 3 (IECID3, R, Address = 0xE080_0FFC)

IECID3	Bit	Description	Initial State
-	[31:8]	Reserved, read undefined, do not modify.	X
IECID3	[7:0]	These bits read back as 0xB1	0xB1

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5.5.3 APC1 RELATED REGISTERS

5.5.3.1 PWI Command Register (APC_PWICMD, R/W, Address = 0xE070_0000)

APC_PWICMD	Bit	Description	Initial State
PWI Slave Register Address	[7:4]	PWI slave Register address of the read and write register.	0x0
PWI Slave Command	[3:0]	PWI slave command: 4'b0000 = Reset 4'b0001 = Authenticate 4'b0010 = Register read 4'b0011 = Register write 4'b0100 = Wakeup 4'b0101 = Sleep 4'b0110 = Shutdown 4'b1001 = Synchronize. Unused command patterns result in a No Operation (NOP) at the PWI interface.	0x0

5.5.3.2 PWI Write Data Register (APC_PWIDATAWR, R/W, Address = 0xE070_0004)

APC_PWIDATAWR	Bit	Description	Initial State
PWI Slave Write Data	[7:0]	Data is written to the PWI slave.	0x00

5.5.3.3 PWI Read Data Register (APC_PWIDATARD, R, Address = 0xE070_0008)

APC_PWIDATARD	Bit	Description	Initial State
PWI Slave Read Data	[7:0]	Data is read from the PWI slave.	0x00

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5.5.3.4 APC Control Register (APC_CONTROL, R/W, Address = 0xE070_0010)

APC_CONTROL	Bit	Description	Initial State
APC_HPM_AUTH_SET	[7]	HPM is set to the ring oscillator mode for a random PC used in the authentication sequence.	0
APC_PWRSV_EN	[6]	Enables the power save mode. On setting this bit: * the apc_refclk_req signal is deasserted when the apc_refclk_c clock signal is not required * the CMU can gate off the clock signal to save the power when the apc_refclk_req signal is deasserted.	0
APC_MULTICAL_EN	[5]	Enables the multiple RCC mode. Default, the APC1 is in the single RCC mode.	0
APC_HPM_EN	[4]	Enables the HPM. Default, the HPM is disabled and the PC is zero.	0
APC_PWRDN_EN	[3]	Enables the PWI sleep and wakeup command functions. Default, this feature is disabled.	0
APC_PLL_STATE_DETECT	[2]	Enable bit for disabling closed loop mode when pll is unstable.	0
APC_LOOP_MODE	[1]	Enable bit for the closed-loop or the open-loop mode: * defaults to the open-loop mode * setting this bit enables the closed-loop mode. The voltage scaling in the open-loop or the closed-loop mode is enabled only after setting the APC_VDD_UD bit of the APC_CONTROL Register.	0
APC_VDD_UD	[0]	Enables voltage scaling feature in the APC1: * defaults to the fixed voltage mode and the core voltage is set to the maximum value * for the closed-loop and the open-loop modes this bit must be enabled.	0

5.5.3.5 APC Status Register (APC_STATUS, R, Address = 0xE070_0014)

APC_STATUS	Bit	Description	Initial State
Reserved	[7:4]	Read undefined.	0
AUTH_DONE	[3]	Authentication procedure is completed.	0
PWI_BUSY	[2]	Bit is set on initiating a PWI command and is cleared when the command sequence is completed.	0
POWERWISE _VERIFIED	[1]	Bit is set on a successful PowerWise capable power supply authentication.	0
VDDOK	[0]	Vdd level is suitable for the current target frequency. This bit is set in the closed-loop mode.	0

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5.5.3.6 Minimum Limit Register (APC_MINVDD_LIMIT, R/W, Address = 0xE070_0018)

APC_MINVDD_LIMIT	Bit	Description	Initial State
Reserved	[7]	Read undefined. Write as zero.	0
Minimum core voltage	[6:0]	Minimum SoC operating core voltage.	0x00

5.5.3.7 VDD Check Register (APC_VDDCHK, R/W, Address = 0xE070_001C)

APC_VDDCHK	Bit	Description	Initial State
vddchkd[3:0]	[7:4]	The upper nibble of this register holds the four LSBs of the 12-bit vddchkd counter.	0x0
vddchk[3:0]	[3:0]	Evaluation time period during the integration of the slack in the closed	0x0

5.5.3.8 VDD Delay Time Register (APC_VDDCHKD, R/W, Address = 0xE070_0020)

APC_VDDCHKD	Bit	Description	Initial State
vddchkd[11:4]	[7:0]	Holds the upper eight bits of the 12-bit vddchkd counter.	0x00

5.5.3.9 VDD Pre-delay Select Register (APC_PREDYSEL, R/W, Address = 0xE070_0024)

APC_PREDYSEL	Bit	Description	Initial State
Reserved	[7:3]	Read undefined. Write as zero.	0
Pre-delay	[2:0]	Selects the predelay value for the HPM.	0x7

5.5.3.10 APC Interrupt Mask Register (APC_IMASK, R/W, Address = 0xE070_0028)

APC_IMASK	Bit	Description	Initial State
Reserved	[7]	Read undefined. Write as zero.	0
APB Write Discard	[6]	The APB write is discarded.	0
PWI Transaction Done	[5]	The PWI transaction is completed.	0
Error Detected in PWI	[4]	Error is detected in the PWI response frame.	0
No PWI Slave Response	[3]	No response frame detected on the PWI interface.	0
Output Voltage Clamped	[2]	The output voltage is clamped to the minimum voltage limit or to the zero voltage.	0
Low VDD Timeout	[1]	Vdd has not reached the optimum voltage in the closed-loop mode for the voltage upward slew within the hardware defined time period.	0
Undershoot Interrupt	[0]	Undershoot interrupt.	0

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5.5.3.11 APC Interrupt Status Register (APC_ISTATUS, R, Address = 0xE070_002C)

APC_ISTATUS	Bit	Description	Initial State
Reserved	[7]	Read undefined.	0
APB Write Discard	[6]	When the PWI command is active in the APC1, the new PWI commands issued by the host are discarded. This discarded status is reflected in this bit.	0
PWI Transaction Done	[5]	Bit is set when the APC1 completes the host issued PWI command. Software has to check this bit as well as the APC_STATUS.PWI_BUSY bit to confirm the completion of the command.	0
Error Detected in PWI	[4]	Bit is set on an error response from the PWI slave for the host issued as well as the APC1 issued PWI commands.	0
No PWI Slave Response	[3]	Bit is set for no response from the PWI slave for the host issued as well as the APC1 issued commands.	0
Output Voltage Clamped	[2]	This bit is set when the output voltage is clamped to the minimum limit or to the zero voltage.	0
Low VDD Timeout	[1]	During upward voltage slew, this bit is set in the closed-loop mode indicating that the dynamic compensator is not able to increase the voltage to the required level for the new higher performance level within the maximum time period set by the hardware.	0
Undershoot Interrupt	[0]	In the closed-loop AVS operation for a performance level change after reaching the optimum voltage the APC1 asserts an interrupt if the voltage correction continues and results in a slack error (+ve) which is more than the undershoot_limit value programmed in the APC_UNSHT_NOISE Register for nine consecutive samples.	0

5.5.3.12 APC Interrupt Clear Register (APC_ICLEAR, W, Address = 0xE070_0030)

APC_ICLEAR	Bit	Description	Initial State
Reserved	[7]	Undefined. Write as zero.	0
APB Write Discard	[6]	The APB write is discarded.	0
PWI Transaction Done	[5]	The PWI transaction is completed.	0
Error Detected in PWI	[4]	Error is detected in PWI response frame.	0
No PWI Slave Response	[3]	No response frame is detected on PWI interface.	0
Output Voltage Clamped	[2]	The output voltage is clamped to minimum limit or zero voltage.	0
Low VDD Timeout	[1]	In the closed-loop mode, Vdd has not reached the target voltage in the programmed time period for the upward voltage slew.	0
Undershoot Interrupt	[0]	Undershoot interrupt.	0

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5.5.3.13 APC Undershoot Threshold and Noise Limit Register (APC_UNSHT_NOISE, R/W, Address = 0xE070_0034)

APC_UNSHT_NOISE	Bit	Description	Initial State
Reserved	[7:6]	Read undefined. Write as zero.	0
Noise Limit for VDDOK	[5:4]	Noise limit for the VDDOK generation due to the power supply regulation errors. Provides the acceptable integrated eHPM (+ve) below the RCC value for updating the performance level in the closed-loop mode. **APC_UNSHT_NOISE[5:4] — Minimum Accumulated eHPM** 00 — 0 01 — 4 10 — 16 11 — 31	0x0
Undershoot Threshold Level	[3:0]	This is the threshold level for the detection of voltage undershoot interrupt on the voltage slew. The value programmed is the amount of eHPM (+ve) allowed after reaching the optimum core voltage for the safe SoC operation.	0x0

5.5.3.14 Wakeup Delay Register (APC_WKUP_DLY, R/W, Address = 0xE070_0038)

APC_WKUP_DLY	Bit	Description	Initial State
Wakeup Delay	[7:0]	Count for the wakeup delay.	0x00

5.5.3.15 Slack Sample Count Register (APC_SLK_SMP, R/W, Address = 0xE070_003C)

APC_SLK_SMP	Bit	Description	Initial State
Reserved	[7:6]	Read undefined. Write as zero.	0
Slack Sample Count	[5:0]	The time period for each count in the vddchkd and the vddchk counters during the performance level change: * set to 0x1D for 2µs when theapc_refclk_c clock is 15MHZ * set to 0x3B for 2µs when the apc_refclk_c clock is 30MHZ.	0x00

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5.5.3.16 PWI Clock Division Register (APC_CLKDIV_PWICLK, R/W, Address = 0xE070_0040)

APC_CLKDIV_PWICLK	Bit	Description	Initial State
Reserved	[7:4]	Read undefined. Write as zero.	0
Programmable Clock Division	[3:0]	Programmable division to theapc_refclk_c clock frequency for the PWI clock. The clock division is equal to 2 * (APC_CLKDIV_PWICLK + 1).	0x0

5.5.3.17 APC Overshoot Limit Register (APC_OVSHT_LMT, R/W, Address = 0xE070_0050)

APC_OVSHT_LMT	Bit	Description	Initial State
overshoot limit	[7:0]	Overshoot limit during the voltage slew in the closed-loop mode.	0x00

5.5.3.18 APC Closed-loop Control Register (APC_CLP_CTRL, R/W, Address = 0xE070_0054)

APC_CLP_CTRL	Bit	Description	Initial State
Reserved	[7:4]	Undefined. Write as zero.	0
APC_SS_GAIN_EN	[3]	Enables steady state gain term.	0
APC_UP_GAIN_EN	[2]	Enables the APC_GAIN2 term for the dynamic compensator. This gain term is selected during voltage upward slew.	0
APC_LOW_GAIN_EN	[1]	Enables the APC_GAIN4 term for the dynamic compensator. This gain term is selected when the slack or eHPM value is between +3 to -3.	0
APC_SAT_GAIN_EN	[0]	Enables the APC_GAIN3 term for the dynamic compensator. This gain term is selected when the PC value is saturated and the voltage is stepping up. This gain term has higher priority over the gain term 2.	0

5.5.3.19 APC Steady State Slew Rate Register (APC_SS_SRATE, R/W, Address = 0xE070_0058)

APC_SS_SRATE	Bit	Description	Initial State
Reserved	[7:4]	Read undefined.	0
APC_SS_SMP_RATE	[3:2]	00 Sample the eHPM every 32 apc_refclk_c cycles. 01 Sample the eHPM every 16 apc_refclk_c cycles. 10 Sample the eHPM every 8 apc_refclk_c cycles. 11 Sample the eHPM every apc_refclk_c cycle.	0x0
APC_GAIN_SEL	[1:0]	00 Gain term value of 0 in steady state mode. 01 Gain term value of 1 in steady state mode. 10 Gain term value of 2 in steady state mode. 11 Gain term value of 3 in steady state mode.	0x0

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5.5.3.20 Integrator's Gain Registers (APC_IGAIN1, R/W, Address = 0xE070_0060)

APC_IGAIN1	Bit	Description	Initial State
Reserved	[7:4]	Read undefined. Write as zero.	0
Gain 1	[3:0]	Default gain term for the dynamic compensator. The programmable values for this gain term are one to ten. Rest of the values are treated as zero in the closed-loop AVS operations.	0x0

5.5.3.21 Integrator's Gain Registers (APC_IGAIN2, R/W, Address = 0xE070_0064)

APC_IGAIN2	Bit	Description	Initial State
Reserved	[7:4]	Read undefined. Write as zero.	0
Gain 2	[3:0]	Gain term for the upward voltage slew when enabled in the APC_CLP_CTRL Register. The programmable values for this gain term are one to ten. Rest of the values are treated as zero in the closed-loop AVS operations.	0x0

5.5.3.22 Integrator's Gain Registers (APC_IGAIN3, R/W, Address = 0xE070_0068)

APC_IGAIN3	Bit	Description	Initial State
Reserved	[7:4]	Read undefined. Write as zero.	0
Gain 3	[3:0]	Dynamic compensator uses this gain term for the saturated HPM output when enabled. The programmable values for this gain term are one to ten. Rest of the values are treated as zero in the closed-loop AVS operations.	0x0

5.5.3.23 Integrator's Gain Registers (APC_IGAIN4, R/W, Address = 0xE070_006C)

APC_IGAIN4	Bit	Description	Initial State
Reserved	[7:4]	Read undefined. Write as zero.	0
Gain 4	[3:0]	Selected by the dynamic compensator when enabled in the APC_CL_CTRL Register for the low slack values. The programmable values for this gain term are one to ten. Rest of the values are treated as zero in the closed-loop AVS operations.	0x0

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5.5.3.24 Integration Test Control Register (APC_ITSTCTRL, R/W, Address = 0xE070_006C)

APC_ITSTCTRL	Bit	Description	Initial State
Reserved	[7:2]	Undefined. Write as zero.	0
IT_OPEN	[1]	Integration test output enable. The reset value is zero. 1 = APC1 is in integration test mode. 0 = APC1 is in normal mode. This control bit also drives the apc_hpm_it_en output signal. When this signal is asserted, the HPM is set to the integration test mode. In this mode the primary inputs are directly connected to the primary outputs.	0
IT_IPEN	[0]	Integration test input enable. The reset value is zero. 1 = APC1 is in integration test mode. 0 = APC1 is in normal mode.	0

5.5.3.25 Integration Test Input Read or Set Registers (APC_ITSTIP1, R/W, Address = 0xE070_0070)

APC_ITSTIP1	Bit	Description	Initial State
Reserved	[7]	Undefined. Write as zero.	0
HPM_DELAY _CODE[4:0]	[6:2]	In integration test mode: • write drives the hpm_delay_code inputs to the design • read returns the register content. In normal mode: • write updates the register • read returns the data from the hpm_delay_code primary inputs.	0x00
APC_SYNC _FROM_HPM	[1]	In integration test mode: • write drives the apc_sync_from_hpm input to the design • read returns the register content. In normal mode: • write updates the register • read returns the data from the apc_sync_from_hpm primary input.	0
APC_CLAMP _ACK	[0]	In integration test mode: • write drives the apc_clamp_ack input to the design • read returns the register content. In normal mode: • write updates the register • read returns the data from the apc_clamp_ack primary input.	0

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5.5.3.26 Integration Test Input Read or Set Registers (APC_ITSTIP2, R/W, Address = 0xE070_0074)

APC_ITSTIP2	Bit	Description	Initial State
Reserved	[7:N]	Read undefined. Write as zero.	0
APC_TARGET_INDEX	[N-1:0]	In integration test mode: • write drives the apc_target_index inputs to the design • read returns the register content. In normal mode: • write updates the register • read returns the data from the apc_target_index primary inputs.	0x00

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5.5.3.27 Integration Test Output Read or Set Registers (APC_ITSTOP1, R/W, Address = 0xE070_0078)

APC_ITSTOP1	Bit	Description	Initial State
APC_PREDELAY _SEL[2:0]	[7:5]	In integration test mode: • write drives the apc_predelay_selprimary outputs • read returns the register content. In normal mode: • write updates the register • read returns the data from the apc_predelay_sel signals of the design.	0x0
APC_HPM_EN	[4]	In integration test mode: • write drives the apc_hpm_enprimary output • read returns the register content. In normal mode: • write updates the register • read returns the data from theapc_hpm_en signal of the design.	0
APC_CLAMP_REQ	[3]	In integration test mode: • write drives the apc_clamp_reqprimary output • read returns the register content. In normal mode: • write updates the register • read returns the data from the apc_clamp_req signal of the design.	0
APC_INTERRUPT	[2]	In integration test mode: • write drives the apc_interruptprimary output • read returns the register content. In normal mode: • write updates the register • read returns the data from the apc_interrupt signal of the design.	0
APC_SYNC_TO_HPM	[1]	In integration test mode: • write drives the apc_sync_to_hpmprimary output • read returns the register content. In normal mode: • write updates the register • read returns the data from the apc_sync_to_hpm signal of the design.	0
APC_REFCLK_REQ	[0]	In integration test mode: • write drives the apc_refclk_reqprimary output • read returns the register content. In normal mode: • write updates the register • read returns the data from theapc_refclk_req signal of the design.	0

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5.5.3.28 Integration Test Output Read or Set Registers (APC_ITSTOP2, R/W, Address = 0xE070_007C)

APC_ITSTOP2	Bit	Description	Initial State
Reserved	[7:N]	Read undefined. Write as zero.	0
APC_CURRENT_INDEX	[N-1:0]	In integration test mode: • write drives the apc_current_index primary outputs • read returns the register content. In normal mode: • write updates the register • read returns the data from the apc_current_index signals of the design.	0x00

5.5.3.29 Integration Test Output Read or Set Registers (APC_ITSTOP3, R/W, Address = 0xE070_00C4)

APC_ITSTOP3	Bit	Description	Initial State
Reserved	[7:1]	Read undefined. Write as zero.	0
APC_HPM_AUTH_SET	[0]	In integration test mode: • write drives the apc_hpm_auth_set primary output • read returns the register content. In normal mode: • write updates the register • read returns the data from the apc_hpm_auth_set signal of the design.	0

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5.5.3.30 Voltage Information Registers

APC1 has two types of voltage information registers. Ones are for closed-loop control, and the others are for open-loop control. Registers for closed-loop control give delay information, while registers for open-loop control give direct voltage information. There is a register containing the retention voltage level for the performance level zero.

- Calibration Code Registers (APC_PL1_CALCODE, R/W, Address = 0xE070_0080)
- Calibration Code Registers (APC_PL2_CALCODE, R/W, Address = 0xE070_0084)
- Calibration Code Registers (APC_PL3_CALCODE, R/W, Address = 0xE070_0088)
- Calibration Code Registers (APC_PL4_CALCODE, R/W, Address = 0xE070_008C)
- Calibration Code Registers (APC_PL5_CALCODE, R/W, Address = 0xE070_0090)
- Calibration Code Registers (APC_PL6_CALCODE, R/W, Address = 0xE070_0094)
- Calibration Code Registers (APC_PL7_CALCODE, R/W, Address = 0xE070_0098)
- Calibration Code Registers (APC_PL8_CALCODE, R/W, Address = 0xE070_009C)

The Calibration Code Registers are eight, 5-bit registers. Their names are **APC_PL1_CALCODE ~ APC_PL8_CALCODE**. They give delay information target for closed-loop operation.

APC_PL*_CALCODE	Bit	Description	Initial State
Reserved	[7:5]	Read undefined. Write as zero.	X
Reference Calibrated Code 1	[4:0]	The RCC for performance level *	0x1F

- Open-loop VDD Core Registers (APC_PL1_COREVDD, R/W, Address = 0xE070_00A0)
- Open-loop VDD Core Registers (APC_PL2_COREVDD, R/W, Address = 0xE070_00A4)
- Open-loop VDD Core Registers (APC_PL3_COREVDD, R/W, Address = 0xE070_00A8)
- Open-loop VDD Core Registers (APC_PL4_COREVDD, R/W, Address = 0xE070_00AC)
- Open-loop VDD Core Registers (APC_PL5_COREVDD, R/W, Address = 0xE070_00B0)
- Open-loop VDD Core Registers (APC_PL6_COREVDD, R/W, Address = 0xE070_00B4)
- Open-loop VDD Core Registers (APC_PL7_COREVDD, R/W, Address = 0xE070_00B8)
- Open-loop VDD Core Registers (APC_PL8_COREVDD, R/W, Address = 0xE070_00BC)

The Open-loop VDD Core Registers are eight, 7-bit registers. Their names are **APC_PL1_COREVDD ~ APC_PL8_COREVDD**. They give direct voltage information for open-loop operation.

APC_PL*_COREVDD	Bit	Description	Initial State
Reserved	[7]	Read undefined. Write as zero.	X
OL_VDD1	[6:0]	The voltage value for the performance level * in the open-loop mode.	0x7F

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5.5.3.31 Retention VDD Registers (APC_RET_VDD, R/W, Address = 0xE070_00C0)

APC_RET_VDD	Bit	Description	Initial State
Reserved	[7]	Read undefined. Write as zero.	0
Retention VDD	[6:0]	The retention voltage level for performance level zero.	0x00

5.5.3.32 Debug Performance Registers (APC_DBG_DLYCODE, R, Address = 0xE070_00E0)

APC_DBG_DLYCODE	Bit	Description	Initial State
Reserved	[7:5]	Read undefined.	0
Performance Code	[4:0]	The PC of the HPM.	0x00

5.5.3.33 Revision Number Registers (APC_REV, R, Address = 0xE070_00FC)

APC_REV	Bit	Description	Initial State
Revision Number	[7:0]	Holds the APC1 revision number.	0x01

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6 BOOTING SEQUENCE

6.1 OVERVIEW OF BOOTING SEQUENCE

S5PV210 consists of 64KB ROM and 96KB SRAM as internal memory. For booting, internal 64KB ROM and internal 96KB SRAM regions can be used. S5PV210 boots from internal ROM to enable secure booting, which ensures that the image cannot be altered by unauthorized users. To select secure booting or normal booting, S5PV210 should use e-fuse information. This information cannot be altered after being programmed.

The booting device can be chosen from following list:

- General NAND Flash memory
- OneNAND memory
- SD/ MMC memory (such as MoviNAND and iNAND)
- eMMC memory
- eSSD memory
- UART and USB devices

At system reset, the program counter starts from the iROM codes in internal ROM region. However, the system reset may be asserted not only on booting time, but also on wakeup from low power modes. Therefore, the iROM code must execute appropriate process according to the reset status (refer to *Table 6-1*).

The boot loader is largely composed of iROM, first and second boot loaders. The characteristics of these boot loaders are:

- iROM code: Contains small and simple code, which is platform-independent and stored in internal memory
- First boot loader: Contains small and simple code, which is platform-independent and stored in external memory device. Related to secure booting.
- Second boot loader: Contains complex code, which is platform-specific and stored in external memory device.

If you select secure booting, iROM code and first boot loader provide integrity checking function (that is it uses public key algorithm) to verify loaded image. There are 160 e-fuse bits of secure boot key, and they are used to authenticate loaded public key before the iROM's integrity check. For more information on secure booting, refer to Chapter.

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Figure 6-1 shows the block diagram of booting time operation.

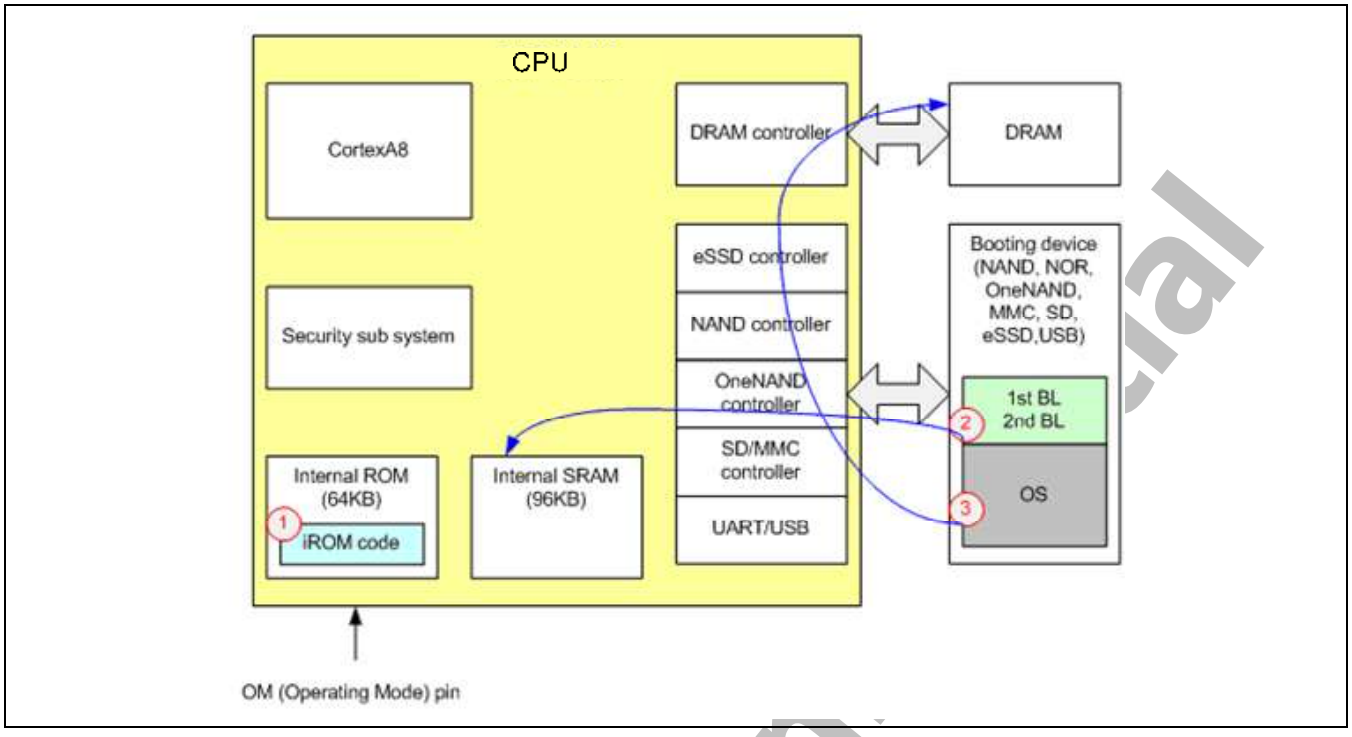

Figure 6-1 Block Diagram of Booting Time Operation

- The iROM code is placed in internal 64KB ROM. It initializes basic system functions such as clock, stack, and heap.
- The iROM loads the first boot loader image from a specific booting device to internal 96KB SRAM. The booting device is selected by Operating Mode (OM) pins. According to the secure boot key values, the iROM code may do an integrity check on the first boot loader image.
- The first boot loader loads the second boot loader then may check the integrity of the second boot loader according the secure boot key values.
- The second boot loader initializes system clock, UART, and DRAM controller. After initializing DRAM controller, it loads OS image from the booting device to DRAM. According to the secure boot key values, the second boot loader can do an integrity check on the OS image.
- After the booting completes, the second boot loader jumps to the operating system.

The iROM code reads the OM pins to find the booting device. The OM register provides the OM pin and other information required for booting. For more information on OM register, refer to Chapter 02.01, "Chip ID".

The OM pin decides the booting devices such as OneNAND, NAND, MoviNAND, eSSD and iNAND. It also decides the device options such as bit width, wait cycles, page sizes, and ECC modes.

NOTE: USB booting is provided for system debugging and flash reprogramming, not for normal booting. Hence, it is selected by toggling OM[5:4] pin to “2’b10” without considering other OM pin values.

The iROM code in internal 64KB ROM is named BL0. And the first boot loader is named BL1

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6.2 SCENARIO DESCRIPTION

6.2.1 RESET STATUS

There are several scenarios for system reset such as hardware reset, watchdog reset, software reset, and wake up from power down modes. For each scenario, the mandatory functions are summarized in *Table 6-1*

Table 6-1 Functions Needed for Various Reset Status

	Basic Initialization in iROM	PLL Setting in iROM	First Boot / Second Boot Loader Loading	DRAM Setting in Second Boot Loader	OS Loading	Restore Previous State
Hardware Reset	O	O	O	O	O	X
Watchdog Reset	O	O	O	O	O	X
Wake up from SLEEP	O	O	O	O	X	O
SW reset	O	O	O	O	O	X
Wake up from DEEP_STOP	O	X	X (note)	X	X	O
Wake up from DEEP_IDLE	O	X	X (note)	X	X	O

NOTE: When the contents of SRAM are preserved by retention option.

At the time of hardware reset and watchdog reset, the system should boot fully with the first boot loader and the second boot loader and loading of OS image. The new reset status is classified as reset group0.

Since the contents of DRAM memory are preserved in the SLEEP mode, it does not require loading the OS image to DRAM. However, SoC internal power is not supplied to internal logic during SLEEP mode and all contents in internal SRAM are not preserved. Therefore, the first boot loader and the second boot loader should be loaded again. This reset status is classified as reset group1.

At the time of software reset, The loading of boot loader is executed. Although top block's power is gated in DEEP_STOP and DEEP_IDLE modes, the internal SRAM can be reserved, so that the re-loading of boot loader is not required. In case of non-retention of SRAM in DEEP_STOP and DEEP_IDLE modes, the first boot loader should be loaded again. These software reset that wake up from DEEP_STOP and DEEP_IDLE statuses are classified as reset group2.

If system enters into all power down modes, the current system status should be saved to safe memory region such as DRAM, so that the system continues processing seamlessly after waking up from power down modes.

Finally, the restoring previous state function is required on wake up from SLEEP, DEEP_STOP, and DEEP_IDLE modes.

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6.2.2 BOOTING SEQUENCE EXAMPLE

Figure 6-2 shows the flow chart related to total booting code sequence.

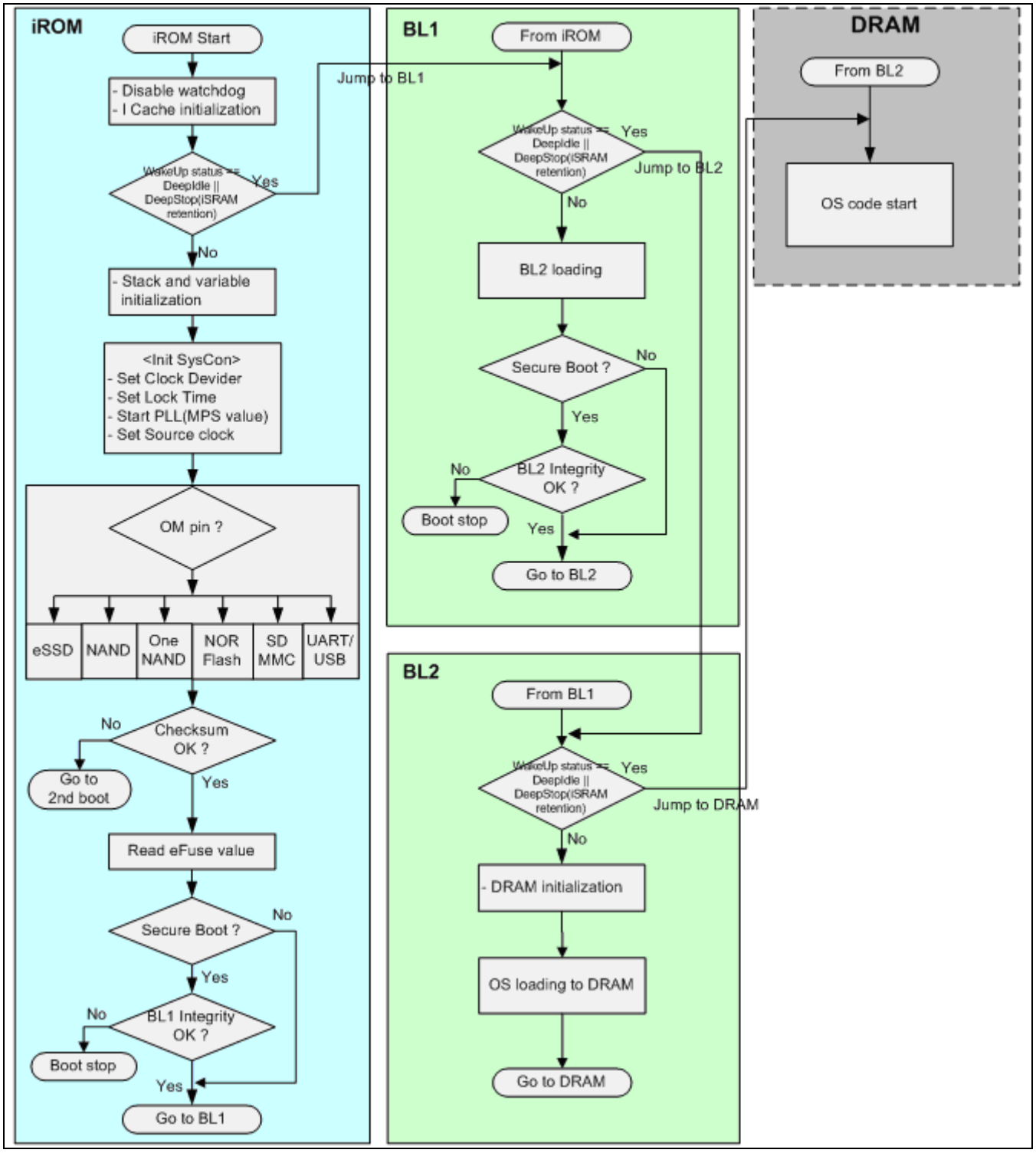

Figure 6-2 Total Booting Code Sequence Flow Chart

Program code starts from internal ROM(iROM) and moves to internal SRAM(iRAM). Finally, program executes on DRAM.

The booting sequence in internal ROM is as follows:

1. Disable the watchdog timer.
2. Initialize the instruction cache controller.
3. Initialize the stack and heap region.
4. Check secure key.
5. Set Clock divider, lock time, PLL (MPS value), and source clock.
6. Check OM pin and load the first boot loader (The size of boot loader depends on S/W) from specific device (block number 0) to iRAM.
7. If secure booting is successful, execute integrity check
8. If integrity check passes, then jump to the first boot loader in iRAM (0xD002_0010)

The booting sequence in internal SRAM is as follows:

1. Load the second boot loader from boot device to iRAM.
2. If secure booting is successful, execute integrity check.
3. If integrity check passes, then jump to the second boot loader in iRAM (The jumping address depends on user's software)
4. If integrity check fails, then stop the first boot loader.
5. The second boot loader Initializes the DRAM controller.
6. Load the OS image from specific device (block number 1) to DRAM.
7. Jump to OS code in DRAM (0x2000_0000 or 0x4000_0000)

The booting sequence in DRAM is as follows:

1. If S5PV210 is powered on from SLEEP, DEEP_STOP, or DEEP_IDLE modes, then restore the previous state.
2. Jump to OS code.

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6.2.3 FIXED PLL AND CLOCK SETTING

To speed up first boot loader's operation, the first boot loader initializes the PLL with fixed value. Fixed PLL setting is as follows:

- APLL: M=200, P=6, S=1 FOUT = (MDIV X FIN)/ (PDIV X $2^{(SDIV-1)}$)) = 800MHz
- MPLL: M=667, P=12, S=1 FOUT = (MDIV X FIN) / (PDIV X 2^{SDIV}) = 667MHz
- EPLL: M=80, P=3, S=3, K=0 FOUT = ((MDIV+KDIV) X FIN) / (PDIV X 2^{SDIV}) = 80MHz

Table 6-2 shows the system clock frequencies for various external crystals after initialization of the PLL by first boot loader.

Table 6-2 First Boot Loader's Clock Speed at 24 MHz External Crystal

ARMCLK	ACLK200	HCLK200	PCLK100	HCLK100	HCLK166	PCLK83	SCLK_FIMC	HCLK133
400	133	133	66	66	133	66	133	133

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6.2.4 OM PIN CONFIGURATION

Table 6-3 shows the booting option that can be set by OM pins.

Table 6-3 OM Pin Setting for Various Booting Option

OM[5]	OM[4]	OM[3]	OM[2]	OM[1]	OM[0]	OM[5]	OM[4]	OM[3] OM[2] OM[1]	OM[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	Boot Mode	I-ROM	eSSD	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			NAND 2 KB, 5cycle (NAND 8-bit ECC)	X-TAL
					1'b1				X-TAL(USB)
			1'b1	1'b0	1'b0			NAND 4 KB, 5cycle (NAND 8-bit ECC)	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			NAND 4 KB, 5cycle (NAND 16-bit ECC)	X-TAL
					1'b1				X-TAL(USB)
		1'b1	1'b0	1'b0	1'b0			OnenandMux(Audi)	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			OnenandDemux(Audi)	X-TAL
					1'b1				X-TAL(USB)
			1'b1	1'b0	1'b0			SD/MMC	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			eMMC(4-bit)	X-TAL
					1'b1				X-TAL(USB)
	1'b1	1'b0	1'b0	1'b1	1'b0			NAND 2 KB, 5cycle (16-bit bus, 4-bit ECC)	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			NAND 2 KB, 4cycle (NAND 8-bit ECC)	X-TAL
					1'b1				X-TAL(USB)
			1'b1	1'b0	1'b0			iROM NOR boot	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			eMMC(8-bit)	X-TAL
					1'b1				X-TAL(USB)
1'b1	1'b0	1'b0	1'b0	1'b0	1'b0		I-ROM First boot UART ->USB	eSSD	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			NAND 2 KB, 5cycle	X-TAL
					1'b1				X-TAL(USB)
			1'b1	1'b0	1'b0			NAND 4 KB, 5cycle	X-TAL
					1'b1				X-TAL(USB)
				1'b1	1'b0			NAND 16-bit ECC (NAND 4 KB, 5cycle)	X-TAL
					1'b1				X-TAL(USB)
		1'b1	1'b0	1'b0	1'b0			OnenandMux(Audi)	X-TAL

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OM[5]	OM[4]	OM[3]	OM[2]	OM[1]	OM[0]	OM[5]	OM[4]	OM[3]	OM[2]	OM[1]	OM[0]
					1'b1						X-TAL(USB)
				1'b1	1'b0			OnenandDemux(Audi)			X-TAL
					1'b1						X-TAL(USB)
			1'b1	1'b0	1'b0			SD/MMC			X-TAL
					1'b1						X-TAL(USB)
				1'b1	1'b0			eMMC(4-bit)			X-TAL
					1'b1						X-TAL(USB)

NOTE: The first boot loader tries to negotiate UART first. If it fails, then it tries to drive the USB device. Hence, you have to disconnect the UART device if you want to boot using USB device.

The hardware logic decides address mapping, and the software routine decides other booting options.
The value of OM pin can be read from OM register, which is described in Chapter 2.1.

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6.2.5 SECURE BOOTING

The basic criterion for security system is "The ‘root of trust’ has to be hardware. You cannot request a software system to ‘validate’ itself.”

In S5PV210, the root of trust is implemented by iROM code in internal ROM. Therefore it cannot be modified by unauthorized users. The hardware design proves the integrity of iROM code. On the other hand, the first boot loader, the second boot loader and OS images are stored in external memory devices. Therefore, the iROM code (that has already been proved as secure) should verify the integrity of first boot loader. If the integrity check passes on first boot loader, the first boot loader is included in trust region. Then, first boot loader verifies the integrity of the second boot loader, the second boot loader verifies the integrity of the OS image.

Figure 6-3 shows the secure booting diagram.

The secure booting sequence is as follows:

The iROM code

1. Checks the integrity of RSA public key using E-fuse RSA key hash value.
2. Loads the first boot loader to iRAM.
3. Checks the integrity of first boot loader using trusted RSA public key.

The first boot loader

1. Loads security software to iRAM.
2. Checks the integrity of software using trusted RSA public key.
3. Loads second boot loader to iRAM.
4. Checks the integrity of second boot loader using trusted RSA public key.

The second boot loader

1. Loads security software to iRAM.
2. Checks the integrity of software using trusted RSA public key.
3. Loads OS kernel and applications to DRAM.
4. Checks the integrity of OS kernel and application using trusted RSA public key

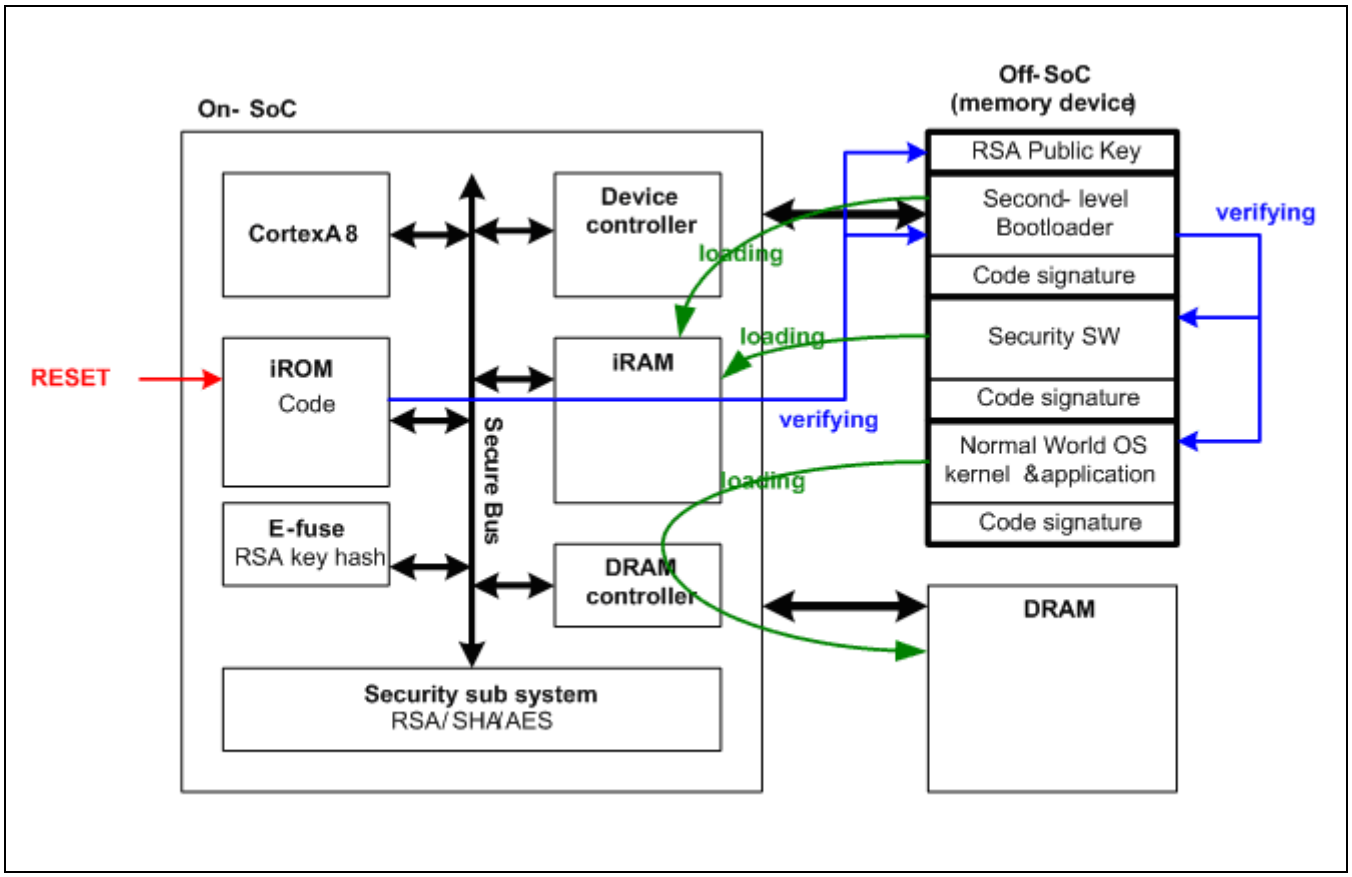

Figure 6-3 Secure Booting Diagram

Section 3

BUS

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1 BUS CONFIGURATION

1.1 OVERVIEW OF BUS CONFIGURATION

This chapter describes the bus configuration in S5PV210.

1.1.1 AXI INTERCONNECT

S5PV210 consists of 12 high-performance AXI interconnect. The role of AXI interconnect is to interconnect bus masters to bus slaves.

1.1.1.1 Key Features of AXI Interconnect

The key features of AXI interconnect include:

- **Quality of Service**
  The Quality of Service (QoS) scheme tracks the number of outstanding transactions. When a specified number is reached, it permits transactions from specified masters only. This scheme only provides support for slaves that have a combined acceptance capability such as the Dynamic Memory Controller (DMC).

The QoS scheme has no effect until the AXI interconnect matrix calculates the following:

At a particular Master Interface (MI), there are a number of outstanding transactions equal to the value stored in QoS tidemark.

It then accepts transactions only from slave ports specified in the QoS access control. This restriction remains until the number of outstanding transactions is again less than the value stored in QoS tidemark.

Figure 1-1 shows the implementation for an interconnect supporting two masters and one slave.

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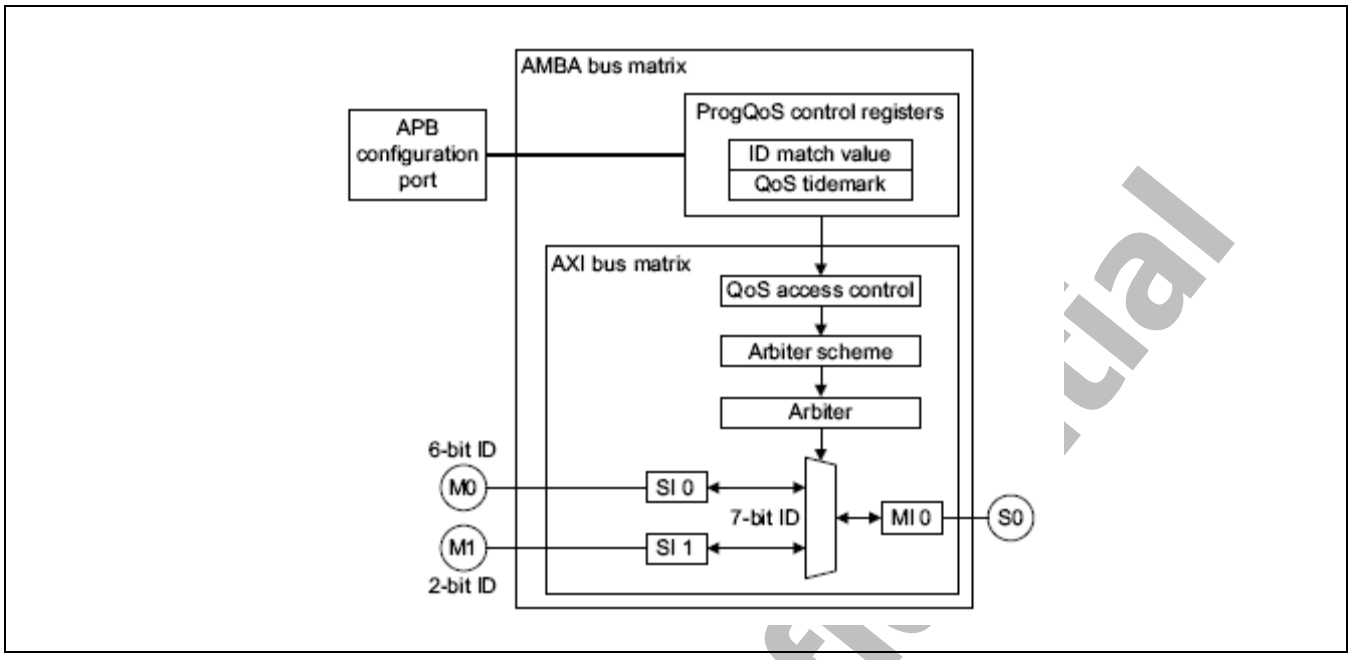

Figure 1-1 Example of ProgQoS Control for 2-1 Interconnect

- **Arbitration scheme**
  In the AXI interconnect, you can configure each MI separately to contain an arbitration scheme. This scheme is further classified as:
  - Non-programmable RR scheme
  - Programmable RR scheme
  - Programmable LRG scheme

The AW and AR channels have separate arbiters, and can be programmed (if applicable) and interrogated separately through APB programming interface. However, both AW and AR channels are configured identically. If these channels are arbitrated separately, MI can permit simultaneous read and write transactions from different SIs.

The arbitration policy is decided by the values of SFRs. An arbitration decision taken in the current cycle does not affect the current cycle.

If no SIs are active, the arbiter adopts default arbitration, that is, the highest priority SI. If default arbitration occurs and the highest priority SI becomes active in the same cycle as (or before) any other SI, then this does not constitute a grant to an active SI and the arbitration scheme does not change its state.

If a QoS provision is active, only a subset of SI is permitted to win arbitration. There is no guarantee that the default arbitration is among these. In these circumstances, no transaction is permitted to use the default arbitration, and arbitration must occur whenever there is an active SI.

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1.1.1.2 Round-robin (RR) Scheme

In the RR scheme, you can select the following design time:

- Number of used slots
- SI to which these slots are allocated
- Order of slots

There must be at least one slot per connected SI and up to 32 slots. By allocating multiple slots for a SI, you can allocate access to the slave on average, in proportion to the number of slots. If the slots are appropriately ordered, this can also reduce the maximum time before a grant is guaranteed. The SI associated with a slot can be interrogated by APB programming interface, but it cannot be changed.

Whenever arbitration is granted to an active SI, the slots are rotated so that the slot in the highest priority position becomes the lowest and all other slots move to a higher priority, but maintain their relative order, as shown in *Figure 1-2*. This means that if an SI is the highest priority active SI, but is not the highest priority interface, then it continues to win the arbitration until it becomes the highest priority interface, and then the lowest priority interface subsequently.

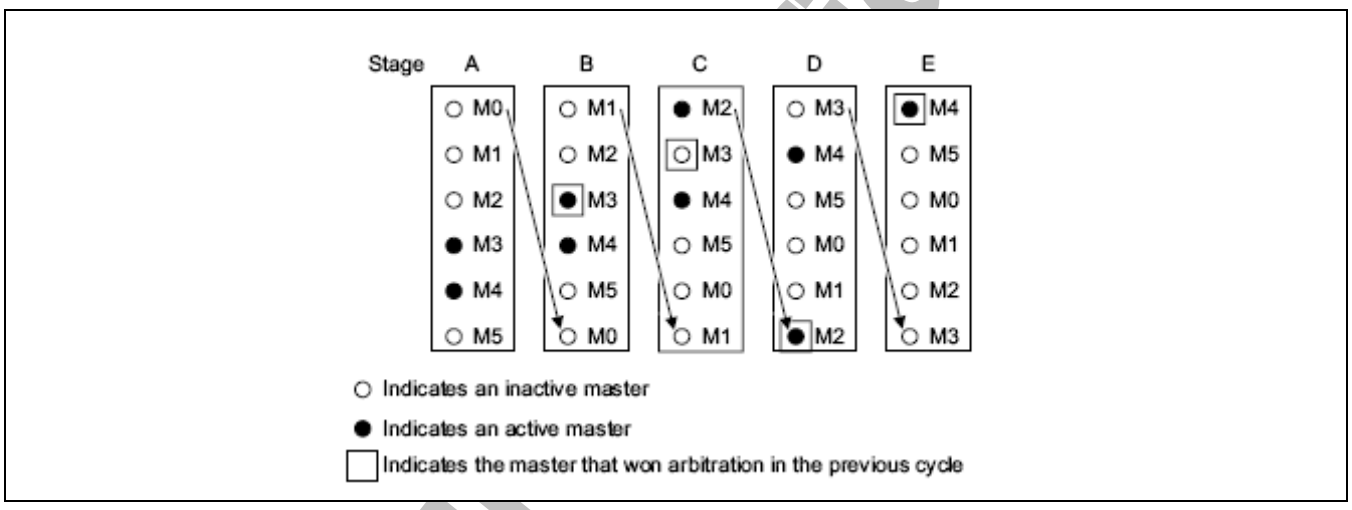

Figure 1-2 Example Operation of RR Arbitration Scheme

Since the arbitration value is registered, the arbitration decision made in this cycle is used in the next cycle. This means that if SI (that currently holds the arbitration) has the highest priority active SI in this cycle, it wins the arbitration again--regardless of whether or not it is active in the next cycle, as shown by the status of M3 in stages A, B, and C in *Figure 1-2*.

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1.1.1.3 Least Recently Granted Scheme

In the Least Recently Granted (LRG) scheme, each connected SI has a single slot associated with it, but each interface also has a priority value. This priority value, whose post-reset value can be configured at design time, programmed, or interrogated through the APB programming interface, can make the arbiter behave as:

- Pure LRG scheme
- Fixed priority encoder
- Combination of the two

All masters with the same priority form a priority group. As a result of arbitration, a master can move within its priority group but cannot leave its group, and no new masters can join the group.

Arbitration is granted to the highest priority group from which a member is trying to win access and within that group to the highest master at that time. When master wins arbitration, it is relegated to the bottom of its group to ensure that it does not prevent other masters in its group from accessing the slave.

If you configure all master priorities to different levels, the arbiter implements a fixed priority scheme. This occurs because in this case, each master is in a group of its own, and therefore, masters maintain their ordering.

If all master priorities are the same, then an LRG scheme is implemented. The reason all master priorities behave as LRG is because the process of relegating the master that was last granted access to the bottom of its group results in the masters being ordered from the LRG master at the top to the Most Recently Granted (MRG) at the bottom.

The LRG and fixed priority modes concurrently exist when the master priority values are set with a combination of identical and unique values. You can mix priority groups that contain one member with priority groups that contain more than one member in an arbitrary manner. The arbiter places no restriction on the number of groups or their membership.

Figure 1-3 shows the movement of masters within their priority groups.

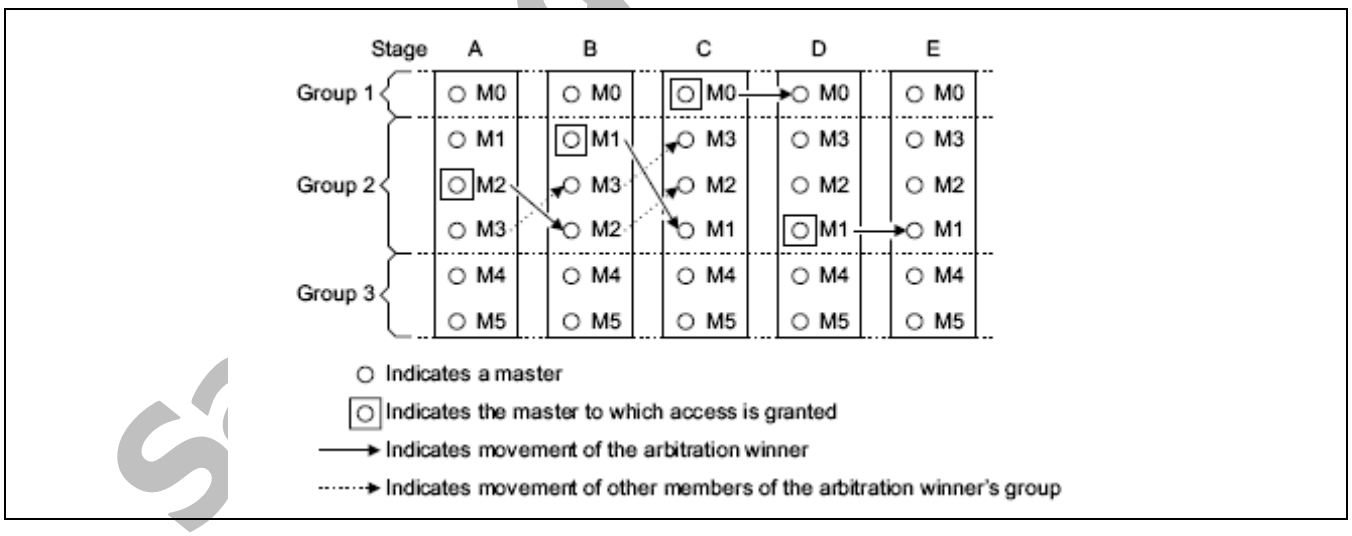

Figure 1-3 Example Operation of LRG Arbitration Scheme

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1.2 REGISTER DESCRIPTION

1.2.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
ASYNC_CONFIG0	0xE0F0_0000	R/W	Synchronizer configuration register	0x0000_0001
ASYNC_CONFIG1	0xE1F0_0000	R/W	Synchronizer configuration register	0x0000_0001
ASYNC_CONFIG2	0xF180_0000	R/W	Synchronizer configuration register	0x0000_0001
ASYNC_CONFIG3	0xF190_0000	R/W	Synchronizer configuration register	0x0000_0001
ASYNC_CONFIG4	0xF1A0_0000	R/W	Synchronizer configuration register	0x0000_0001
ASYNC_CONFIG5	0xF1B0_0000	R/W	Synchronizer configuration register	0x0000_0001
ASYNC_CONFIG6	0xF1C0_0000	R/W	Synchronizer configuration register	0x0000_0001
ASYNC_CONFIG7	0xF1D0_0000	R/W	Synchronizer configuration register	0x0000_0001
ASYNC_CONFIG8	0xF1E0_0000	R/W	Synchronizer configuration register	0x0000_0001
ASYNC_CONFIG9	0xF1F0_0000	R/W	Synchronizer configuration register	0x0000_0001
ASYNC_CONFIG10	0xFAF0_0000	R/W	Synchronizer configuration register	0x0000_0001

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1.2.2 SYNCHRONIZER CONFIGURATION REGISTER (ASYNC_CONFIG0~10, R/W)

ASYNC_CONFIG0~10	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0x0
HALF_SYNC_SEL	[0]	Use half synchronizer for asynchronous clock domain crossing.	0x1

HALF_SYNC_SEL field of ASYNC_CONFIG0~10 registers decides whether to use half or full synchronization for synchronizer, which separates two different clock domains. Setting this field to HIGH selects half synchronizer, which has better performance over full synchronizer. On the contrary, full synchronizer has a better MTBF (Mean Time Between Failure) resulting from crossing clock domains. It is recommended to use full synchronization for stable operation.

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2 CORESIGHT

2.1 CORESIGHT SYSTEM OVERVIEW

2.1.1 ABOUT CORESIGHT SYSTEMS GENERALS

CoreSight systems provide the entire infrastructure required to debug, monitor, and optimize the performance of a complete System on Chip (SoC) design.

There are historically three main ways of debugging an ARM processor based SoC:

- Conventional JTAG debug. This is invasive debug with the core halted using:
  - Breakpoints and watchpoints to halt the core on specific activity
  - A debug connection to examine and modify registers and memory and provide single-step execution.
- Conventional monitor debug. This is invasive debug with the core running using a debug monitor that resides in memory.
- Trace. This is non-invasive debug with the core running at full speed using:
  - Collection of information on instruction execution and data transfers
  - Delivery off-chip in real-time
  - Tools to merge data with source code on a development workstation for later analysis.

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2.1.2 KEY FEATURES OF CORESIGHT

2.1.2.1 Debug Access

You gain debug access in CoreSight systems through the Debug Access Port (DAP) that provides:

- Real-time access to physical memory without halting the core and without any target resident code
- Debug control and access to all status registers

The same mechanism provides fast access to download code at the start of the debug session. This is faster than the traditional JTAG mechanism that uses the ARM core to write data to memory. You can still use the ARM core to write data to virtual memory and to ease migration when the debugger does not support this approach.

Figure 2-1 shows an example system with debug components and a DAP in a SoC design.

The DAP provides the following advantages for multi-core SoC designs:

- There is no requirement to run at the lowest common speed. A slow or powered down component has no effect on access to other components. This means that power management has minimal impact on debug.
- The number of devices in the system does not affect the access speed. You have direct access to individual devices.
- You can add third party debug components with the Advanced Microcontroller Bus Architecture (AMBA) debug bus interface, AMBA 3 Advanced Peripheral Bus (APB), which provides internal and external access to the component.
- More than one core can control debug functionality, rather than restricting this to the core being debugged. One core can debug another. In particular this enables a multi-core SoC when used as a single core platform to have complex on-chip debug and analysis features. You could use this, for example, during application development.

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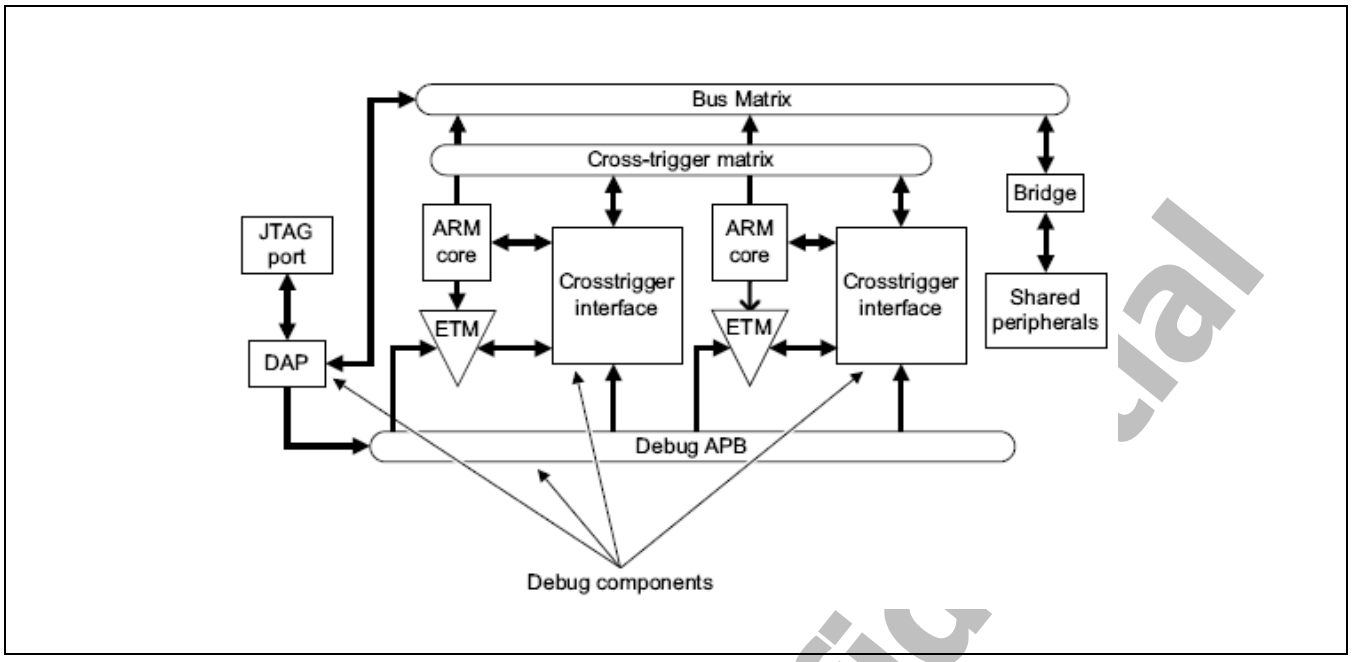

Figure 2-1 DAP Connections Inside a SoC Cross Triggering

The Embedded Cross Trigger (ECT), comprising of the Cross Trigger Interface (CTI) and Cross Trigger Matrix (CTM), provides a standard interconnect mechanism to pass debug or profiling events around the SoC.

The ECT provides a standard mechanism to connect different signal types. A set of standard triggers for cores are predefined and you can add triggers for third party cores.

The ECT enables tool developers to supply a standard control dialog so that software programmers can connect trigger events.

2.1.2.2 Trace

The CoreSight Design Kit provides components that support a standard infrastructure for the capture and transmission of trace data, combination of multiple data streams by funneling together, and then output of data to a trace port or storing in an on-chip buffer.

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2.1.2.3 Coresight System in S5PV210

S5PV210 is single processor system with CortexA8 core. Its main bus system is based on AMBA3 AXI interconnects. It does not support Serial Wire debug port protocol.

Figure 2-2 shows configuration of debugging system.

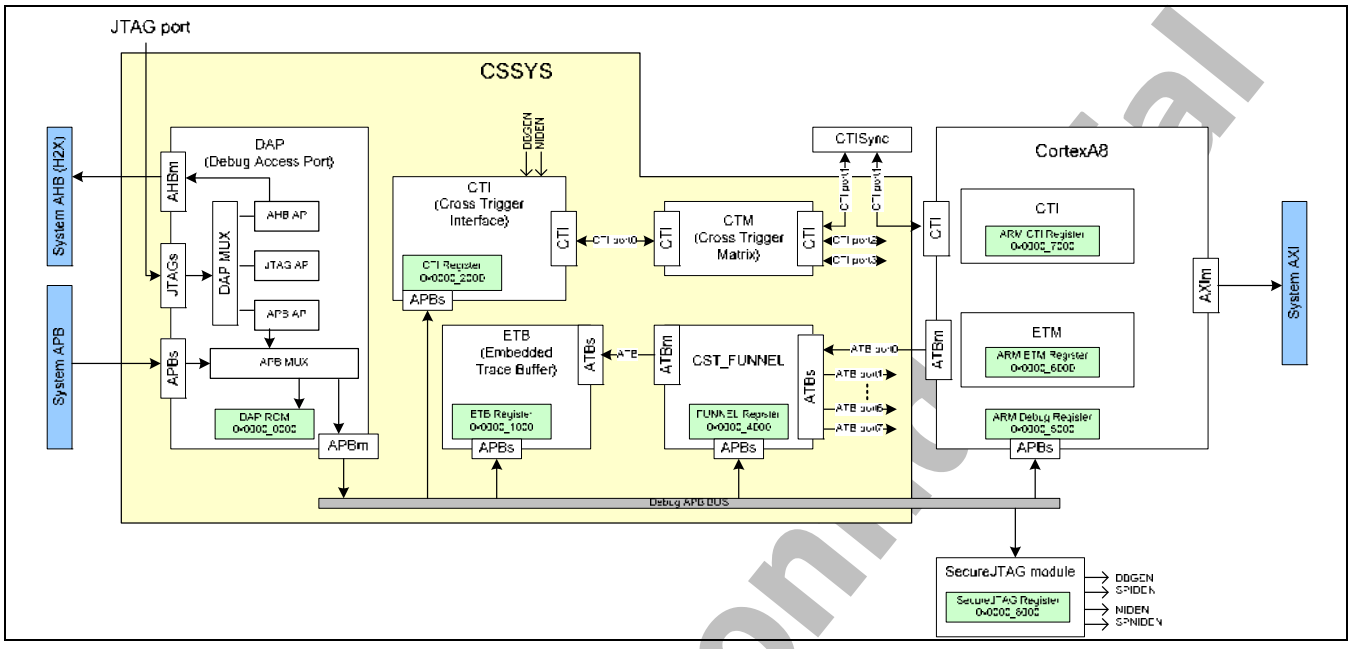

Figure 2-2 S5PV210 Coresight Structure

Although Coresight's registers can be accessed through system APB bus as well as JTAG port, the address map of those registers are observed differently. While the memory map for JTAG port is same as shows in *Figure 2-2*, the memory map for system view is same as the memory map for JTAG port + system register offset. The debugger register map of S5PV210 is summarized in *Figure 2-3*.

System view		Debugger view
0xE0D0_8000	SecureJTAG	0x0000_8000 or 0x8000_8000
0xE0D0_7000	CortexA8 CTI	0x0000_7000 or 0x8000_7000
0xE0D0_6000	CortexA8 embedded trace mactocell	0x0000_6000 or 0x8000_6000
0xE0D0_5000	CortexA8 Debug	0x0000_5000 or 0x8000_5000
0xE0D0_4000	Coresight FUNNEL	0x0000_4000 or 0x8000_4000
0xE0D0_3000	Reserved	0x0000_3000 or 0x8000_3000
0xE0D0_2000	Coresight CTI	0x0000_2000 or 0x8000_2000
0xE0D0_1000	Coresight ETB	0x0000_1000 or 0x8000_1000
0xE0D0_0000	ROM table	0x0000_0000 or 0x8000_0000

Figure 2-3 Debugger Register Map of S5PV210

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2.2 DEBUG ACCESS PORT

2.2.1 ABOUT DEBUG ACCESS PORT

The Debug Access Port (DAP) is an implementation of ARM Debug Interface version 5 (ADIv5) comprising a number of components supplied in a single configuration. All the supplied components fit into the various architectural components for Debug Ports (DPs), which are used to access the DAP from an external debugger and Access Ports (APs), to access on-chip system resources.

The debug port and access ports together are referred to as DAP.

The DAP provides real-time access to the debugger without halting the core to:

- AMBA system memory and peripheral registers
- All debug configuration registers.

The DAP also provides debugger access to JTAG scan chains of system components, for example non-CoreSight compliant processors. *Figure 2-4* shows the top-level view of the functional blocks of the DAP.

The DAP enables debug access to the complete SoC using a number of master ports.

Access to the CoreSight Debug Advanced Peripheral Bus (APB) is enabled through the APB Access Port (APB-AP) and APB Multiplexer (APB-MUX), and system access through the Advanced High-performance Bus Access Port (AHB-AP).

The DAP comprises of following interface blocks:

- External debug access using the JTAG Debug Port.
  - External JTAG access using the JTAG Debug Port (JTAG-DP).
- System access using:
  - AHB-AP
  - APB-AP
  - JTAG-AP
  - DAPBUS exported interface.
- An APB multiplexer enables system access to CoreSight components connected to the Debug APB.
- The ROM table provides a list of memory locations of CoreSight components connected to the Debug APB. This is visible from both tools and system access.

There are three access ports supplied in the DAP, and it is possible to connect a fourth access port externally.

The supplied access ports within this release are:

- AHB-AP for connection to the main system bus
- APB-AP to enable direct connection to the dedicated Debug Bus
- JTAG-AP to control up to eight scan chains.

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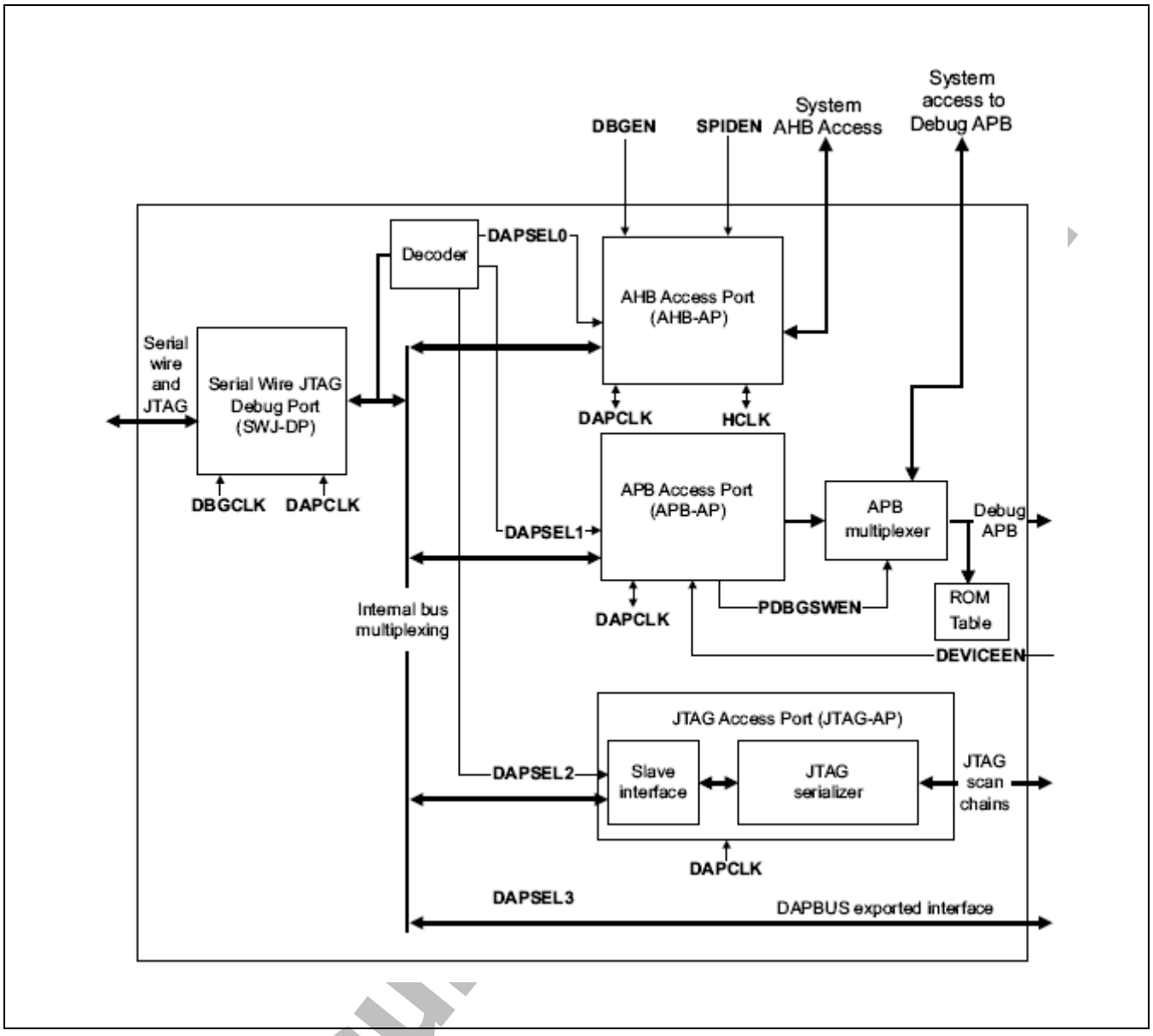

Figure 2-4 Structure of the Coresight DAP Components

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2.3 ETB

2.3.1 ABOUT THE ETB

The ETB provides on-chip storage of trace data using 32-bit RAM. *Figure 2-5* shows the main ETB blocks. The ETB accepts trace data from CoreSight trace source components through an AMBA Trace Bus (ATB).

The ETB contains the following blocks:

- Formatter - Inserts source ID signals into the data packet stream so that trace data can be re-associated with its trace source after the data is read back out of the ETB.
- Control - Control registers for trace capture and flushing.
- APB interface - Read, write, and data pointers provide access to ETB registers. In addition, the APB interface supports wait states through the use of a PREADYDBG signal output by the ETB. The APB interface is synchronous to the ATB domain.
- Register bank - Contains the management, control, and status registers for triggers, flushing behavior, and external control.
- Trace RAM interface - Controls reads and writes to the Trace RAM.
- Memory BIST interface - Provides test access to the Trace RAM.

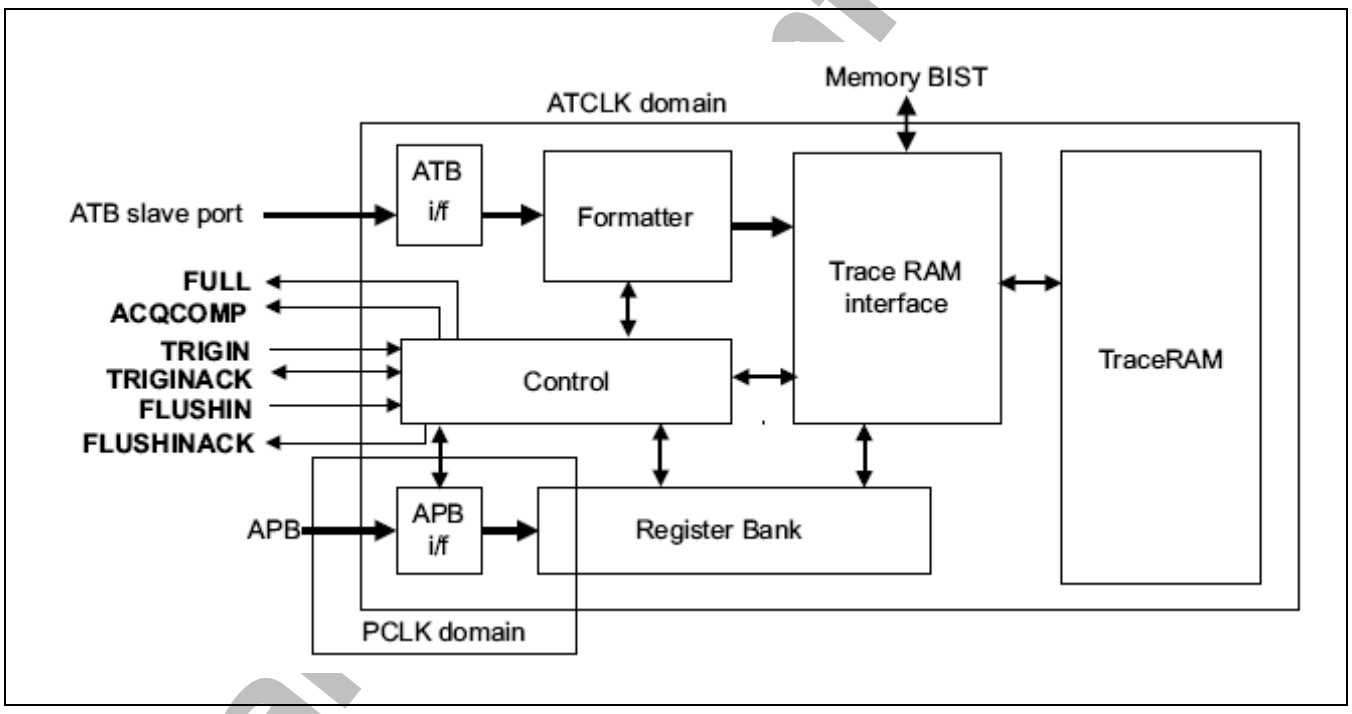

Figure 2-5 ETB Block Diagram ECT (CTI + CTM)

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2.3.2 ABOUT THE ECT

The ECT provides an interface to the debug system as shown in *Figure 2-6.* This enables an ARM subsystem to interact, that is cross trigger, with each other. The debug system enables debug support for multiple cores, together with cross triggering between the cores and their respective internal embedded trace macrocells.

The main function of the ECT (CTI and CTM) is to pass debug events from one processor to another. For example, the ECT can communicate debug state information from one core to another, so that program execution on both processors can be stopped at the same time if required.

- Cross Trigger Interface (CTI)
  The CTI combines and maps the trigger requests, and broadcasts them to all other interfaces on the ECT as channel events. When the CTI receives a channel event it maps this onto a trigger output. This enables subsystems to cross trigger with each other. The receiving and transmitting of triggers is performed through the trigger interface.
- Cross Trigger Matrix (CTM)
  This block controls the distribution of channel events. It provides Channel Interfaces (CIs) for connection to either CTIs or CTMs. This enables multiple CTIs to be linked together.

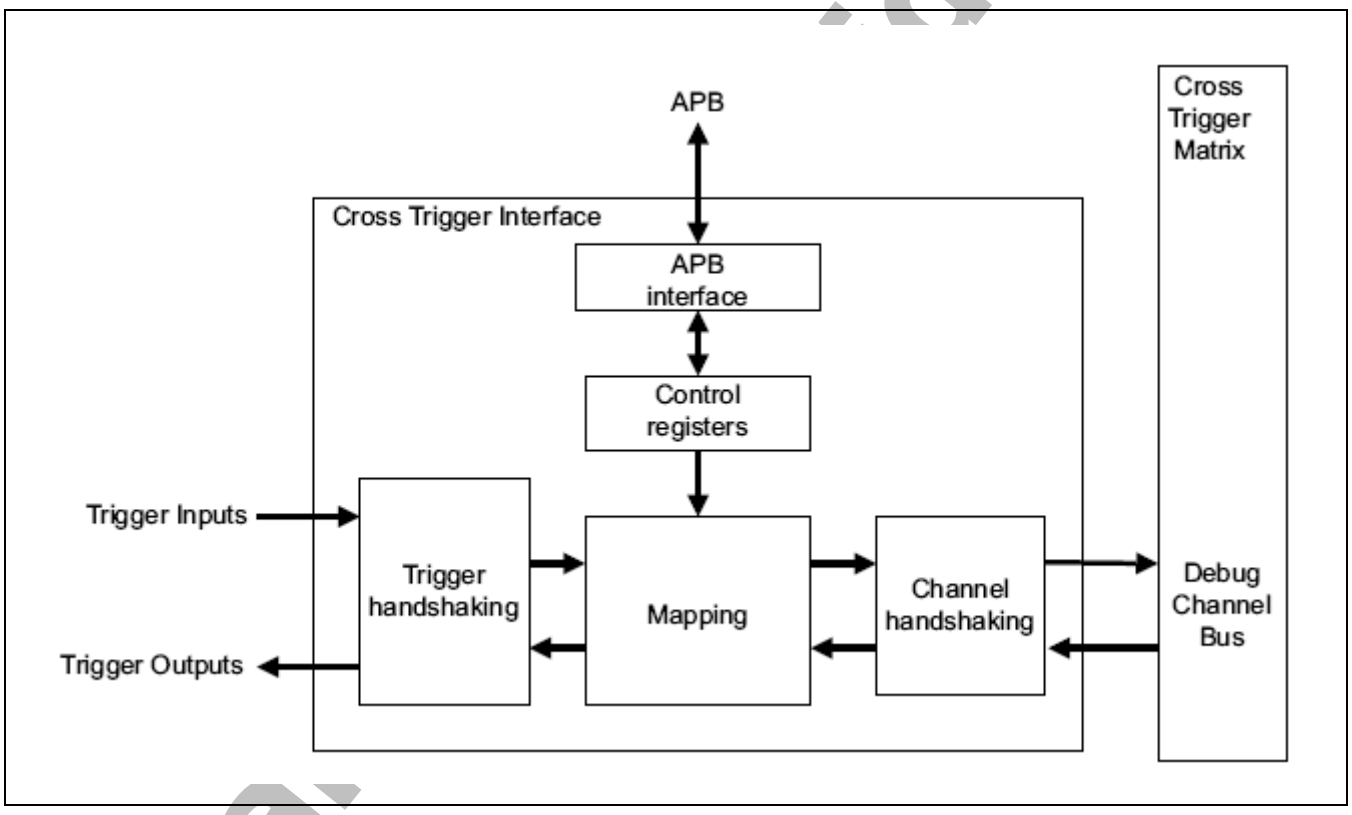

Figure 2-6 Coresight CTI and CTM Block Diagram

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3 ACCESS CONTROLLER (TZPC)

3.1 OVERVIEW OF ACCESS CONTROLLER (TZPC)

The TrustZone Protection Controller (TZPC) is an AMBA-compliant, tested, and licensed by ARM Limited. The TZPC provides a software interface to the protection bits in a secure system in a TrustZone design. It provides system flexibility that enables to configure different areas of memory as secure or non-secure.

The S5PV210 comprises of four TZPC.

3.1.1 KEY FEATURES OF ACCESS CONTROLLER (TZPC)

Protection bits: This enables you to program maximum 32 areas of memory as secure or non-secure

Secure region bits: This enables you to split an area of internal RAM into both secure and non-secure regions

The Access Controller includes AMBA APB system interface

3.1.2 BLOCK DIAGRAM OF ACCESS CONTROLLER (TZPC)

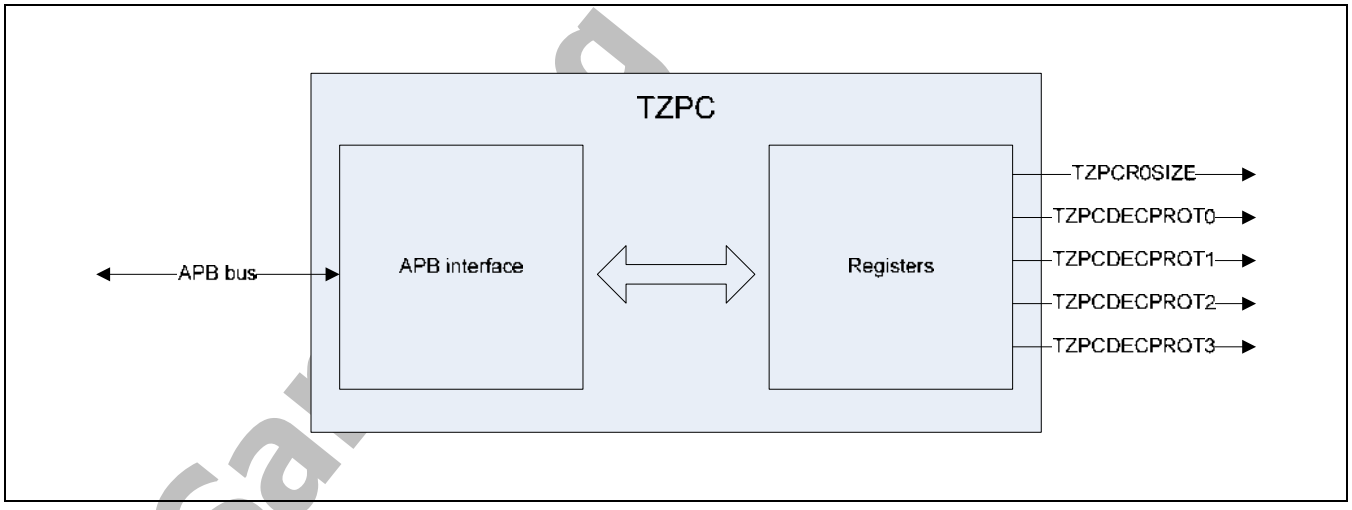

Figure 3-1 Block Diagram of Access Controller (TZPC)

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3.2 FUNCTIONAL DESCRIPTION

The TZPC provides a software interface to set up memory areas as secure or non-secure.

The two ways to set up memory area as secure or non-secure is as follows:

- Programmable protection bits that can be allocated to memory area as determined by the external decoder.
- Programmable region size value for use by an AXI TrustZone Memory Adapter (TZMA). You can use this to split the RAM into two regions:
  - One secure
  - One non-secure

This enables the best use of memory and other system resources. It is assumed that the specific secure and non-secure requirements for an application are determined during:

- Boot-up
- OS or secure kernel port development work

This means that the secure and non-secure memory partitioning is not expected to change dynamically during normal software operation because it is fixed at compile time and is only configured once during system boot-up. Ensure that this boot-up is always made in secure-state to guarantee full security protection.

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3.3 TZPC CONFIGURATION

Table 3-1 TZPC Table

Register	Bit	TZPC0	TZPC1	TZPC2	TZPC3
		Module Name	Module Name	Module Name	Module Name
TZPCDECPROT0	[0]	-	XBLOCK*	CHIPID	HDMI_CEC
	[1]	-	TBLOCK*	SYSCON	UBLOCK*
	[2]	DMC0	-	GPIO	GBLOCK*
	[3]	DMC1	HDMI_LINK	-	AUDIO(I2S0)**
	[4]	-	MDMA	-	-
	[5]	INTC*	-	-	-
	[6]	MFC	DSIM	IEM_APC	I2S2
	[7]	G3D	CSIS	IEM_IEC	PCM2
TZPCDECPROT1	[0]	-	-	PDMA0	-
	[1]	SDM	-	PDMA1	-
	[2]	-	I2C_HDMI_PHY	CORESIGHT	-
	[3]	-	-	-	-
	[4]	-	I2C_HDMI_DDC	SPDIF	-
	[5]	-	-	PCM1	-
	[6]	-	-	SPI0	-
	[7]	-	LBLOCK*	SPI1	-
TZPCDECPROT2	[0]	-	MDNIE	SPI2	-
	[1]	-	-	KEYIF	-
	[2]	-	-	TSADC	-
	[3]	-	-	I2C0(general)	-
	[4]	-	-	I2C(PMIC)	-
	[5]	-	-	I2S1	-
	[6]	-	-	AC97	-
	[7]	-	-	PCM0	-
TZPCDECPROT3	[0]	-	-	-	
	[1]	-	-	PWM	
	[2]	-	-	ST	
	[3]	-	-	WDT	
	[4]	-	-	RTC	-
	[5]	-	-	UART	-
	[6]	-	-	SBLOCK*	-
	[7]	-	-	CBLOCK*	-
TZPCR0SIZE		IntMEM	-	-	-

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* XBLOCK, TBLOCK, UBLOCK, GBLOCK, LBLOCK, SBLOCK, CBLOCK and INTC

Refer to *Figure 3-1* of Section 2-3.S5PV210_CMU.

** AUDIO includes I2S0.

If non-secure master accesses to secure slave area, DECERR occurs.

Table 3-2 TZPC Transfer Attribute

Master Attribute	Transfer Attribute	Slave/Area Attribute	Response
Secure Master	Secure Transfer	Secure Slave / Area	OK
	Secure Transfer	Non-Secure Slave / Area	OK
	Non-Secure Transfer	Secure Slave / Area	DECERR
	Non-Secure Transfer	Non-Secure Slave / Area	OK

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3.4 REGISTER DISCRIPTION

3.4.1 REGISTER MAP

Table 3-3 TZPC Registers

Register	Address	R/W	Description	Reset Value
TZPC0				
TZPCR0SIZE	0xF150_0000	R/W	Specifies the Secure RAM Region Size Register	0x00000000
TZPCDECPROT0Stat	0xF150_0800	R	Specifies the Decode Protection 0 Status Register	0x00000000
TZPCDECPROT0Set	0xF150_0804	W	Specifies the Decode Protection 0 Set Register	-
TZPCDECPROT0Clr	0xF150_0808	W	Specifies the Decode Protection 0 Clear Register	-
TZPCDECPROT1Stat	0xF150_080C	R	Specifies the Decode Protection 1 Status Register	0x00000000
TZPCDECPROT1Set	0xF150_0810	W	Specifies the Decode Protection 1 Set Register	-
TZPCDECPROT1Clr	0xF150_0814	W	Specifies the Decode Protection 1 Clear Register	-
TZPCDECPROT2Stat	0xF150_0818	R	Specifies the Decode Protection 2 Status Register	0x00000000
TZPCDECPROT2Set	0xF150_081C	W	Specifies the Decode Protection 2 Set Register	-
TZPCDECPROT2Clr	0xF150_0820	W	Specifies the Decode Protection 2 Clear Register	-
TZPCDECPROT3Stat	0xF150_0824	R	Not used	0x00000000
TZPCDECPROT3Set	0xF150_0828	W	Not used	-
TZPCDECPROT3Clr	0xF150_082C	W	Not used	-
TZPCPERIPHID0	0xF150_0FE0	R	Specifies the TZPC Peripheral Identification Register 0	0x00000070
TZPCPERIPHID1	0xF150_0FE4	R	Specifies the TZPC Peripheral Identification Register 1	0x00000018
TZPCPERIPHID2	0xF150_0FE8	R	Specifies the TZPC Peripheral Identification Register 2	0x00000004
TZPCPERIPHID3	0xF150_0FEC	R	Not used	0x00000000
TZPCPCELLID0	0xF150_0FF0	R	Specifies the TZPC Identification Register 0	0x0000000D
TZPCPCELLID1	0xF150_0FF4	R	Specifies the TZPC Identification Register 1	0x000000F0
TZPCPCELLID2	0xF150_0FF8	R	Specifies the TZPC Identification Register 2	0x00000005
TZPCPCELLID3	0xF150_0FFC	R	Not used	0x000000B1
TZPC1				

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Register	Address	R/W	Description	Reset Value
TZPCR0SIZE	0xFAD0_0000	R/W	Not used	0x00000200
TZPCDECPROT0Stat	0xFAD0_0800	R	Specifies the Decode Protection 0 Status Register	0x00000000
TZPCDECPROT0Set	0xFAD0_0804	W	Specifies the Decode Protection 0 Set Register	-
TZPCDECPROT0Clr	0xFAD0_0808	W	Specifies the Decode Protection 0 Clear Register	-
TZPCDECPROT1Stat	0xFAD0_080C	R	Specifies the Decode Protection 1 Status Register	0x00000000
TZPCDECPROT1Set	0xFAD0_0810	W	Specifies the Decode Protection 1 Set Register	-
TZPCDECPROT1Clr	0xFAD0_0814	W	Specifies the Decode Protection 1 Clear Register	-
TZPCDECPROT2Stat	0xFAD0_0818	R	Specifies the Decode Protection 2 Status Register	0x00000000
TZPCDECPROT2Set	0xFAD0_081C	W	Specifies the Decode Protection 2 Set Register	-
TZPCDECPROT2Clr	0xFAD0_0820	W	Specifies the Decode Protection 2 Clear Register	-
TZPCDECPROT3Stat	0xFAD0_0824	R	Not used	0x00000000
TZPCDECPROT3Set	0xFAD0_0828	W	Not used	-
TZPCDECPROT3Clr	0xFAD0_082C	W	Not used	-
TZPCPERIPHID0	0xFAD0_0FE0	R	Specifies the TZPC Peripheral Identification Register 0	0x00000070
TZPCPERIPHID1	0xFAD0_0FE4	R	Specifies the TZPC Peripheral Identification Register 1	0x00000018
TZPCPERIPHID2	0xFAD0_0FE8	R	Specifies the TZPC Peripheral Identification Register 2	0x00000004
TZPCPERIPHID3	0xFAD0_0FEC	R	Not used	0x00000000
TZPCPCELLID0	0xFAD0_0FF0	R	Specifies the TZPC Identification Register 0	0x0000000D
TZPCPCELLID1	0xFAD0_0FF4	R	Specifies the TZPC Identification Register 1	0x000000F0
TZPCPCELLID2	0xFAD0_0FF8	R	Specifies the TZPC Identification Register 2	0x00000005
TZPCPCELLID3	0xFAD0_0FFC	R	Not used	0x000000B1
TZPC2				
TZPCR0SIZE	0xE060_0000	R/W	Not used	0x00000200
TZPCDECPROT0Stat	0xE060_0800	R	Specifies the Decode Protection 0 Status Register	0x00000000
TZPCDECPROT0Set	0xE060_0804	W	Specifies the Decode Protection 0 Set Register	-
TZPCDECPROT0Clr	0xE060_0808	W	Specifies the Decode Protection 0 Clear Register	-

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Register	Address	R/W	Description	Reset Value
TZPCDECPROT1Stat	0xE060_080C	R	Specifies the Decode Protection 1 Status Register	0x00000000
TZPCDECPROT1Set	0xE060_0810	W	Specifies the Decode Protection 1 Set Register	-
TZPCDECPROT1Clr	0xE060_0814	W	Specifies the Decode Protection 1 Clear Register	-
TZPCDECPROT2Stat	0xE060_0818	R	Specifies the Decode Protection 2 Status Register	0x00000000
TZPCDECPROT2Set	0xE060_081C	W	Specifies the Decode Protection 2 Set Register	-
TZPCDECPROT2Clr	0xE060_0820	W	Specifies the Decode Protection 2 Clear Register	-
TZPCDECPROT3Stat	0xE060_0824	R	Specifies the Decode Protection 3 Status Register	0x00000000
TZPCDECPROT3Set	0xE060_0828	W	Specifies the Decode Protection 3 Set Register	-
TZPCDECPROT3Clr	0xE060_082C	W	Specifies the Decode Protection 3 Clear Register	-
TZPCPERIPHID0	0xE060_0FE0	R	Specifies the TZPC Peripheral Identification Register 0	0x00000070
TZPCPERIPHID1	0xE060_0FE4	R	Specifies the TZPC Peripheral Identification Register 1	0x00000018
TZPCPERIPHID2	0xE060_0FE8	R	Specifies the TZPC Peripheral Identification Register 2	0x00000000
TZPCPERIPHID3	0xE060_0FEC	R	Specifies the TZPC Peripheral Identification Register 3	0x00000004
TZPCPCELLID0	0xE060_0FF0	R	Specifies the TZPC Identification Register 0	0x0000000D
TZPCPCELLID1	0xE060_0FF4	R	Specifies the TZPC Identification Register 1	0x000000F0
TZPCPCELLID2	0xE060_0FF8	R	Specifies the TZPC Identification Register 2	0x00000005
TZPCPCELLID3	0xE060_0FFC	R	Specifies the TZPC Identification Register 3	0x000000B1
TZPC3				
TZPCR0SIZE	0xE1C0_0000	R/W	Not used	0x00000200
TZPCDECPROT0Stat	0xE1C0_0800	R	Specifies the Decode Protection 0 Status Register	0x00000000
TZPCDECPROT0Set	0xE1C0_0804	W	Specifies the Decode Protection 0 Set Register	-
TZPCDECPROT0Clr	0xE1C0_0808	W	Specifies the Decode Protection 0 Clear Register	-
TZPCDECPROT1Stat	0xE1C0_080C	R	Not used	0x00000000
TZPCDECPROT1Set	0xE1C0_0810	W	Not used	-
TZPCDECPROT1Clr	0xE1C0_0814	W	Not used	-

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Register	Address	R/W	Description	Reset Value
TZPCDECPROT2Stat	0xE1C0_0818	R	Not used	0x00000000
TZPCDECPROT2Set	0xE1C0_081C	W	Not used	-
TZPCDECPROT2Clr	0xE1C0_0820	W	Not used	-
TZPCDECPROT3Stat	0xE1C0_0824	R	Not used	0x00000000
TZPCDECPROT3Set	0xE1C0_0828	W	Not used	-
TZPCDECPROT3Clr	0xE1C0_082C	W	Not used	-
TZPCPERIPHID0	0xE1C0_0FE0	R	Specifies the TZPC Peripheral Identification Register 0	0x00000070
TZPCPERIPHID1	0xE1C0_0FE4	R	Not used	0x00000018
TZPCPERIPHID2	0xE1C0_0FE8	R	Not used	0x00000004
TZPCPERIPHID3	0xE1C0_0FEC	R	Not used	0x00000000
TZPCPCELLID0	0xE1C0_0FF0	R	Specifies the TZPC Identification Register 0	0x0000000D
TZPCPCELLID1	0xE1C0_0FF4	R	Not used	0x000000F0
TZPCPCELLID2	0xE1C0_0FF8	R	Not used	0x00000005
TZPCPCELLID3	0xE1C0_0FFC	R	Not used	0x000000B1

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3.4.1.1 Secure RAM Region Size Register (TZPCR0SIZE(TZPC0), RW, Address = 0xF150_0000)

TZPCR0SIZE	Bit	Description	Initial State
Reserved	[31:6]	Read undefined. Write as zero.	0
R0Size	[5:0]	Secure RAM region size in 4KB steps. 0x00000000 = no secure region 0x00000001 = 4KB secure region 0x00000002 = 8KB secure region … 0x0000001F = 128KB secure region 0x00000020 or above sets the entire RAM to secure regardless of size	0x0

3.4.1.2 Decode Protection 0-3 Status Registers

- TZPCDECPROTxSTAT(TZPC0), R, Address = 0xF150_0800, 0xF150_080C, 0xF150_0818
- TZPCDECPROTxSTAT(TZPC1), R, Address = 0xFAD0_0800, 0xFAD0_080C, 0xFAD0_0818
- TZPCDECPROTxSTAT(TZPC2), R, Address = 0xE060_0800, 0xE060_080C, 0xE060_0818
- TZPCDECPROTxSTAT(TZPC3), R, Address = 0xE1C0_0800, 0xE1C0_080C, 0xE1C0_0818

TXPCDECPROTxStat	Bit	Description	Initial State
Reserved	[31:8]	Read undefined.	0
DECPROTxStat	[7:0]	Show the status of the decode protection output: 0 = Decode region corresponding to the bit is secure 1 = Decode region corresponding to the bit is non-secure There is one bit of the register for each protection output, eight outputs are implemented as standard.	0x000

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3.4.1.3 Decode Protection 0-2 Set Registers

- TZPCDECPROTxSet(TZPC0), W, Address = 0xF150_0804, 0xF150_0810, 0xF150_081C
- TZPCDECPROTxSet(TZPC1), W, Address = 0xFAD0_0804, 0xFAD0_0810, 0xFAD0_081C
- TZPCDECPROTxSet(TZPC2), W, Address = 0xE060_0804, 0xE060_0810, 0xE060_081C
- TZPCDECPROTxSet(TZPC3), W, Address = 0xE1C0_0804, 0xE1C0_0810, 0xE1C0_081C

TXPCDECPROTxSet	Bit	Description	Initial State
Reserved	[31:8]	Write as zero.	-
DECPROTxSet	[7:0]	Sets the corresponding decode protection output: 0 = No effect 1 = Set decode region to non-secure There is one bit of the register for each protection output, eight outputs are implemented as standard.	-

3.4.1.4 Decode Protection 0-2 Clear Registers

- TZPCDECPROTxClr(TZPC0), W, Address = 0xF150_0808, 0xF150_081C, 0xF150_0820
- TZPCDECPROTxClr(TZPC1), W, Address = 0xFAD0_0808, 0xFAD0_081C, 0xFAD0_0820
- TZPCDECPROTxClr(TZPC2), W, Address = 0xE060_0808, 0xE060_081C, 0xE060_0820
- TZPCDECPROTxClr(TZPC3), W, Address = 0xE1C0_0808, 0xE1C0_081C, 0xE1C0_0820

TXPCDECPROTxClr	Bit	Description	Initial State
Reserved	[31:8]	Write as zero.	
DECPROTxClr	[7:0]	Clears the corresponding decode protection output: 0 = No effect 1 = Set decode region to secure There is one bit of the register for each protection output, eight outputs are implemented as standard.	

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3.4.1.5 TZPC Peripheral Identification Register 0
(TZPCPERIPHID0, R, Address = 0xF150_0FE0, 0xFAD0_0FE0, 0xE060_0FE0, 0xE1C0_0FE0)

TZPCPERIPHID0	Bit	Description	Initial State
Reserved	[31:8]	Read undefined	0
Partnumber0	[7:0]	These bits read back as 0x70	0x70

3.4.1.6 TZPC Peripheral Identification Register 1
(TZPCPERIPHID1, R, Address = 0xF150_0FE4, 0xFAD0_0FE4, 0xE060_0FE4, 0xE1C0_0FE4)

TZPCPERIPHID1	Bit	Description	Initial State
Reserved	[31:8]	Read undefined	0
Designer0	[7:4]	These bits read back as 0x1	0x1
Partnumber1	[3:0]	These bits read back as 0x8	0x8

3.4.1.7 TZPC Peripheral Identification Register 2
(TZPCPERIPHID2, R, Address = 0xF150_0FE8, 0xFAD0_0FE8, 0xE060_0FE8, 0xE1C0_0FE8)

TZPCPERIPHID2	Bit	Description	Initial State
Reserved	[31:8]	Read undefined	0
Revision	[7:4]	These bits read back as the revision number which can be 0-15	0x0
Designer1	[3:0]	These bits read back as 0x4	0x4

3.4.1.8 TZPC Peripheral Identification Register 3
(TZPCPERIPHID3, R, Address = 0xF150_0FEC, 0xFAD0_0FEC, 0xE060_0FEC, 0xE1C0_0FEC)

TZPCPERIPHID3	Bit	Description	Initial State
Reserved	[31:8]	Read undefined	0
Configuration	[7:0]	These bits read back as 0x00	0x0

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3.4.1.9 Identification Register 0
(TZPCPCELLID0, R, Address = 0xF150_0FF0, 0xFAD0_0FF0, 0xE060_0FF0, 0xE1C0_0FF0)

TZPCPCELLID0	Bit	Description	Initial State
Reserved	[31:8]	Read undefined	0
TZPCPCELLID0	[7:0]	These bits read back as 0x0D	0x0D

3.4.1.10 Identification Register 1
(TZPCPCELLID1, R, Address = 0xF150_0FF4, 0xFAD0_0FF4, 0xE060_0FF4, 0xE1C0_0FF4)

TZPCPCELLID1	Bit	Description	Initial State
Reserved	[31:8]	Read undefined	0
TZPCPCELLID1	[7:0]	These bits read back as 0xF0	0xF0

3.4.1.11 Identification RegisteR 2
(TZPCPCELLID2, R, Address = 0xF150_0FF8, 0xFAD0_0FF8, 0xE060_0FF8, 0xE1C0_0FF8)

TZPCPCELLID2	Bit	Description	Initial State
Reserved	[31:8]	Read undefined	0
TZPCPCELLID2	[7:0]	These bits read back as 0x05	0x05

3.4.1.12 Identification RegisteR 3
(TZPCPCELLID3, R, Address = 0xF150_0FFC, 0xFAD0_0FFC, 0xE060_0FFC, 0xE1C0_0FFC)

TZPCPCELLID3	Bit	Description	Initial State
Reserved	[31:8]	Read undefined	0
TZPCPCELLID3	[7:0]	These bits read back as 0x00	0x00

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Section 4

INTERRUPT

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1 Vectored Interrupt Controller 1-1

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1 VECTORED INTERRUPT CONTROLLER

1.1 OVERVIEW OF VECTORED INTERRUPT CONTROLLER

The interrupt controller in S5PV210 is composed of four Vectored Interrupt Controller (VIC), ARM PrimeCell PL192 and four TrustZone Interrupt Controller (TZIC), SP890.

Four TZIC's and four VIC's are daisy-chained to support up to 93 interrupt sources. The TZIC provides a software interface to the secure interrupt system in a TrustZone design. It provides secure control of the nFIQ interrupt and masks the interrupt source(s) from the interrupt controller on the non-secure side of the system (VIC). Use the latter to generate nIRQ signal.

To generate nFIQ from the non-secure interrupt sources, the TZIC0 takes the nNSFIQIN signal from the non-secure interrupt controller.

1.1.1 KEY FEATURES OF VECTORED INTERRUPT CONTROLLER

- Supports 93 vectored IRQ interrupts
- Fixed hardware interrupts priority levels
- Programmable interrupt priority levels
- Supports Hardware interrupt priority level masking
- Programmable interrupt priority level masking
- Generates IRQ and FIQ
- Generates Software interrupt
- Test registers
- Raw interrupt status
- Interrupt request status
- Supports Privileged mode for restricted access

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1.2 NTERRUPT SOURCE

The S5PV210 supports interrupt sources as shown in the Table below.

Module	VIC port no	No	INT Request	Remark
VIC3 Multimedia, Audio, Security, Etc.,	31	127		
	30	126		
	29	125		
	28	124		
	27	123		
	26	122		
	25	121		
	24	120		
	23	119		
	22	118		
	21	117		
	20	116		
	19	115		
	18	114		
	17	113		
	16	112		
	15	111		
	14	110		
	13	109		
	12	108		
	11	107		
	10	106	PENDN1 (TSADC)	
	9	105	ADC1 (TSADC)	
	8	104		
	7	103		
	6	102		
	5	101		
	4	100	TSI	
	3	99	CEC	
	2	98	MMC3	
	1	97		
	0	96		
VIC2	31	95	SDM_FIQ (security)	

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Module	VIC port no	No	INT Request	Remark
Multimedia, Audio, Security, Etc.,	30	94	SDM_IRQ (security)	
	29	93	PCM2	
	28	92	IntFeedCtrl_SSS	
	27	91	IntHash_SSS	
	26	90		
	25	89	KEYPAD	
	24	88	PENDN (TSADC)	
	23	87	ADC (TSADC)	
	22	86	SPDIF	
	21	85	PCM1	
	20	84	PCM0	
	19	83	AC97	
	18	82		
	17	81	I2S1	
	16	80	I2S0	
	15	79	TVENC	
	14	78	MFC	
	13	77	I2C_HDMI_DDC	
	12	76	HDMI	
	11	75	Mixer	
	10	74	3D	
	9	73	2D	
	8	72	JPEG	
	7	71	FIMC2	
	6	70	FIMC1	
	5	69	FIMC0	
	4	68	ROTATOR	
	3	67		
	2	66	LCD[2]	
	1	65	LCD[1]	
	0	64	LCD[0]	
VIC1 ARM, power, memory,	31	63	ONENAND_AUDI	
	30	62	MIPI_DSI	
	29	61	MIPI_CSI	
	28	60	HSMMC2	
	27	59	HSMMC1	

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Module	VIC port no	No	INT Request	Remark
Connectivity, Storage	26	58	HSMMC0	
	25	57	MODEMIF	
	24	56	OTG (usb)	
	23	55	UHOST (usb)	
	22	54		
	21	53		
	20	52	I2C_HDMI_PHY	
	19	51	I2C2	
	18	50	AUDIO_SS	
	17	49		
	16	48	SPI1	
	15	47	SPI0	
	14	46	I2C0	
	13	45	UART3	
	12	44	UART2	
	11	43	UART1	
	10	42	UART0	
	9	41	CFC	
	8	40	NFC	
	7	39		
	6	38	IEM_IEC	
	5	37	IEM_APC	
	4	36	CORTEX4	
			(nCTIIRQ)	
	3	35	CORTEX3	
			(nDMAEXTERIRQ)	
	2	34	CORTEX2	
			(nDMAIRQ)	
	1	33	CORTEX1 (nDMASIRQ)	
	0	32	CORTEX0 (nPMUIRQ)	
VIC0 System, DMA, Timer	31	31	FIMC3	
	30	30	GPIOINT	All other GPIO interrupt mux
	29	29	RTC_TIC	
	28	28	RTC_ALARM	
	27	27	WDT	

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Module	VIC port no	No	INT Request	Remark
	26	26	System Timer	
	25	25	TIMER4	
	24	24	TIMER3	
	23	23	TIMER2	
	22	22	TIMER1	
	21	21	TIMER0	
	20	20	PDMA1	
	19	19	PDMA0	
	18	18	MDMA	
	17	17		
	16	16	EINT 16_31	EXT_INT[16] ~ [31]
	15	15	EINT15	EXT_INT[15]
	14	14	EINT14	EXT_INT[14]
	13	13	EINT13	EXT_INT[13]
	12	12	EINT12	EXT_INT[12]
	11	11	EINT11	EXT_INT[11]
	10	10	EINT10	EXT_INT[10]
	9	9	EINT9	EXT_INT[9]
	8	8	EINT8	EXT_INT[8]
	7	7	EINT7	EXT_INT[7]
	6	6	EINT6	EXT_INT[6]
	5	5	EINT5	EXT_INT[5]
	4	4	EINT4	EXT_INT[4]
	3	3	EINT3	EXT_INT[3]
	2	2	EINT2	EXT_INT[2]
	1	1	EINT1	EXT_INT[1]
	0	0	EINT0	EXT_INT[0]

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1.3 FUNCTIONAL DESCRIPTION

When user clears interrupt pending, user must write 0 to all the VICADDRESS registers (VIC0ADDRESS, VIC1ADDRESS, VIC2ADDRESS, and VIC3ADDRESS).

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1.4 REGISTER DESCRIPTION

1.4.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
VIC0IRQSTATUS	0xF200_0000	R	Specifies the IRQ Status Register	0x00000000
VIC0FIQSTATUS	0xF200_0004	R	Specifies the FIQ Status Register	0x00000000
VIC0RAWINTR	0xF200_0008	R	Specifies the Raw Interrupt Status Register	-
VIC0INTSELECT	0xF200_000C	R/W	Specifies the Interrupt Select Register	0x00000000
VIC0INTENABLE	0xF200_0010	R/W	Specifies the Interrupt Enable Register	0x00000000
VIC0INTENCLEAR	0xF200_0014	W	Specifies the Interrupt Enable Clear Register	-
VIC0SOFTINT	0xF200_0018	R/W	Specifies the Software Interrupt Register	0x00000000
VIC0SOFTINTCLEAR	0xF200_001C	W	Specifies the Software Interrupt Clear Register	-
VIC0PROTECTION	0xF200_0020	R/W	Specifies the Protection Enable Register	0x0
VIC0SWPRIORITYMASK	0xF200_0024	R/W	Software Priority Mask Register	0xFFFF
VIC0PRIORITYDAISY	0xF200_0028	R/W	Specifies the Vector Priority Register for Daisy Chain	0xF
VIC0VECTADDR0	0xF200_0100	R/W	Specifies the Vector Address 0 Register	0x00000000
VIC0VECTADDR1	0xF200_0104	R/W	Specifies the Vector Address 1 Register	0x00000000
VIC0VECTADDR2	0xF200_0108	R/W	Specifies the Vector Address 2 Register	0x00000000
VIC0VECTADDR3	0xF200_010C	R/W	Specifies the Vector Address 3 Register	0x00000000
VIC0VECTADDR4	0xF200_0110	R/W	Specifies the Vector Address 4 Register	0x00000000
VIC0VECTADDR5	0xF200_0114	R/W	Specifies the Vector Address 5 Register	0x00000000
VIC0VECTADDR6	0xF200_0118	R/W	Specifies the Vector Address 6 Register	0x00000000
VIC0VECTADDR7	0xF200_011C	R/W	Specifies the Vector Address 7 Register	0x00000000
VIC0VECTADDR8	0xF200_0120	R/W	Specifies the Vector Address 8 Register	0x00000000
VIC0VECTADDR9	0xF200_0124	R/W	Specifies the Vector Address 9 Register	0x00000000
VIC0VECTADDR10	0xF200_0128	R/W	Specifies the Vector Address 10 Register	0x00000000
VIC0VECTADDR11	0xF200_012C	R/W	Specifies the Vector Address 11 Register	0x00000000
VIC0VECTADDR12	0xF200_0130	R/W	Specifies the Vector Address 12 Register	0x00000000
VIC0VECTADDR13	0xF200_0134	R/W	Specifies the Vector Address 13 Register	0x00000000
VIC0VECTADDR14	0xF200_0138	R/W	Specifies the Vector Address 14 Register	0x00000000
VIC0VECTADDR15	0xF200_013C	R/W	Specifies the Vector Address 15 Register	0x00000000
VIC0VECTADDR16	0xF200_0140	R/W	Specifies the Vector Address 16 Register	0x00000000
VIC0VECTADDR17	0xF200_0144	R/W	Specifies the Vector Address 17 Register	0x00000000
VIC0VECTADDR18	0xF200_0148	R/W	Specifies the Vector Address 18 Register	0x00000000
VIC0VECTADDR19	0xF200_014C	R/W	Specifies the Vector Address 19 Register	0x00000000

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Register	Address	R/W	Description	Reset Value
VIC0VECTADDR20	0xF200_0150	R/W	Specifies the Vector Address 20 Register	0x00000000
VIC0VECTADDR21	0xF200_0154	R/W	Specifies the Vector Address 21 Register	0x00000000
VIC0VECTADDR22	0xF200_0158	R/W	Specifies the Vector Address 22 Register	0x00000000
VIC0VECTADDR23	0xF200_015C	R/W	Specifies the Vector Address 23 Register	0x00000000
VIC0VECTADDR24	0xF200_0160	R/W	Specifies the Vector Address 24 Register	0x00000000
VIC0VECTADDR25	0xF200_0164	R/W	Specifies the Vector Address 25 Register	0x00000000
VIC0VECTADDR26	0xF200_0168	R/W	Specifies the Vector Address 26 Register	0x00000000
VIC0VECTADDR27	0xF200_016C	R/W	Specifies the Vector Address 27 Register	0x00000000
VIC0VECTADDR28	0xF200_0170	R/W	Specifies the Vector Address 28 Register	0x00000000
VIC0VECTADDR29	0xF200_0174	R/W	Specifies the Vector Address 29 Register	0x00000000
VIC0VECTADDR30	0xF200_0178	R/W	Specifies the Vector Address 30 Register	0x00000000
VIC0VECTADDR31	0xF200_017C	R/W	Specifies the Vector Address 31 Register	0x00000000
VIC0VECPRIORITY0	0xF200_0200	R/W	Specifies the Vector Priority 0 Register	0xF
VIC0VECTPRIORITY1	0xF200_0204	R/W	Specifies the Vector Priority 1 Register	0xF
VIC0VECTPRIORITY2	0xF200_0208	R/W	Specifies the Vector Priority 2 Register	0xF
VIC0VECTPRIORITY3	0xF200_020C	R/W	Specifies the Vector Priority 3 Register	0xF
VIC0VECTPRIORITY4	0xF200_0210	R/W	Specifies the Vector Priority 4 Register	0xF
VIC0VECTPRIORITY5	0xF200_0214	R/W	Specifies the Vector Priority 5 Register	0xF
VIC0VECTPRIORITY6	0xF200_0218	R/W	Specifies the Vector Priority 6 Register	0xF
VIC0VECTPRIORITY7	0xF200_021C	R/W	Specifies the Vector Priority 7 Register	0xF
VIC0VECTPRIORITY8	0xF200_0220	R/W	Specifies the Vector Priority 8 Register	0xF
VIC0VECTPRIORITY9	0xF200_0224	R/W	Specifies the Vector Priority 9 Register	0xF
VIC0VECTPRIORITY10	0xF200_0228	R/W	Specifies the Vector Priority 10 Register	0xF
VIC0VECTPRIORITY11	0xF200_022C	R/W	Specifies the Vector Priority 11 Register	0xF
VIC0VECTPRIORITY12	0xF200_0230	R/W	Specifies the Vector Priority 12 Register	0xF
VIC0VECTPRIORITY13	0xF200_0234	R/W	Specifies the Vector Priority 13 Register	0xF
VIC0VECTPRIORITY14	0xF200_0238	R/W	Specifies the Vector Priority 14 Register	0xF
VIC0VECTPRIORITY15	0xF200_023C	R/W	Specifies the Vector Priority 15 Register	0xF
VIC0VECTPRIORITY16	0xF200_0240	R/W	Specifies the Vector Priority 16 Register	0xF
VIC0VECTPRIORITY17	0xF200_0244	R/W	Specifies the Vector Priority 17 Register	0xF
VIC0VECTPRIORITY18	0xF200_0248	R/W	Specifies the Vector Priority 18 Register	0xF
VIC0VECTPRIORITY19	0xF200_024C	R/W	Specifies the Vector Priority 19 Register	0xF
VIC0VECTPRIORITY20	0xF200_0250	R/W	Specifies the Vector Priority 20 Register	0xF
VIC0VECTPRIORITY21	0xF200_0254	R/W	Specifies the Vector Priority 21 Register	0xF
VIC0VECTPRIORITY22	0xF200_0258	R/W	Specifies the Vector Priority 22 Register	0xF
VIC0VECTPRIORITY23	0xF200_025C	R/W	Specifies the Vector Priority 23 Register	0xF

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Register	Address	R/W	Description	Reset Value
VIC0VECTPRIORITY24	0xF200_0260	R/W	Specifies the Vector Priority 24 Register	0xF
VIC0VECTPRIORITY25	0xF200_0264	R/W	Specifies the Vector Priority 25 Register	0xF
VIC0VECTPRIORITY26	0xF200_0268	R/W	Specifies the Vector Priority 26 Register	0xF
VIC0VECTPRIORITY27	0xF200_026C	R/W	Specifies the Vector Priority 27 Register	0xF
VIC0VECTPRIORITY28	0xF200_0270	R/W	Specifies the Vector Priority 28 Register	0xF
VIC0VECTPRIORITY29	0xF200_0274	R/W	Specifies the Vector Priority 29 Register	0xF
VIC0VECTPRIORITY30	0xF200_0278	R/W	Specifies the Vector Priority 30 Register	0xF
VIC0VECTPRIORITY31	0xF200_027C	R/W	Specifies the Vector Priority 31 Register	0xF
VIC0ADDRESS	0xF200_0F00	R/W	Specifies the Vector Address Register	0x00000000
VIC0PERIPHID0	0xF200_0FE0	R	Specifies the Peripheral Identification Register bit 7:0	0x92
VIC0PERIPHID1	0xF200_0FE4	R	Specifies the Peripheral Identification Register bit 15:9	0x11
VIC0PERIPHID2	0xF200_0FE8	R	Specifies the Peripheral Identification Register bit 23:16	0x04
VIC0PERIPHID3	0xF200_0FEC	R	Specifies the Peripheral Identification Register bit 31:24	0x00
VIC0PCELLID0	0xF200_0FF0	R	Specifies the PrimeCell Identification Register bit 7:0	0x0D
VIC0PCELLID1	0xF200_0FF4	R	Specifies the PrimeCell Identification Register bit 15:9	0xF0
VIC0PCELLID2	0xF200_0FF8	R	Specifies the PrimeCell Identification Register bit 23:16	0x05
VIC0PCELLID3	0xF200_0FFC	R	Specifies the PrimeCell Identification Register bit 31:24	0xB1
VIC1IRQSTATUS	0xF210_0000	R	Specifies the IRQ Status Register	0x00000000
VIC1FIQSTATUS	0xF210_0004	R	Specifies the FIQ Status Register	0x00000000
VIC1RAWINTR	0xF210_0008	R	Specifies the Raw Interrupt Status Register	-
VIC1INTSELECT	0xF210_000C	R/W	Specifies the Interrupt Select Register	0x00000000
VIC1INTENABLE	0xF210_0010	R/W	Specifies the Interrupt Enable Register	0x00000000
VIC1INTENCLEAR	0xF210_0014	W	Specifies the Interrupt Enable Clear Register	-
VIC1SOFTINT	0xF210_0018	R/W	Specifies the Software Interrupt Register	0x00000000
VIC1SOFTINTCLEAR	0xF210_001C	W	Specifies the Software Interrupt Clear Register	-
VIC1PROTECTION	0xF210_0020	R/W	Specifies the Protection Enable Register	0x0
VIC1SWPRIORITYMASK	0xF210_0024	R/W	Specifies the Software Priority Mask Register	0xFFFF
VIC1PRIORITYDAISY	0xF210_0028	R/W	Specifies the Vector Priority Register for	0xF

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Register	Address	R/W	Description	Reset Value
			Daisy Chain	
VIC1VECTADDR0	0xF210_0100	R/W	Specifies the Vector Address 0 Register	0x00000000
VIC1VECTADDR1	0xF210_0104	R/W	Specifies the Vector Address 1 Register	0x00000000
VIC1VECTADDR2	0xF210_0108	R/W	Specifies the Vector Address 2 Register	0x00000000
VIC1VECTADDR3	0xF210_010C	R/W	Specifies the Vector Address 3 Register	0x00000000
VIC1VECTADDR4	0xF210_0110	R/W	Specifies the Vector Address 4 Register	0x00000000
VIC1VECTADDR5	0xF210_0114	R/W	Specifies the Vector Address 5 Register	0x00000000
VIC1VECTADDR6	0xF210_0118	R/W	Specifies the Vector Address 6 Register	0x00000000
VIC1VECTADDR7	0xF210_011C	R/W	Specifies the Vector Address 7 Register	0x00000000
VIC1VECTADDR8	0xF210_0120	R/W	Specifies the Vector Address 8 Register	0x00000000
VIC1VECTADDR9	0xF210_0124	R/W	Specifies the Vector Address 9 Register	0x00000000
VIC1VECTADDR10	0xF210_0128	R/W	Specifies the Vector Address 10 Register	0x00000000
VIC1VECTADDR11	0xF210_012C	R/W	Specifies the Vector Address 11 Register	0x00000000
VIC1VECTADDR12	0xF210_0130	R/W	Specifies the Vector Address 12 Register	0x00000000
VIC1VECTADDR13	0xF210_0134	R/W	Specifies the Vector Address 13 Register	0x00000000
VIC1VECTADDR14	0xF210_0138	R/W	Specifies the Vector Address 14 Register	0x00000000
VIC1VECTADDR15	0xF210_013C	R/W	Specifies the Vector Address 15 Register	0x00000000
VIC1VECTADDR16	0xF210_0140	R/W	Specifies the Vector Address 16 Register	0x00000000
VIC1VECTADDR17	0xF210_0144	R/W	Specifies the Vector Address 17 Register	0x00000000
VIC1VECTADDR18	0xF210_0148	R/W	Specifies the Vector Address 18 Register	0x00000000
VIC1VECTADDR19	0xF210_014C	R/W	Specifies the Vector Address 19 Register	0x00000000
VIC1VECTADDR20	0xF210_0150	R/W	Specifies the Vector Address 20 Register	0x00000000
VIC1VECTADDR21	0xF210_0154	R/W	Specifies the Vector Address 21 Register	0x00000000
VIC1VECTADDR22	0xF210_0158	R/W	Specifies the Vector Address 22 Register	0x00000000
VIC1VECTADDR23	0xF210_015C	R/W	Specifies the Vector Address 23 Register	0x00000000
VIC1VECTADDR24	0xF210_0160	R/W	Specifies the Vector Address 24 Register	0x00000000
VIC1VECTADDR25	0xF210_0164	R/W	Specifies the Vector Address 25 Register	0x00000000
VIC1VECTADDR26	0xF210_0168	R/W	Specifies the Vector Address 26 Register	0x00000000
VIC1VECTADDR27	0xF210_016C	R/W	Specifies the Vector Address 27 Register	0x00000000
VIC1VECTADDR28	0xF210_0170	R/W	Specifies the Vector Address 28 Register	0x00000000
VIC1VECTADDR29	0xF210_0174	R/W	Specifies the Vector Address 29 Register	0x00000000
VIC1VECTADDR30	0xF210_0178	R/W	Specifies the Vector Address 30 Register	0x00000000
VIC1VECTADDR31	0xF210_017C	R/W	Specifies the Vector Address 31 Register	0x00000000
VIC1VECPRIORITY0	0xF210_0200	R/W	Specifies the Vector Priority 0 Register	0xF
VIC1VECTPRIORITY1	0xF210_0204	R/W	Specifies the Vector Priority 1 Register	0xF
VIC1VECTPRIORITY2	0xF210_0208	R/W	Specifies the Vector Priority 2 Register	0xF
VIC1VECTPRIORITY3	0xF210_020C	R/W	Specifies the Vector Priority 3 Register	0xF

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Register	Address	R/W	Description	Reset Value
VIC1VECTPRIORITY4	0xF210_0210	R/W	Specifies the Vector Priority 4 Register	0xF
VIC1VECTPRIORITY5	0xF210_0214	R/W	Specifies the Vector Priority 5 Register	0xF
VIC1VECTPRIORITY6	0xF210_0218	R/W	Specifies the Vector Priority 6 Register	0xF
VIC1VECTPRIORITY7	0xF210_021C	R/W	Specifies the Vector Priority 7 Register	0xF
VIC1VECTPRIORITY8	0xF210_0220	R/W	Specifies the Vector Priority 8 Register	0xF
VIC1VECTPRIORITY9	0xF210_0224	R/W	Specifies the Vector Priority 9 Register	0xF
VIC1VECTPRIORITY10	0xF210_0228	R/W	Specifies the Vector Priority 10 Register	0xF
VIC1VECTPRIORITY11	0xF210_022C	R/W	Specifies the Vector Priority 11 Register	0xF
VIC1VECTPRIORITY12	0xF210_0230	R/W	Specifies the Vector Priority 12 Register	0xF
VIC1VECTPRIORITY13	0xF210_0234	R/W	Specifies the Vector Priority 13 Register	0xF
VIC1VECTPRIORITY14	0xF210_0238	R/W	Specifies the Vector Priority 14 Register	0xF
VIC1VECTPRIORITY15	0xF210_023C	R/W	Specifies the Vector Priority 15 Register	0xF
VIC1VECTPRIORITY16	0xF210_0240	R/W	Specifies the Vector Priority 16 Register	0xF
VIC1VECTPRIORITY17	0xF210_0244	R/W	Specifies the Vector Priority 17 Register	0xF
VIC1VECTPRIORITY18	0xF210_0248	R/W	Specifies the Vector Priority 18 Register	0xF
VIC1VECTPRIORITY19	0xF210_024C	R/W	Specifies the Vector Priority 19 Register	0xF
VIC1VECTPRIORITY20	0xF210_0250	R/W	Specifies the Vector Priority 20 Register	0xF
VIC1VECTPRIORITY21	0xF210_0254	R/W	Specifies the Vector Priority 21 Register	0xF
VIC1VECTPRIORITY22	0xF210_0258	R/W	Specifies the Vector Priority 22 Register	0xF
VIC1VECTPRIORITY23	0xF210_025C	R/W	Specifies the Vector Priority 23 Register	0xF
VIC1VECTPRIORITY24	0xF210_0260	R/W	Specifies the Vector Priority 24 Register	0xF
VIC1VECTPRIORITY25	0xF210_0264	R/W	Specifies the Vector Priority 25 Register	0xF
VIC1VECTPRIORITY26	0xF210_0268	R/W	Specifies the Vector Priority 26 Register	0xF
VIC1VECTPRIORITY27	0xF210_026C	R/W	Specifies the Vector Priority 27 Register	0xF
VIC1VECTPRIORITY28	0xF210_0270	R/W	Specifies the Vector Priority 28 Register	0xF
VIC1VECTPRIORITY29	0xF210_0274	R/W	Specifies the Vector Priority 29 Register	0xF
VIC1VECTPRIORITY30	0xF210_0278	R/W	Specifies the Vector Priority 30 Register	0xF
VIC1VECTPRIORITY31	0xF210_027C	R/W	Specifies the Vector Priority 31 Register	0xF
VIC1ADDRESS	0xF210_0F00	R/W	Specifies the Vector Address Register	0x00000000
VIC1PERIPHID0	0xF210_0FE0	R	Specifies the Peripheral Identification Register bit 7:0	0x92
VIC1PERIPHID1	0xF210_0FE4	R	Specifies the Peripheral Identification Register bit 15:9	0x11
VIC1PERIPHID2	0xF210_0FE8	R	Specifies the Peripheral Identification Register bit 23:16	0x04
VIC1PERIPHID3	0xF210_0FEC	R	Specifies the Peripheral Identification Register bit 31:24	0x00
VIC1PCELLID0	0xF210_0FF0	R	Specifies the PrimeCell Identification	0x0D

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Register	Address	R/W	Description	Reset Value
			Register bit 7:0	
VIC1PCELLID1	0xF210_0FF4	R	Specifies the PrimeCell Identification Register bit 15:9	0xF0
VIC1PCELLID2	0xF210_0FF8	R	Specifies the PrimeCell Identification Register bit 23:16	0x05
VIC1PCELLID3	0xF210_0FFC	R	Specifies the PrimeCell Identification Register bit 31:24	0xB1
VIC2IRQSTATUS	0xF220_0000	R	Specifies the IRQ Status Register	0x00000000
VIC2FIQSTATUS	0xF220_0004	R	Specifies the FIQ Status Register	0x00000000
VIC2RAWINTR	0xF220_0008	R	Specifies the Raw Interrupt Status Register	-
VIC2INTSELECT	0xF220_000C	R/W	Specifies the Interrupt Select Register	0x00000000
VIC2INTENABLE	0xF220_0010	R/W	Specifies the Interrupt Enable Register	0x00000000
VIC2INTENCLEAR	0xF220_0014	W	Specifies the Interrupt Enable Clear Register	-
VIC2SOFTINT	0xF220_0018	R/W	Specifies the Software Interrupt Register	0x00000000
VIC2SOFTINTCLEAR	0xF220_001C	W	Specifies the Software Interrupt Clear Register	-
VIC2PROTECTION	0xF220_0020	R/W	Specifies the Protection Enable Register	0x0
VIC2SWPRIORITYMASK	0xF220_0024	R/W	Specifies the Software Priority Mask Register	0xFFFF
VIC2PRIORITYDAISY	0xF220_0028	R/W	Specifies the Vector Priority Register for Daisy Chain	0xF
VIC2VECTADDR0	0xF220_0100	R/W	Specifies the Vector Address 0 Register	0x00000000
VIC2VECTADDR1	0xF220_0104	R/W	Specifies the Vector Address 1 Register	0x00000000
VIC2VECTADDR2	0xF220_0108	R/W	Specifies the Vector Address 2 Register	0x00000000
VIC2VECTADDR3	0xF220_010C	R/W	Specifies the Vector Address 3 Register	0x00000000
VIC2VECTADDR4	0xF220_0110	R/W	Specifies the Vector Address 4 Register	0x00000000
VIC2VECTADDR5	0xF220_0114	R/W	Specifies the Vector Address 5 Register	0x00000000
VIC2VECTADDR6	0xF220_0118	R/W	Specifies the Vector Address 6 Register	0x00000000
VIC2VECTADDR7	0xF220_011C	R/W	Specifies the Vector Address 7 Register	0x00000000
VIC2VECTADDR8	0xF220_0120	R/W	Specifies the Vector Address 8 Register	0x00000000
VIC2VECTADDR9	0xF220_0124	R/W	Specifies the Vector Address 9 Register	0x00000000
VIC2VECTADDR10	0xF220_0128	R/W	Specifies the Vector Address 10 Register	0x00000000
VIC2VECTADDR11	0xF220_012C	R/W	Specifies the Vector Address 11 Register	0x00000000
VIC2VECTADDR12	0xF220_0130	R/W	Specifies the Vector Address 12 Register	0x00000000
VIC2VECTADDR13	0xF220_0134	R/W	Specifies the Vector Address 13 Register	0x00000000
VIC2VECTADDR14	0xF220_0138	R/W	Specifies the Vector Address 14 Register	0x00000000
VIC2VECTADDR15	0xF220_013C	R/W	Specifies the Vector Address 15 Register	0x00000000

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Register	Address	R/W	Description	Reset Value
VIC2VECTADDR16	0xF220_0140	R/W	Specifies the Vector Address 16 Register	0x00000000
VIC2VECTADDR17	0xF220_0144	R/W	Specifies the Vector Address 17 Register	0x00000000
VIC2VECTADDR18	0xF220_0148	R/W	Specifies the Vector Address 18 Register	0x00000000
VIC2VECTADDR19	0xF220_014C	R/W	Specifies the Vector Address 19 Register	0x00000000
VIC2VECTADDR20	0xF220_0150	R/W	Specifies the Vector Address 20 Register	0x00000000
VIC2VECTADDR21	0xF220_0154	R/W	Specifies the Vector Address 21 Register	0x00000000
VIC2VECTADDR22	0xF220_0158	R/W	Specifies the Vector Address 22 Register	0x00000000
VIC2VECTADDR23	0xF220_015C	R/W	Specifies the Vector Address 23 Register	0x00000000
VIC2VECTADDR24	0xF220_0160	R/W	Specifies the Vector Address 24 Register	0x00000000
VIC2VECTADDR25	0xF220_0164	R/W	Specifies the Vector Address 25 Register	0x00000000
VIC2VECTADDR26	0xF220_0168	R/W	Specifies the Vector Address 26 Register	0x00000000
VIC2VECTADDR27	0xF220_016C	R/W	Specifies the Vector Address 27 Register	0x00000000
VIC2VECTADDR28	0xF220_0170	R/W	Specifies the Vector Address 28 Register	0x00000000
VIC2VECTADDR29	0xF220_0174	R/W	Specifies the Vector Address 29 Register	0x00000000
VIC2VECTADDR30	0xF220_0178	R/W	Specifies the Vector Address 30 Register	0x00000000
VIC2VECTADDR31	0xF220_017C	R/W	Specifies the Vector Address 31 Register	0x00000000
VIC2VECPRIORITY0	0xF220_0200	R/W	Specifies the Vector Priority 0 Register	0xF
VIC2VECTPRIORITY1	0xF220_0204	R/W	Specifies the Vector Priority 1 Register	0xF
VIC2VECTPRIORITY2	0xF220_0208	R/W	Specifies the Vector Priority 2 Register	0xF
VIC2VECTPRIORITY3	0xF220_020C	R/W	Specifies the Vector Priority 3 Register	0xF
VIC2VECTPRIORITY4	0xF220_0210	R/W	Specifies the Vector Priority 4 Register	0xF
VIC2VECTPRIORITY5	0xF220_0214	R/W	Specifies the Vector Priority 5 Register	0xF
VIC2VECTPRIORITY6	0xF220_0218	R/W	Specifies the Vector Priority 6 Register	0xF
VIC2VECTPRIORITY7	0xF220_021C	R/W	Specifies the Vector Priority 7 Register	0xF
VIC2VECTPRIORITY8	0xF220_0220	R/W	Specifies the Vector Priority 8 Register	0xF
VIC2VECTPRIORITY9	0xF220_0224	R/W	Specifies the Vector Priority 9 Register	0xF
VIC2VECTPRIORITY10	0xF220_0228	R/W	Specifies the Vector Priority 10 Register	0xF
VIC2VECTPRIORITY11	0xF220_022C	R/W	Specifies the Vector Priority 11 Register	0xF
VIC2VECTPRIORITY12	0xF220_0230	R/W	Specifies the Vector Priority 12 Register	0xF
VIC2VECTPRIORITY13	0xF220_0234	R/W	Specifies the Vector Priority 13 Register	0xF
VIC2VECTPRIORITY14	0xF220_0238	R/W	Specifies the Vector Priority 14 Register	0xF
VIC2VECTPRIORITY15	0xF220_023C	R/W	Specifies the Vector Priority 15 Register	0xF
VIC2VECTPRIORITY16	0xF220_0240	R/W	Specifies the Vector Priority 16 Register	0xF
VIC2VECTPRIORITY17	0xF220_0244	R/W	Specifies the Vector Priority 17 Register	0xF
VIC2VECTPRIORITY18	0xF220_0248	R/W	Specifies the Vector Priority 18 Register	0xF
VIC2VECTPRIORITY19	0xF220_024C	R/W	Specifies the Vector Priority 19 Register	0xF

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Register	Address	R/W	Description	Reset Value
VIC2VECTPRIORITY20	0xF220_0250	R/W	Specifies the Vector Priority 20 Register	0xF
VIC2VECTPRIORITY21	0xF220_0254	R/W	Specifies the Vector Priority 21 Register	0xF
VIC2VECTPRIORITY22	0xF220_0258	R/W	Specifies the Vector Priority 22 Register	0xF
VIC2VECTPRIORITY23	0xF220_025C	R/W	Specifies the Vector Priority 23 Register	0xF
VIC2VECTPRIORITY24	0xF220_0260	R/W	Specifies the Vector Priority 24 Register	0xF
VIC2VECTPRIORITY25	0xF220_0264	R/W	Specifies the Vector Priority 25 Register	0xF
VIC2VECTPRIORITY26	0xF220_0268	R/W	Specifies the Vector Priority 26 Register	0xF
VIC2VECTPRIORITY27	0xF220_026C	R/W	Specifies the Vector Priority 27 Register	0xF
VIC2VECTPRIORITY28	0xF220_0270	R/W	Specifies the Vector Priority 28 Register	0xF
VIC2VECTPRIORITY29	0xF220_0274	R/W	Specifies the Vector Priority 29 Register	0xF
VIC2VECTPRIORITY30	0xF220_0278	R/W	Specifies the Vector Priority 30 Register	0xF
VIC2VECTPRIORITY31	0xF220_027C	R/W	Specifies the Vector Priority 31 Register	0xF
VIC2ADDRESS	0xF220_0F00	R/W	Specifies the Vector Address Register	0x00000000
VIC2PERIPHID0	0xF220_0FE0	R	Specifies the Peripheral Identification Register bit 7:0	0x92
VIC2PERIPHID1	0xF220_0FE4	R	Specifies the Peripheral Identification Register bit 15:9	0x11
VIC2PERIPHID2	0xF220_0FE8	R	Specifies the Peripheral Identification Register bit 23:16	0x04
VIC2PERIPHID3	0xF220_0FEC	R	Specifies the Peripheral Identification Register bit 31:24	0x00
VIC2PCELLID0	0xF220_0FF0	R	Specifies the PrimeCell Identification Register bit 7:0	0x0D
VIC2PCELLID1	0xF220_0FF4	R	Specifies the PrimeCell Identification Register bit 15:9	0xF0
VIC2PCELLID2	0xF220_0FF8	R	Specifies the PrimeCell Identification Register bit 23:16	0x05
VIC2PCELLID3	0xF220_0FFC	R	Specifies the PrimeCell Identification Register bit 31:24	0xB1
VIC3IRQSTATUS	0xF230_0000	R	Specifies the IRQ Status Register	0x00000000
VIC3FIQSTATUS	0xF230_0004	R	Specifies the FIQ Status Register	0x00000000
VIC3RAWINTR	0xF230_0008	R	Specifies the Raw Interrupt Status Register	-
VIC3INTSELECT	0xF230_000C	R/W	Specifies the Interrupt Select Register	0x00000000
VIC3INTENABLE	0xF230_0010	R/W	Specifies the Interrupt Enable Register	0x00000000
VIC3INTENCLEAR	0xF230_0014	W	Specifies the Interrupt Enable Clear Register	-
VIC3SOFTINT	0xF230_0018	R/W	Specifies the Software Interrupt Register	0x00000000
VIC3SOFTINTCLEAR	0xF230_001C	W	Specifies the Software Interrupt Clear Register	-

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Register	Address	R/W	Description	Reset Value
VIC3PROTECTION	0xF230_0020	R/W	Specifies the Protection Enable Register	0x0
VIC3SWPRIORITYMASK	0xF230_0024	R/W	Specifies the Software Priority Mask Register	0xFFFF
VIC3PRIORITYDAISY	0xF230_0028	R/W	Specifies the Vector Priority Register for Daisy Chain	0xF
VIC3VECTADDR0	0xF230_0100	R/W	Specifies the Vector Address 0 Register	0x00000000
VIC3VECTADDR1	0xF230_0104	R/W	Specifies the Vector Address 1 Register	0x00000000
VIC3VECTADDR2	0xF230_0108	R/W	Specifies the Vector Address 2 Register	0x00000000
VIC3VECTADDR3	0xF230_010C	R/W	Specifies the Vector Address 3 Register	0x00000000
VIC3VECTADDR4	0xF230_0110	R/W	Specifies the Vector Address 4 Register	0x00000000
VIC3VECTADDR5	0xF230_0114	R/W	Specifies the Vector Address 5 Register	0x00000000
VIC3VECTADDR6	0xF230_0118	R/W	Specifies the Vector Address 6 Register	0x00000000
VIC3VECTADDR7	0xF230_011C	R/W	Specifies the Vector Address 7 Register	0x00000000
VIC3VECTADDR8	0xF230_0120	R/W	Specifies the Vector Address 8 Register	0x00000000
VIC3VECTADDR9	0xF230_0124	R/W	Specifies the Vector Address 9 Register	0x00000000
VIC3VECTADDR10	0xF230_0128	R/W	Specifies the Vector Address 10 Register	0x00000000
VIC3VECTADDR11	0xF230_012C	R/W	Specifies the Vector Address 11 Register	0x00000000
VIC3VECTADDR12	0xF230_0130	R/W	Specifies the Vector Address 12 Register	0x00000000
VIC3VECTADDR13	0xF230_0134	R/W	Specifies the Vector Address 13 Register	0x00000000
VIC3VECTADDR14	0xF230_0138	R/W	Specifies the Vector Address 14 Register	0x00000000
VIC3VECTADDR15	0xF230_013C	R/W	Specifies the Vector Address 15 Register	0x00000000
VIC3VECTADDR16	0xF230_0140	R/W	Specifies the Vector Address 16 Register	0x00000000
VIC3VECTADDR17	0xF230_0144	R/W	Specifies the Vector Address 17 Register	0x00000000
VIC3VECTADDR18	0xF230_0148	R/W	Specifies the Vector Address 18 Register	0x00000000
VIC3VECTADDR19	0xF230_014C	R/W	Specifies the Vector Address 19 Register	0x00000000
VIC3VECTADDR20	0xF230_0150	R/W	Specifies the Vector Address 20 Register	0x00000000
VIC3VECTADDR21	0xF230_0154	R/W	Specifies the Vector Address 21 Register	0x00000000
VIC3VECTADDR22	0xF230_0158	R/W	Specifies the Vector Address 22 Register	0x00000000
VIC3VECTADDR23	0xF230_015C	R/W	Specifies the Vector Address 23 Register	0x00000000
VIC3VECTADDR24	0xF230_0160	R/W	Specifies the Vector Address 24 Register	0x00000000
VIC3VECTADDR25	0xF230_0164	R/W	Specifies the Vector Address 25 Register	0x00000000
VIC3VECTADDR26	0xF230_0168	R/W	Specifies the Vector Address 26 Register	0x00000000
VIC3VECTADDR27	0xF230_016C	R/W	Specifies the Vector Address 27 Register	0x00000000
VIC3VECTADDR28	0xF230_0170	R/W	Specifies the Vector Address 28 Register	0x00000000
VIC3VECTADDR29	0xF230_0174	R/W	Specifies the Vector Address 29 Register	0x00000000
VIC3VECTADDR30	0xF230_0178	R/W	Specifies the Vector Address 30 Register	0x00000000
VIC3VECTADDR31	0xF230_017C	R/W	Specifies the Vector Address 31 Register	0x00000000

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Register	Address	R/W	Description	Reset Value
VIC3VECPRIORITY0	0xF230_0200	R/W	Specifies the Vector Priority 0 Register	0xF
VIC3VECTPRIORITY1	0xF230_0204	R/W	Specifies the Vector Priority 1 Register	0xF
VIC3VECTPRIORITY2	0xF230_0208	R/W	Specifies the Vector Priority 2 Register	0xF
VIC3VECTPRIORITY3	0xF230_020C	R/W	Specifies the Vector Priority 3 Register	0xF
VIC3VECTPRIORITY4	0xF230_0210	R/W	Specifies the Vector Priority 4 Register	0xF
VIC3VECTPRIORITY5	0xF230_0214	R/W	Specifies the Vector Priority 5 Register	0xF
VIC3VECTPRIORITY6	0xF230_0218	R/W	Specifies the Vector Priority 6 Register	0xF
VIC3VECTPRIORITY7	0xF230_021C	R/W	Specifies the Vector Priority 7 Register	0xF
VIC3VECTPRIORITY8	0xF230_0220	R/W	Specifies the Vector Priority 8 Register	0xF
VIC3VECTPRIORITY9	0xF230_0224	R/W	Specifies the Vector Priority 9 Register	0xF
VIC3VECTPRIORITY10	0xF230_0228	R/W	Specifies the Vector Priority 10 Register	0xF
VIC3VECTPRIORITY11	0xF230_022C	R/W	Specifies the Vector Priority 11 Register	0xF
VIC3VECTPRIORITY12	0xF230_0230	R/W	Specifies the Vector Priority 12 Register	0xF
VIC3VECTPRIORITY13	0xF230_0234	R/W	Specifies the Vector Priority 13 Register	0xF
VIC3VECTPRIORITY14	0xF230_0238	R/W	Specifies the Vector Priority 14 Register	0xF
VIC3VECTPRIORITY15	0xF230_023C	R/W	Specifies the Vector Priority 15 Register	0xF
VIC3VECTPRIORITY16	0xF230_0240	R/W	Specifies the Vector Priority 16 Register	0xF
VIC3VECTPRIORITY17	0xF230_0244	R/W	Specifies the Vector Priority 17 Register	0xF
VIC3VECTPRIORITY18	0xF230_0248	R/W	Specifies the Vector Priority 18 Register	0xF
VIC3VECTPRIORITY19	0xF230_024C	R/W	Specifies the Vector Priority 19 Register	0xF
VIC3VECTPRIORITY20	0xF230_0250	R/W	Specifies the Vector Priority 20 Register	0xF
VIC3VECTPRIORITY21	0xF230_0254	R/W	Specifies the Vector Priority 21 Register	0xF
VIC3VECTPRIORITY22	0xF230_0258	R/W	Specifies the Vector Priority 22 Register	0xF
VIC3VECTPRIORITY23	0xF230_025C	R/W	Specifies the Vector Priority 23 Register	0xF
VIC3VECTPRIORITY24	0xF230_0260	R/W	Specifies the Vector Priority 24 Register	0xF
VIC3VECTPRIORITY25	0xF230_0264	R/W	Specifies the Vector Priority 25 Register	0xF
VIC3VECTPRIORITY26	0xF230_0268	R/W	Specifies the Vector Priority 26 Register	0xF
VIC3VECTPRIORITY27	0xF230_026C	R/W	Specifies the Vector Priority 27 Register	0xF
VIC3VECTPRIORITY28	0xF230_0270	R/W	Specifies the Vector Priority 28 Register	0xF
VIC3VECTPRIORITY29	0xF230_0274	R/W	Specifies the Vector Priority 29 Register	0xF
VIC3VECTPRIORITY30	0xF230_0278	R/W	Specifies the Vector Priority 30 Register	0xF
VIC3VECTPRIORITY31	0xF230_027C	R/W	Specifies the Vector Priority 31 Register	0xF
VIC3ADDRESS	0xF230_0F00	R/W	Specifies the Vector Address Register	0x00000000
VIC3PERIPHID0	0xF230_0FE0	R	Specifies the Peripheral Identification Register bit 7:0	0x92
VIC3PERIPHID1	0xF230_0FE4	R	Specifies the Peripheral Identification Register bit 15:9	0x11

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Register	Address	R/W	Description	Reset Value
VIC3PERIPHID2	0xF230_0FE8	R	Specifies the Peripheral Identification Register bit 23:16	0x04
VIC3PERIPHID3	0xF230_0FEC	R	Specifies the Peripheral Identification Register bit 31:24	0x00
VIC3PCELLID0	0xF230_0FF0	R	Specifies the PrimeCell Identification Register bit 7:0	0x0D
VIC3PCELLID1	0xF230_0FF4	R	Specifies the PrimeCell Identification Register bit 15:9	0xF0
VIC3PCELLID2	0xF230_0FF8	R	Specifies the PrimeCell Identification Register bit 23:16	0x05
VIC3PCELLID3	0xF230_0FFC	R	Specifies the PrimeCell Identification Register bit 31:24	0xB1
TZIC0FIQStatus	0xF280_0000	R	Specifies the FIQ Status Register	0x00000000
TZIC0RawIntr	0xF280_0004	R	Specifies the Raw Interrupt Status Register	-
TZIC0IntSelect	0xF280_0008	R/W	Specifies the Interrupt Select Register	0x00000000
TZIC0FIQEnable	0xF280_000C	R/W	Specifies the FIQ Enable Register	0x00000000
TZIC0FIQENClear	0xF280_0010	W	Specifies the FIQ Enable Clear Register	-
TZIC0FIQBypass	0xF280_0014	R/W	Specifies the FIQ Bypass Register	0x00000000
TZIC0Protection	0xF280_0018	R/W	Specifies the Protection Register	0x00000000
TZIC0Lock	0xF280_001C	W	Specifies the Lock Enable Register	-
TZIC0LockStatus	0xF280_0020	R	Specifies the Lock Status Register	0x00000001
TZIC0PeriphID0	0xF280_0FE0	R	Specifies the Peripheral Identification Registers	0x00000090
TZIC0PeriphID1	0xF280_0FE4	R		0x00000018
TZIC0PeriphID2	0xF280_0FE8	R		0x00000004
TZIC0PeriphID3	0xF280_0FEC	R		0x00000000
TZIC0PCellID0	0xF280_0FF0	R	Specifies the Identification Registers	0x0000000D
TZIC0PCellID1	0xF280_0FF4	R		0x000000F0
TZIC0PCellID2	0xF280_0FF8	R		0x00000005
TZIC0PCellID3	0xF280_0FFC	R		0x000000B1
TZIC1FIQStatus	0xF290_0000	R	Specifies the FIQ Status Register	0x00000000
TZIC1RawIntr	0xF290_0004	R	Specifies the Raw Interrupt Status Register	-
TZIC1IntSelect	0xF290_0008	R/W	Specifies the Interrupt Select Register	0x00000000
TZIC1FIQEnable	0xF290_000C	R/W	Specifies the FIQ Enable Register	0x00000000
TZIC1FIQENClear	0xF290_0010	W	Specifies the FIQ Enable Clear Register	-
TZIC1FIQBypass	0xF290_0014	R/W	Specifies the FIQ Bypass Register	0x00000000
TZIC1Protection	0xF290_0018	R/W	Specifies the Protection Register	0x00000000

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Register	Address	R/W	Description	Reset Value
TZIC1Lock	0xF290_001C	W	Specifies the Lock Enable Register	-
TZIC1LockStatus	0xF290_0020	R	Specifies the Lock Status Register	0x00000001
TZIC1PeriphID0	0xF290_0FE0	R	Specifies the Peripheral Identification Registers	0x00000090
TZIC1PeriphID1	0xF290_0FE4	R		0x00000018
TZIC1PeriphID2	0xF290_0FE8	R		0x00000004
TZIC1PeriphID3	0xF290_0FEC	R		0x00000000
TZIC1PCellID0	0xF290_0FF0	R	Specifies the Identification Registers	0x0000000D
TZIC1PCellID1	0xF290_0FF4	R		0x000000F0
TZIC1PCellID2	0xF290_0FF8	R		0x00000005
TZIC1PCellID3	0xF290_0FFC	R		0x000000B1
TZIC2FIQStatus	0xF2A0_0000	R	Specifies the FIQ Status Register	0x00000000
TZIC2RawIntr	0xF2A0_0004	R	Specifies the Raw Interrupt Status Register	-
TZIC2IntSelect	0xF2A0_0008	R/W	Specifies the Interrupt Select Register	0x00000000
TZIC2FIQEnable	0xF2A0_000C	R/W	Specifies the FIQ Enable Register	0x00000000
TZIC2FIQENClear	0xF2A0_0010	W	Specifies the FIQ Enable Clear Register	-
TZIC2FIQBypass	0xF2A0_0014	R/W	Specifies the FIQ Bypass Register	0x00000000
TZIC2Protection	0xF2A0_0018	R/W	Specifies the Protection Register	0x00000000
TZIC2Lock	0xF2A0_001C	W	Specifies the Lock Enable Register	-
TZIC2LockStatus	0xF2A0_0020	R	Specifies the Lock Status Register	0x00000001
TZIC2PeriphID0	0xF2A0_0FE0	R	Specifies the Peripheral Identification Registers	0x00000090
TZIC2PeriphID1	0xF2A0_0FE4	R		0x00000018
TZIC2PeriphID2	0xF2A0_0FE8	R		0x00000004
TZIC2PeriphID3	0xF2A0_0FEC	R		0x00000000
TZIC2PCellID0	0xF2A0_0FF0	R	Specifies the Identification Registers	0x0000000D
TZIC2PCellID1	0xF2A0_0FF4	R		0x000000F0
TZIC2PCellID2	0xF2A0_0FF8	R		0x00000005
TZIC2PCellID3	0xF2A0_0FFC	R		0x000000B1
TZIC3FIQStatus	0xF2B0_0000	R	Specifies the FIQ Status Register	0x00000000
TZIC3RawIntr	0xF2B0_0004	R	Specifies the Raw Interrupt Status Register	-
TZIC3IntSelect	0xF2B0_0008	R/W	Specifies the Interrupt Select Register	0x00000000
TZIC3FIQEnable	0xF2B0_000C	R/W	Specifies the FIQ Enable Register	0x00000000
TZIC3FIQENClear	0xF2B0_0010	W	Specifies the FIQ Enable Clear Register	-
TZIC3FIQBypass	0xF2B0_0014	R/W	Specifies the FIQ Bypass Register	0x00000000
TZIC3Protection	0xF2B0_0018	R/W	Specifies the Protection Register	0x00000000

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Register	Address	R/W	Description	Reset Value
TZIC3Lock	0xF2B0_001C	W	Specifies the Lock Enable Register	-
TZIC3LockStatus	0xF2B0_0020	R	Specifies the Lock Status Register	0x00000001
TZIC3PeriphID0	0xF2B0_0FE0	R	Specifies the Peripheral Identification Registers	0x00000090
TZIC3PeriphID1	0xF2B0_0FE4	R		0x00000018
TZIC3PeriphID2	0xF2B0_0FE8	R		0x00000004
TZIC3PeriphID3	0xF2B0_0FEC	R		0x00000000
TZIC3PCellID0	0xF2B0_0FF0	R	Specifies the Identification Registers	0x0000000D
TZIC3PCellID1	0xF2B0_0FF4	R		0x000000F0
TZIC3PCellID2	0xF2B0_0FF8	R		0x00000005
TZIC3PCellID3	0xF2B0_0FFC	R		0x000000B1

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1.4.1.1 IRQ Status Register
(VICIRQSTATUS, R, Address=0xF200_0000, 0xF210_0000, 0xF220_0000, 0XF230_0000)

VICIRQSTATUS	Bit	Description	Initial State
IRQStatus	[31:0]	Shows the status of the interrupts after masking by the VICINTENABLE and VICINTSELECT Registers: 0 = Interrupt is inactive 1 = Interrupt is active. There is one bit of the register for each interrupt source.	0x00000000

1.4.1.2 FIQ Status Register
(VICFIQSTATUS, R, Address=0xF200_0004, 0xF210_0004, 0xF220_0004, 0xF230_0004)

VICFIQSTATUS	Bit	Description	Initial State
FIQStatus	[31:0]	Shows the status of the FIQ interrupts after masking by the VICINTENABLE and VICINTSELECT Registers: 0 = Interrupt is inactive 1 = Interrupt is active. There is one bit of the register for each interrupt source.	0x00000000

1.4.1.3 Raw Interrupt Status Register
(VICRAWINTR, R, Address=0xF200_0008, 0xF210_0008, 0xF220_0008, 0xF230_0008)

VICRAWINTR	Bit	Description	Initial State
RawInterrupt	[31:0]	Shows the status of the FIQ interrupts before masking by the VICINTENABLE and VICINTSELECT Registers: 0 = Interrupt is inactive before masking 1 = Interrupt is active before masking Because this register provides a direct view of the raw interrupt inputs, the reset value is unknown. There is one bit of the register for each interrupt source.	-

1.4.1.4 Interrupt Select Register
(VICINTSELECT, R/W, Address=0xF200_000C, 0xF210_000C, 0xF220_000C, 0xF230_000C)

VICINTSELECT	Bit	Description	Initial State
IntSelect	[31:0]	Selects interrupt type for interrupt request: 0 = IRQ interrupt 1 = FIQ interrupt There is one bit of the register for each interrupt source.	0x00000000

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1.4.1.5 Interrupt Enable Register (VICINTENABLE, R/W, Address=0xF200_0010, 0xF210_0010, 0xF220_0010, 0xF230_0010)

VICINTENABLE	Bit	Description	Initial State
IntEnable	[31:0]	Enables the interrupt request lines, which allows the interrupts to reach the processor. Read: 0 = Disables Interrupt 1 = Enables Interrupt Use this register to enable interrupt. The VICINTENCLEAR Register must be used to disable the interrupt enable. Write: 0 = No effect 1 = Enables Interrupt. On reset, all interrupts are disabled. There is one bit of the register for each interrupt source.	0x00000000

1.4.1.6 Interrupt Enable Clear (VICINTENCLEAR, W, Address=0xF200_0014, 0xF210_0014, 0xF220_0014, 0xF230_0014)

VICINTENCLEAR	Bit	Description	Initial State
IntEnable Clear	[31:0]	Clears corresponding bits in the VICINTENABLE Register: 0 = No effect 1 = Disables Interrupt in VICINTENABLE Register. There is one bit of the register for each interrupt source.	-

1.4.1.7 Software Interrupt Register (VICSOFTINT, R/W, Address=0xF200_0018, 0xF210_0018, 0xF220_0018, 0xF230_0018)

VICSOFTINT	Bit	Description	Initial State
SoftInt	[31:0]	Setting a bit HIGH generates a software interrupt for the selected source before interrupt masking. Read: 0 = Software interrupt inactive 1 = Software interrupt active Write: 0 = No effect 1 = Enables Software interrupt There is one bit of the register for each interrupt source.	0x00000000

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1.4.1.8 Software Interrupt Clear Register (VICSOFTINTCLEAR, W, Address=0xF200_001C, 0xF210_001C, 0xF220_001C, 0xF230_001C)

VICSOFTINTCLEAR	Bit	Description	Initial State
SoftIntClear	[31:0]	Clears corresponding bits in the VICSOFTINT Register: 0 = No effect 1 = Disables Software interrupt in the VICSOFTINT Register. There is one bit of the register for each interrupt source.	-

1.4.1.9 Protection Enable Register (VICPROTECTION, R/W, Address=0xF200_0020, 0xF210_0020, 0xF220_0020, 0xF230_0020)

VICPROTECTION	Bit	Description	Initial State
Reserved	[31:1]	Reserved, read as 0, do not modify.	0x0
Protection	[0]	Enables or disables protected register access: 0 = Disables Protection mode 1 = Enables Protection mode. If enabled, only privileged mode accesses (reads and writes) can access the interrupt controller registers, that is, if HPROT[1] is set HIGH for the current transfer. If disabled, both user mode and privileged mode can access the registers. This register can only be accessed in privileged mode, even if protection mode is disabled.	0x0

1.4.1.10 Vector Address Register (VICADDRESS, R/W, Address=0xF200_0F00, 0xF210_0F00, 0xF220_0F00, 0xF230_0F00)

VICADDRESS	Bit	Description	Initial State
VectAddr	[31:0]	Contains the address of the currently active ISR, with reset value 0x00000000. A read of this register returns the address of the ISR and sets the current interrupt as being serviced. A read must be performed while there is an active interrupt. A write of any value to this register clears the current interrupt. A write must only be performed at the end of an interrupt service routine.	0x00000000

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1.4.1.11 Software Priority Mask Register (VICSWPRIORITYMASK, R/W, Address=0xF200_0024, 0xF210_0024, 0xF220_0024, 0xF230_0024)

VICSWPRIORITYMASK	Bit	Description	Initial State
Reserved	[31:16]	Reserved, read as 0, do not modify	0x0
SWPriorityMask	[15:0]	Controls software masking of the 16 interrupt priority levels: 0 = Interrupt priority level is masked 1 = Interrupt priority level is not masked Each bit of the register is applied to each of the 16 interrupt priority levels.	0xFFFF

1.4.1.12 Vector Address Registers (VICVECTADDR[0-31], R/W, Address=0xF200_0100~017C, 0xF210_0100~017C, 0xF220_0100~017C, 0xF230_0100~017C)

VICVECTADDR[0-31]	Bit	Description	Initial State
VectorAddr 0-31	[31:0]	Contains ISR vector addresses.	0x00000000

1.4.1.13 Vector Priority Registers (VICVECTPRIORITY[0-31] and VICVECTPRIORITYDAISY, R/W, Address=0xF200_0200~027C, 0xF210_0200~027C, 0xF220_0200~027C, 0xF230_0200~027C)

VICVECTPRIORITY[0-31] and VICVECTPRIORITYDAISY	Bit	Description	Initial State
Reserved	[31:4]	Reserved, read as 0, do not modify.	0x0
VectPriority	[3:0]	Selects vectored interrupt priority level. You can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0-15.	0xF

1.4.1.14 VICPERIPHID0 Register (VICPERIPHID0, R, Address=0xF200_0FE0, 0xF210_0FE0, 0xF220_0FE0, 0xF230_0FE0)

VICPERIPHID0	Bit	Description	Initial State
-	[31:8]	Reserved, read as 0, do not modify.	0x0
Partnumber0	[7:0]	These bits read back as 0x92	0x92

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1.4.1.15 VICPERIPHID1 Register (VICPERIPHID1, R, Address=0xF200_0FE4, 0xF210_0FE4, 0xF220_0FE4, 0xF230_0FE4)

VICPERIPHID1	Bit	Description	Initial State
-	[31:8]	Reserved, read as 0, do not modify.	0x0
Designer0	[7:4]	These bits read back as 0x1.	0x1
Partnumber1	[3:0]	These bits read back as 0x1.	0x1

1.4.1.16 VICPERIPHID2 Register (VICPERIPHID2, R, Address=0xF200_0FE8, 0xF210_0FE8, 0xF220_0FE8, 0xF230_0FE8)

VICPERIPHID2	Bit	Description	Initial State
-	[31:8]	Reserved, read as 0, do not modify.	0x0
Revision	[7:4]	These bits read back as the revision number, which can be between 0 and 15.	0x0
Designer1	[3:0]	These bits read back as 0x4.	0x4

1.4.1.17 VICPERIPHID3 Register (VICPERIPHID3, R, Address=0xF200_0FEC, 0xF210_0FEC, 0xF220_0FEC, 0xF230_0FEC)

VICPERIPHID3	Bit	Description	Initial State
-	[31:8]	Reserved, read as 0, do not modify.	0x0
Configuration	[7:2]	These bits read back as 0x0.	0x0
Configuration	[1:0]	Indicates the number of interrupts supported: 00 = 32 (default) 01 = 64 10 = 128 11 = 256	0x0

1.4.1.18 VICPCELLID0 Register (VICPCELLID0, R, Address=0xF200_0FF0, 0xF210_0FF0, 0xF220_0FF0, 0xF230_0FF0)

VICPCELLID0	Bit	Description	Initial State
-	[31:8]	Reserved, read as 0, do not modify.	0x0
VICPCellID0	[7:0]	These bits read back as 0x0D.	0x0D

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1.4.1.19 VICPCELLID1 Register (VICPCELLID1, R, Address=0xF200_0FF4, 0xF210_0FF4, 0xF220_0FF4, 0xF230_0FF4)

VICPCELLID1	Bit	Description	Initial State
-	[31:8]	Reserved, read as 0, do not modify.	0x0
VICPCellID1	[7:0]	These bits read back as 0xF0.	0xF0

1.4.1.20 VICPCELLID2 Register (VICPCELLID2, R, Address=0xF200_0FF8, 0xF210_0FF8, 0xF220_0FF8, 0xF230_0FF8)

VICPCELLID2	Bit	Description	Initial State
-	[31:8]	Reserved, read as 0, do not modify.	0x0
VICPCellID2	[7:0]	These bits read back as 0x05.	0x05

1.4.1.21 VICPCELLID3 Register (VICPCELLID3, R, Address=0xF200_0FFC, 0xF210_0FFC, 0xF220_0FFC, 0xF230_0FFC)

VICPCELLID3	Bit	Description	Initial State
-	[31:8]	Reserved, read as 0, do not modify.	0x0
VICPCellID3	[7:0]	These bits read back as 0xB1.	0xB1

1.4.1.22 FIQ Status Register (TZICFIQStatus, R, Address=0xF280_0000, 0xF290_0000, 0xF2A0_0000, 0xF2B0_0000)

TZICFIQStatus	Bit	Description	Initial State
FIQStatus	[31:0]	Shows the status of the interrupts after masking by the TZICFIQIntEnable and TZICFIQIntEnClear Registers. A HIGH bit indicates that the interrupt is active, and generates an nFIQ interrupt to the processor.	0x00000000

1.4.1.23 Raw Interrupt Status Register (TZICRawIntr, R, Address=0xF280_0004, 0xF290_0004, 0xF2A0_0004, 0xF2B0_0004)

TZICRawIntr	Bit	Description	Initial State
RawIntr	[31:0]	Shows the status of the interrupts before masking by the TZICFIQIntEnable and TZICFIQIntEnClear Registers. A HIGH bit indicates that the interrupt is active before masking.	-

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1.4.1.24 Interrupt select register
(TZICIntSelect, R/W, Address=0xF280_0008, 0xF290_0008, 0xF2A0_0008, 0xF2B0_0008)

TZICRawIntr	Bit	Description	Initial State
IntSelect	[31:0]	Selects whether the interrupt source generates an FIQ interrupt or passes straight through to TZICIRQOUT. 0 = Interrupt passes through to TZICIRQOUT 1 = Interrupt is available for FIQ generation	0x00000000

1.4.1.25 FIQ Enable Register
(TZICFIQEnable, R/W, Address=0xF280_000C, 0xF290_000C, 0xF2A0_000C, 0xF2B0_000C)

TZICFIQEnable	Bit	Description	Initial State
FIQEnable	[31:0]	Enables the FIQ-selected interrupt lines, allowing the interrupts to reach the processor. Read: 0 = Disables Interrupt 1 = Enables Interrupt. To enable the interrupt use this register. You must use the TZICFIQEnClear Register to disable the interrupt enable. Write: 0 = No effect 1 = Enables Interrupt. If Reset it disables all interrupts. There is 1 bit of the register for each interrupt source.	0x00000000

1.4.1.26 FIQ Enable Clear Register
(TZICFIQENClear, W, Address=0xF280_0010, 0xF290_0010, 0xF2A0_0010, 0xF2B0_0010)

TZICFIQENClear	Bit	Description	Initial State
FIQEnClear	[31:0]	Clears bits in the TZICFIQEnable Register. Writing a HIGH clears the corresponding bit in the TZICFIQEnable Register. Writing a LOW has no effect.	-

1.4.1.27 FIQ Bypass Register
(TZICFIQBypass, R/W, Address=0xF280_0014, 0xF290_0014, 0xF2A0_0014, 0xF2B0_0014)

TZICFIQBypass	Bit	Description	Initial State
-	[31:1]	Read undefined. Write as 0.	0x0
FIQBypass	[0]	Enables nNSFIQIN to route directly to nFIQ. 0 = No Bypass 1 = Bypass.	0x0

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1.4.1.28 Protection Register (TZICProtection, R/W, Address=0xF280_0018, 0xF290_0018, 0xF2A0_0018, 0xF2B0_0018)

TZICProtection	Bit	Description	Initial State
-	[31:1]	Read undefined. Write as 0.	0x0
Protection	[0]	Enables or disables protected register access: 0 = Disables Protection mode 1 = Enables Protection mode. If enabled, you can only make privileged mode access (reads and writes) to the TZIC. This register is accessed in privileged mode, even if protection mode is disabled.	0x0

1.4.1.29 Lock Enable Register (TZICLock, W, Address=0xF280_001C, 0xF290_001C, 0xF2A0_001C, 0xF2B0_001C)

TZICLock	Bit	Description	Initial State
Lock	[31:0]	To enable access to the other registers in the TZIC, you must write the correct access code of 0x0ACCE550 to this register. To disable access to the other TZIC registers, you must write any other value except 0x0ACCE550 to this register.	-

1.4.1.30 Lock Status Register (TZICLockStatus, R, Address=0xF280_0020, 0xF290_0020, 0xF2A0_0020, 0xF2B0_0020)

TZICLockStatus	Bit	Description	Initial State
-	[31:1]	Read undefined.	0x0
Locked	[0]	Shows the locked status of the TZIC: 0 = Access to the TZIC is not locked 1 = Access to the TZIC is locked Use TZICLock Register to unlock the access	0x1

1.4.1.31 Peripheral Identification Register (TZICPeriphID0, R, Address=0xF280_0FE0, 0xF290_0FE0, 0xF2A0_0FE0, 0xF2B0_0FE0)

TZICPeriphID0	Bit	Description	Initial State
-	[31:8]	Read undefined	0x0
Partnumber0	[7:0]	These bits read back as 0x90	0x90

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1.4.1.32 Peripheral Identification Register (TZICPeriphID1, R, Address=0xF280_0FE4, 0xF290_0FE4, 0xF2A0_0FE4, 0xF2B0_0FE4)

TZICPeriphID1	Bit	Description	Initial State
-	[31:8]	Read undefined	0x0
Designer0	[7:4]	These bits read back as 0x1	0x1
Partnumber1	[3:0]	These bits read back as 0x8	0x8

1.4.1.33 Peripheral Identification Register (TZICPeriphID2, R, Address=0xF280_0FE8, 0xF290_0FE8, 0xF2A0_0FE8, 0xF2B0_0FE8)

TZICPeriphID2	Bit	Description	Initial State
-	[31:8]	Read undefined	0x0
Revision	[7:4]	These bits read back as the revision number and can be between 0 and 15	0x0
Designer1	[3:0]	These bits read back as 0x4	0x4

1.4.1.34 Peripheral Identification Register (TZICPeriphID3, R, Address=0xF280_0FEC, 0xF290_0FEC, 0xF2A0_0FEC, 0xF2B0_0FEC)

TZICPeriphID3	Bit	Description	Initial State
-	[31:8]	Read undefined	0x0
Configuration	[7:0]	These bits read back as 0x00	0x0

1.4.1.35 Identification Register (TZICPCellID0, R, Address=0xF280_0FF0, 0xF290_0FF0, 0xF2A0_0FF0, 0xF2B0_0FF0)

TZICPCellID0	Bit	Description	Initial State
-	[31:8]	Read undefined	0x0
TZICPCellID0	[7:0]	These bits read back as 0x0D	0x0D

1.4.1.36 Identification Register (TZICPCellID1, R, Address=0xF280_0FF4, 0xF290_0FF4, 0xF2A0_0FF4, 0xF2B0_0FF4)

TZICPCellID1	Bit	Description	Initial State
-	[31:8]	Read undefined	0x0
TZICPCellID1	[7:0]	These bits read back as 0xF0	0xF0

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1.4.1.37 Identification Register (TZICPCellID2, R, Address=0xF280_0FF8, 0xF290_0FF8, 0xF2A0_0FF8, 0xF2B0_0FF8)

TZICPCellID2	Bit	Description	Initial State
-	[31:8]	Read undefined	0x0
TZICPCellID2	[7:0]	These bits read back as 0x05	0x05

1.4.1.38 Identification Register (TZICPCellID3 Register, R, Address=0xF280_0FFC, 0xF290_0FFC, 0xF2A0_0FFC, 0xF2B0_0FFC)

TZICPCellID3	Bit	Description	Initial State
-	[31:8]	Read undefined	0x0
TZICPCellID3	[7:0]	These bits read back as 0xB1	0xB1

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Section 5

MEMORY

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1 DRAM CONTROLLER

1.1 OVERVIEW OF DRAM CONTROLLER

1.1.1 INTRODUCTION OF DRAM CONTROLLER

The DRAM controller is an Advanced Microcontroller Bus Architecture (AMBA^{tm}) AXI compliant slave to interface external JEDEC DDR-type SDRAM devices.

To support high-speed memory devices, the DRAM controller uses a SEC DDR PHY interface. The controller includes an advanced embedded scheduler to utilize memory device efficiently and an optimized pipeline stage to minimize latency. S5PV210 has two independent DRAM Controllers and Ports, namely, DMC0 and DMC1. DMC0 support maximum 512MByte and DMC1 1GByte memory size but both controllers must use the memory of the same type.

1.1.2 KEY FEATURES OF DRAM CONTROLLER

- Compatible with JEDEC DDR2, low power DDR and low power DDR2 SDRAM specification
- Uses the SEC LPDDR2 PHY interface to support high-speed memory devices
- Supports up to two external chip selects and 1/2/4/8 banks per one chip
- Supports 128 Mb, 256 Mb, 512 Mb, 1 Gb, 2 Gb and 4 Gb density Memory Devices
- Supports 16/ 32-bit wide memory data width
- Optimized pipeline stage for low latency
- Supports QoS scheme to ensure low latency for some applications
- Advanced embedded scheduler enables out-of order operations to utilize memory device efficiently
- Supports excellent chip/bank interleaving and memory interrupting
- Supports AMBA AXI low power channel for systematic power control
- Adapts to various low power schemes to reduce the dynamic and static current of memory
- Supports outstanding exclusive accesses
- Supports bank selective precharge policy

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1.1.3 SUPPORTS CLOCK FREQUENCY UP TO 200MHZ BLOCK DIAGRAM

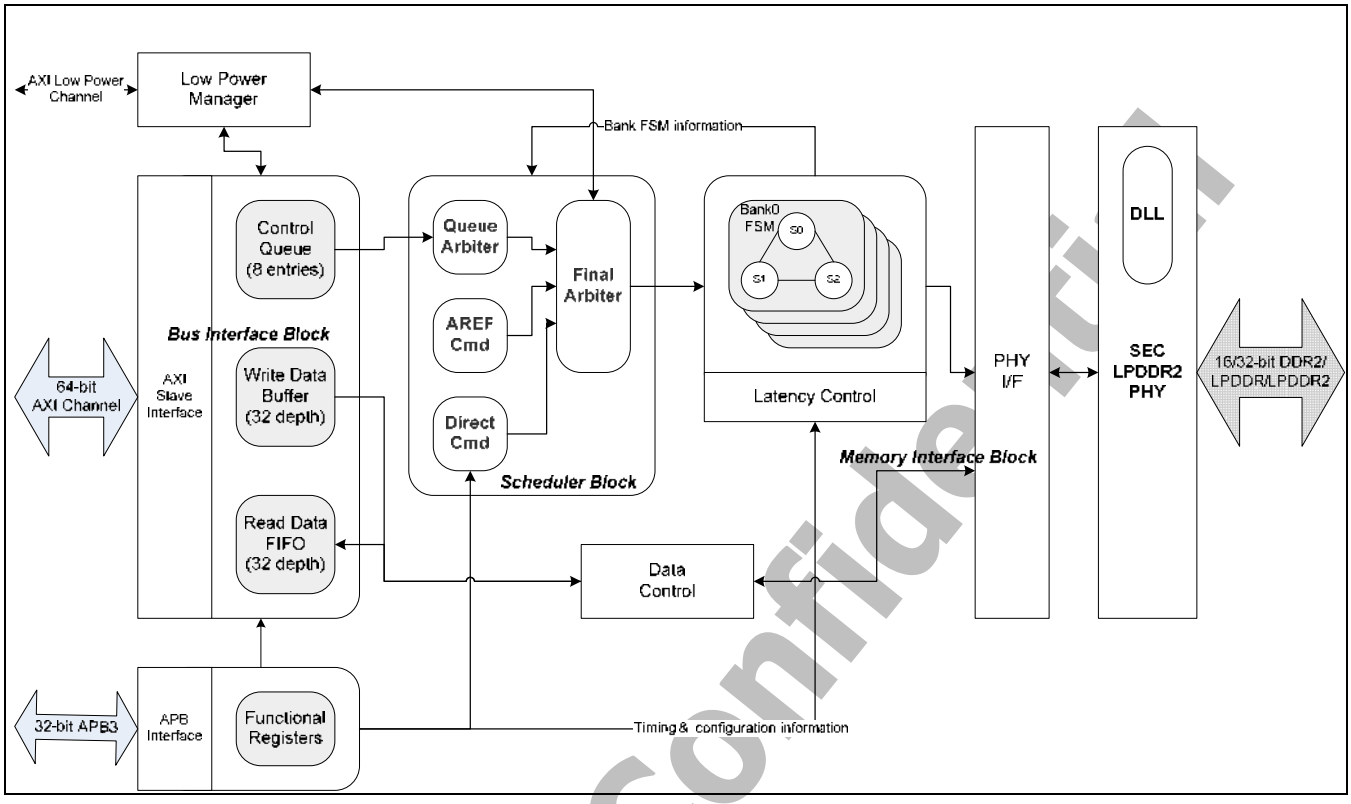

Figure 1-1 Overall Block Diagram

Figure 1-1 shows the overall block diagram of the controller. The block diagram shows the bus interface block, scheduler block, and memory interface block, which connects and interfaces with the SEC LPDDR2 PHY.

The bus interface block saves the bus transactions for memory access that come from the AXI slave port to the command queue. Additionally it saves the write data to the write buffer or sends the read data to the Master via the AXI bus. It also acts as a read FIFO if AXI Master is not ready and has an APB interface for special function registers/ direct commands and an AXI low power channel interface.

The Scheduler block uses the memory bank Finite State Machine (FSM) information to arbitrate the bus transactions in the command queues and transforms the commands into a memory command type, which is sent to the Memory interface block. It also controls the write and read data flow between the memory and the AXI bus.

The Memory interface block updates each memory bank state according to the memory command coming from the scheduler and sends the bank state back to the scheduler. It creates a memory command depending on the memory latency and sends the command to the SEC LPDDR2 PHY via the PHY interface.

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1.2 FUNCTIONAL DESCRIPTION

1.2.1 INITIALIZATION

An Initialization procedure consists of PHY DLL initialization, setting controller register and memory initialization. For memory initialization, refer to JEDEC specifications and data sheets of memory devices. There are three different memory types, namely, LPDDR, LPDDR2, and DDR2. According to the memory types, initialization sequences are as follows.

1.2.1.1 LPDDR

Initialization sequence for LPDDR memory type:

1. To provide stable power for controller and memory device, the controller must assert and hold CKE to a logic high level. Then apply stable clock. **Note:** XDDR2SEL should be Low level to hold CKE to high.
2. Set the **PhyControl0.ctrl_start_point** and **PhyControl0.ctrl_inc** bit-fields to correct value according to clock frequency. Set the PhyControl0.ctrl_dll_on bit-field to '1' to activate the PHY DLL.
3. DQS Cleaning: Set the **PhyControl1.ctrl_shiftc** and **PhyControl1.ctrl_offsetc** bit-fields to the correct value according to clock frequency and memory tAC parameters.
4. Set the **PhyControl0.ctrl_start** bit-field to '1'.
5. Set the **ConControl**. At this moment, an auto refresh counter should be off.
6. Set the **MemControl**. At this moment, all power down modes should be off.
7. Set the **MemConfig0** register. If there are two external memory chips, also set the **MemConfig1** register.
8. Set the **PrechConfig** and **PwrdnConfig** registers.
9. Set the **TimingAref**, **TimingRow, TimingData and TimingPower** registers according to memory AC parameters.
10. If QoS scheme is required, set the **QosControl0~15** and **QosConfig0~15** registers.
11 Wait for the PhyStatus0.ctrl_locked bit-fields to change to '1'. Check whether PHY DLL is locked.
12. PHY DLL compensates the changes of delay amount caused by Process, Voltage and Temperature (PVT) variation during memory operation. Therefore, it should not be off for reliable operation. PHY DLL can be off if frequency is low. If off mode is used, set the **PhyControl0.ctrl_force** bit-field to the correct value according to the **PhyStatus0.ctrl_lock_value[9:2]** bit-field for fix delay amount. Clear the **PhyControl0.ctrl_dll_on** bit-field to turn off PHY DLL.
13. Confirm whether stable clock issues minimum 200us after power on
14. Issue a **PALL** command using the **DirectCmd** register.
15. Issue two **Auto Refresh** commands using the **DirectCmd** register.
16. Issue a **MRS** command using the **DirectCmd** register to program the operating parameters.

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17. Issue an **EMRS** command using the **DirectCmd** register to program the operating parameters.
18. If there are two external memory chips, perform steps 14~17 for chip1 memory device.
19. Set the **ConControl to turn on an auto refresh counter**.
20. If power down modes is required, set the **MemControl** registers.

1.2.1.2 LPDDR2

Initialization sequence for LPDDR2 memory type:

1. To provide stable power for controller and memory device, the controller must assert and hold CKE to a logic low level. Then apply stable clock. **Note:** XDDR2SEL should be High level to hold CKE to low.
2. Set the **PhyControl0.ctrl_start_point** and **PhyControl0.ctrl_inc** bit-fields to correct value according to clock frequency. Set the **PhyControl0.ctrl_dll_on** bit-field to '1' to activate the PHY DLL.
3. DQS Cleaning: Set the **PhyControl1.ctrl_shiftc** and **PhyControl1.ctrl_offsetc** bit-fields to correct value according to clock frequency and memory tAC parameters.
4. Set the **PhyControl0.ctrl_start** bit-field to '1'.
5. Set the **ConControl**. At this moment, an auto refresh counter should be off.
6. Set the **MemControl**. At this moment, all power down modes should be off.
7. Set the **MemConfig0** register. If there are two external memory chips, set the **MemConfig1** register.
8. Set the **PrechConfig** and **PwrdnConfig** registers.
9. Set the **TimingAref**, **TimingRow**, **TimingData** and **TimingPower** registers according to memory AC parameters.
10. If QoS scheme is required, set **the QosControl0~15** and **QosConfig0~15** registers.
11. Wait for **the PhyStatus0.ctrl_locked** bit-fields to change to '1'. Check whether PHY DLL is locked.
12. PHY DLL compensates the changes of delay amount caused by Process, Voltage and Temperature (PVT) variation during memory operation. Therefore, PHY DLL should not be off for reliable operation. It can be off except runs at low frequency. If off mode is used, set the **PhyControl0.ctrl_force** bit-field to correct value according to the **PhyStatus0.ctrl_lock_value[9:2]** bit-field to fix delay amount. Clear the **PhyControl0.ctrl_dll_on** bit-field to turn off PHY DLL.
13. Set the **PhyControl1.fp_resync** bit-field to '1' to update DLL information.
14. Confirm that CKE still maintains a logic low level at minimum 100ns after power on.
15. Issue a **NOP** command using the **DirectCmd** register to assert and to hold CKE to a logic high level.
16. Wait for at least 200us.

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17. Issue a **MRS** command using the **DirectCmd** register to reset memory device and program the operating parameters.
18. Wait for minimum 1us.
19. Issue a **MRR** command using the **DirectCmd** register to poll the DAI bit of the **MRStatus** register to know whether Device Auto-Initialization is completed or not.
20. If there are two external memory chips, perform steps 15 ~ 19 for chip1 memory device.
21. Set the **ConControl** to turn on an auto refresh counter.
22. If power down modes is required, set the **MemControl** registers.

1.2.1.3 DDR2

Initialization sequence for DDR2 memory type:

1. To provide stable power for controller and memory device, the controller must assert and hold CKE to a logic low level. Then apply stable clock. **Note**: XDDR2SEL should be High level to hold CKE to low.
2. Set the **PhyControl0.ctrl_start_point** and **PhyControl0.ctrl_inc** bit-fields to correct value according to clock frequency. Set the **PhyControl0.ctrl_dll_on** bit-field to '1' to turn on the PHY DLL.
3. DQS Cleaning: Set the **PhyControl1.ctrl_shiftc** and **PhyControl1.ctrl_offsetc** bit-fields to correct value according to clock frequency and memory tAC parameters.
4. Set the **PhyControl0.ctrl_start** bit-field to '1'.
5. Set the **ConControl**. At this moment, an auto refresh counter should be off.
6. Set the **MemControl**. At this moment, all power down modes should be off.
7. Set the **MemConfig0** register. If there are two external memory chips, set the MemConfig1 register.
8. Set the **PrechConfig** and **PwrdnConfig** registers.
9. Set the **TimingAref**, **TimingRow**, **TimingData** and **TimingPower** registers according to memory AC parameters.
10. If QoS scheme is required, set the **QosControl0~15** and **QosConfig0~15** registers.
11. Wait for the **PhyStatus0.ctrl_locked** bit-fields to change to '1'. Check whether PHY DLL is locked.
12. PHY DLL compensates the changes of delay amount caused by Process, Voltage and Temperature (PVT) variation during memory operation. Therefore, PHY DLL should not be off for reliable operation. It can be off except runs at low frequency. If off mode is used, set the **PhyControl0.ctrl_force** bit-field to correct value according to the **PhyStatus0.ctrl_lock_value[9:2]** bit-field to fix delay amount. Clear the **PhyControl0.ctrl_dll_on** bit-field to turn off PHY DLL.
13. Confirm whether stable clock is issued minimum 200us after power on
14. Issue a **NOP** command using the **DirectCmd** register to assert and to hold CKE to a logic high level.

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15. Wait for minimum 400ns.
16. Issue a **PALL** command using the **DirectCmd** register.
17. Issue an **EMRS2** command using the **DirectCmd** register to program the operating parameters.
18. Issue an **EMRS3** command using the **DirectCmd** register to program the operating parameters.
19. Issue an **EMRS** command using the **DirectCmd** register to enable the memory DLLs.
20. Issue a **MRS** command using the **DirectCmd** register to reset the memory DLL.
21. Issue a **PALL** command using the **DirectCmd** register.
22. Issue two **Auto Refresh** commands using the **DirectCmd** register.
23. Issue a **MRS** command using the **DirectCmd** register to program the operating parameters without resetting the memory DLL.
24. Wait for minimum 200 clock cycles.
25. Issue an **EMRS** command using the **DirectCmd** register to program the operating parameters. If OCD calibration is not used, issue an **EMRS** command to set OCD Calibration Default. After that, issue an **EMRS** command to exit OCD Calibration Mode and to program the operating parameters.
26. If there are two external memory chips, perform steps 14~25 for chip1 memory device.
27. Set the **ConControl** to turn on an auto refresh counter. 28. If power down modes is required, set the **MemControl** registers.

1.2.2 ADDRESS MAPPING

The controller modifies the address of the bus transaction coming from the AXI slave port into a memory address - chip select, bank address, row address, column address and memory data width.

To map chip select0 of the memory device to a specific area of the address map, the **chip_base** and **chip_mask** bit-fields of the **MemConfig0** register must be set (Refer to Register Descriptions). If chip1 of the memory device exists, the **MemConfig1** register must also be set.

Then, the AXI address requested by the AXI Master is divided into AXI base address and AXI offset address. The AXI base address activates the appropriate memory chip select and the AXI offset address is mapped to a memory address according to the bank, row, column number, and data width set by the **MemConfig** register.

There are two ways to map the AXI offset address as shown in *Figure 1-2* Linear mapping and Interleaved mapping.

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1.2.2.1 Linear Mapping

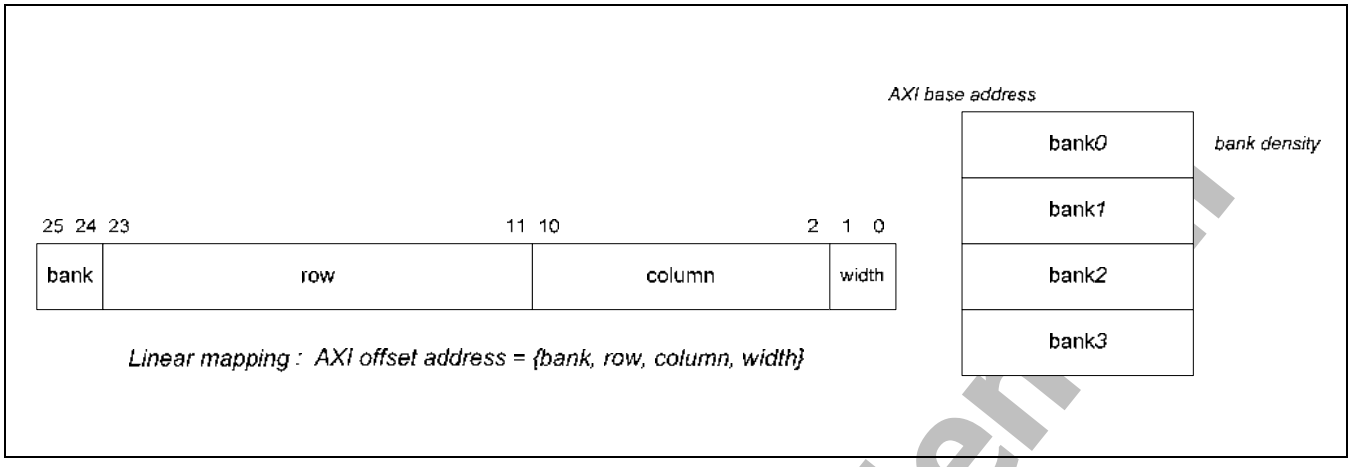

Figure 1-2 Linear Address Mapping

As shown in *Figure 1-2*, the linear mapping method maps the AXI address in the order of bank, row, column and width. Since the bank address does not change for at least one bank size, applications that use linear address mapping have a high possibility to access the same bank.

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1.2.2.2 Interleaved Mapping

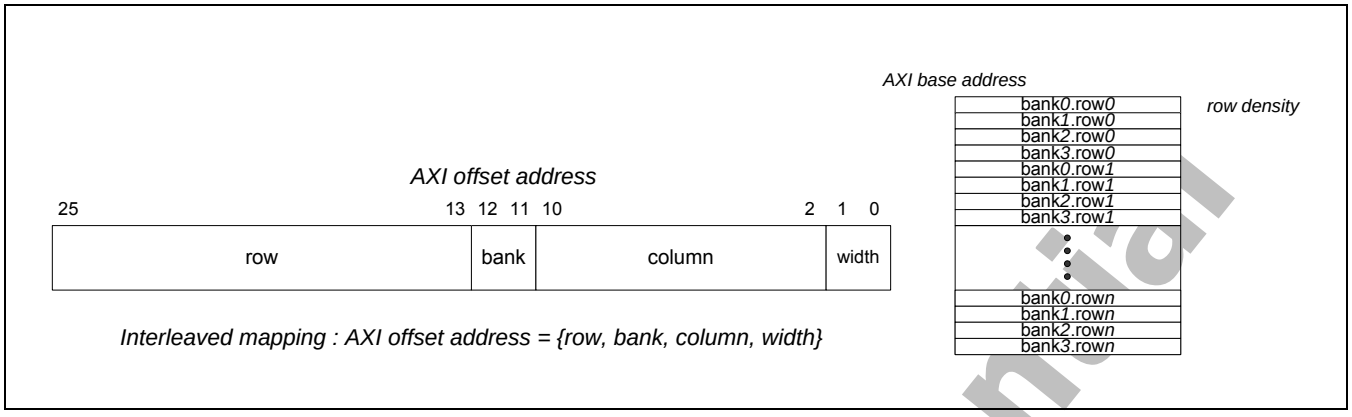

Figure 1-3 Interleaved Address Mapping

As shown in *Figure 1-3*, the interleaved mapping method maps the AXI address in the order of row, bank, column and width. The difference between the linear mapping method and the interleaved method is that the bank and row order is different. For accesses beyond a row size, interleaved mapping accesses a different bank. Therefore, applications that use interleaved mapping access numerous banks. This improves the performance but increases power consumption.

1.2.3 LOW POWER OPERATION

The DRAM controller executes a low power memory operation in five ways, namely:

- AXI Low power channel
- Dynamic power down
- Dynamic self-refresh
- Clock stop
- Direct command
- Each feature is independent of each other and executed at the same time.

1.2.3.1 AXI Low Power Channel

The controller has an AXI low power channel interface to communicate with low power management units such as the system controller, which makes the memory device go into self-refresh mode. To request through the AXI low power channel, refer the **chip1_empty** and **chip0_empty** bit-fields of **ConControl** register to check if the command queue is currently empty.

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1.2.3.2 Dynamic Power Down

The SDRAM device has an active/ precharge power down mode. This mode is entered if CKE becomes LOW. To enter active power down mode minimum one row of a bank must be open. To enter precharge power down mode CKE must be low.

If no AXI transaction enters the controller and the command queue becomes empty for a specific number of cycles (**PwrdnConfig.dpwrdn_cyc** bit-field), the controller changes the memory device's state to active/ precharge power down automatically. Then, there are two ways to enter the active/ precharge power down state and it is selected by **MEMCONTROL.dpwrdn_type** bit.

1. Active/ precharge power down mode: Enter power down without considering whether there is a row open or not,

2. Force precharge power down mode: Enter power down after closing all banks.

If a new AXI transaction enters the controller, the controller automatically wakes up the memory device from power down state and executes in a normal operation state.

1.2.3.3 Dynamic Self Refresh

Similar to the dynamic power down feature (Refer to Section 2.3.2 Dynamic Power Down), if the command queue is empty for a specific amount of cycles (**PwrdnConfig.dsref_cyc** bit-field), the memory device enters self-refresh mode. Since exiting power down mode requires many cycles, we recommend to choose a greater cycle size for dynamic self-refresh entry than dynamic power down.

1.2.3.4 Clock Stop

To reduce the I/O power of the memory device and the controller, it is possible to stop the clock if the LPDDR / LPDDR2 is in idle mode, or self refresh mode and DDR2 is in self refresh mode. If this feature is enabled, the controller automatically executes the clock stop feature.

1.2.3.5 Direct Command

Use the direct command feature to send a command to the memory device through the APB3 port. This way, you force the memory device to enter active/ precharge power down, self-refresh or deep power down mode.

1.2.4 PRECHARGE POLICY

There are two ways for the controller to decide precharge policy, namely:

- Bank selective precharge policy
- Timeout precharge

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1.2.4.1 Bank Selective Precharge Policy

Since applications include different page policy preferences, it is hard for the engineer to decide whether to use open page policy, or close page (auto precharge) policy. Instead of applying the page policy to entire banks, the bank selective precharge policy allows the user to choose a precharge policy for each bank (Refer to **PrechConfig.chip1_policy**). You can assign certain applications to a bank that uses an open page policy, and other applications to a bank that uses a close page (auto precharge) policy.

Open Page Policy: After a READ or WRITE, the accessed row is left open.

Close Page (Auto Precharge) Policy: Right after a READ or WRITE command, the controller issues an auto precharge to the bank.

1.2.4.2 Timeout Precharge

If a certain bank uses an open page policy, the row is left open after a data access. If this happens and the bank that is left open is not scheduled for a specific number of cycles (**PrechConfig.tp_cnt** bit-field) the controller automatically issues a precharge command to close the bank.

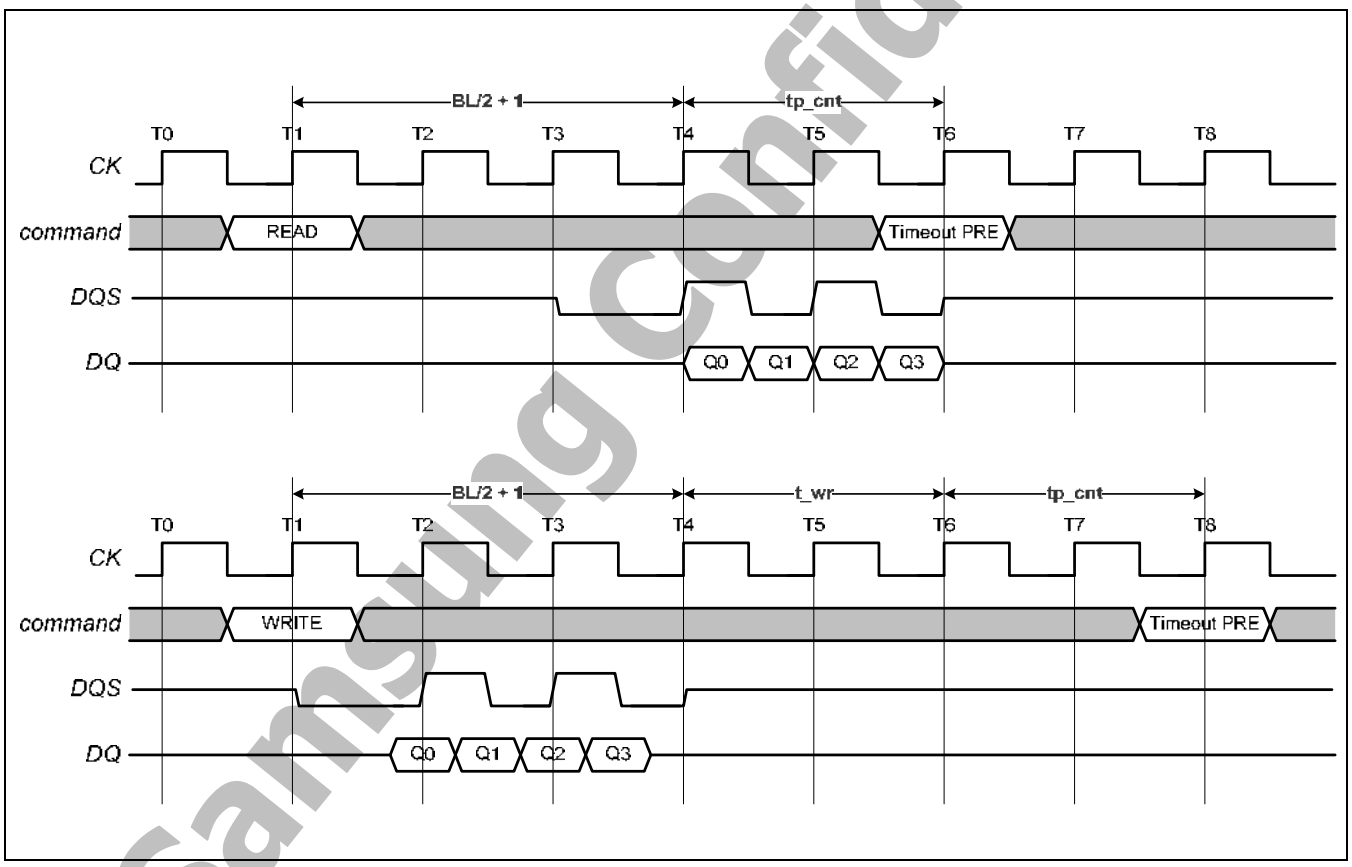

Figure 1-4 Timing Diagram of Timeout Precharge

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1.2.5 QUALITY OF SERVICE

The Quality of Service (QoS) is defined for the controller to increase the arbitration priority of a master that requires low latency read data. The QoS is determined if the control queue (Refer to Figure 1-1*Figure 1-1*) receives the command through the AXI bus and the QoS count starts depreciating at this moment. If the count reaches zero, this command becomes the highest priority among the other commands that are in the control queue.

There are three types of QoS, namely:

- qos_cnt
- qos_cnt_f
- default_qos

1.2.5.1 qos_cnt

There are 16 configurable QoSControls, which have independent qos_masks that masks the ARID/AWID from one bit up to the ARID/AWID width. All 16 QoSControls are either enabled or disabled,

1. If the command is received via the AXI bus, the ARID/AWID is masked by the qos_masks (**QoSConfig(n).qos_mask**) from the 16 QoSControls that are enabled.
2. The masked results are then compared to the qos_ids (**QoSConfig(n).qos_id**). If one of the result are equal, the qos_cnt (**QoSControl(n).qos_cnt**) value is applied to the command and saved in the control queue.

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1.2.5.2 qos_cnt_f

To service latency sensitive commands faster, an adaptive DRAM QoS scheme called QoS fast can be enabled. This policy cannot be done by the memory controller itself, but the IP has to observe its FIFO level.

For read transactions, for example, when the IP's FIFO is less than 1/4th full, there is no margin of time available between the FIFO and the memory controller. At this moment, if the IP flags the memory controller through it's qos_fast index path, the qos_cnt_f (**QoSControl(index).qos_cnt_f**) value that is specified for the IP is applied to the command to give a higher QoS priority over other IP commands.

For write transactions, for example, when the IP's FIFO is more than 3/4th full, there is almost no margin of time available before the FIFO becomes full. At this moment, if the IP flags the memory controller through it's index path, the qos_cnt_f (**QoSControl(index).qos_cnt_f**) value that is specified for the IP is applied to the command to give a higher QoS priority over other IP commands.

Figure 1-5 shows the adaptive DRAM QoS scheme configuration in SoC.

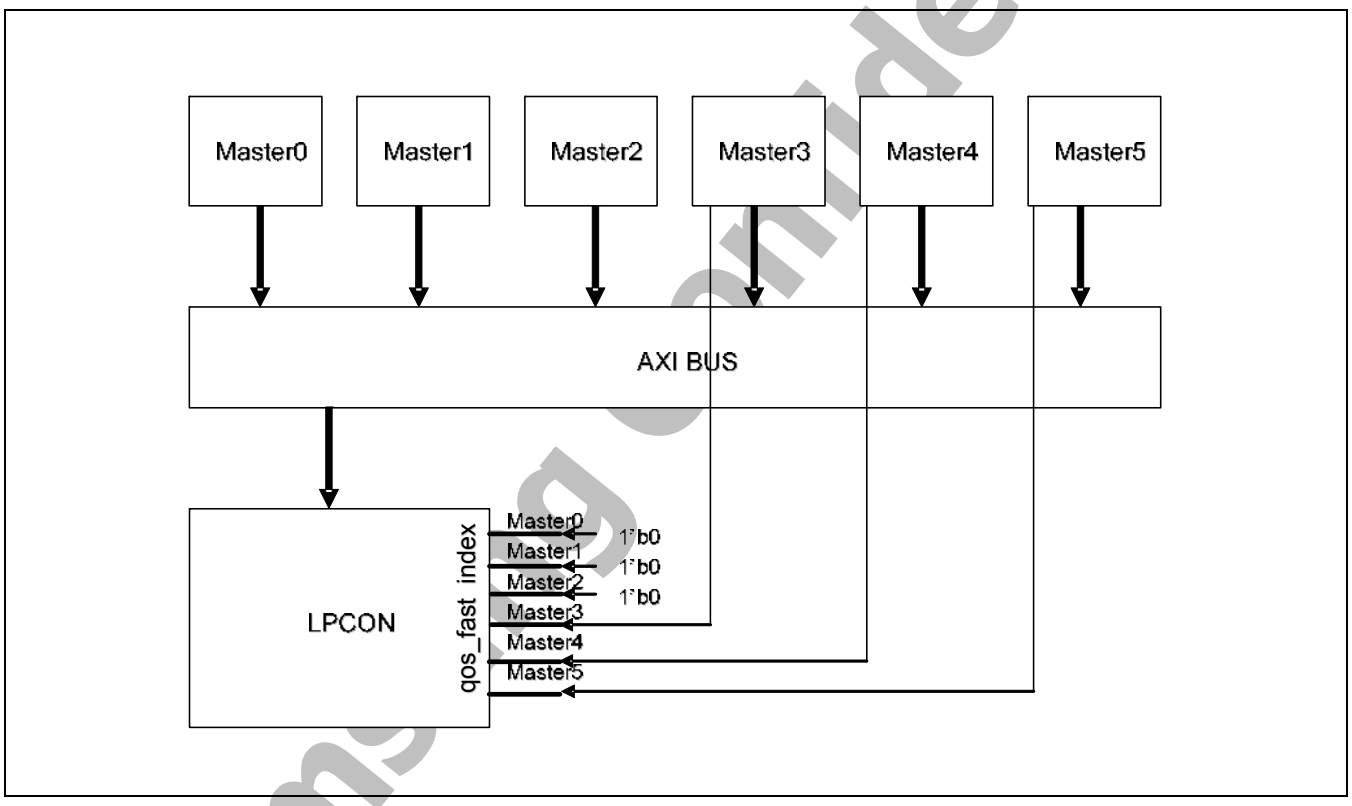

Figure 1-5 Adaptive DRAM QoS Scheme Configuration

Each IP is able to flag the memory controller by accessing a one-bit side-band channel.

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If qos fast (Concontrol.qos_fast_en) is enabled, and the master that sent the command has raised the qos_fast flag of it's specific channel index, instead of qos_cnt (**QoSControl(index**).qos_cnt) being applied to the command, the QoS Cycles for fast request (**QoSControl(index).qos_cnt_f**) is applied. *Table 1-1* shows the QoS fast index of each IP.

Table 1-1 Fast Qos index table

qos_fast index	Master
0	Reserved
1	Reserved
2	Reserved
3	Reserved
4	FIMD window0
5	FIMD window4
6	FIMD window1
7	FIMD window2
8	FIMD window3
9	FIMC0
10	FIMC1
11	FIMC2
12	Reserved
13	VP
14	MIXER_GRP0
15	MIXER_GRP1

1.2.5.3 Default Qos

If qos_cnt is not applied to the command, a default QoS counter (Is set to a different value by modifying ConControl.timeout_cnt) is applied to the command. (Default QoS counter is applied to both read and write)

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1.2.6 READ DATA CAPTURE

A memory device that receives a read command sends the data to the controller after a read latency (i.e. CAS latency). After clearing the DQS, the PHY uses the PHY DLL to phase shift the DQS 90 degrees. Using the shifted DQS, the PHY samples the read data and saves the data into the read data input FIFO, which is located inside the PHY. Then, the controller fetches the data from the PHY while considering the read latency and the read fetch delay, and then sends it to the AXI read channel. The following figures show the read data capture process's timing diagram for each memory type.

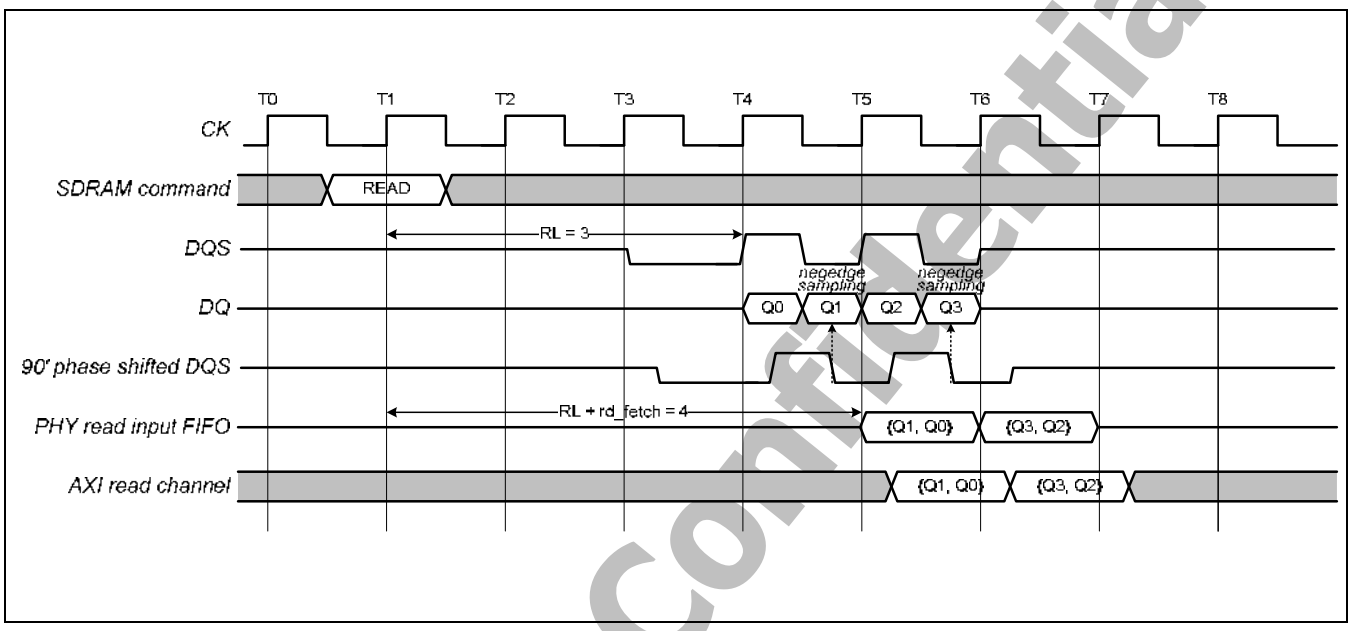

Figure 1-6 Timing Diagram of Read Data Capture (DDR2, zero delay, RL=3, rd_fetch=1)

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Figure 1-6 is for DDR2 having an internal DLL. An internal DLL exists which allows it to send the data after an exact amount of read latency. If we assume there are minimal or no board/ PHY input delay, if sampling the negedge (Q1, Q3 sampling), since the data gets saved into the PHY read data input FIFO, the controller sends the read data to the AXI read channel in 'read latency + 1(read fetch)' cycles. The read fetch cycle is set using the ConControl.rd_fetch bit-field.

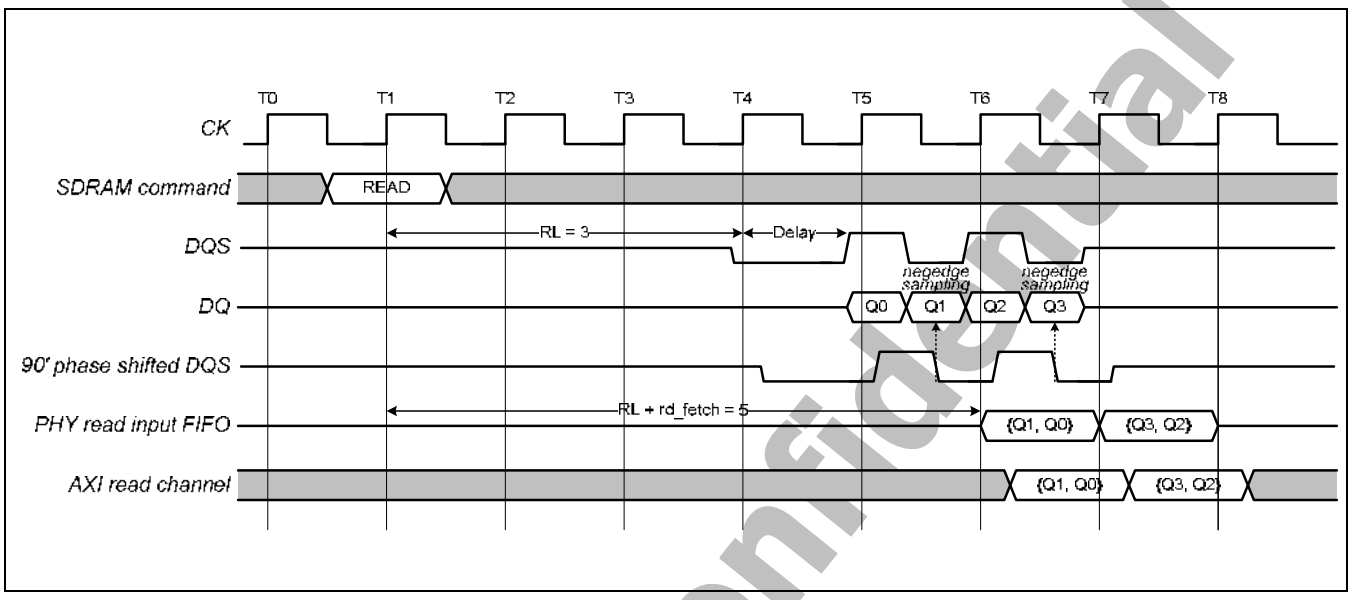

Figure 1-7 Timing Diagram of Read Data Capture (DDR2, non-zero delay, RL=3, rd_fetch=2)

Figure 1-7 is different from Figure 1-6 because a delay exists. Negedge sampling happens at T5 and T6, which is one cycle slower than T4/T5 shown in Figure 1-4. Therefore, the read fetch cycle should be set to two since the sampled read data is saved slowly into the read input FIFO.

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To calculate the DDR2 rd_fetch value:

rd_fetch DDR2) = INT((Delay + 0.5T + 0.25T)/T) = INT(Delay/T + 0.75),

Delay: board delay + PHY input/output delay, T: clock period, INT(x): the rounded-up integer value of x

Therefore, rd_fetch must have minimum one value.

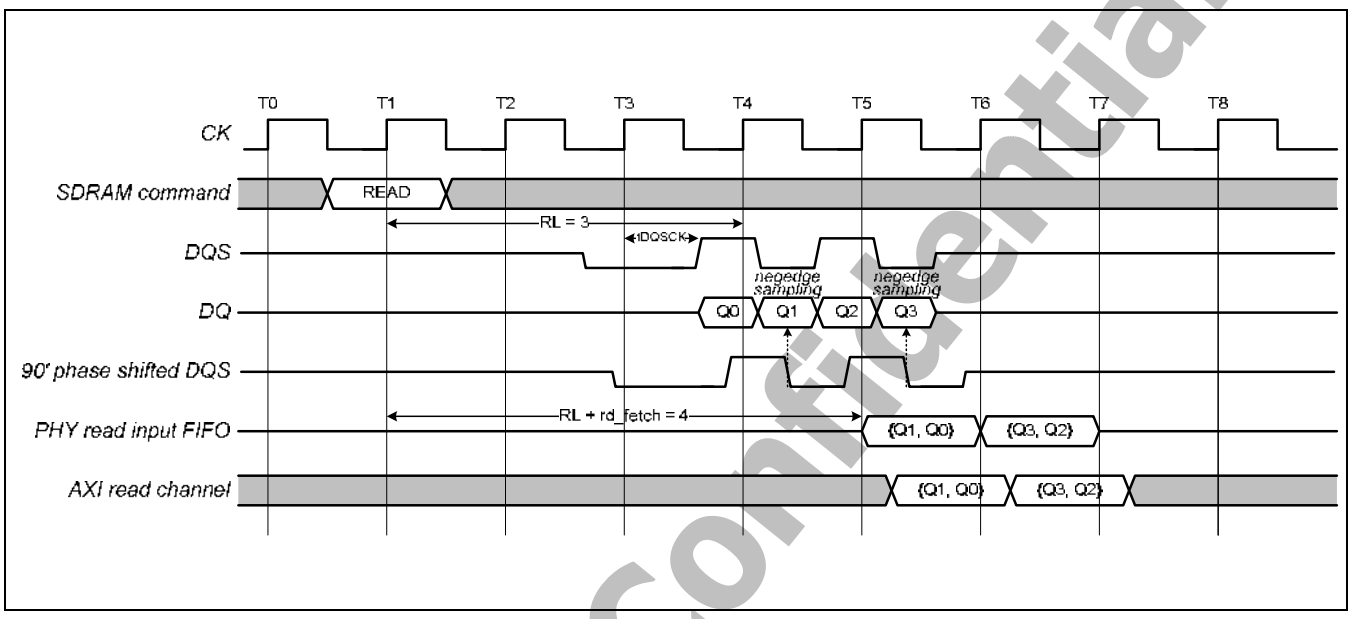

Figure 1-8 Timing Diagram of Read Data Capture (LPDDR/LPDDR2, zero delay, RL=3, rd_fetch=1)

An LPDDR/LPDDR2 does not have an internal DLL. Without an internal DLL as shown in *Figure 1-8* the data is sent out after tDQSCK before the read latency is over. Even if we assume zero delay, since tDQSCK becomes relatively large in high frequencies, the read fetch cycle should be set to one.

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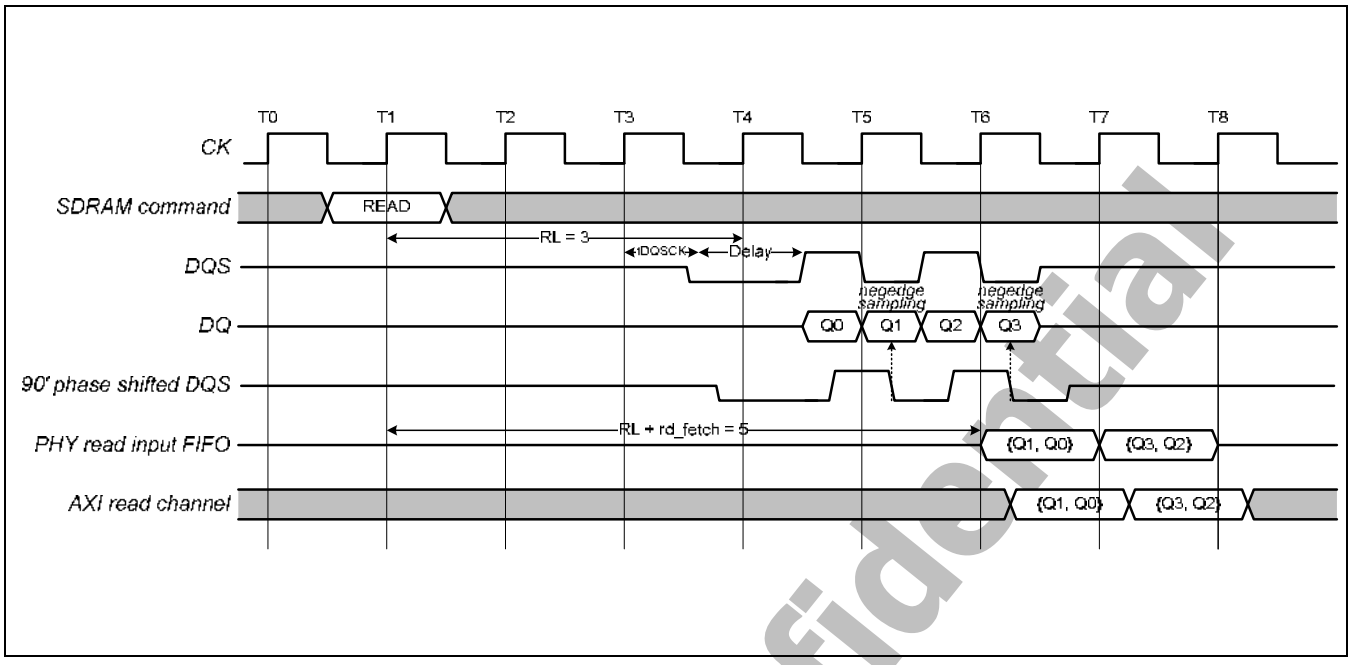

Figure 1-9 Timing Diagram of Read Data Capture (LPDDR/LPDDR2, non-zero delay, RL=3, rd_fetch=2)

If a delay exists as shown in *Figure 1-9*, a bigger value should be assigned to rd_fetch

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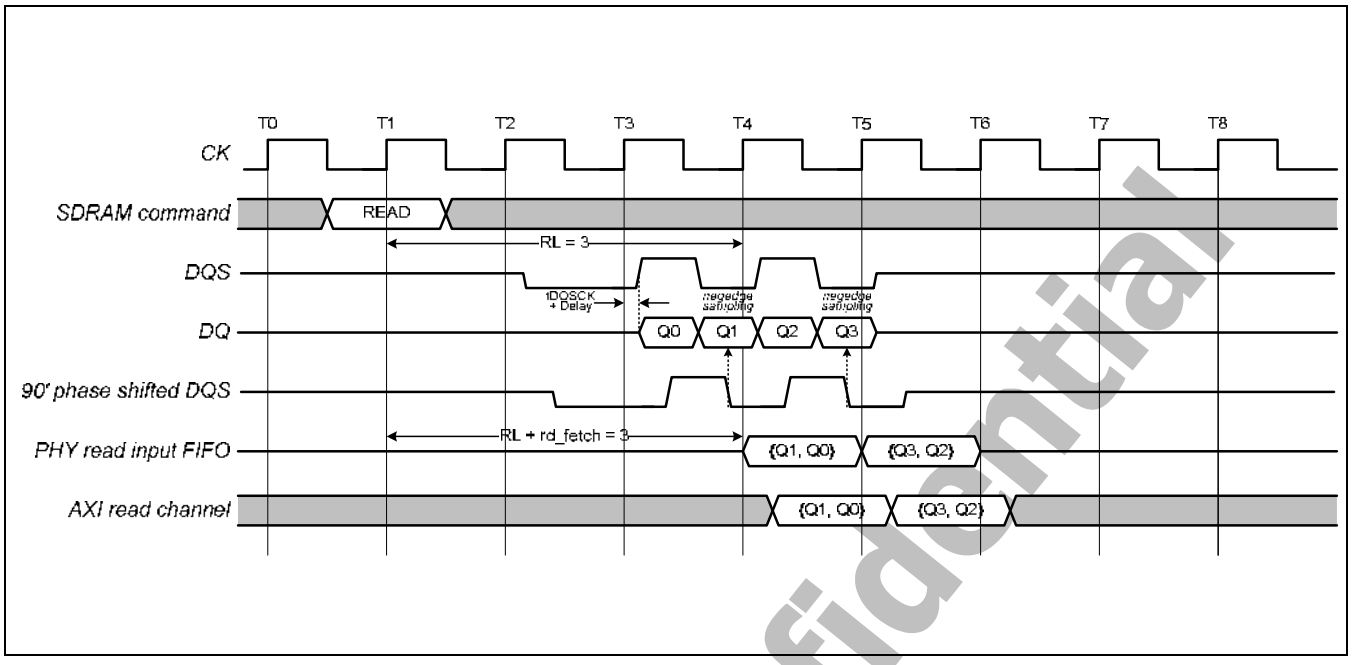

Figure 1-10 Timing Diagram of Read Data Capture (LPDDR/LPDDR2, low frequency, RL=3, rd_fetch=0)

tDQSCK + Delay is relatively small compared to the clock period during low frequencies as shown in *Figure 1-10*. In this situation, negedge sampling happens before read latency and therefore read fetch is set to zero.

To calculate the LPDDR/LPDDR2 rd_fetch value:

rd_fetch (LPDDR/LPDDR2) = INT((-1 + Delay + 0.5T + 0.25T)/T) = INT(Delay/T - 0.25),

Delay: board delay + PHY input delay, T: clock period, INT(x): the rounded-up integer value of x

Therefore, if the value of Delay/T is less than 0.25, rd_fetch is set to zero

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1.3 I/O DESCRIPTION

Signal	I/O	Description	PAD	Type
DDR2SEL	I	Memory Type Selection (0: LPDDR1, 1: DDR2, LPDDR2)	XDDR2SEL	dedicated
SCLK	O	Memory Clock	Xm1(2)SCLK	dedicated
nSCLK	O	Memory Negative Clock	Xm1(2)nSCLK	dedicated
RASn	O	Row Address Selection	Xm1(2)RASn	dedicated
CASn	O	Column Address Selection	Xm1(2)CASn	dedicated
WEn	O	Write Enable	Xm1(2)WEn	dedicated
DATA[31:0]	I/O	Memory Data Bus	Xm1(2)DATA[31:0]	dedicated
DQM[3:0]	O	Write Masking Per Byte	Xm1(2)DQM[3:0]	dedicated
DQSp[3:0]	I/O	Data Strobe Signal Per Byte	Xm1(2)DQS[3:0]	dedicated
DQSn[3:0]	I/O	Data Strobe Negative Signal Per Byte	Xm1(2)DQSn[3:0]	dedicated
ADDR[15:0]	O	Memory Address, Bank Address	Xm1(2)ADDR[15:0]	dedicated
CSn[1:0],	O	Memory CS signals	Xm1(2)CSn[1:0]	dedicated
CKE[1:0]	O	Memory CKE signals	Xm1(2)CKE[1:0]	dedicated

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1.3.1 PAD MUX FOR ADDRESS CONFIGURATION

PAD Name	Config. 1	Config. 2	Config. 3	Config. 4	LPDDR2
Xm1(2)ADDR[0]	ADDR_0	ADDR_0	ADDR_0	ADDR_0	CA_0
Xm1(2)ADDR[1]	ADDR_1	ADDR_1	ADDR_1	ADDR_1	CA_1
Xm1(2)ADDR[2]	ADDR_2	ADDR_2	ADDR_2	ADDR_2	CA_2
Xm1(2)ADDR[3]	ADDR_3	ADDR_3	ADDR_3	ADDR_3	CA_3
Xm1(2)ADDR[4]	ADDR_4	ADDR_4	ADDR_4	ADDR_4	CA_4
Xm1(2)ADDR[5]	ADDR_5	ADDR_5	ADDR_5	ADDR_5	CA_5
Xm1(2)ADDR[6]	ADDR_6	ADDR_6	ADDR_6	ADDR_6	CA_6
Xm1(2)ADDR[7]	ADDR_7	ADDR_7	ADDR_7	ADDR_7	CA_7
Xm1(2)ADDR[8]	ADDR_8	ADDR_8	ADDR_8	ADDR_8	CA_8
Xm1(2)ADDR[9]	ADDR_9	ADDR_9	ADDR_9	ADDR_9	CA_9
Xm1(2)ADDR[10]	ADDR_10	ADDR_10	ADDR_10	ADDR_10	
Xm1(2)ADDR[11]	ADDR_11	ADDR_11	ADDR_11	ADDR_11	
Xm1(2)ADDR[12]	ADDR_12	ADDR_12	ADDR_12	ADDR_12	
Xm1(2)ADDR[13]	ADDR_13	ADDR_13	ADDR_13	ADDR_13	
Xm1(2)ADDR[14]	BA_0	BA_0	BA_0	BA_0	
Xm1(2)ADDR[15]	BA_1	BA_1	BA_1	BA_1	
Xm1(2)CSn[1]	CS_1		BA_2	BA_2	CS_1
Xm1(2)CSn[0]	CS_0	CS_0	CS_0	CS_0	CS_0
Xm1(2)CKE[1]	CKE_1	ADDR_14		ADDR_14	CKE_1
Xm1(2)CKE[0]	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0

NOTE:

1. Address Config. 1 : The Number of Banks (**MEMCONFIGn.chip_bank**) is set under 4banks and the Number of Row Address Bits(**MEMCONFIGn.chip_row**) is set under 14bits.
2. Address Config. 2: The Number of Banks (**MEMCONFIGn.chip_bank**) is set under 4banks and the Number of Row Address Bits(**MEMCONFIGn.chip_row**) is set 15 bits.
3. Address Config. 3: The Number of Banks (**MEMCONFIGn.chip_bank**) is set 8 banks and the Number of Row Address Bits(**MEMCONFIGn.chip_row**) is set under 14 bits
4. Address Config. 4: The Number of Banks (**MEMCONFIGn.chip_bank**) is set 8 banks and the Number of Row Address Bits(**MEMCONFIGn.chip_row**) is set 15bits.
5. Address LPDDR2 : The Type of Memory(**MEMCONTROL.mem_type**) is selected LPDDR2.

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1.4 REGISTER DESCRIPTION

1.4.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
DMC0				
CONCONTROL	0xF000_0000	R/W	Specifies the Controller Control Register	0x0FFF_1350
MEMCONTROL	0xF000_0004	R/W	Specifies the Memory Control Register	0x0020_2100
MEMCONFIG0	0xF000_0008	R/W	Specifies the Memory Chip0 Configuration Register	0x20F0_0312
MEMCONFIG1	0xF000_000C	R/W	Specifies the Memory Chip1 Configuration Register	0x30F0_0312
DIRECTCMD	0xF000_0010	R/W	Specifies the Memory Direct Command Register	0x0000_0000
PRECHCONFIG	0xF000_0014	R/W	Specifies the Precharge Policy Configuration Register	0xFF00_0000
PHYCONTROL0	0xF000_0018	R/W	Specifies the PHY Control0 Register	0x0000_0000
PHYCONTROL1	0xF000_001C	R/W	Specifies the PHY Control1 Register	0x0000_0040
RESERVED	0xF000_0020	R	Reserved	0x0000_0000
PWRDNCONFIG	0xF000_0028	R/W	Specifies the Dynamic Power Down Configuration Register	0xFFFF_00FF
TIMINGAREF	0xF000_0030	R/W	Specifies the AC Timing Register for SDRAM Auto Refresh	0x0000_040E
TIMINGROW	0xF000_0034	R/W	Specifies the AC Timing Register for SDRAM Row	0x0F23_3286
TIMINGDATA	0xF000_0038	R/W	Specifies the AC Timing Register for SDRAM Data	0x1213_0204
TIMINGPOWER	0xF000_003C	R/W	Specifies the AC Timing Register for Power Mode of SDRAM	0x0E1B_0422
PHYSTATUS	0xF000_0040	R	Specifies the PHY Status Register	0x0000_000X
CHIP0STATUS	0xF000_0048	R	Specifies the Memory Chip0 Status Register	0x0000_0000
CHIP1STATUS	0xF000_004C	R	Specifies the Memory Chip1 Status Register	0x0000_0000
AREFSTATUS	0xF000_0050	R	Specifies the Counter Status Register for Auto Refresh	0x0000_FFFF
MRSTATUS	0xF000_0054	R	Specifies the Memory Mode Registers Status Register	0x0000_0000
PHYTEST0	0xF000_0058	R/W	Specifies the PHY Test Register 0	0x0000_0000
PHYTEST1	0xF000_005C	R	Specifies the PHY Test Register 1	0x0000_0000
QOSCONTROL0	0xF000_0060	R/W	Specifies the Quality of Service Control Register 0	0x0000_0000
QOSCONFIG0	0xF000_0064	R/W	Specifies the Quality of Service Configuration Register 0	0x0000_0000
QOSCONTROL1	0xF000_0068	R/W	Specifies the Quality of Service Control Register 1	0x0000_0000
QOSCONFIG1	0xF000_006C	R/W	Specifies the Quality of Service Configuration Register 1	0x0000_0000
QOSCONTROL2	0xF000_0070	R/W	Specifies the Quality of Service Control Register 2	0x0000_0000

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Register	Address	R/W	Description	Reset Value
QOSCONFIG2	0xF000_0074	R/W	Specifies the Quality of Service Configuration Register 2	0x0000_0000
QOSCONTROL3	0xF000_0078	R/W	Specifies the Quality of Service Control Register 3	0x0000_0000
QOSCONFIG3	0xF000_007C	R/W	Specifies the Quality of Service Configuration Register 3	0x0000_0000
QOSCONTROL4	0xF000_0080	R/W	Specifies the Quality of Service Control Register 4	0x0000_0000
QOSCONFIG4	0xF000_0084	R/W	Specifies the Quality of Service Configuration Register 4	0x0000_0000
QOSCONTROL5	0xF000_0088	R/W	Specifies the Quality of Service Control Register 5	0x0000_0000
QOSCONFIG5	0xF000_008C	R/W	Specifies the Quality of Service Configuration Register 5	0x0000_0000
QOSCONTROL6	0xF000_0090	R/W	Specifies the Quality of Service Control Register 6	0x0000_0000
QOSCONFIG6	0xF000_0094	R/W	Specifies the Quality of Service Configuration Register 6	0x0000_0000
QOSCONTROL7	0xF000_0098	R/W	Specifies the Quality of Service Control Register 7	0x0000_0000
QOSCONFIG7	0xF000_009C	R/W	Specifies the Quality of Service Configuration Register 7	0x0000_0000
QOSCONTROL8	0xF000_00A0	R/W	Specifies the Quality of Service Control Register 8	0x0000_0000
QOSCONFIG8	0xF000_00A4	R/W	Specifies the Quality of Service Configuration Register 8	0x0000_0000
QOSCONTROL9	0xF000_00A8	R/W	Specifies the Quality of Service Control Register 9	0x0000_0000
QOSCONFIG9	0xF000_00AC	R/W	Specifies the Quality of Service Configuration Register 9	0x0000_0000
QOSCONTROL10	0xF000_00B0	R/W	Specifies the Quality of Service Control Register 10	0x0000_0000
QOSCONFIG10	0xF000_00B4	R/W	Specifies the Quality of Service Configuration Register 10	0x0000_0000
QOSCONTROL11	0xF000_00B8	R/W	Specifies the Quality of Service Control Register 11	0x0000_0000
QOSCONFIG11	0xF000_00BC	R/W	Specifies the Quality of Service Configuration Register 11	0x0000_0000
QOSCONTROL12	0xF000_00C0	R/W	Specifies the Quality of Service Control Register 12	0x0000_0000
QOSCONFIG12	0xF000_00C4	R/W	Specifies the Quality of Service Configuration Register 12	0x0000_0000
QOSCONTROL13	0xF000_00C8	R/W	Specifies the Quality of Service Control Register 13	0x0000_0000
QOSCONFIG13	0xF000_00CC	R/W	Specifies the Quality of Service Configuration Register 13	0x0000_0000
QOSCONTROL14	0xF000_00D0	R/W	Specifies the Quality of Service Control Register 14	0x0000_0000
QOSCONFIG14	0xF000_00D4	R/W	Specifies the Quality of Service Configuration Register 14	0x0000_0000
QOSCONTROL15	0xF000_00D8	R/W	Specifies the Quality of Service Control Register 15	0x0000_0000
QOSCONFIG15	0xF000_00DC	R/W	Specifies the Quality of Service Configuration Register 15	0x0000_0000

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Register	Address	R/W	Description	Reset Value
DMC1				
CONCONTROL	0xF140_0000	R/W	Specifies the Controller Control Register	0x0FFF1350
MEMCONTROL	0xF140_0004	R/W	Specifies the Memory Control Register	0x00202100
MEMCONFIG0	0xF140_0008	R/W	Specifies the Memory Chip0 Configuration Register	0x40E00312
MEMCONFIG1	0xF140_000C	R/W	Specifies the Memory Chip1 Configuration Register	0x60E00312
DIRECTCMD	0xF140_0010	R/W	Specifies the Memory Direct Command Register	0x00000000
PRECHCONFIG	0xF140_0014	R/W	Specifies the Precharge Policy Configuration Register	0xFF000000
PHYCONTROL0	0xF140_0018	R/W	Specifies the PHY Control0 Register	0x00000000
PHYCONTROL1	0xF140_001C	R/W	Specifies the PHY Control1 Register	0x00000040
RESERVED	0xF140_0020	R/W	Reserved	0x00000000
PWRDNCONFIG	0xF140_0028	R/W	Specifies the Dynamic Power Down Configuration Register	0xFFFF00FF
TIMINGAREF	0xF140_0030	R/W	Specifies the AC Timing Register for SDRAM Auto Refresh	0x0000040E
TIMINGROW	0xF140_0034	R/W	Specifies the AC Timing Register for SDRAM Row	0x0F233286
TIMINGDATA	0xF140_0038	R/W	Specifies the AC Timing Register for SDRAM Data	0x12130204
TIMINGPOWER	0xF140_003C	R/W	Specifies the AC Timing Register for Power Specifies the Mode of SDRAM	0x0E1B0422
PHYSTATUS	0xF140_0040	R	Specifies the PHY Status Register	0x0000000X
CHIP0STATUS	0xF140_0048	R	Specifies the Memory Chip0 Status Register	0x00000000
CHIP1STATUS	0xF140_004C	R	Specifies the Memory Chip1 Status Register	0x00000000
AREFSTATUS	0xF140_0050	R	Specifies the Counter Status Register for Auto Refresh	0x0000FFFF
MRSTATUS	0xF140_0054	R	Specifies the Memory Mode Registers Status Register	0x00000000
PHYTEST0	0xF140_0058	R/W	Specifies the PHY Test Register 0	0x00000000
PHYTEST1	0xF140_005C	R	Specifies the PHY Test Register 1	0x00000000
QOSCONTROL0	0xF140_0060	R/W	Specifies the Quality of Service Control Register 0	0x00000000
QOSCONFIG0	0xF140_0064	R/W	Specifies the Quality of Service Configuration Register 0	0x00000000
QOSCONTROL1	0xF140_0068	R/W	Specifies the Quality of Service Control Register 1	0x00000000
QOSCONFIG1	0xF140_006C	R/W	Specifies the Quality of Service Configuration Register 1	0x00000000
QOSCONTROL2	0xF140_0070	R/W	Specifies the Quality of Service Control Register 2	0x00000000
QOSCONFIG2	0xF140_0074	R/W	Specifies the Quality of Service Configuration Register 2	0x00000000
QOSCONTROL3	0xF140_0078	R/W	Specifies the Quality of Service Control Register 3	0x00000000

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Register	Address	R/W	Description	Reset Value
QOSCONFIG3	0xF140_007C	R/W	Specifies the Quality of Service Configuration Register 3	0x00000000
QOSCONTROL4	0xF140_0080	R/W	Specifies the Quality of Service Control Register 4	0x00000000
QOSCONFIG4	0xF140_0084	R/W	Specifies the Quality of Service Configuration Register 4	0x00000000
QOSCONTROL5	0xF140_0088	R/W	Specifies the Quality of Service Control Register 5	0x00000000
QOSCONFIG5	0xF140_008C	R/W	Specifies the Quality of Service Configuration Register 5	0x00000000
QOSCONTROL6	0xF140_0090	R/W	Specifies the Quality of Service Control Register 6	0x00000000
QOSCONFIG6	0xF140_0094	R/W	Specifies the Quality of Service Configuration Register 6	0x00000000
QOSCONTROL7	0xF140_0098	R/W	Specifies the Quality of Service Control Register 7	0x00000000
QOSCONFIG7	0xF140_009C	R/W	Specifies the Quality of Service Configuration Register 7	0x00000000
QOSCONTROL8	0xF140_00A0	R/W	Specifies the Quality of Service Control Register 8	0x00000000
QOSCONFIG8	0xF140_00A4	R/W	Specifies the Quality of Service Configuration Register 8	0x00000000
QOSCONTROL9	0xF140_00A8	R/W	Specifies the Quality of Service Control Register 9	0x00000000
QOSCONFIG9	0xF140_00AC	R/W	Specifies the Quality of Service Configuration Register 9	0x00000000
QOSCONTROL10	0xF140_00B0	R/W	Specifies the Quality of Service Control Register 10	0x00000000
QOSCONFIG10	0xF140_00B4	R/W	Specifies the Quality of Service Configuration Register 10	0x00000000
QOSCONTROL11	0xF140_00B8	R/W	Specifies the Quality of Service Control Register 11	0x00000000
QOSCONFIG11	0xF140_00BC	R/W	Specifies the Quality of Service Configuration Register 11	0x00000000
QOSCONTROL12	0xF140_00C0	R/W	Specifies the Quality of Service Control Register 12	0x00000000
QOSCONFIG12	0xF140_00C4	R/W	Specifies the Quality of Service Configuration Register 12	0x00000000
QOSCONTROL13	0xF140_00C8	R/W	Specifies the Quality of Service Control Register 13	0x00000000
QOSCONFIG13	0xF140_00CC	R/W	Specifies the Quality of Service Configuration Register 13	0x00000000
QOSCONTROL14	0xF140_00D0	R/W	Specifies the Quality of Service Control Register 14	0x00000000
QOSCONFIG14	0xF140_00D4	R/W	Specifies the Quality of Service Configuration Register 14	0x00000000
QOSCONTROL15	0xF140_00D8	R/W	Specifies the Quality of Service Control Register 15	0x00000000
QOSCONFIG15	0xF140_00DC	R/W	Specifies the Quality of Service Configuration Register 15	0x00000000

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1.4.1.1 Controller Control Register (ConControl, R/W, Address = 0xF000_0000, 0xF140_0000)

CONCONTROL	Bit	Description	R/W	Initial State
Reserved	[31:28]	Should be zero		0x0
timeout_cnt	[27:16]	Default Timeout Cycles 0xn = n aclk cycles (aclk: AXI clock) This counter prevents transactions in command queue from starvation. This counter starts if a new AXI transaction comes into a queue. If the counter becomes zero, the corresponding transaction becomes the highest priority command of all the transactions in the command queue. This is a default timeout counter and overridden by the QoS counter if the ARID/AWID matched with the QoS ID comes into the command queue. Refer to *"1.2.5 Quality of Service"*.	R/W	0xFFF
rd_fetch	[15:12]	Read Data Fetch Cycles 0xn = n mclk cycles (mclk: Memory clock) This register is for the unpredictable latency of read data coming from memory devices by tDQSCK variation or the board flying time. The read fetch delay of PHY read FIFO must be controlled by this parameter. The controller will fetch read data from PHY after (read_latency + n) mclk cycles. Refer to *"1.2.6 Read Data Capture"*.	R/W	0x1
qos_fast_en	[11]	Enables adaptive QoS 0x0 = Disables 0x1 = Enables If enabled, the controller loads QoS counter value from QoSControl.qos_cnt_f instead of QoSControl.qos_cnt if the corresponding input pin qos_fast is turned on. Refer to *"1.2.5 Quality of Service"*.	R/W	0x0
dq_swap	[10]	DQ Swap 0x0 = Disables 0x1 = Enables If enabled, the controller reverses the bit order of memory data pins. (For example, DQ[31] <-> DQ[0], DQ[30] <-> DQ[1])	R/W	0x0
chip1_empty	[9]	Command Queue Status of Chip1 0x0 = Not Empty 0x1 = Empty There is no AXI transaction corresponding to chip1 memory in the command queue entries	R	0x1
chip0_empty	[8]	Command Queue Status of Chip0 0x0 = Not Empty 0x1 = Empty There is no AXI transaction corresponding to chip0 memory in the command queue entries	R	0x1

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CONCONTROL	Bit	Description	R/W	Initial State
drv_en	[7]	PHY Driving 0x0 = Disables 0x1 = Enables During the high-Z state of the memory bidirectional pins, PHY drives these pins with the zeros or pull down these pins for preventing current leakage. Set PhyControl1.drv_type register to select driving type.	R/W	0x0
ctc_rtr_gap_en	[6]	Read Cycle Gap for Two Different Chips 0x0 = Disables 0x1 = Enables To prevent collision between reads from two different memory devices, a one-cycle gap is required. Enable this register to insert the gap automatically for continuous reads from two different memory devices.	R/W	0x1
aref_en	[5]	Auto Refresh Counter 0x0 = Disables 0x1 = Enables Enable this to decrease the auto refresh counter by 1 at the rising edge of the mclk.	R/W	0x0
out_of	[4]	Out of Order Scheduling 0x0 = Disables 0x1 = Enables The embedded scheduler enables out-of order operation to improve SDRAM utilization	R/W	0x1
Reserved	[3:0]	Should be zero		0x0

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1.4.1.2 Memory Control Register (MemControl, R/W, Address = 0xF000_0004, 0xF140_0004)

MEMCONTROL	Bit	Description	R/W	Initial State
Reserved	[31:23]	Should be zero		0x0
bl	[22:20]	Memory Burst Length 0x0 = Reserved 0x1 = 2 0x2 = 4 0x3 = 8 0x4 = 16 0x5 ~ 0x7 = Reserved In case of DDR2/ LPDDR2, the controller only supports burst length 4.	R/W	0x2
num_chip	[19:16]	Number of Memory chips 0x0 = 1 chip 0x1 = 2 chips 0x2 ~ 0xf = Reserved	R/W	0x0
mem_width	[15:12]	Width of Memory Data Bus 0x0 = Reserved 0x1 = 16-bit 0x2 = 32-bit 0x3 ~ 0xf = Reserved	R/W	0x2
mem_type	[11:8]	Type of Memory 0x0 = Reserved 0x1 = LPDDR 0x2 = LPDDR2 0x3 = Reserved 0x4 = DDR2 0x5 ~ 0xf = Reserved	R/W	0x1
add_lat_pall	[7:6]	Additional Latency for PALL 0x0 = 0 cycle 0x1 = 1 cycle 0x2 = 2 cycle 0x3 = 3 cycle If all banks precharge command is issued, the latency of precharging will be tRP + add_lat_pall	R/W	0x0
dsref_en	[5]	Dynamic Self Refresh 0x0 = Disables 0x1 = Enables Refer to *"1.2.3.3 . Dynamic Self Refresh"*	R/W	0x0
tp_en	[4]	Timeout Precharge 0x0 = Disables 0x1 = Enables If tp_en is enabled, it automatically precharges an open bank after a specified amount of mclk cycles (if no access has been made in between the cycles) in an open page policy. If PrechConfig.tp_cnt bit-field is set, it specifies the amount of	R/W	0x0

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MEMCONTROL	Bit	Description	R/W	Initial State
		mclk cycles to wait until timeout precharge precharges the open bank. Refer to *"1.2.4.2 . Timeout Precharge".*		
dpwrdn_type	[3:2]	Type of Dynamic Power Down 0x0 = Active/ Precharge power down 0x1 = Force precharge power down 0x2 ~ 0x3 = Reserved Refer to *"1.2.3.2 Dynamic Power Down"*.	R/W	0x0
dpwrdn_en	[1]	Dynamic Power Down 0x0 = Disable 0x1 = Enable	R/W	0x0
clk_stop_en	[0]	Dynamic Clock Control 0x0 = Always running 0x1 = Stops during idle periods Refer to *"1.2.3.4 . Clock Stop".*	R/W	0x0

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1.4.1.3 Memory Chip0 Configuration Register (MemConfig0, R/W, Address=0xF000_0008, 0xF140_0008)

MEMCONFIG0	Bit	Description	R/W	Initial State
chip_base	[31:24]	AXI Base Address AXI base address [31:24] = chip_base For example, if chip_base = 0x20, then AXI base address of memory chip0 becomes 0x2000_0000.	R/W	DMC0: 0x20 DMC1: 0X40
chip_mask	[23:16]	AXI Base Address Mask Upper address bit mask to determine AXI offset address of memory chip0. 0 = Corresponding address bit is not to be used for comparison 1 = Corresponding address bit is to be used for comparison For example, if chip_mask = 0xF8, then AXI offset address becomes 0x0000_0000 ~ 0x07FF_FFFF. If AXI base address of memory chip0 is 0x2000_0000, then memory chip0 has an address range of 0x2000_0000 ~ 0x27FF_FFFF.	R/W	DMC0: 0xF0 DMC1: 0xE0
chip_map	[15:12]	Address Mapping Method (AXI to Memory) 0x0 = Linear ({bank, row, column, width}), 0x1 = Interleaved ({row, bank, column, width}), 0x2 = Mixed1 (if bank(MSB) = 1'b1, {1'b1, bank(except MSB), row, column, width} else {1'b0, row, bank(except MSB), column, width}), 0x3 ~ 0xf = Reserved	R/W	0x0
chip_col	[11:8]	Number of Column Address Bits 0x0 = Reserved 0x1 = 8 bits 0x2 = 9 bits 0x3 = 10 bits 0x4 = 11 bits 0x5 ~ 0xf = Reserved	R/W	0x3
chip_row	[7:4]	Number of Row Address Bits 0x0 = 12 bits 0x1 = 13 bits 0x2 = 14 bits 0x3 = 15 bits 0x4 ~ 0xf = Reserved	R/W	0x1
chip_bank	[3:0]	Number of Banks 0x0 = 1 bank 0x1 = 2 banks 0x2 = 4 banks 0x3 = 8 banks 0x4 ~ 0xf = Reserved	R/W	0x2

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1.4.1.4 Memory Chip1 Configuration Register (MemConfig1, R/W, Address = 0xF000_000C, 0xF140_000C)

MEMCONFIG1	Bit	Description	R/W	Initial State
chip_base	[31:24]	AXI Base Address AXI base address [31:24] = chip_base, For example, if chip_base = 0x28, then AXI base address of chip1 becomes 0x2800_0000.	R/W	DMC0: 0x30 DMC1: 0x60
chip_mask	[23:16]	AXI Base Address Mask Upper address bit mask to determine AXI offset address of memory chip1. 0 = Corresponding address bit is not to be used for comparison 1 = Corresponding address bit is to be used for comparison For example, if chip_mask = 0xF0, then AXI offset address becomes 0x0000_0000 ~ 0x0FFF_FFFF. If AXI base address of memory chip1 is 0x2800_0000, then memory chip1 has an address range of 0x2800_0000 ~ 0x37FF_FFFF.	R/W	DMC0: 0xF0 DMC1: 0xE0
chip_map	[15:12]	Address Mapping Method (AXI to memory) 0x0 = Linear ({bank, row, column, width}), 0x1 = Interleaved ({row, bank, column, width}), 0x2 = Mixed1 (if bank(MSB) = 1'b1, {1'b1, bank(except MSB), row, column, width} else {1'b0, row, bank(except MSB), column, width}), 0x3 ~ 0xf = Reserved	R/W	0x0
chip_col	[11:8]	Number of Column Address Bits 0x0 = Reserved 0x1 = 8 bits 0x2 = 9 bits 0x3 = 10 bits 0x4 = 11 bits 0x5 ~ 0xf = Reserved	R/W	0x3
chip_row	[7:4]	Number of Row Address Bits 0x0 = 12 bits 0x1 = 13 bits 0x2 = 14 bits 0x3 = 15 bits 0x4 ~ 0xf = Reserved	R/W	0x1
chip_bank	[3:0]	Number of Banks 0x0 = 1 bank 0x1 = 2 banks 0x2 = 4 banks 0x3 = 8 banks 0x4 ~ 0xf = Reserved	R/W	0x2

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1.4.1.5 Memory Direct Command Register (DirectCmd, R/W, Address = 0xF000_0010, 0xF140_0010)

DIRECTCMD	Bit	Description	R/W	Initial State
Reserved	[31:28]	Should be zero.		0x0
cmd_type	[27:24]	Type of Direct Command 0x0 = MRS/EMRS (mode register setting), 0x1 = PALL (all banks precharge), 0x2 = PRE (per bank precharge), 0x3 = DPD (deep power down), 0x4 = REFS (self refresh), 0x5 = REFA (auto refresh), 0x6 = CKEL (active/ precharge power down), 0x7 = NOP (exit from active/ precharge power down or deep power down, 0x8 = REFSX (exit from self refresh) 0x9 = MRR (mode register reading), 0xa ~ 0xf = Reserved If a direct command is issued, AXI masters must not access memory. It is strongly recommended to check the command queue's state by Concontrol.chip0/1_empty before issuing a direct command You must disable dynamic power down, dynamic self refresh and force precharge function (MemControl register). MRS/EMRS and MRR commands should be issued if all banks are in idle state. If MRS/EMRS and MRR is issued to LPDDR2, the CA pins must be mapped as follows. MA[7:0] = {cmd_addr[1:0], cmd_bank[2:0], cmd_addr[12:10]}, OP[7:0] = cmd_addr[9:2]	R/W	0x0
Reserved	[23:21]	Should be zero.		0x0
cmd_chip	[20]	Chip Number to send the direct command to 0 = Chip 0 1 = Chip 1	R/W	0x0
cmd_bank	[18:16]	Related Bank Address when issuing a direct command To send a direct command to a chip, additional information such as the bank address is required. This register is used in such situations.	R/W	0x0
cmd_addr	[14:0]	Related Address Value when issuing a direct command To send a direct command to a chip, additional information such as the address is required. This register is used in such situations.	R/W	0x0

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1.4.1.6 Precharge Policy Configuration Register (PrechConfig, R/W, Address = 0xF000_0014, 0xF140_0014)

PRECHCONFIG	Bit	Description	R/W	Initial State
tp_cnt	[31:24]	Timeout Precharge Cycles 0xn = n mclk cycles, If the timeout precharge function (MemControl.tp_en) is enabled and the timeout precharge counter becomes zero, the controller forces the activated memory bank into the precharged state. Refer to *"1.2.4.2 . Timeout Precharge"*.	R/W	0xFF
Reserved	[23:16]	Should be zero		0x0
chip1_policy	[15:8]	Memory Chip1 Precharge Bank Selective Policy 0x0 = Open page policy 0x1 = Close page (auto precharge) policy chip1_policy[n], n is the bank number of chip1. Open Page Policy: After a READ or WRITE, the row accessed before is left open. Close Page (Auto Precharge) Policy: Right after a READ or WRITE command, memory devices automatically precharges the bank. This is a bank selective precharge policy. For example, if chip1_policy[2] is 0x0, bank2 of chip1 has an open page policy and if chip1_policy[6] is 0x1, bank6 of chip1 has a close page policy. Refer to "*1.2.4.1 Bank Selective Precharge Policy*".	R/W	0x0
chip0_policy	[7:0]	Memory chip0 Precharge Bank Selective Policy 0x0 = open page policy 0x1 = close page (auto precharge) policy Chip0_policy[n], n is the bank number of chip0. This is for memory chip0.	R/W	0x0

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1.4.1.7 PHY Control0 Register (PhyControl0, R/W, Address = 0xF000_0018, 0xF140_0018)

PHYCONTROL0	Bit	Description	R/W	Initial State
ctrl_force	[31:24]	DLL Force Delay This field is used instead of ctrl_lock_value[9:2] from the PHY DLL when ctrl_dll_on is LOW. (i.e. If the DLL is off, this field is used to generate 270' clock and shift DQS by 90'.)	R/W	0x0
ctrl_inc	[23:16]	DLL Delay Increment Increase the amount of start point This value should be 0x10	R/W	0x0
ctrl_start_point	[15:8]	DLL Lock Start Point Initial DLL lock start point. This is the number of delay cells and is the start point where "DLL" start tracing to lock. Calculates Initial delay time by multiplying the unit delay of delay cell and this value. This value should be 0x10	R/W	0x0
dqs_delay	[7:4]	Delay Cycles for DQS Cleaning This register is to enable PHY to clean incoming DQS signals delayed by external circumstances. If DQS is coming with read latency plus n mclk cycles, this registers must be set to n mclk cycles.	R/W	0x0
ctrl_dfdqs	[3]	Differential DQS If enabled, PHY generates differential DQS out signals for write command and receives differential DQS input signals for read command. This function is used in case of DDR2/LPDDR2.	R/W	0x0
ctrl_half	[2]	DLL Low Speed HIGH active signal to activate the low speed mode for DLL. If this bit is set, DLL runs at low speed (80MHz ~ 100MHz)	R/W	0x0
ctrl_dll_on	[1]	DLL On HIGH active start signal to activate the DLL. This signal should be kept HIGH for normal operation. If this signal becomes LOW, DLL is turned off and ctrl_clock and ctrl_flock become HIGH. This bit should be set before ctrl_start is set to turn on the DLL	R/W	0x0
ctrl_start	[0]	DLL Start HIGH active start signal to initiate the DLL run and lock. This signal should be kept HIGH during normal operation. If this signal becomes LOW, DLL stops running. To re-run DLL, make this signal HIGH again. In the case of re-running, DLL loses previous lock information. Before ctrl_start is set, make sure that ctrl_dll_on is HIGH.	R/W	0x0

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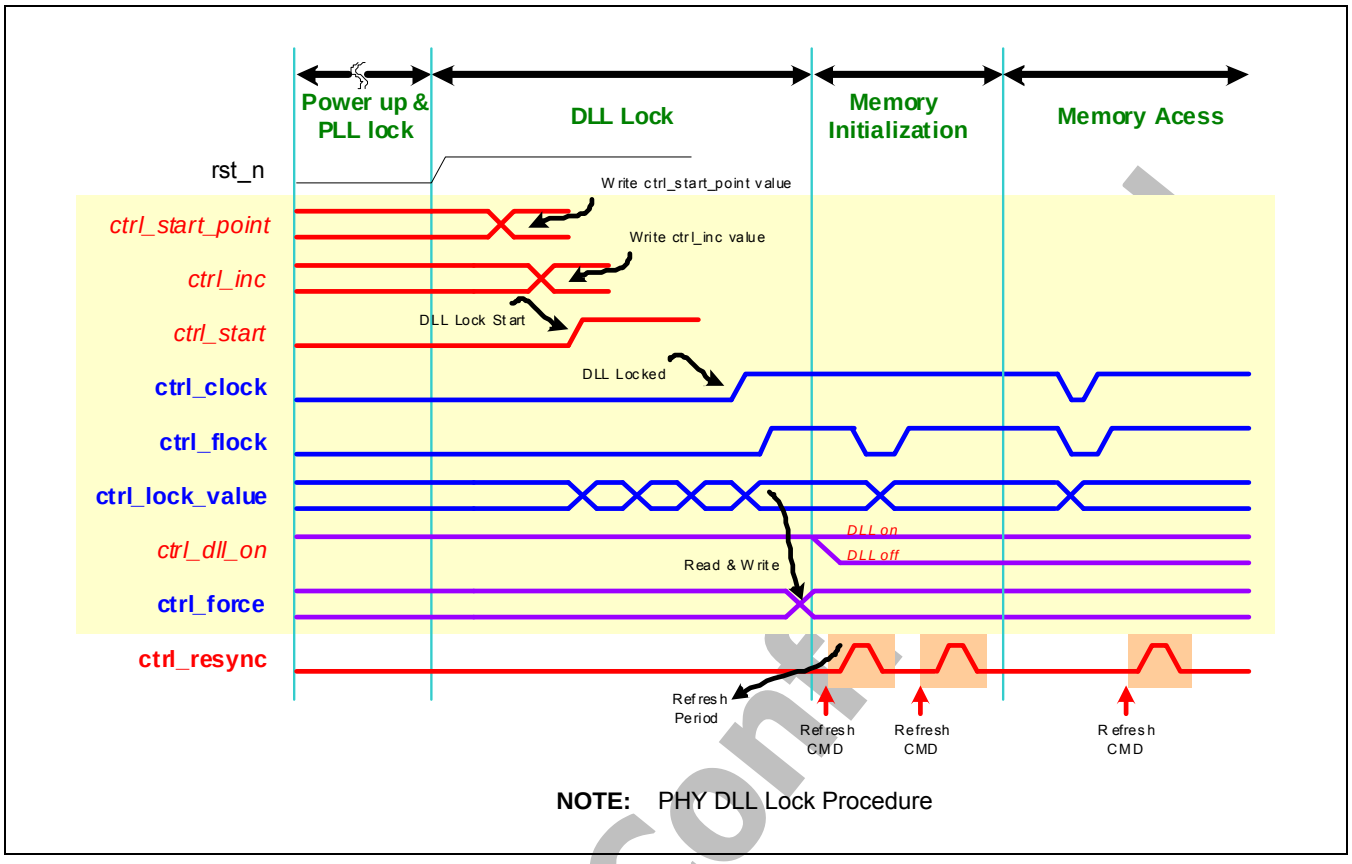

Figure 1-11 DLL Lock Procedure

Use DLL to compensate Process, Voltage and Temperature (PVT) condition. Therefore DLL should not be turned-off for reliable operation except for the case of frequency scaling (To lower frequency scaling is permitted)

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1.4.1.8 PHY Control1 Register (PhyControl1, R/W, Address = 0xF000_001C, 0xF140_001C)

PHYCONTROL1	Bit	Description	R/W	Initial State
Reserved	[31:23]	Should be zero		0x0
ctrl_offsetd	[22:16]	This field is for debug purpose. If this field is fixed, field value must not be changed during operation. This value is valid after ctrl_resync becomes HIGH and LOW. offset amount for 270' clock generation ctrl_offsetd[6] = 1 : (tFS : fine step delay) 270' delay amount - ctrl_offsetd[5:0] x **tFS** ctrl_offsetd[6] = 0 : 270' delay amount + ctrl_offsetd[5:0] x **tFS**	R/W	0x0
drv_type	[15]	Driving Type of Bidirectional Pins in Idle State 0x0 = Drive all to zeros 0x1 = Pull down all If CAS or read data latency is 2, this register must not set be to 0x0.		0x0
ctrl_offsetc	[14:8]	Delay Offset for DQS Cleaning Gate offset amount for DDR. If this field is fixed, this value should not be changed during operation. This value is valid after ctrl_resync becomes HIGH and LOW. ctrl_offsetc[6] = 1 : (tFS : fine step delay) GATEout delay amount - ctrl_offsetc[5:0] x **tFS** ctrl_offsetc[6] = 0 : GATEout delay amount + ctrl_offsetc[5:0] x **tFS**	R/W	0x0
ctrl_ref	[7:4]	Reference Count for DLL Lock Confirmation	R/W	0x4
fp_resync	[3]	Force DLL Resynchronization	R/W	0x0
ctrl_shiftc	[2:0]	Phase Delay for DQS Cleaning GATEout signal delay amount for DDR. If this field is fixed, this value should not be changed during operation. This value is valid after ctrl_resync becomes HIGH and LOW. 0x0 = T/128 (2.8125' shift) 0x1 = T/64 (5.625' shift) 0x2 = T/32 (11.25' shift) 0x3 = T/16 (22.5' shift) 0x4 = T/8 (45' shift) 0x5 = T/4 (90' shift) 0x6 = T/2 (180' shift) 0x7 = T (360' shift) Recommended values according to memory type : 0x5 when LPDDR/LPDDR2 @200MHz 0x6 when DDR2 @200MHz	R/W	0x0

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Use DQS cleaning to remove high-Z state of DQS.

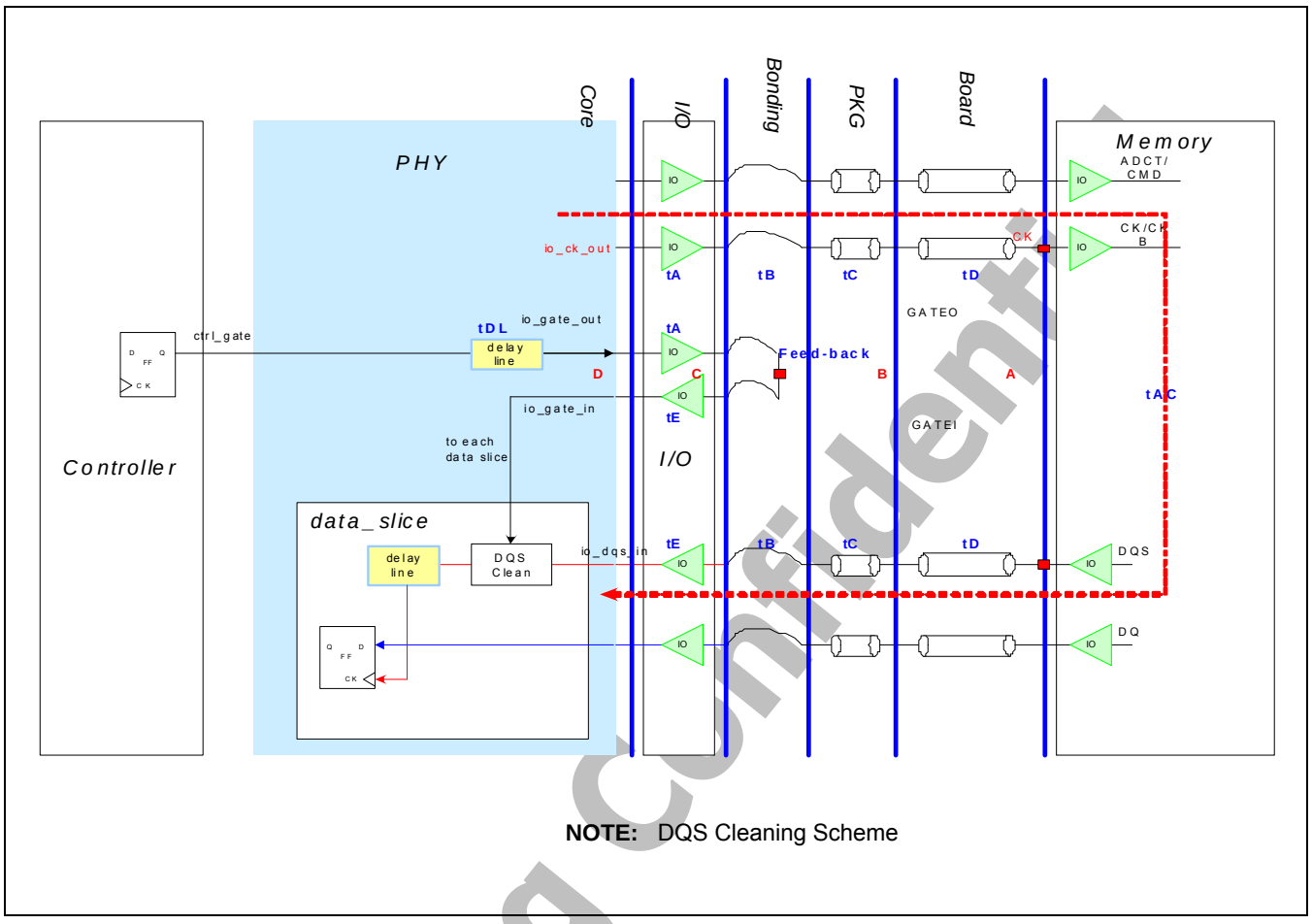

Figure 1-12 Board Level Connection Diagram for DQS Cleaning

- **tA**: I/O output delay
- **tB**: Package bonding wire delay
- **tC**: Package board delay
- **tD**: Board trace delay
- **tE**: I/O input delay
- **tDL**: delay line delay
- **tAC**: minimum CK-to-DQS timing of LPDDR/DDR2 memory spec. (LPDDR ≈ 1ns, DDR2 ≈ 0.5tCK)
- **tFS**: Fine step delay in DLL, From **PhyStatus0**.ctrl_lock_value[9:0], tFS is calculated.
  - If ctrl_half = 0, tFS = tCK / ctrl_lock_value[9:0].
  - **If ctrl_half = 1, tFS = tCK*0.5 / ctrl_lock_value[9:0] ctrl_shiftc** controls PVT-independent delay amount(tF) and **ctrl_offsetc** controls PVT-dependent delay amount(tV).

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Delay line programming value; tDL ≈tAC + 2*(tB+tC+tD).

tDL = tF (ctrl_shiftc[2:0]) + tV (ctrl_offsetc[6:0])

If ctrl_shiftc[2:0] is 3'b100, tF is Tperiod/8 ≈ 0.9375ns. (If tCK is 7.5ns)

If ctrl_offsetc[6:0] is 7'b00010_00, tV is 0.320ns(40ps * 8) @ worst case (if tFS = 40ps)

Therefore tDL = tF + tV = 0.9375ns + 0.320ns = 1.2575ns

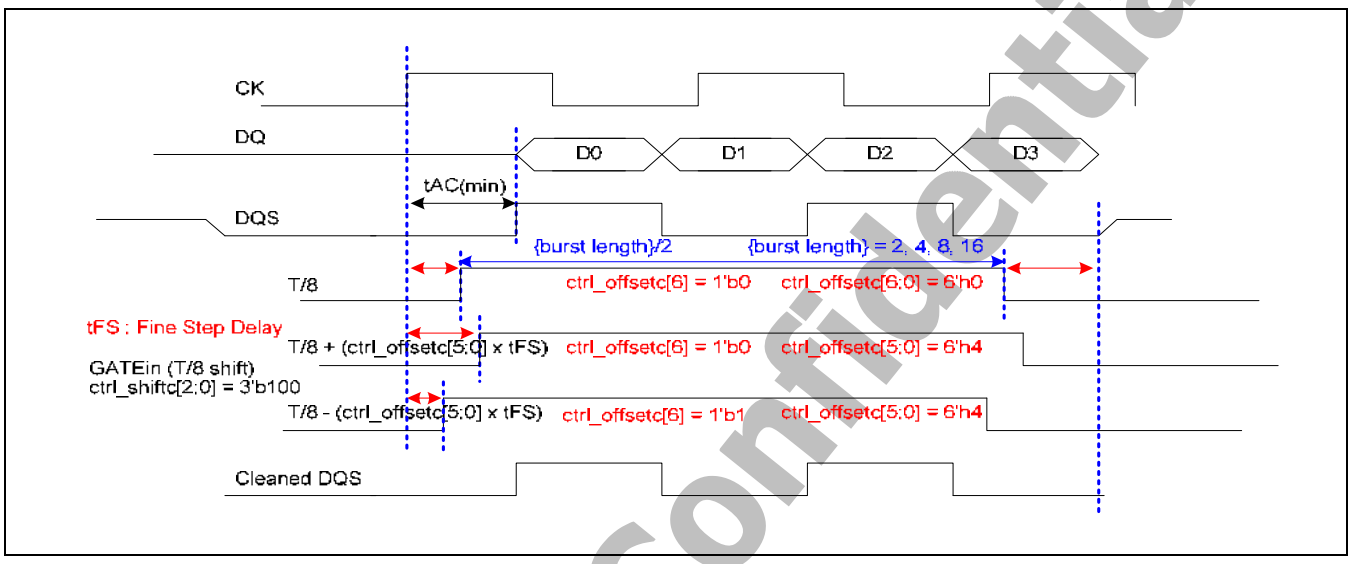

Figure 1-13 DQS Cleaning for LPDDR if tAC Min

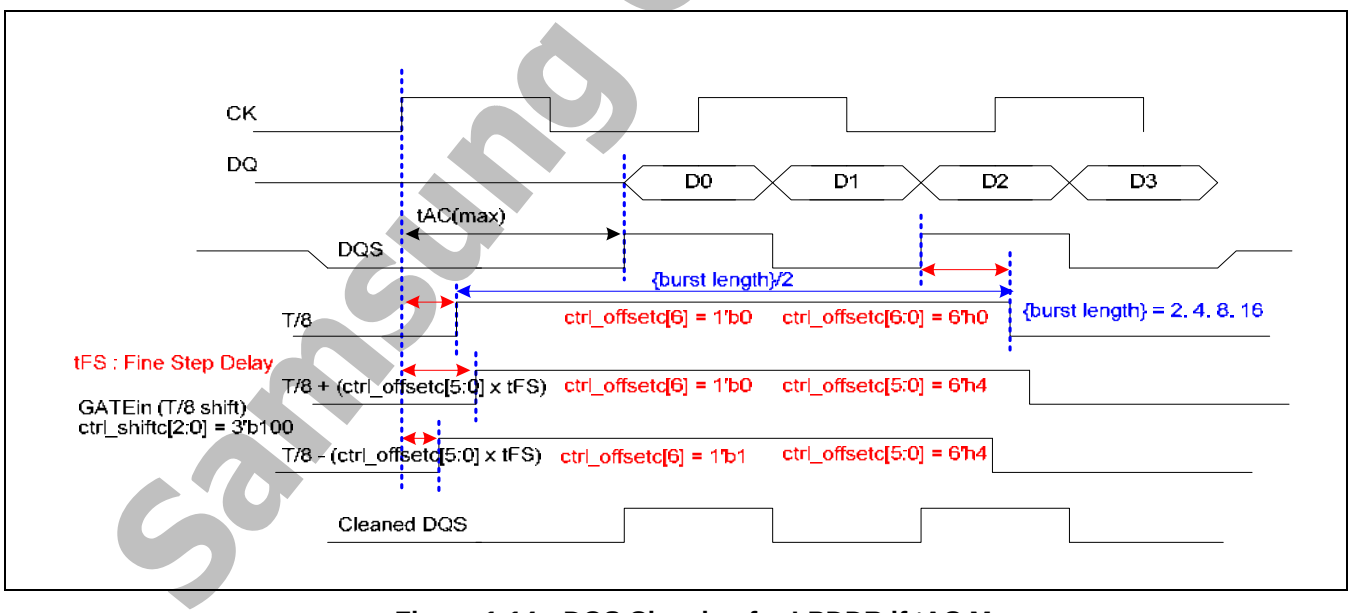

Figure 1-14 DQS Cleaning for LPDDR if tAC Max

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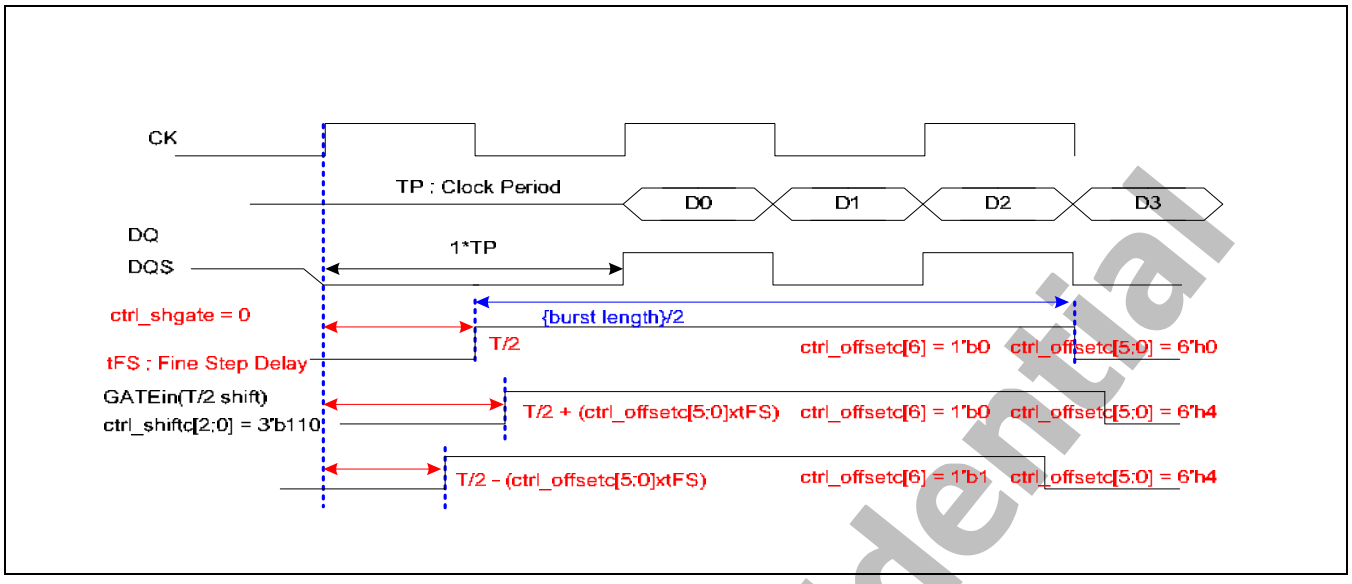

Figure 1-15 DQS cleaning for DDR2

1.4.1.9 Dynamic Power Down Configuration Register (PwrdnConfig, R/W, Address = 0xF000_0028, 0xF140_0028)

PWRDNCONFIG	Bit	Description	R/W	Initial State
dsref_cyc	[31:16]	Number of Cycles for Dynamic Self Refresh Entry 0xn = n aclk cycles, If the command queue is empty for n+1 cycles, the controller forces the memory device into self refresh state. Refer to "*1.2.3.3 . Dynamic Self Refresh*".	R/W	0xFFFF
Reserved	[15:8]	Should be zero		0x0
dpwrdn_cyc	[7:0]	Number of Cycles for Dynamic Power Down Entry 0xn = n aclk cycles, If the command queue is empty for n+1 cycles, the controller forces the memory device into active/ precharge power down state. Refer to *"1.2.3.2 Dynamic Power Down"*.	R/W	0xFF

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1.4.1.10 AC Timing Register for Auto Refresh of memory (TimingAref, R/W, Address = 0xF000_0030, 0xF140_0030)

TIMINGAREF	Bit	Description	R/W	Initial State
Reserved	[31:16]	Should be zero		0x0
t_refi	[15:0]	Average Periodic Refresh Interval Should be minimum memory tREFI (all bank) < t_refi * T(mclk), For example, for the all bank refresh period of 7.8us, and an mclk frequency of 133MHz, the following value should be programmed : 7.8 us * 133 MHz = 1038	R/W	0x40E

1.4.1.11 AC Timing Register for the Row of memory (TimingRow, R/W, Address = 0xF000_0034, 0xF140_0034)

TIMINGROW	Bit	Description	R/W	Initial State
t_rfc	[31:24]	Auto refresh to Active / Auto refresh command period, in cycles t_rfc * T(mclk) should be greater than or equal to the minimum value of memory tRFC.	R/W	0xF
t_rrd	[23:20]	Active bank A to Active bank B delay, in cycles t_rrd * T(mclk) should be greater than or equal to the minimum value of memory tRRD.	R/W	0x2
t_rp	[19:16]	Precharge command period, in cycles t_rp * T(mclk) should be greater than or equal to the minimum value of memory tRP.	R/W	0x3
t_rcd	[15:12]	Active to Read or Write delay, in cycles t_rcd * T(mclk) should be greater than or equal to the minimum value of memory tRCD	R/W	0x3
t_rc	[11:6]	Active to Active period, in cycles t_rc * T(mclk) should be greater than or equal to the minimum value of memory tRC.	R/W	0xA
t_ras	[5:0]	Active to Precharge command period, in cycles t_ras * T(mclk) should be greater than or equal to the minimum value of memory tRAS.	R/W	0x6

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1.4.1.12 AC Timing Register for the Data of memory (TimingData, R/W, Address = 0xF000_0038, 0xF140_0038)

TIMINGDATA	Bit	Description	R/W	Initial State
t_wtr	[31:28]	Internal write to Read command delay, in cycles t_wtr * T(mclk) should be greater than or equal to the minimum value of memory tWTR.	R/W	0x1
t_wr	[27:24]	Write recovery time, in cycles t_wr * T(mclk) should be greater than or equal to the minimum value of memory tWR	R/W	0x2
t_rtp	[23:20]	Internal read to Precharge command delay, in cycles t_rtp * T(mclk) should be greater than or equal to the minimum value of memory tRTP.	R/W	0x1
cl	[19:16]	CAS Latency (for LPDDR/DDR/DDR2), in cycles cl should be greater than or equal to the minimum value of memory CL.	R/W	0x3
Reserved	[15:12]	Should be zero		0x0
wl	[11:8]	Write data latency (for only LPDDR2), in cycles wl should be greater than or equal to the minimum value of memory WL	R/W	0x2
Reserved	[7:4]	Should be zero		0x0
rl	[3:0]	Read data latency (for only LPDDR2), in cycles rl should be greater than or equal to the minimum value of memory RL	R/W	0x4

NOTE: * tDAL (Auto precharge write recovery + precharge time) = t_wr + t_rp (automatically calculated)

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1.4.1.13 AC Timing Register for the Power mode of Memory (TimingPower, R/W, Address = 0xF000_003C, 0xF140_003C)

TIMINGPOWER	Bit	Description	R/W	Initial State
Reserved	[31:30]	Should be zero		0x0
t_faw	[29:24]	Four Active Window t_faw * T(mclk) should be greater than or equal to the minimum value of memory tFAW	R/W	0xE
t_xsr	[23:16]	Self refresh exit power down to next valid command delay, in cycles t_xsr * T(mclk) should be greater than or equal to the minimum value of memory tXSR. In case of DDR/DDR2, this value should be greater than or equal to the minimum value of memory tXSRD.	R/W	0x1B
t_xp	[15:8]	Exit power down to next valid command delay, in cycles t_xp * T(mclk) should be greater than or equal to the minimum value of memory tXP	R/W	0x4
t_cke	[7:4]	CKE minimum pulse width (minimum power down mode duration), in cycles t_cke should be greater than or equal to the minimum value of memory tCKE	R/W	0x2
t_mrd	[3:0]	Mode Register Set command period, in cycles t_mrd should be greater than or equal to the minimum value of memory tMRD.	R/W	0x2

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1.4.1.14 PHY Status Register (PhyStatus, Read Only, Address=0xF000_0040, 0xF140_0040)

PHYSTATUS0	Bit	Description	R/W	Initial State
Reserved	[31:14]	Should be zero		0x0
ctrl_lock_value	[13:4]	Locked Delay Locked delay line encoding value ctrl_lock_value[9:2]: number of delay cells for coarse lock ctrl_lock_value[1:0]: control value for fine lock	R	0x0
Reserved	[3]	Should be zero		0x0
ctrl_locked	[2]	DLL Lock 0 = Unlocks DLL 1 = Locks DLL	R	0x0
ctrl_flock	[1]	Fine Lock Information It is indicated that DLL is locked with fine resolution, “phase offset error” is less than 80ps.	R	0xX
ctrl_clock	[0]	Coarse Lock Information It is indicated that DLL changes step delays of the “delay line” and “phase offset error” is less than 160ps.	R	0xX

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1.4.1.15 Memory Chip0 Status Register (Chip0Status, Read Only, Address = 0xF000_0048, 0xF140_0048)

CHIP0STATUS	Bit	Description	R/W	Initial State
bank7_state	[31:28]	The current state of bank 7 of memory chip0	R	0x0
bank6_state	[27:24]	The current state of bank 6 of memory chip0	R	0x0
bank5_state	[23:20]	The current state of bank 5 of memory chip0	R	0x0
bank4_state	[19:16]	The current state of bank 4 of memory chip0	R	0x0
bank3_state	[15:12]	The current state of bank 3 of memory chip0	R	0x0
bank2_state	[11:8]	The current state of bank 2 of memory chip0	R	0x0
bank1_state	[7:4]	The current state of bank 1 of memory chip0	R	0x0
bank0_state	[3:0]	The current state of bank 0 of memory chip0 0x0 = Idle (precharged) 0x1 = MRS/EMRS 0x2 = Deep power down 0x3 = Self refresh 0x4 = Auto refresh 0x5 = Precharge power down 0x6 = Row active 0x7 = Active power down 0x8 = Write 0x9 = Write with auto precharge 0xA = Read 0xB = Read with auto precharge 0xC = Burst stop 0xD = Precharging 0xE = MRR 0xF = Reserved	R	0x0

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1.4.1.16 Memory Chip1 Status Register (Chip1Status, Read Only, Address=0xF000_004C, 0xF140_004C)

CHIP1STATUS	Bit	Description	R/W	Initial State
bank7_state	[31:28]	The current state of bank 7 of SDRAM chip1	R	0x0
bank6_state	[27:24]	The current state of bank 6 of SDRAM chip1	R	0x0
bank5_state	[23:20]	The current state of bank 5 of SDRAM chip1	R	0x0
bank4_state	[19:16]	The current state of bank 4 of SDRAM chip1	R	0x0
bank3_state	[15:12]	The current state of bank 3 of SDRAM chip1	R	0x0
bank2_state	[11:8]	The current state of bank 2 of SDRAM chip1	R	0x0
bank1_state	[7:4]	The current state of bank 1 of SDRAM chip1	R	0x0
bank0_state	[3:0]	The current state of bank 0 of SDRAM chip1 0x0 = Idle (precharged) 0x1 = MRS/EMRS 0x2 = Deep power down 0x3 = Self refresh 0x4 = Auto refresh 0x5 = Precharge power down 0x6 = Row active 0x7 = Active power down 0x8 = Write 0x9 = Write with auto precharge 0xA = Read 0xB = Read with auto precharge 0xC = Burst stop 0xD = Precharging 0xE = MRR 0xF = Reserved	R	0x0

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1.4.1.17 Counter Status Register for the Auto Refresh (ArefStatus, R, Address=0xF000_0050, 0xF140_0050)

AREFSTATUS	Bit	Description	R/W	Initial State
Reserved	[31:16]	Should be zero		0x0
aref_cnt	[15:0]	Current Value of Auto Refresh Counter Shows the current value of all bank auto refresh counter. This is updated if a new t_refi is programmed into the TimingAref register and decreases by 1 at the rising edge of mclk. An all bank auto refresh command is issued to memory device and this counter is reloaded with TimingAref.t_ref if this becomes zero.	R	0xFFFF

1.4.1.18 Memory Mode Registers Status Register (MrStatus, Read Only, Address = 0xF000_0054, 0xF140_0054)

MRSTATUS	Bit	Description	R/W	Initial State
Reserved	[31:8]	Should be zero		0x0
mr_status	[7:0]	Mode Registers Status	R	0x0

1.4.1.19 PHY Test Register 0 (PhyTest0, R/W, Address = 0xF000_0058, 0xF140_0058)

PHYTEST0	Bit	Description	R/W	Initial State
ctrl_fb_cnt4	[31:24]	Count Value for Control Channel	R	0x0
Reserved	[23:21]	Should be zero		0x0
ctrl_fb_oky	[20:16]	ctrl_fb_okay[4] : Error status for control, ctrl_fb_okay[3:0] : Error status for data	R	0x0
Reserved	[15:13]	Should be zero		0x0
ctrl_fb_err	[12:8]	ctrl_fb_err[4] : Error for control, ctrl_fb_err[3:0] : Error for data	R	0x0
Reserved	[7:5]	Should be zero		0x0
ctrl_fb_start	[4:0]	ctrl_fb_start[4] : Start for control, ctrl_fb_start[3:0] : Start for data	R/W	0x0

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1.4.1.20 PHY Test Register 1 (PhyTest1, R, Address = 0xF000_005C, 0xF140_005C)

PHYTEST1	Bit	Description	R/W	Initial State
ctrl_fb_cnt3	[31:24]	Count value for data3 channel	R	0x0
ctrl_fb_cnt2	[23:16]	Count value for data2 channel	R	0x0
ctrl_fb_cnt1	[15:8]	Count value for data1 channels	R	0x0
ctrl_fb_cnt0	[7:0]	Count value for data0 channel	R	0x0

1.4.1.21 Quality of Service Control Register n (QosControl n, R/W, Address = 0xF000_0060 + 8n (n=0~15, integer), 0xF140_0060 + 8n (n=0~15, integer)

QOSCONTROLn	Bit	Description	R/W	Initial State
Reserved	[31:28]	Should be zero		0x0
qos_cnt	[27:16]	QoS Cycles 0xn = n aclk cycles The matched ARID/AWID uses this value for its timeout counters instead of ConControl.timeout_cnt.	R/W	0x0
qos_cnt_f	[15:4]	QoS cycles for fast request 0xn = n aclk cycles When Concontrol.qos_fast_en is enabled and input pin qos_fast[n] bit is 1, this qos_cnt_f value is loaded to the timeout counter.	R/W	0x0
Reserved	[3:1]	Should be zero		0x0
qos_en	[0]	QoS Enable 0x0 = Disable 0x1 = Enable If this function is enabled, its timeout counter works and the ARID/AWID is masked with QoSConfig.qos_mask and compared with QoSConfig.qos_id	R/W	0x0

NOTE: If qos fast is enabled, the QoSControl(n) of 4,5,6,7,8,9,10,11,13,14 & 15 are dedicated to each specific IP that is refer to *Table 1-1*.

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1.4.1.22 Quality of Service Configuration Register n (QosConfig n, R/W, Address = 0xF000_0064 + 8n (n=0~15, integer), 0xF140_0064 + 8n (n=0~15, integer)

QOSCONFIGn	Bit	Description	R/W	Initial State
qos_mask	[31:16]	QoS Mask Bits This is used to mask the incoming ARID/AWID to compare with the qos_id. For example, to have 0b00110XX000 IDs the same QoS, the 4th and 5th bits must be masked. Therefore, qos_mask would be 0b1111100111.	R/W	0x0
qos_id	[15:0]	QoS ID This is used to compare with the masked ARID/AWID to check whether its timeout counter should be used for QoS. After applying the qos_mask to these ARID/AWID, it is compared with qos_id. The qos_id would be 0b001100_0000 using the example above. Comparing the masked ID, if the result is equal to the qos_id, then the QoSControl0.qos_cnt is applied to this ARID/AWID transaction for timeout. Don't care bits must be assigned zeros.	R/W	0x0

NOTE: If qos fast is enabled, the QoSConfig(n) of 4,5,6,7,8,9,10,11,13,14 & 15 are dedicated to each specific IP, and it's qos_id & qos_mask value should be set proper to each IP's Transaction ID

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Table 1-2 Master Transaction ID for DMC0 in S5PV210

Transaction Master	R/W	Transaction ID	Description
ARM	R/W	14'b000_0000_0xxx_x000	
MFC	R/W	14'b000_000x_xxx0_0001	
G3D	R/W	14'b000_000x_xxx1_0001	
FIMC0	R/W	14'b00x_xxx0_0000_0010	
FIMC1	R/W	14'b00x_xxx0_0100_0010	
FIMC2	R/W	14'b00x_xxx0_1000_0010	
JPEG	R/W	14'b000_0000_1100_0010	
ROT	R/W	14'b000_0001_0000_0010	
FIMD_W0	R/W	14'b000_0000_0001_0010	FIMD window 0
FIMD_W4	R/W	14'b000_0001_0001_0010	FIMD window 4
FIMD_W1	R/W	14'b000_0000_0101_0010	FIMD window 1
FIMD_W2	R/W	14'b000_0001_0101_0010	FIMD window 2
FIMD_W3	R/W	14'b000_0010_0101_0010	FIMD window 3
G2D	R/W	14'b000_xxxx_1001_0010	
VP	R/W	14'b000_0xxx_x010_0010	
MIXER_GRP0	R/W	14'b000_0000_0110_0010	
MIXER_GRP1	R/W	14'b000_0000_1110_0010	
SSYS	R/W	14'b000_0000_0011_0010	
GSYS	R/W	14'b000_0000_0111_0010	
ESYS0	R/W	14'b000_0000_1011_0010	
ESYS1	R/W	14'b000_0000_1111_0010	
CSYS	R/W	14'b000_0001_0011_0010	
USYS	R/W	14'b000_0001_0111_0010	
AUDIO	R/W	14'b000_0001_1011_0010	
PDMA0	R/W	14'b0xx_xx01_1111_0010	
PDMA1	R/W	14'b0xx_xx11_1111_0010	
MDMA	R/W	14'b000_00xx_xx11_1010	

NOTE: Transaction ID in S5PV210

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Table 1-3 Master Transaction ID for DMC1 in S5PV210

Transaction Master	R/W	Transaction ID	Description
ARM	R/W	14'b000_0000_0xxx_x000	
MFC	R/W	14'b000_000x_xxx0_1100	
G3D	R/W	14'b000_000x_xxx1_0100	
FIMC0	R/W	14'b00x_xxx0_0000_1011	
FIMC1	R/W	14'b00x_xxx0_0100_1011	
FIMC2	R/W	14'b00x_xxx0_1000_1011	
JPEG	R/W	14'b000_0000_1100_1011	
ROT	R/W	14'b000_0001_0000_1011	
FIMD_W0	R/W	14'b000_0000_0001_1011	FIMD window 0
FIMD_W4	R/W	14'b000_0001_0001_1011	FIMD window 4
FIMD_W1	R/W	14'b000_0000_0101_1011	FIMD window 1
FIMD_W2	R/W	14'b000_0001_0101_1011	FIMD window 2
FIMD_W3	R/W	14'b000_0010_0101_1011	FIMD window 3
G2D	R/W	14'b000_xxxx_1001_0011	
VP	R/W	14'b000_0xxx_x010_1011	
MIXER_GRP0	R/W	14'b000_0000_0110_1011	
MIXER_GRP1	R/W	14'b000_0000_1110_1011	
SSYS	R/W	14'b000_0000_0011_0011	
GSYS	R/W	14'b000_0000_0111_0011	
ESYS0	R/W	14'b000_0000_1011_0011	
ESYS1	R/W	14'b000_0000_1111_0011	
CSYS	R/W	14'b000_0001_0011_0011	
USYS	R/W	14'b000_0001_0111_0011	
AUDIO	R/W	14'b000_0001_1011_0011	
PDMA0	R/W	14'b0xx_xx01_1111_0011	
PDMA1	R/W	14'b0xx_xx11_1111_0011	
MDMA	R/W	14'b000_00xx_xx11_1011	

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2 SROM CONTROLLER

2.1 SROM CONTROLLER

2.1.1 OVERVIEW OF SROM CONTROLLER

S5PV210 SROM Controller (SROMC) support external 8 / 16-bit NOR Flash/ PROM/ SRAM memory.

S5PV210 SROM Controller supports 6-bank memory up to maximum 16Mbyte per bank.

2.1.2 KEY FEATURES OF SROM CONTROLLER

- Supports SRAM, various ROMs and NOR flash memory
- Supports only 8 or 16-bit data bus (only 16-bit data bus for BANK0)
- Address space: Up to 16MB per Bank
- Supports 6 banks.
- Fixed memory bank start address
- External wait to extend the bus cycle
- Supports byte and half-word access for external memory

2.1.3 BLOCK DIAGRAM OF SROM CONTROLLER

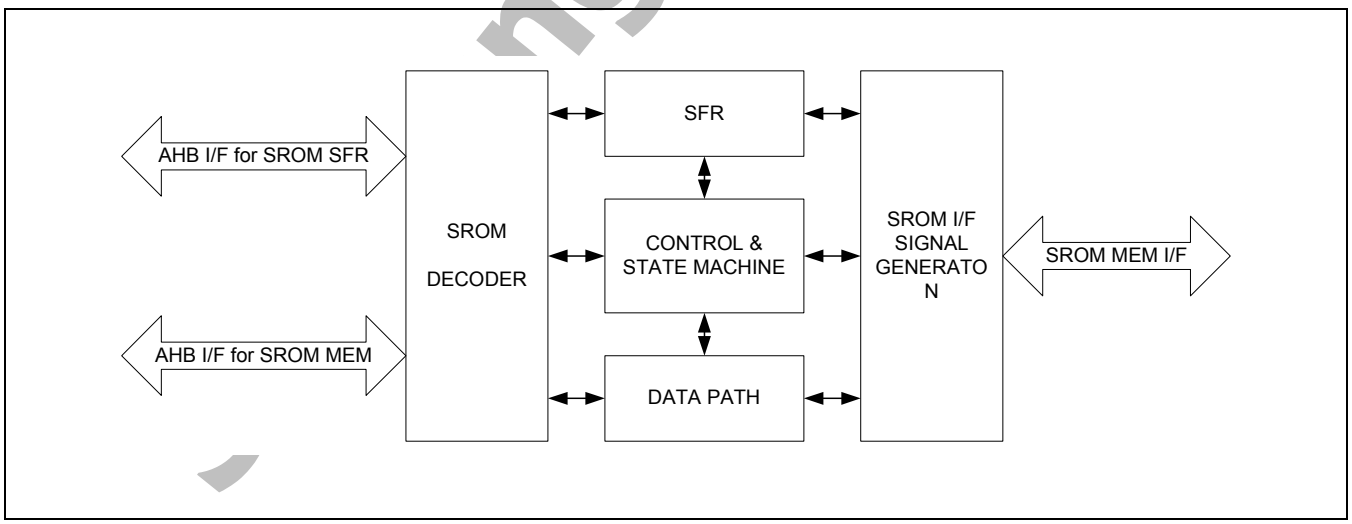

Figure 2-1 Block Diagram of SROM Controller

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2.2 FUNCTIONAL DESCRIPTION

SROM Controller supports SROM interface for Bank0 to Bank5.

2.2.1 NWAIT PIN OPERATION

If the WAIT signal corresponding to each memory bank is enabled, the external nWAIT pin should prolong the duration of nOE while the memory bank is active. nWAIT is checked from tacc-1. nOE will be deasserted at the next clock after sampling nWAIT is high. The nWE signal has the same relation with nOE signal.

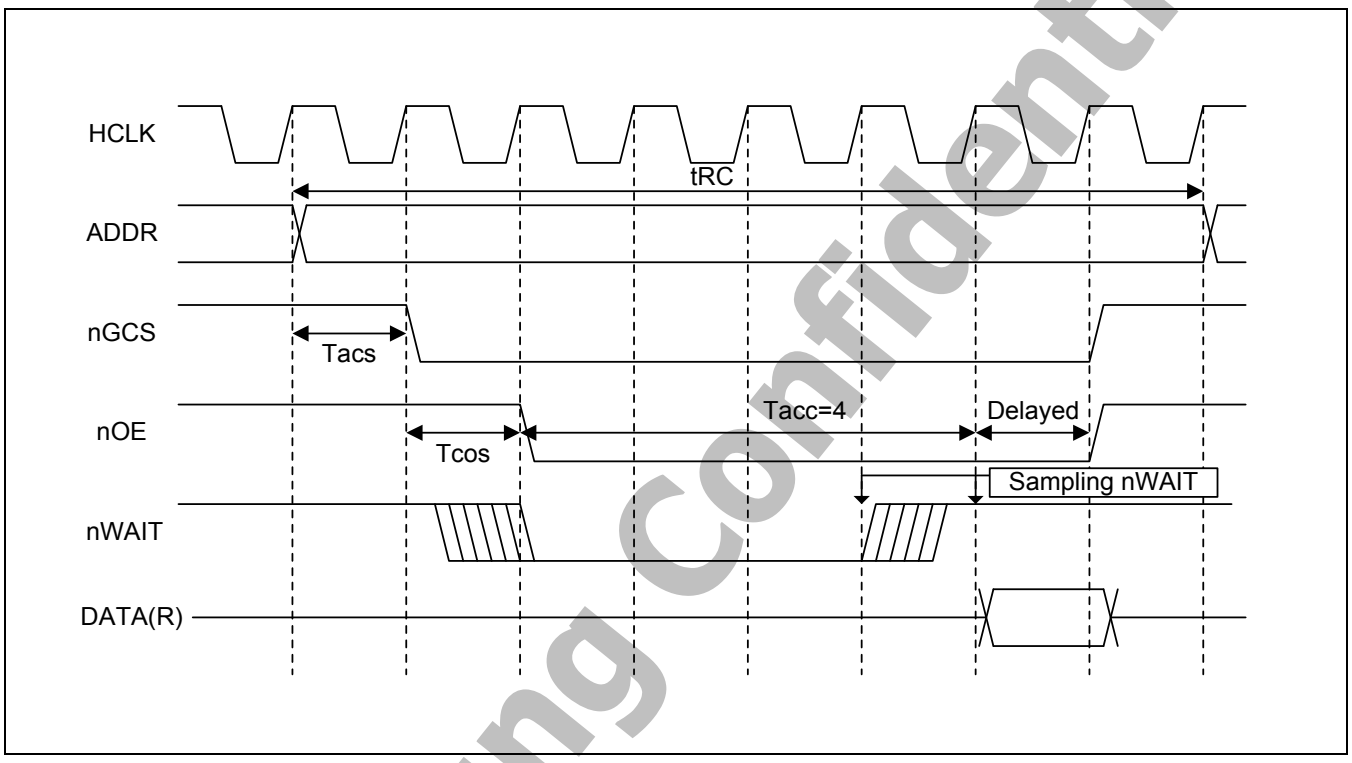

Figure 2-2 SROM Controller nWAIT Timing Diagram

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2.2.2 PROGRAMMABLE ACCESS CYCLE

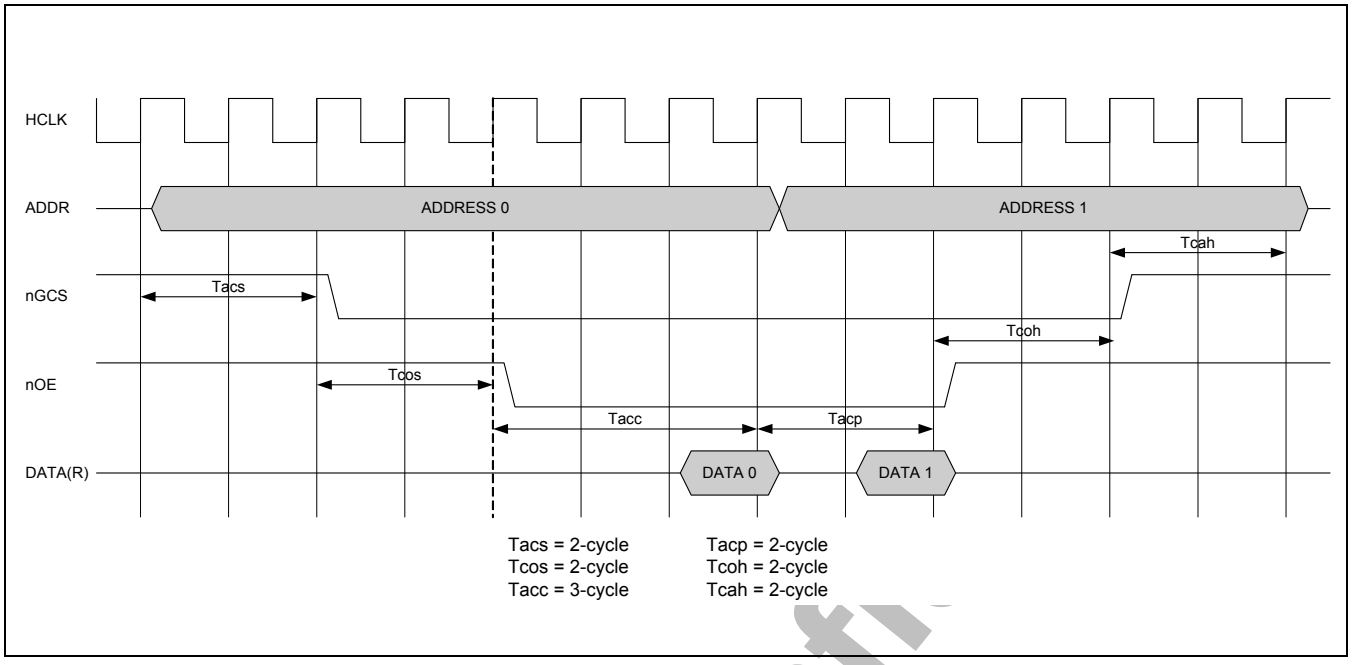

Figure 2-3 SROM Controller Read Timing Diagram

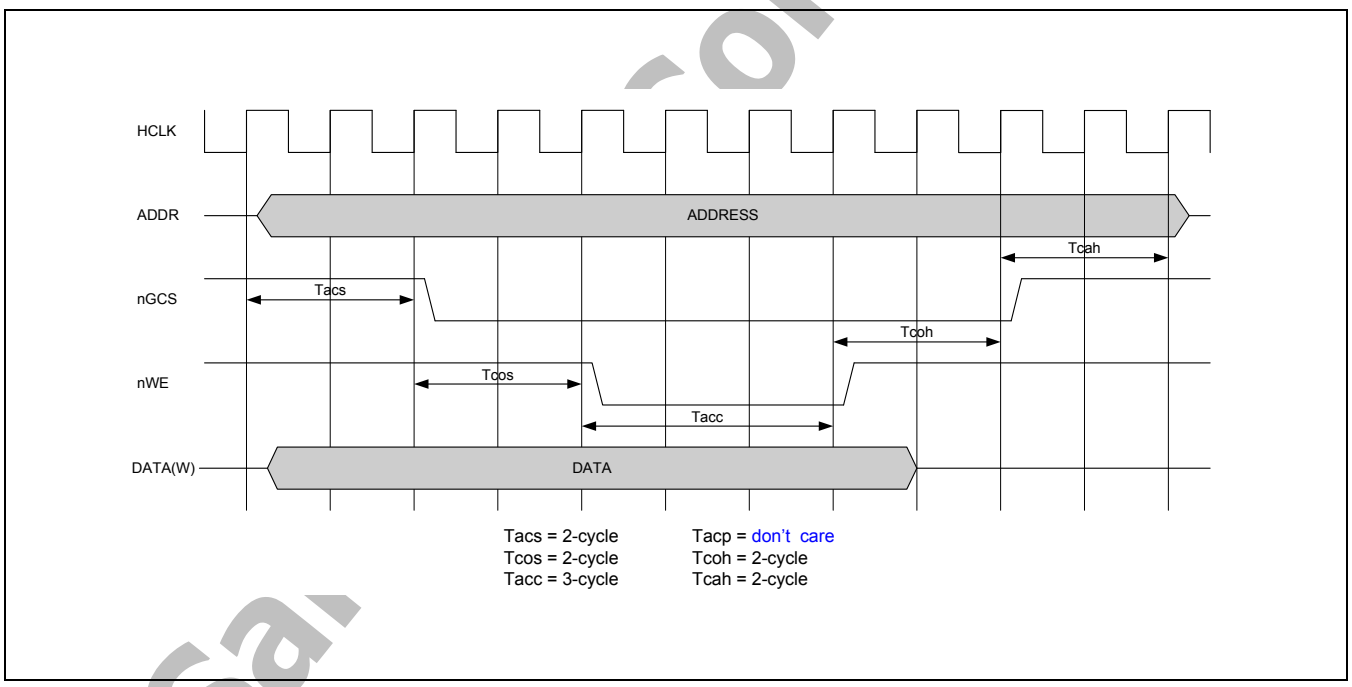

Figure 2-4 SROM Controller Write Timing Diagram

NOTE: Page mode is only supported on read cycle.

2.3 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
nGCS[5:0]	Output	Bank selection signal	Xm0CSn[5:0]	muxed
ADDR[22:0]	Output	SROM Address bus	Xm0ADDR[22:0]	muxed
nOE	Output	SROM Output Enable	Xm0OEn	muxed
nWE	Output	SROM Write Enable	Xm0WEn	muxed
nWBE/nBE [1:0]	Output	SROM Byte write Enable / Byte Enable	Xm0BEn	muxed
DATA[15:0]	In/Out	SROM Data bus	Xm0DATA[15:0]	muxed
nWAIT	Input	SROM Wait input	Xm0WAITn	muxed

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2.4 REGISTER DESCRIPTION

2.4.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
SROM_BW	0xE800_0000	R/W	Specifies the SROM Bus width & wait control	0x0000_0009
SROM_BC0	0xE800_0004	R/W	Specifies the SROM Bank0 control register	0x000F_0000
SROM_BC1	0xE800_0008	R/W	Specifies the SROM Bank1 control register	0x000F_0000
SROM_BC2	0xE800_000C	R/W	Specifies the SROM Bank2 control register	0x000F_0000
SROM_BC3	0xE800_0010	R/W	Specifies the SROM Bank3 control register	0x000F_0000
SROM_BC4	0xE800_0014	R/W	Specifies the SROM Bank4 control register	0x000F_0000
SROM_BC5	0xE800_0018	R/W	Specifies the SROM Bank5 control register	0x000F_0000

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2.4.1.1 SROM Bus Width & Wait Control Register (SROM_BW, R/W, Address = 0x0000_0000)

SROM_BW	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
ByteEnable5	[23]	nWBE / nBE(for UB/LB) control for Memory Bank5 0 = Not using UB/LB (XrnWBE[1:0] is dedicated nWBE[1:0]) 1 = Using UB/LB (XrnWBE[1:0] is dedicated nBE[1:0]	0
WaitEnable5	[22]	Wait enable control for Memory Bank5 0 = Disables WAIT 1 = Enables WAIT	0
AddrMode5	[21]	Select SROM ADDR Base for Memory Bank5 0 = SROM_ADDR is Half-word base address. (SROM_ADDR[22:0] <= HADDR[23:1]) 1 = SROM_ADDR is byte base address (SROM_ADDR[22:0] <= HADDR[22:0]) Note: When DataWidth5 is “0”, SROM_ADDR is byte base address. (Ignored this bit.)	0
DataWidth5	[20]	Data bus width control for Memory Bank5 0 = 8-bit 1 = 16-bit	0
ByteEnable4	[19]	nWBE / nBE(for UB/LB) control for Memory Bank4 0 = Not using UB/LB (XrnWBE[1:0] is dedicated nWBE[1:0]) 1 = Using UB/LB (XrnWBE[1:0] is dedicated nBE[1:0]	0
WaitEnable4	[18]	Wait enable control for Memory Bank4 0 = Disables WAIT 1 = Enables WAIT	0
AddrMode4	[17]	Select SROM ADDR Base for Memory Bank4 0= SROM_ADDR is Half-word base address. (SROM_ADDR[22:0] <= HADDR[23:1]) 1= SROM_ADDR is byte base address (SROM_ADDR[22:0] <= HADDR[22:0]) Note: When DataWidth4 is “0”, SROM_ADDR is byte base address. (Ignored this bit.)	0
DataWidth4	[16]	Data bus width control for Memory Bank4 0 = 8-bit 1 = 16-bit	0
ByteEnable3	[15]	nWBE / nBE(for UB/LB) control for Memory Bank3 0 = Not using UB/LB (XrnWBE[1:0] is dedicated nWBE[1:0]) 1 = Using UB/LB (XrnWBE[1:0] is dedicated nBE[1:0]	0
WaitEnable3	[14]	Wait enable control for Memory Bank3 0 = Disables WAIT 1 = Enables WAIT	0
AddrMode3	[13]	Select SROM ADDR Base for Memory Bank3 0 = SROM_ADDR is Half-word base address. (SROM_ADDR[22:0] <= HADDR[23:1]) 1 = SROM_ADDR is byte base address	0

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SROM_BW	Bit	Description	Initial State
		(SROM_ADDR[22:0] <= HADDR[22:0]) Note: When DataWidth3 is “0”, SROM_ADDR is byte base address. (Ignored this bit.)	
DataWidth3	[12]	Data bus width control for Memory Bank3 0 = 8-bit 1 = 16-bit	0
ByteEnable2	[11]	nWBE / nBE(for UB/LB) control for Memory Bank2 0 = Not using UB/LB (XrnWBE[1:0] is dedicated nWBE[1:0]) 1 = Using UB/LB (XrnWBE[1:0] is dedicated nBE[1:0]	0
WaitEnable2	[10]	Wait enable control for Memory Bank2 0 = Disables WAIT 1 = Enables WAIT	0
AddrMode2	[9]	Select SROM ADDR Base for Memory Bank2 0 = SROM_ADDR is Half-word base address. (SROM_ADDR[22:0] <= HADDR[23:1]) 1 = SROM_ADDR is byte base address (SROM_ADDR[22:0] <= HADDR[22:0]) Note: When DataWidth2 is “0”, SROM_ADDR is byte base address. (Ignored this bit.)	0
DataWidth2	[8]	Data bus width control for Memory Bank2 0 = 8-bit 1 = 16-bit	0
ByteEnable1	[7]	nWBE / nBE(for UB/LB) control for Memory Bank1 0 = Not using UB/LB (XrnWBE[1:0] is dedicated nWBE[1:0]) 1 = Using UB/LB (XrnWBE[1:0] is dedicated nBE[1:0]	0
WaitEnable1	[6]	Wait enable control for Memory Bank1 0 = Disables WAIT 1 = Enables WAIT	0
AddrMode1	[5]	Select SROM ADDR Base for Memory Bank1 0 = SROM_ADDR is Half-word base address. (SROM_ADDR[22:0] <= HADDR[23:1]) 1 = SROM_ADDR is byte base address (SROM_ADDR[22:0] <= HADDR[22:0]) Note: When DataWidth1 is “0”, SROM_ADDR is byte base address. (Ignored this bit.)	0
DataWidth1	[4]	Data bus width control for Memory Bank1 0 = 8-bit 1 = 16-bit	0
ByteEnable0	[3]	nWBE / nBE(for UB/LB) control for Memory Bank0 0 = Not using UB/LB (XrnWBE[1:0] is dedicated nWBE[1:0]) 1 = Using UB/LB (XrnWBE[1:0] is dedicated nBE[1:0]	1
WaitEnable0	[2]	Wait enable control for Memory Bank0 0 = Disables WAIT 1 = Enables WAIT	0

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SROM_BW	Bit	Description	Initial State
AddrMode0	[1]	Select SROM ADDR Base for Memory Bank0 0 = SROM_ADDR is Half-word base address. (SROM_ADDR[22:0] <= HADDR[23:1]) 1 = SROM_ADDR is byte base address (SROM_ADDR[22:0] <= HADDR[22:0]) Note: When DataWidth0 is “0”, SROM_ADDR is byte base address. (Ignored this bit.)	0
DataWidth0	[0]	Data bus width control for Memory Bank0 1 = 16-bit Note: Only 16bit for bank0, can’t change	1

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2.4.1.2 SROM Bank Control Register (SROM_BC: XrCSn0 ~ XrCSn2)

- SROM_BC0, R/W, Address = 0xE800_0004
- SROM_BC1, R/W, Address = 0xE800_0008
- SROM_BC2, R/W, Address = 0xE800_000C
- SROM_BC3, R/W, Address = 0xE800_0010
- SROM_BC4, R/W, Address = 0xE800_0014
- SROM_BC5, R/W, Address = 0xE800_0018

SROM_BCn	Bit	Description	Initial State
Tacs	[31:28]	Adress set-up before nGCS 0000 = 0 clock 0001 = 1 clocks 0010 = 2 clocks 0011 = 3 clocks …… 1100 = 12 clocks 1101 = 13 clocks 1110 = 14 clocks 1111 = 15 clocks Note: More 1~2 cycles according to bus i/f status	0000
Tcos	[27:24]	Chip selection set-up before nOE 0000 = 0 clock 0001 = 1 clocks 0010 = 2 clocks 0011 = 3 clocks …… 1100 = 12 clocks 1101 = 13 clocks 1110 = 14 clocks 1111 = 15 clocks	0000
Reserved	[23:21]	Reserved	000
Tacc	[20:16]	Access cycle 00000 = 1 clock 00001 = 2 clocks 00001 = 3 clocks 00010 = 4 clocks …… 11100 = 29 clocks 11101 = 30 clocks 11110 = 31 clocks 11111 = 32 clocks	01111

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SROM_BCn	Bit	Description	Initial State
Tcoh	[15:12]	Chip selection hold on nOE 0000 = 0 clock 0001 = 1 clocks 0010 = 2 clocks 0011 = 3 clocks ……. 1100 = 12 clocks 1101 = 13 clocks 1110 = 14 clocks 1111 = 15 clocks	0000
Tcah	[11:8]	Address holding time after nGCSn 0000 = 0 clock 0001 = 1 clocks 0010 = 2 clocks 0011 = 3 clocks ……. 1100 = 12 clocks 1101 = 13 clocks 1110 = 14 clocks 1111 = 15 clocks Note: More 1~2 cycles according to bus i/f status	0000
Tacp	[7:4]	Page mode access cycle @ Page mode 0000 = 0 clock 0001 = 1 clocks 0010 = 2 clocks 0011 = 3 clocks ……. 1100 = 12 clocks 1101 = 13 clocks 1110 = 14 clocks 1111 = 15 clocks	0000
Reserved	[3:2]	Reserved	
PMC	[1:0]	Page mode configuration 00 = Normal (1 data) 01 = 4 data 10 = Reserved 11 = Reserved	00

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3 ONENAND CONTROLLER

3.1 OVERVIEW OF ONENAND CONTROLLER

S5PV210 supports external 16-bit bus for OneNAND and Flex-OneNAND memory devices. The OneNAND controller supports asynchronous and synchronous read/ write bus operations. It also integrates its own dedicated DMA engine to accelerate the operations of OneNAND memory device.

3.2 KEY FEATURES OF ONENAND CONTROLLER

The key features of OneNAND controller include:

- Supports data buffering (32-entry read prefetch FIFO and 32-entry posted write FIFO) where necessary, to achieve maximum performance.
- Supports asynchronous FIFOs for matching speed between OneNAND flash memory and AHB system bus interface.
- Supports both asynchronous and synchronous read/ write of the OneNAND flash memory device.
- Programmable burst transfer size of the OneNAND flash memory interface (4, 8, 16, 32, 1024 and continuous).
- Supports 16-bit data path to memory and 32-bit data path to the AHB system bus interface.
- Supports multiple memory devices in the OneNAND family (OneNAND and Flex-OneNAND) with a single bus interface protocol.
- Supports up to two OneNAND devices. All the chip selects are available by default.
- Supports the warm reset function of the OneNAND device.

The advanced features of OneNAND controller include:

- Supports internal dedicated DMA engine to maximize the data transfer speed between OneNAND flash and system memory.

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3.3 CONTROLLER USAGE EXPECTATIONS

The OneNAND controller is designed with the following expectations:

- Supported transfer types are SINGLE/ INCR4/ INCR8/ INCR16 transactions.
- Supported transfer sizes are WORD/ HALFWORD transactions for the OneNAND slave.
- Supported transfer sizes are WORD transactions for the register slave.

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3.4 FUNCTIONAL DESCRIPTION OF ONENAND

By default, the ARM processor directly accesses OneNAND. In addition, internal DMA engine can access OneNAND. For example, the internal DMA engine transfers data between OneNAND DataRAM and system main memory (like DRAM) without wasting the processing power of ARM processor. These additional hardware resources can be utilized to maximize the performance and minimize the usage of ARM processor for OneNAND read/ write/ copy operation.

3.4.1 BLOCK DIAGRAM OF ONENAND CONTROLLER

Figure 3-1 shows the block diagram of OneNAND controller that comprises one AHB slave port (A), one AHB master port (B), and one OneNAND interface port (C).

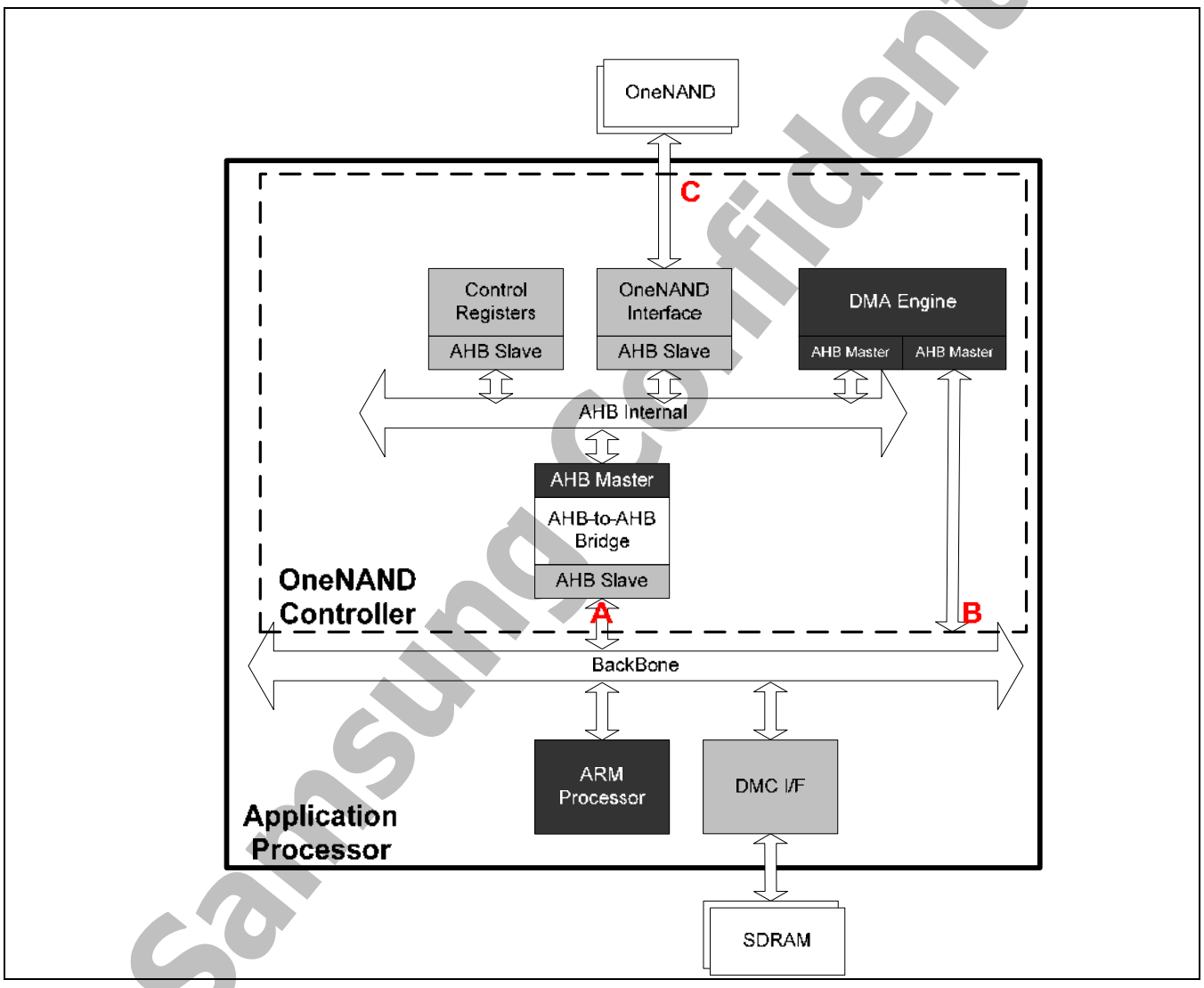

Figure 3-1 OneNAND Controller Block Diagram
(A: AHB Slave Port, B: AHB Master Port, and C: OneNAND Interface Port)

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3.4.2 CLOCK CONTROL

The OneNAND controller has three clock source inputs, namely, HCLK, OA_CLK_OUT, and O_CLK_2X. Bus system interface gets AHB bus clock, HCLK. On the other hand, OneNAND controller core gets one controller clock input, O_CLK_2X. It generates OneNAND memory clock output, OA_CLK_OUT, which is supplied to external OneNAND flash memory. The clock frequency of OA_CLK_OUT is half the clock frequency of O_CLK_2X.

You can set the frequency ratio in special function register (SFR) of the system controller. For more information about clock ratio setting, refer to *Section 2.3, "Clock Controller".*To change the clock frequency ratio, perform these steps:

1. Check OneNAND Read Write Busy (ORWB) bit of OneNAND Interface Status (ONENAND_IF_STATUS) register to ensure there are no memory transfers.
2. Switch the clock ratio in the SFR of system controller.
3. Write to the clock ratio register.
4. Start the memory accesses.

3.4.3 INITIALIZATION PROTOCOL

3.4.3.1 Power On

After power on, the S5PV210 and OneNAND controller are initialized. Thereafter, OneNAND controller will automatically configure itself to work with the OneNAND flash memory devices. This automatic configuration can be achieved using one of the following:

- Mux-type OneNAND or Demux-type OneNAND
- Asynchronous read and write mode
- Read prefetch disabled

3.4.3.2 Boot Code

On initialization, the OneNAND flash device will automatically load boot data in boot buffer.

To access this code, one or more reads to the boot address can be issued. This operation will happen asynchronously until both OneNAND devices and OneNAND controller are configured to run in synchronous mode.

To configure both OneNAND devices and OneNAND controller, update the OneNAND Interface Control (ONENAND_IF_CTRL) register.

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3.5 MEMORY MAP

OneNAND controller occupies 16MB address space in the system address space. The base address of OneNAND controller is configured by 0xB00000000 in S5PV210.

OneNAND controller has three AHB slaves, namely:

1. OneNAND interface

2. Control registers The three AHB slaves share 16MB address space.

OneNAND controller assigns 2MB address space to each AHB slave. Therefore, total 8MB address space is used to address the four AHB slaves. Other 8MB address space is reserved for future use. For more information about address space, refer to *Table 3-1*.

The OneNAND interface provides eight chip-enable (nCE) signals to support up to eight OneNAND devices. As shown in *Table 3-1*, 2MB address space is shared by eight OneNAND devices. *Figure 3-2* shows the data path when OneNAND device is accessed by the external AHB master (like ARM processor).

If AHB address offset from the base address belongs to the bottom 2MB address space, this AHB transaction goes to the OneNAND interface to access the OneNAND device. Each OneNAND device has its own 128KB address space and this 128KB address space is used to address the BootRAM, DataRAM, and registers of the OneNAND device.

As shown in *Figure 3-2*, the ARM processor can access OneNAND device directly through the OneNAND interface. The ARM processor can read or write all OneNAND address area (BootRAM, DataRAM, or registers).

If block erase, page program, and page load operations are required, then the following must be set:

- OneNAND device address registers
  - Start Address 1 (device address offset: 0x1E200)
  - Start Address 2 (device address offset: 0x1E202)
  - Start Address 8 (device address offset: 0x1E20E)

- Start Buffer registers (device address offset: 0x1E400)

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The corresponding commands must be issued to the device command register (Command register (device address offset: 0x1E440)). For more information about the OneNAND device memory map, refer to *Figure 3-3* that shows the data path when the external AHB master accesses control registers.

Table 3-1 OneNAND Controller Memory Map

	OneNAND Controller Address (Start)	OneNAND Controller Address (End)	Window Size	Note
OneNAND Interface	0xB0000000	0xB001FFFF	128KB	OneNAND nCE[0] (For more information about OneNAND Chip #0 address map, refer to *Table 3-3*.
	0xB0020000	0xB003FFFF	128KB	Reserved for future use
	0xB0040000	0xB005FFFF	128KB	OneNAND nCE[1]
	0xB0060000	0xB007FFFF	128KB	Reserved for future use
	0xB0080000	0xB009FFFF	128KB	Reserved for future use
	0xB00A0000	0xB00BFFFF	128KB	Reserved for future use
	0xB00C0000	0xB00DFFFF	128KB	Reserved for future use
	0xB00E0000	0xB00FFFFF	128KB	Reserved for future use
	0xB0100000	0xB011FFFF	128KB	Reserved for future use
	0xB0120000	0xB013FFFF	128KB	Reserved for future use
	0xB0140000	0xB015FFFF	128KB	Reserved for future use
	0xB0160000	0xB017FFFF	128KB	Reserved for future use
	0xB0180000	0xB019FFFF	128KB	Reserved for future use
	0xB01A0000	0xB01BFFFF	128KB	Reserved for future use
	0xB01C0000	0xB01DFFFF	128KB	Reserved for future use
	0xB01E0000	0xB01FFFFF	128KB	Reserved for future use
Reserved	0xB0200000	0xB03FFFFF	2MB	Reserved for future use
Reserved	0xB0400000	0xB05FFFFF	2MB	Reserved for future use
Control Registers	0xB0600000	0xB07FFFFF	2MB	32-bit Registers
Reserved	0xB0800000	0xB0FFFFFF	8MB	Reserved for future use

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Table 3-2 OneNAND Chip #0 (nCE[0]) Address Map
(If the OneNAND device is Connected to nCE[0])

	OneNAND Controller Address (Start)	OneNAND Controller Address (End)	Size (Total 128KBytes)		Description
Main area (64KBytes)	0xB0000000	0xB00001FE	512B	1KB	BootRAM Main sector0
	0xB0000200	0xB00003FE	512B		BootRAM Main sector1
	0xB0000400	0xB00005FE	512B	4KB	DataRAM Main page0/ sector0
	0xB0000600	0xB00007FE	512B		DataRAM Main page0/ sector1
	0xB0000800	0xB00009FE	512B		DataRAM Main page0/ sector2
	0xB0000A00	0xB0000BFE	512B		DataRAM Main page0/ sector3
	0xB0000C00	0xB0000DFE	512B		DataRAM Main page1/ sector0
	0xB0000E00	0xB0000FFE	512B		DataRAM Main page1/ sector1
	0xB0001000	0xB00011FE	512B		DataRAM Main page1/ sector2
	0xB0001200	0xB00013FE	512B		DataRAM Main page1/ sector3
	0xB0001400	0xB000FFFE	59K	59K	Reserved
Spare area (8KBytes)	0xB0010000	0xB001000E	16B	32B	BootRAM Spare sector0
	0xB0010010	0xB001001E	16B		BootRAM Spare sector1
	0xB0010020	0xB001002E	16B	128B	DataRAM Spare page0/ sector0
	0xB0010030	0xB001003E	16B		DataRAM Spare page0/ sector1
	0xB0010040	0xB001004E	16B		DataRAM Spare page0/ sector2
	0xB0010050	0xB001005E	16B		DataRAM Spare page0/ sector3
	0xB0010060	0xB001006E	16B		DataRAM Spare page1/ sector0
	0xB0010070	0xB001007E	16B		DataRAM Spare page1/ sector1
	0xB0010080	0xB001008E	16B		DataRAM Spare page1/ sector2
	0xB0010090	0xB001009E	16B		DataRAM Spare page1/ sector3
	0xB00100A0	0xB0011FFE	8032B	8032B	Reserved
Reserved (24KBytes)	0xB0012000	0xB0017FFE	24KB	24KB	Reserved
Reserved (8KBytes)	0xB0018000	0xB0019FFE	8KB	8KB	Reserved
Reserved (16KBytes)	0xB001A000	0xB001DFFE	16KB	16KB	Reserved
Registers (8KBytes)	0xB001E000	0xB001FFFE	8KB	8KB	Registers

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Table 3-3 Flex-OneNAND Chip #0 (nCE[0]) Address Map (If the Flex-OneNAND device is Connected to nCE[0])

	OneNAND Controller Address (Start)	OneNAND Controller Address (End)	Size (Total 128KBytes)		Description
Main area (64KBytes)	0xB0000000	0xB00001FE	512B	1KB	BootRAM Main sector0
	0xB0000200	0xB00003FE	512B		BootRAM Main sector1
	0xB0000400	0xB00005FE	512B	4KB	DataRAM Main n-th page/ sector0
	0xB0000600	0xB00007FE	512B		DataRAM Main n-th page/ sector1
	0xB0000800	0xB00009FE	512B		DataRAM Main n-th page/ sector2
	0xB0000A00	0xB0000BFE	512B		DataRAM Main n-th page/ sector3
	0xB0000C00	0xB0000DFE	512B		DataRAM Main n-th page/ sector4
	0xB0000E00	0xB0000FFE	512B		DataRAM Main n-th page/ sector5
	0xB0001000	0xB00011FE	512B		DataRAM Main n-th page/ sector6
	0xB0001200	0xB00013FE	512B		DataRAM Main n-th page/ sector7
	0xB0001400	0xB000FFFE	59K	59K	Reserved
Spare area (8KBytes)	0xB0010000	0xB001000E	16B	32B	BootRAM Spare sector0
	0xB0010010	0xB001001E	16B		BootRAM Spare sector1
	0xB0010020	0xB001002E	16B	128B	DataRAM Spare n-th page/ sector0
	0xB0010030	0xB001003E	16B		DataRAM Spare n-th page/ sector1
	0xB0010040	0xB001004E	16B		DataRAM Spare n-th page/ sector2
	0xB0010050	0xB001005E	16B		DataRAM Spare n-th page/ sector3
	0xB0010060	0xB001006E	16B		DataRAM Spare n-th page/ sector4
	0xB0010070	0xB001007E	16B		DataRAM Spare n-th page/ sector5
	0xB0010080	0xB001008E	16B		DataRAM Spare n-th page/ sector6
	0xB0010090	0xB001009E	16B		DataRAM Spare n-th page/ sector7
	0xB00100A0	0xB0011FFE	8032B	8032B	Reserved
Reserved (24KBytes)	0xB0012000	0xB0017FFE	24KB	24KB	Reserved
Reserved (8KBytes)	0xB0018000	0xB0019FFE	8KB	8KB	Reserved
Reserved (16KBytes)	0xB001A000	0xB001DFFE	16KB	16KB	Reserved
Registers (8KBytes)	0xB001E000	0xB001FFFE	8KB	8KB	Registers

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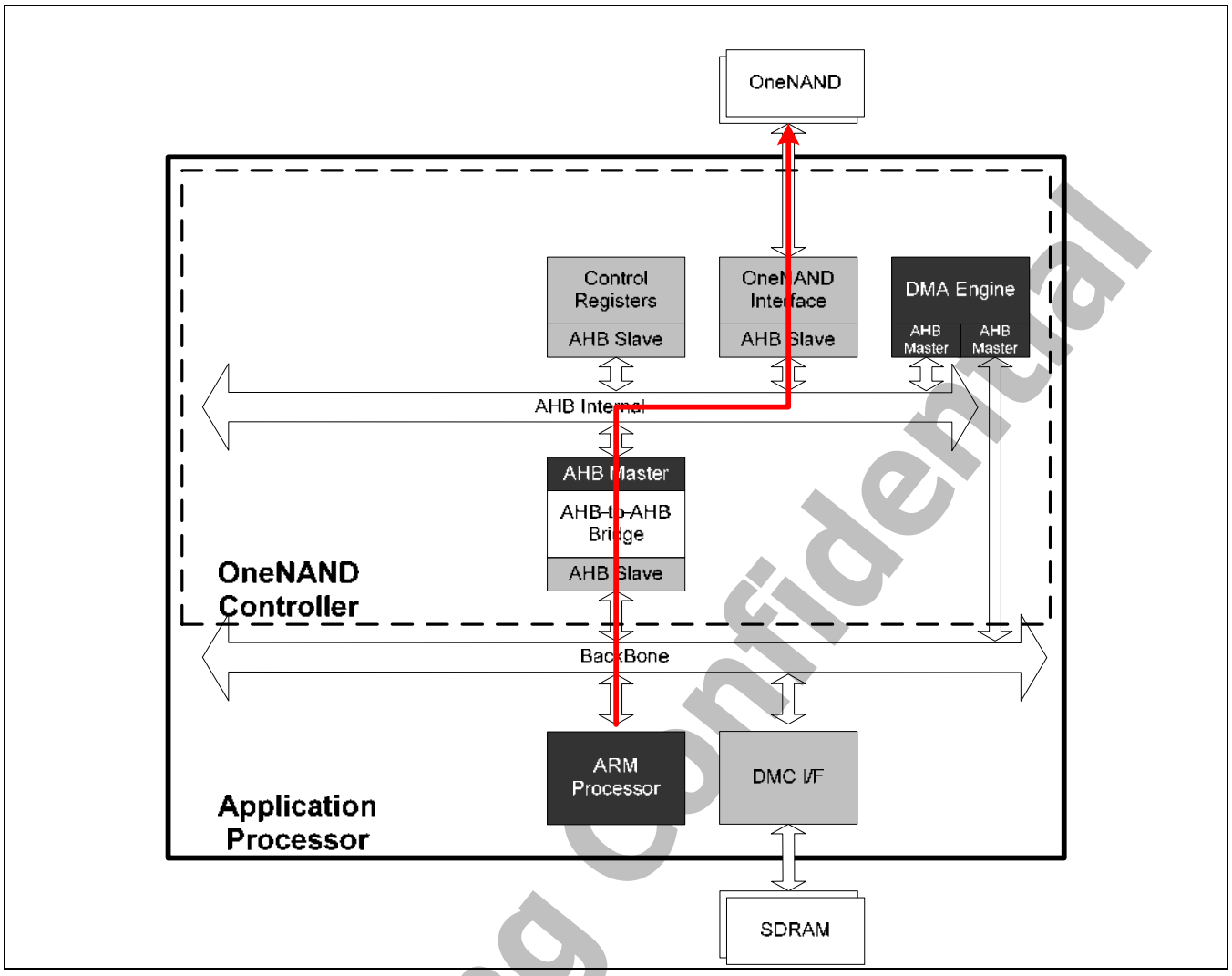

Figure 3-2 OneNAND Accesses (OneNAND Controller Address: 0xB0000000 ~ 0xB01FFFFF) by the External AHB Master (ARM Processor)

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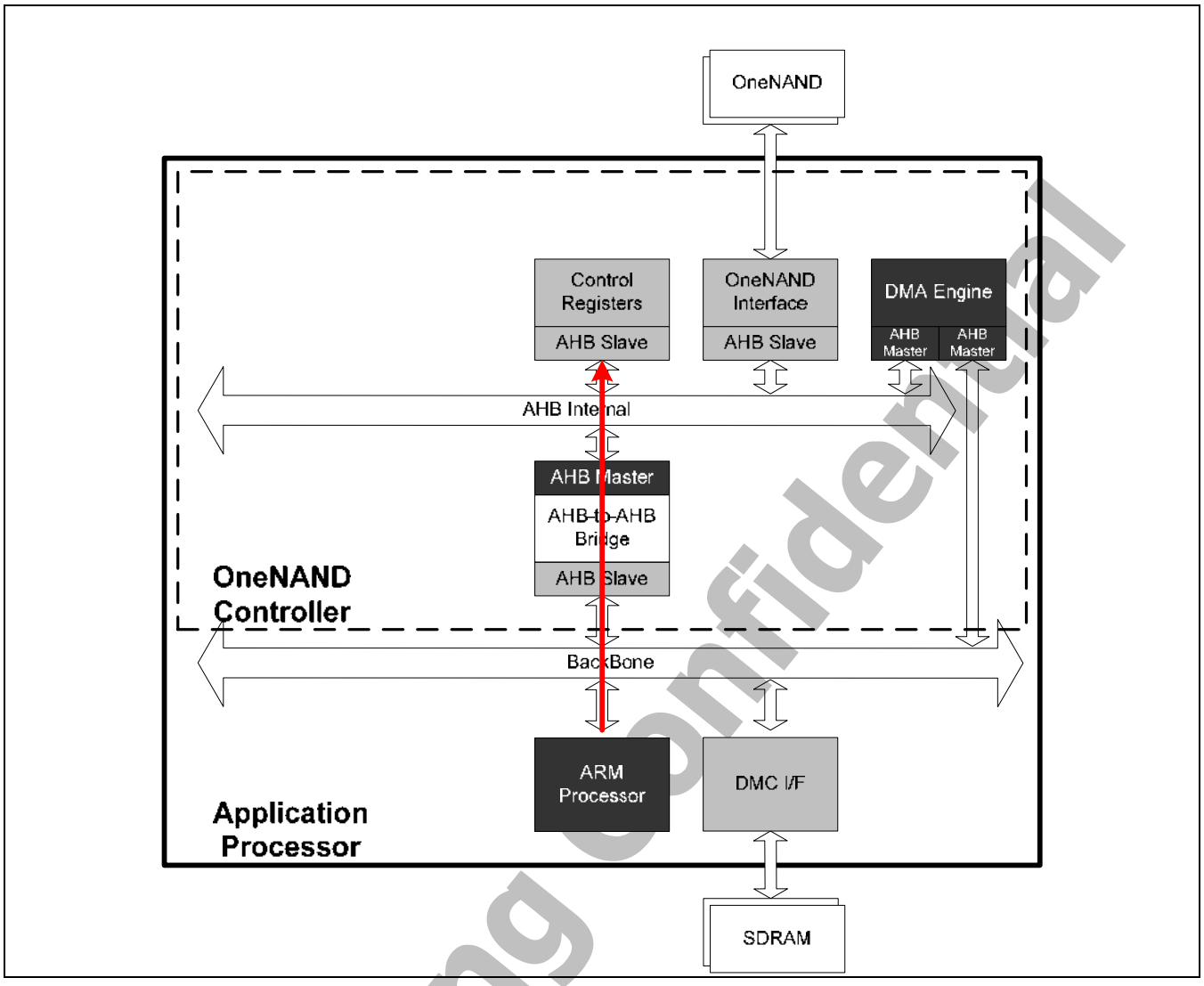

Figure 3-3 Control Register Accesses (OneNAND Controller Address: 0xB0600000 ~ 0xB07FFFFF) by the External AHB Master (ARM Processor)

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3.6 ONENAND INTERFACE

3.6.1 OVERVIEW OF ONENAND INTERFACE

The OneNAND interface is an AHB slave module that provides an interface for the AHB master to access OneNAND devices on the internal AHB bus of OneNAND controller. For example,

1. The external AHB master can access OneNAND device through the AHB2AHB bridge and OneNAND interface (*Figure 3-2*)

2. The internal AHB master can access the OneNAND deice through the OneNAND interface (*Figure 3-10* and *Figure 3-9*).

The OneNAND interface slave has few AHB transaction constraints. It supports HSIZE of HALFWORD and WORD transactions on the AHB system bus. It also supports HBURST of SINGLE, INCR4, INCR8, and INCR16. This interface outputs HRESP of ERROR at the first data phase of AHB transaction.

Both OneNAND and Flex-OneNAND flash memory devices are supported by OneNAND controller.

Both mux-type and demux-type OneNAND devices are supported by OneNAND controller. Use SFR to configure the OneNAND device type.

Both asynchronous and synchronous read/ write operations are supported by OneNAND controller for OneNAND flash memory devices. This mode of read/ write operations can be configured through the SFR. For more information, refer to the OneNAND Interface Control (ONENAND_IF_CTRL) register.

To connect OneNAND controller with eight OneNAND devices, eight chip enable (CE) signals are provided.

Asynchronous FIFOs are used for speed matching between OneNAND flash memory and AHB system bus. The clock frequency relationship between OneNAND device and AHB system bus is fully asynchronous.

The OneNAND device supports only 16-bit data bus width. On the other hand, the OneNAND controller supports 32-bit AHB data bus width. While reading data from OneNAND device and writing that data to FIFO, the OneNAND interface automatically resolves the data bus width mismatch. This interface also resolves the data bus width mismatch while reading data from FIFO and writing that data to OneNAND device.

32-entry read prefetch FIFO supports read prefetching. This feature accelerates the sequential read performance of OneNAND BootRAM and DataRAM areas. Use SFR to enable or disable this feature. For more information, refer to the OneNAND Interface Control (ONENAND_IF_CTRL) register.

To accelerate the write performance of the OneNAND DataRAM area, perform posted write. This feature is implemented using the 32-entry posted write FIFOs.

Use SFR to configure the strobe signals' timing for asynchronous read/write operation. For more information, refer to the OneNAND Interface Asynchronous Timing Control (ONENAND_IF_ASYNC_TIMING_CTRL) register.

Use SFR to configure the burst read write latency (BRWL) for the synchronous read/ write operation with 3, 4, 5, 6, and 7. For more information, refer to the OneNAND Interface Control (ONENAND_IF_CTRL) register.

The OneNAND interface does NOT support the initial read write latency control through the RDY pin of the OneNAND device.

The Burst Length (BL) also can be configured to 4-/ 8-/16-/ 32-/ 1024-burst and continuous burst through the SFR. For more information, refer to the OneNAND Interface Control (ONENAND_IF_CTRL) register.

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To reduce the power consumption for OneNAND interface and drive the clock output to OneNAND device, the gated clock output is supported. If this feature is enabled, the OneNAND device clock is toggled only if the OneNAND device is accessed to perform read or write operation. For more information, refer to the OneNAND Interface Control (ONENAND_IF_CTRL) register.

The warm reset operation is supported. For more information, refer to the OneNAND Interface Command (ONENAND_IF_CMD) register.

3.6.2 ONENAND INTERFACE CONFIGURATION

There are two configuration registers for the OneNAND Interface, namely:

1. OneNAND Interface Control (OneNAND_IF_CTRL) register
2. OneNAND Interface Asynchronous Timing Control (OneNAND_IF_ASYNC_TIMING_CTRL) register.

The OneNAND Interface Control Register (ONENAND_IF_CTRL) register holds configuration bits for following:

- MUX : Mux/ Demux select (mux-type or demux-type)
- GCE: Gated-clock enable (enable or disable)
- RPE: Read prefetch enable (enable or disable)
- RM : Read mode (synchronous vs. asynchronous)
- BRWL: Burst read write latency (3 clock, … , 7 clock)
- BL: Burst length (4-/8-/16-/32-/1024-burst or continuous)
- HF: High frequency (enable or disable)
- WM : Write mode (synchronous vs. asynchronous)

The OneNAND controller requires a correct operation sequence to change the OneNAND Interface Control (ONENAND_IF_CTRL) register value. To update this register the system software must follow the specific sequence illustrated in *Figure 3-4*. Note that the OneNAND Read Write Busy (ORWB) bit must be checked to confirm that there is no bus transaction in progress on the OneNAND interface before write new configuration to the OneNAND Interface Control (ONENAND_IF_CTRL) register. Also note that the System Configuration 1 registers of all the OneNAND devices must be set by the same configuration value though the OneNAND interface supports multiple (up to eight) OneNAND devices.

The OneNAND Interface Asynchronous Timing Control (ONENAND_IF_ASYNC_TIMING_CTRL) register holds configuration bits for following:

- WHL: nWE signal high length (1 clock, … , 15 clock)
- WLL: nWE signal low length (1 clock, … , 15 clock)
- OHL: nOE signal high length (1 clock, … , 15 clock)
- OLL: nOE signal low length (2 clock, … , 16 clock)

The OneNAND controller requires a correct operation sequence to change the OneNAND Interface Asynchronous Timing Control (ONENAND_IF_ASYNC_TIMING_CTRL) register value. To update this register the system software must follow the specific sequence illustrated in *Figure 3-6*. Note that the OneNAND Read Write Busy(ORWB) bit must be checked to confirm that there is no bus transaction in progress on the OneNAND interface before write new configuration to the OneNAND Interface Asynchronous Timing Control (ONENAND_IF_ASYNC_TIMING_CTRL) register.

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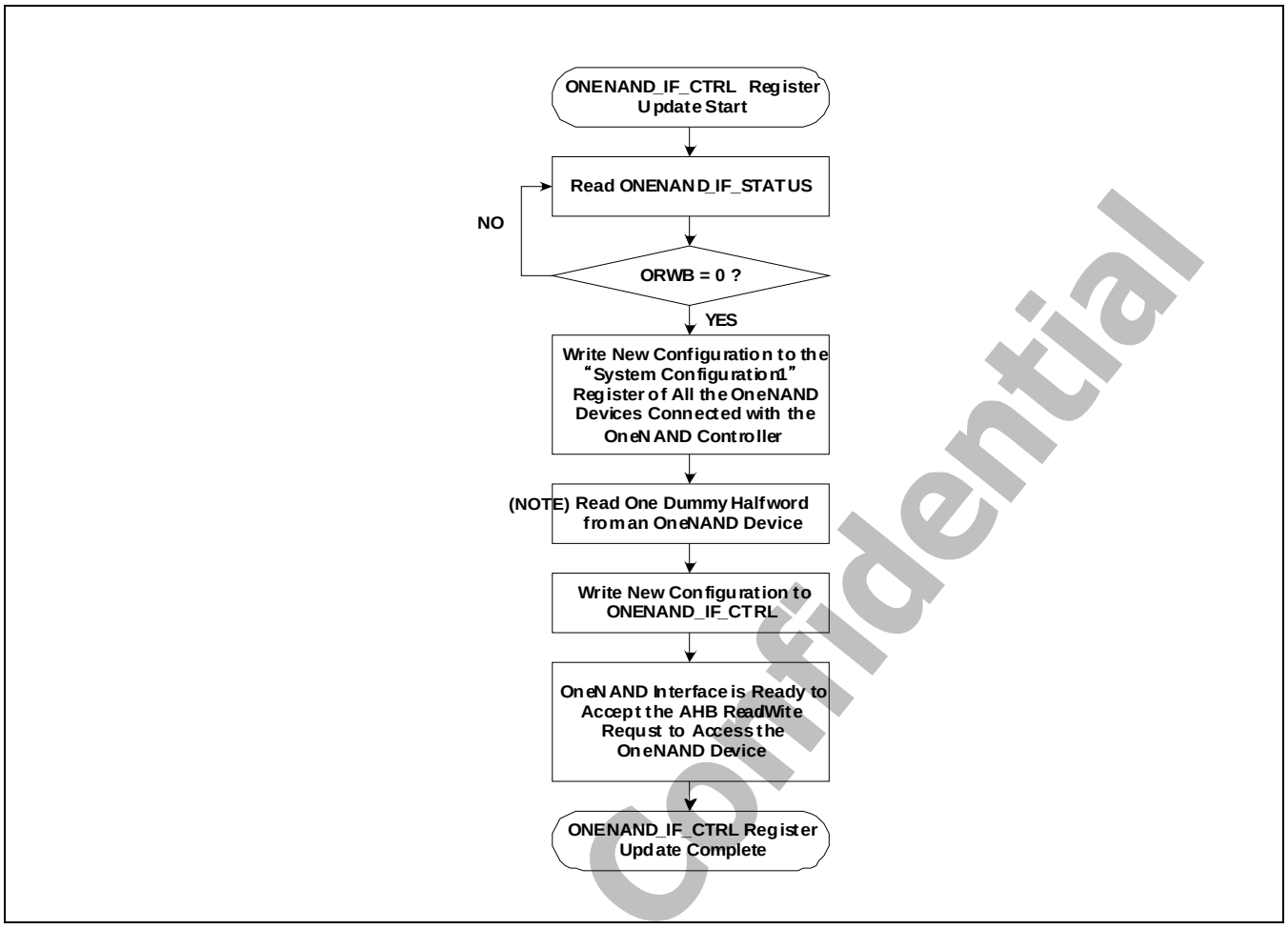

Figure 3-4 ONENAND_IF_CTRL (OneNAND Interface Control) Register Update Flow

NOTE: This dummy halfword read is necessary to confirm that new configuration value is written to the OneNAND device before updating the ONENAND_IF_CTRL register. We recommend 0x0000 for this dummy read address from OneNAND device.

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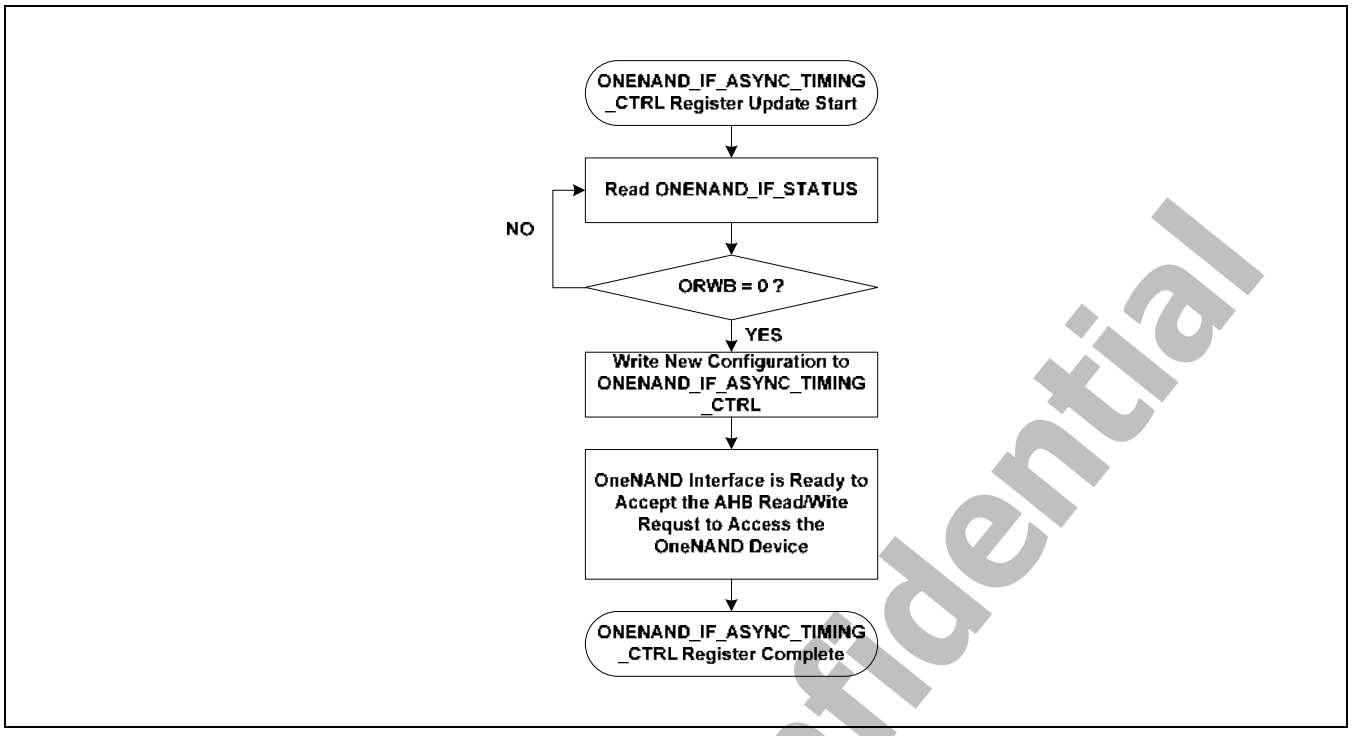

Figure 3-5 ONENAND_IF_ASYNC_TIMING_CTRL (OneNAND Interface Async Timing Control) Register Update Flow

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3.6.3 ONENAND DEVICE INTERRUPT HANDLING

The OneNAND interface provides two mechanisms to check the INT pin status of the OneNAND devices, namely:

1. Polling the INTD (INT Done) bits of the OneNAND Interface Status (ONENAND_IF_STATUS) register
2. Interrupt-driven checking.

The OneNAND controller requires that the system software should follow the correct operation sequence to check the INT pin status of the OneNAND device as shown in *Figure 3-6* and *Figure 3-7*.

Note that the OneNAND interface detects only the rising edge of the INT pin. Therefore, set the INT Polarity (INTpol) bit of the System Configuration 1 register (device address offset: 0x1E442) of the OneNAND device to 1.

Figure 3-8 illustrates the timing diagram of the INT pin of the OneNAND device and related SFR signals. The *Figure 3-8* is described below:

- T1: New command (ex. load, program or erase) is written to the OneNAND device Command register
- T2: OneNAND device INT pin rising edge occurs
- T3: The INTD[x] bit of the OneNAND Interface Status (ONENAND_IF_STATUS) register is set to 1.
- T4: OSINTD[x] (OneNAND Status INT Done) bit of the Interrupt Controller OneNAND Status (INTC_ONENAND_STATUS) register is set to 1 because OMINTD[x] (OneNAND Mask INT Done) bit of the Interrupt Controller OneNAND Mask (INTC_ONENAND_MASK) is deasserted to 0. Simultaneously, ARM_IRQ pin is asserted to high to generate an interrupt to the system
- T5: The system software (ex. ISR (Interrupt Service Routine)) writes 1 to the INTC[x] bit of the OneNAND Interface Command (ONENAND_IF_CMD) register to clear the INTD[x] bit of the OneNAND Interface Status (ONENAND_IF_STATUS) register.
- T6: The INTD[x] bit of the OneNAND Interface Status (ONENAND_IF_STATUS) register is cleared to 0. T7: The system software (ex. ISR (Interrupt Service Routine)) writes 1 to the OCINTD[x] bit (OneNAND Clear INT Done) of the Interrupt Controller OneNAND Clear (INTC_ONENAND_CLR) register to clear the OSINTD[x] (OneNAND Status INT Done) bit of the Interrupt Controller OneNAND Status (INTC_ONENAND_STATUS) register.
- T8: The OSINTD[x] (OneNAND Status INT Done) bit of the Interrupt Controller OneNAND Status (INTC_ONENAND_STATUS) register is cleared to 0. Simultaneously, ARM_IRQ pin is deasserted to low.

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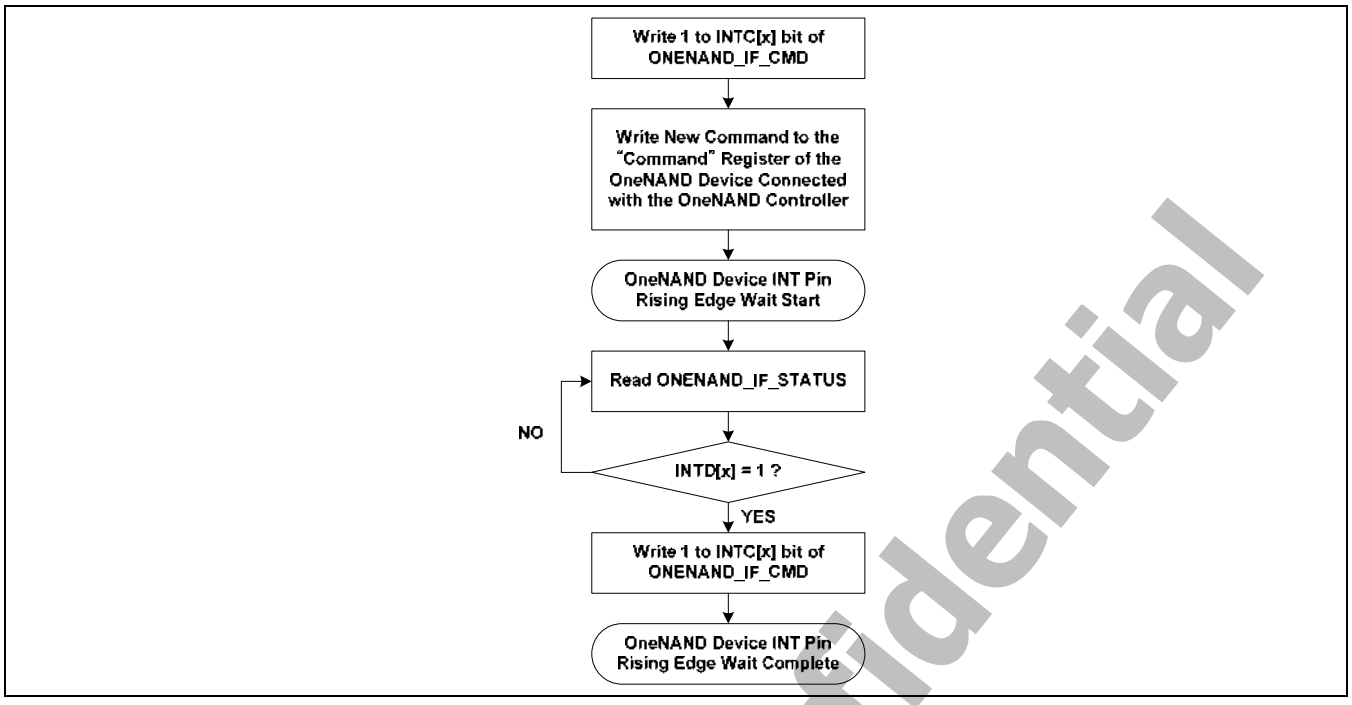

Figure 3-6 OneNAND Device INT Pin Rising Edge Wait Operations with a Polling Method

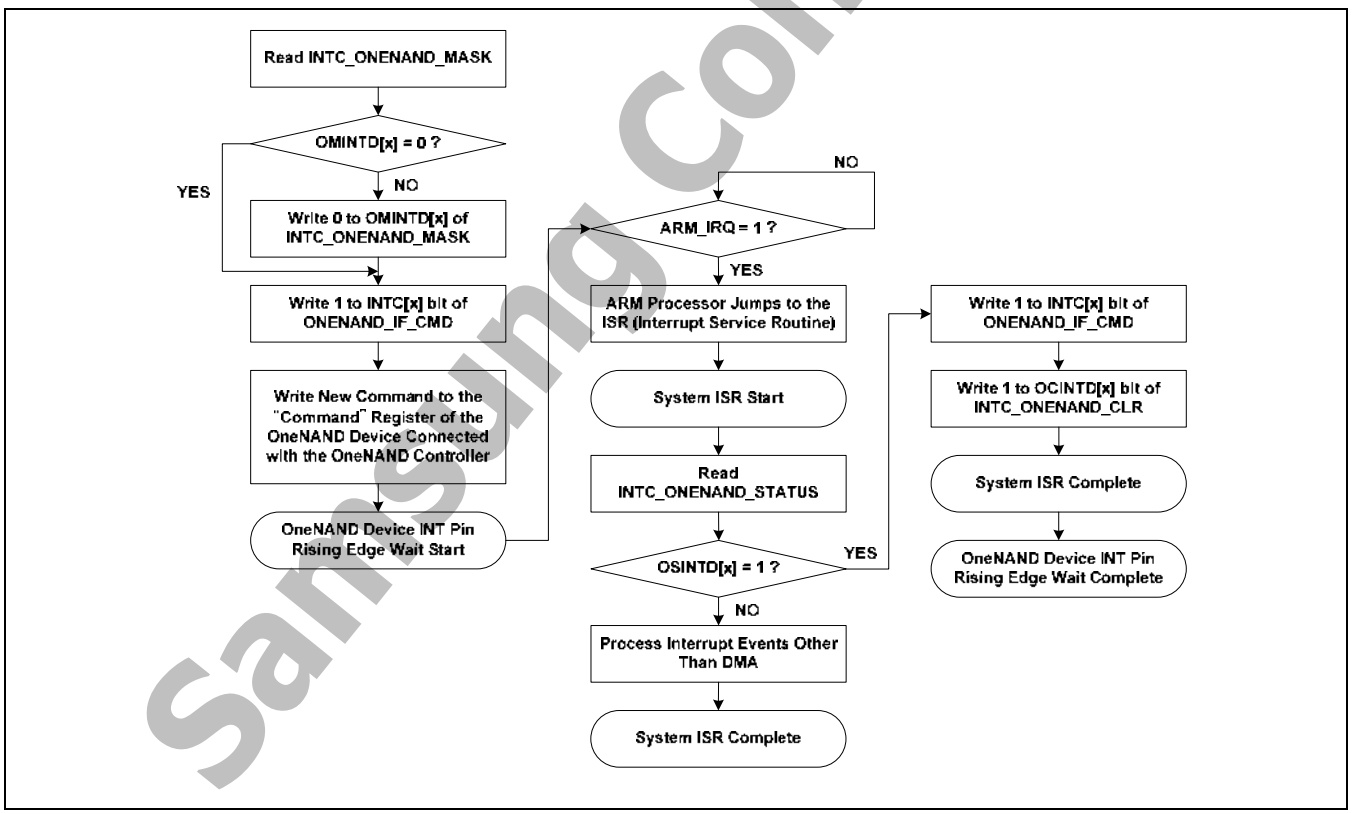

Figure 3-7 OneNAND Device INT Pin Rising Edge Wait Operations with an Interrupt-Driven Method

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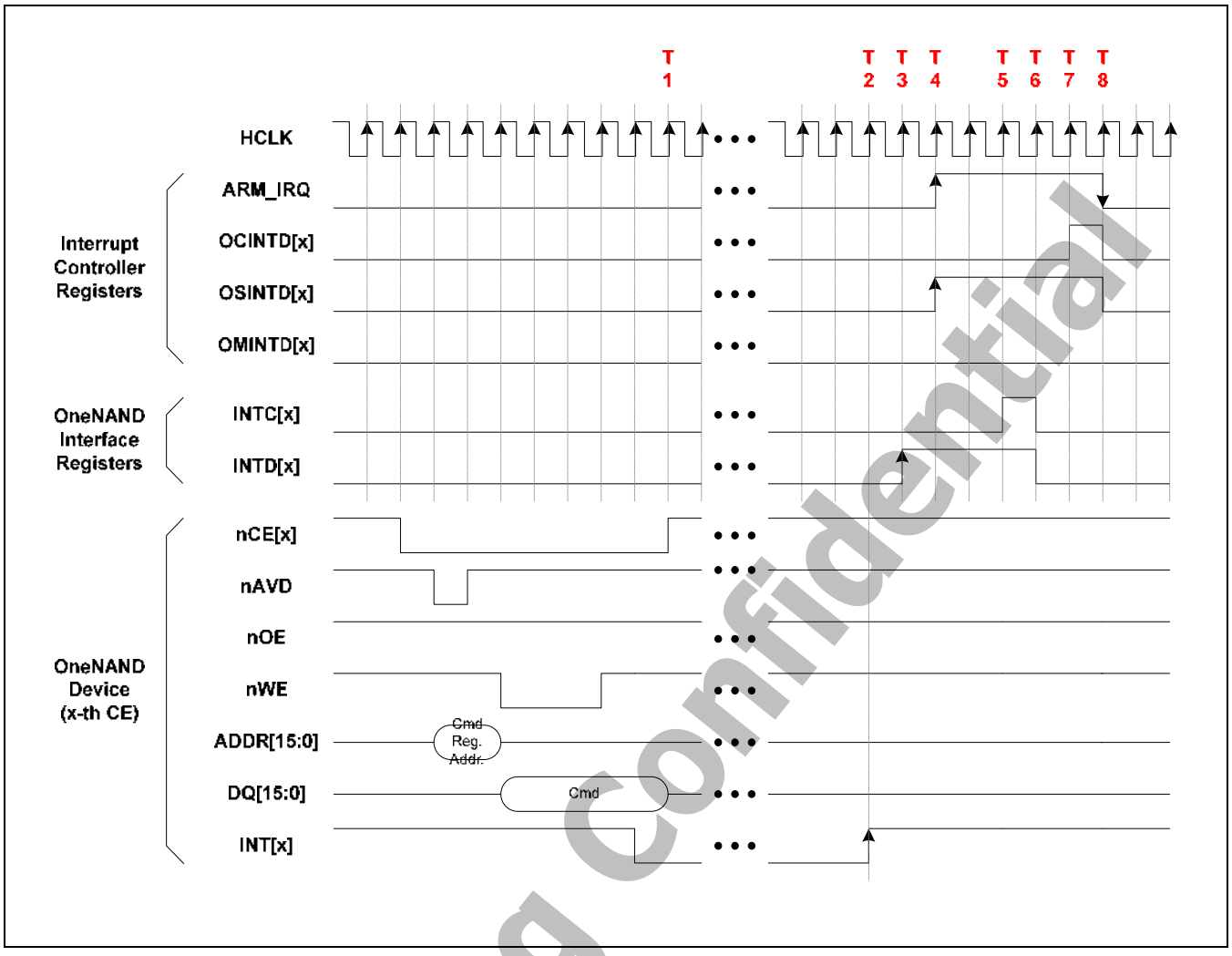

Figure 3-8 OneNAND Device INT Pin Rising Edge Wait Operation Timing Diagram DMA Engin

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3.6.4 DMA ENGINE OVERVIEW

To perform data transfer between internal AHB memory (such as OneNAND device) and external AHB memory (such as SDRAM), the internal dedicated DMA engine is embedded in the OneNAND controller.

The DMA engine supports single transfer, 4-/ 8-/ 16-burst transfer with 8-/ 16-/ 32-bit data width on the AHB. In addition, it supports even unaligned transfers.

The DMA engine has two AHB master ports. One port can access OneNAND or control registers on the internal AHB. The other port can access SDRAM on the external AHB (AHB backbone), as shown in Figure 3-9. Each port has 32-entry synchronous FIFOs as data buffer, through which two AHB masters of the DMA engine transfer data. This helps to improve the performance of data transfer, because two AHB master ports of DMA engine access the source and destination memories at the same time. Note that a general DMA engine has a single AHB master port, and the memory accesses to the source and destination memories are serialized.

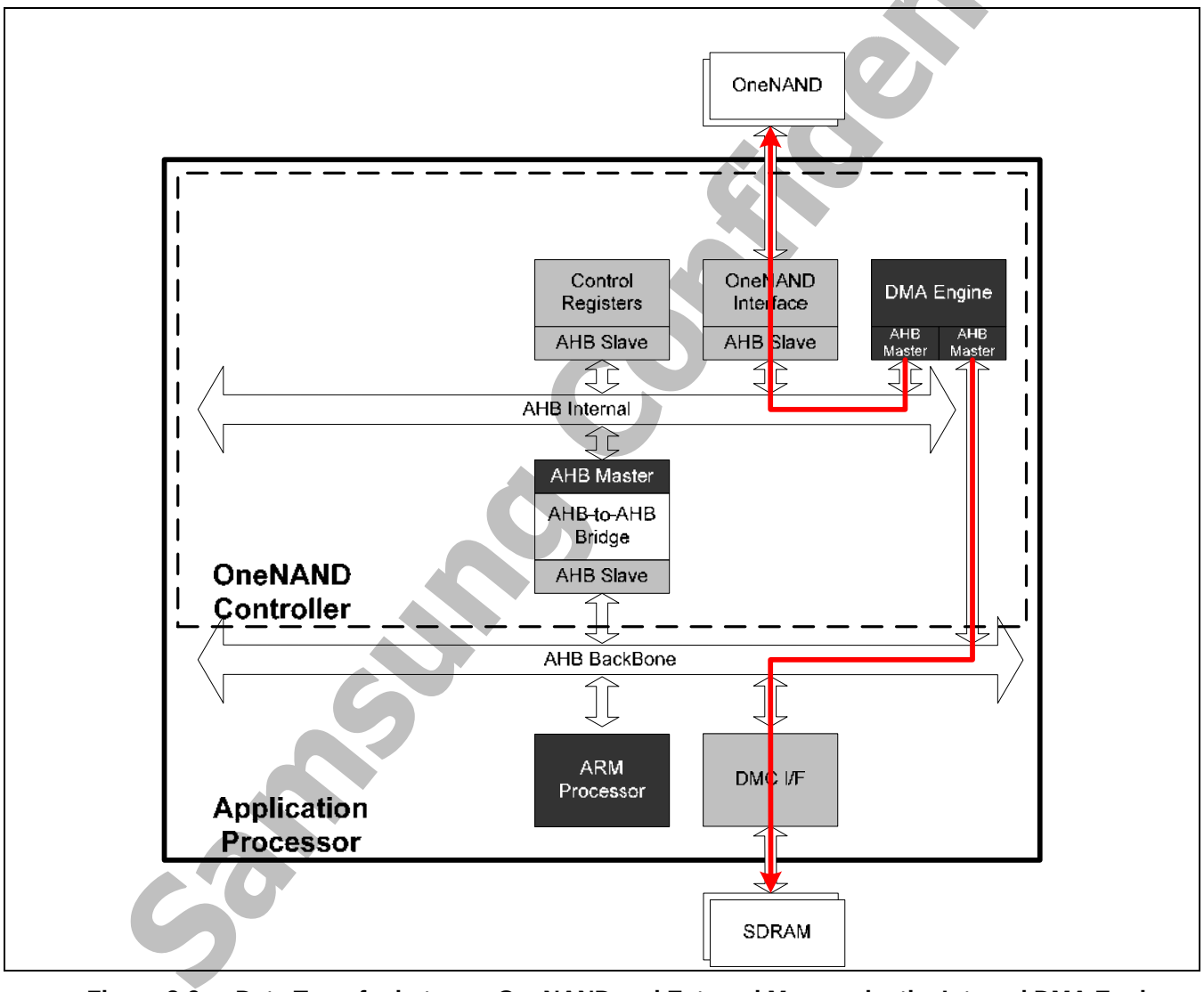

Figure 3-9 Data Transfer between OneNAND and External Memory by the Internal DMA Engine (OneNAND Read/ Write)

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3.6.5 DMA OPERATION

Set DMA control registers to configure the DMA operation. The DMA engine begins to transfer data after setting the Transfer Run (TR) bit of the DMA Transfer Command (DMA_TRANS_CMD) register to 1. The Transfer Busy (TB) bit of the DMA Transfer Status (DMA_TRANS_STATUS) register is maintained as 1 during the data transfer to indicate that the DMA engine is busy. After the DMA operation has been finished successfully, the Transfer Done (TD) bit of the DMA Transfer Status (DMA_TRANS_STATUS) register is set to 1 to notify the system software that the DMA operation is completed. There are two methods, with which the system software waits for the completion of the DMA operation and determines the DMA engine's completion status.

- DMA operation with a polling method
- DMA operation with an interrupt-driven method

3.6.5.1 DMA Operation With a Polling Method

The system software polls DMA_TRANS_STATUS register to check the status of the DMA engine.

The DMA engine sets the TD bit of the DMA Transfer Status (DMA_TRANS_STATUS) register to 1 when the data transfer is completed. It sets the Transfer Error (TE) bit of the DMA Transfer Status (DMA_TRANS_STATUS) register to 1 when an error occurs during the transfer.

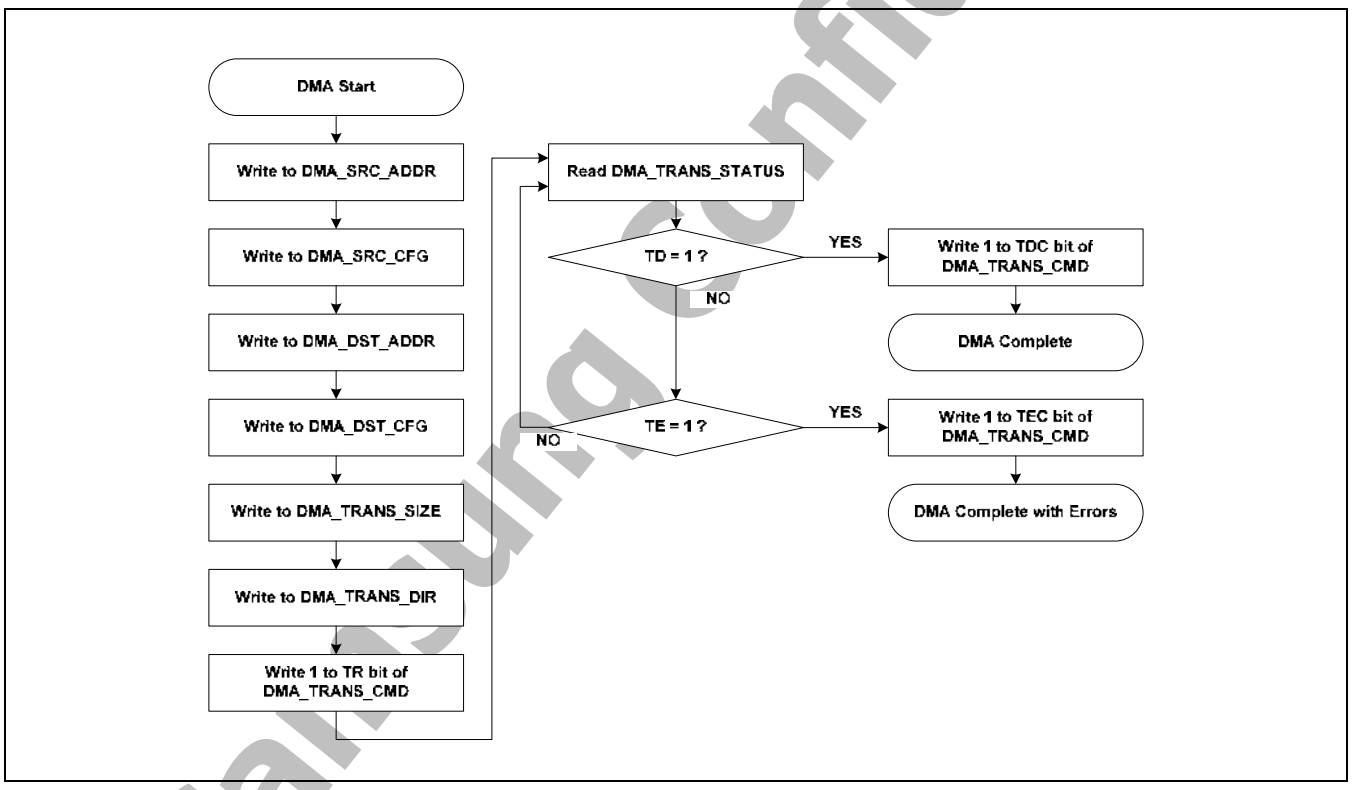

Figure 3-10 Internal DMA Engine Operations with a Polling Method

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3.6.5.2 DMA Operation With an Interrupt-driven Method

The DMA engine asserts system interrupt signal for the transfer done or the transfer error event

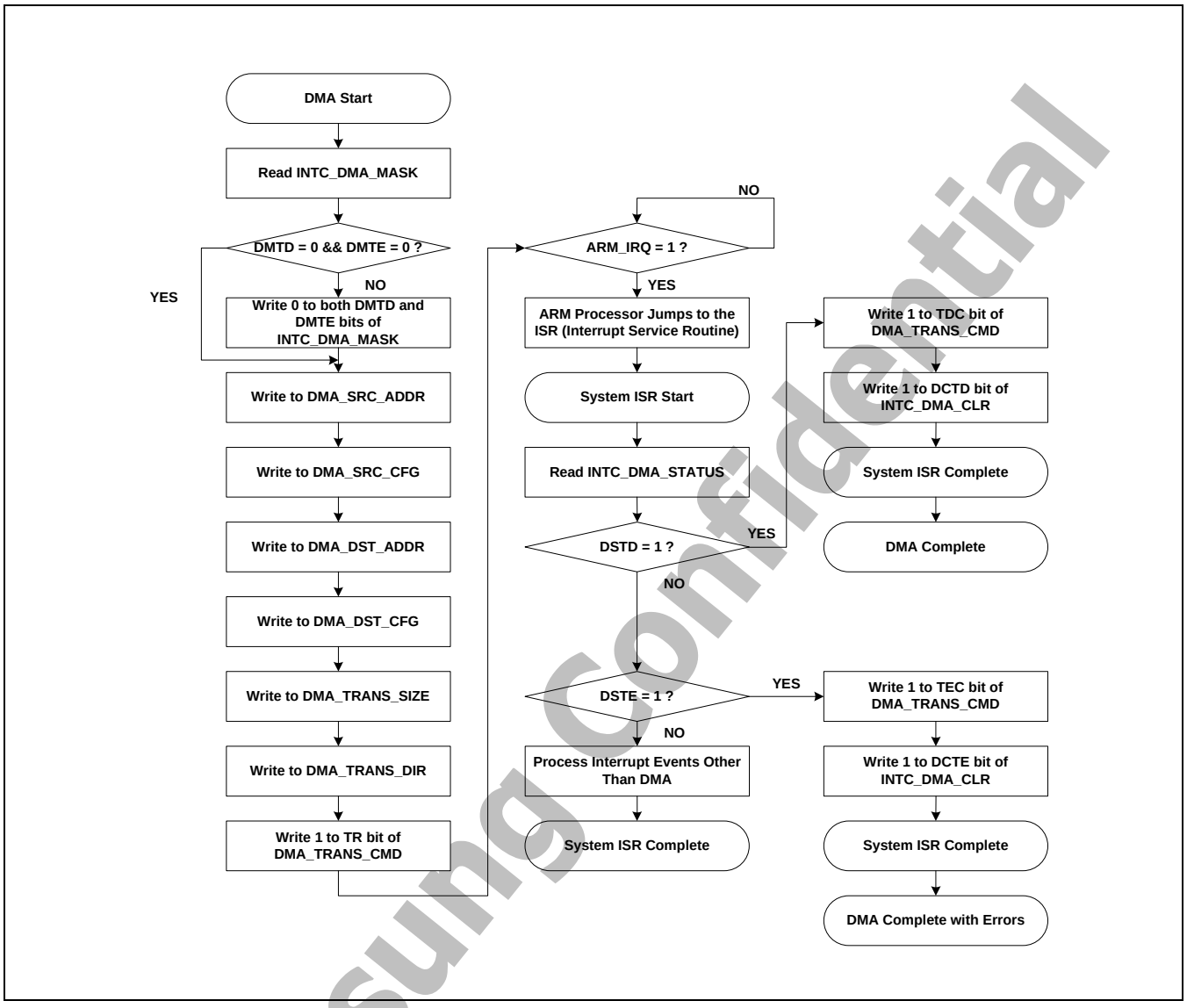

Figure 3-11 Internal DMA Engine Operations with an Interrupt-Driven Method

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3.7 I/O INTERFACE

Signal	I/O	Description	PAD	Type
ADDR[15:0]	I/O	Address Bus outputs, during memory read/ write address phase	Xm0ADDR [15:0]	muxed
DQ[15:0]	I/O	Data Bus outputs address during memory read/ write address phase, inputs data during memory read data phase and outputs data during memory write data phase.	Xm0DATA [15:0]	muxed
nCE[1:0]	O	Chip Selects are activated when the address of a memory is within the address region of each bank. Xm0CSn[3:2] can be assigned to either SROMC or OneNAND controller by System Controller SFR setting. Active LOW.	Xm0CSn [5:4]	muxed
nWE	O	Write Enable indicates that the current bus cycle is a write cycle. Active LOW.	Xm0WEn	muxed
nOE	O	Output Enable indicates that the current bus cycle is a read cycle. Active LOW.	Xm0OEn	muxed
INT[1:0]	I	Interrupt inputs from OneNAND memory Bank 0, 1. If OneNAND memory is not used, these signals should be tied to zero.	Xm0FRnB [5:4]	muxed
nAVD	O	Address valid output. In the POP products, address and data are multiplexed. Xm0ADDRVALID indicate when the bus is used for address. Active LOW.	Xm0FCLE	muxed
nRP	O	System reset output for OneNAND memory. Active LOW.	Xm0FWEn	muxed
CLK	O	Static memory clock for synchronous static memory devices.	Xm0FALE	muxed

NOTE: The INT pin of each OneNAND Device must be pulled up by a 4.7K-ohm external pull-up resistor.

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3.8 REGISTER DESCRIPTION

3.8.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
ONENAND_IF_CTRL	0xB060_0100	R/W	OneNAND Interface Control register	0x80004000 or 0x00004000
ONENAND_IF_CMD	0xB060_0104	W	OneNAND Interface Command register	0x00000000
ONENAND_IF_ASYNC_TIMING_CTRL	0xB060_0108	R/W	OneNAND Interface Async. Timing Control register	0x00003415
ONENAND_IF_STATUS	0xB060_010C	R	OneNAND Interface Status Register	0x00FF0000
DMA_SRC_ADDR	0xB060_0400	R/W	DMA Source Address Register	0x00000000
DMA_SRC_CFG	0xB060_0404	R/W	DMA Source Configuration Register	0x00040002
DMA_DST_ADDR	0xB060_0408	R/W	DMA Destination Address Register	0x00000000
DMA_DST_CFG	0xB060_040C	R/W	DMA Destination Configuration Register	0x00040002
DMA_TRANS_SIZE	0xB060_0414	R/W	DMA Transfer Size Register	0x00000000
DMA_TRANS_CMD	0xB060_0418	W	DMA Transfer Command Register	0x00000000
DMA_TRANS_STATUS	0xB060_041C	R	DMA Transfer Status Register	0x00000000
DMA_TRANS_DIR	0xB060_0420	R/W	DMA Transfer Direction Register	0x00000000
INTC_DMA_CLR	0xB060_1004	W	Interrupt Controller DMA Clear Register	0x00000000
INTC_ONENAND_CLR	0xB060_1008	W	Interrupt Controller OneNAND Clear Register	0x00000000
INTC_DMA_MASK	0xB060_1024	R/W	Interrupt Controller DMA Mask Register	0x01010000
INTC_ONENAND_MASK	0xB06_01028	R/W	Interrupt Controller OneNAND Mask Register	0x000000FF
INTC_DMA_PEND	0xB060_1044	R	Interrupt Controller DMA Pending Register	0x00000000
INTC_ONENAND_PEND	0xB060_1048	R	Interrupt Controller OneNAND Pending Register	0x000000FF
INTC_DMA_STATUS	0xB060_1064	R	Interrupt Controller DMA Status Register	0x00000000
INTC_ONENAND_STATUS	0xB060_1068	R	Interrupt Controller OneNAND Status Register	0x00000000

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3.8.2 ONENAND INTERFACE REGISTER

3.8.2.1 OneNAND Interface Control Register (ONENAND_IF_CTRL, R/W, Address = 0xB060_0100)

ONENAND_IF_CTRL	Bit	Description	Initial State
MUX	[31]	**Mux or Demux OneNAND Type Select** OneNAND interface supports both Demux and Mux type OneNAND devices. This bit is used to specify whether OneNAND is Demux or Mux type. The value of OM pins determines the reset value of this bit If the OM pins are of Demuxed type OneNAND boot, the reset value of this bit is 1. Otherwise, the reset value is 0. (For more information, refer to *Chapter 2.6. Booting Sequence*) 0b = Mux type 1b = Demux type	1b or 0b
-	[30:27]	Reserved	-
GCE	[26]	**Gated Clock Enable** To reduce power consumption, OneNAND interface supports gated clock method. If this bit is set, the OneNAND clock toggles only during OneNAND read/ write execution time. 0b = Disable 1b = Enable	0b
-	[25:18]	Reserved	-
RPE	[17]	Enables **Read Prefetch.** This bit is used to enable or disable the read prefetch operation of the OneNAND interface. 0b = Read Prefetch Disable 1b = Read Prefetch Enable OneNAND Interface has its own read prefetch FIFO. This FIFO is implemented as an asynchronous FIFO of 32-bit x 32-depth between AHB and OneNAND clock domains. If the sequential read access is dominant, prefetch next read data in advance to increase the OneNAND read bandwidth. If Read Prefetch Enable (RPE) bit is set to 1 OneNAND interface will start to prefetch read data when it receives AHB read request. If the read prefetch FIFO becomes full during the prefetch operation, the prefetch operation will be stopped immediately. As soon as the read prefetch FIFO is ready to accept the next read data by successive AHB read operation, the prefetch operation will be resumed. If the read prefetch address reaches 1-KByte aligned address during the prefetch operation, the prefetch operation will be stopped.	0b
-	[16]	Reserved	-
RM	[15]	**Read Mode** This bit is used to select the OneNAND read mode between synchronous and asynchronous modes. 0b = Asynchronous Read 1b = Synchronous Read	0b
BRWL	[14:12]	**Burst Read Write Latency**	100b

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ONENAND_IF_CTRL	Bit	Description	Initial State
		This bit is used to select the burst read/ write latency between 3 clocks and 7 clocks. BRWL (burst read write latency) bits specify the access latency in the burst read/ write transfer for the initial access. Note that these bits are valid only for the synchronous read/ write operation. 000b = Reserved 001b = Reserved 010b = Reserved 011b = 3 CLK 100b = 4 CLK 101b = 5 CLK 110b = 6 CLK 111b = 7 CLK	
BL	[11:9]	**Burst Length** These bits are used to select the burst length among 4-burst, 8-burst, 16-burst, 32-burst, 1024-burst and continuous-burst. Note that BL (burst length) bits are valid only for the synchronous read/ write operation. 000b = Continuous-Burst 001b = 4-Burst 010b = 8-Burst 011b = 16-Burst 100b = 32-Burst 101b = 1024-Burst 110b = Reserved 111b = Reserved	000b
-	[8:3]	Reserved	-
HF	[2]	**High Frequency** This bit is used to enable or disable the high frequency mode. High frequency (HF) bit must be set when the OneNAND clock frequency is more than 66MHz. 0b = High Frequency Disable (66MHz and under) 1b = High Frequency Enable (Over 66MHz)	0b
WM	[1]	**Write Mode** This bit is used to select the OneNAND write mode between synchronous and asynchronous modes. 0b = Asynchronous Write 1b = Synchronous Write	0b
-	[0]	Reserved	-

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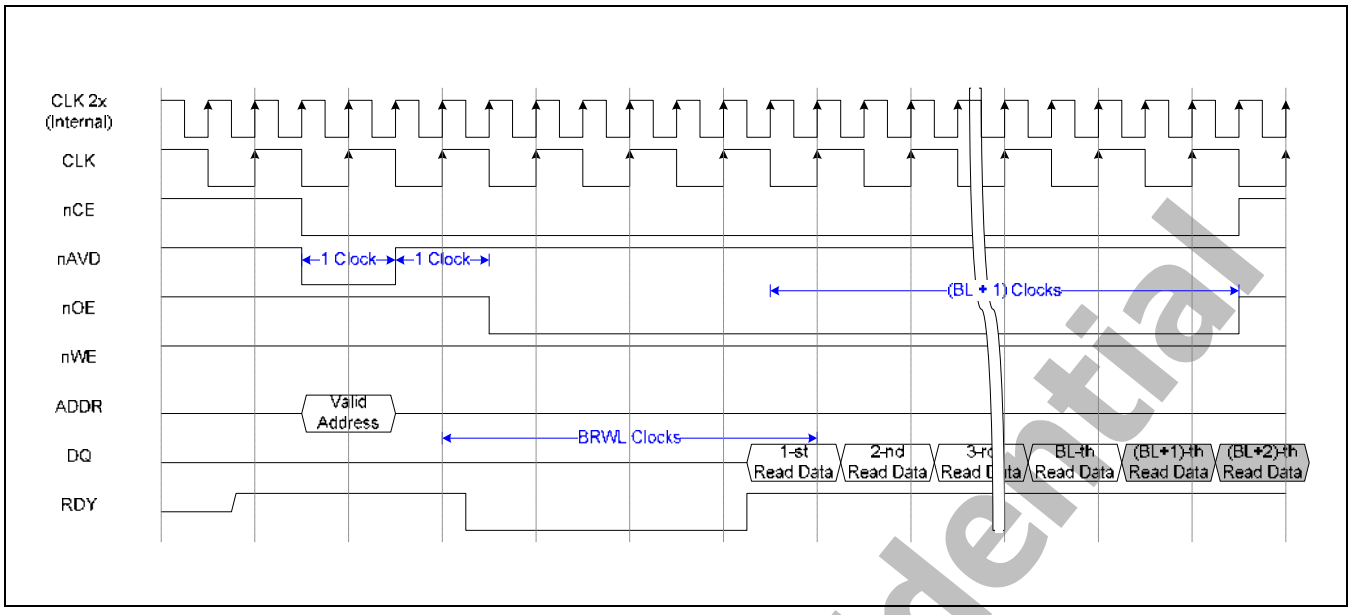

Figure 3-12 ONENAND Interface Synchronous Read Timing

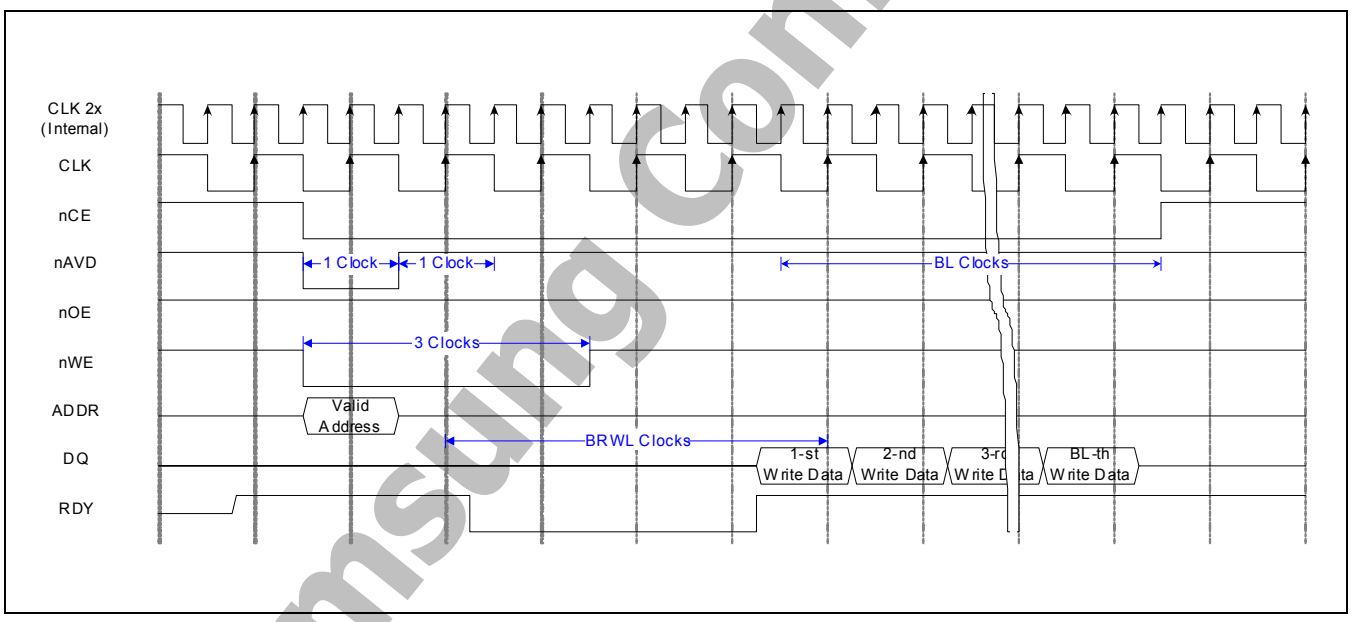

Figure 3-13 OneNAND Interface Synchronous Write Timing

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3.8.2.2 OneNAND Interface Command Register (ONENAND_IF_CMD, W, Address = 0xB060_0104)

ONENAND_IF_CMD	Bit	Description	Initial State
-	[31:18]	Reserved	-
INTC	[17:16]	**OneNAND INT Done Clear** When this bit is set to 1, the INTD (OneNAND INT done) bit flag of the OneNAND Interface Status Register (ONENAND_IF_STATUS) is cleared to 0. INTC[0] 1b = Device[0] OneNAND Interrupt Done clear 0b = no operation INTC[1] 1b = Device[1] OneNAND Interrupt Done clear 0b = no operation	00h
-	[15:2]	Reserved	-
WR	[1]	**Warm Reset** For OneNAND warm reset, writing 1 to this bit makes nRP pin of OneNAND device low during 20 CLK. It is mandatory to assert the nRP pin to zero for warm reset during tRP time and the tRP time is more than 200ns. After warm reset, it should wait for tREADY1 to access the OneNAND BootRAM and tREADY2 time is needed to issue the new command. tREADY1 time and tREADY2 time are at least 5us and 500us respectively. 1b = nPR pin low for 20 CLK 0b = no operation	0b
-	[0]	Reserved	-

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3.8.2.3 OneNAND Interface Async Timing Control Register (ONENAND_IF_ASYNC_TIMING_CTRL, R/W, Address = 0xB060_0108)

ONENAND_IF_ASYNC_TIMING_CTRL	Bit	Description	Initial State
-	[31:16]	Reserved	-
WHL	[15:12]	**nWE High Length** nWE signal is held to high for WHL clock time at OneNAND asynchronous read/ write execution. 0000b = Reserved (Do NOT Use) 0001b = 1 CLK 0010b = 2 CLK ... ... 1111b = 15 CLK	3h
WLL	[11:8]	**nWE Low Length** nWE signal is held to low for WLL clock time at OneNAND asynchronous read/ write execution. 0000b = Reserved (Do NOT Use) 0001b = 1 CLK 0010b = 2 CLK ... ... 1111b = 15 CLK	4h
OHL	[7:4]	**nOE High Length** nOE signal is held to high for OHL clock time at OneNAND asynchronous read/ write execution. 0000b = Reserved (Do NOT Use) 0001b = 1 CLK 0010b = 2 CLK ... ... 1111b = 15 CLK	1h
OLL	[3:0]	**nOE Low Length** nOE signal is held to low for (OLL+2) clock time at OneNAND asynchronous read/ write execution. 0000b = 2 CLK 0001b = 3 CLK 0010b = 4 CLK ... ... 1110b = 16 CLK 1111b : Reserved (Do NOT Use)	5h

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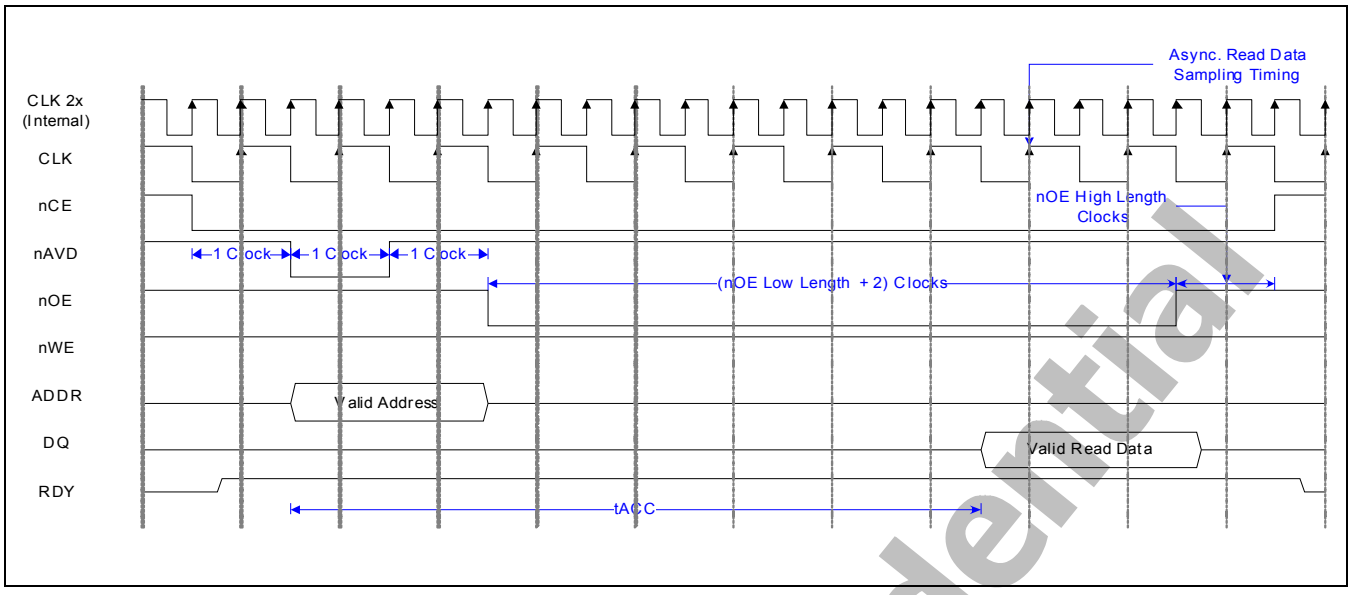

Figure 3-14 OneNAND Interface Asynchronous Read Timing

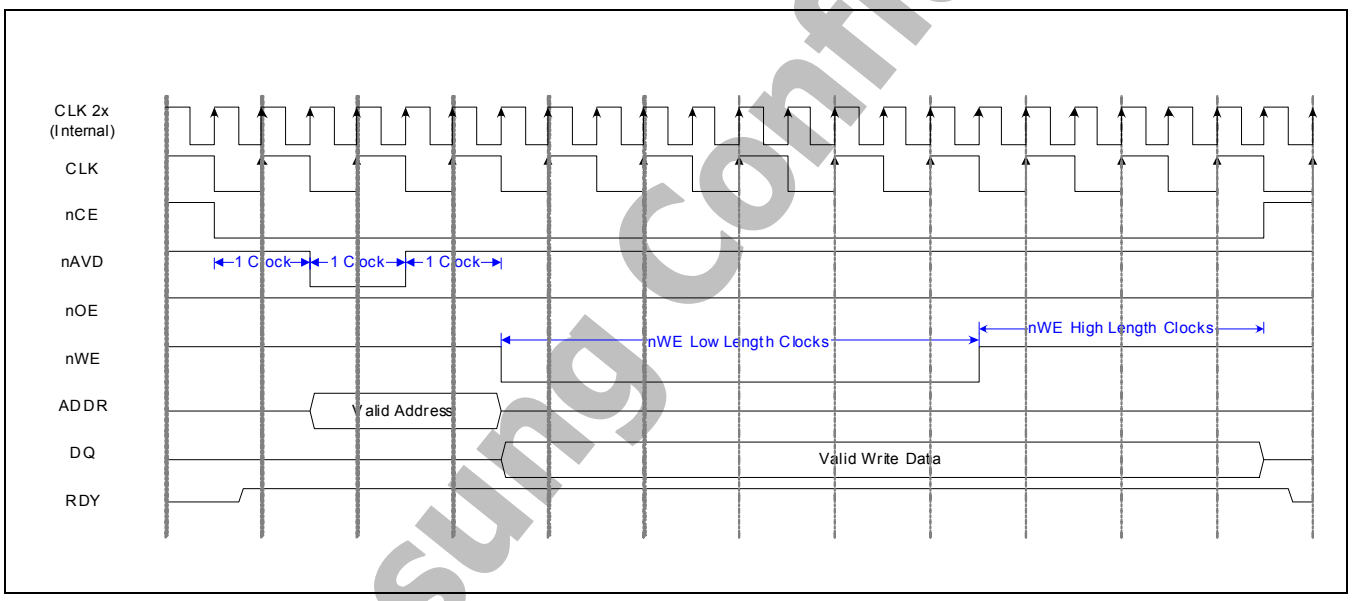

Figure 3-15 OneNAND Interface Asynchronous Write Timing

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3.8.2.4 OneNAND Interface Status Register (ONENAND_IF_STATUS, R, Address = 0xB060_010C)

ONENAND_IF_STATUS	Bit	Description	Initial State
-	[31:24]	Reserved	-
-	[23:18]	Reserved	111111b
INTD	[17:16]	**OneNAND INT Done** This status is used to check whether the OneNAND command execution is complete or not. Check whether the OneNAND INT pin's rising edge has been occurred or not after issuing a command to the OneNAND to notify command execution completion. This bit is set to 1 automatically when OneNAND INT pin's rising edge is detected and is cleared to 0 when INTC (OneNAND INT Done Clear) bit of OneNAND Interface Command Register (ONENAND_IF_CMD) is set to 1. INTD[0] 1b = Device[0] OneNAND Interrupt Done 0b = No operation INTD[1] 1b = Device[1] OneNAND Interrupt Done 0b = No operation	11b
-	[15:1]	Reserved	-
ORWB	[0]	**OneNAND Read Write Busy** This status is used to check whether the OneNAND interface is busy or not to read or write data. This bit must be checked to confirm that there is no (For example, posted writes or read prefetch operations) bus transaction in progress on the OneNAND interface before writing new configurations to ONENAND_IF_CTRL and ONENAND_IF_ASYNC_TIMING_CTRL registers. 1b = Busy 0b = Not Busy	0b

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3.8.3 DMA CONTROL REGISTERS

3.8.3.1 DMA Source Address Register (DMA_SRC_ADDR, R/W, Address = 0xB060_0400)

DMA_SRC_ADDR	Bit	Description	Initial State
SA	[31:0]	**Source Address** Source address on the AHB for the DMA operation. The start address for the DMA engine to perform read operation.	00000000h

3.8.3.2 DMA Source Configuration Register (DMA_SRC_CFG, R/W, Address = 0xB060_0404)

DMA_SRC_CFG	Bit	Description	Initial State
-	[31:19]	Reserved	-
SBL	[18:16]	**Source Burst Length** Burst length during the source memory access on the AHB for the DMA operation. This burst length is valid only when the memory address is aligned. The DMA engine requires that the memory address should be the multiple of the HSIZE (data width) x HBURST (burst length) to initiate the burst transfer on the AHB during the DMA transfer. If this address alignment condition is not satisfied, the actual burst length on the AHB will be single until this condition is met. 000b = Single 001b = Reserved 010b = 4-Burst 011b = 8-Burst 100b = 16-Burst 101b = Reserved 110b = Reserved 111b = Reserved	100b
-	[15:9]	Reserved	-
SAM	[8]	**Source Addressing Mode** This bit refers to addressing mode during the source memory access on the AHB for the DMA operation. The incremental addressing mode is used for the general DMA operation and the constant mode is used to access repeatedly the specific address like a data register. 0b = Incremental addressing mode 1b = Constant addressing mode	0b
-	[7:2]	Reserved	-
SDW	[1:0]	**Source Data Width** Access size during the source memory access on the AHB for the DMA operation. The data width is valid only if the memory address is aligned. To initiate the AHB transfer, the DMA engine requires that the	10b

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DMA_SRC_CFG	Bit	Description	Initial State
		memory address should be the multiple of the HSIZE (data width). If this address alignment condition is not satisfied, the actual data width on the AHB during the DMA transfer will be smaller than the access size specified in these bits. 00b = 8-bit (byte) 01b = 16-bit (half word) 10b = 32-bit (word) 11b = Reserved	

3.8.3.3 DMA Destination Address Register (DMA_DST_ADDR, R/W, Address = 0xB060_0408)

DMA_DST_ADDR	Bit	Description	Initial State
DA	[31:0]	**Destination Address** Destination address on the AHB for the DMA operation. This address is the start address to which the DMA engine performs write operation.	00000000h

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3.8.3.4 DMA Destination Configuration Register (DMA_DST_CFG, R/W, Address = 0xB060_040C)

DMA_DST_CFG	Bit	Description	Initial State
-	[31:19]	Reserved	-
DBL	[18:16]	**Destination Burst Length** Burst length during the destination memory access on the AHB for the DMA operation. This burst length is valid only when the memory address is aligned. The DMA engine requires that the memory address should be the multiple of the HSIZE (data width) x HBURST (burst length) to initiate the burst transfer on the AHB during the DMA transfer. If this address alignment condition is not satisfied, the actual burst length on the AHB will be single until this condition is met. 000b = Single 001b = Reserved 010b = 4-Burst 011b = 8-Burst 100b = 16-Burst 101b = Reserved 110b = Reserved 111b = Reserved	100b
-	[15:9]	Reserved	-
DAM	[8]	**Destination Addressing Mode** It specifies Addressing mode during the destination memory access on the AHB for the DMA operation. The incremental addressing mode is used for the general DMA operation and the constant mode is used to access repeatedly the specific address like a data register. 0b = Incremental addressing mode 1b = Constant addressing mode	0b
-	[7:2]	Reserved	-
DDW	[1:0]	**Destination Data Width** Access size during the destination memory access on the AHB for the DMA operation. The data width is valid only if the memory address is aligned. To initiate the AHB transfer, the DMA engine requires that the memory address should be the multiple of the HSIZE (data width). If this address alignment condition is not satisfied, the actual data width on the AHB during the DMA transfer will be smaller than the access size specified in these bits. 00b = 8-bit (byte) 01b = 16-bit (half word) 10b = 32-bit (word) 11b = Reserved	10b

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3.8.3.5 DMA Transfer Size Register (DMA_TRANS_SIZE, R/W, Address = 0xB060_0414)

DMA_TRANS_SIZE	Bit	Description	Initial State
-	[31:24]	Reserved	-
TS	[23:0]	**Transfer Size** The number of bytes to be transferred to the AHB by the DMA engine. Transfer size must be less than 16MBytes. If the DMA source or destination address is in the OneNAND interface slave address space, TS (Transfer Size) must be the multiple of 2 because OneNAND interface slave does NOT support BYTE transactions.	000000h

3.8.3.6 DMA Transfer Command Register (DMA_TRANS_CMD, W, Address = 0xB060_0418)

DMA_TRANS_CMD	Bit	Description	Initial State
-	[31:19]	Reserved	-
TDC	[18]	**Transfer Done Clear** When this bit is set to 1, the TD (Transfer Done) bit flag of the DMA Transfer Status Register (DMA_TRANS_STATUS) in the DMA engine is cleared to 0	0b
-	[17]	Reserved	-
TEC	[16]	**Transfer Error Clear** When this bit is set to 1, the TE (Transfer Error) bit flag of the DMA Transfer Status Register (DMA_TRANS_STATUS) in the DMA engine is cleared to 0	0b
-	[15:1]	Reserved	-
TR	[0]	**Transfer Run** When this bit is set to 1, the DMA engine starts to transfer data from the source memory to the destination memory in the AHB	0b

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3.8.3.7 DMA Transfer Status Register (A_TRANS_STATUS, R, Address = 0xB060_041C)

A_TRANS_ STATUS	Bit	Description	Initial State
-	[31:19]	Reserved	-
TD	[18]	**Transfer Done** This status is used to check whether the DMA transfer is complete or not. After the DMA transfer is successfully completed, TD bit is set to 1.	0b
TB	[17]	**Transfer Busy** This status is used to check whether the DMA transfer is in progress or not	0b
TE	[16]	**Transfer Error** This status is used to check whether there has been an error during the DMA transfer. There are three error sources in the DMA engine. First error source is the response signal (HRESP) from the slave on the AHB. As soon as the DMA engine receives any ERROR response from the slave on the AHB during the DMA transfer, TE bit is set to 1 and the DMA operation stops. Second error sources are the incorrect source/ destination address and transfer direction configurations. The DMA engine has two AHB master ports and these are connected to the external AHB and the internal AHB, respectively. Therefore source and destination address registers cannot be configured to the slaves on the same AHB for the DMA operation. Due to this fact, only following two cases are allowed for source/ destination address register value: 1) source memory is the slave on the external AHB and destination memory is the slave on the internal AHB, 2) source memory is the slave on the internal AHB and destination memory is the slave on the external AHB. If source/ destination address registers are not configured to satisfy this condition, the DMA engine does not perform any data transfer and TE bit is set to 1. Also, if the transfer direction register is not configured correctly according to source/ destination addresses, the DMA engine does not perform any data transfer and TE bit is set to 1. Third error source is the incorrect source/ destination burst length or data width configurations. If any of these four fields (SBL, DBL, SDW, DDW) is configured with reserved value, the DMA engine does not perform any data transfer and TE bit is set to 1.	0b
-	[15:0]	Reserved	0000h

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3.8.3.8 DMA Transfer Direction Register (DMA_TRANS_DIR, R/W, Address = 0xB060_0420)

DMA_TRANS_DIR	Bit	Description	Initial State
-	[31:1]	Reserved	-
TDIR	[0]	**Transfer Direction** This bit specifies the transfer direction of the DMA operation between the OneNAND controller's internal AHB memory and the OneNAND controller's external AHB memory. 0b = OneNAND controller read (Internal AHB memory to external AHB memory) 1b = OneNAND controller write (External AHB memory to internal AHB memory)	0b

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3.8.4 INTERRUPT CONTROLLER REGISTERS

Interrupt controller registers can be classified into following four register types: 1) interrupt pending registers, 2) interrupt status registers, 3) interrupt mask registers, and 4) interrupt clear registers.

Each interrupt pending register represents the raw status of the interrupt sources such as DMA transfer done, DMA transfer error, and OneNAND INT pin done. Interrupt pending register is the exact copy of the peripheral device status registers (ONENAND_IF_STATUS, DMA_TRANS_STATUS, and SQC_STATUS). Therefore, if the raw status bit of the peripheral device status register is cleared by writing a clear command to the peripheral device command register (ONENAND_IF_CMD, DMA_TRANS_CMD, and SQC_CMD), the corresponding bit of the interrupt pending register is also cleared automatically.

For example, let us consider a DMA operation scenario, in which the DMA engine generates an interrupt and this interrupt is cleared.

After DMA transfer is successfully completed, the TD (Transfer Done) bit of DMA Transfer Status Register (DMA_TRANS_STATUS) is set to 1. Simultaneously, the DPTD (DMA Pending Transfer Done) bit of Interrupt Controller DMA Pending Register (INTC_DMA_PEND) is also set to 1. On the other hand, interrupt controller status registers represent the interrupt sources, which actually generate an interrupt after the masking logic. If the DMTD (DMA Mask Transfer Done) bit of Interrupt Controller DMA Mask Register (INTC_DMA_MASK) is 0, the DSTD (DMA Status Transfer Done) bit of the Interrupt Controller DMA Status Register (INTC_DMA_STATUS) is set to 1 because this interrupt source is not masked. Now, the ARM_IRQ pin of the OneNAND controller is asserted to 1 and an interrupt is generated by the OneNAND controller. Note that the ARM_IRQ pin is OR-ed value of all the bits of interrupt controller status registers (INTC_SQC_STATUS, INTC_DMA_STATUS, and INTC_ONENAND_STATUS) and that this output is asserted if any bit of theses registers is set to 1.

To handle this interrupt in a system, the ISR (interrupt service routine) should perform as follows. The TD (Transfer Done) bit of DMA Transfer Status Register (DMA_TRANS_STATUS) must be cleared to 0 by writing 1 to the TDC (Transfer Done Clear) bit of DMA Transfer Command Register (DMA_TRANS_CMD). And then, the DSTD (DMA Status Transfer Done) bit of the Interrupt Controller DMA Status Register (INTC_DMA_STATUS) must be cleared to 0 by writing 1 to the DCTD (DMA Clear Transfer Done) bit of the Interrupt Controller DMA Clear Register (INTC_DMA_CLR).

3.8.4.1 Interrupt Controller DMA Clear Register (INTC_DMA_CLR, W, Address = 0xB060_1004)

INTC_DMA_CLR	Bit	Description	Initial State
-	[31:25]	Reserved	-
DCTD	[24]	**DMA Clear Transfer Done** When this bit is set to 1, the DSTD (DMA status transfer done) bit flag of the Interrupt Controller DMA Status Register (INTC_DMA_STATUS) in the interrupt controller is cleared to 0	0b
-	[13:17]	Reserved	-
DCTE	[16]	**DMA Clear Transfer Error** When this bit is set to 1, the DPTE (DMA status transfer error) bit flag of the Interrupt Controller DMA Status Register (INTC_DMA_STATUS) in the interrupt controller is cleared to 0	0b
-	[15:0]	Reserved	-

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3.8.4.2 Interrupt Controller OneNAND Clear Register (INTC_ONENAND_CLR, W, Address = 0xB060_1008)

INTC_ONENAND_CLR	Bit	Description	Initial State
-	[31:2]	Reserved	-
OCINTD	[1:0]	**OneNAND Clear INT Done** When this bit is set to 1, the corresponding OSINTD (OneNAND status INT done) bit flag of the Interrupt Controller OneNAND Status Register (INTC_ONENAND_STATUS) in the interrupt controller is cleared to 0. Each bit corresponds to each OneNAND chip. For example, writing 1 to OCINTD[0] bit clears OSINTD[0] for OneNAND chip #0.	00b

3.8.4.3 Interrupt Controller DMA Mask Register (INTC_DMA_MASK, R/W, Address = 0xB060_1024)

INTC_DMA_MASK	Bit	Description	Initial State
-	[31:25]	Reserved	-
DMTD	[24]	**DMA Mask Transfer Done** When this bit is set to 1, the DSTD (DMA status transfer done) bit flag of the Interrupt Controller DMA Status Register (INTC_DMA_STATUS) in the interrupt controller is disabled to generate an interrupt.	1b
-	[13:17]	Reserved	-
DMTE	[16]	**DMA Mask Transfer Error** When this bit is set to 1, the DPTE (DMA status transfer error) bit flag of the Interrupt Controller DMA Status Register (INTC_DMA_STATUS) in the interrupt controller is disabled to generate an interrupt.	1b
-	[15:0]	Reserved	-

3.8.4.4 Interrupt Controller OneNAND Mask Register (INTC_ONENAND_MASK, R/W, Address = 0xB060_1028)

INTC_ONENAND_MASK	Bit	Description	Initial State
-	[31:2]	Reserved	-
OMINTD	[1:0]	**OneNAND Mask INT Done** When this bit is set to 1, the corresponding OSINTD (OneNAND status INT done) bit flag of the Interrupt Controller OneNAND Status Register (INTC_ONENAND_STATUS) in the interrupt controller is disabled to generate an interrupt. Each bit corresponds to each OneNAND chip. For example, writing a 1 to OMINTD[0] bit disables OSINTD[0] to generate an interrupt for OneNAND chip #0.	11b

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3.8.4.5 Interrupt Controller DMA Pending Register (INTC_DMA_PEND, R, Address = 0xB060_1044)

INTC_DMA_PEND	Bit	Description	Initial State
-	[31:25]	Reserved	-
DPTD	[24]	**DMA Pending Transfer Done** This bit is the exact copy of the TD (transfer done) bit flag of the DMA Status Register (DMA_STATUS)	0b
-	[13:17]	Reserved	-
DPTE	[16]	**DMA Pending Transfer Error** This bit is the exact copy of the TE (transfer error) bit flag of the DMA status register (DMA_STATUS)	0b
-	[15:0]	Reserved	-

3.8.4.6 Interrupt Controller OneNAND Pending Register (INTC_ONENAND_PEND, R, Address = 0xB060_1048)

INTC_ONENAND_PEND	Bit	Description	Initial State
-	[31:8]	Reserved	-
-	[7:2]	Reserved	111111b
OPINTD	[1:0]	**OneNAND Pending INT Done** This bits are the exact copy of the INTD (INT done) bit flag of the OneNAND Interface Status Register (ONENAND_IF_STATUS)	11b

3.8.4.7 Interrupt Controller DMA Status Register (INTC_DMA_STATUS, R, Address = 0xB060_1064)

INTC_DMA_STATUS	Bit	Description	Initial State
-	[31:25]	Reserved	-
DSTD	[24]	**DMA Status Transfer Done** This bit is logical AND operation result of DPTD (DMA pending transfer done) bit flag of the interrupt controller DMA pending register (INTC_DMA_PEND) and inverse of DMTD (DMA mask transfer done) bit flag of the Interrupt Controller DMA Mask Register (INTC_DMA_MASK)	0b
-	[13:17]	Reserved	-
DSTE	[16]	**DMA Status Transfer Error** This bit is logical AND operation result of DPTE (DMA pending transfer error) bit flag of the interrupt controller DMA pending register (INTC_DMA_PEND) and inverse of DMTE (DMA mask transfer error) bit flag of the Interrupt Controller DMA Mask Register (INTC_DMA_MASK)	0b
-	[15:0]	Reserved	-

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3.8.4.8 Interrupt Controller OneNAND Status Register (INTC_ONENAND_STATUS, R, Address = 0xB060_1068)

INTC_ONENAND_ STATUS	Bit	Description	Initial State
-	[31:2]	Reserved	-
OSINTD	[1:0]	**OneNAND Status INT Done** This bits are logical AND operation result of OPINTD (OneNAND pending INT done) bit flags of the interrupt controller OneNAND pending register (INTC_ONENAND_PEND) and inverse of OMINTD (OneNAND mask INT done) bit flag of the Interrupt Controller OneNAND Mask Register (INTC_ONENAND_MASK)	00b

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4 NAND FLASH CONTROLLER

4.1 OVERVIEW OF NAND FLASH CONTROLLER

Owing to the recent increase in the prices of NOR flash memory and the moderately priced DRAM and NAND flash, customers prefer to execute boot code on NAND flash and execute the main code on DRAM.

The boot code in S5PV210 can be executed on external NAND flash. It will copy NAND flash data to DRAM. To validate the NAND flash data, S5PV210 comprises of hardware Error Correction Code (ECC). After the NAND flash content is copied to DRAM, main program will be executed on DRAM.

4.2 KEY FEATURES OF NAND FLASH CONTROLLER

The key features of NAND flash controller include:

- NAND flash memory interface: Supports 512Bytes, 2KB, 4KB, and 8KB pages.
- Software mode: You can directly access NAND flash memory, for example, this feature can be used in read/ erase/ program NAND flash memory.
- Interface: Supports 8-bit NAND flash memory interface bus.
- Generates, detects, and indicates hardware ECC (Software correction).
- Supports both SLC and MLC NAND flash memories.
- ECC: Supports 1-/ 4-/ 8-/ 12-/ 16-bit ECC
- SFR interface: Supports byte/ half word/ word access to Data and ECC data registers, and Word access to other registers.

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4.2.1 BLOCK DIAGRAM

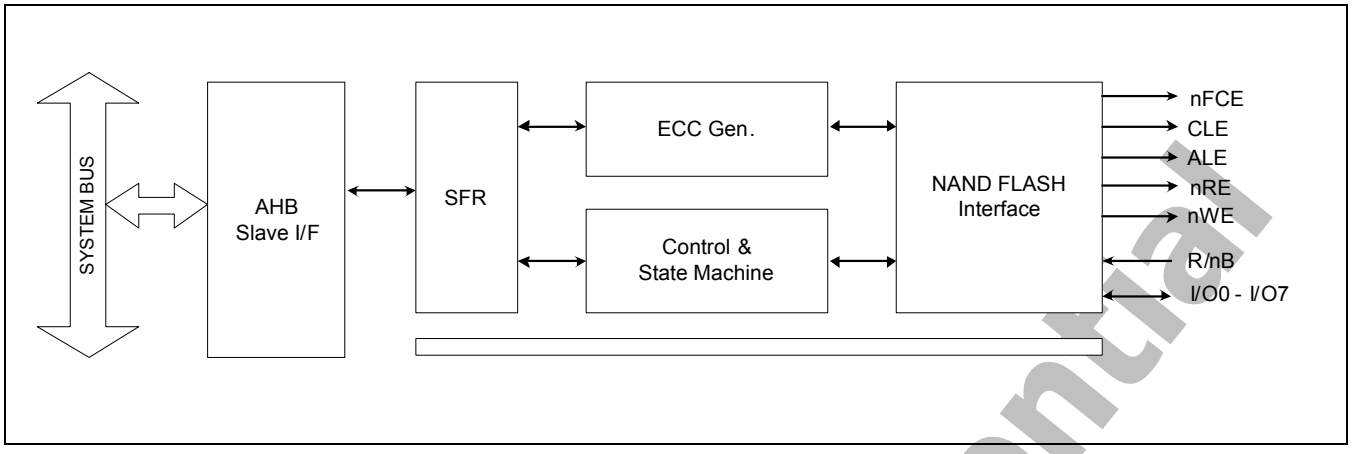

Figure 4-1 NAND Flash Controller Block Diagram

4.2.2 NAND FLASH MEMORY TIMING

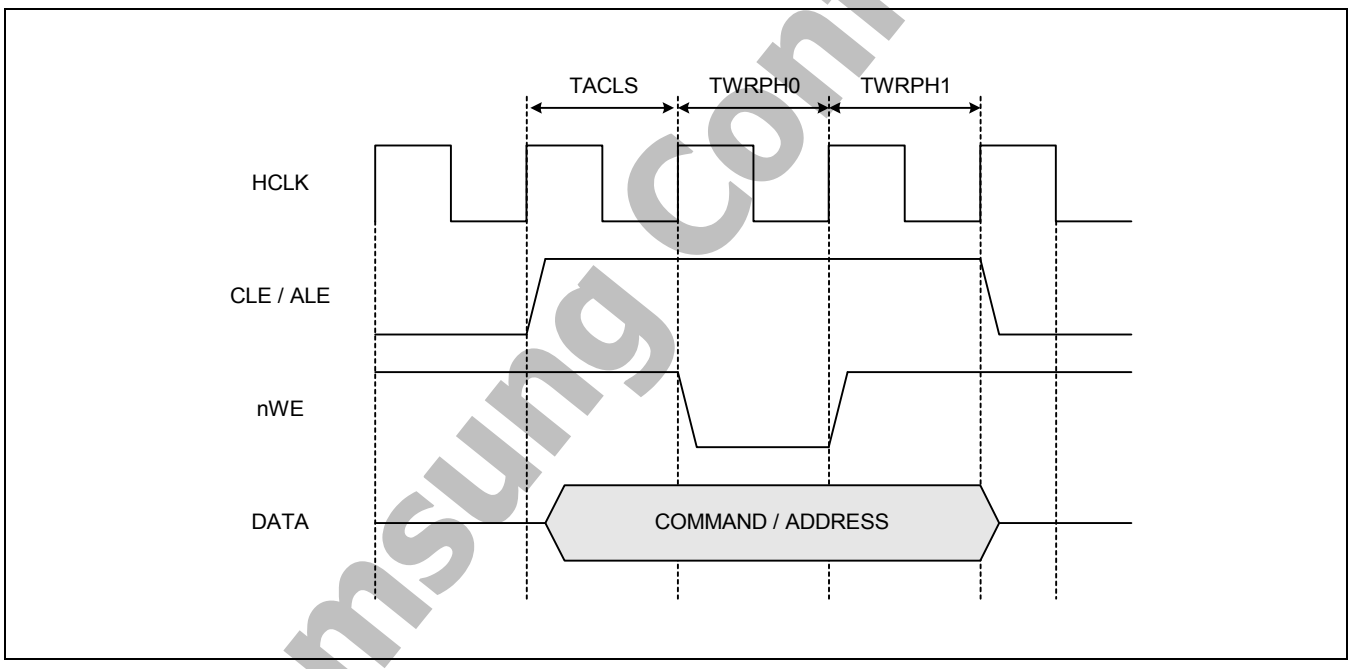

Figure 4-2 CLE and ALE Timing (TACLS=1, TWRPH0=0, TWRPH1=0)

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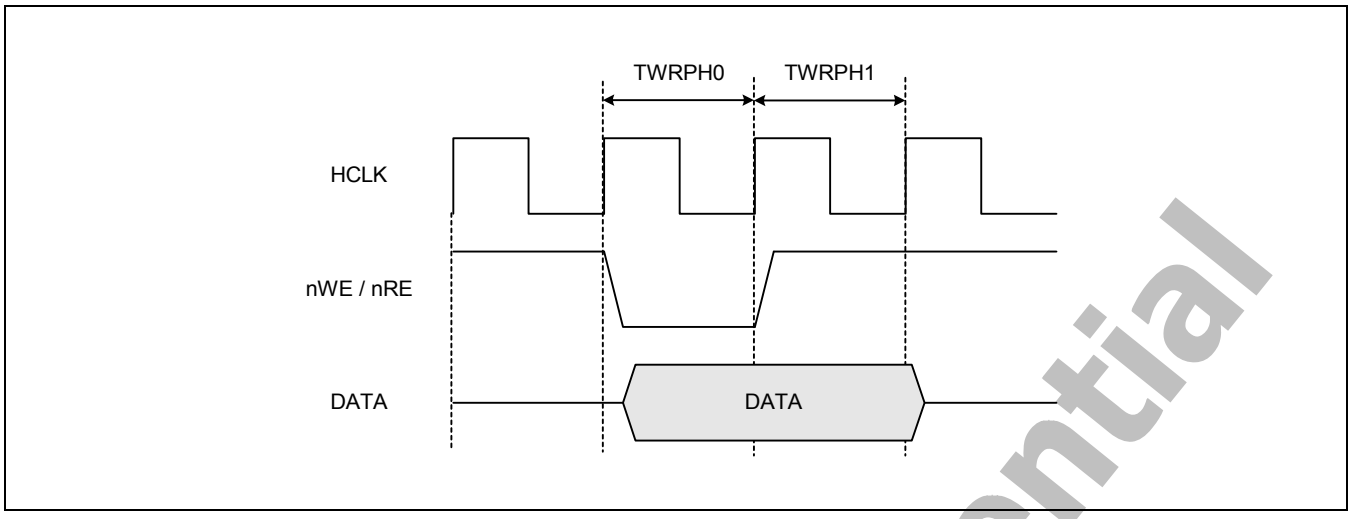

Figure 4-3 nWE and nRE Timing (TWRPH0=0, TWRPH1=0)

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4.3 SOFTWARE MODE

S5PV210 supports only software mode access. Use this mode to access NAND flash memory. The NAND flash controller supports direct access to interface with the NAND flash memory.

- Writing to the command register (NFCMMD) specifies the NAND Flash Memory command cycle
- Writing to the address register (NFADDR) specifies the NAND Flash Memory address cycle
- Writing to the data register (NFDATA) specifies write data to the NAND Flash Memory (write cycle)
- Reading from the data register (NFDATA) specifies read data from the NAND Flash Memory (read cycle)
- Reading main ECC registers (NFMECCD0/NFMECCD1) and Spare ECC registers (NFSECCD) specify read data from the NAND Flash Memory

NOTE: In the software mode, use polling or interrupt to check the RnB status input pin.

4.3.1 DATA REGISTER CONFIGURATION

4.3.1.1 8-bit NAND Flash Memory Interface

- A. Word Access

Register	Endian	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFDATA	Little	4th I/O[7:0]	3rd I/O[7:0]	2nd I/O[7:0]	1st I/O[7:0]

- B. Half-word Access

Register	Endian	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFDATA	Little	Invalid value	Invalid value	2nd I/O[7:0]	1st I/O[7:0]

- C. Byte Access

Register	Endian	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFDATA	Little	Invalid value	Invalid value	Invalid value	1st I/O[7:0]

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4.3.2 1-/ 4-/ 8-/ 12-/ 16-BIT ECC

NAND flash controller supports 1-/ 4-/ 8-/ 12-/ 16-bit ECC.

For 1-bit ECC, NAND flash controller comprises ECC modules for main and spare (meta) data. Main data ECC module generates ECC parity code for 2048 bytes (maximum) data/ message length, whereas spare (meta) data ECC module generates ECC Parity code for 32 bytes (maximum).

For 4-bit ECC, NAND flash controller comprises of an ECC module. It generates 512 or 24 bytes of ECC parity code. Set MsgLength (NFCONF[25]) to select 512 or 24 bytes message length.

For 8-/ 12-/ 16-bit ECC, NAND flash controller comprises ECC modules for each ECC. You can select data/ message length for main and spare (meta) data length. Usually, the length of main data is 512 bytes, and the length of spare (meta) data depends on user application.

Since these ECC modules support variable length of main and spare (meta) data, you must set the ECC parity conversion codes to handle free page (For more information on ECC parity conversion codes, refer to the *4.3.11*). Free page specifies an erased page. The value of erased page is '0xff'. Therefore, set the ECC parity conversion codes to generate '0xff' ECC parity codes for all '0xff' data. This allows ECC module to detect errors on a free page.

ECC parity codes are described as follows:

- 28-bit ECC Parity Code = 22-bit Line parity + 6-bit Column Parity
- 10-bit ECC Parity Code = 4-bit Line parity + 6bit Column Parity

Each 1-/ 4-/ 8-/ 12-/ 16-bit ECC module guarantees up to 1-/ 4-/ 8-/ 12-/ 16-bit errors, respectively. If the errors cross the number of guaranteed errors, the result cannot be guaranteed.

4.3.3 and *4.3.4* show 1-bit ECC parity code assignment.

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4.3.3 2048 BYTE 1-BIT ECC PARITY CODE ASSIGNMENT TABLE

	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
MECCn_0	~P64	~P64'	~P32	~P32'	~P16	~P16'	~P8	~P8'
MECCn_1	~P1024	~P1024'	~P512	~P512'	~P256	~P256'	~P128	~P128'
MECCn_2	~P4	~P4'	~P2	~P2'	~P1	~P1'	~P2048	~P2048'
MECCn_3	1	1	1	1	~P8192	~P8192'	~P4096	~P4096'

4.3.4 32 BYTE 1-BIT ECC PARITY CODE ASSIGNMENT TABLE

	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
SECCn_0	~P2	~P2'	~P1	~P1'	~P16	~P16'	~P8	~P8'
SECCn_1	~P128	~P128`	~P64	~P64`	~P32	~P32`	~P4	~P4'

4.3.5 1-BIT ECC MODULE FEATURES

The ECC Lock (MainECCLock and SpareECCLock) bit of the control register generates the 1-bit ECC. If ECCLock is low, the hardware ECC modules generate the ECC codes.

- 1-bit ECC Register Configuration

The following table shows the configuration of 1-bit ECC value read from spare area of external NAND flash memory. The format of ECC read from memory is important to compare the ECC parity code generated by the hardware modules.

NOTE: 4-bit/ 8-bit/ 12-bit/ 16-bit ECC decoding scheme is different compared to 1-bit ECC.

- NAND Flash Memory Interface

Register	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFMECCD0	Not used	2nd ECC	Not used	1st ECC
NFMECCD1	Not used	4th ECC	Not used	3rd ECC

Register	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFSECCD	Not used	2nd ECC	Not used	1st ECC

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4.3.6 1-BIT ECC PROGRAMMING GUIDE

1. To use SLC ECC in software mode, reset the ECCType to '0' (enable SLC ECC)'. ECC module generates ECC parity code for all read / write data when MainECCLock (NFCON[7]) and SpareECCLock (NFCON[6]) are unlocked('0'). You must reset ECC value. To reset ECC value write the InitMECC (NFCONT[5]) and InitSECC (NFCON[4]) bit as '1' and clear the MainECCLock (NFCONT[7]) bit to '0'(Unlock) before reading or writing data.
   MainECCLock (NFCONT[7]) and SpareECCLock(NFCONT[6]) bits control whether ECC Parity code is generated or not.
2. The ECC module generates ECC parity code on register NFMECC0/1 whenever data is read or written.
3. After you complete reading or writing one page (not including spare area data), set the MainECCLock bit to '1' (Lock). ECC Parity code is locked and the value of the ECC status register does not change.
4. To generate spare area ECC parity code, Clear SpareECCLock (NFCONT[6]) bit as '0' (Unlock).
5. The spare area ECC module generates ECC parity code on register NFSECC whenever data is read or written.
6. After you complete reading or writing spare area, set the SpareECCLock bit to '1' (Lock). ECC Parity code is locked and the value of the ECC status register will not be changed.
7. From now on, you can use these values to record to the spare area or check the bit error.
8. For example, to check the bit error of main data area on page read operation, you must move the ECC parity codes (is stored to spare area) to NFMECCD0 and NFMECCD1 after ECC codes for main data area is generated. From this point, the NFECCERR0 and NFECCERR1 have the valid error status values.

NOTE: NFSECCD is for ECC in the spare area (Usually, the user will write the ECC value generated from main data area to spare area, of which the value will be the same as NFMECC0/1) which is generated from the main data area.

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4.3.7 4-BIT ECC PROGRAMMING GUIDE (ENCODING)

1. To use 4-bit ECC in software mode, set the MsgLength to 0(512-byte message length) and the ECCType to “10”(enable 4bit ECC). ECC module generates ECC parity code for 512-byte write data. To reset ECC value write the InitMECC (NFCONT[5]) bit as ‘1’ and clear the MainECCLock (NFCONT[7]) bit to ‘0’(Unlock) before writing data.
   MainECCLock (NFCONT[7]) bit controls whether ECC Parity code is generated or not.

2. The 4-bit ECC module generates ECC parity code internally whenever data is written.

3. After you finish writing 512-byte data (not including spare area data), the parity codes are automatically updated to NFMECC0 and NFMECC1 registers. If you use 512-byte NAND Flash memory, you can program these values to spare area. However, if you use NAND Flash memory more than 512-byte page, you cannot program immediately. In this case, you have to copy these parity codes to other memory like DRAM. After writing all main data, you can write the copied ECC values to spare area.
   The parity codes have self-correctable information including parity code itself.

4. To generate spare area ECC parity code, set the MsgLength to 1(24-byte message length) and the ECCType to “10”(enable 4bit ECC). ECC module generates ECC parity code for 24-byte write data. To reset ECC value write the InitMECC (NFCONT[5]) bit as ‘1’ and clear the MainECCLock (NFCONT[7]) bit to ‘0’(Unlock) before writing data.
   MainECCLock (NFCONT[7]) bit controls whether ECC Parity code is generated or not.

5. Whenever data is written, the 4-bit ECC module generates ECC parity code internally.

6. When you finish writing 24-byte meta or extra data, the parity codes are automatically updated to NFMECC0 and NFMECC1 registers. You can program these parity codes to spare area.
   The parity codes have self-correctable information including parity code itself.

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4.3.8 4-BIT ECC PROGRAMMING GUIDE (DECODING)

1. To use 4-bit ECC in software mode, set the MsgLength to 0 (512-byte message length) and the ECCType to “10” (enable 4-bit ECC). ECC module generates ECC parity code for 512-byte read data. Therefore, to reset ECC value write the InitMECC (NFCONT[5]) bit as ‘1’ and clear the MainECCLock (NFCONT[7]) bit to ‘0’(Unlock) before reading data.
   MainECCLock (NFCONT[7]) bit controls whether ECC Parity code is generated or not.

2. Whenever data is read, the 4-bit ECC module generates ECC parity code internally.

3. After you complete reading 512-byte (not including spare area data), you must read parity codes. MLC ECC module needs parity codes to detect whether error bits have occurred or not. Therefore, you must read ECC parity code immediately after reading 512-byte. After ECC parity code is read, 4-bit ECC engine starts searching for error internally. 4-bit ECC error searching engine needs minimum of 155 cycles to find any error. During this time, you can continue reading main data from external NAND Flash memory. Use ECCDecDone(NFSTAT[6]) to check whether ECC decoding is completed or not.

4. When ECCDecDone (NFSTAT[6]) is set (‘1’), NFECCERR0 indicates whether error bit exists or not. If any error exists, refer NFECCERR0/1 and NFMLCBITPT registers to fix.

5. If you have more main data to read, go back to step 1.

6. To check meta data error, set the MsgLength to 1 (24-byte message length) and the ECCType to ‘1’ (enable 4-bit ECC). ECC module generates ECC parity code for 512-byte read data. Therefore, you must reset ECC value by writing the InitMECC (NFCONT[5]) bit as ‘1’ and clear the MainECCLock (NFCONT[7]) bit to ‘0’(Unlock) before reading data.
   MainECCLock (NFCONT[7]) bit controls whether ECC Parity code is generated or not.

7. Whenever data is read, the 4-bit ECC module generates ECC parity code internally.

8. After you complete reading 512-byte (not include spare area data), you must read parity codes. 4-bit ECC module needs parity codes to detect whether error bits have occurred or not. Therefore, ensure to read ECC parity codes immediately after reading 512-byte. After ECC parity code is read, 4-bit ECC engine starts searching for error internally. 4-bit ECC error searching engine needs minimum of 155 cycles to find any error. During this time, you can continue reading main data from external NAND Flash memory. Use ECCDecDone(NFSTAT[6]) to check whether ECC decoding is completed or not.

9. When ECCDecDone (NFSTAT[6]) is set (‘1’), NFECCERR0 indicates whether error bit exists or not. If any error exists, you can fix it by referring to NFECCERR0/1 and NFMLCBITPT registers.

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4.3.9 8-BIT / 12-BIT / 16-BIT ECC PROGRAMMING GUIDE (ENCODING)

1. To use 8/ 12/ 16-bit ECC in software mode, set the MsgLength(NFECCCONF[25:16]) to 511(512byte message length) and the ECCType to “001/100/101”(enable 8/12/16-bit ECC, respectively). ECC module generates ECC parity code for 512 byte write data. Therefore, reset ECC value by writing the InitMECC (NFECCCONT[2]) bit as ‘1’ before writing data, and clear the MainECCLock(NFCONT[7]) bit to ‘0’(Unlock) before writing data.

2. Whenever data is written, the corresponding 8/12/16-bit ECC module generates ECC parity code internally.

3. After you finish writing 512bbyte data (This does not include spare area data), the parity codes are automatically updated to the NFECCPRG0 ~ NFECCPRGECC6 registers. If you use a NAND Flash memory having 512 byte page, you can program these values to spare area. However, if you use a NAND Flash memory more than 512-byte page, you cannot program immediately. In this case, you must copy these ECC parity codes to other memory like DRAM. After writing all main data, you can write the copied ECC values to spare area.

   The parity codes have self-correctable information including parity code itself.

   Table below shows the ECC parity size:

ECC type	Size of ECC Parity Codes
8-bit ECC	13 byte
12-bit ECC	20 byte
16-bit ECC	26 byte

4. To generate spare area ECC parity code for meta data, the steps are same (from 1 ~ 3), except setting the MsgLenght(NFECCCONF[25:16]) to the size that you prefer. When you set InitMECC(NFECCCONT[2]), all ECC parity codes generated for main data are cleared. Therefore, you should copy the ECC parity codes for main data.

NOTE: You should set the ECC parity conversion codes to check free page error. For more information about, refer to 4.3.11

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4.3.10 8/12/16-BIT ECC PROGRAMMING GUIDE (DECODING)

1. To use 8/ 12/ 16-bit ECC in software mode, set the MsgLength(NFECCCONF[25:16] to 511(512-byte message length) and the ECCType to “001/100/101”(enable 8/12/16-bit ECC, respectively). ECC module generates ECC parity code for 512-byte read data. Therefore, you must reset ECC value by writing the InitMECC (NFECCCONT[2]) bit as ‘1’, and clear the MainECCLock(NFCONT[7]) bit to ‘0’(Unlock) before read data.

2. Whenever data is read, the 8/12/16-bit ECC module generates ECC parity code internally.

3. After you complete reading 512-byte (not including spare area data), ensure to read the corresponding parity codes. ECC module needs parity codes to detect whether error bits have occurred or not. Therefore, you have to read ECC parity code immediately after reading 512-byte. After ECC parity code is read, the 8/12/16-bit ECC engine searches for error internally. 8/12/16-bit ECC search engine needs minimum of 155 cycles to find any errors. DecodeDone(NFECCSTAT[24]) can be used to check whether ECC decoding is completed or not.

4. When DecodeDone (NFECCSTAT[24]) is set (‘1’), ECCError(NFECCSECSTAT[4:0]) indicates whether error bit exists or not. If any error exists, you can fix it by referencing NFECCERL0~NFECCERL7 and NFECCERP0 ~ NFECCERP3 registers.

5. If you have additional main data to read, continue the steps 1 ~ 4.

6. To check spare area data (meta data) error, the sequences are same (steps 1 ~ 4), except setting the MsgLenght(NFECCCONF[25:16]) to the size that you want.

NOTE: You should set the ECC parity conversion codes to check free page error. For more information, refer to refer to 4.3.11 .

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4.3.11 ECC PARITY CONVERSION CODE GUIDE FOR 8/12/16-BIT ECC

The ECC parity conversion codes are there to fix errors, which occur when reading a free page. Free page means the page erased. The 8/ 12/ 16-bit ECC modules support variable message size for meta data stored in spare area. Generally, the size of main data (sector) is 512-byte and user should set the corresponding ECC parity conversion codes as shown in Table below.

ECC type	ECC Parity Conversion Codes
8-bit ECC	Here, 13 byte ECC parity conversion codes
12-bit ECC	Here, 20 byte ECC parity conversion codes
16-bit ECC	Here, 26 byte ECC parity conversion codes

The message size for meta data stored spare area can be different depending on user's needs. Hence, you can change the size of meta data by changing MsgLength(NFECCCONF[25:16]) and change ECC parity conversion codes.

Steps to know ECC parity conversion codes according to the size of message length:

1. Clear all ECC parity conversion registers (NFECCCONECC0 ~ NFECCCONECC6) as all zero.
2. Set all registers for page program
3. Reset InitMECC (NFECCCONT[2] bit as '1'
4. Write '0xff' data as much as the size of meta data.
5. After you write data as MsgLength(NFECCCONF[25:16]), the EncodeDone(NFECCSTAT[25]) is set as '1' and generates the corresponding ECC parity codes.
6. Set ECC parity conversion registers as inverted values of ECC parity codes generated.
   For testing if these ECC parity conversion codes work well, repeat step 3 ~ 5. After you set ECC parity conversion codes, if the generated ECC parity code are all '0xff', then it is working correctly.

Constraints to support free page function:

- Free page check is for only data area (512-byte)
- If there is an error during reading a page erased (free page), then free page engine indicates that the page is not free page.
- To detect error(s) on free page, user should set corresponding conversion codes.

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4.3.12 LOCK SCHEME FOR DATA PROTECTION

NFCON provides a lock scheme to protect data stored in external NAND Flash memories from malicious program.

For this scheme, the NFSBLK and NFEBLK registers are used to provide access control methods; only the memory area between NFSBLK and NFEBLK is erasable and programmable, but the read access is available to whole memory area.

This lock scheme is only available when you enable LockTight(NFCONT[17]) and LOCK(NFCONT[16]).

1. **Unlock mode**

   In unlock mode, user can access whole NAND memory; there are no constraints to access memory.

2. **Soft lock mode**

   In soft lock mode, you can access NAND block area between NFSBLK and NFEBLK.
   When you try to program or erase the locked area, an illegal access error will occur (NFSTAT [5] bit will be set).

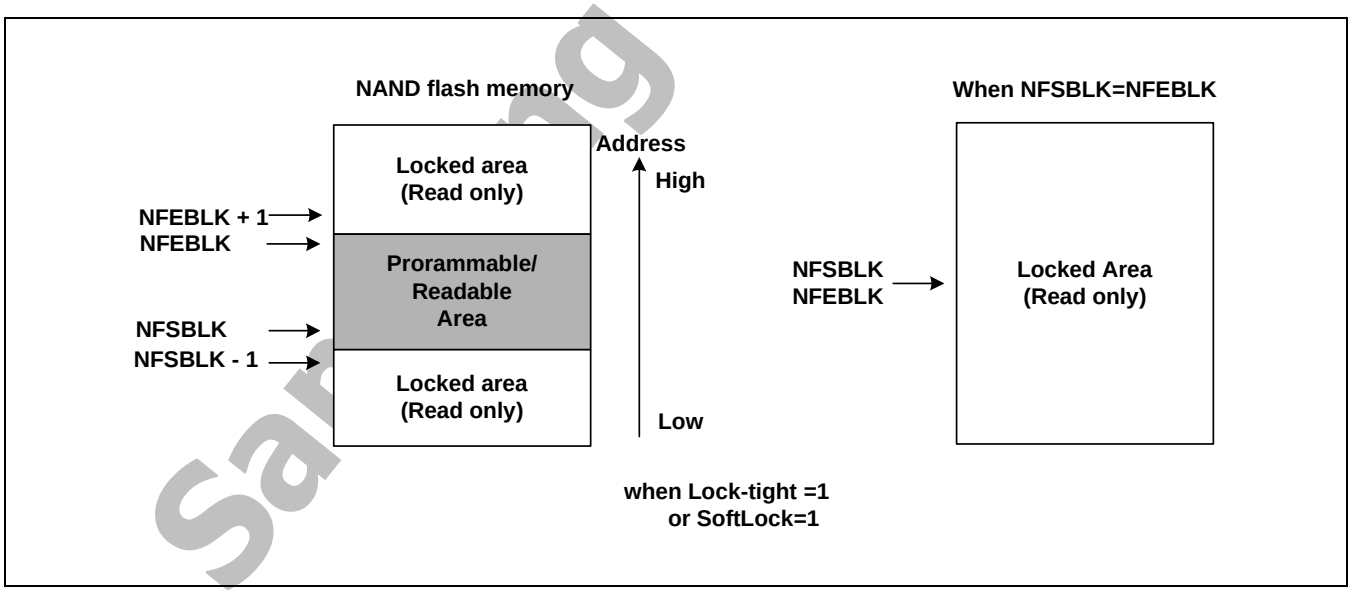
3. **Lock-tight mode**

   In lock-tight mode, you can access NAND block area between NFSBLK and NFEBLK as soft lock mode. The differences is that you cannot change NFSBLK and NFEBLK registers, and also LOCK(NFCONT[16]) and LockTight(NFCONT[17]) bits.

When you try to program or erase the locked area, an illegal access error will occur (NFSTAT[5] bit will be set).

The LockTight(NFCONT[17]) bit is only cleared when reset or wake up from sleep mode (It is impossible to clear it by software).

The accessibility of NAND area is illustrated in the figure below.



NOTE: If the address of NFSBLK and NFEBLK are same, then the erase and program to all NAND memory are not allowed.

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4.4 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
Xm0DATA	Input / Output	Address / Data Bus	Xm0DATA	muxed
Xm0FRnB[3:0]	Input	Ready and Busy	Xm0FRnB	muxed
Xm0FCLE	Output	Command Latch Enable	Xm0FCLE	muxed
Xm0FALE	Output	Address Latch Enable	Xm0FALE	muxed
Xm0CSn[2:5]	Output	Chip Enable	Xm0CSn	muxed
Xm0FREn	Output	Read Enable	Xm0FREn	muxed
Xm0FWEn	Output	Write Enable	Xm0FWEn	muxed

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4.5 REGISTER DESCRIPTION

4.5.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
NFCONF	0xB0E0_0000	R/W	Configuration Register	0x0000_1000
NFCONT	0xB0E0_0004	R/W	Control Register	0x00C1_00C6
NFCMMD	0xB0E0_0008	R/W	Command Register	0x0000_0000
NFADDR	0xB0E0_000C	R/W	Address Register	0x0000_0000
NFDATA	0xB0E0_0010	R/W	Data Register	0x0000_0000
NFMECCD0	0xB0E0_0014	R/W	1st and 2nd Main ECC Data Register	0x0000_0000
NFMECCD1	0xB0E0_0018	R/W	3rd and 4th Main ECC Data Register	0x0000_0000
NFSECCD	0xB0E0_001C	R/W	Spare ECC Read Register	0xFFFF_FFFF
NFSBLK	0xB0E0_0020	R/W	Programmable Start Block Address Register	0x0000_0000
NFEBLK	0xB0E0_0024	R/W	Programmable End Block Address Register	0x0000_0000
NFSTAT	0xB0E0_0028	R/W	NAND Status Registet	0xF080_0F0D
NFECCERR0	0xB0E0_002C	R	ECC Error Status0 Register	0x0003_FFF2
NFECCERR1	0xB0E0_0030	R	ECC Error Status1 Register	0x0000_0000
NFMECC0	0xB0E0_0034	R	Generated ECC Status0 Register	0xFFFF_FFFF
NFMECC1	0xB0E0_0038	R	Generated ECC Status1 Register	0xFFFF_FFFF
NFSECC	0xB0E0_003C	R	Generated Spare Area ECC Status Register	0xFFFF_FFFF
NFMLCBITPT	0xB0E0_0040	R	4-bit ECC Error Bit Pattern Register	0x0000_0000
8/ 12/ 16-bit ECC Register Map				
NFECCCONF	0xB0E2_0000	R/W	ECC Configuration Register	0x0000_0000
NFECCCONT	0xB0E2_0020	R/W	ECC Control Register	0x0000_0000
NFECCSTAT	0xB0E2_0030	R	ECC Status Register	0x0000_0000
NFECCSECSTAT	0xB0E2_0040	R	ECC Sector Status Register	0x0000_0000
NFECCPRGECC0	0xB0E2_0090	R	ECC Parity Code0 Register for Page program	0x0000_0000
NFECCPRGECC1	0xB0E2_0094	R	ECC Parity Code1 Register for Page Program	0x0000_0000
NFECCPRGECC2	0xB0E2_0098	R	ECC parity code2 register for page program	0x0000_0000
NFECCPRGECC3	0xB0E2_009C	R	ECC parity code3 register for page program	0x0000_0000
NFECCPRGECC4	0xB0E2_00A0	R	ECC parity code4 register for page program	0x0000_0000
NFECCPRGECC5	0xB0E2_00A4	R	ECC parity code5 register for page program	0x0000_0000
NFECCPRGECC6	0xB0E2_00A8	R	ECC parity code6 register for page program	0x0000_0000
NFECCERL0	0xB0E2_00C0	R	ECC error byte location0 register	0x0000_0000
NFECCERL1	0xB0E2_00C4	R	ECC error byte location1 register	0x0000_0000
NFECCERL2	0xB0E2_00C8	R	ECC error byte location2 register	0x0000_0000
NFECCERL3	0xB0E2_00CC	R	ECC error byte location3 register	0x0000_0000

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Register	Address	R/W	Description	Reset Value
NFECCERL4	0xB0E2_00D0	R	ECC error byte location4 register	0x0000_0000
NFECCERL5	0xB0E2_00D4	R	ECC error byte location5 register	0x0000_0000
NFECCERL6	0xB0E2_00D8	R	ECC error byte location6 register	0x0000_0000
NFECCERL7	0xB0E2_00DC	R	ECC error byte location7 register	0x0000_0000
NFECCERP0	0xB0E2_00F0	R	ECC error bit pattern0 register	0x0000_0000
NFECCERP1	0xB0E2_00F4	R	ECC error bit pattern1 register	0x0000_0000
NFECCERP2	0xB0E2_00F8	R	ECC error bit pattern2 register	0x0000_0000
NFECCERP3	0xB0E2_00FC	R	ECC error bit pattern3 register	0x0000_0000
NFECCCONECC0	0xB0E2_0110	R/W	ECC parity conversion code0 register	0x0000_0000
NFECCCONECC1	0xB0E2_0114	R/W	ECC parity conversion code1 register	0x0000_0000
NFECCCONECC2	0xB0E2_0118	R/W	ECC parity conversion code2 register	0x0000_0000
NFECCCONECC3	0xB0E2_011C	R/W	ECC parity conversion code3 register	0x0000_0000
NFECCCONECC4	0xB0E2_0120	R/W	ECC parity conversion code4 register	0x0000_0000
NFECCCONECC5	0xB0E2_0124	R/W	ECC parity conversion code5 register	0x0000_0000
NFECCCONECC6	0xB0E2_0128	R/W	ECC parity conversion code6 register	0x0000_0000

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4.5.2 NAND FLASH INTERFACE AND 1 / 4-BIT ECC REGISTERS

4.5.2.1 Nand Flash Configuration Register (NFCONF, R/W, Address = 0xB0E0_0000)

NFCONF	Bit	Description	Initial State
Reserved	[31:26]	Reserved	0
MsgLength	[25]	0 = 512 byte Message Length 1 = 24 byte Message Length	0
ECCType0	[24:23]	This bit indicates the kind of ECC to use. 00 = 1-bit ECC 10 = 4-bit ECC 01 = 11 = Disable 1-bit and 4-bit ECC	0
Reserved	[22:16]	Reserved	0000000
TACLS	[15:12]	CLE and ALE duration setting value (0~15) Duration = HCLK x TACLS	0x1
TWRPH0	[11:8]	TWRPH0 duration setting value (0~15) Duration = HCLK x (TWRPH0 + 1) Note: You should add additional cycles about 10ns for page read because of additional signal delay on PCB pattern.	0x0
TWRPH1	[7:4]	TWRPH1 duration setting value (0~15) Duration = HCLK x (TWRPH1 + 1)	0x0
MLCFlash	[3]	This bit indicates the kind of NAND Flash memory to use. 0 = SLC NAND Flash 1 = MLC NAND Flash	0
PageSize	[2]	This bit indicates the page size of NAND Flash Memory, When MLCFlash is 0, the value of PageSize is as follows: 0 = 2048 Bytes/page 1 = 512 Bytes/page When MLCFlash is 1, the value of PageSize is as follows: 0 = 4096 Bytes/page 1 = 2048 Bytes/page	0
AddrCycle	[1]	This bit indicates the number of Address cycle of NAND Flash memory. When Page Size is 512 Bytes, 0 = 3 address cycle 1 = 4 address cycle When page size is 2K or 4K, 0 = 4 address cycle 1 = 5 address cycle	0
Reserved	[0]	Reserved	0

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4.5.2.2 Control Register (NFCONT, R/W, Address = 0xB0E0_0004)

NFCONT	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
Reg_nCE3	[23]	NAND Flash Memory nRCS[3] signal control 0 = Force nRCS[3] to low (Enable chip select) 1 = Force nRCS[3] to High (Disable chip select)	1
Reg_nCE2	[22]	NAND Flash Memory nRCS[2] signal control 0 = Force nRCS[2] to low (Enable chip select) 1 = Force nRCS[2] to High (Disable chip select)	1
Reserved	[21:19]	Reserved	0
MLCEccDirection	[18]	4-bit, ECC encoding / decoding control 0 = Decoding 4-bit ECC, It is used for page read 1 = Encoding 4-bit ECC, It is be used for page program	0
LockTight	[17]	Lock-tight configuration 0 = Disable lock-tight 1 = Enable lock-tight, If this bit is set to 1, you cannot clear this bit. For more information, refer to the *4.3.12 "Lock scheme for data protection"*.	0
LOCK	[16]	Soft Lock configuration 0 = Disable lock 1 = Enable lock Software can modify soft lock area any time. For more information, refer to the *4.3.12 "*.	1
Reserved	[15:14]	Reserved	00
EnbMLCEncInt	[13]	4-bit ECC encoding completion interrupt control 0 = Disable interrupt 1 = Enable interrupt	0
EnbMLCDecInt	[12]	4-bit ECC decoding completion interrupt control 0 = Disable interrupt 1 = Enable interrupt	0
	[11]	Reserved	0
EnbIllegalAccINT	[10]	Illegal access interrupt control 0 = Disable interrupt 1 = Enable interrupt Illegal access interrupt occurs when CPU tries to program or erase locking area (the area setting in NFSBLK (0xB0E0_0020) to NFEBLK (0xB0E0_0024)-1.	0
EnbRnBINT	[9]	RnB status input signal transition interrupt control 0 = Disable RnB interrupt 1 = Enable RnB interrupt	0
RnB_TransMode	[8]	RnB transition detection configuration 0 = Detect rising edge 1 = Detect falling edge	0

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NFCONT	Bit	Description	Initial State
MECCLock	[7]	Lock Main area ECC generation 0 = Unlock Main area ECC 1 = Lock Main area ECC Main area ECC status register is NFMECC0/NFMECC1(0xB0E0_0034/0xB0E0_0038),	1
SECCLock	[6]	Lock Spare area ECC generation. 0 = Unlock Spare ECC 1 = Lock Spare ECC Spare area ECC status register is NFSECC(0xB0E0_003C),	1
InitMECC	[5]	1 = Initialize main area ECC decoder/encoder (write-only)	0
InitSECC	[4]	1 = Initialize spare area ECC decoder/encoder (write-only)	0
HW_nCE	[3]	Reserved (HW_nCE)	0
Reg_nCE1	[2]	NAND Flash Memory nRCS[1] signal control	1
Reg_nCE0	[1]	NAND Flash Memory nRCS[0] signal control 0 = Force nRCS[0] to low (Enable chip select) 1 = Force nRCS[0] to High (Disable chip select) Note: The setting all nCE[3:0] zero can not be allowed. Only one nCE can be asserted to enable external NAND flash memory. The lower bit has more priority when user set all nCE[3:0] zeros.	1
MODE	[0]	NAND Flash controller operating mode 0 = Disable NAND Flash Controller 1 = Enable NAND Flash Controller	0

4.5.2.3 Command Register (NFCMMD, R/W, Address = 0xB0E0_0008)

NFCMMD	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0x000000
REG_CMMD	[7:0]	NAND Flash memory command value	0x00

4.5.2.4 Address Register (NFADDR, R/W, Address = 0xB0E0_000C)

NFADDR	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0x000000
REG_ADDR	[7:0]	NAND Flash memory address value	0x00

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4.5.2.5 Data Register (NFDATA, R/W, Address = 0xB0E0_0010)

NFDATA	Bit	Description	Initial State
NFDATA	[31:0]	NAND Flash read/ program data value for I/O Note: For more information, refer to 4.3.1 Data Register Configuration in page 4-4.	0x00000000

4.5.2.6 Main Data Area ECC Register (NFMECCD0, R/W, Address = 0xB0E0_0014)

NFMECCD0	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
ECCData1 (ECC1)	[23:16]	2nd ECC Note: In software mode, read this register when you need to read 2nd ECC value from NAND Flash memory	0x00
Reserved	[15:8]	Reserved	0x00
ECCData0 (ECC0)	[7:0]	1st ECC Note: In software mode, read this register when you need to read 1st ECC value from NAND flash memory. This register has the same read function as NFDATA.	0x00

NOTE: Only word access is allowed.

4.5.2.7 Main Data Area ECC Register (NFMECCD0, R/W, Address = 0xB0E0_0018)

NFMECCD1	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
ECCData3 (ECC3)	[23:16]	4th ECC Note: In software mode, read this register when you need to read 4th ECC value from NAND Flash memory	0x00
Reserved	[15:8]	Reserved	0x00
ECCData2 (ECC2)	[7:0]	3rd ECC Note: In software mode, read this register when you need to read 3rd ECC value from NAND Flash memory. This register has the same read function as NFDATA.	0x00

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4.5.2.8 Only Word Access is Allowed Spare Area ECC Register (NFSECCD, R/W, Address = 0xB0E0_001C)

NFSECCD	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
SECCData1	[23:16]	2nd ECC Note: In software mode, read this register when you need to read 2nd ECC value from NAND Flash memory	0xFF
Reserved	[15:8]	Reserved	0x00
SECCData0	[7:0]	1st ECC Note: In software mode, read this register when you need to read 1st ECC value from NAND Flash memory. This register has the same read function as NFDATA.	0xFF

NOTE: Only word access is allowed.

4.5.2.9 Programmable Start Block Address Register (NFSBLK, R/W, Address = 0xB0E0_0020)

NFSBLK	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
SBLK_ADDR2	[23:16]	The 3rd block address of the block erase operation	0x00
SBLK_ADDR1	[15:8]	The 2nd block address of the block erase operation	0x00
SBLK_ADDR0	[7:0]	The 1st block address of the block erase operation (Only bit [7:5] are valid)	0x00

NOTE: Advance Flash's block Address start from 3-address cycle. So block address register only needs 3-bytes. For more information about lock scheme, refer to the 4.3.12 .

4.5.2.10 Programmable End Block Address Register (NFEBLK, R/W, Address = 0xB0E0_0024)

NFEBLK	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
EBLK_ADDR2	[23:16]	The 3rd block address of the block erase operation	0x00
EBLK_ADDR1	[15:8]	The 2nd block address of the block erase operation	0x00
EBLK_ADDR0	[7:0]	The 1st block address of the block erase operation (Only bit [7:5] are valid)	0x00

NOTE: Advance Flash's block Address start from 3-address cycle. So block address register only needs 3-bytes. For more information about lock scheme, refer to the 4.3.12 .

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4.5.2.11 NFCON Status Register (NFSTAT, R/W, Address = 0xB0E0_0028)

NFSTAT	Bit	Description	Initial State
Flash_RnB_GRP	[31:28]	The status of RnB[3:0] input pin. 0 = NAND Flash memory busy 1 = NAND Flash memory ready to operate	0xF
RnB_TransDetect_GRP	[27:24]	When RnB[3:0] low to high transition occurs, this bit is set and an interrupt is issued if RnB_TransDetect_GRP is enabled. To clear this, write '1'. 0 = RnB transition is not detected 1 = RnB transition is detected Transition configuration is set in RnB_TransMode(NFCONT[8]).	
Reserved	[23:12]	Reserved	0x800
Flash_nCE[3:0] (Read-only)	[11:8]	The status of nCE[3:0] output pin.	0xF
MLCEncodeDone	[7]	When 4-bit ECC encodng is finished, this bit is set and an interrupt is issued if MLCEncodeDone is enabled. The NFMLCECC0 and NFMLCECC1 have valid values. To clear this, write '1'. 1 = 4-bit ECC encoding is completed	0
MLCDecodeDone	[6]	When 4-bit ECC decoding is finished, this bit is set and an interrupt is issued if MLCDecodeDone is enabled. The NFMLCBITPT, NFMLCL0, and NFMLCEL1 have valid values. To clear this, write '1'. 1 = 4-bit ECC decoding is completed	0
IllegalAccess	[5]	Once Soft Lock or Lock-tight is enabled and any illegal access (program, erase) to the memory takes place, then this bit is set. 0 = Illegal access is not detected 1 = Illegal access is detected To clear this value, write 1 to this bit.	0
RnB_TransDetect	[4]	When RnB[0] low to high transition occurs, this bit is set and an interrupt is issued if RnB_TransDetect is enabled. To clear this, write '1'. 0 = RnB transition is not detected 1 = RnB transition is detected Transition configuration is set in RnB_TransMode(NFCONT[8]).	0
Flash_nCE[1] (Read-only)	[3]	The status of nCE[1] output pin	1
Flash_nCE[0] (Read-only)	[2]	The status of nCE[0] output pin	1
Reserved	[1]	Reserved	0
Flash_RnB (Read-only)	[0]	The status of RnB[0] input pin. 0 = NAND Flash memory busy 1 = NAND Flash memory ready to operate	1

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4.5.2.12 ECC0/1 Error Status Register (NFECCERR0, R, Address = 0xB0E0_002C)

- When ECC Type is 1-bit ECC

NFECCERR0	Bit	Description	Initial State
Reserved	[31:25]	Reserved	0x00
ECCSDataAddr	[24:21]	In spare area, Indicates which number data is error	0x0
ECCSBitAddr	[20:18]	In spare area, Indicates which bit is error	000
ECCDataAddr	[17:7]	In main data area, Indicates which number data is error	0x7FF
ECCBitAddr	[6:4]	In main data area, Indicates which bit is error	111
ECCSprErrNo	[3:2]	Indicates whether spare area bit fail error occurred 00 = No Error 01 = 1-bit error(correctable) 10 = Multiple error 11 = ECC area error	00
ECCMainErrNo	[1:0]	Indicates whether main data area bit fail error occurred 00 = No Error 01 = 1-bit error(correctable) 10 = Multiple error 11 = ECC area error	10

NOTE: The above values are valid only when both ECC register and ECC status register have valid value.

- When ECC Type is 4-bit ECC

NFECCERR0	Bit	Description	Initial State
MLCECCBusy	[31]	Indicates the 4-bit ECC decoding engine is searching whether a error exists or not 0 = Idle 1 = Busy	0
MLCECCReady	[30]	ECC Ready bit	1
MLCFreePage	[29]	Indicates the page data read from NAND flash has all ‘FF’ value.	0
MLCECCError	[28:26]	4-bit ECC decoding result 000 = No error 001 = 1-bit error 010 = 2-bit error 011 = 3-bit error 100 = 4-bit error 101 = Uncorrectable 11x = reserved	000
MLCErrLocation2	[25:16]	Error byte location of 2nd bit error	0x000
Reserved	[15:10]	Reserved	0x00
MLCErrLocation1	[9:0]	Error byte location of 1st bit error	0x000

NOTE: These values are updated when ECCDecodeDone (NFSTAT[6]) is set (‘1’).

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4.5.2.13 ECC0/1 Error Status Register (NFECCERR1, R, Address = 0xB0E0_0030)

- When ECC Type is 4-bit ECC

NFECCERR1	Bit	Description	Initial State
Reserved	[31:26]	Reserved	0x00
MLCErrLocation4	[25:16]	Error byte location of 4th bit error	0x00
Reserved	[15:10]	Reserved	0x00
MLCErrLocation3	[9:0]	Error byte location of 3rd bit error	0x000

NOTE: These values are updated when ECCDecodeDone (NFSTAT[6]) is set ('1').

4.5.2.14 Main data area ECC0 status Register (NFMECC0, R, Address = 0xE810_0034)

- When ECCType is 1-bit ECC.

NFMECC0	Bit	Description	Initial State
MECC3	[31:24]	ECC3 for data	0xFF
MECC2	[23:16]	ECC2 for data	0xFF
MECC1	[15:8]	ECC1 for data	0xFF
MECC0	[7:0]	ECC0 for data	0xFF

NOTE: The NAND flash controller generate NFMECC0/1 when read or write main area data while the MainECCLock(NFCONT[7]) bit is '0'(Unlock).

- When ECCType is 4-bit ECC

NFMECC0	Bit	Description	Initial State
4th Parity	[31:24]	4th Check Parity generated from main area (512-byte)	0x00
3rd Parity	[23:16]	3rd Check Parity generated from main area (512-byte)	0x00
2nd Parity	[15:8]	2nd Check Parity generated from main area (512-byte)	0x00
1st Parity	[7:0]	1st Check Parity generated from main area (512-byte)	0x00

NOTE: The NAND flash controller generate these ECC parity codes when write main area data while the MainECCLock (NFCON[7]) bit is '0'(unlock).

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4.5.2.15 Main data area ECC0 status Register (NFMECC1, R, Address = 0xB0E0_0038)

- When ECCType is 4-bit ECC

NFMECC1	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
7th Parity	[23:16]	7th Check Parity generated from main area (512-byte)	0x00
6th Parity	[15:8]	6th Check Parity generated from main area (512-byte)	0x00
5th Parity	[7:0]	5th Check Parity generated from main area (512-byte)	0x00

NOTE: The NAND flash controller generate these ECC parity codes when write main area data while the MainECCLock (NFCON[7]) bit is '0'(unlock).

4.5.2.16 Spare Area ECC Status Register (NFSECC, R, Address = 0xB0E0_003C)

NFSECC	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0xFFFF
SECC1	[15:8]	Spare area ECC1 Status	0xFF
SECC0	[7:0]	Spare area ECC0 Status	0xFF

NOTE: The NAND flash controller generate NFSECC when read or write spare area data while the SpareECCLock(NFCONT[6]) bit is '0'(Unlock).

4.5.2.17 MLC 4-bit ECC Error Patten Register (NFMLCBITPT, R, Address = 0xB0E0_0040)

NFMLCBITPT	Bit	Description	Initial State
4^{th} Error bit pattern	[31:24]	4^{th} Error bit pattern	0x00
3^{rd} Error bit pattern	[23:16]	3^{rd} Error bit pattern	0x00
2^{nd} Error bit pattern	[15:8]	2^{nd} Error bit pattern	0x00
1^{st} Error bit pattern	[7:0]	1^{st} Error bit pattern	0x00

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4.5.3 ECC REGISTERS FOR 8, 12 AND 16-BIT ECC

4.5.3.1 Nand Flash ECC Configuration Register (NFECCCONF, R/W, Address = 0xB0E2_0000)

NFECCCONF	Bit	Description	Initial State
Reserved	[31]	Reserved	0
Reserved	[28]	Reserved	0
MsgLength	[25:16]	The ECC message size. For 512-byte message, you should set 511.	
Reserved	[15:4]	Reserved	0
ECCType	[3:0]	These bits indicate what kind of ECC is used. 000 = Disable 8/ 12/ 16-bit ECC 001 = Reserved 010 = Reserved 011 = 8-bit ECC/512B 100 = 12-bit ECC 101 = 16-bit ECC/512B 110 = Reserved 111 = Reserved	0x0

4.5.3.2 Nand Flash ECC Control Register (NFECCCONT, R/W, Address = 0xB0E2_0020)

NFECCCONT	Bit	Description	Initial State
Reserved	[31:26]	Reserved	0x00
EnbMLCEncInt	[25]	MLC ECC encoding completion interrupt control 0 = Disable interrupt 1 = Enable interrupt	0
EnbMLCDecInt	[24]	MLC ECC decoding completion interrupt control 0 = Disable interrupt 1 = Enable interrupt	0
EccDirection	[16]	MLC ECC encoding / decoding control 0 = Decoding, used for page read 1 = Encoding, used for page program	0
Reserved	[15:3]	Reserved	0x0
InitMECC	[2]	1 = Initialize main area ECC decoder/ encoder (write-only)	0
Reserved	[1]	Reserved	0
ResetECC	[0]	1 = Reset ECC logic. (Write-only)	0

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4.5.3.3 Nand Flash ECC Status Register (NFECCSTAT, R/W, Address = 0xB0E2_0030)

NFECCSTAT	Bit	Description	Initial State
ECCBusy	[31]	Indicates the 8-bit ECC decoding engine is searching whether a error exists or not 0 = Idle 1 = Busy	0
Reserved	[30]	Reserved	1
EncodeDone	[25]	When MLC ECC encoding is finished, this value set and issue interrupt if EncodeDone is enabled. The NFMLCECC0 and NFMLCECC1 have valid values. To clear this, write '1'. 1 = MLC ECC encoding is completed	0
DecodeDone	[24]	When MLC ECC decoding is finished, this value set and issue interrupt if DecodeDone is enabled. The NFMLCBITPT, NFMLCL0 and NFMLCEL1 have valid values. To clear this, write '1'. 1 = MLC ECC decoding is completed	0
Reserved	[23:9]	Reserved	0x0000
FreePageStat	[8]	It indicates whether the sector is free page or not.	0
Reserved	[7:0]	Reserved	0x00

4.5.3.4 Nand Flash ECC Sector Status Register (NFECCSECSTAT, R, Address = 0xB0E2_0040)

NFECCSECSTAT	Bit	Description	Initial State
ValdErrorStat	[31:8]	Each bit indicates which ERL and ERP is valid or not.	0x0000_00
ECCErrorNo	[4:0]	ECC decoding result when page read 00000 = No error 00001 = 1-bit error 00010 = 2-bit error 00011 = 3-bit error .... 01110 = 14-bit error 01111 = 15-bit error 10000 = 16-bit error Note: If 8-bit ECC is used, the valid number of error is until 8. If the number exceeds the supported error number, it means that uncorrectable error occurs.	0x00

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4.5.3.5 Nand Flash ECC Parity code for Page Program Register (NFECCPRGECC*, R, Address = 0xB0E2_0090 ~ 0xB0E2_00A8)

NFECCPRGECC0	Bit	Description	Initial State
4th Parity	[31:24]	4th Check Parity for page program from main area	0x00
3rd Parity	[23:16]	3rd Check Parity for page program from main area	0x00
2nd Parity	[15:8]	2nd Check Parity for page program from main area	0x00
1st Parity	[7:0]	1st Check Parity for page program from main area	0x00
NFECCPRGECC1	**Bit**	**Description**	**Initial State**
8th Parity	[31:24]	8th Check Parity generated from main area	0x00
7th Parity	[23:16]	7th Check Parity generated from main area	0x00
6th Parity	[15:8]	6th Check Parity generated from main area	0x00
5th Parity	[7:0]	5th Check Parity generated from main area	0x00
NFECCPRGECC2	**Bit**	**Description**	**Initial State**
12th Parity	[31:24]	12th Check Parity generated from main area	0x00
11th Parity	[23:16]	11th Check Parity generated from main area	0x00
10th Parity	[15:8]	10th Check Parity generated from main area	0x00
9th Parity	[7:0]	9th Check Parity generated from main area	0x00
NFECCPRGECC3	**Bit**	**Description**	**Initial State**
16th Parity	[31:24]	16th Check Parity generated from main area	0x00
15th Parity	[23:16]	15th Check Parity generated from main area	0x00
14th Parity	[15:8]	14th Check Parity generated from main area	0x00
13th Parity	[7:0]	13th Check Parity generated from main area	0x00
NFECCPRGECC4	**Bit**	**Description**	**Initial State**
20th Parity	[31:24]	20th Check Parity generated from main area	0x00
19th Parity	[23:16]	19th Check Parity generated from main area	0x00
18th Parity	[15:8]	18th Check Parity generated from main area	0x00
17th Parity	[7:0]	17th Check Parity generated from main area	0x00
NFECCPRGECC5	**Bit**	**Description**	**Initial State**
24th Parity	[31:24]	24th Check Parity generated from main area	0x00
23rd Parity	[23:16]	23rd Check Parity generated from main area	0x00
22th Parity	[15:8]	22th Check Parity generated from main area	0x00
21th Parity	[7:0]	21th Check Parity generated from main area	0x00
NFECCPRGECC6	**Bit**	**Description**	**Initial State**
Reserved	[31:16]	Reserved	-
26th Parity	[15:8]	26th Check Parity generated from main area	0x00
25th Parity	[7:0]	25th Check Parity generated from main area	0x00

NOTE: The NAND flash controller generate these ECC parity codes when write main area data while the MainECCLock (NFCON[7]) bit is '0'(unlock).

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4.5.3.6 MLC ECC Error Byte Location Status Register (NFECCERL0~7, R, Address = 0xB0E2_00C0 ~ 0xB0E2_00DC)

NFECCERL0	Bit	Description	Initial State
Reserved	[31:26]	Reserved	0x0
ErrByteLoc2	[25:16]	Error byte location of 2nd bit error	0x000
Reserved	[15:10]	Reserved	0x0
ErrByteLoc1	[9:0]	Error byte location of 1st bit error	0x000
NFECCERL1	**Bit**	**Description**	**Initial State**
Reserved	[31:26]	Reserved	0x0
ErrByteLoc4	[25:16]	Error byte location of 4th bit error	0x000
Reserved	[15:10]	Reserved	0x0
ErrByteLoc3	[9:0]	Error byte location of 3rd bit error	0x000
NFECCERL2	**Bit**	**Description**	**Initial State**
Reserved	[31:26]	Reserved	0x0
ErrByteLoc6	[25:16]	Error byte location of 6th bit error	0x000
Reserved	[15:10]	Reserved	0x0
ErrByteLoc5	[9:0]	Error byte location of 5th bit error	0x000
NFECCERL3	**Bit**	**Description**	**Initial State**
Reserved	[31:26]	Reserved	0x0
ErrByteLoc8	[25:16]	Error byte location of 8th bit error	0x000
Reserved	[15:10]	Reserved	0x0
ErrByteLoc7	[9:0]	Error byte location of 7th bit error	0x000
NFECCERL4	**Bit**	**Description**	**Initial State**
Reserved	[31:26]	Reserved	0x0
ErrByteLoc10	[25:16]	Error byte location of 10th bit error	0x000
Reserved	[15:10]	Reserved	0x0
ErrByteLoc9	[9:0]	Error byte location of 9th bit error	0x000
NFECCERL5	**Bit**	**Description**	**Initial State**
Reserved	[31:26]	Reserved	0x0
ErrByteLoc12	[25:16]	Error byte location of 12th bit error	0x000
Reserved	[15:10]	Reserved	0x0
ErrByteLoc11	[9:0]	Error byte location of 11th bit error	0x000
NFECCERL6	**Bit**	**Description**	**Initial State**
Reserved	[31:26]	Reserved	0x0
ErrByteLoc14	[25:16]	Error byte location of 14th bit error	0x000
Reserved	[15:10]	Reserved	0x0
ErrByteLoc13	[9:0]	Error byte location of 13th bit error	0x000
NFECCERL7	**Bit**	**Description**	**Initial State**

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Reserved	[31:26]	Reserved	0x0
ErrByteLoc16	[25:16]	Error byte location of 16th bit error	0x000
Reserved	[15:10]	Reserved	0x0
ErrByteLoc15	[9:0]	Error byte location of 15th bit error	0x000

NOTE: These values are updated when DecodeDone (NFECCSTAT[24]) is set ('1').

4.5.3.7 MLC ECC Error Patten Register (NFECCERP0~3, R, Address = 0xB0E2_00F0 ~ 0xB0E2_00FC)

NFECCERP0	Bit	Description	Initial State
4th ErrBitPattern	[31:24]	4th Error bit pattern	0x00
3rd ErrBitPattern	[23:16]	3rd Error bit pattern	0x00
2nd ErrBitPattern	[15:8]	2nd Error bit pattern	0x00
1st ErrBitPattern	[7:0]	1st Error bit pattern	0x00
NFECCERP1	**Bit**	**Description**	**Initial State**
8th ErrBitPattern	[31:24]	8th Error bit pattern	0x00
7th ErrBitPattern	[23:16]	7th Error bit pattern	0x00
6th ErrBitPattern	[15:8]	6th Error bit pattern	0x00
5th ErrBitPattern	[7:0]	5th Error bit pattern	0x00
NFECCERP2	**Bit**	**Description**	**Initial State**
12th ErrBitPattern	[31:24]	12th Error bit pattern	0x00
11th ErrBitPattern	[23:16]	11th Error bit pattern	0x00
10th ErrBitPattern	[15:8]	10th Error bit pattern	0x00
9th ErrBitPattern	[7:0]	9th Error bit pattern	0x00
NFECCERP3	**Bit**	**Description**	**Initial State**
16th ErrBitPattern	[31:24]	16th Error bit pattern	0x00
15th Error bit pattern	[23:16]	15th Error bit pattern	0x00
14th ErrBitPattern	[15:8]	14th Error bit pattern	0x00
13th ErrBitPattern	[7:0]	13th Error bit pattern	0x00

NOTE: These values are updated when DecodeDone (NFECCSTAT[25]) is set ('1').

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4.5.3.8 ECC Parity Conversion Register (NFECCCONECC0~6, R/W, Address = 0xB0E2_0110 ~ 0xB0E2_0128)

NFECCCONECC0	Bit	Description	Initial State
4th Conversion Code	[31:24]	4th ECC Parity conversion code	0x00
3rd Conversion Code	[23:16]	3rd ECC Parity conversion code	0x00
2nd Conversion Code	[15:8]	2nd ECC Parity conversion code	0x00
1st Conversion Code	[7:0]	1st ECC Parity conversion code	0x00
NFECCCONECC1	**Bit**	**Description**	**Initial State**
8th Conversion Code	[31:24]	8th ECC Parity conversion code	0x00
7th Conversion Code	[23:16]	7th ECC Parity conversion code	0x00
6th Conversion Code	[15:8]	6th ECC Parity conversion code	0x00
5th Conversion Code	[7:0]	5th ECC Parity conversion code	0x00
NFECCCONECC2	**Bit**	**Description**	**Initial State**
12th Conversion Code	[31:24]	12th ECC Parity conversion code	0x00
11th Conversion Code	[23:16]	11th ECC Parity conversion code	0x00
10th Conversion Code	[15:8]	10th ECC Parity conversion code	0x00
9th Conversion Code	[7:0]	9th ECC Parity conversion code	0x00
NFECCCONECC3	**Bit**	**Description**	**Initial State**
16th Conversion Code	[31:24]	16th ECC Parity conversion code	0x00
15th Conversion Code	[23:16]	15th ECC Parity conversion code	0x00
14th Conversion Code	[15:8]	14th ECC Parity conversion code	0x00
13th Conversion Code	[7:0]	13th ECC Parity conversion code	0x00
NFECCCONECC4	**Bit**	**Description**	**Initial State**
20th Conversion Code	[31:24]	20th ECC Parity conversion code	0x00
19th Conversion Code	[23:16]	19th ECC Parity conversion code	0x00
18th Conversion Code	[15:8]	18th ECC Parity conversion code	0x00
17th Conversion Code	[7:0]	17th ECC Parity conversion code	0x00
NFECCCONECC5	**Bit**	**Description**	**Initial State**
24th Conversion Code	[31:24]	24th ECC Parity conversion code	0x00
23th Conversion Code	[23:16]	23th ECC Parity conversion code	0x00
22th Conversion Code	[15:8]	22th ECC Parity conversion code	0x00
21th Conversion Code	[7:0]	21th ECC Parity conversion code	0x00
NFECCCONECC6	**Bit**	**Description**	**Initial State**
Reserved	[31:16]	Reserved	0x0000
26th Conversion Code	[15:8]	26th ECC Parity conversion code	0x00
25th Conversion Code	[7:0]	25th ECC Parity conversion code	0x00

For more information about ECC parity conversion codes, refer to the *4.3.11 .*

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5 COMPACT FLASH CONTROLLER

5.1 OVERVIEW OF COMPACT FLASH CONTROLLER

A Compact Flash Controller (CFC) connects seamlessly to the AHB Bus as a Bus slave and AHB Master. The CFC subsystem recognizes AHB Bus transactions that target the compact flash card. The Master Interface initiates compact flash card requests to the CFC block requester interface. The Slave interface responds to the requests initiated. To complete the AHB Bus transaction, the CFC drives the appropriate AHB response onto the AHB Bus.

The CFC can control the Hard Disk and the Compact Flash that can operate in true IDE mode.

5.2 KEY FEATURES OF COMPACT FLASH CONTROLLER

The key features of CFC are as follows:

- Supports all ATA PIO from mode 0 to mode 4.
- Supports Multi-Word DMA (MDMA) from mode 0 to mode 2.
- Supports Ultra DMA (UDMA) from mode 0 to mode 4.
- Connects up to two devices.

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5.3 BLOCK DIAGRAM OF COMPACT FLASH CONTROLLER

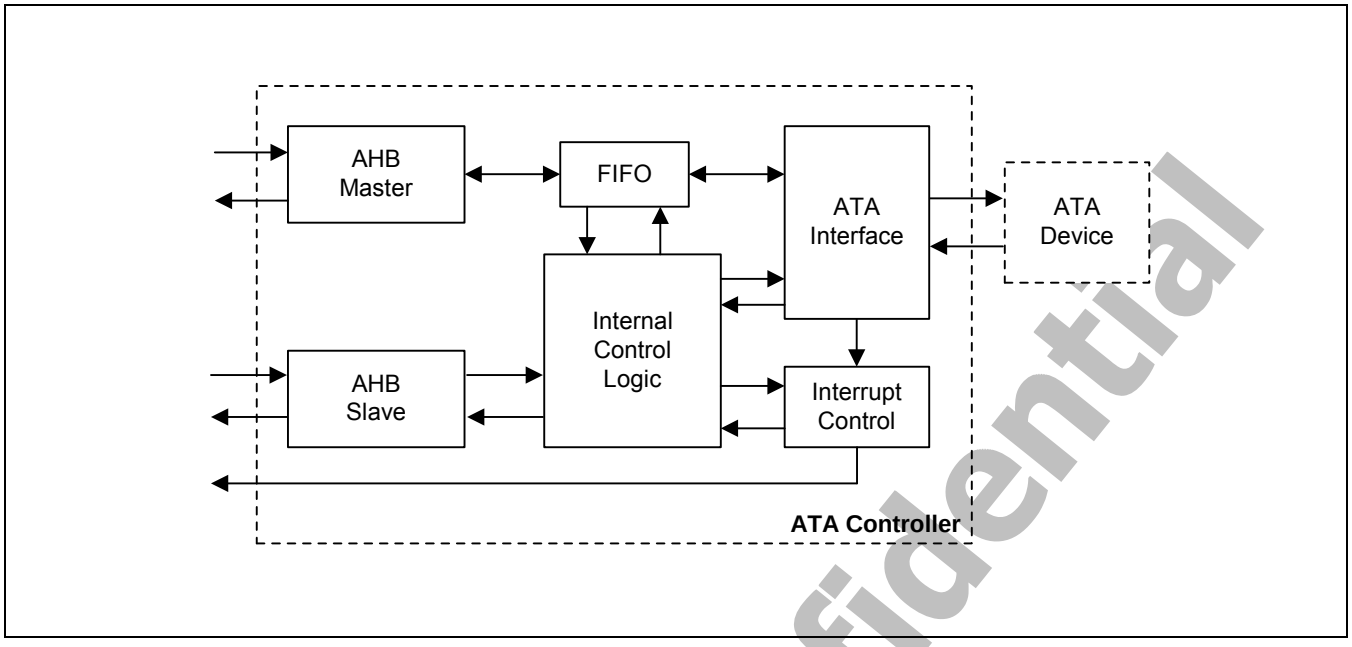

Figure 5-1 Block Diagram of Compact Flash Controller

5.4 FUNCTIONAL DESCRIPTION

The ATAPI controller is compatible with the ATA/ATAPI-5 standard. This mode allows I/O operations to the task file and data registers. It has access to one FIFO that is 16X32-bit. The ATAPI controller has internal DMA controller for data transfer between ATA device and memory. The ATAPI controller has 32 word-sized (32-bits) Special Function Registers.

The ATAPI controller directly accesses the system RAM when it implements MDMA and UDMA data transfer. Therefore, there are three operating modes called PIO, MDMA, and UDMA in the ATA controller. The signal timing depends on the transfer class and its modes. The ATA host controller supports several classes PIO, MDMA, and UDMA. They have various modes according to transfer data rate. The PIO class has five modes. The maximum transfer rate is mode 4. The MDMA has 3 modes, the maximum data rate is 16.7MB/s. The maximum transfer rates supported for the UDMA is mode 4(66MB/s).

This ATAPI controller does not supported the ATA special driver(IO PAD) for UDMA. So user has to use the ATA cable which is shorter than 10cm.

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5.5 TRUE IDE MODE PIO/ PDMA TIMING DIAGRAM

The PIO transfer protocol supports 8-bit register access in driver and 16-bit PIO data access. If PIO mode 3 or 4 is the currently selected mode of operation, both hosts and devices support ATA_IORDY. The *Figure 5-2* defines the relationships between host and device interface signals for data and registers transfer.

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Table 5-1

Table 5-1 describes the timing parameters of PIO modes.

The *Figure 5-2* shows the timing cycle of the true IDE PIO mode, if ATA controller is in the ATA_TRANS state. The figure indicates various timing parameters. Timing ‘t1’ indicates the time between address valid and IORD/IOWR asserted. Timing ‘t2’ indicates the time for which IORD/ IOWR is asserted. The ATA state transfer in PDMA class follows similar timing.

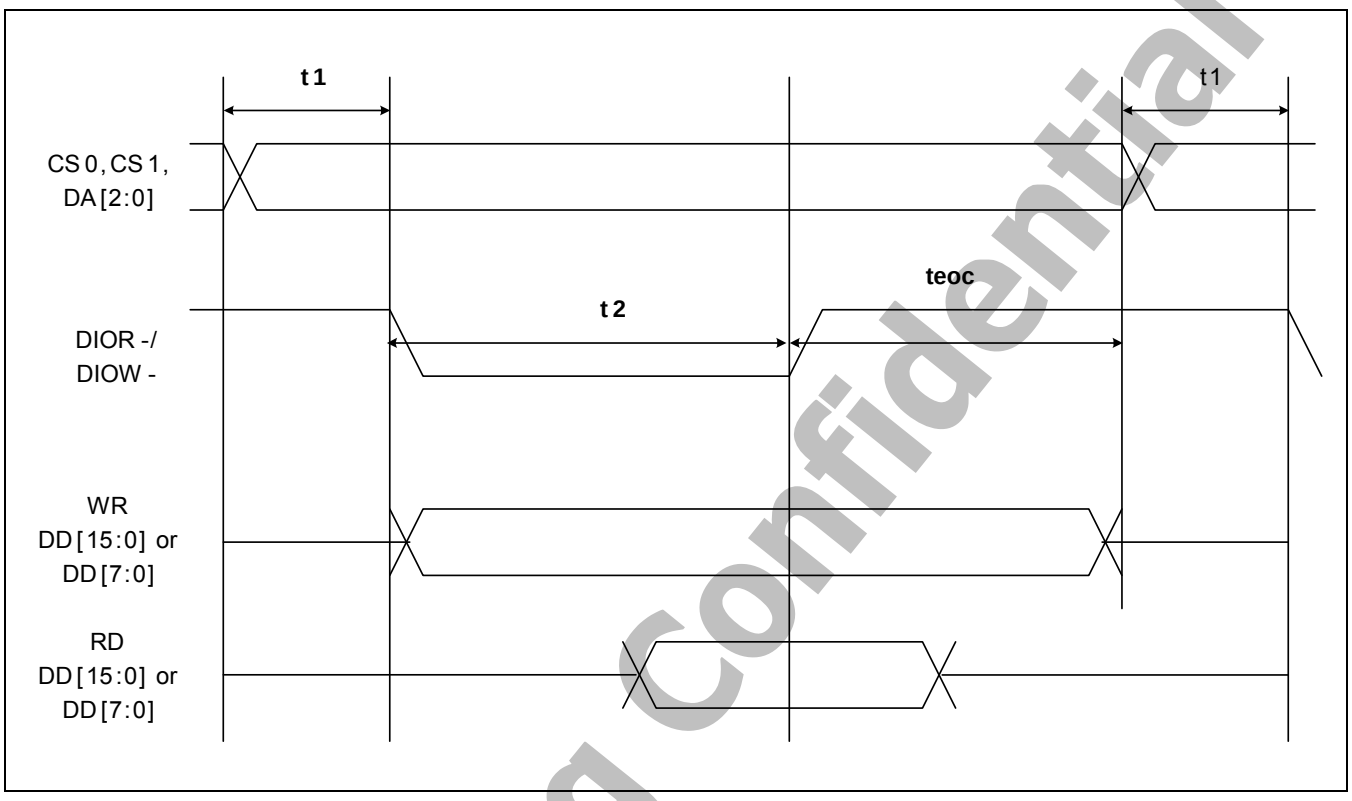

Figure 5-2 PIO Mode Waveform

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Table 5-1 Timing Parameter Each PIO Mode

Register Transfer	MODE0	MODE1	MODE2	MODE3	MODE4
t1	(70, --)	(50, --)	(30, --)	(30, --)	(25, --)
t2	(290, --)	(290, --)	(290, --)	(80, --)	(70, --)
tEOC	(240, --)	(43, --)	(10, --)	(70, --)	(25, --)
t1+t2+tEOC	(600, --)	(383, --)	(330, --)	(180, --)	(120, --)
Data Transfer	**MODE0**	**MODE1**	**MODE2**	**MODE3**	**MODE4**
t1	(70, --)	(50, --)	(30, --)	(30, --)	(25, --)
t2	(165, --)	(125, --)	(100, --)	(80, --)	(70, --)
tEOC	(365, --)	(208, --)	(110, --)	(70, --)	(25, --)
t1+t2+tEOC	(600, --)	(383, --)	(240, --)	(180, --)	(120, --)

NOTE: unit "ns"

5.5.1 ATA_PIO_TIME REGISTER SETTING EXAMPLE (IN CASE OF DATA TRANSFER)

The "t1" minimum time is 70ns in the system clock of 100MHz (10ns). It gives 7; "t1" divided by 10ns. This case has no residual, therefore pio_t1[3:0] assigns 6 which is 7 minus 1. If it has residual, assign the quotient at pio_t1[3:0].

- ATA_PIO_TIME (Tpara) = PIO mode (Minimum, Maximum)/ system clock - 1
- tPIO0 (Timing Parameter of PIO Mode 0 in case of Register Transfer) : 32'h000_17_1c_6
- t1: 70/10 = 7 pio_t1 value = 7- 1 = 6 pio_t1[3:0] : 0x6
- t2: 290/10 = 29 pio_t2 value = 29 - 1 = 28 pio_t2[11 :4] : 0x1c
- teoc: 240/10 = 24 pio_teoc value = 24 - 1 = 23 pio_teoc[19:12] : 0x17

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5.6 FLOWCHART FOR PIO READ / WRITE

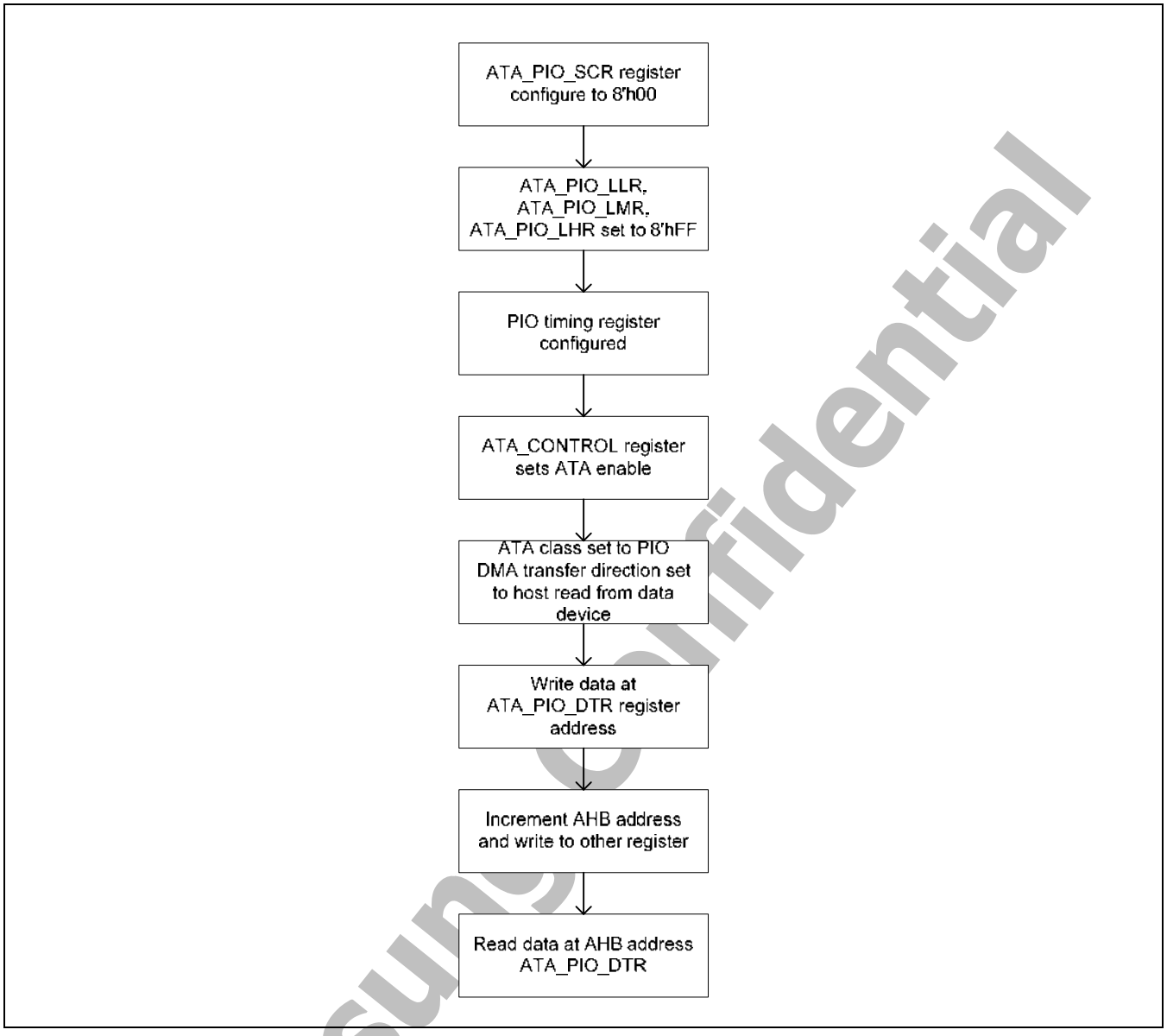

Figure 5-3 Flowchart for Read / Write in PIO Class

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5.7 TRUE IDE MDMA MODE TIMING DIAGRAM

The ATAPI MDMA streams data continuously across the ATA interface between the host and the target device. This transfer class allows either the driver or host to pause or terminate the data flow. To support various transfer speed classes, the CPU programs appropriate timing parameters. The ATA_CS0n and CS1n are inactive during MDMA transfer. The ATA Host controller is always the master in the MDMA transfer classes. The MDMA has three transfer modes (Mode 0 ~ 2). The fastest mode is mode 2.

The *Figure 5-4* defines the relationships between host and device interface signals for data transfer. The *Table 5-2* describes the timing parameters of MDMA read and write transfer.

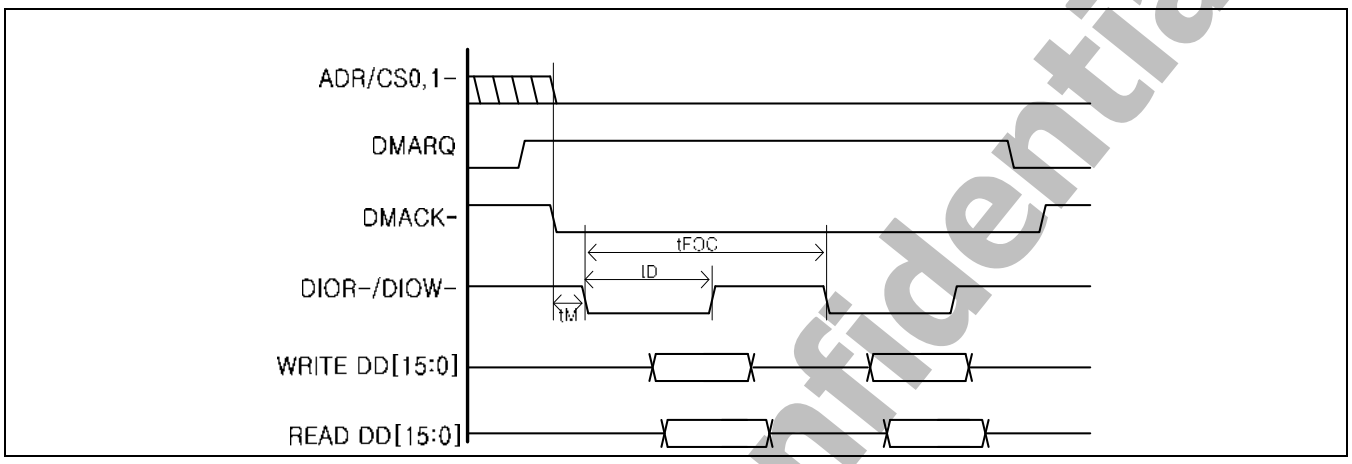

Figure 5-4 MDMA Timing Diagram

Table 5-2 MDMA Timing Parameters

	MODE0	MODE1	MODE2
tm	(50, --)	(30, --)	(25, --)
td	(215, --)	(80, --)	(70, --)
tEOC	(265, --)	(70, --)	(50, --)
td+tEOC	(480, --)	(150, --)	(120, --)

unit: ns

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5.7.1 ATA_MDMA_TIME REGISTER SETTING EXAMPLE

The “td” minimum time is 215ns in the system clock 100MHz (10ns). It gives 21.5; “td” divided by 10ns. This case has residual, assigning quotient (21) to the dma_td[3:0]. If it has no residual, assign the quotient minus 1 at dma_td[3:0].

- tMDMA0 (Timing Parameter of MDMA Mode 0) : 32’h000_1a_15_4
- tm: 50/10 = 5 dma_td value = 5 - 1 = 4 dma_tm[3 :0] : 0x4
- td: 215/10 = 21.5 dma_td value = 21 dma_td[11:4] : 0x15
- teoc: 265/10 = 26.5 dma_teoc value = 26 dma_teoc[19:12] : 0x1a

Steps for ATAPI MDMA transfer protocol (To write and read transfer):

Steps to Write Protocol:

1. Wait for the driver to activate ATA_DMARQ.
2. Activate ATA_DMACKn, deactivate ATA_CS0n/CS1n, and set time to 0.
3. Activate ATA_DIOWn at time tM.
4. Drive 16-bit data on the lines at time tD.
5. Deactivate ATA_DIOWn after tD.
6. If ATA_DMARQ is still active, repeat step 3 to 6 for another word, and deactivate ATA_DMACKn at time tM.

Steps to Read Protocol:

1. Wait for the driver to activate ATA_DMARQ.
2. Activate ATA_DMACKn, deactivate ATA_CS0n/CS1n, and set time to 0.
3. Activate ATA_DIORn at time tM.
4. Deactivate ATA_DIORn and latch 16-bit data lines at time tD.
5. If ATA_DMARQ is still active, repeat step 3 to 5 for another word, and deactivate ATA_DMACKn at time tM.

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5.8 TRUE IDE UDMA MODE TIMING DIAGRAM

The Ultra-DMA (UDMA) is a fast DMA protocol which supports six timing modes (mode 0 ~ 5). Mode 5 is the fastest; it operates at 100MHz. This ATAPI host controller supports upto mode 4. It operates at 66MHz. Both host and device driver perform CRC check during UDMA burst transfer. At the end of the burst, the host sends its CRC result to the device. If the CRC result does not match, the driver reports an error in the error register and asserts the ATA_INTRQ signal.

The following figures (*Figure 5-5*, *Figure 5-6*, Figure 5-7 and Figure 5-8) defines the relationships between host and device interface signals for UDMA data transfer.

The timing parameters involved is tACKENV, tRP, tSS, tDVS, and tDVH.

- tACKENV indicates the setup and hold times of DMACK (Before assertion or negation) and envelope time (From DMACKn to STOP and HDMARDYn).
- tRP indicates Ready-to-pause time.
- tSS indicates time from STROBE edge to negation of DMARQ or assertion of STOP.
- tDVS is time for which data is valid until STROBE edge.
- tDVH is time from STROBE edge until data is invalid.

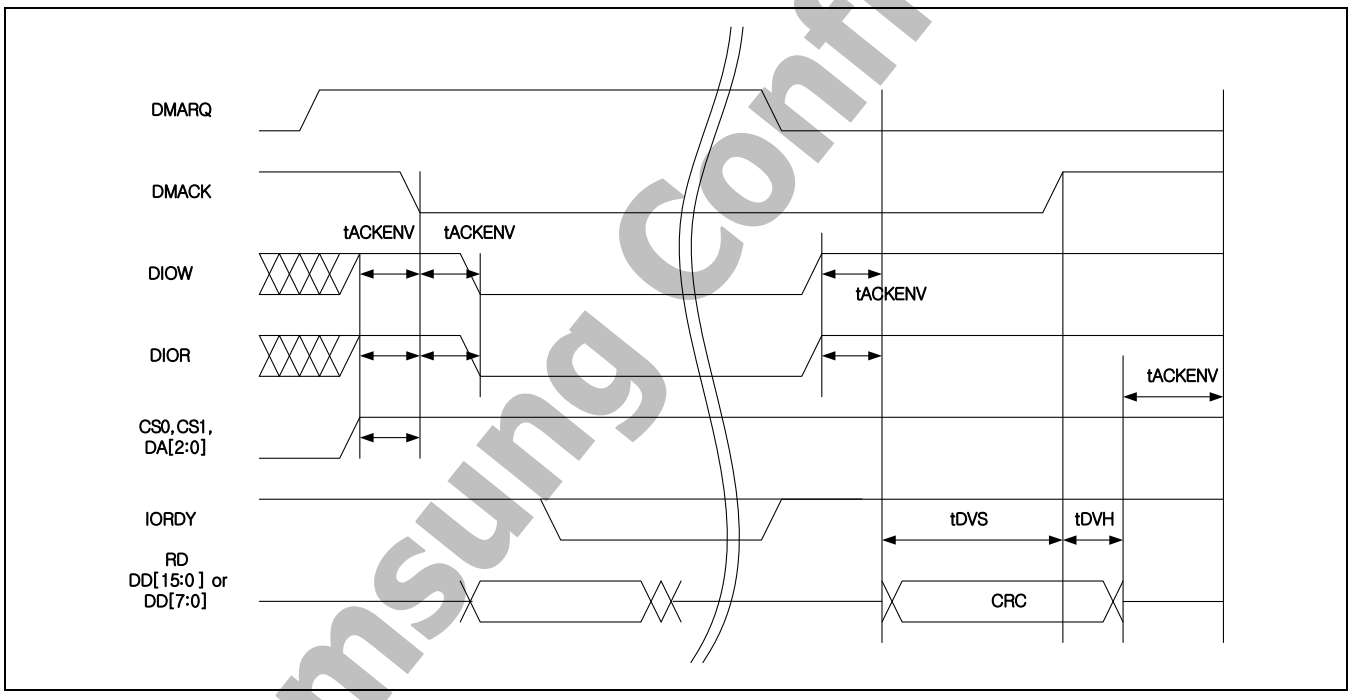

Figure 5-5 UDMA- In Operation (Terminated by Device)

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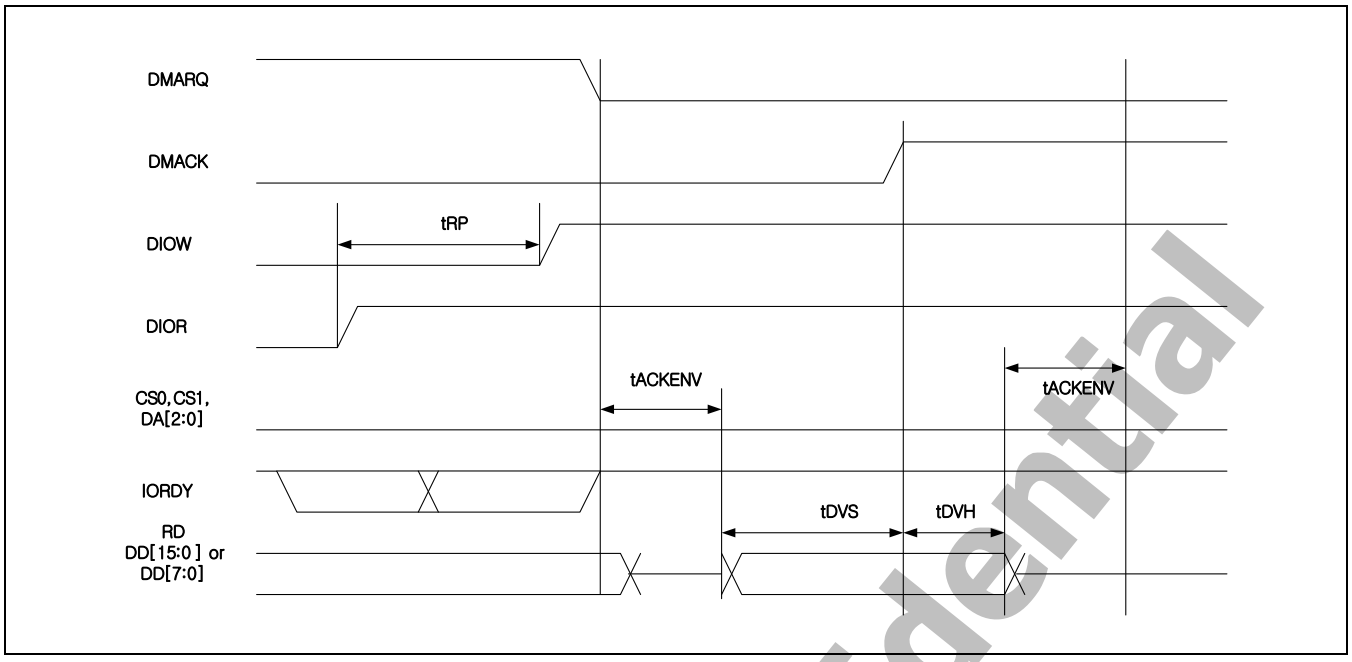

Figure 5-6 UDMA - In Operation (Terminated by Host)

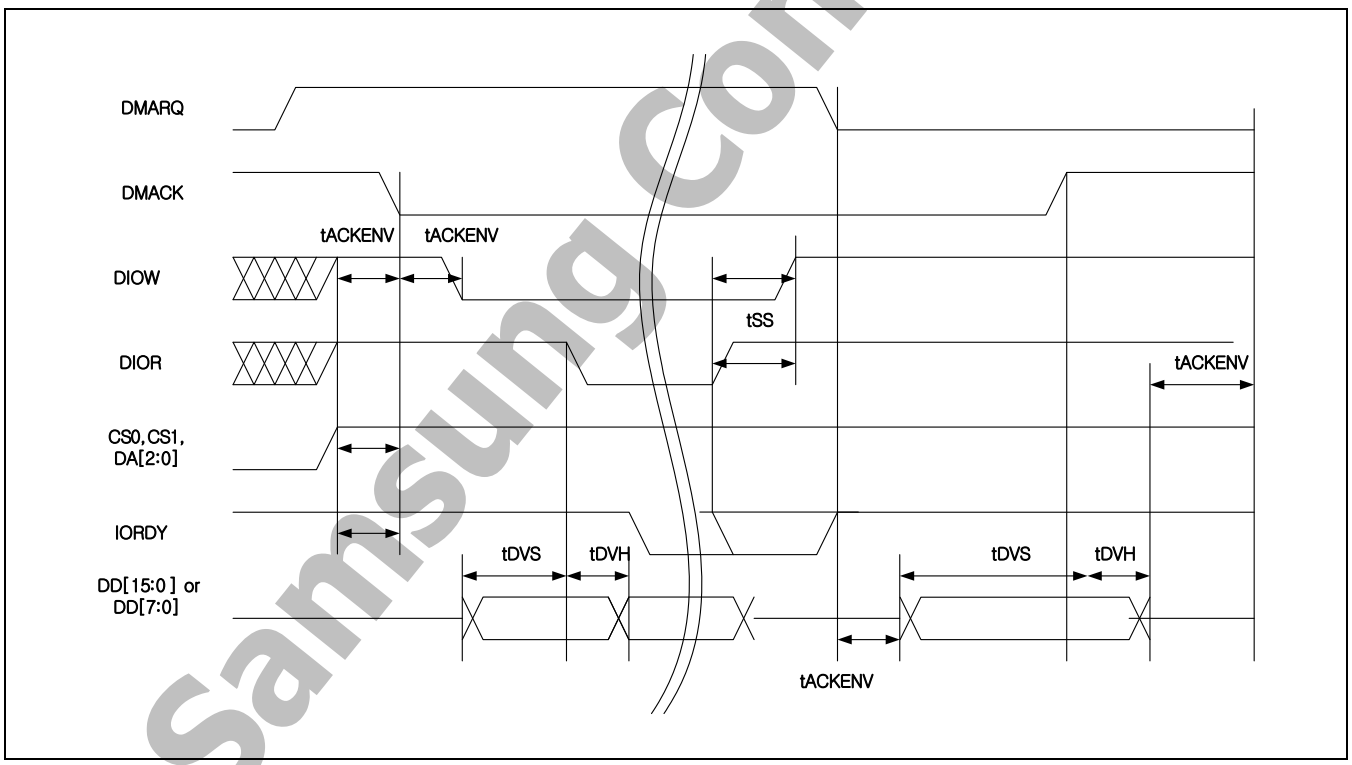

Figure 5-7 UDMA - Out Operation (Terminated by Device)

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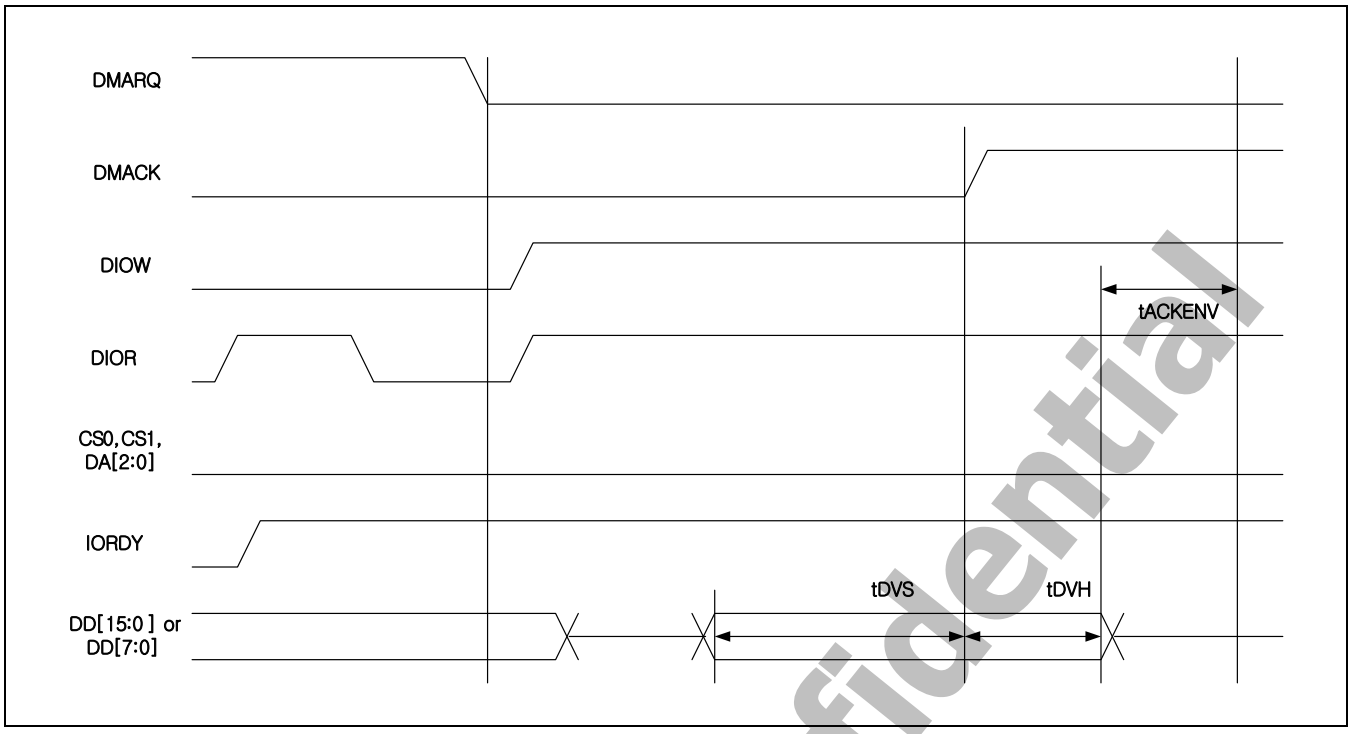

Figure 5-8 UDMA - Out Operation (Terminated by Host)

Table 5-3 Timing Parameter Each UDMA Mode

UDMA mode	UDMA 0	UDMA 1	UDMA 2	UDMA 3	UDMA 4
tACKENV	(20, 70)	(20, 70)	(20, 70)	(20, 55)	(20, 55)
tSS	(50, --)	(50, --)	(50, --)	(50, --)	(50, --)
tRP	(160, --)	(125, --)	(100, --)	(100, --)	(100, --)
tDVS	(70, --)	(48, --)	(31, --)	(20, --)	(6.7, --)
tDVH	(6.2, --) *(50)	(6.2, --) *(32)	(6.2, --) *(29)	(6.2, --) *(25)	(6.2, --) *(23.3)
tDVS+tDVH	(120, --)	(80, --)	(60, --)	(45, --)	(30, --)

NOTE: unit: ns, *(50) is “(tDVS+tDVH)” – “tDVS” = 120 – 70 = 50

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5.8.1 ATA_UDMA_TIME REGISTER SETTING EXAMPLE

The “tackenv” minimum time is 20ns in the system clock of 100MHz (10ns). It gives 2; “tackenv” divided by 10ns. This case has no residual, therefore the udma_tackenv[3:0] assigns 1 which is 2 minus 1. If it has residual, assign the quotient at udma_tackenv[3:0].

ATA_UDMA_TIME (Tpara) = UDMA mode(min, max) / system clock – 1

tUDMA0(Timing Parameter of UDMA Mode 0) : 32’h04_06_0f_4_1

tackenv: 20/10 = 2	udma_tackenv value = 2 - 1 = 1	udma_tackenv[3 :0]	: 0x1
tss: 50/10 = 5	udma_tss value = 5 - 1 = 4	udma_tss[7:4]	: 0x4
trp: 160/10 = 16	udma_trp value = 16 -1 = 15	udma_trp[15:8]	: 0x0f
tdvs: 70/10 = 7	udma_tdvs value = 7 - 1 =6	udma_tdvs[23:16]	: 0x06
tdvh: 50/10 = 5	udma_tdvh value = 5 - 1 = 4	udma_tdvh[27:24]	: 0x4

(tdvh minimum timing is 6.2ns, but the timing parameter sets 50ns since the tDVS and tDVH summation is 120ns)

The *Table 5-4* shows True-IDE Mode Control Signaling:

Table 5-4 True-IDE Mode I/O Decoding

nCE2	nCE1	A2	A1	A0	nDMACK	nIORD=0	nIOWR=0	Note
1	0	0	0	0	1	PIO RD data	PIO WR data	8 or 16 bit
1	1	X	X	X	0	DMA RD data	DMA WR data	16bit
1	0	0	0	1	1	Error Register	Feature	8 bit
1	0	0	1	0	1	Sector Count	Sector Count	8 bit
1	0	0	1	1	1	Sector No.	Sector No.	8 bit
1	0	1	0	0	1	Cylinder Low	Cylinder Low	8 bit
1	0	1	0	1	1	Cylinder High	Cylinder High	8 bit
1	0	1	1	0	1	Select Card/Head	Select Card/Head	8 bit
1	0	1	1	1	1	Status	Command	8 bit
0	1	1	1	0	1	Alt Status	Device Control	8 bit

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5.9 TRANSFER STATE ABORT

The PIO, PDMA, MDMA or UDMA checks for abort or stop transfer state after completing one full cycle of the finite state machine (FSM). The FSM transition from IDLE state happens if ATA transfer state is in ATA_TRANS. The FSM continues the cycle while the abort is asserted. The transfer in any class stays in IDLE after detecting ATA state in ATA_ABORT.

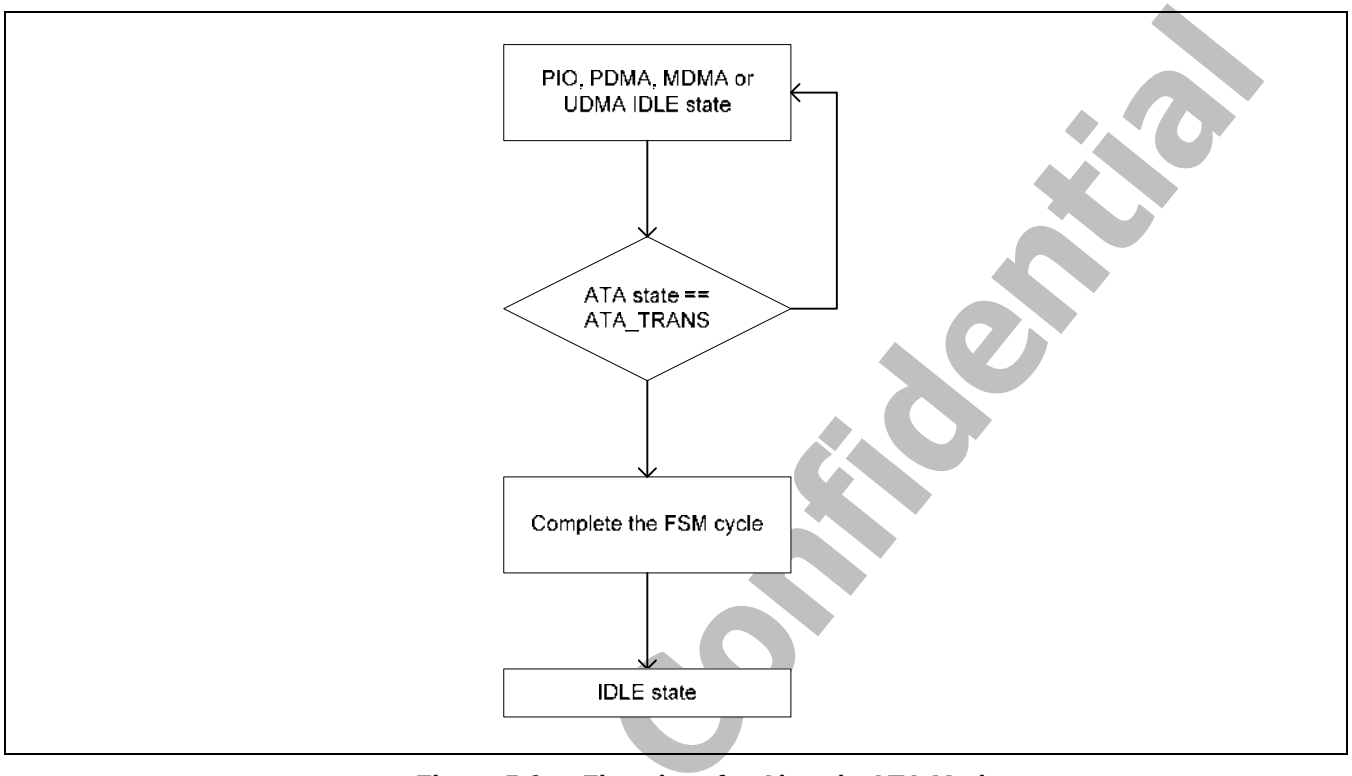

Figure 5-9 Flowchart for Abort in ATA Mode

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5.10 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
CSn0	O	Device chip selection signal To select the control block registers	XmsmCSn	muxed
CSn1	O	Device chip selection signal To select the command block registers	XmsmWEn	muxed
DA[2:0]	O	register address signals	XmsmADDR[2:0]	muxed
DD_RD[15:0]	I	Read Data Bus	XmsmDATA[15:0]	muxed
DD_WR[15:0]	O	Write Data Bus	XmsmDATA[15:0]	muxed
DD_wr_en	O	Data Output Enable Strobe		
IORDY	I	Data transfer wait signal. DMA ready during UDMA write. DMA strobe during UDMA read.	XmsmADDR[3]	muxed
INTRQ	I	Device Interrupt signal.	XmsmADDR[4]	muxed
DMARQ	I	The DMA request signal for data transfers between host and device.	XmsmADDR[5]	muxed
DRESETn	O	Device reset signal from host.	XmsmADDR[6]	muxed
DMACKn	O	The DMA acknowledge signal that data has been accepted or data is available.	XmsmADDR[7]	muxed
DIORn (HDMA_RDYn, HSTROBE)	O	IO Read Enable Strobe. DMA ready during UDMA read. Data strobe during UDMA write	XmsmRn	muxed
DIOWn	O	IO Write Enable Strobe Stop during UDMA read.	XmsmIRQn	muxed

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5.11 REGISTER DESCRIPTION

5.11.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
ATA_CONTROL	0xE820_0000	R/W	Specifies the ATA enable and clock down status	0x00000002
ATA_STATUS	0xE820_0004	R	Specifies the ATA status	0x00000008
ATA_COMMAND	0xE820_0008	R/W	Specifies the ATA command	0x00000000
ATA_SWRST	0xE820_000C	R/W	Specifies the ATA software reset	0x00000000
ATA_IRQ	0xE820_0010	R/W	Specifies the ATA interrupt sources	0x00000000
ATA_IRQ_MASK	0xE820_0014	R/W	Specifies the ATA interrupt mask	0x00000000
ATA_CFG	0xE820_0018	R/W	Specifies the ATA configuration for ATA interface	0x80000000
Reserved	0xE820_001C	R/W	Reserved	-
Reserved	0xE820_0020	R/W	Reserved	-
Reserved	0xE820_0024	R/W	Reserved	-
ATA_MDMA_TIME	0xE820_0028	R/W	Specifies the ATA multi-word DMA timing	0x0002c238
ATA_PIO_TIME	0xE820_002C	R/W	Specifies the ATA PIO timing	0x000272fa
ATA_UDMA_TIME	0xE820_0030	R/W	Specifies the ATA UDMA timing	0x080b1a83
ATA_XFR_NUM	0xE820_0034	R/W	Specifies the ATA transfer number	0x00000000
ATA_XFR_CNT	0xE820_0038	R	Specifies the ATA current transfer count	0x00000000
ATA_TBUF_BASE	0xE820_003C	R/W	Specifies the ATA start address of track buffer	0x00000000
ATA_TBUF_SIZE	0xE820_0040	R/W	Specifies the ATA size of track buffer	0x00000000
ATA_SBUF_BASE	0xE820_0044	R/W	Specifies the ATA start address of source buffer	0x00000000
ATA_SBUF_SIZE	0xE820_0048	R/W	Specifies the ATA size of source buffer	0x00000000
ATA_CADR_TBUF	0xE820_004C	R	Specifies the ATA current write address of track buffer	0x00000000
ATA_CADR_SBUF	0xE820_0050	R	Specifies the ATA current read address of source buffer	0x00000000
ATA_PIO_DTR	0xE820_0054	R/W	Specifies the ATA PIO device data register	0x00000000
ATA_PIO_FED	0xE820_0058	R/W	Specifies the ATA PIO device Feature/ Error register	0x00000000
ATA_PIO_SCR	0xE820_005C	R/W	Specifies the ATA PIO sector count register	0x00000000
ATA_PIO_LLR	0xE820_0060	R/W	Specifies the ATA PIO device LBA low register	0x00000000
ATA_PIO_LMR	0xE820_0064	R/W	Specifies the ATA PIO device LBA middle register	0x00000000

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Register	Address	R/W	Description	Reset Value
ATA_PIO_LHR	0xE820_0068	R/W	Specifies the ATA PIO device LBA high register	0x00000000
ATA_PIO_DVR	0xE820_006C	R/W	Specifies the ATA PIO device register	0x00000000
ATA_PIO_CSD	0xE820_0070	R/W	Specifies the ATA PIO device command/ status register	0x00000000
ATA_PIO_DAD	0xE820_0074	R/W	Specifies the ATA PIO device control/ alternate status register	0x00000000
ATA_PIO_READY	0xE820_0078	R	Specifies the ATA PIO data read/ write ready	0x00000003
ATA_PIO_RDATA	0xE820_007C	R	Specifies the ATA PIO read data from device data register	0x00000000
BUS_FIFO_STATUS	0xE820_0080	R	Specifies the ATA internal AHB FIFO status	0x00000000
ATA_FIFO_STATUS	0xE820_0084	R	Specifies the ATA internal ATA FIFO status	0x00000000

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5.11.1.1 ATA Control Register (ATA_CONTROL, R/W, Address = 0xE820_0000)

ATA_CONTROL	Bit	Description	R/W	Initial State
Reserved	[31:2]	Reserved	R	0x0
clk_down_ready	[1]	Status for clock down This bit is asserted in idle state if ATA_CONTROL bit [0] is zero. 0 = Not ready for clock down 1 = Ready for clock down	R	0x1
ata_enable	[0]	Enables ATA 0 = Disables ATA and preparation for clock down. 1 = Enables ATA.	R/W	0x0

5.11.1.2 ATA Status Register (ATA_STATUS, R, Address = 0xE820_0004)

ATA_STATUS	Bit	Description	R/W	Initial State
Reserved	[31:6]	Reserved	R	0x0
atadev_cblid	[5]	ATAPI cable identification	R	0x0
atadev_irq	[4]	ATAPI interrupt signal line	R	0x0
atadev_iordy	[3]	ATAPI iordy signal line	R	0x1
atadev_dmareq	[2]	ATAPI dmareq signal line	R	0x0
xfr_state	[1:0]	Transfer state 2'b00 = Idle state 2'b01 = Transfer state 2'b10 = Abort state 2'b11 = Wait for completion state	R	0x0

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5.11.2 ATA COMMAND REGISTER (ATA_COMMAND, R/W, ADDRESS = 0XE820_0008)

ATA_COMMAND	Bit	Description	R/W	Initial State
Reserved	[31:2]	Reserved	R	0x0
xfr_command	[1:0]	ATA transfer command Four command types (START, STOP, ABORT and CONTINUE) are supported for data transfer control. The “START” command starts data transfer. The “STOP” command pause transfer temporarily. The “CONTINUE” command is used after “STOP” command or internal state of “pause” if track buffer is full or UDMA hold state. The “ABORT” command terminates current data transfer sequences and make ATA host controller move to idle state. 00 = Stop command 01 = Start command (Available in idle state) 10 = Abort command 11 = Continue command (Available in transfer pause) ** After CPU ABORT commands, make a software reset by ATA_SWRST to clear the leftover values of internal registers.	R/W	0x0

The STOP command controls the ATA Device side signal but does not control DMA side. Namely, if the FIFO has data after STOP command, DMA operation progresses until the FIFO becomes empty at read operation. In case of write operation, the DMA acts similarly until the FIFO becomes full.

Use the ABORT command if the transmitting data has proven useless data or discontinues absurd state by error interrupt from device. At that time, it clears all data in ATA Host controller (register, FIFO) and the transmission state machine goes to IDLE.

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5.11.2.1 ATA Software Reset (ATA_SWRST, R/W, Address = 0xE820_000C)

ATA_SWRST	Bit	Description	R/W	Initial State
Reserved	[31:1]	Reserved	R	0x0
ata_swrst	[0]	Software reset for the ATAPI host 0 = No reset 1 = Resets device registers and all registers of ATAPI host controller except CPU interface registers. After software reset, to continue transfer, user must configure all registers of host controller and device registers.	R/W	0x0

5.11.2.2 ATA Interrupt Register (ATA_IRQ, R/W, Address = 0xE820_0010)

ATA_IRQ	Bit	Description	R/W	Initial State
Reserved	[31:6]	Reserved	R	0x0
mdma_hold_int	[5]	If ATAPI device makes pending in MDMA class. CPU clears this interrupt by writing “1”.	R/W	0x0
sbuf_empty_int	[4]	If source buffer is empty. CPU clears this interrupt by writing “1”.	R/W	0x0
tbuf_full_int	[3]	If track buffer is half-full. CPU clears this interrupt by writing “1”.	R/W	0x0
atadev_irq_int	[2]	If ATAPI device generates interrupt. CPU clears this interrupt by writing “1”.	R/W	0x0
udma_hold_int	[1]	If ATAPI device makes early termination in UDMA class. CPU clears this interrupt by writing “1”.	R/W	0x0
xfr_done_int	[0]	If all data transfers are complete. CPU clears this interrupt by writing “1”.	R/W	0x0

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5.11.2.3 ATA Interrupt Mask Register (ATA_IRQ_MASK, R/W, Address = 0xE820_0014)

ATA_IRQ_MASK	Bit	Description	R/W	Initial State
Reserved	[31:6]	Reserved	R	0x0
mask_mdma_hold_int	[5]	0 = Mask mdma_hold_int; Disable 1 = Unmask mdma_hold_int; Enable	R/W	0x0
mask_sbut_empty_int	[4]	0 = Mask sbut_empty_int; Disable 1 = Unmask sbuf_empty_int; Enable	R/W	0x0
mask_tbuf_full_int	[3]	0 = Mask tbuf_full_int; Disable 1 = Unmask tbuf_full_int; Enable	R/W	0x0
mask_atadev_irq_int	[2]	0 = Mask atadev_irq_int; Disable 1 = Unmask ata_irq_int; Enable	R/W	0x0
mask_udma_hold_int	[1]	0 = Mask udma_hold_int; Disable 1 = Unmask udma_hold_int; Enable	R/W	0x0
mask_xfr_done_int	[0]	0 = Mask xfr_done_int; Disable 1 = Unmask xfr_done_int; Enable	R/W	0x0

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5.11.2.4 ATA Configuration Register (ATA_CFG, R/W, Address = 0xE820_0018)

ATA_CFG	Bit	Description	R/W	Initial State
Reserved	[31]	Reserved (This field should be 0x1)	R/W	0x1
Reserved	[30:13]	Reserved	R	0x0
dma_mode	[12]	Determines whether DMA is normal DMA 0 = Normal DMA mode 1 = Reserved.	R/W	0x0
Reserved	[11]	Reserved	R	
word_swap	[10]	Determines whether endian is little or big in AHB word data. (half word swapping) 0 = Little endian {byte3, byte2, byte1, byte0} 1 = Big endian {byte1, byte0, byte3, byte2}	R/W	0x0
udma_auto_mode	[9]	Determines whether to continue automatically in case of early termination in UDMA mode by Device. This bit shoud not be changed during runtime operation. 0 = Stay in pause state and wait for CPU's action. 1 = Continue automatically	R/W	0x0
Reserved	[8]	Reserved	R	0x0
Reserved	[7]	Reserved	R	0x0
byte_swap	[6]	Determines whether data endian is little or big in 16-bit data. 0 = Little endian (data[15:8], data[7:0]) 1 = Big endian (data[7:0], data[15:8]) In case of PIO mode; 0 = Big endian 1 = Little endian.	R/W	0x0
atadev_irq_al	[5]	Device interrupt signal level 0 = Active high 1 = Active low	R/W	0x0
dma_dir	[4]	DMA transfer direction 0 = Host read data from device 1 = Host write data to device	R/W	0x0
ata_class	[3:2]	Selects ATA transfer class 2'b00 = Transfer class is PIO 2'b01 = Transfer class is PIO DMA 2'b10 = Transfer class is Multi-word DMA 2'b11 = Transfer class is UDMA	R/W	0x0
ata_iordy_en	[1]	Determines whether IORDY input extends data transfer. 0 = Disables IORDY (ignored) 1 = Enables IORDY (can extend)	R/W	0x0
ata_rst	[0]	ATAPI device reset by this host. 0 = No reset 1 = Reset	R/W	0x0

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5.11.2.5 ATA Multi_word DMA Timing (ATA_MDMA_TIME, R/W, Address = 0xE820_0028)

ATA_MDMA_TIME	Bit	Description	R/W	Initial State
Reserved	[31:20]	Reserved	R	0x0
dma_teoc	[19:12]	DMA timing parameter, Teoc, end of cycle time	R/W	0x2C
dma_t2	[11:4]	DMA timing parameter, tD, DIOR/DIOWn pulse width	R/W	0x23
dma_t1	[3:0]	DMA timing parameter, tM, CS0,1n valid to DIOR/Wn	R/W	0x8

5.11.2.6 ATA PIO Time (ATA_PIO_TIME, R/W, Address = 0xE820_002C)

ATA_PIO_TIME	Bit	Description	R/W	Initial State
Reserved	[31:20]	Reserved	R	0x0
pio_teoc	[19:12]	PIO timing parameter, teoc, end of cycle time It shall not have zero value.	R/W	0x27
pio_t2	[11:4]	PIO timing parameter, t2, DIOR/Wn pulse width It cannot have zero value.	R/W	0x2f
pio_t1	[3:0]	PIO timing parameter, t1, address valid to DIOR/Wn	R/W	0xa

5.11.2.7 ATA UDMA Time (ATA_UDMA_TIME, R/W, Address = 0xE820_0030)

ATA_UDMA_TIME	Bit	Description	R/W	Initial State
Reserved	[31:28]	Reserved	R	0x0
udma_tdvh	[27:24]	UDMA timing parameter tDVH	R/W	0x8
udma_tdvs	[23:16]	UDMA timing parameter tDVS It cannot have zero value.	R/W	0x0b
udma_trp	[15:8]	UDMA timing parameter tRP	R/W	0x1a
udma_tss	[7:4]	UDMA timing parameter, tSS	R/W	0x8
udma_tackenv	[3:0]	UDMA timing parameter tENV (envelope time (From DMACKn to STOP and HDMARDYn), tACK (setup and hold time for DMACKn)	R/W	0x3

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5.11.2.8 ATA Transfer Count Number (ATA_XFR_NUM, R/W, Address = 0xE820_0034)

ATA_XFR_NUM	Bit	Description	R/W	Initial State
xfr_num	[31:1]	Data transfer number. To transfer 1-sector (512-byte), you should set 32'h1ff.	R/W	0x00000000
Reserved	[0]	Reserved	R	0x0

5.11.2.9 ATA Current Transfer Count (ATA_XFR_CNT, R, Address = 0xE820_0038)

ATA_XFR_CNT	Bit	Description	R/W	Initial State
xfr_cnt	[31:1]	Current remaining transfer counter. This value counts down from ATA_XFR_NUM. It goes to zero if all pre-defined data are transferred. In case of read transfer, ATA_XFR_NUM decreases by 1(2-byte). In case of write transfer, ATA_XFR_NUM decreases by 16(32-byte), because the AHB burst size is 8.	R	0x00000000
Reserved	[0]	Reserved	R	0x0

5.11.2.10 Start Address of the Track Buffer (ATA_TBUF_BASE, R/W, Address = 0xE820_003C)

ATA_TBUF_BASE	Bit	Description	R/W	Initial State
track_buffer_base	[31:2]	Start address of track buffer (4 byte unit)	R/W	0x00000000
Reserved	[1:0]	Reserved	R	0x0

5.11.2.11 Size of the Track Buffer (ATA_TBUF_SIZE, R/W, Address = 0xE820_0040)

ATA_TBUF_SIZE	Bit	Description	R/W	Initial State
track_buffer_size	[31:5]	Size of track buffer (32 byte unit) This should be set to "size_of_data_in_bytes – 1". For example, to transfer 1-sector (512-byte, 32'h200), you should set 32'h1FF (= 32'h200 – 1).	R/W	0x0000000
Reserved	[4:0]	Reserved	R	0x00

5.11.2.12 Start Address of the Source Buffer (ATA_SBUF_BASE, R/W, Address = 0xE820_0044)

ATA_SBUF_BASE	Bit	Description	R/W	Initial State
src_buffer_base	[31:2]	Start address of source buffer (4byte unit)	R/W	0x00000000
Reserved	[1:0]	Reserved	R	0x0

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5.11.2.13 Size of Source Buffer (ATA_SBUF_SIZE, R/W, Address = 0xE820_0048)

ATA_SBUF_SIZE	Bit	Description	R/W	Initial State
src_buffer_size	[31:5]	Size of source buffer (32byte unit) This should be set to “size_of_data_in_bytes – 1”. For example, to transfer 1-sector (512-byte, 32’h200), you should set 32’h1FF (= 32’h200 – 1).	R/W	0x0000000
Reserved	[4:0]	Reserved	R	0x00

5.11.2.14 Current Address of Track Buffer (ATA_CADDR_TBUF, R, Address = 0xE820_004C)

ATA_CADDR_TBUF	Bit	Description	R/W	Initial State
track_buf_cur_adr	[31:2]	Current address of track buffer	R	0x00000000
Reserved	[1:0]	Reserve	R	0x0

5.11.2.15 Current Address of Source Buffer (ATA_CADDR_SBUF, R, Address = 0xE820_0050)

ATA_CADDR_SBUF	Bit	Description	R/W	Initial State
source_buf_cur_adr	[31:2]	Current address of source buffer	R	0x00000000
Reserved	[1:0]	Reserved	R	0x0

5.11.2.16 ATA PIO Data Register (ATA_PIO_DTR, R/W, Address = 0xE820_0054)

ATA_PIO_DTR	Bit	Description	R/W	Initial State
Reserved	[31:16]	Reserved	R	0x0
pio_dev_dtr	[15:0]	16-bit PIO data register	R/W	0x0000

5.11.2.17 ATA PIO Device Feature/Error Register (ATA_PIO_FED, R/W, Address = 0xE820_0058)

ATA_PIO_FED	Bit	Description	R/W	Initial State
Reserved	[31:8]	Reserved	R	0x0
pio_dev_fed	[7:0]	8-bit PIO device feature/ error (command block) register	R/W	0x00

5.11.2.18 ATA PIO Device Sector Count Register (ATA_PIO_SCR, R/W, Address = 0xE820_005C)

ATA_PIO_SCR	Bit	Description	R/W	Initial State
Reserved	[31:8]	Reserved	R	0x0
pio_dev_scr	[7:0]	8-bit PIO device sector count (command block) register	R/W	0x00

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5.11.2.19 ATA PIO Device LBA Low Register (ATA_PIO_LLR, R/W, Address = 0xE820_0060)

ATA_PIO_LLR	Bit	Description	R/W	Initial State
Reserved	[31:8]	Reserved	R	0x0
pio_dev_llr	[7:0]	8-bit PIO device LBA low (command block) register	R/W	0x00

5.11.2.20 ATA PIO Device LBA Middle Register (ATA_PIO_LMR, R/W, Address = 0xE820_0064)

ATA_PIO_LMR	Bit	Description	R/W	Initial State
Reserved	[31:8]	Reserved	R	0x0
pio_dev_lmr	[7:0]	8-bit PIO device LBA middle (command block) register	R/W	0x00

5.11.2.21 ATA PIO Device LBA High Register (ATA_PIO_LHR, R/W, Address = 0xE820_0068)

ATA_PIO_LHR	Bit	Description	R/W	Initial State
Reserved	[31:8]	Reserved	R	0x0
pio_dev_lhr	[7:0]	8-bit PIO LBA high (command block) register	R/W	0x00

5.11.2.22 ATA PIO Device Register (ATA_PIO_DVR, R/W, Address = 0xE820_006C)

ATA_PIO_DVR	Bit	Description	R/W	Initial State
Reserved	[31:8]	Reserved	R	0x0
pio_dev_dvr	[7:0]	8-bit PIO device (command block) register	R/W	0x00

5.11.2.23 ATA PIO Device Command Status Register (ATA_PIO_CSD, R/W, Address = 0xE820_0070)

ATA_PIO_CSD	Bit	Description	R/W	Initial State
Reserved	[31:8]	Reserved	R	0x0
pio_dev_csd	[7:0]	8-bit PIO device command/status (command block) register	R/W	0x00

5.11.2.24 ATA PIO Device Control/Alternate Status Register (ATA_PIO_DAD, R/W, Address = 0xE820_0074)

ATA_PIO_DAD	Bit	Description	R/W	Initial State
Reserved	[31:8]	Reserved	R	0x0
pio_dev_dad	[7:0]	8-bit PIO device control/ alternate status (control block) register	R/W	0x00

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5.11.2.25 ATA PIO Data Ready Register (ATA_PIO_READY, R, Address = 0xE820_0078)

ATA_PIO_READY	Bit	Description	R/W	Initial State
Reserved	[31:2]	Reserved	R	0x0
dev_acc_ready	[1]	Indicates whether host can start access to device register 0 = Not ready to start access ATA device register 1 = Ready to start access ATA device register	R	0x1
pio_data_ready	[0]	Indicates whether data is valid in ATA_PIO_DATA register 0 = No valid data in ATA_PIO_DATA register 1 = Valid data in ATA_PIO_DATA register	R	0x1

5.11.2.26 ATA PIO Read Data Register (ATA_PIO_RDATA, R, Address = 0xE820_007C)

ATA_PIO_RDATA	Bit	Description	R/W	Initial State
Reserved	[31:16]	Reserved	R	0x0
pio_rdata	[15:0]	PIO read data register while HOST read from ATA device register	R	0x0000

5.11.2.27 AHB Bus FIFO Status Register (BUS_FIFO_STATUS, R, Address = 0xE820_0080)

BUS_FIFO_STATUS	Bit	Description	R/W	Initial State
Reserved	[31:19]	Reserved	R	0x0
bus_state[2:0]	[18:16]	3'b000 = IDLE 3'b001 = BUSYW 3'b010 = PREP 3'b011 = BUSYR 3'b100 = PAUSER 3'b101 = PAUSEW 3'b110 = PAUSER2	R	0x00
Reserved	[15:14]	Reserved	R	0x0
bus_fifo_rdpnt	[13:8]	Bus FIFO read pointer	R	0x00
Reserved	[7:6]	Reserved	R	0x0
bus_fifo_wrpnt	[5:0]	Bus FIFO write pointer	R	0x00

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5.11.2.28 ATA FIFO Status Register (ATA_FIFO_STATUS, R, Address = 0xE820_0084)

ATA_FIFO_STATUS	Bit	Description	R/W	Initial State
Reserved	[31]	Reserved	R	0x0
ata_state	[30:28]	0 = ATA_IDLE 1 = ATA_TRANS 2 = ATA_PAUSE 3 = ATA_PAUSE2 4 = ATA_ABORT	R	0x0000
pio_state	[27:26]	2'b00 = IDLE 2'b01 = T1 2'b10 = T2 2'b11 = TEOC	R	0x0
pdma_state	[25:24]	2'b00 = IDLE 2'b01 = T1 2'b10 = T2 2'b11 = TEOC	R	0x0
Reserved	[23]	Reserved	R	0x0
dma_state[1:0]	[22:21]	0 = IDLE 1 = TD 2 = TM 3 = TEOC	R	0x00
udma_state[4:0]	[20:16]	5'b00000 = IDLE 5'b00001 = TMI 5'b00010 = CRCS 5'b00011 = CRCH 5'b00100 = END 5'b01000 = STOPW 5'b01001 = ACKW 5'b01010 = NSEQWS 5'b01011 = NSEQWH 5'b01100 = SEQWS 5'b01101 = SEQWH 5'b01110 = TSSW 5'b10000 = STOPR 5'b10001 = ACKR 5'b10010 = NSEQR 5'b10011 = SEQR 5'b10100 = TRPR 5'b10101 = STRPR	R	0x00
Reserved	[15:0]	Reserved	R	0x0

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6 EXTERNAL BUS INTERFACE

6.1 OVERVIEW OF EXTERNAL BUS INTERFACE

The External Bus Interface (EBI) is used as a peripheral in S5PV210. It relies on memory controller to release external requests for external bus when the memory controller is idle, since it has no knowledge of when memory access will begin or complete. It enables one SROM controller, one OneNAND controller, and one NAND Flash controller, to share an external memory bus, Memory Port 0.

6.2 KEY FEATURES OF S5PV210 EBI

The key features of S5PV210 EBI include:

Memory Port 0 is shared using EBI.

* Reference: ARM PrimeCell External Bus Interface (PL220) and ARM DDI 0249B.

- Three memory controllers (SROMC, OneNANDC, and NFCON) share the pad interface.
- Priority determines the pad interface ownership (can be changed).
- The handshaking between EBI and memory controller consists of a three-wire interface: EBIREQ, EBIGNT, and EBIBACKOFF (all Active High).
- The memory controllers assert EBIREQ signals when they require external bus access.
- The arbitrated EBIGNT is issued to the memory controller with highest priority.
- The memory controller must complete the current transfer and release the bus. To signal these actions, EBIBACKOFF is made the output of EBI.
- The EBI arbitration scheme tracks the memory controller that is currently granted and waits for the transaction from the memory controller to finish (EBIREQ is set to Low by the memory controller) before it grants the next memory controller. If a higher priority memory controller requests the bus, then EBIBACKOFF signal informs the currently granted memory controller to terminate the current transfer as soon as possible.
- The System Controller provides booting method and CS selection information to Memory Subsystem.
- nCS0 and nCS1 in memory port 0 are only reserved for SROMC.
- If NAND Flash or OneNAND is selected for boot device, nCS2 is used to access the boot media.
- EBIGNT is required to be deasserted one cycle after EBIREQ is deasserted in sync. mode.
- EBIBACKOFF is required to be deasserted one cycle after EBIREQ is deasserted in sync. mode.
- In case EBIREQ is deasserted because of higher priority EBIBACKOFF, EBIREQ signal must be set to low for at least one clock cycle in sync. mode.
- EBI_REQ duration is not required for at least 4 cycles from CSYSREQ to CACTIVE

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6.3 BLOCK DIAGRAM OF MEMORY INTERFACE THROUGH EBI

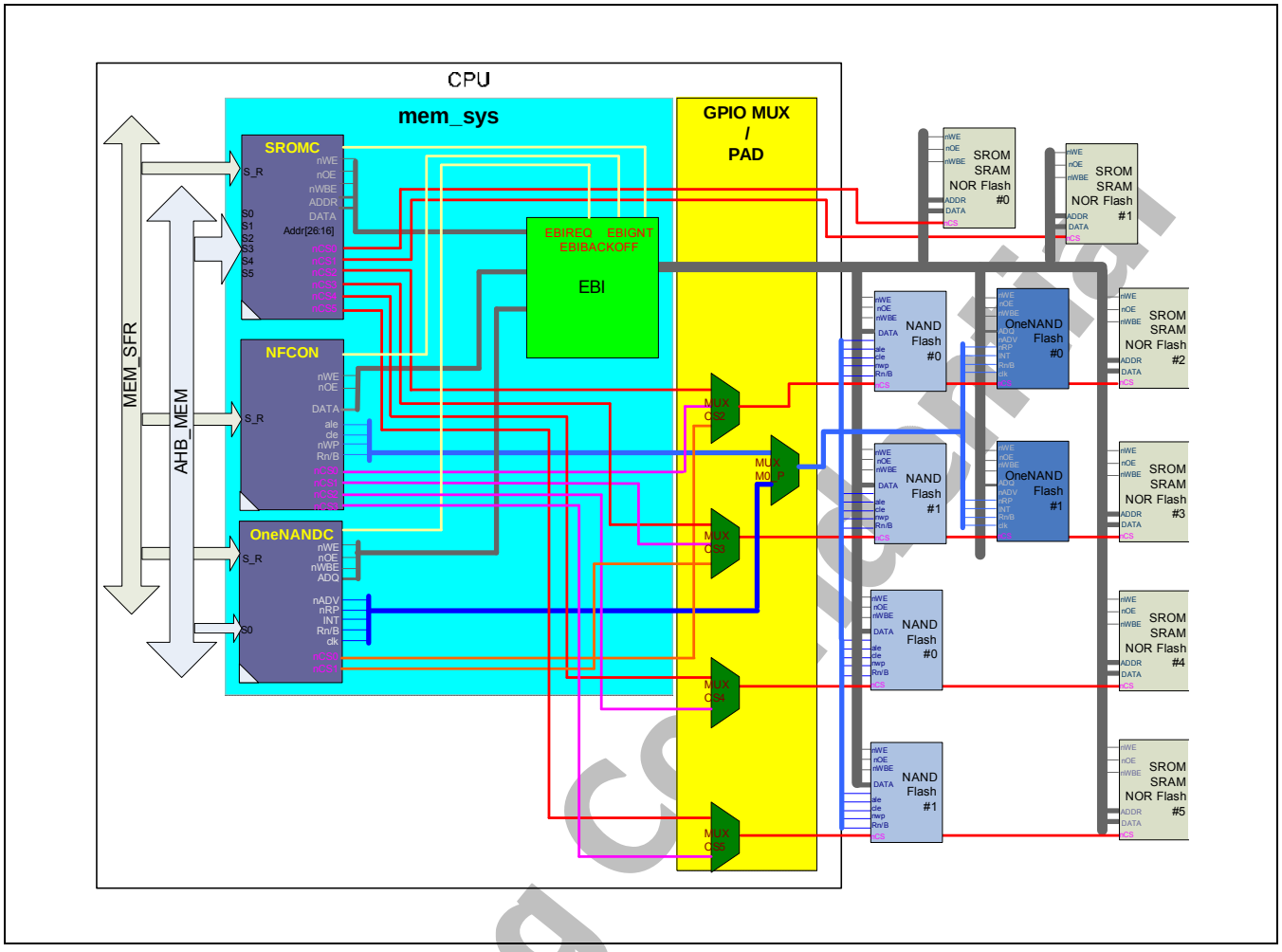

Figure 6-1 Memory Interface Through EBI

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6.4 CLOCK SCHEME OF MEMORY CONTROLLERS AND EBI

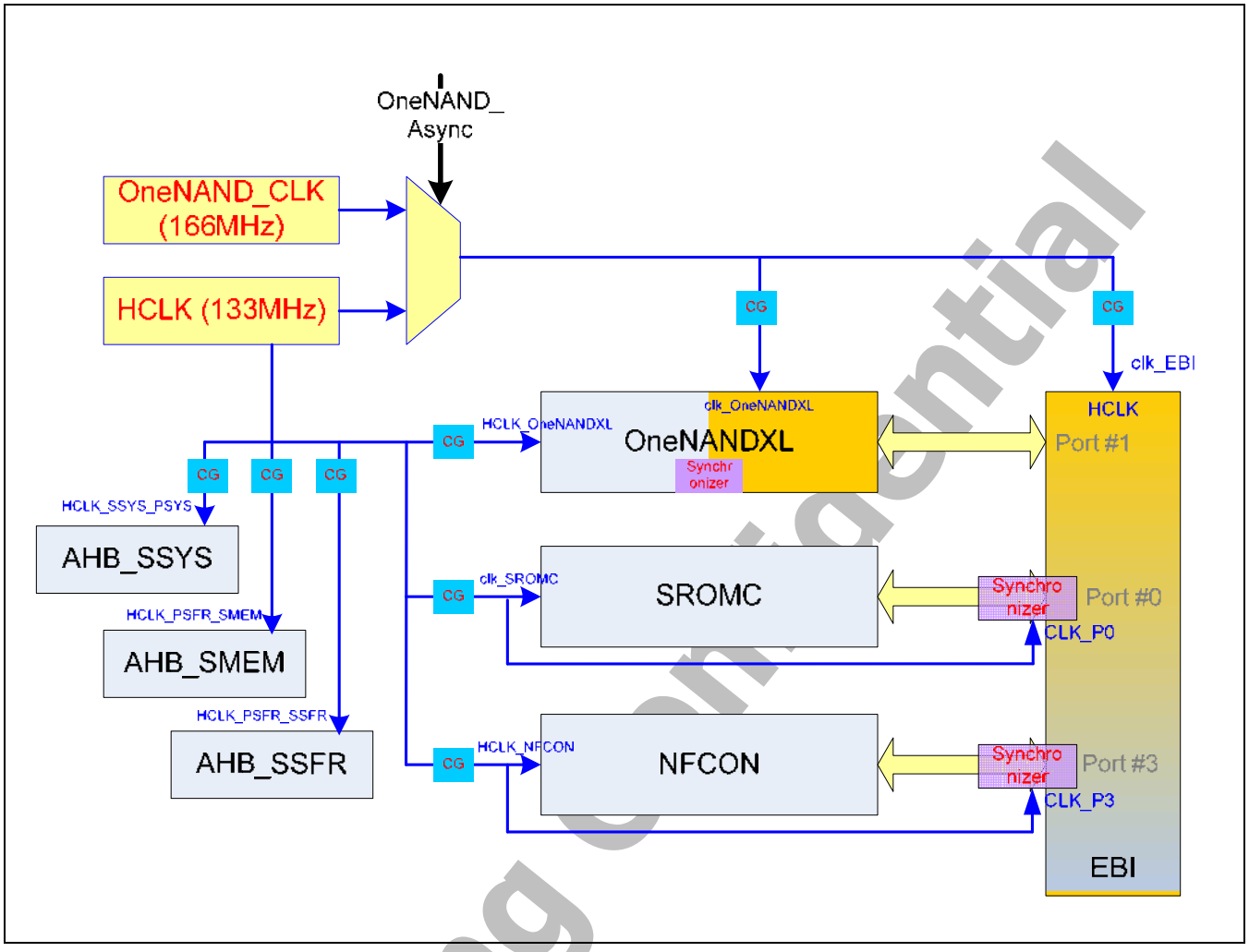

Figure 6-2 Clock Scheme of Memory Controllers and EBI

NOTE: The OneNAND Clock selection register name in Section 2-3, “Clock Controller” is OneNAND_SEL (OneNAND_Async). The register address is 0xE010_0200 (CLK_SRC0[28]).

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Section 6

DMA

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1 DMA CONTROLLER

1.1 OVERVIEW OF DMA CONTROLLER

S5PV210 supports two Direct Memory Access (DMA) tops: one for Memory-to-Memory (M2M) transfer (DMA_mem) and other for Peripheral-to-memory transfer and vice-versa (DMA_peri). The M2M DMA top consists of PL330 and some logics. On the other hand, Peri DMA top consists of two PL330s (DMA0 and DMA1) and dma_map.

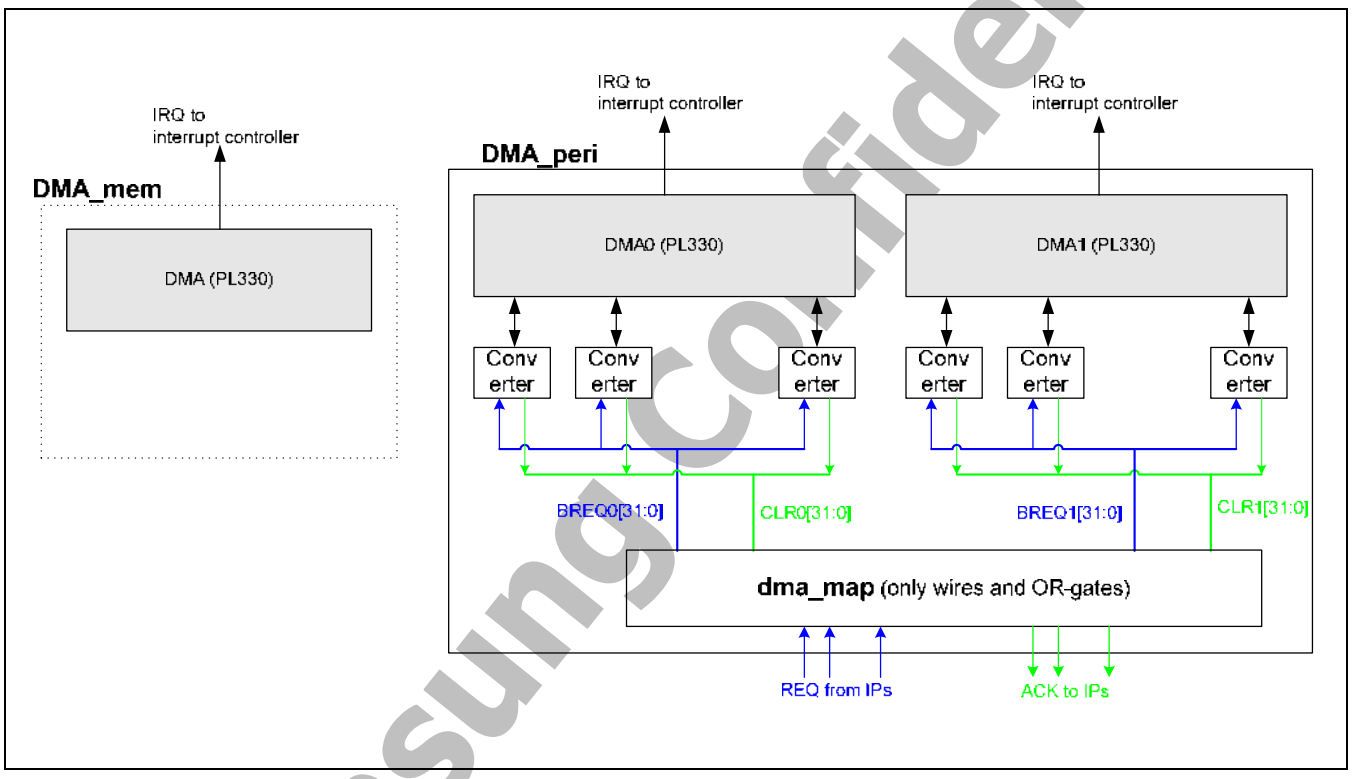

Figure 1-1 Two DMA Tops

All peripherals must be set as non-secure at TrustZone Protection Controller (TZPC) module, since DMA_peri operates only as non-secure.

The bus interface of PL330 is AXI, so that DMA_mem and DMA_peri are attached to AXI_B0 and AXI_B1 respectively (For more information, refer to Section, “3-1.Bus Configuration”).

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1.1.1 KEY FEATURES OF DMA CONTROLLER

The key features of DMA Controller are listed below as reference for DMA and for writing DMA assembly code.

Key Features	DMA_mem	DMA_peri
Supports Data Size	Up to double word (64-bit)	Up to word (32-bit)
Supports Burst Size	Up to 16 burst	Word transfer: Up to 8 burst
		Byte or word transfer: Up to 16 burst
Supports Channel	8 channels at the same time	16 channels at the same time

Although each DMA module has 32 interrupt sources, only one interrupt is sent to Vectored Interrupt Controller (VIC) for each DMA. To see the interrupt number of DMA, refer to the interrupt number table in Chapter, “04.01.Interrupt Controller”. The software reads Interrupt Status (INTSTATUS) register for each module to check whether an interrupt occurs.

Table 1-1 DMA Request Mapping Table

Module	No.	DMA Request	Category	Service Module
Peri DMA1	31	PCM2_TX	Audio	by only DMA1
	30	PCM2_RX		
	29	MSM_REQ3	Others	
	28	MSM_REQ2		
	27	MSM_REQ1		
	26	MSM_REQ0		
	25	PCM1_TX	Audio and SPI	
	24	PCM1_RX		
	23	PCM0_TX		
	22	PCM0_RX		
	21			
	20			
	19	SPI1_TX		
	18	SPI1_RX		
	17	SPI0_TX		
	16	SPI0_RX		
	15	I2S2_TX		
	14	I2S2_RX		
	13	I2S1_TX		
	12	I2S1_RX		
	11	I2S0S_TX		
	10	I2S0_TX		
	9	I2S0_RX		
	8	Reserved	System	

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Module	No.	DMA Request	Category	Service Module
	7	UART3_TX		
	6	UART3_RX		
	5	UART2_TX		
	4	UART2_RX		
	3	UART1_TX		
	2	UART1_RX		
	1	UART0_TX		
	0	UART0_RX		
Peri DMA0	31	Reserved		
	30	Reserved		
	29	Reserved	Others	by only DMA0
	28	Reserved		
	27	SPDIF		
	26	PWM		
	25	Reserved		
	24	AC_PCMout	Audio and SPI	
	23	AC_PCMin		
	22	AC_MICin		
	21			
	20			
	19	SPI1_TX		
	18	SPI1_RX		
	17	SPI0_TX		
	16	SPI0_RX		
	15	Reserved		
	14	Reserved		
	13	I2S1_TX		
	12	I2S1_RX		
	11	I2S0S_TX		
	10	I2S0_TX		
	9	I2S0_RX		
	8	Reserved	System	
	7	UART3_TX		
	6	UART3_RX		
	5	UART2_TX		
	4	UART2_RX		

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Module	No.	DMA Request	Category	Service Module
	3	UART1_TX		
	2	UART1_RX		
	1	UART0_TX		
	0	UART0_RX		
DMA_mem			Security	by M2M DMA only

Caution: When PDMA0 or PDMA1 are enabled, the CLK_GATE_IP2[8] at SYSCON must be set to 1.

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1.2 REGISTER DESCRIPTION

Most Special Function Registers (SFRs) are read-only. The main role of SFR is to check the PL330 status. There are many SFRs for PL330. In this section, only S5PV210-specific SFRs are explained. For more information, refer to Chapter 3, “PL330 TRM”.

1.2.1 REGISTER MAP

Table 1-2 describes the base address of each PL330 block.

Table 1-2 DMA_mem Register Summary

Register	Address	R/W	Description	Reset Value
DS	0xFA20_0000	R	Specifies the DMA Status Register. For more information, refer to page 3-11 of “PL330 TRM”.	0x0
DPC	0xFA20_0004	R	Specifies the DMA Program Counter Register. For more information, refer to page 3-13 of “PL330 TRM”.	0x0
-	0xFA20_0008-0xFA20_001C	-	Reserved	-
INTEN	0xFA20_0020	R/W	Specifies the Interrupt Enable Register. For more information, refer to page 3-13 of “PL330 TRM”.	0x0
ES	0xFA20_0024	R	Specifies the Event Status Register. For more information, refer to page 3-14 of “PL330 TRM”.	0x0
INTSTATUS	0xFA20_0028	R	Specifies the Interrupt Status Register. For more information, refer to page 3-16 of “PL330 TRM”.	0x0
INTCLR	0xFA20_002C	W	Specifies the Interrupt Clear Register. For more information, refer to page 3-17 of “PL330 TRM”.	0x0
FSM	0xFA20_0030	R	Specifies the Fault Status DMA Manager Register. For more information, refer to page 3-18 of “PL330 TRM”.	0x0
FSC	0xFA20_0034	R	Specifies the Fault Status DMA Channel Register. For more information, refer to page 3-19 of “PL330 TRM”.	0x0
FTM	0xFA20_0038	R	Specifies the Fault Type DMA Manager Register. For more information, refer to page 3-20 of “PL330 TRM”.	0x0
-	0xFA20_003C	-	Reserved	-
FTC0	0xFA20_0040	R	Specifies the Fault type for DMA Channel 0.	0x0
FTC1	0xFA20_0044	R	Specifies the Fault type for DMA Channel 1.	0x0
FTC2	0xFA20_0048	R	Specifies the Fault type for DMA Channel 2.	0x0
FTC3	0xFA20_004C	R	Specifies the Fault type for DMA Channel 3.	0x0
FTC4	0xFA20_0050	R	Specifies the Fault type for DMA Channel 4.	0x0
FTC5	0xFA20_0054	R	Specifies the Fault type for DMA Channel 5.	0x0
FTC6	0xFA20_0058	R	Specifies the Fault type for DMA Channel 6.	0x0
FTC7	0xFA20_005C	R	Specifies the Fault type for DMA Channel 7.	0x0

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Register	Address	R/W	Description	Reset Value
	0xFA20_0060- 0xFA20_00FC		Reserved	
Channel Status Registers. For more information, refer to page 3-24 of “PL330 TRM”.				
CS0	0xFA20_0100	R	Specifies the Channel Status for DMA Channel 0.	0x0
CS1	0xFA20_0108	R	Specifies the Channel Status for DMA Channel 1.	0x0
CS2	0xFA20_0110	R	Specifies the Channel Status for DMA Channel 2.	0x0
CS3	0xFA20_0118	R	Specifies the Channel Status for DMA Channel 3.	0x0
CS4	0xFA20_0120	R	Specifies the Channel Status for DMA Channel 4.	0x0
CS5	0xFA20_0128	R	Specifies the Channel Status for DMA Channel 5.	0x0
CS6	0xFA20_0130	R	Specifies the Channel Status for DMA Channel 6.	0x0
CS7	0xFA20_0138	R	Specifies the Channel Status for DMA Channel 7.	0x0
Channel Program Counter Registers. For more information, refer to page 3-26 of “PL330 TRM”.				
CPC0	0xFA20_0104	R	Specifies the Channel PC for DMA Channel 0.	0x0
CPC1	0xFA20_010C	R	Specifies the Channel PC for DMA Channel 1.	0x0
CPC2	0xFA20_0114	R	Specifies the Channel PC for DMA Channel 2.	0x0
CPC3	0xFA20_011C	R	Specifies the Channel PC for DMA Channel 3.	0x0
CPC4	0xFA20_0124	R	Specifies the Channel PC for DMA Channel 4.	0x0
CPC5	0xFA20_012C	R	Specifies the Channel PC for DMA Channel 5.	0x0
CPC6	0xFA20_0134	R	Specifies the Channel PC for DMA Channel 6.	0x0
CPC7	0xFA20_013C	R	Specifies the Channel PC for DMA Channel 7.	0x0
-	0xFA20_0140- 0xFA20_03FC	-	Reserved	-
Source Address Registers. For more information, refer to page 3-27 of “PL330 TRM”.				
SA_0	0xFA20_0400	R	Specifies the Source Address for DMA Channel 0.	0x0
SA_1	0xFA20_0420	R	Specifies the Source Address for DMA Channel 1.	0x0
SA_2	0xFA20_0440	R	Specifies the Source Address for DMA Channel 2.	0x0
SA_3	0xFA20_0460	R	Specifies the Source Address for DMA Channel 3.	0x0
SA_4	0xFA20_0480	R	Specifies the Source Address for DMA Channel 4.	0x0
SA_5	0xFA20_04A0	R	Specifies the Source Address for DMA Channel 5.	0x0
SA_6	0xFA20_04C0	R	Specifies the Source Address for DMA Channel 6.	0x0
SA_7	0xFA20_04E0	R	Specifies the Source Address for DMA Channel 7.	0x0
Destination Address Registers. For more information, refer to page 3-29 of “PL330 TRM”.				
DA_0	0xFA20_0404	R	Specifies the Destination Address for DMA Channel 0.	0x0
DA_1	0xFA20_0424	R	Specifies the Destination Address for DMA Channel 1.	0x0
DA_2	0xFA20_0444	R	Specifies the Destination Address for DMA Channel 2.	0x0

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Register	Address	R/W	Description	Reset Value
DA_3	0xFA20_0464	R	Specifies the Destination Address for DMA Channel 3.	0x0
DA_4	0xFA20_0484	R	Specifies the Destination Address for DMA Channel 4.	0x0
DA_5	0xFA20_04A4	R	Specifies the Destination Address for DMA Channel 5.	0x0
DA_6	0xFA20_04C4	R	Specifies the Destination Address for DMA Channel 6.	0x0
DA_7	0xFA20_04E4	R	Specifies the Destination Address for DMA Channel 7.	0x0
Channel Control Registers. For more information, refer to page 3-30 of “PL330 TRM”.				
CC_0	0xFA20_0408	R	Specifies the Channel Control for DMA Channel 0.	0x0
CC_1	0xFA20_0428	R	Specifies the Channel Control for DMA Channel 1.	0x0
CC_2	0xFA20_0448	R	Specifies the Channel Control for DMA Channel 2.	0x0
CC_3	0xFA20_0468	R	Specifies the Channel Control for DMA Channel 3.	0x0
CC_4	0xFA20_0488	R	Specifies the Channel Control for DMA Channel 4.	0x0
CC_5	0xFA20_04A8	R	Specifies the Channel Control for DMA Channel 5.	0x0
CC_6	0xFA20_04C8	R	Specifies the Channel Control for DMA Channel 6.	0x0
CC_7	0xFA20_04E8	R	Specifies the Channel Control for DMA Channel 7.	0x0
Loop Counter 0 Registers. For more information, refer to page 3-35 of “PL330 TRM”.				
LC0_0	0xFA20_040C	R	Specifies the Loop Counter 0 for DMA Channel 0.	0x0
LC0_1	0xFA20_042C	R	Specifies the Loop Counter 0 for DMA Channel 1.	0x0
LC0_2	0xFA20_044C	R	Specifies the Loop Counter 0 for DMA Channel 2.	0x0
LC0_3	0xFA20_046C	R	Specifies the Loop Counter 0 for DMA Channel 3.	0x0
LC0_4	0xFA20_048C	R	Specifies the Loop Counter 0 for DMA Channel 4.	0x0
LC0_5	0xFA20_04AC	R	Specifies the Loop Counter 0 for DMA Channel 5.	0x0
LC0_6	0xFA20_04CC	R	Specifies the Loop Counter 0 for DMA Channel 6.	0x0
LC0_7	0xFA20_04EC	R	Specifies the Loop Counter 0 for DMA Channel 7.	0x0
Loop Counter 1 Registers. For more information, refer to page 3-36 of “PL330 TRM”.				
LC1_0	0xFA20_0410	R	Specifies the Loop Counter 1 for DMA Channel 0.	0x0
LC1_1	0xFA20_0430	R	Specifies the Loop Counter 1 for DMA Channel 1.	0x0
LC1_2	0xFA20_0450	R	Specifies the Loop Counter 1 for DMA Channel 2.	0x0
LC1_3	0xFA20_0470	R	Specifies the Loop Counter 1 for DMA Channel 3.	0x0
LC1_4	0xFA20_0490	R	Specifies the Loop Counter 1 for DMA Channel 4.	0x0
LC1_5	0xFA20_04B0	R	Specifies the Loop Counter 1 for DMA Channel 5.	0x0
LC1_6	0xFA20_04D0	R	Specifies the Loop Counter 1 for DMA Channel 6.	0x0
LC1_7	0xFA20_04F0	R	Specifies the Loop Counter 1 for DMA Channel 7.	0x0
Reserved	0xFA20_0414-0xFA20_041C	-	Reserved	-

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Register	Address	R/W	Description	Reset Value
Reserved	0xFA20_0434-0xFA20_043C	-	Reserved	-
Reserved	0xFA20_0454-0xFA20_045C	-	Reserved	-
Reserved	0xFA20_0474-0xFA20_047C	-	Reserved	-
Reserved	0xFA20_0494-0xFA20_049C	-	Reserved	-
Reserved	0xFA20_04B4-0xFA20_04BC	-	Reserved	-
Reserved	0xFA20_04D4-0xFA20_04DC	-	Reserved	-
Reserved	0xFA20_04F4-0xFA20_0CFC	-	Reserved	-
DBGSTATUS	0xFA20_0D00	R	Specifies the Debug Status Register. For more information, refer to page 3-37 of “PL330 TRM”.	0x0
DBGCMD	0xFA20_0D04	W	Specifies the Debug Command Register. For more information, refer to page 3-37 of “PL330 TRM”.	-
DBGINST0	0xFA20_0D08	W	Specifies the Debug Instruction-0 Register. For more information, refer to page 3-38 of “PL330 TRM”.	-
DBGINST1	0xFA20_0D0C	W	Specifies the Debug Instruction-1 Register. For more information, refer to page 3-39 of “PL330 TRM”.	-
CR0	0xFA20_0E00	R	Specifies the Configuration Register 0. For more information, refer to page 3-40 of “PL330 TRM”.	0x003E_1071
CR1	0xFA20_0E04	R	Specifies the Configuration Register 1. For more information, refer to page 3-42 of “PL330 TRM”.	0x0000_0075
CR2	0xFA20_0E08	R	Specifies the Configuration Register 2. For more information, refer to page 3-43 of “PL330 TRM”.	0x0
CR3	0xFA20_0E0C	R	Specifies the Configuration Register 3. For more information, refer to page 3-44 of “PL330 TRM”.	0xFFFF_FFFF
CR4	0xFA20_0E10	R	Specifies the Configuration Register 4. For more information, refer to page 3-45 of “PL330 TRM”.	0x0000_0003
CRDn	0xFA20_0E14	R	Specifies the Configuration Register Dn. For more information, refer to page 3-46 of “PL330 TRM”.	0x01F7_3733
periph_id_n	0xFA20_0FE0 - 0xFA20_0FEC	R	Specifies the Peripheral Identification Registers 0-3. For more information, refer to page 3-48 of “PL330 TRM”.	Configuration-dependent
pcell_id_n	0xFA20_0FF0 – 0xFA20_0FFC	R	Specifies the PrimeCell Identification Registers 0-3. For more information, refer to page 3-50 of “PL330 TRM”.	Configuration-dependent

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Table 1-3 DMA_peri0 Register Summary

Register	Address	R/W	Description	Reset Value
DS	0xE090_0000	R	Specifies the DMA Status Register. For more information, refer to page 3-11 of “PL330 TRM”.	0x0
DPC	0xE090_0004	R	Specifies the DMA Program Counter Register. For more information, refer to page 3-13 of “PL330 TRM”.	0x0
Reserved	0xE090_0008-0xE090_001C	-	Reserved	-
INTEN	0xE090_0020	R/W	Specifies the Interrupt Enable Register. For more information, refer to page 3-13 of “PL330 TRM”.	0x0
ES	0xE090_0024	R	Specifies the Event Status Register. For more information, refer to page 3-14 of “PL330 TRM”.	0x0
INTSTATUS	0xE090_0028	R	Specifies the Interrupt Status Register. For more information, refer to page 3-16 of “PL330 TRM”.	0x0
INTCLR	0xE090_002C	W	Specifies the Interrupt Clear Register. For more information, refer to page 3-17 of “PL330 TRM”.	0x0
FSM	0xE090_0030	R	Specifies the Fault Status DMA Manager Register. For more information, refer to page 3-18 of “PL330 TRM”.	0x0
FSC	0xE090_0034	R	Specifies the Fault Status DMA Channel Register. For more information, refer to page 3-19 of “PL330 TRM”.	0x0
FTM	0xE090_0038	R	Specifies the Fault Type DMA Manager Register. For more information, refer to page 3-20 of PL330 TRM”.	0x0
Reserved	0xE090_003C	-	Reserved	-
FTC0	0xE090_0040	R	Specifies the Fault Type for DMA Channel 0.	0x0
FTC1	0xE090_0044	R	Specifies the Fault Type for DMA Channel 1.	0x0
FTC2	0xE090_0048	R	Specifies the Fault Type for DMA Channel 2.	0x0
FTC3	0xE090_004C	R	Specifies the Fault Type for DMA Channel 3.	0x0
FTC4	0xE090_0050	R	Specifies the Fault Type for DMA Channel 4.	0x0
FTC5	0xE090_0054	R	Specifies the Fault Type for DMA Channel 5.	0x0
FTC6	0xE090_0058	R	Specifies the Fault Type for DMA Channel 6.	0x0
FTC7	0xE090_005C	R	Specifies the Fault Type for DMA Channel 7.	0x0
Reserved	0xE090_0060-0xE090_00FC		Reserved	
Channel Status Registers. For more information, refer to page 3-24 of “PL330 TRM”.				
CS0	0xE090_0100	R	Specifies the Channel Status for DMA Channel 0.	0x0
CS1	0xE090_0108	R	Specifies the Channel Status for DMA Channel 1.	0x0
CS2	0xE090_0110	R	Specifies the Channel Status for DMA Channel 2.	0x0
CS3	0xE090_0118	R	Specifies the Channel Status for DMA Channel 3.	0x0

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Register	Address	R/W	Description	Reset Value
CS4	0xE090_0120	R	Specifies the Channel Status for DMA Channel 4.	0x0
CS5	0xE090_0128	R	Specifies the Channel Status for DMA Channel 5.	0x0
CS6	0xE090_0130	R	Specifies the Channel Status for DMA Channel 6.	0x0
CS7	0xE090_0138	R	Specifies the Channel Status for DMA Channel 7.	0x0
Channel Program Counter Registers. For more information, refer to page 3-26 of “PL330 TRM”.				
CPC0	0xE090_0104	R	Specifies the Channel PC for DMA Channel 0.	0x0
CPC1	0xE090_010C	R	Specifies the Channel PC for DMA Channel 1.	0x0
CPC2	0xE090_0114	R	Specifies the Channel PC for DMA Channel 2.	0x0
CPC3	0xE090_011C	R	Specifies the Channel PC for DMA Channel 3.	0x0
CPC4	0xE090_0124	R	Specifies the Channel PC for DMA Channel 4.	0x0
CPC5	0xE090_012C	R	Specifies the Channel PC for DMA Channel 5.	0x0
CPC6	0xE090_0134	R	Specifies the Channel PC for DMA Channel 6.	0x0
CPC7	0xE090_013C	R	Specifies the Channel PC for DMA Channel 7.	0x0
Reserved	0xE090_0140- 0xE090_03FC	-	Reserved	-
Source Address Registers. For more information, refer to page 3-27 of “PL330 TRM”.				
SA_0	0xE090_0400	R	Specifies the Source Address for DMA Channel 0.	0x0
SA_1	0xE090_0420	R	Specifies the Source Address for DMA Channel 1.	0x0
SA_2	0xE090_0440	R	Specifies the Source Address for DMA Channel 2.	0x0
SA_3	0xE090_0460	R	Specifies the Source Address for DMA Channel 3.	0x0
SA_4	0xE090_0480	R	Specifies the Source Address for DMA Channel 4.	0x0
SA_5	0xE090_04A0	R	Specifies the Source Address for DMA Channel 5.	0x0
SA_6	0xE090_04C0	R	Specifies the Source Address for DMA Channel 6.	0x0
SA_7	0xE090_04E0	R	Specifies the Source Address for DMA Channel 7.	0x0
Destination Address Registers. For more information, refer to page 3-29 of “PL330 TRM”.				
DA_0	0xE090_0404	R	Specifies the Destination Address for DMA Channel 0.	0x0
DA_1	0xE090_0424	R	Specifies the Destination Address for DMA Channel 1.	0x0
DA_2	0xE090_0444	R	Specifies the Destination Address for DMA Channel 2.	0x0
DA_3	0xE090_0464	R	Specifies the Destination Address for DMA Channel 3.	0x0
DA_4	0xE090_0484	R	Specifies the Destination Address for DMA Channel 4.	0x0
DA_5	0xE090_04A4	R	Specifies the Destination Address for DMA Channel 5.	0x0
DA_6	0xE090_04C4	R	Specifies the Destination Address for DMA Channel 6.	0x0

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Register	Address	R/W	Description	Reset Value
DA_7	0xE090_04E4	R	Specifies the Destination Address for DMA Channel 7.	0x0
Channel Control Registers. For more information, refer to page 3-30 of “PL330 TRM”.				
CC_0	0xE090_0408	R	Specifies the Channel Control for DMA Channel 0.	0x0
CC_1	0xE090_0428	R	Specifies the Channel Control for DMA Channel 1.	0x0
CC_2	0xE090_0448	R	Specifies the Channel Control for DMA Channel 2.	0x0
CC_3	0xE090_0468	R	Specifies the Channel Control for DMA Channel 3.	0x0
CC_4	0xE090_0488	R	Specifies the Channel Control for DMA Channel 4.	0x0
CC_5	0xE090_04A8	R	Specifies the Channel Control for DMA Channel 5.	0x0
CC_6	0xE090_04C8	R	Specifies the Channel Control for DMA Channel 6.	0x0
CC_7	0xE090_04E8	R	Specifies the Channel Control for DMA Channel 7.	0x0
Loop Counter 0 Registers. For more information, refer to page 3-35 of “PL330 TRM”.				
LC0_0	0xE090_040C	R	Specifies the Loop Counter 0 for DMA Channel 0.	0x0
LC0_1	0xE090_042C	R	Specifies the Loop Counter 0 for DMA Channel 1.	0x0
LC0_2	0xE090_044C	R	Specifies the Loop Counter 0 for DMA Channel 2.	0x0
LC0_3	0xE090_046C	R	Specifies the Loop Counter 0 for DMA Channel 3.	0x0
LC0_4	0xE090_048C	R	Specifies the Loop Counter 0 for DMA Channel 4.	0x0
LC0_5	0xE090_04AC	R	Specifies the Loop Counter 0 for DMA Channel 5.	0x0
LC0_6	0xE090_04CC	R	Specifies the Loop Counter 0 for DMA Channel 6.	0x0
LC0_7	0xE090_04EC	R	Specifies the Loop Counter 0 for DMA Channel 7.	0x0
Loop Counter 1 Registers. For more information, refer to page 3-36 of “PL330 TRM”.				
LC1_0	0xE090_0410	R	Specifies the Loop Counter 1 for DMA Channel 0.	0x0
LC1_1	0xE090_0430	R	Specifies the Loop Counter 1 for DMA Channel 1.	0x0
LC1_2	0xE090_0450	R	Specifies the Loop Counter 1 for DMA Channel 2.	0x0
LC1_3	0xE090_0470	R	Specifies the Loop Counter 1 for DMA Channel 3.	0x0
LC1_4	0xE090_0490	R	Specifies the Loop Counter 1 for DMA Channel 4.	0x0
LC1_5	0xE090_04B0	R	Specifies the Loop Counter 1 for DMA Channel 5.	0x0
LC1_6	0xE090_04D0	R	Specifies the Loop Counter 1 for DMA Channel 6.	0x0
LC1_7	0xE090_04F0	R	Specifies the Loop Counter 1 for DMA Channel 7.	0x0
Reserved	0xE090_0414-0xE090_041C	-	Reserved	-
Reserved	0xE090_0434-0xE090_043C	-	Reserved	-
Reserved	0xE090_0454-0xE090_045C	-	Reserved	-
Reserved	0xE090_0474-0xE090_047C	-	Reserved	-
Reserved	0xE090_0494-0xE090_049C	-	Reserved	-

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Register	Address	R/W	Description	Reset Value
Reserved	0xE090_04B4-0xE090_04BC	-	Reserved	-
Reserved	0xE090_04D4-0xE090_04DC	-	Reserved	-
Reserved	0xE090_04F4-0xE090_0CFC	-	Reserved	-
DBGSTATUS	0xE090_0D00	R	Specifies the Debug Status Register on page 3-37 of “TRM”.	0x0
DBGCMD	0xE090_0D04	W	Specifies the Debug Command Register. For more information, refer to page 3-37 of “PL330 TRM”.	-
DBGINST0	0xE090_0D08	W	Specifies the Debug Instruction-0 Register. For more information, refer to page 3-38 of “PL330 TRM”.	-
DBGINST1	0xE090_0D0C	W	Specifies the Debug Instruction-1 Register. For more information, refer to page 3-39 of “PL330 TRM”.	-
CR0	0xE090_0E00	R	Specifies the Configuration Register 0. For more information, refer to page 3-40 of “PL330 TRM”.	0x003F_F075
CR1	0xE090_0E04	R	Specifies the Configuration Register 1. For more information, refer to page 3-42 of “PL330 TRM”.	0x0000_0074
CR2	0xE090_0E08	R	Specifies the Configuration Register 2. For more information, refer to page 3-43 of “PL330 TRM”.	0x0000_0000
CR3	0xE090_0E0C	R	Specifies the Configuration Register 3. For more information, refer to page 3-44 of “PL330 TRM”.	0xFFFF_FFFF
CR4	0xE090_0E10	R	Specifies the Configuration Register 4. For more information, refer to page 3-45 of “PL330 TRM”.	0xFFFF_FFFF
CRDn	0xE090_0E14	R	Specifies the Configuration Register Dn. For more information, refer to page 3-46 of “PL330 TRM”.	0x0077_3732
periph_id_n	0xE090_0FE0 - 0xE090_0FEC	R	Specifies the Peripheral Identification Registers 0-3. For more information, refer to page 3-48 of “PL330 TRM”.	Configuration-dependent
pcell_id_n	0xE090_0FF0 – 0xE090_0FFC	R	Specifies the PrimeCell Identification Registers 0-3. For more information refer to page 3-50 of PL330 TRM”	Configuration-dependent

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Table 1-4 DMA_peri0 Register Summary

Register	Address	R/W	Description	Reset Value
DS	0xE090_0000	R	Specifies the DMA Status Register. For more information, refer to page 3-11 of “PL330 TRM”.	0x0
DPC	0xE090_0004	R	Specifies the DMA Program Counter Register. For more information, refer to page 3-13 of “PL330 TRM”.	0x0
Reserved	0xE090_0008-0xE090_001C	-	Reserved	-
INTEN	0xE090_0020	R/W	Specifies the Interrupt Enable Register. For more information, refer to page 3-13 of “PL330 TRM”.	0x0
ES	0xE090_0024	R	Specifies the Event Status Register. For more information, refer to page 3-14 of “PL330 TRM”.	0x0
INTSTATUS	0xE090_0028	R	Specifies the Interrupt Status Register. For more information, refer to page 3-16 of “PL330 TRM”.	0x0
INTCLR	0xE090_002C	W	Specifies the Interrupt Clear Register. For more information, refer to page 3-17 of “PL330 TRM”.	0x0
FSM	0xE090_0030	R	Specifies the Fault Status DMA Manager Register. For more information, refer to page 3-18 of “PL330 TRM”.	0x0
FSC	0xE090_0034	R	Specifies the Fault Status DMA Channel Register. For more information, refer to page 3-19 of “PL330 TRM”.	0x0
FTM	0xE090_0038	R	Specifies the Fault Type DMA Manager Register. For more information, refer to page 3-20 of PL330 TRM”.	0x0
Reserved	0xE090_003C	-	Reserved	-
FTC0	0xE090_0040	R	Specifies the Fault Type for DMA Channel 0.	0x0
FTC1	0xE090_0044	R	Specifies the Fault Type for DMA Channel 1.	0x0
FTC2	0xE090_0048	R	Specifies the Fault Type for DMA Channel 2.	0x0
FTC3	0xE090_004C	R	Specifies the Fault Type for DMA Channel 3.	0x0
FTC4	0xE090_0050	R	Specifies the Fault Type for DMA Channel 4.	0x0
FTC5	0xE090_0054	R	Specifies the Fault Type for DMA Channel 5.	0x0
FTC6	0xE090_0058	R	Specifies the Fault Type for DMA Channel 6.	0x0
FTC7	0xE090_005C	R	Specifies the Fault Type for DMA Channel 7.	0x0
Reserved	0xE090_0060-0xE090_00FC		Reserved	
Channel Status Registers. For more information, refer to page 3-24 of “PL330 TRM”.				
CS0	0xE090_0100	R	Specifies the Channel Status for DMA Channel 0.	0x0
CS1	0xE090_0108	R	Specifies the Channel Status for DMA Channel 1.	0x0
CS2	0xE090_0110	R	Specifies the Channel Status for DMA Channel 2.	0x0
CS3	0xE090_0118	R	Specifies the Channel Status for DMA Channel 3.	0x0

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Register	Address	R/W	Description	Reset Value
CS4	0xE090_0120	R	Specifies the Channel Status for DMA Channel 4.	0x0
CS5	0xE090_0128	R	Specifies the Channel Status for DMA Channel 5.	0x0
CS6	0xE090_0130	R	Specifies the Channel Status for DMA Channel 6.	0x0
CS7	0xE090_0138	R	Specifies the Channel Status for DMA Channel 7.	0x0
Channel Program Counter Registers. For more information, refer to page 3-26 of “PL330 TRM”.				
CPC0	0xE090_0104	R	Specifies the Channel PC for DMA Channel 0.	0x0
CPC1	0xE090_010C	R	Specifies the Channel PC for DMA Channel 1.	0x0
CPC2	0xE090_0114	R	Specifies the Channel PC for DMA Channel 2.	0x0
CPC3	0xE090_011C	R	Specifies the Channel PC for DMA Channel 3.	0x0
CPC4	0xE090_0124	R	Specifies the Channel PC for DMA Channel 4.	0x0
CPC5	0xE090_012C	R	Specifies the Channel PC for DMA Channel 5.	0x0
CPC6	0xE090_0134	R	Specifies the Channel PC for DMA Channel 6.	0x0
CPC7	0xE090_013C	R	Specifies the Channel PC for DMA Channel 7.	0x0
Reserved	0xE090_0140- 0xE090_03FC	-	Reserved	-
Source Address Registers. For more information, refer to page 3-27 of “PL330 TRM”.				
SA_0	0xE090_0400	R	Specifies the Source Address for DMA Channel 0.	0x0
SA_1	0xE090_0420	R	Specifies the Source Address for DMA Channel 1.	0x0
SA_2	0xE090_0440	R	Specifies the Source Address for DMA Channel 2.	0x0
SA_3	0xE090_0460	R	Specifies the Source Address for DMA Channel 3.	0x0
SA_4	0xE090_0480	R	Specifies the Source Address for DMA Channel 4.	0x0
SA_5	0xE090_04A0	R	Specifies the Source Address for DMA Channel 5.	0x0
SA_6	0xE090_04C0	R	Specifies the Source Address for DMA Channel 6.	0x0
SA_7	0xE090_04E0	R	Specifies the Source Address for DMA Channel 7.	0x0
Destination Address Registers. For more information, refer to page 3-29 of “PL330 TRM”.				
DA_0	0xE090_0404	R	Specifies the Destination Address for DMA Channel 0.	0x0
DA_1	0xE090_0424	R	Specifies the Destination Address for DMA Channel 1.	0x0
DA_2	0xE090_0444	R	Specifies the Destination Address for DMA Channel 2.	0x0
DA_3	0xE090_0464	R	Specifies the Destination Address for DMA Channel 3.	0x0
DA_4	0xE090_0484	R	Specifies the Destination Address for DMA Channel 4.	0x0
DA_5	0xE090_04A4	R	Specifies the Destination Address for DMA Channel 5.	0x0
DA_6	0xE090_04C4	R	Specifies the Destination Address for DMA Channel 6.	0x0

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Register	Address	R/W	Description	Reset Value
DA_7	0xE090_04E4	R	Specifies the Destination Address for DMA Channel 7.	0x0
Channel Control Registers. For more information, refer to page 3-30 of “PL330 TRM”.				
CC_0	0xE090_0408	R	Specifies the Channel Control for DMA Channel 0.	0x0
CC_1	0xE090_0428	R	Specifies the Channel Control for DMA Channel 1.	0x0
CC_2	0xE090_0448	R	Specifies the Channel Control for DMA Channel 2.	0x0
CC_3	0xE090_0468	R	Specifies the Channel Control for DMA Channel 3.	0x0
CC_4	0xE090_0488	R	Specifies the Channel Control for DMA Channel 4.	0x0
CC_5	0xE090_04A8	R	Specifies the Channel Control for DMA Channel 5.	0x0
CC_6	0xE090_04C8	R	Specifies the Channel Control for DMA Channel 6.	0x0
CC_7	0xE090_04E8	R	Specifies the Channel Control for DMA Channel 7.	0x0
Loop Counter 0 Registers. For more information, refer to page 3-35 of “PL330 TRM”.				
LC0_0	0xE090_040C	R	Specifies the Loop Counter 0 for DMA Channel 0.	0x0
LC0_1	0xE090_042C	R	Specifies the Loop Counter 0 for DMA Channel 1.	0x0
LC0_2	0xE090_044C	R	Specifies the Loop Counter 0 for DMA Channel 2.	0x0
LC0_3	0xE090_046C	R	Specifies the Loop Counter 0 for DMA Channel 3.	0x0
LC0_4	0xE090_048C	R	Specifies the Loop Counter 0 for DMA Channel 4.	0x0
LC0_5	0xE090_04AC	R	Specifies the Loop Counter 0 for DMA Channel 5.	0x0
LC0_6	0xE090_04CC	R	Specifies the Loop Counter 0 for DMA Channel 6.	0x0
LC0_7	0xE090_04EC	R	Specifies the Loop Counter 0 for DMA Channel 7.	0x0
Loop Counter 1 Registers. For more information, refer to page 3-36 of “PL330 TRM”.				
LC1_0	0xE090_0410	R	Specifies the Loop Counter 1 for DMA Channel 0.	0x0
LC1_1	0xE090_0430	R	Specifies the Loop Counter 1 for DMA Channel 1.	0x0
LC1_2	0xE090_0450	R	Specifies the Loop Counter 1 for DMA Channel 2.	0x0
LC1_3	0xE090_0470	R	Specifies the Loop Counter 1 for DMA Channel 3.	0x0
LC1_4	0xE090_0490	R	Specifies the Loop Counter 1 for DMA Channel 4.	0x0
LC1_5	0xE090_04B0	R	Specifies the Loop Counter 1 for DMA Channel 5.	0x0
LC1_6	0xE090_04D0	R	Specifies the Loop Counter 1 for DMA Channel 6.	0x0
LC1_7	0xE090_04F0	R	Specifies the Loop Counter 1 for DMA Channel 7.	0x0
Reserved	0xE090_0414-0xE090_041C	-	Reserved	-
Reserved	0xE090_0434-0xE090_043C	-	Reserved	-
Reserved	0xE090_0454-0xE090_045C	-	Reserved	-
Reserved	0xE090_0474-0xE090_047C	-	Reserved	-
Reserved	0xE090_0494-0xE090_049C	-	Reserved	-

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Register	Address	R/W	Description	Reset Value
Reserved	0xE090_04B4-0xE090_04BC	-	Reserved	-
Reserved	0xE090_04D4-0xE090_04DC	-	Reserved	-
Reserved	0xE090_04F4-0xE090_0CFC	-	Reserved	-
DBGSTATUS	0xE090_0D00	R	Specifies the Debug Status Register on page 3-37 of “TRM”.	0x0
DBGCMD	0xE090_0D04	W	Specifies the Debug Command Register. For more information, refer to page 3-37 of “PL330 TRM”.	-
DBGINST0	0xE090_0D08	W	Specifies the Debug Instruction-0 Register. For more information, refer to page 3-38 of “PL330 TRM”.	-
DBGINST1	0xE090_0D0C	W	Specifies the Debug Instruction-1 Register. For more information, refer to page 3-39 of “PL330 TRM”.	-
CR0	0xE090_0E00	R	Specifies the Configuration Register 0. For more information, refer to page 3-40 of “PL330 TRM”.	0x003F_F075
CR1	0xE090_0E04	R	Specifies the Configuration Register 1. For more information, refer to page 3-42 of “PL330 TRM”.	0x0000_0074
CR2	0xE090_0E08	R	Specifies the Configuration Register 2. For more information, refer to page 3-43 of “PL330 TRM”.	0x0000_0000
CR3	0xE090_0E0C	R	Specifies the Configuration Register 3. For more information, refer to page 3-44 of “PL330 TRM”.	0xFFFF_FFFF
CR4	0xE090_0E10	R	Specifies the Configuration Register 4. For more information, refer to page 3-45 of “PL330 TRM”.	0xFFFF_FFFF
CRDn	0xE090_0E14	R	Specifies the Configuration Register Dn. For more information, refer to page 3-46 of “PL330 TRM”.	0x0077_3732
periph_id_n	0xE090_0FE0 - 0xE090_0FEC	R	Specifies the Peripheral Identification Registers 0-3. For more information, refer to page 3-48 of “PL330 TRM”.	Configuration-dependent
pcell_id_n	0xE090_0FF0 – 0xE090_0FFC	R	Specifies the PrimeCell Identification Registers 0-3. For more information refer to page 3-50 of PL330 TRM”	Configuration-dependent

The SFR description shows only the restricted and fixed part of some SFR. PL330 TRM shows detailed information of other parts and other SFRs.

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1.2.1.1 Channel Control Register for DMA_mem (CC, R)

- CC_0, R, Address = 0xFA20_0408
- CC_1, R, Address = 0xFA20_0428
- CC_2, R, Address = 0xFA20_0448
- CC_3, R, Address = 0xFA20_0468
- CC_4, R, Address = 0xFA20_0488
- CC_5, R, Address = 0xFA20_04A8
- CC_6, R, Address = 0xFA20_04C8
- CC_7, R, Address = 0xFA20_04E8

CCn	Bit	Description	Initial State
dst_burst_size	[17:15]	Programs the burst size that DMAC uses when it writes the destination data. b000 = 1 byte b001 = 2 bytes b010 = 4 bytes b011 = 8 bytes Other = Reserved	0
src_burst_size	[3:1]	Programs the burst size that DMAC uses when it reads the source data. b000 = 1 byte b001 = 2 bytes b010 = 4 bytes b011 = 8 bytes Other = Reserved	0

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1.2.1.2 Channel Control Register for DMA_PERI(0,1) (CC, R)

- CC_0, R, Address = 0xE090_0408, 0xE0A0_0408
- CC_1, R, Address = 0xE090_0428, 0xE0A0_0428
- CC_2, R, Address = 0xE090_0448, 0xE0A0_0448
- CC_3, R, Address = 0xE090_0468, 0xE0A0_0468
- CC_4, R, Address = 0xE090_0488, 0xE0A0_0488
- CC_5, R, Address = 0xE090_04A8, 0xE0A0_04A8
- CC_6, R, Address = 0xE090_04C8, 0xE0A0_04C8
- CC_7, R, Address = 0xE090_04E8, 0xE0A0_04E8

CCn	Bit	Description	Initial State
D st_burst_size	[17:15]	Programs the burst size that DMAC uses when it writes the destination data. b000 = 1 byte b001 = 2 bytes b010 = 4 bytes Other = Reserved	0
src_burst_size	[3:1]	Programs the burst size that DMAC uses when it reads the source data. b000 = 1 byte b001 = 2 bytes b010 = 4 bytes Other = Reserved	0

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1.2.1.3 Configuration Register0 for DMA_PERI(0,1) (CR0, R)

- CR0 for DMA_PERI0, R, Address = 0xE090_0E00
- CR0 for DMA_PERI1, R, Address = 0xE0A0_0E00

CR0	Bit	Description	Initial State
num_events	[21:17]	Specifies the number of interrupt outputs that the DMAC provides. b11111 = 32 interrupt outputs, irq[31:0]	0x1F
num_periph_req	[16:12]	Specifies the number of peripheral request interfaces that the DMAC provides. b11111 = 32 peripheral request interfaces	0x1F
num_chnls	[6:4]	Specifies the number of DMA channels that the DMAC supports. b111 = 8 DMA channels	0x7
mgr_ns_at_rst	[2]	Indicates the status of the boot_manager_ns signal when the DMAC exits from reset. 1 = boot_manager_ns was HIGH	1
boot_en	[1]	Indicates the status of the boot_from_pc signal when the DMAC exits from reset. 0 = boot_from_pc was LOW	0
periph_req	[0]	Indicates the peripheral request interface. 1 = DMAC provides the number of peripheral request interfaces that the num_periph_req field specifies.	1

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1.2.1.4 Configuration Register1 for DMA_PERI(0,1) (CR1, R)

- CR1 for DMA_PERI0, R, Address = 0xE090_0E04
- CR1 for DMA_PERI1, R, Address = 0xE0A0_0E04

CR1	Bit	Description	Initial State
num_i-cache_lines	[7:4]	The read value is always 7. It means DMA_PERI(0,1) has 8 i-cache lines.	0x7
i-cache_len	[2:0]	The read value is always 4. It means the length of an i-cache line is 16 bytes.	0x4

* PL330 contains a built-in instruction cache controller.

1.2.1.5 Configuration Register2 for DMA_PERI(0,1) (CR2, R)

- CR2 for DMA_PERI0, R, Address = 0xE090_0E08
- CR2 for DMA_PERI1, R, Address = 0xE0A0_0E08

CR2	Bit	Description	Initial State
boot_addr	[31:0]	Provides the value of boot_addr[31:0] when the DMAC exits from reset. 32'b0	0

* The first DMAC instruction fetch is to the address specified by DMA PC at reset value.

1.2.1.6 Configuration Register3 for DMA_PERI(0,1) (CR3, R)

- CR3 for DMA_PERI0, R, Address = 0xE090_0E0C
- CR3 for DMA_PERI1, R, Address = 0xE0A0_0E0C

CR3	Bit	Description	Initial State
INS	[31:0]	Specifies the security state of interrupt outputs. Bit [N] = 1: Assigns irq[N] to non-secure state. 32'hffff_ffff	0xFFFF_FFFF

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1.2.1.7 Configuration Register4 for DMA_PERI(0,1) (CR4, R)

- CR4 for DMA_PERI0, R, Address = 0xE090_0E10
- CR4 for DMA_PERI1, R, Address = 0xE0A0_0E10

CR4	Bit	Description	Initial State
PNS	[31:0]	Specifies the security state of peripheral request interfaces. Bit [N] = 1: Assigns peripheral request interface N to non-secure state. 32'hffff_ffff	0xFFFF_FFFF

1.2.1.8 Configuration Register DN for DMA_PERI(0,1) (CRdn, R)

- CRDn for DMA_PERI0, R, Address = 0xE090_0E14
- CRDn for DMA_PERI1, R, Address = 0xE0A0_0E14

CRDn	Bit	Description	Initial State
data_buffer_dep	[29:20]	Specifies the number of lines that data buffer contains. b000000111 = 8 lines	0x7
rd_q_dep	[19:16]	Specifies the depth of read queue. b0111 = 8 lines	0x7
rd_cap	[14:12]	Specifies the read issuing capability that programs the number of outstanding read transactions. b011 = 4	0x3
wr_q_dep	[11:8]	Specifies the depth of write queue. b0111 = 8 lines	0x7
wr_cap	[6:4]	Specifies the write issuing capability that programs the number of outstanding write transactions. b011 = 4	0x3
data_width	[2:0]	Specifies the data bus width of AXI interface. b010 = 32-bit	0x2

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1.2.1.9 Configuration Register0 for DMA_mem (CR0, R, Address = 0xFA20_0E00)

CR0	Bit	Description	Initial State
num_events	[21:17]	Specifies the number of interrupt outputs that the DMAC provides. b11111 = 32 interrupt outputs, irq[31:0]	0x1F
num_periph_req	[16:12]	Specifies the number of peripheral request interfaces that the DMAC provides. b00001 = 2 peripheral request interfaces	0x1
num_chnls	[6:4]	Specifies the number of DMA channels that the DMAC supports. b111 = 8 DMA channels	7
mgr_ns_at_rst	[2]	Indicates the status of boot_manager_ns signal when the DMAC exits from reset. 0 = boot_manager_ns is set to LOW	0
boot_en	[1]	Indicates the status of boot_from_pc signal when the DMAC exits from reset. 0 = boot_from_pc is set to LOW	0
periph_req	[0]	Supports peripheral requests. 1 = DMAC provides the number of peripheral request interfaces that num_periph_req field specifies.	1

1.2.1.10 Configuration Register1 for DMA_MEM (CR1, R, Address = 0xFA20_0E04)

CR1	Bit	Description	Initial State
num_i-cache_lines	[7:4]	Specifies the number of i-cache lines. b0111 = 8 i-cache lines.	0x7
i-cache_len	[2:0]	Specifies the length of an i-cache line. b101 = 32 bytese	0x5

* PL330 contains a built-in instruction cache controller.

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1.2.1.11 Configuration Register2 for DMA_MEM (CR2, R, Address = 0xFA20_0E08)

CR2	Bit	Description	Initial State
boot_addr	[31:0]	Specifies the value of boot_addr[31:0] when DMAC exits from reset. 32'b0	0

1.2.1.12 Configuration Register3 for DMA_MEM (CR3, R, Address = 0xFA20_0E0C)

CR3	Bit	Description	Initial State
INS	[31:0]	Specifies the security state of interrupt outputs. Bit [N] = 1: Assigns irq[N] to non-secure state. 32'hffff_ffff	0xFFFF_FFFF

1.2.1.13 Configuration Register4 for DMA_MEM (CR4, R, Address = 0xFA20_0E10)

CR4	Bit	Description	Initial State
PNS	[31:0]	Specifies the security state of peripheral request interfaces. Bit [N] = 1: Assigns peripheral request interface N to non-secure state. b11	0x3

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1.2.1.14 Configuration Register DN for DMA_MEM (CRdn, R, Address = 0xFA20_0E14)

CRDn	Bit	Description	Initial State
data_buffer_dep	[29:20]	Specifies the number of lines that the data buffer contains. b000011111 = 32 lines	0x1F
rd_q_dep	[19:16]	Specifies the depth of read queue. b0111 = 8 lines	0x7
rd_cap	[14:12]	Specifies the read issuing capability that programs the number of outstanding read transactions. b011 = 4	0x3
wr_q_dep	[11:8]	Specifies the depth of write queue. b0111 =8 lines	0x7
wr_cap	[6:4]	Specifies the write issuing capability that programs the number of outstanding write transactions. b011 = 4	0x3
data_width	[2:0]	Specifies the data bus width of AXI interface. b011 = 64-bit	0x3

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1.3 INSTRUCTION

Table 1-5 Instruction Syntax Summary

Mnemonic	Instruction	Thread usage: M = DMA manager C = DMA channel		Description
DMAADDH	Add Halfword	-	C	See DMAADDH on page 4-5 of “PL330 TRM”.
DMAEND	End	M	C	See DMAEND on page 4-5 of “PL330 TRM”.
DMAFLUSHP	Flush and notify Peripheral	-	C	See DMAFLUSHP on page 4-6 of “PL330 TRM”.
DMAGO	Go	M	-	See DMAGO on page 4-6 of “PL330 TRM”.
DMALD	Load	-	C	See DMALD[S|B] on page 4-8 of “PL330 TRM”.
DMALDP	Load Peripheral	-	C	See DMALDP<S|B> on page 4-9 of “PL330 TRM”.
DMALP	Loop	-	C	See DMALP on page 4-10 of “PL330 TRM”.
DMALPEND	Loop End	-	C	See DMALPEND[S|B] on page 4-11 of “PL330 TRM”.
DMALPFE	Loop Forever	-	C	See DMALPFE on page 4-13 of “PL330 TRM”.
DMAKILL	Kill	M	C	See DMAKILL on page 4-13 of “PL330 TRM”.
DMAMOV	Move	-	C	See DMAMOV on page 4-14 of “PL330 TRM”.
DMANOP	No operation	M	C	See DMANOP on page 4-16 of “PL330 TRM”.
DMARMB	Read Memory Barrier	-	C	See DMARMB on page 4-16 of “PL330 TRM”.
DMASEV	Send Event	M	C	See DMASEV on page 4-17 of “PL330 TRM”.
DMAST	Store	-	C	See DMAST[S|B] on page 4-17 of “PL330 TRM”.
DMASTP	Store and notify Peripheral	-	C	See DMASTP<S|B> on page 4-19 of “PL330 TRM”.
DMASTZ	Store Zero	-	C	See DMASTZ on page 4-20 of “PL330 TRM”.
DMAWFE	Wait For Event	M	C	See DMAWFE on page 4-20 of “PL330 TRM”.
DMAWFP	Wait For Peripheral	-	C	See DMAWFP<S|B|P> on page 4-21 of “PL330 TRM”.
DMAWMB	Write Memory Barrier	-	C	See DMAWMB on page 4-22 of “PL330 TRM”.

Each PL330 has a manager thread and eight channel threads. A manager thread controls the overall operation of DMAC, including initiating and killing channel. The channel thread operates the DMA.

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1.3.1 KEY INSTRUCTION

To run the channel thread, you must write assembly code.

The description of key instruction is listed below. For full instruction set, refer to Chapter 4, “PL330 TRM”.

1.3.1.1 DMAMOV

“Move” instructs the DMAC to move 32-bits immediately into Source Address REG (SAR), Destination Address REG (DAR), and Channel Control REG (CCR).

SAR

- A. Example: DMAMOV SAR, 0x24000000
  - 0x2400_0000 is the source address of DMA operation.

DAR

- A. Example: DMAMOV DAR, 0x24001000
  - 0x2400_1000 is destination address of DMA operation.

CCR

- A. Example: DMAMOV CCR, SB2 SS32 SP0 DB2 DS32 DP0
  - Source: Burst length is 2, 32-bit data width.
  - Destination: Burst length is 2, 32-bit data width.
  - SP0 and DP0 mean normal and secure respectively. SP2 and DP2 means normal and non-secure respectively
- B. Refer to pages 4-25~4-26 in Chapter 4, “PL330 TRM” to know about the exact DMA setting such as burst length, bit-width, address increment, and so on.

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1.3.1.2 DMALD, DMALDP

“Load” instructs the DMAC to perform DMA load using AXI transactions specified by SAR and CCR. For example, if you define CCR as 32-bit and burst length as 2, the DMALD generates a bus transaction of 32-bit and burst length 2. DMALDP notifies the peripheral when the data transfer is complete.

1.3.1.3 DMAST, DMASTP

“Store” instructs the DMAC to transfer data from FIFO to a location specified by DAR, using AXI transactions specified by DAR and CCR. For example, if you define CCR as 32-bit and burst length as 2, the DMAST generates a bus transaction of 32-bit and burst length 2. DMASTP notifies the peripheral when the data transfer is complete.

1.3.1.4 DMASTZ

“Store Zero” instructs the DMAC to store zeros using AXI transactions specified by DAR and CCR. For example, if you define CCR as 32-bit and burst length as 2, the DMASTZ generates a bus transaction of 32-bit and burst length 2 with zeros at data bus.

1.3.1.5 DMALP, DMALPEND

“DMALP lc0, 4 [code] ~ DMALPEND lc0” loops (iterates) the “[code]” 4 times. There are two loop counters, lc0 and lc1. You can use nested loop by two loop counters.

1.3.1.6 DMAWFP

This is used for peripheral DMA. “Wait for Peripheral” instructs the DMAC to stop the execution of thread until the specified peripheral signals a DMA request for that DMA channel.

1.3.1.7 DMAFLUSHP

This is used for peripheral DMA. "Flush Peripheral" clears the state in DMA that describes the contents of the peripheral. It also sends a message to the peripheral to resend its level status. This instruction asserts DMAACK. If you need DMAACK at a certain point, place this instruction to that point.

1.3.1.8 DMAEND

Instructs a channel to stop.

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1.3.2 USAGE MODEL

PL330 needs its own binary.

The usage model is described as follows:

1. Load DMA binary into memory.
2. Use DMA debug SFRs to start DMA controller, PL330.
   - A. Using debug SFRs
     - DBGCMD, DBGINST0, and DBGINST1 (all write-only)
     - Before writing the above three SFRs, check whether DBGSTATUS is busy or not.
     - For more information, refer to pages 3-37~3-40 in “PL330 TRM”.
   - B. DBGINST0 and DBGINST1 will contain debug instructions.
     - These SFRs can receive only three instructions, namely, DMAGO, DMASEV, and DMAKILL.
     - DMAGO starts a channel (For more information, refer to page number 3-38~3.40 and page number 4-6~4.8 in “PL330 TRM”).
   - C. DBGCMD executes the instruction stored in the DBGINST0 and SFRs.

Example:

```
; Load channel control register

; Single transfer, 32 bit/ non-secure

DMAMOV      CCR, SB1   SS32   SP2   DB1   DS32   DP2
      ; SB1, DB1          : Burst length: 1
      ; SS32, DS32        : 32-bit Data I/F
      ; SP0, DP0          : Secure access
      ; SP2, DP2          : Non-secure access

; in case of Peripheral transfer , should be Initialise peripheral

DMAFLUSHP 0

; Source: IntRAM0,     Destination: IntRAM1

DMAMOV     SAR, 0xd0020000
DMAMOV     DAR, 0xd0028000

DMALP   lc0, 32
DMALD
DMAST
DMALPEND lc0
DMASEV   E0
DMAEND
```

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1.3.2.1 Security Scheme

DMA_mem runs in both secure and non-secure modes, while DMA_peri runs only in non-secure mode.

1. Channel thread
   - A. DMA_mem: Runs in both secure (ns bit at DMAGO instruction is 0) and non-secure (ns bit at DMAGO instruction is 1) modes.
   - B. DMA_peri: Runs in non-secure (ns bit at DMAGO instruction is 1) mode only.

2. ASM code
   - A. For non-secure transaction,
     - Use SP2 and DP2 at DMAMOV instruction.
     - APROT[1] will be 1'b1.
   - B. For secure transaction,
     - Use SP0 and DP0 at DMAMOV instruction.
     - APROT[1] will be 1'b0.

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1.3.2.2 Interrupts

DMAC provides IRQ signals for use as level sensitive interrupts to external CPUs. If you program the Interrupt Enable Register to generate an interrupt after DMAC executes DMASEV, it sets the corresponding IRQ as high.

You can clear the interrupt by writing to the Interrupt Clear Register.

To control the interrupt, follow these steps:

1. Set up the Interrupt Enable Register to generate interrupts.
   - The interrupt enable register is a 32-bit register. Each bit of the INTEN register checks whether the DMAC signals an interrupt using the corresponding IRQ.
   - Program the appropriate bit to control the DMAC response on execution of DMASEV.
     - Bit [N] = 0: If executing DMASEV for event N, then the DMAC signals event N to all the threads.
     - Bit [N] = 1 If executing DMASEV for event N, then the DMAC sets irq[N] as HIGH.

2. To set the corresponding IRQ HIGH by executing DMASEV, program assembly code.
   - Use DMASEV instruction means an interrupt using one of the IRQ outputs.

3. Clear the interrupt by writing to the Interrupt Clear Register.
   - Each bit in the INTCLR register controls the clearing of an interrupt.
   - Program to control the clearing of the IRQ outputs:
     - Bit [N] = 0: The status of irq[N] does not change. Bit [N] = 1: The DMAC sets irq[N] as low.
     - If DMA is set to fault status, an interrupt occurs.

1.3.2.3 Summary

1. You can configure the DMAC with up to eight DMA channels, with each channel being capable of supporting a single concurrent thread of DMA operation. In addition, there is a single DMA manager thread to initialize the DMA channel thread.

2. Channel thread
   - A. Each channel thread can operate the DMA. You must write assembly code accordingly. If you need a number of independent DMA channels, you must write a number of assembly codes for each channel.
   - B. Assemble them, link them into one file, and load this file into memory.

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Section 7

TIMER

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1 PULSE WIDTH MODULATION TIMER

1.1 OVERVIEW OF PULSE WIDTH MODULATION TIMER

The S5PV210 has five 32-bit Pulse Width Modulation (PWM) timers. These timers generate internal interrupts for the ARM subsystem. In addition, Timers 0, 1, 2 and 3 include a PWM function, which drives an external I/O signal. The PWM in timer 0 has an optional dead-zone generator capability to support a large current device. Timer 4 is internal timers without output pins.

The Timers use the APB-PCLK as source clock. Timers 0 and 1 share a programmable 8-bit prescaler that provides the first level of division for the PCLK. Timers 2, 3, and 4 share a different 8-bit prescaler. Each timer has its own private clock-divider that provides a second level of clock division (prescaler divided by 2, 4, 8, or 16). Alternatively, the timers can select a clock source from CMU. Timers 0, 1, 2, 3, and 4 select SCLK_PWM.

Each timer has its own 32-bit down-counter which is driven by the timer clock. The down-counter is initially loaded from the Timer Count Buffer register (TCNTBn). If the down-counter reaches zero, the timer interrupt request is generated to inform the CPU that the timer operation is complete. If the timer down-counter reaches zero, the value of corresponding TCNTBn automatically reloads into the down-counter to start a next cycle. However, if the timer stops, for example, by clearing the timer enable bit of TCONn during the timer running mode, the value of TCNTBn is not reloaded into the counter.

The PWM function uses the value of the TCMPBn register. The timer control logic changes the output level if down-counter value matches the value of the compare register in timer control logic. Therefore, the compare register determines the turn-on time (or turn-off time) of a PWM output.

The TCNTBn and TCMPBn registers are double buffered to allow the timer parameters to be updated in the middle of a cycle. The new values do not take effect until the current timer cycle completes.

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The *Figure 1-1* shows a simple example of a PWM cycle.

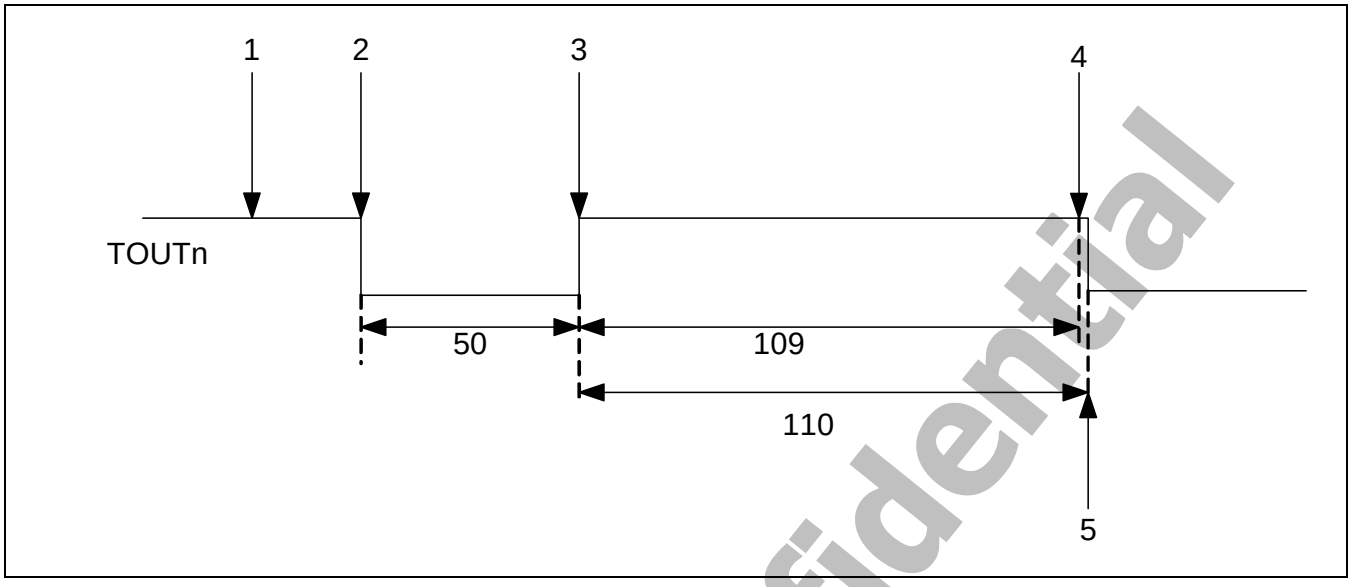

Figure 1-1 Simple Example of a PWM Cycle

Steps in PWM cycle:

- Initialize the TCNTBn register with 159(50+109) and TCMPBn with 109.
- Start Timer: Set the start bit and manually update this bit to off.
  The TCNTBn value of 159 is loaded into the down-counter, and then the output TOUTn is set to low.
- If down-counter counts down the value from TCNTBn to value in the TCMPBn register 109, the output changes from low to high
- If the down-counter reaches 0, it generates an interrupt request.
- The down-counter automatically reloads TCNTBn. This restarts the cycle.

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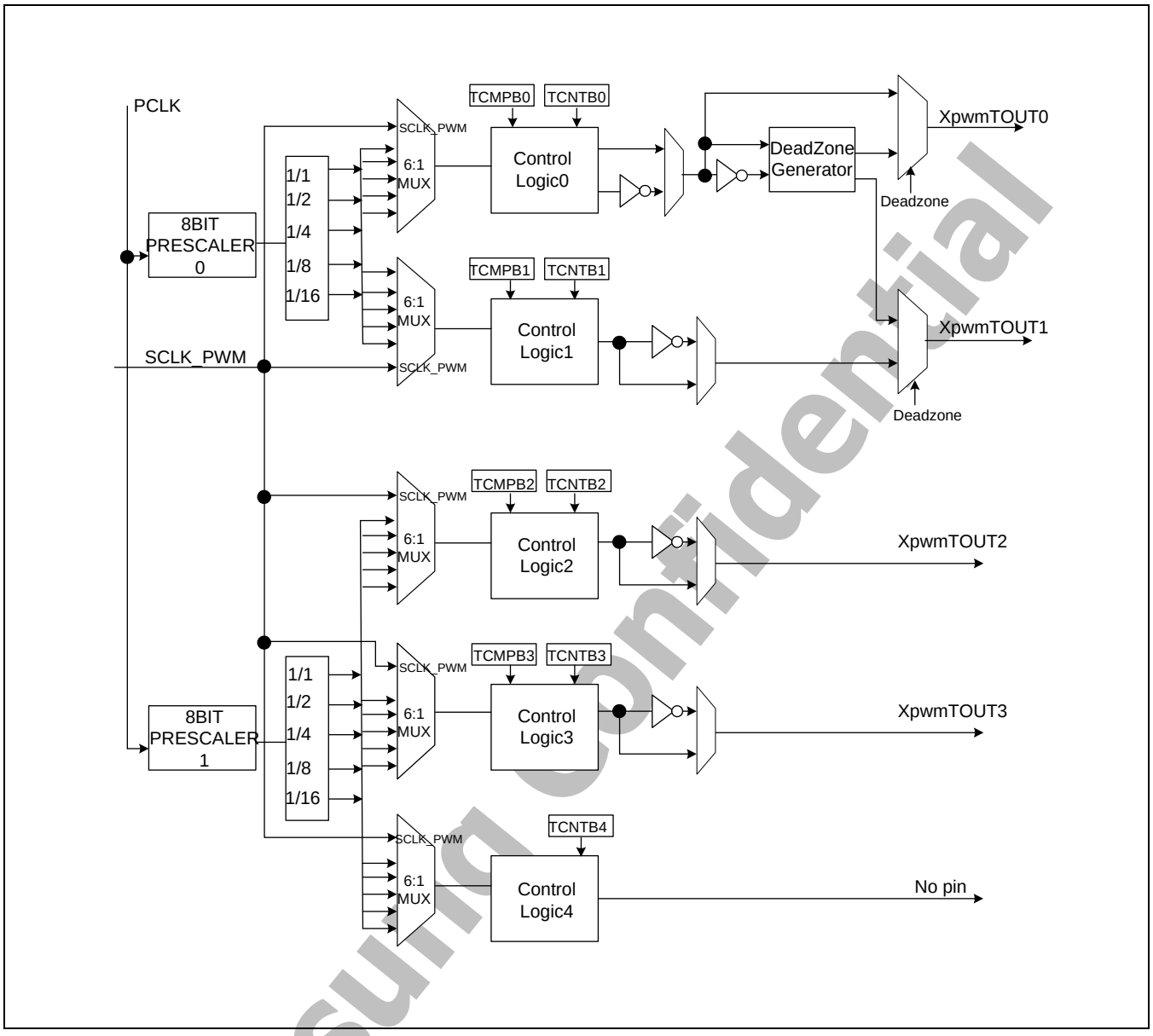

Figure 1-2 PWM TIMER Clock Tree Diagram

The *Figure 1-2* shows the clock generation scheme for individual PWM Channels.

Each timer can generate level interrupts.

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1.2 KEY FEATURES OF PULSE WIDTH MODULATION TIMER

The Features supported by the PWM include:

- Five 32-bit Timers.
- Two 8-bit Clock Prescalers providing first level of division for the PCLK, and five Clock Dividers and Multiplexers providing second level of division for the Prescaler clock and SCLK_PWM
- Programmable Clock Select Logic for individual PWM Channels.
- Four Independent PWM Channels with Programmable Duty Control and Polarity.
- Static Configuration: PWM is stopped
- Dynamic Configuration: PWM is running.
- Auto-Reload and One-Shot Pulse Mode.
- One external input to start the PWM.
- Dead Zone Generator on two PWM Outputs.
- Level Interrupt Generation.

The PWM has two operation modes, namely, Auto-Reload and One-Shot Pulse:

- Auto-Reload Mode
  In this mode, continuous PWM pulses are generated based on programmed duty cycle and polarity.
- One-Shot Pulse Mode
  In this mode, only one PWM pulse is generated based on programmed duty cycle and polarity.

To control the functionality of PWM, 18 special function registers are provided. The PWM is a programmable output, dual clock input AMBA slave module and connects to the Advanced Peripheral Bus (APB). These 18 special function registers within PWM are accessed via APB transactions.

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1.3 PWM OPERATION

1.3.1 PRESCALER AND DIVIDER

An 8-bit prescaler and 3-bit divider generates the following output frequencies:

Table 1-1 Minimum and Maximum Resolution based on Prescaler and Clock Divider Values

4-bit Divider Settings	Minimum Resolution (prescaler value=1)	Maximum Resolution (prescaler value=255)	Maximum Interval (TCNTBn=4294967295)
1/1(PCLK=66MHz)	0.030us(33.0MHz)	3.879us(257.8KHz)	16659.27s
1/2 (PCLK=66MHz)	0.061us (16.5MHz)	7.758us (128.9KHz)	33318.53s
1/4 (PCLK=66MHz)	0.121us (8.25MHz)	15.515us (64.5KHz)	66637.07s
1/8 (PCLK=66MHz)	0.242us (4.13MHz)	31.03us (32.2KHz)	133274.14s
1/16 (PCLK=66MHz)	0.485us (2.06MHz)	62.061us (16.1KHz)	266548.27s

1.3.2 BASIC TIMER OPERATION

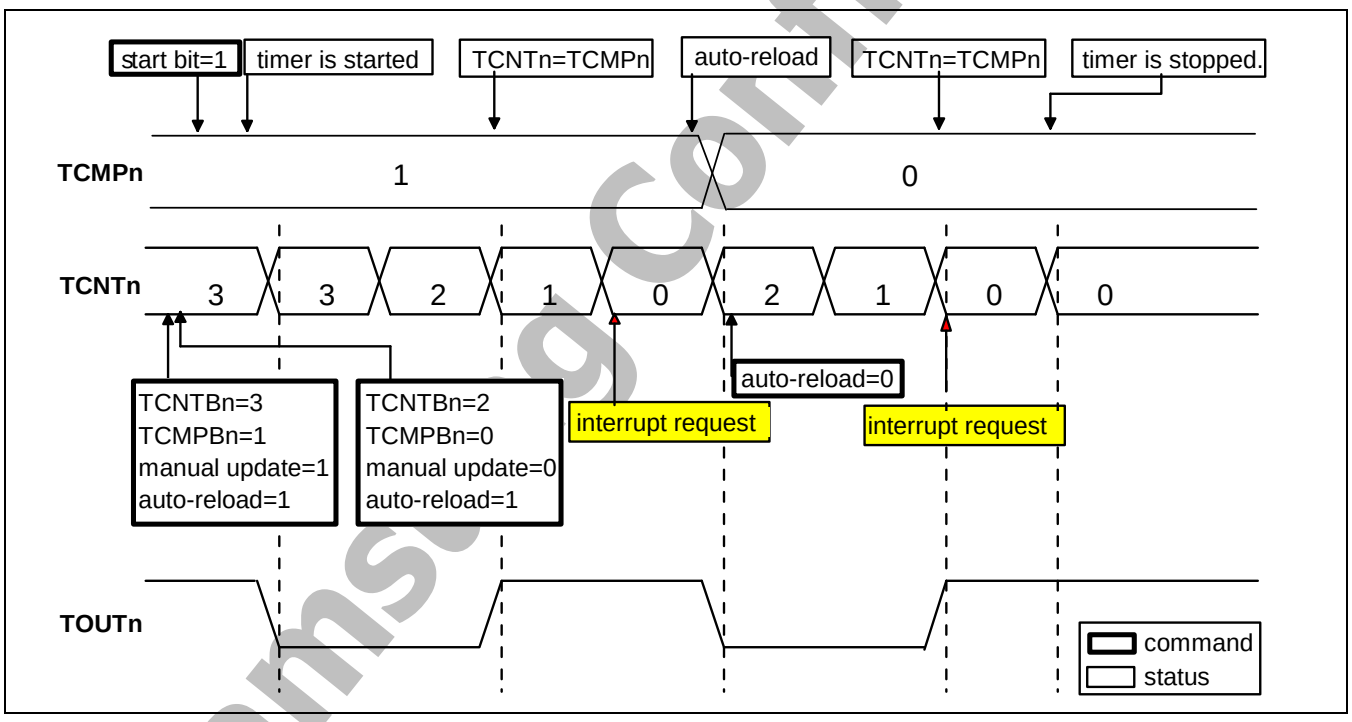

Figure 1-3 Timer Operations

The timer (except the timer channel 4) comprises of four registers, namely, TCNTBn, TCNTn, TCMPBn and TCMPn. If the timer reaches 0, then TCNTBn and TCMPBn registers are loaded into TCNTn and TCMPn. If TCNTn reaches 0, then the interrupt request occurs if the interrupt is enabled (TCNTn and TCMPn are the names of the internal registers. The TCNTn register is read from the TCNTOn register).

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To generate interrupt at intervals 3cycle of XpwmTOUTn, set TCNTBn, TCMPBn and TCON register as shown in *Figure 1-3*.

Steps to generate interrupt:

1. Set TCNTBn=3 and TCMPBn=1.
2. Set auto-reload=1 and manual update=1.
   If manual update bit is 1, then TCNTBn and TCMPBn values are loaded to TCNTn and TCMPn.
3. Set TCNTBn=2 and TCMPBn=0 for the next operation. 4. Set auto-reload=1 and manual update=0.
   If you set manual update=1 at this time, TCNTn is changed to 2 and TCMP is changed to 0.
   Therefore, interrupt is generated at interval two-cycle instead of three-cycle.
   You must set auto-reload=1 automatically for the next operation.
5. Set start = 1 for starting the operation. Then TCNTn is down counting.
   If TCNTn is 0, interrupt is generated and if auto-reload is enable, TCNTn is loaded 2 (TCNTBn value) and TCMPn is loaded 0 (TCMPn value).
6. TCNTn is down counting before it stops.

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1.3.3 AUTO-RELOAD AND DOUBLE BUFFERING

The PWM Timers includes a double buffering feature, which changes the reload value for the next timer operation without stopping the current timer operation.

The timer value is written into TCNTBn (Timer Count Buffer register) and the current counter value of the timer is read from TCNTOn (Timer Count Observation register). If TCNTBn is read, the read value does not reflect the current state of the counter but the reload value for the next timer duration.

Auto-reload is the operation copies the TCNTBn into TCNTn, if TCNTn reaches 0. The value written to TCNTBn, is loaded to TCNTn if the TCNTn reaches to 0 and auto-reload is enabled. If the TCNTn is 0 and the auto-reload bit is 0, then TCNTn does not operate further.

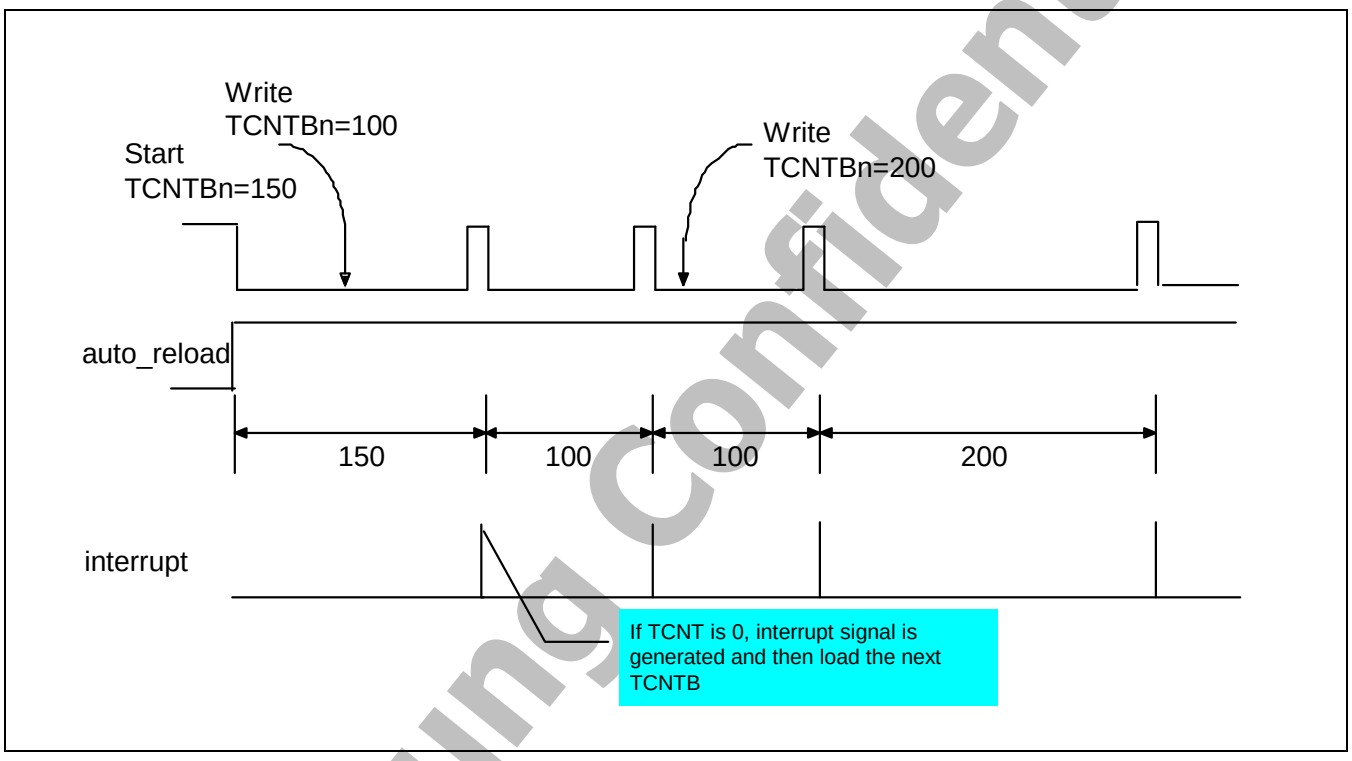

Figure 1-4 Example of Double Buffering Feature

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1.3.4 TIMER OPERATION EXAMPLE

Example of timer operation is shown in *Figure 1-5*.

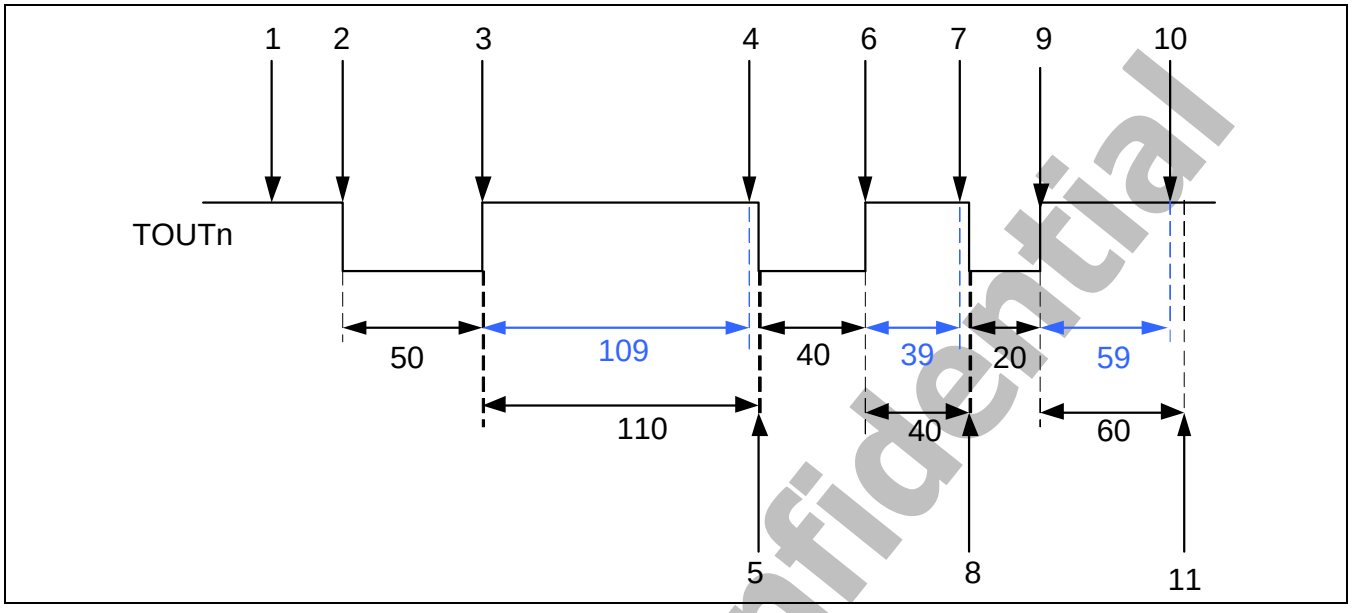

Figure 1-5 Example of a Timer Operation

Steps in timer operation:

1. Enable the auto-reload feature. Set the TCNTBn as 159(50+109) and TCMPBn as 109. Set the manual update bit on and set the manual update bit off. Set the inverter on/ off bit. The manual update bit sets TCNTn and TCMPn to the value of TCNTBn and TCMPBn.
2. Set TCNTBn and TCMPBn as 79(40+39) and 39.
3. Start Timer: Set the start bit in TCON
4. If TCNTn and TCMPn have the same value, the logic level of TOUTn is changed from low to high
5. When TCNTn reaches 0, it generates interrupt request.
6. TCNTn and TCMPn are automatically reloaded with TCNTBn and TCMPBn as (79(40+39)) and 39. In the Interrupt Service Routine (ISR), the TCNTBn and TCMPBn are set as 79(20+59) and 59.
7. If TCNTn and TCMPn have the same value, the logic level of TOUTn is changed from low to high
8. When TCNTn reaches to 0, it generates interrupt request.
9. TCNTn and TCMPn are automatically reloaded with TCNTBn, TCMPBn as (79(20+59)) and 59. The, auto-reload and interrupt request are disabled to stop the timer in the ISR.
10. If TCNTn and TCMPn have the same value, the logic level of TOUTn is changed from low to high
11. Even if TCNTn reaches to 0, no interrupt request is generated.
12. TCNTn is not reloaded and the timer is stopped because auto-reload is disabled.

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1.3.5 INITIALIZE TIMER (SETTING MANUAL-UP DATA AND INVERTER)

User must define the starting value of the TCNTn, because an auto-reload operation of the timer occurs when the down counter reaches to 0. In this case, the starting value must be loaded by manual update bit. The sequence to start a timer is as follows:

1. Write the initial value into TCNTBn and TCMPBn.
2. Set the manual update bit and clear only manual update bit of the corresponding timer.

NOTE: It is recommended to set the inverter on/off bit (whether inverter is used or not).

3. Set the start bit of the corresponding timer to start the timer

1.3.6 PWM (PULSE WIDTH MODULATION)

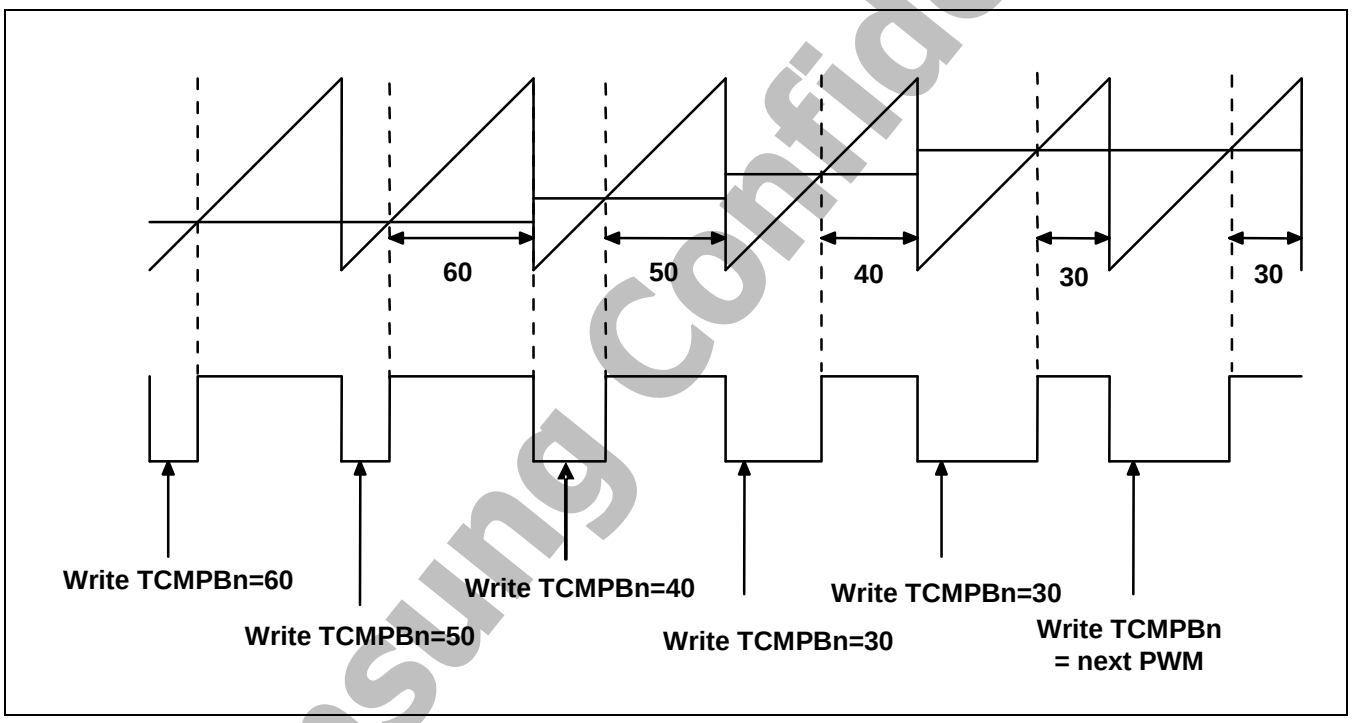

Figure 1-6 Example of PWM

Use TCMPBn to implement the PWM feature. PWM frequency is determined by TCNTBn. A PWM value is determined by TCMPBn as shown in the *Figure 1-6*.

For a higher PWM value, decrease the TCMPBn value. For a lower PWM value, increase the TCMPBn value. If the output inverter is enabled, the increment/ decrement can be opposite.

Due to the double buffering feature, TCMPBn, for a next PWM cycle is written by ISR at any point of current PWM cycle.

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1.3.7 OUTPUT LEVEL CONTROL

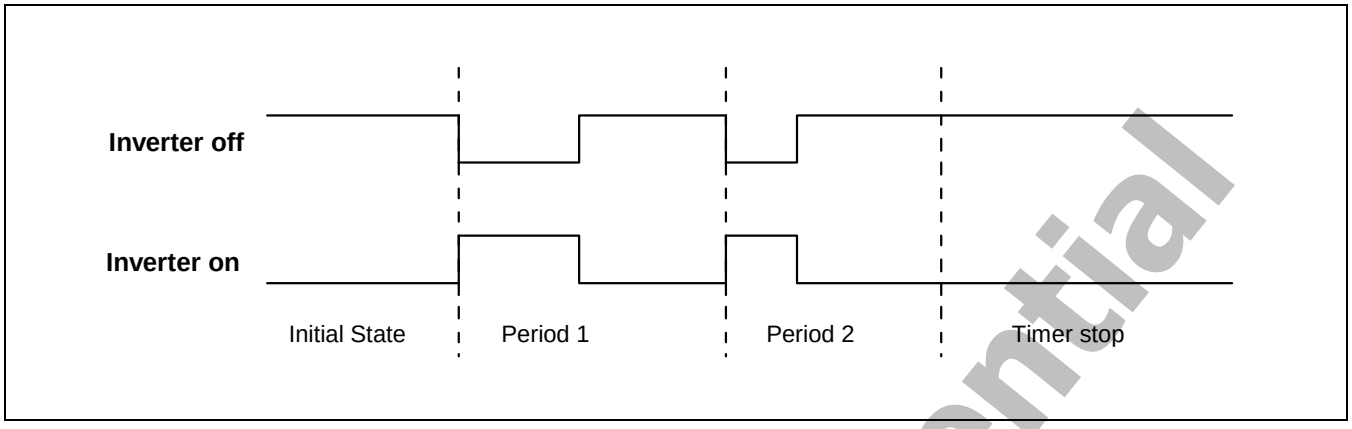

Figure 1-7 Inverter on/off

Steps to maintain TOUT as high or low (Assume that inverter is off).

1. Turn off the auto-reload bit. Then, TOUTn goes to high level and the timer is stopped after TCNTn reaches to 0. This method is recommended.
2. Stop the timer by clearing the timer start/ stop bit to 0. If TCNTn <= TCMPn, the output level is high. If TCNTn >TCMPn, the output level is low
3. TOUTn is inverted by the inverter on/ off bit in TCON. The inverter removes the additional circuit to adjust the output level.

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1.3.8 DEAD ZONE GENERATOR

This feature inserts the time gap between a turn-off and turn-on of two different switching devices. This time gap prohibits the two switching device turning on simultaneously even for a very short time.

TOUT_0 specifies the PWM output. nTOUT_0 specifies the inversion of the TOUT_0. If the dead-zone is enabled, the output wave-form of TOUT_0 and nTOUT_0 is TOUT_0_DZ and nTOUT_0_DZ. TOUT0_DZ and nTOUT_0_DZ cannot be turned on simultaneously by the dead zone interval. For functional correctness, the dead zone length must be set smaller than compare counter value.

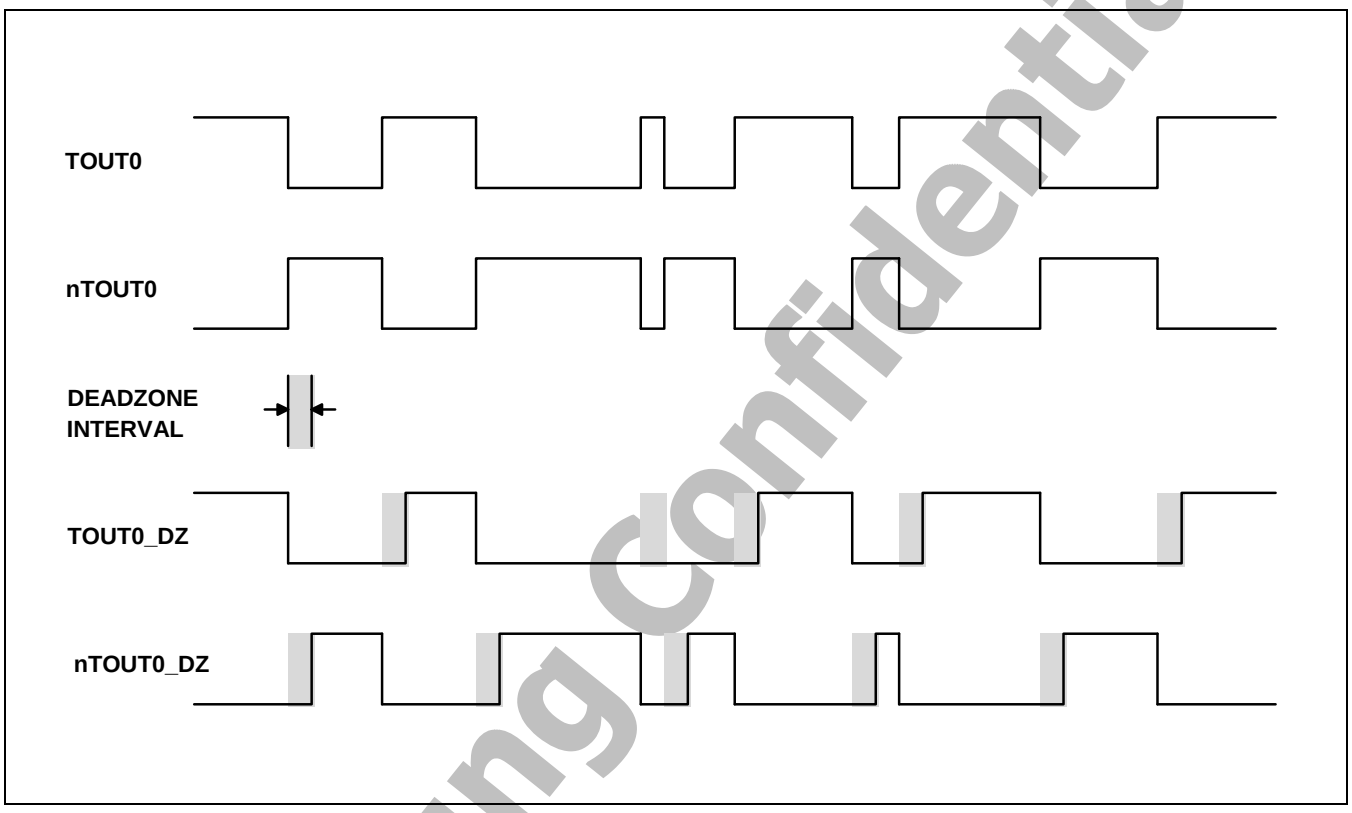

Figure 1-8 Waveform when a Deadzone Feature is Enabled

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1.4 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
TOUT_0	Output	PWMTIMER TOUT[0]	XpwmTOUT[0]	muxed
TOUT_1	Output	PWMTIMER TOUT[1]	XpwmTOUT[1]	muxed
TOUT_2	Output	PWMTIMER TOUT[2]	XpwmTOUT[2]	muxed
TOUT_3	Output	PWMTIMER TOUT[3]	XpwmTOUT[3]	muxed

NOTE: Type field indicates whether pads are dedicated to the signal or pads are connected to the multiplexed signals.

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1.5 REGISTER DESCRIPTION

1.5.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
TCFG0	0xE250_0000	R/W	Specifies the Timer Configuration Register 0 that configures the two 8-bit Prescaler and DeadZone Length	0x0000_0101
TCFG1	0xE250_0004	R/W	Specifies the Timer Configuration Register 1 that controls 5 MUX Select Bit	0x0000_0000
TCON	0xE250_0008	R/W	Specifies the Timer Control Register	0x0000_0000
TCNTB0	0xE250_000C	R/W	Specifies the Timer 0 Count Buffer Register	0x0000_0000
TCMPB0	0xE250_0010	R/W	Specifies the Timer 0 Compare Buffer Register	0x0000_0000
TCNTO0	0xE250_0014	R	Specifies the Timer 0 Count Observation Register	0x0000_0000
TCNTB1	0xE250_0018	R/W	Specifies the Timer 1 Count Buffer Register	0x0000_0000
TCMPB1	0xE250_001C	R/W	Specifies the Timer 1 Compare Buffer Register	0x0000_0000
TCNTO1	0xE250_0020	R	Specifies the Timer 1 Count Observation Register	0x0000_0000
TCNTB2	0xE250_0024	R/W	Specifies the Timer 2 Count Buffer Register	0x0000_0000
TCMPB2	0xE250_0028	R/W	Specifies the Timer 2 Compare Buffer Register	0x0000_0000
TCNTO2	0xE250_002C	R	Specifies the Timer 2 Count Observation Register	0x0000_0000
TCNTB3	0xE250_0030	R/W	Specifies the Timer 3 Count Buffer Register	0x0000_0000
TCMPB3	0xE250_0034	R/W	Specifies the Timer 3 Compare Buffer Register	0x0000_0000
TCNTO3	0xE250_0038	R	Specifies the Timer 3 Count Observation Register	0x0000_0000
TCNTB4	0xE250_003C	R/W	Specifies the Timer 4 Count Buffer Register	0x0000_0000
TCNTO4	0xE250_0040	R	Specifies the Timer 4 Count Observation Register	0x0000_0000
TINT_CSTAT	0xE250_0044	R/W	Specifies the Timer Interrupt Control and Status Register	0x0000_0000

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1.5.1.1 Timer Configuration Register (TCFG0, R/W, Address = 0xE250_0000)

Timer Input Clock Frequency = PCLK / ({prescaler value + 1}) / {divider value}
{prescaler value} = 1~255
{divider value} = 1, 2, 4, 8, 16, TCLK
Dead zone length = 0~254

TCFG0	Bit	Description	Initial State
Reserved	[31:24]	Reserved Bits	0x00
Dead zone length	[23:16]	Dead zone length	0x00
Prescaler 1	[15:8]	Prescaler 1 value for Timer 2, 3 and 4	0x01
Prescaler 0	[7:0]	Prescaler 0 value for timer 0 and 1	0x01

NOTE: If deadzone Length is set as ‘n’, Real Dead Zone Length is ‘n+1’ (n=0~254).

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1.5.1.2 Timer Configuration Register (TCFG1, R/W, Address = 0xE250_0004)

TCFG1	Bit	Description	Initial State
Reserved	[31:24]	Reserved Bits	0x00
Divider MUX4	[19:16]	Selects Mux input for PWM Timer 4 0000 = 1/1 0001 = 1/2 0010 = 1/4 0011 = 1/8 0100 = 1/16 0101 = SCLK_PWM	0x00
Divider MUX3	[15:12]	Selects Mux input for PWM Timer 3 0000 = 1/1 0001 = 1/2 0010 = 1/4 0011 = 1/8 0100 = 1/16 0101 = SCLK_PWM	0x00
Divider MUX2	[11:8]	Selects Mux input for PWM Timer 2 0000 = 1/1 0001 = 1/2 0010 = 1/4 0011 = 1/8 0100 = 1/16 0101 = SCLK_PWM	0x00
Divider MUX1	[7:4]	Selects Mux input for PWM Timer 1 0000 = 1/1 0001 = 1/2 0010 = 1/4 0011 = 1/8 0100 = 1/16 0101 = SCLK_PWM	0x00
Divider MUX0	[3:0]	Selects Mux input for PWM Timer 0 0000 = 1/1 0001 = 1/2 0010 = 1/4 0011 = 1/8 0100 = 1/16 0101 = SCLK_PWM	0x00

NOTE: If you use SCLK_PWM, duty of TOUT can show minimal error. SCLK_PWM is sampled by PCLK in PWM module.
But SCLK_PWM and PCLK is asynchronous clock. Therefore SCLK_PWM is not sampled at exact time. This minimal error can be reduced if SCLK_PWM is slower than PCLK. Therefore, it is recommended to use SCLK_PWM under 1MHz.
(For Example: If PCLK is 66MHz and SCLK_PWM is 1MHz, duty error is 1.5%. If PCLK is 66MHz and SCLK_PWM is 0.5MHz, duty error is 0.75%)

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1.5.1.3 Timer Control Register (CON, R/W, Address = 0xE250_0008)

TCON	Bit	Description	Initial State
Reserved	[31:23]	Reserved Bits	0x000
Timer 4 Auto Reload on/off	[22]	0 = One-Shot 1 = Interval Mode(Auto-Reload)	0x0
Timer 4 Manual Update	[21]	0 = No Operation 1 = Update TCNTB4	0x0
Timer 4 Start/Stop	[20]	0 = Stop 1 = Start Timer 4	0x0
Timer 3 Auto Reload on/off	[19]	0 = One-Shot 1 = Interval Mode(Auto-Reload)	0x0
Timer 3 Output Inverter on/off	[18]	0 = Inverter Off 1 = TOUT_3 Inverter-On	0x0
Timer 3 Manual Update	[17]	0 = No Operation 1 =Update TCNTB3	0x0
Timer 3 Start/Stop	[16]	0 = Stop 1 = Start Timer 3	0x0
Timer 2 Auto Reload on/off	[15]	0 = One-Shot 1 = Interval Mode(Auto-Reload)	0x0
Timer 2 Output Inverter on/off	[14]	0 = Inverter Off 1 = TOUT_2 Inverter-On	0x0
Timer 2 Manual Update	[13]	0 = No Operation 1 = Update TCNTB2,TCMPB2	0x0
Timer 2 Start/Stop	[12]	0 = Stop 1 = Start Timer 2	0x0
Timer 1 Auto Reload on/off	[11]	0 = One-Shot 1 = Interval Mode(Auto-Reload)	0x0
Timer 1 Output Inverter on/off	[10]	0 = Inverter Off 1 = TOUT_1 Inverter-On	0x0
Timer 1 Manual Update	[9]	0 = No Operation 1 = Update TCNTB1,TCMPB1	0x0
Timer 1 Start/Stop	[8]	0 = Stop 1 = Start Timer 1	0x0
Reserved	[7:5]	Reserved Bits	0x0
Dead Zone Enable/Disable	[4]	Dead Zone Generator Enable/Disable	0x0
Timer 0 Auto Reload on/off	[3]	0 = One-Shot 1 = Interval Mode(Auto-Reload)	0x0
Timer 0 Output Inverter on/off	[2]	0 = Inverter Off 1 = TOUT_0 Inverter-On	0x0
Timer 0 Manual Update	[1]	0 = No Operation 1 = Update TCNTB0,TCMPB0	0x0
Timer 0 Start/Stop	[0]	0 = Stop 1 = Start Timer 0	0x0

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1.5.1.4 Timer0 Counter Register (TCNTB0, R/W, Address = 0xE250_000C)

TCNTB0	Bit	Description	Initial State
Timer 0 Count Buffer	[31:0]	Timer 0 Count Buffer Register	0x0000_0000

1.5.1.5 Timer0 Compare Register (TCMPB0, R/W, Address = 0xE250_0010)

TCMPB0	Bit	Description	Initial State
Timer 0 Compare Buffer	[31:0]	Timer 0 Compare Buffer Register	0x0000_0000

1.5.1.6 Timer0 Observation Register (TCNTO0, R, Address = 0xE250_0014)

TCNTO0	Bit	Description	Initial State
Timer 0 Count Observation	[31:0]	Timer 0 Count Observation Register	0x0000_0000

1.5.1.7 Timer1 Counter Register (TCNTB1, R/W, Address = 0xE250_0018)

TCNTB1	Bit	Description	Initial State
Timer 1 Count Buffer	[31:0]	Timer 1 Count Buffer Register	0x0000_0000

1.5.1.8 Timer1 Compare Register (TCMPB1, R/W, Address = 0xE250_001C)

TCMPB1	Bit	Description	Initial State
Timer 1 Compare Buffer	[31:0]	Timer 1 Compare Buffer Register	0x0000_0000

1.5.1.9 Timer1 Observation Register (TCNTO1, R, Address = 0xE250_0020)

TCNTO1	Bit	Description	Initial State
Timer 1 Count Observation	[31:0]	Timer 1 Count Observation Register	0x0000_0000

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1.5.1.10 Timer2 Counter Register (TCNTB2, R/W, Address = 0xE250_0024)

TCNTB2	Bit	Description	Initial State
Timer 2 Count Buffer	[31:0]	Timer 2 Count Buffer Register	0x0000_0000

1.5.1.11 Timer2 Compare Register (TCMPB2, R/W, Address = 0xE250_0028)

TCMPB2	Bit	Description	Initial State
Timer 2 Compare Buffer	[31:0]	Timer 2 Compare Buffer Register	0x0000_0000

1.5.1.12 Timer2 Observation Register (TCNTO2, R, Address = 0xE250_002C)

TCNTO2	Bit	Description	Initial State
Timer 2 Count Observation	[31:0]	Timer 2 Count Observation Register	0x0000_0000

1.5.1.13 Timer3 Counter Register (TCNTB3, R/W, Address = 0xE250_0030)

TCNTB3	Bit	Description	Initial State
Timer 3 Count Buffer	[31:0]	Timer 3 Count Buffer Register	0x0000_0000

1.5.1.14 Timer2 Compare Register (TCMPB2, R/W, Address = 0xE250_0034)

TCMPB2	Bit	Description	Initial State
Timer 3 Compare Buffer	[31:0]	Timer 3 Compare Buffer Register	0x0000_0000

1.5.1.15 Timer3 Observation Register (TCNTO3, R, Address = 0xE250_0038)

TCNTO3	Bit	Description	Initial State
Timer 3 Count Observation	[31:0]	Timer 3 Count Observation Register	0x0000_0000

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1.5.1.16 Timer4 Counter Register (TCNTB4, R/W, Address = 0xE250_003C)

TCNTB4	Bit	Description	Initial State
Timer 4 Count Buffer	[31:0]	Timer 4 Count Buffer Register	0x0000_0000

1.5.1.17 Timer4 Observation Register (TCNTO4, R, Address = 0xE250_0040)

TCNTO4	Bit	Description	Initial State
Timer 4 Count Observation	[31:0]	Timer 4 Count Observation Register	0x0000_0000

1.5.1.18 Interrupt Control and Status Register (TINT_CSTAT, R/W, Address = 0xE250_0044)

TINT_CSTAT	Bit	Description	Initial State
Reserved	[31:10]	Reserved Bits	0x00000
Timer 4 Interrupt Status	[9]	Timer 4 Interrupt Status Bit. Clears by writing ‘1’ on this bit.	0x0
Timer 3 Interrupt Status	[8]	Timer 3 Interrupt Status Bit. Clears by writing ‘1’ on this bit.	0x0
Timer 2 Interrupt Status	[7]	Timer 2 Interrupt Status Bit. Clears by writing ‘1’ on this bit.	0x0
Timer 1 Interrupt Status	[6]	Timer 1 Interrupt Status Bit. Clears by writing `1’ on this bit.	0x0
Timer 0 Interrupt Status	[5]	Timer 0 Interrupt Status Bit. Clears by writing ‘1’ on this bit.	0x0
Timer 4 interrupt Enable	[4]	Enables Timer 4 Interrupt. 1 = Enabled 0 = Disabled	0x0
Timer 3 interrupt Enable	[3]	Enables Timer 3 Interrupt. 1 = Enables 0 = Disables	0x0
Timer 2 interrupt Enable	[2]	Enables Timer 2 Interrupt. 1 = Enables 0 = Disables	0x0
Timer 1 interrupt Enable	[1]	Enables Timer 1 Interrupt. 1 = Enables 0 = Disables	0x0
Timer 0 interrupt Enable	[0]	Enables Timer 0 Interrupt. 1 = Enables 0 = Disabled	0x0

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2 SYSTEM TIMER

2.1 OVERVIEW OF SYSTEM TIMER

System timer provides two distinctive features, namely:

It provides 1ms time tick at any power mode except sleep mode.

Changeable interrupt interval without stopping reference tick timer.

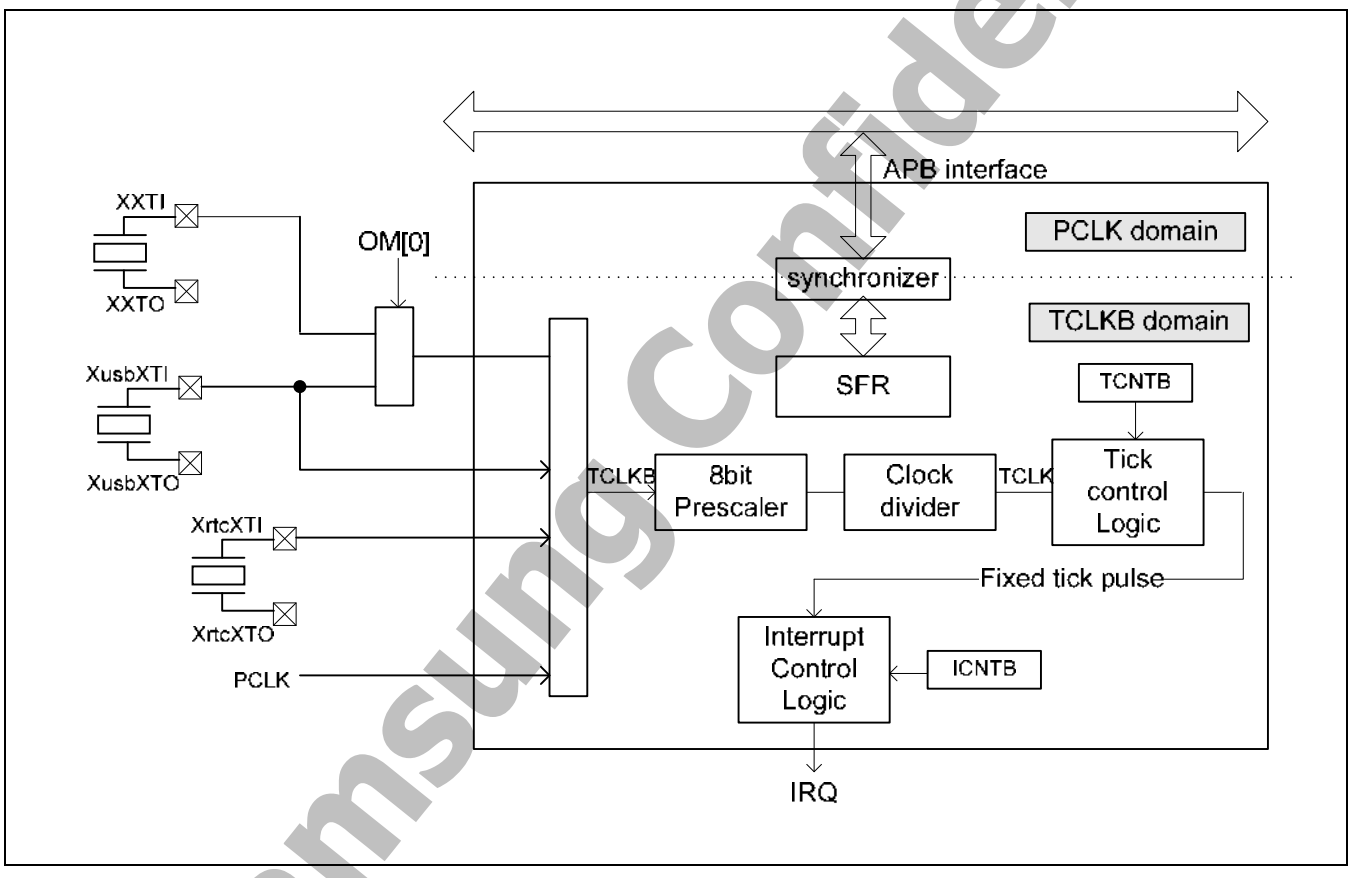

Figure 2-1 Overall System Timer Block Diagram

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2.2 KEY FEATURES OF SYSTEM TIMER

- Clock sources of ST such as, main OSC (XXTI), RTC OSC (XrtcXTI), USB OSC (XusbXTI), and PCLK
- Counter bit: 32-bit like PWM timer
- Changeable interrupt-interval without stopping reference tick
- Used in all power modes except sleep mode.
- Tick generation: fractional divider for 1ms tick generation with RTC clock frequency (32.768 kHz)

2.3 INTERNAL FUNCTION OF SYSTEM TIMER

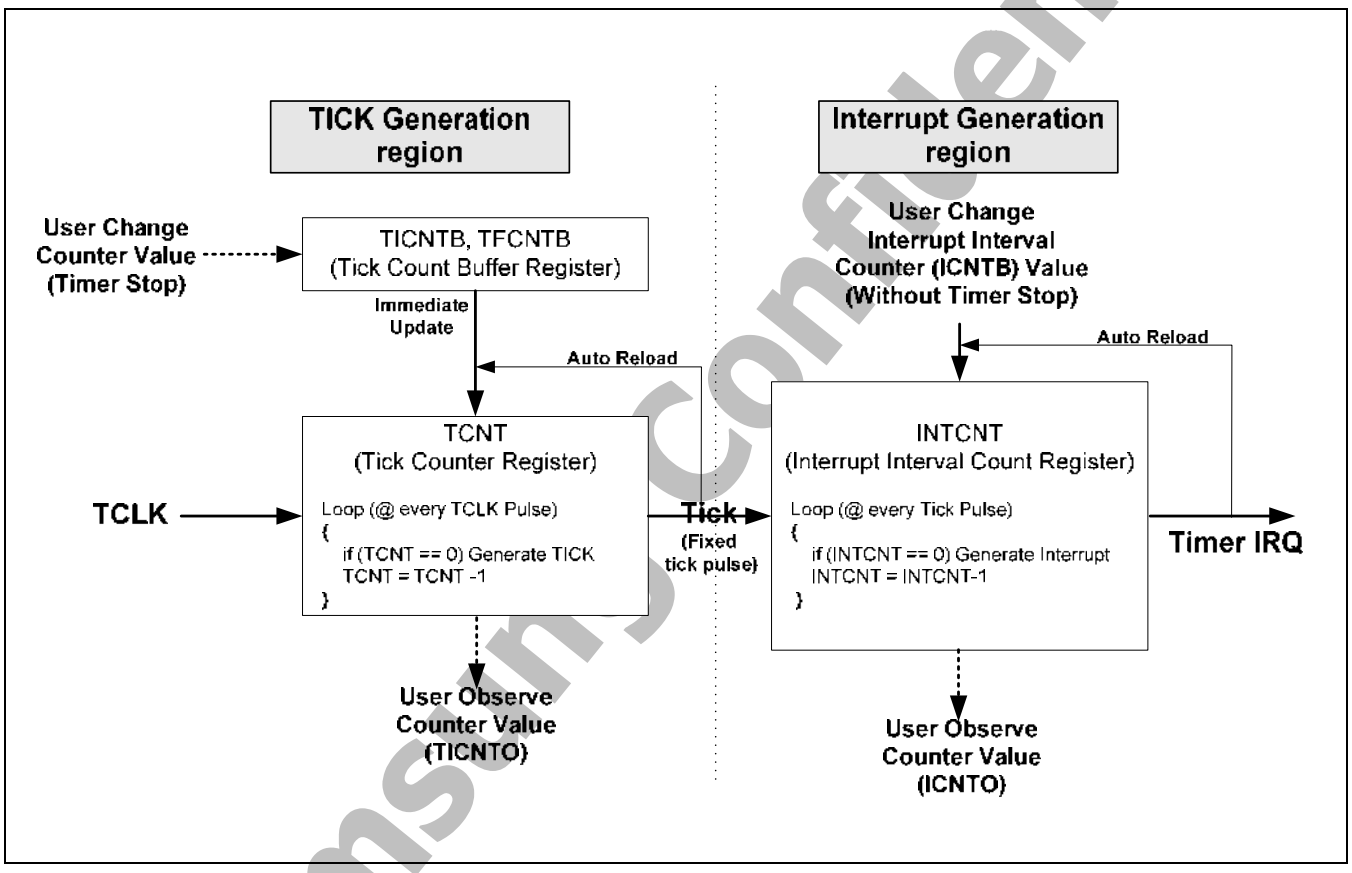

Figure 2-2 Two Separate Timers

There are two separate system timers in S5PV210. The first timer is used for tick generation, while the other is used for interrupt generation. Two independent SFR sets and logic blocks are used for tick and interrupt region. Each logic block operates separately. Therefore, you can change interrupt interval independent to reference tick generation. This is very useful feature for some power-saving modes.

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2.4 DETAILED OPERATION

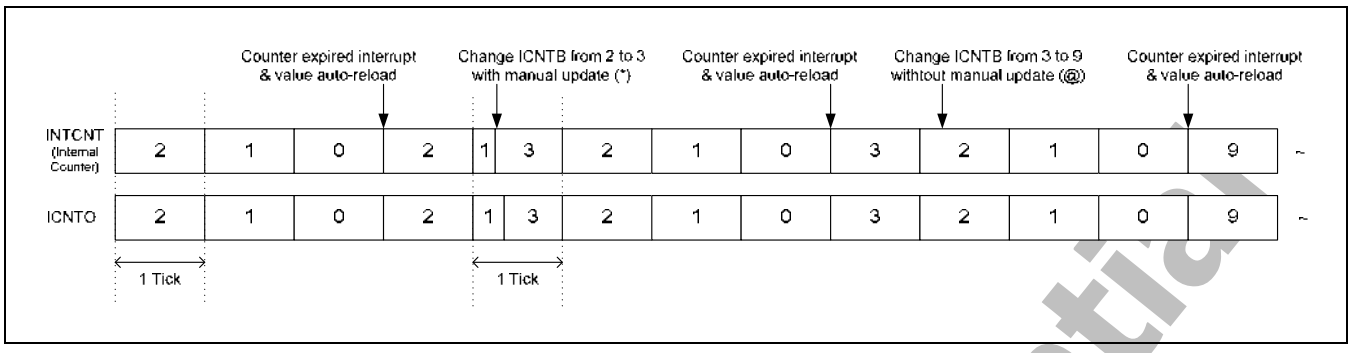

Figure 2-3 Timer Operation with Always on of Auto-reload

Usually, the tick interval is fixed after initial setting and you can change the interrupt interval at run-time. *Figure 2-3* shows the detailed operation of interrupt counter (INTCNT) and interrupt counter observation SFR (ICNTO) with auto-reload. Each rectangular block shows one tick time. Although the interrupt interval is changed, one tick time is fixed because tick and interrupt counter are independent of each other.
Interrupt is asserted when INTCNT value is expired (INTCNT=0). SW reads ICNTO to know elapsed time.

NOTE: As shown in *Figure 2-3* when ICNTB is changed with interrupt manual update (TCON[4] or ICNTB[31]), the new changed value is applied to interrupt counter (INTCNT) at that time. When ICNTB is changed without interrupt manual update (TCON[4] or ICNTB[31]) (@ at *Figure 2-3*), the new changed value is applied to INTCNT (interrupt counter) after interrupt counter expires. When auto reload is needed, write Interrupt Type (TCON[5]) as 1.

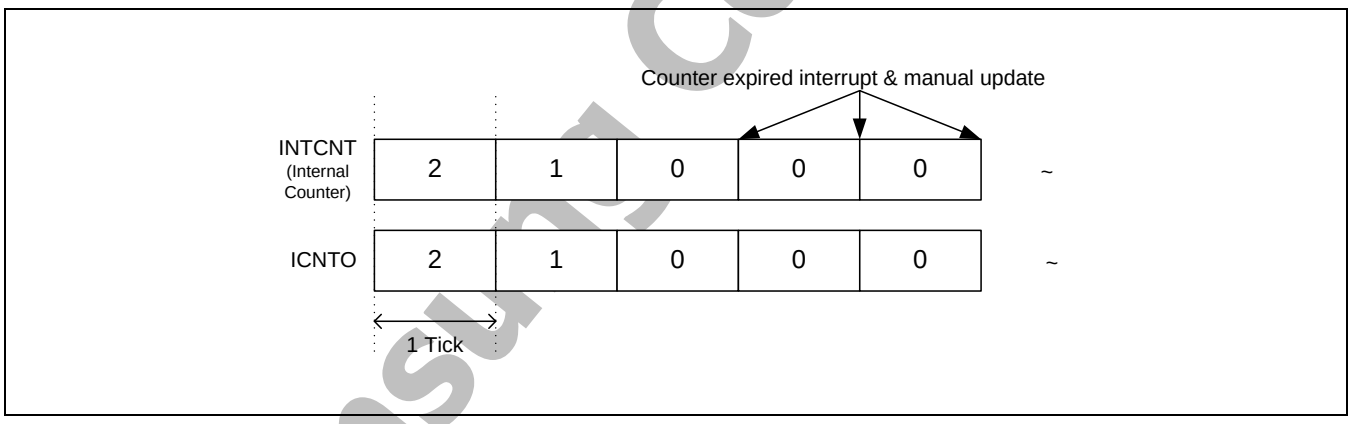

Figure 2-4 Timer Operation Without Auto Reload (One-shot mode)

When one-shot mode is needed, set the Interrupt Type (TCON[5]) as 0. After timer is expired, INTCNT (interrupt counter) is set as 0 and interrupt occurs at every TICK.

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2.5 TICK GENERATION WITH FRACTIONAL DIVIDER

System timer uses fractional divider to generate tick with any input clock. Especially, system timer can make approximate 1ms tick with RTC input clock (32.768 kHz).
The output clock from fractional divider can have local frequency error. If local frequency error is not important for some applications, you can use that output clock with low-power consumption.

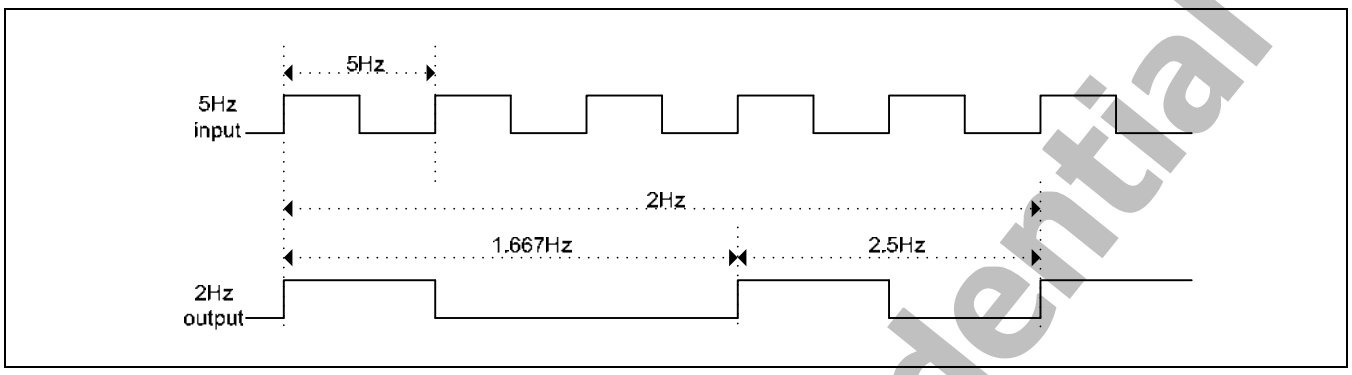

Figure 2-5 Approximate 5Hz tick with 2Hz input clock

Figure 2-5 shows a simple example describing theory of fractional divider. As shown in *Figure 2-5*, the fractional divider can generate any output clock with changing clock duty.
Although local frequency error exists (1.667Hz and 2.5Hz in this case), there is no global frequency error. If output clock frequency is much slower than input clock frequency, the instance of local frequency error decreases.

To configure fractional divider **divider mux and pre-scaler cannot be used for fractional divider. (write TCFG[10:0] as 0)**
Write TCFG[14] as 1.

1. General
   Write TCFG[15] as 0.

   Input frequency must be 4 times larger than target frequency.
   VALUE = **Frequency of TCLKB / 2 /** target frequency
   If VALUE is fractional number (a.b), write TICNTB as a-1, and TFCNTB as b*65536.
   For example, if you want to generate 2kHz output with 9kHz input, VALUE is 9 / 2 / 2 = 2.25. It means that a is 2 and b is 0.25. Write TICNTB as 1 (= 2 -1) and TFCNTB as 16384 (= 0.25*65536) in this case.

NOTE: If TFCNTB is not integer number, fractional divider inevitably generates timing error. SEC can give timing error table to determine whether you can use system timer or not for specific application.
If you require timing error table contact SEC.

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2. 1ms with RTC clock
   Write TCFG[15] as 1
   Write TICNTB as 15 and any value to TFCNTB.

Then you can get approximate 1ms tick. Although this tick has local error (frequency of one tick is 0.993 kHz or 1.024kHz, they are not 1ms tick), after 125 ticks, it represents exact 125ms passed. In other words, there is no accumulation error.

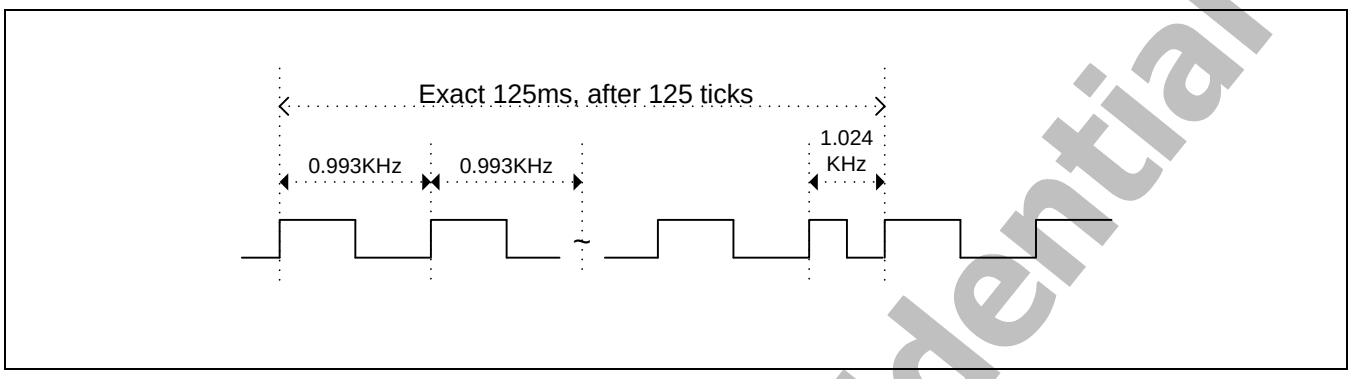

Figure 2-6 Approximate 1ms tick with RTC Clock Dedicated Fractional Divider

If you do not required to use fractional divider for making tick, method for writing TICNTB and TFCNTB is as follows:

- Write TCFG[14] as 0
- Write TICNTB as the value that you want to divide – 1

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2.6 USAGE MODEL

Follow the restrictions given below:

- TCLKB must be equal to or slower than PCLK.
- Set the count value as high as possible (To improve resolution).
- TCFG and tick interval must not be changed at run-time. If you want to change them, stop timers, do TICK SW reset (TCFG[16]) in advance and then change. TICK SW reset all logic in TICK generation region and TICNTO SFR.

2.6.1 COUNTER SETTING

1. TICNTB, and TFCNTB: refer "TICK GENERATION"
2. ICNTB: Interrupt Counter Value = ICNTB+1.

2.6.2 INTERRUPT

There are five kinds of interrupt sources in system timer. The first one is interrupt counter expired, and the other four are SFR write status.
When you write a value to TCON, TICNTB, TFCNTB, and ICNTB SFR, the value may not be immediately updated to system timer's internal counter, because sometimes the system timer uses RTC or XXTI clock for counter. These clocks are slower than PCLK, the operating clock of SFR. After the write status interrupts are asserted, the software can check whether the new value is really updated at the internal counter. SW must wait until that time. If you do not want to assert an interrupt, continuously read INT_CSTAT (polling method) to know update timing. In that case, you can selectively enable or disable each source of interrupt. For more information, refer INT_CSTAT[10:6] and INT_CSTAT[0].

2.6.3 COUNT VALUE UPDATE

When TFCNTB or TICNTB write interrupt are asserted after writing the counter value to TICNTB or TFCNTB, tick timer counter is updated.

Interrupt manual update (TCON[4] or ICNTB[31]) updates the interrupt timer at that time. As described in *Chapter 2.6.2* , after write status interrupt occurs, you can check whether internal counter is really updated.

The Interrupt Interval mode (TCON[5]) allows interrupt timer to update value in ICNTB automatically, after interrupt timer counter is expired.

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2.6.4 START TIMER

1. **Reset tick generation logic (by setting TCFG[16] as 1). And TCFG[16] is auto-cleared.**
2. Set TCFG SFR to make appropriate TCLK.
   A. Select clock source.
   B. Set pre-scaler and divider value.
3. Set tick counter by writing appropriate values to TICNTB and TFCNTB (if you use fractional divider) SFR.
4. Wait until TICNTB write interrupt occurs, and write 1 to INT_CSTAT[2] to clear interrupt status bit.
5. If you use fractional divider, additionally wait TFCNTB write interrupt occurs, and write 1 to INT_CSTAT[3] to clear interrupt status bit.
6. Set interrupt counter by writing to ICNTB SFR.
7. Wait until ICNTB write interrupt occurs, and write 1 to INT_CSTAT[4] to clear interrupt status bit.
8. Write (**TCON[4] = 1'b1 or ICNTB[31] = 1'b1**) **and TCON[0] = 1'b1** to update wanted value to internal interrupt counter at that time.
9. Wait until TCON write interrupt occurs, and write 1 to INT_CSTAT[5] to clear interrupt status bit.
10. **Write both TCON[3] = 1 to run interrupt and tick timer. And also set interrupt type by TCON[5] at this time.**
11. **Wait until TCON write interrupt occurs, and write 1 to INT_CSTAT[5] to clear interrupt status bit.**

2.6.5 STOP TIMER

1. Write INT_CSTAT[6] = 1'b0 to disable Interrupt counter expired (INTCNT=0) interrupt.
2. Write TCON[3] = 1'b0 to stop internal interrupt counter.
3. Write TCON[0] = 1'b0 To stop internal timer counter.

2.6.6 CHANGE INTERVAL INTERRUPT AT RUN-TIME

To run system timer as shown in *Figure 2-4.*

1. Set new interrupt counter value by writing to ICNTB SFR.
2. Wait until ICNTB write interrupt occurs, and write 1 to INT_CSTAT[4] to clear interrupt status bit.
3. Write TCON [4] = 1'b1 or ICNTB[31] = 1'b1 to update new value to internal interrupt counter at that time.
4. Wait until TCON write interrupt occurs, and write 1 to INT_CSTAT[5] to clear interrupt status bit.

And the new value is updated after interrupt counter is expired.

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2.7 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
XT_I & XT_O	In& Out	Oscillator pads for system clock	XXTI & XXTO	Dedicated
XT_RTC_I & XT_RTC_O	In& Out	Oscillator pads for RTC clock	XrtcXTI & XrtcXTO	Dedicated
XT_USB_I & XT_USB_O	I/O	Oscillator pads for USB clock	XusbXTI & XusbXTO	Dedicated

NOTE: Type field indicates whether pads are dedicated to the signal or pads are connected to the multiplexed signals.

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2.8 REGISTER DESCRIPTION

2.8.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
Software Interface and Registers				
TCFG	0xE260_0000	R/W	Specifies the Configures 8-bit-Prescaler and Clock MUX	0x0000_0000
TCON	0xE260_0004	R/W	Specifies the Timer Control Register	0x0000_0000
TICNTB	0xE260_0008	R/W	Specifies the Tick Integer Count Buffer Register	0x0000_0000
TICNTO	0xE260_000C	R	Specifies the Tick Integer Count Observation Register	0x0000_0000
TFCNTB	0xE260_0010	R/W	Specifies the Tick Fractional Count Buffer Register	0x0000_0000
-	0xE260_0014	-	Reserved	0x0000_0000
ICNTB	0xE260_0018	R/W	Specifies the Interrupt Count Buffer Register	0x0000_0000
ICNTO	0xE260_001C	R	Specifies the Interrupt Count Observation Register	0x0000_0000
INT_CSTAT	0xE260_0020	R/W	Specifies the Clears Interrupt	0x0000_0000

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2.8.1.1 Timer Configuration Register (TCFG, R/W, Address = 0xE260_0000)

Timer Input Clock Frequency = TCLKB / ({prescaler value + 1}) / {divider value}
{prescaler value} = 1~255 / {divider value} = 1, 2, 4, 8, 16

TCFG	Bit	Description	Initial State
Reserved	[31:17]	Reserved	0x0
TICK_SWRST	[16]	SW reset of TICK generation logic and TICNTO SFR Before re-setting TICK generation logic, write 1 to just this bit. After reset, this bit is auto-cleared.	0x0
FDIV SEL	[15]	Fractional divider select 0 = General 1 = RTC clock-dedicated to make 1ms This bit is only available when system timer uses fractional divider for TICKGEN (TCFG[14]=1).	0x0
TICKGEN SEL	[14]	0 = Integer divider 1 = Fractional divider When integer divider is used, don't care TCFG[15] and TFCNTB.	0x0
TCLKB MUX	[13:12]	Selects clock input for TCLKB 00 = System Main Clock(XXTI or XUSB, depends on OM[0] pin) 01 = XrtcXTI 10 = XusbXTI 11 = P(APB)CLK Usable clock source is restricted by power mode & oscillator pad configuration. XrtcXTI for any power mode and oscillator pad configuration. XXTI & XusbXTI are used for any power mode by turning on OSCs (XXTI and XusbXTI) PCLK is used just normal and idle mode For more information, refer to Power Management Unit user's manual.	0x0
Divider MUX	[10:8]	Selects Mux input for Timer 000 = 1 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16	0x0
Prescaler	[7:0]	Prescaler value for timer	0x00

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2.8.1.2 Timer Control Register (TCON, R/W, Address = 0xE260_0004)

TCON	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0x0
Interrupt Type	[5]	0 = One-shot mode 1 = Interval mode(auto-reload)	0x0
Interrupt Manual Update	[4]	0 = No operation 1 = Update ICNTB This bit is auto-cleared.	0x0
Interrupt Start / Stop	[3]	0 = Stop 1 = Start timer	0x0
Reserved	[2]	Reserved	0x0
Reserved	[1]	Reserved	0x0
Timer Start / Stop	[0]	0 = Stop 1 = Start timer	0x0

If you want to use the One-shot mode for interrupt, set TCON[5] as 0. In that case, the interrupt occurs at every TICK after interrupt counter reaches zero.

If you want to use interval mode for interrupt, set TCON[5] as 1. In that case, the value in ICNTB is automatically reloaded to INTCNT counter when INTCNT expires.

2.8.1.3 TICK Integer Counter Register (TICNTB, R/W, Address = 0xE260_0008)

Real Timer Counter Value = TICNTB+1, Do not use 0 for TICNTB

TICNTB	Bit	Description	Initial State
Tick Integer Count Buffer	[31:0]	Tick Integer Count Buffer Register	0x0

2.8.1.4 TICK Integer Observation Register (TICNTO, R, Address = 0xE260_000C)

TICNTO	Bit	Description	Initial State
Tick Integer Count Observation	[31:0]	Tick Integer Count Observation Register	0x0

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2.8.1.5 TICK Fractional Counter Register (TFCNTB, R/W, Address = 0xE260_0010)

TFCNTB	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0
Tick Fractional Count Buffer	[15:0]	Tick Fractional Count Buffer Register	0x0

2.8.1.6 Interrupt Counter Register (ICNTB, R/W, Address = 0xE260_0018)

Real Interrupt Counter Value = ICNTB+1.
If ICNTB value is 0, interrupt occurs at every TICK.

ICNTB	Bit	Description	Initial State
Interrupt Manual Update	[31]	0 = No operation 1 = Update ICNTB This bit is auto-cleared.	0x0
Interrupt Count Buffer	[30:0]	Interrupt Count Buffer Register	0x0

2.8.1.7 Interrupt Observation Register (ICNTO, R, Address = 0xE260_001C)

ICNTO	Bit	Description	Initial State
Reserved	[31]	Reserved	0x0
Interrupt Count Observation	[30:0]	Interrupt Count Observation Register	0x0

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2.8.1.8 Interrupt Control and Status Register (INT_CSTAT, R/W, Address = 0xE260_0020)

INT_CSTAT	Bit	Description	Initial State
Reserved	[31:11]	Reserved	0x0
TWIE	[10]	TCON Write Interrupt Enable 0 = Disable 1 = Enable	0x0
IWIE	[9]	ICNTB write Interrupt Enable 0 = Disable 1 = Enable	0x0
TFWIE	[8]	TFCNTB write Interrupt Enable 0 = Disable 1 = Enable	0x0
TIWIE	[7]	TICNTB write Interrupt Enable 0 = Disable 1 = Enable	0x0
ICNTEIE	[6]	Interrupt counter expired (INTCNT=0) Interrupt Enable. 0 = Disable 1 = Enable	0x0
TCON Write Status	[5]	TCON Write Interrupt Status Bit. After user writes value to TCON, this bit is asserted. Clear by writing '1' on this bit.	0x0
ICNTB Write Status	[4]	ICNTB Write Interrupt Status Bit. After user writes value to ICNTB, this bit is asserted. Clear by writing '1' on this bit.	0x0
TFCNTB Write Status	[3]	TFCTNB Write Interrupt Status Bit. After user writes value to TFCNTB, this bit is asserted. Clear by writing '1' on this bit.	0x0
TICNTB Write Status	[2]	TICTNB Write Interrupt Status Bit. After user writes value to TICNTB, this bit is asserted. Clear by writing '1' on this bit.	0x0
INTCNT counter expired Status	[1]	Interrupt counter expired (INTCNT=0) Interrupt Status Bit. When timer interrupt is occurred, this bit is asserted. Clear by writing '1' on this bit.	0x0
Interrupt Enable	[0]	Enables Interrupt. 1 = Enable 0 = Disable	0x0

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3 WATCHDOG TIMER

3.1 OVERVIEW OF WATCHDOG TIMER

The Watchdog Timer (WDT) in S5PV210 is a timing device that resumes the controller operation after malfunctioning due to noise and system errors. WDT can be used as a normal 16-bit interval timer to request interrupt service. The WDT generates the reset signal.

The difference between WDT and PWM timer is that WDT generates the reset signal.

3.2 KEY FEATURES OF WATCHDOG TIMER

- Supports Normal interval timer mode with interrupt request
- Activates Internal reset signal if the timer count value reaches 0 (Time-out).
- Supports Level-triggered Interrupt mechanism

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3.3 FUNCTIONAL DESCRIPTION OF WATCHDOG TIMER

3.3.1 WATCHDOG TIMER OPERATION

Figure 3-1 shows the functional block diagram of the watchdog timer. The watchdog timer uses PCLK as its source clock. The PCLK frequency is prescaled to generate the corresponding watchdog timer clock, and the resulting frequency is divided again.

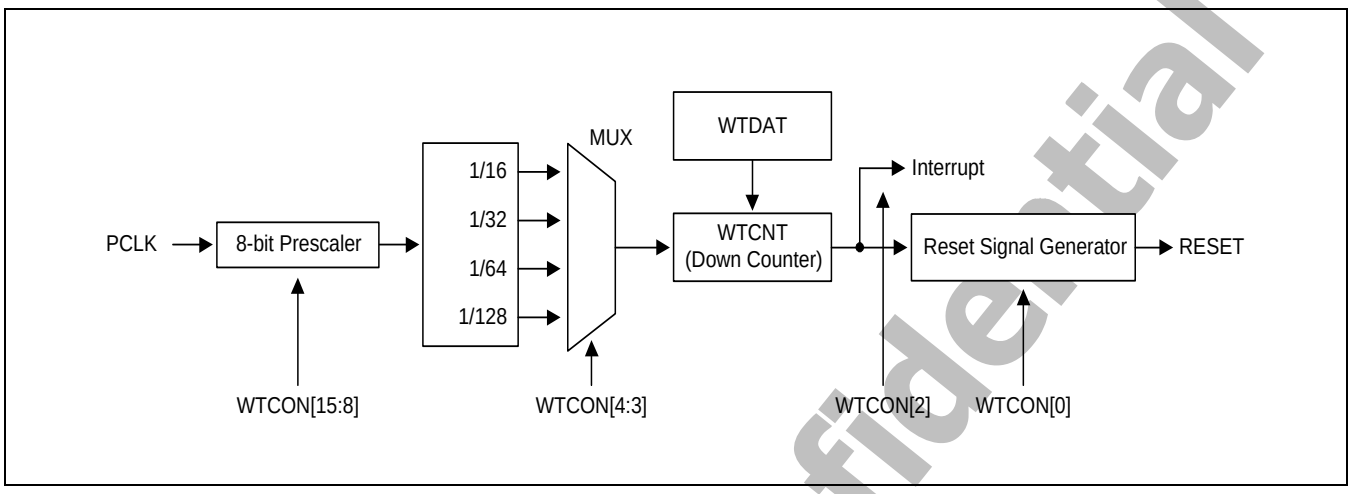

Figure 3-1 Watchdog Timer Block Diagram

The prescaler value and frequency division factor are specified in the watchdog timer control (WTCON) register. Valid prescaler values range from 0 to 2^8-1. The frequency division factor can be selected as, 16, 32, 64, or 128.

Use the following equation to calculate the watchdog timer clock frequency and the duration of each timer clock cycle:

– t_watchdog = 1/(PCLK / (Prescaler value + 1) / Division_factor)

3.3.2 WTDAT AND WTCNT

Once the watchdog timer is enabled, the value of watchdog timer data (WTDAT) register cannot be automatically reloaded into the timer counter (WTCNT). Therefore, an initial value must be written to the watchdog timer count (WTCNT) register, before the watchdog timer starts.

3.3.3 WDT START

To start WDT, set WTCON[0] and WTCON[5] as 1.

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3.3.4 CONSIDERATION OF DEBUGGING ENVIRONMENT

The watchdog timer must not operate if the S5PV210 is in debug mode using Embedded ICE.

The watchdog timer determines from the CPU core signal (DBGACK signal) whether it is currently in the debug mode. Once the DBGACK signal is asserted, the reset output of the watchdog timer is not activated as the watchdog timer expires.

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3.4 REGISTER DESCRIPTION

3.4.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
WTCON	0xE270_0000	R/W	Watchdog Timer Control Register	0x00008021
WTDAT	0xE270_0004	R/W	Watchdog Timer Data Register	0x00008000
WTCNT	0xE270_0008	R/W	Watchdog Timer Count Register	0x00008000
WTCLRINT	0xE270_000C	W	Watchdog Timer Interrupt Clear Register	-

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3.4.1.1 Watchdog Timer Control Register (WTCON, R/W, Address = 0xE270_0000)

The WTCON register allows you to enable/ disable the watchdog timer, select the clock signal from four different sources, enable/ disable interrupts, and enable/ disable the watchdog timer output.
The Watchdog timer is used to restart the S5PV210 to recover from mal-function; if controller restart is not desired, the Watchdog timer should be disabled.

If you want to use the normal timer provided by the Watchdog timer, enable the interrupt and disable the Watchdog timer.

WTCON	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
Prescaler value	[15:8]	Prescaler value. The valid range is from 0 to (2^8-1).	0x80
Reserved	[7:6]	Reserved. These two bits must be 00 in normal operation.	00
Watchdog timer	[5]	Enables or disables Watchdog timer bit. 0 = Disables 1 = Enables	1
Clock select	[4:3]	Determines the clock division factor. 00 = 16 01 = 32 10 = 64 11 = 128	00
Interrupt generation	[2]	Enables or disables interrupt bit. 0 = Disables 1 = Enables	0
Reserved	[1]	Reserved. This bit must be 0 in normal operation.	0
Reset enable/disable	[0]	Enables or disables Watchdog timer output bit for reset signal. 1 = Asserts reset signal of the S5PV210 at watchdog time-out 0 = Disables the reset function of the watchdog timer.	1

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3.4.1.2 Watchdog Timer Data Register (WTDAT, R/W, Address = 0xE270_0004)

The WTDAT register specifies the time-out duration. The content of WTDAT cannot be automatically loaded into the timer counter at initial watchdog timer operation. However, using 0x8000 (initial value) drives the first time-out. In this case, the value of WTDAT is automatically reloaded into WTCNT.

WTDAT	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
Count reload value	[15:0]	Watchdog timer count value for reload.	0x8000

3.4.1.3 Watchdog Timer Count Register (WTCNT, R/W, Address = 0xE270_0008)

The WTCNT register contains the current count values for the watchdog timer during normal operation. Note that the content of the WTDAT register cannot be automatically loaded into the timer count register if the watchdog timer is enabled initially, therefore the WTCNT register must be set to an initial value before enabling it.

WTCNT	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
Count value	[15:0]	The current count value of the watchdog timer	0x8000

3.4.1.4 Watchdog Timer Interrupt Clear Register (WTCLRINT, R/W, Address = 0xE270_000C)

The WTCLRINT register is used to clear the interrupt. Interrupt service routine is responsible to clear the relevant interrupt after the interrupt service is complete. Writing any values on this register clears the interrupt. Reading this register is not allowed.

WTCLRINT	Bit	Description	Initial State
Interrupt clear	[31:0]	Write any value to clear the interrupt	-

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4 REAL TIME CLOCK (RTC)

4.1 OVERVIEW OF REAL TIME CLOCK

The Real Time Clock (RTC) unit can operate using the backup battery while the system power is off. Although power is off, backup battery can store the time by Second, Minute, Hour, Day of the week, Day, Month, and Year data. The RTC unit works with an external 32.768 kHz crystal and performs the function of alarm.

4.2 KEY FEATURES OF REAL TIME CLOCK

- Supports BCD Number, that is Second, Minute, Hour, Day of the week, Day, Month, and Year.
- Supports Leap Year Generator
- Supports Alarm Function, that is ,Alarm-Interrupt or Wake-up from power down modes (idle, deep idle, stop, deep stop, and sleep)
- Supports Tick Counter Function, that is Tick-Interrupt or Wake-up from power down modes (idle, deep idle, stop, deep stop, and sleep)
- Supports Independent Power Pin (RTCVDD)
- Supports millisecond tick time interrupt for RTOS kernel time tick .

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4.2.1 REAL TIME CLOCK OPERATION DESCRIPTION

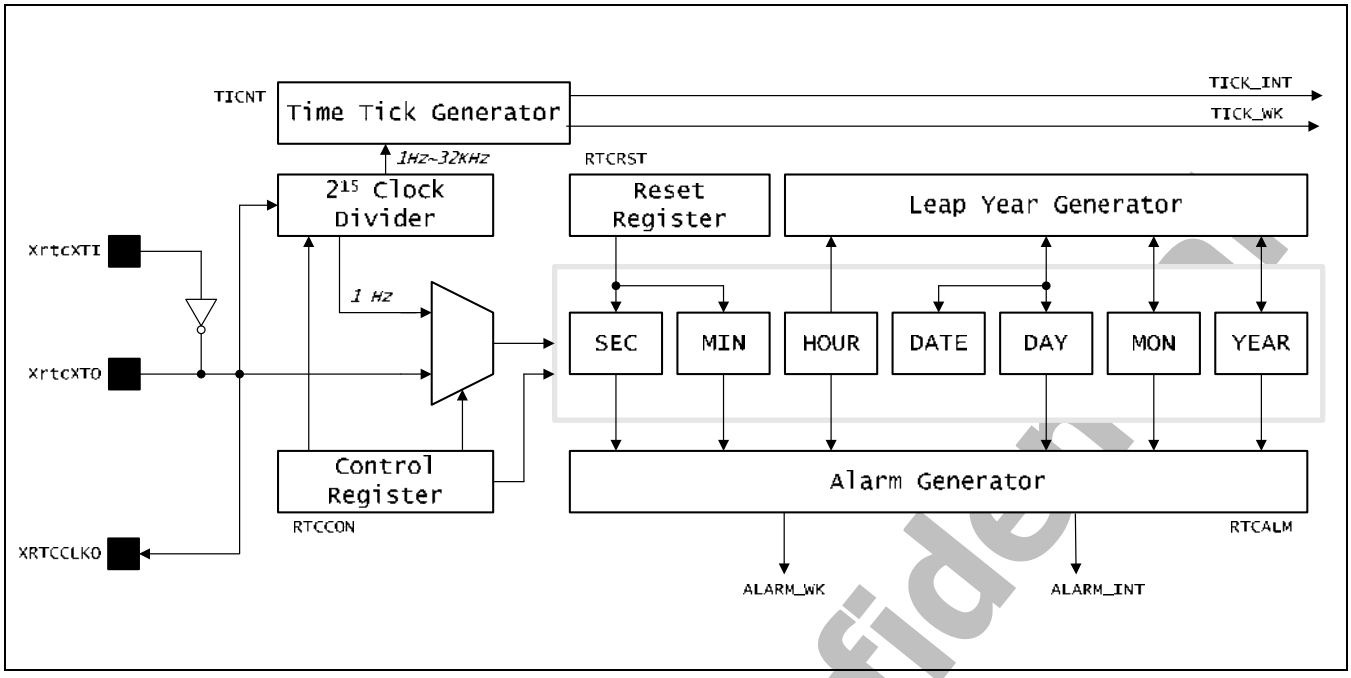

Figure 4-1 Real Time Clock Block Diagram

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4.3 LEAP YEAR GENERATOR

The leap year generator determines the last day of each month out of 28, 29, 30, or 31. This is calculated based on the data from BCDDAY, BCDMON, and BCDYEAR. This block considers leap year while deciding on the last day of a month.

NOTE: The BCDYEAR register is 12-bit wide. It can represent maximum three BCD digits. The implicit number of thousands place is 2. Therefore, it can represent years from 400*n to 400*n + 999 (n = 0, 1, 2, 3, 4, 5, …).

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4.4 READ / WRITE REGISTER

To write the BCD register in RTC block, set the Bit 0 of the RTCCON register. To display the second, minute, hour, day of the week, day, month, and year, the CPU should read the data in BCDSEC, BCDMIN, BCDHOUR, BCDDAYWEEK, BCDDAY, BCDMON, and BCDYEAR registers, respectively, in the RTC block. However, a one-second deviation can exist because multiple registers are read.

For example, if you read the registers from BCDYEAR to BCDMIN, the result is assumed to be 2059 (Year), 12 (Month), 31 (Day), 23 (Hour) and 59 (Minute). If you read the BCDSEC register and the value ranges from 1 to 59 (Second), there is no problem. However, if the value is 0 sec., the year, month, day, hour, and minute can change to 2060 (Year), 1 (Month), 1 (Day), 0 (Hour) and 0 (Minute) because of the one second deviation. In this case, you must read again from BCDYEAR to BCDSEC if BCDSEC is zero.

4.4.1 BACKUP BATTERY OPERATION

The backup battery can drive the RTC logic. The backup battery supplies the power through the RTCVDD pin into the RTC block, even if the system power is off. If the system is off, the interfaces of the CPU and RTC logic should be blocked, and to minimize power dissipation the backup battery only drives the oscillation circuit and the BCD counters.

4.5 ALARM FUNCTION

The RTC generates ALARM_INT (alarm interrupt) and ALARM_WK (alarm wake-up) at a specific time in the power-off mode or normal operation mode. In normal operation mode, ALARM_INT is activated. In the power-off mode, ALARM_WK signal is activated as well as the ALARM_INT. The RTC alarm register (RTCALM) determines the alarm enable/disable status and the condition of the alarm time setting.

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4.6 TICK TIME INTERRUPT

The RTC tick time is used for interrupt request. The TICNT register contains an interrupt enable bit and count value for the interrupt. If the count value reaches '0' if the tick time interrupt occurs. Then the period of interrupt is as follows:

- Period = (n+1) / (Tick clock source frequency) second (n= tick counter value)

Table 4-1 Tick Interrupt Resolution

Tick Counter Clock Source Selection	Tick Clock Source Frequency(Hz)	Clock Range (s)	Resolution (ms)
4'b0000	32768 (2^15)	0 ~ 131071	0.03
4'b0001	16384 (2^14)	0 ~ 262143	0.06
4'b0010	8192 (2^13)	0 ~ 524287	0.12
4'b0011	4096 (2^12)	0 ~ 1048575	0.24
4'b0100	2048 (2^11)	0 ~ 2097151	0.49
4'b0101	1024 (2^10)	0 ~ 4194303	0.97
4'b0110	512 (2^9)	0 ~ 8388607	1.95
4'b0111	256 (2^8)	0 ~ 16777215	3.90
4'b1000	128 (2^7)	0 ~ 33554431	7.81
4'b1001	64 (2^6)	0 ~ 67108863	15.62
4'b1010	32 (2^5)	0 ~ 134217727	31.25
4'b1011	16 (2^4)	0 ~ 268435455	62.50
4'b1100	8 (2^3)	0 ~ 536870911	125
4'b1101	4 (2^2)	0 ~ 1073741823	250
4'b1110	2	0 ~ 2147483647	500
4'b1111	1	0 ~ 4294967295	1000

NOTE: You can select the appropriate tick time clock source to extend the tick time resolution.

This RTC time tick can be used for Real Time Operating System (RTOS) kernel time tick. If RTC time tick generates time tick, the time related function of RTOS always synchronized in real time.

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4.7 32.768KHZ X-TAL CONNECTION EXAMPLE

Figure 4-2 shows a circuit of the RTC unit oscillation at 32.768kHz. The capacitance 20pF of the load capacitor is an example value. It should be adjusted according to the crystal load capacitance.

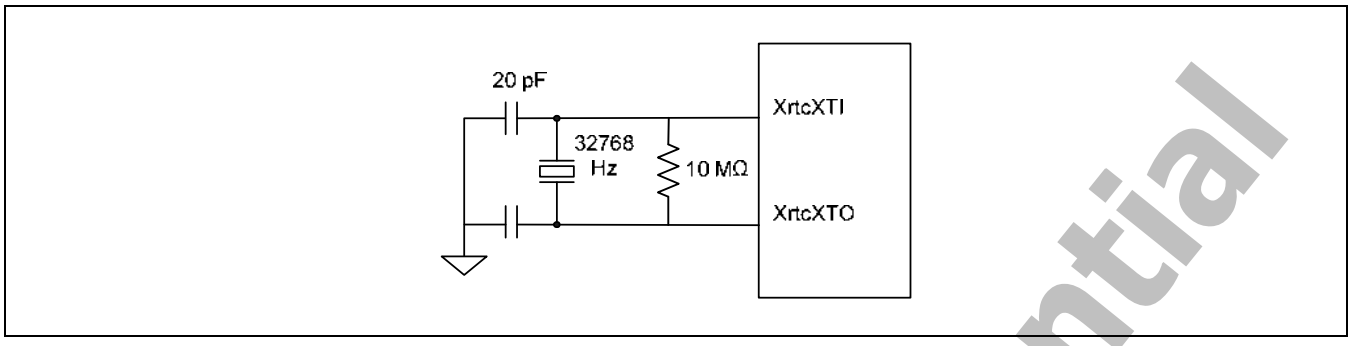

Figure 4-2 Main Oscillator Circuit Example

4.8 RTC START

To start RTC, set RTCCON[0] as 1.

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4.9 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
XT_RTC_I	Input	32.768 kHz RTC Oscillator Clock Input	XrtcXTI	Dedicated
XT_RTC_O	Output	32.768 kHz RTC Oscillator Clock Output	XrtcXTO	Dedicated
XRTCCLKO	Output	32.768 kHz RTC Clock Output (1.8 ~ 3.3V). This signal is turned off by default. It can be enabled by setting 1 in CLKOUTEN field of RTCCON register. Note: In order to use XRTCCLO, ALIVE power must be supplied.	XRTCCLKO	Dedicated

NOTE: Type field indicates whether pads are dedicated to the signal or pads are connected to the multiplexed signals .

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4.10 REGISTER DESCRIPTION

4.10.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
INTP	0xE280_0030	R/W	Specifies the Interrupt Pending Register	0x00000000
RTCCON	0xE280_0040	R/W	Specifies the RTC Control Register	0x00000000
TICCNT	0xE280_0044	R/W	Specifies the Tick Time Count Register	0x00000000
RTCALM	0xE280_0050	R/W	Specifies the RTC Alarm Control Register	0x00000000
ALMSEC	0xE280_0054	R/W	Specifies the Alarm Second Data Register	0x00000000
ALMMIN	0xE280_0058	R/W	Specifies the Alarm Minute Data Register	0x00000000
ALMHOUR	0xE280_005C	R/W	Specifies the Alarm Hour Data Register	0x00000000
ALMDAY	0xE280_0060	R/W	Specifies the Alarm Day Data Register	0x00000000
ALMMON	0xE280_0064	R/W	Specifies the Alarm Month Data Register	0x00000000
ALMYEAR	0xE280_0068	R/W	Specifies the Alarm Year Data Register	0x00000000
BCDSEC	0xE280_0070	R/W	Specifies the BCD Second Register	Undefined
BCDMIN	0xE280_0074	R/W	Specifies the BCD Minute Register	Undefined
BCDHOUR	0xE280_0078	R/W	Specifies the BCD Hour Register	Undefined
BCDDAYWEEK	0xE280_007C	R/W	Specifies the BCD Day of the Week Register	Undefined
BCDDAY	0xE280_0080	R/W	Specifies the BCD Day Register	Undefined
BCDMON	0xE280_0084	R/W	Specifies the BCD Month Register	Undefined
BCDYEAR	0xE280_0088	R/W	Specifies the BCD Year Register	Undefined
CURTICCNT	0xE280_0090	R	Specifies the Current Tick Time Counter Register	0x00000000

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4.10.1.1 Interrupt Pending Register (INTP, R/W, Address = 0xE280_0030)

You can clear specific bits of INTP register by writing 1's to the bits that you want to clear regardless of RTCEN value.

INTP	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0
ALARM	[1]	Alarm interrupt pending bit 0 = No interrupt occurred 1 = Interrupt occurred	0
Time TIC	[0]	Time TIC interrupt pending bit 0 = No interrupt occurred 1 = Interrupt occurred.	0

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4.10.1.2 Real Time Clock Control Register (RTCCON, R/W, Address = 0xE280_0040)

The RTCCON register consists of 10 bits such as the RTCEN, which controls the read/ write enable of the BCD SEL, CNTSEL, CLKRST, TICCKSEL and TICEN for testing, and CLKOUTEN for RTC clock output control.

RTCEN bit controls all interfaces between the CPU and the RTC, therefore it should be set to 1 in an RTC control routine to enable data read/ write after a system reset. To prevent inadvertent writing into BCD counter registers the RTCEN bit should be cleared to 0 before power off.

CLKRST is counter reset for 2^{15} clock divider. Before RTC clock setting, 2^{15} clock divider must be reset for exact RTC operation.

RTCCON	Bit	Description	Initial State
Reserved	[31:10]	Reserved	0
CLKOUTEN	[9]	Enables RTC clock output on XRTCCLKO pad. 0 = Disables 1 = Enables	0
TICEN	[8]	Enables Tick timer 0 = Disables 1 = Enables	0
TICCKSEL	[7:4]	Tick timer sub clock selection. 4'b0000 = 32768 Hz 4'b0001 = 16384 Hz 4'b0010 = 8192 Hz 4'b0011 = 4096 Hz 4'b0100 = 2048 Hz 4'b0101 =1024 Hz 4'b0110 =512 Hz 4'b0111 =256 Hz 4'b1000 =128 Hz 4'b1001 =64 Hz 4'b1010 =32 Hz 4'b1011 =16 Hz 4'b1100 =8 Hz 4'b1101 =4 Hz 4'b1110 =2 Hz 4'b1111 =1 Hz	4'b0000
CLKRST	[3]	RTC clock count reset. 0 = RTC counter (2^{15} clock divider) enable 1 = RTC counter reset and disable Note: When RTCEN is enabled, CLKRST affects RTC.	0
CNTSEL	[2]	BCD count select. 0 = Merge BCD counters 1 = Reserved (Separate BCD counters) Note: When RTCEN is enabled, CNTSEL affects RTC.	0
CLKSEL	[1]	BCD clock select. 0 = XTAL 1/2^{15} divided clock 1 = Reserved (XTAL clock only for test) Note: When RTCEN is enabled, CLKSEL affects RTC.	0
RTCEN	[0]	Enables RTC control. 0 = Disables 1 = Enables Note: When RTCEN is enabled, you can change the BCD time count setting, 2^{15} clock divider reset, BCD counter select, and BCD clock select can be performed.	0

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4.10.1.3 Tick Time Count Register (TICNT, R/W, Address = 0xE280_0044)

TICNT	Bit	Description	Initial State
TICK_TIME_COUNT	[31:0]	32-bit tick time count value. This value must not be 0.	32'b0

4.10.1.4 RTC Alarm Control Register (RTCALM, R/W, Address = 0xE280_0050)

The RTCALM register determines the alarm enable and the alarm time. Note that the RTCALM register generates the alarm signal through both ALARM_INT and ALARM_WK in power down mode, but only through ALARM_INT in the normal operation mode. Enable ALMEN to use ALARM_INT and ALARM_WK.

If compare value is year, ALMEN and YEAREN must be enabled. If compare values are year, month, day, hour, min and sec, ALMEN, YEAREN, MONEN, DAYEN, HOUREN, MINEN and SECEN must be enabled.

RTCALM	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
ALMEN	[6]	Enables Alarm global 0 = Disables 1 = Enables Note: For using ALARM_INT and ALARM_WK, set ALMEN as 1'b1.	0
YEAREN	[5]	Enables Year alarm 0 = Disables 1 = Enables	0
MONEN	[4]	Enables Month alarm 0 = Disables 1 = Enables	0
DAYEN	[3]	Enables Day alarm 0 = Disables 1 = Enables	0
HOUREN	[2]	Enables Hour alarm 0 = Disables 1 = Enables	0
MINEN	[1]	Enables Minute alarm 0 = Disables 1 = Enables	0
SECEN	[0]	Enables Second alarm 0 = Disables 1 = Enables	0

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4.10.1.5 Alarm Second Data Register (ALMSEC, R/W, Address = 0xE280_0054)

ALMSEC	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
SECDATA	[6:4]	BCD value for alarm second. 0 ~ 5	000
	[3:0]	0 ~ 9	0000

4.10.1.6 Alarm Min Data Register (ALMMIN, R/W, Address = 0xE280_0058)

ALMMIN	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
MINDATA	[6:4]	BCD value for alarm minute. 0 ~ 5	000
	[3:0]	0 ~ 9	0000

4.10.1.7 Alarm Hour Data Register (ALMHOUR, R/W, Address = 0xE280_005C)

ALMHOUR	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0
HOURDATA	[5:4]	BCD value for alarm hour. 0 ~ 2	00
	[3:0]	0 ~ 9	0000

4.10.1.8 Alarm DaY Data Register (ALMDAY, R/W, Address = 0xE280_0060)

ALMDAY	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0
DAYDATA	[5:4]	BCD value for alarm day, from 0 to 28, 29, 30, 31. 0 ~ 3	00
	[3:0]	0 ~ 9	0000

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4.10.1.9 ALARM Month Data Register (ALMMON, R/W, Address = 0xE280_0064)

ALMMON	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
MONDATA	[4]	BCD value for alarm month. 0 ~ 1	0
	[3:0]	0 ~ 9	0000

4.10.1.10 ALARM Year Data Register (ALMYEAR, R/W, Address = 0xE280_0068)

ALMYEAR	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
YEARDATA	[11:8]	BCD value for alarm year. 0 ~ 9	0000
	[7:4]	0 ~ 9	0000
	[3:0]	0 ~ 9	0000

4.10.1.11 BCD Second Register (BCDSEC, R/W, Address = 0xE280_0070)

BCDSEC	Bit	Description	Initial State
Reserved	[31:7]	Reserved	-
SECDATA	[6:4]	BCD value for second. 0 ~ 5	-
	[3:0]	0 ~ 9	-

4.10.1.12 BCD Minute Register (BCDMIN, R/W, Address = 0xE280_0074)

BCDMIN	Bit	Description	Initial State
Reserved	[31:7]	Reserved	-
MINDATA	[6:4]	BCD value for minute. 0 ~ 5	-
	[3:0]	0 ~ 9	-

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4.10.1.13 BCD Hour Register (BCDHOUR, R/W, Address = 0xE280_0078)

BCDHOUR	Bit	Description	Initial State
Reserved	[31:6]	Reserved	-
HOURDATA	[5:4]	BCD value for hour. 0 ~ 2	-
	[3:0]	0 ~ 9	-

4.10.1.14 BCD Day Register (BCDDAY R/W, Address = 0xE280_007C)

BCDDAY	Bit	Description	Initial State
Reserved	[31:6]	Reserved	-
DAYDATA	[5:4]	BCD value for day. 0 ~ 3	-
	[3:0]	0 ~ 9	-

4.10.1.15 BCD Day of the Week Register (BCDDAYWEEK, R/W, Address = 0xE280_0080)

BCDDAYWEEK	Bit	Description	Initial State
Reserved	[31:3]	Reserved	-
DAYWEEKDATA	[2:0]	BCD value for a day of the week. 1 ~ 7	-

4.10.1.16 BCD Month Register (BCDMON, R/W, Address = 0xE280_0084)

BCDMON	Bit	Description	Initial State
Reserved	[31:5]	Reserved	-
MONDATA	[4]	BCD value for month. 0 ~ 1	-
	[3:0]	0 ~ 9	-

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4.10.1.17 BCD Year Register (BCDYEAR, R/W, Address = 0xE280_0088)

BCDYEAR	Bit	Description	Initial State
Reserved	[31:8]	Reserved	-
YEARDATA	[11:8]	BCD value for year. 0 ~ 9	-
	[7:4]	0 ~ 9	-
	[3:0]	0 ~ 9	-

4.10.1.18 Tick Counter Register (CURTICCNT, R, Address = 0xE280_0090)

CURTICCNT	Bit	Description	Initial State
Tick counter observation	[31:0]	Current tick count value	-

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Section 8

CONNECTIVITY/ STORAGE

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1 UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

1.1 OVERVIEW OF UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

The Universal Asynchronous Receiver and Transmitter (UART) in S5PV210 provide four independent asynchronous, and serial input/output (I/O) ports. All the ports operate in an interrupt-based or a DMA-based mode. The UART generates an interrupt or a DMA request to transfer data to and from the CPU and the UART. The UART supports bit rates up to 3Mbps. Each UART channel contains two FIFOs to receive and transmit data: 256 bytes in ch0, 64 bytes in ch1 and 16 bytes in ch2 and ch3.

UART includes programmable baud rates, infrared (IR) transmitter/receiver, one or two stop bit insertion, 5-bit, 6-bit, 7-bit, or 8-bit data width and parity checking.

Each UART contains a baud-rate generator, a transmitter, a receiver and a control unit, as shown in *Figure 1-1*. The baud-rate generator uses PCLK or SCLK_UART. The transmitter and the receiver contain FIFOs and data shifters. The data to be transmitted is written to Tx FIFO, and copied to the transmit shifter. The data is then shifted out by the transmit data pin (TxDn). The received data is shifted from the receive data pin (RxDn), and copied to Rx FIFO from the shifter.

1.2 KEY FEATURES OF UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

- RxD0, TxD0, RxD1, TxD1, RxD2, TxD2, RxD3 and TxD3 with DMA-based or interrupt-based operation
- UART Ch 0, 1, 2 and 3 with IrDA 1.0
- UART Ch 0 with 256-byte FIFO, Ch 1 with 64-byte FIFO, Ch2 and 3 with 16-byte FIFO
- UART Ch 0, 1 and 2 with nRTS0, nCTS0, nRTS1, nCTS1, nCTS2 and nRTS2 for Auto Flow Control
- Supports handshake transmit/receive.

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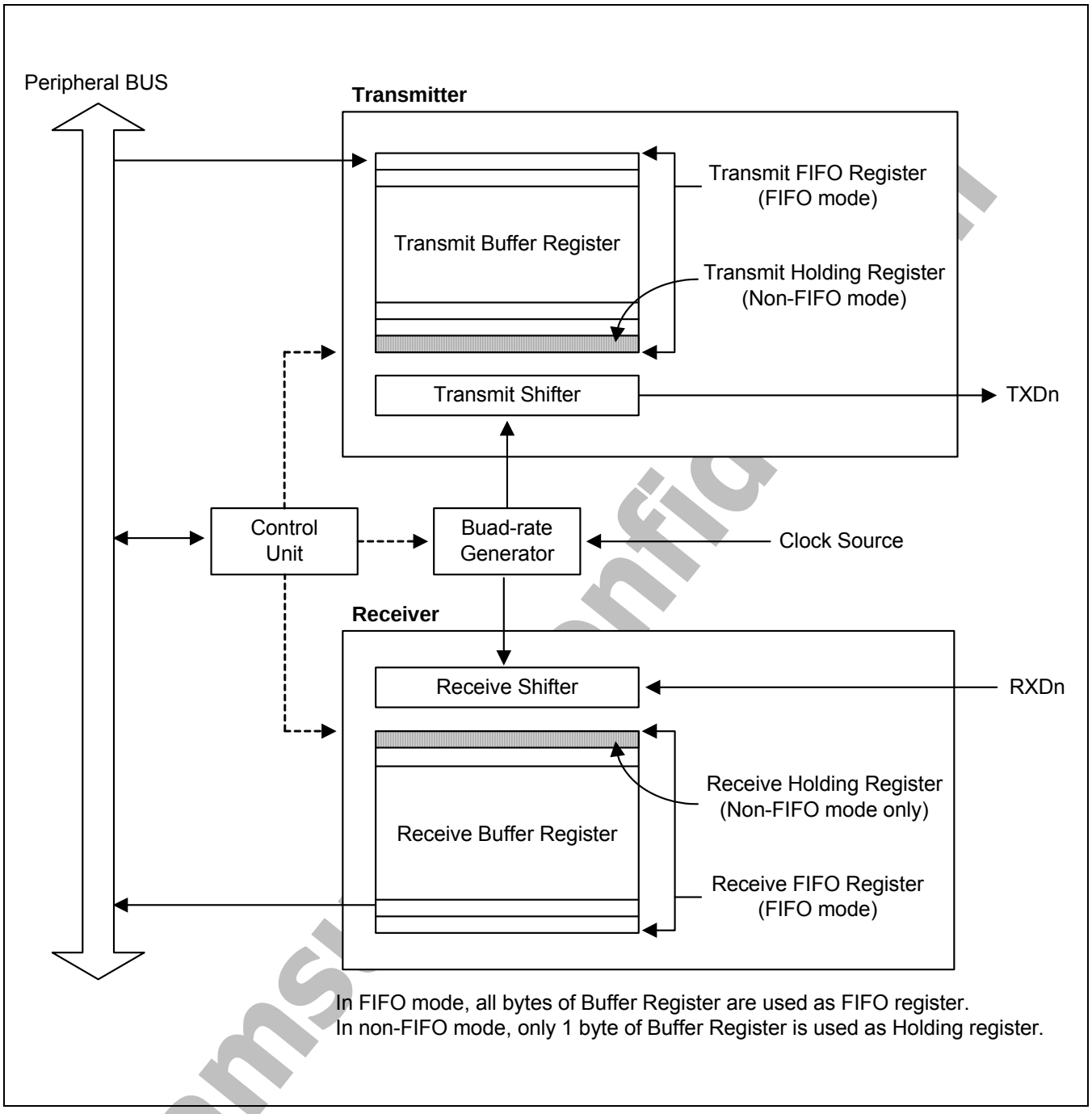

Figure 1-1 Block Diagram of UART

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1.3 UART DESCRIPTION

The following sections describe UART operations, such as data transmission, data reception, interrupt generation, baud-rate generation, loop-back mode, infrared modes, and auto flow control.

1.3.1 DATA TRANSMISSION

The data frame for transmission is programmable. It consists of a start bit, five to eight data bits, an optional parity bit, and one to two stop bits, specified by the line control register (ULCONn). The transmitter can also produce a break condition that forces the serial output to logic 0 state for one frame transmission time. This block transmits the break signals after the present transmission word is transmitted completely. After the break signal transmission, the transmitter continuously transmits data to Tx FIFO (Tx holding register, in case of Non-FIFO mode).

1.3.2 DATA RECEPTION

Similar to data transmission, the data frame for reception is also programmable. It consists of a start bit, five to eight data bits, an optional parity bit, and one to two stop bits in the line control register (ULCONn). The receiver detects overrun error, parity error, frame error and break condition, each of which sets an error flag.

- Overrun error indicates that new data has overwritten the old data before the old data was read.
- Parity error indicates that the receiver has detected an unexpected parity condition.
- Frame error indicates that the received data does not have a valid stop bit.
- Break condition indicates that the RxDn input is held in the logic 0 state for more than one frame transmission time.

Receive time-out condition occurs if no data is received during the 3-word time (this interval follows the setting of Word Length bit) and the Rx FIFO is not empty in the FIFO mode.

1.3.3 AUTO FLOW CONTROL (AFC)

The UART0 and UART1 in S5PV210 support auto flow control (AFC) using nRTS and nCTS signals. UART2 supports auto flow control if TxD3 and RxD3 are set as nRTS2 and nCTS2 by GPA1CON(GPIO SFR). In this case, it can be connected to external UARTs. To connect UART to a Modem, disable the AFC bit in UMCONn register and control the signal of nRTS using software.

In AFC, the nRTS signal depends on the condition of the receiver, whereas the nCTS signals control the operation of transmitter. The UART's transmitter transfers the data to FIFO if nCTS signals are activated (in AFC, nCTS signals means that other UART's FIFO is ready to receive data). Before UART receives data, the nRTS signals must be activated if its receive FIFO has more than 2-byte as spare. The nRTS signals must be inactivated if its receive FIFO has less than 1-byte as spare (in AFC, the nRTS signals means that its own receive FIFO is ready to receive data).

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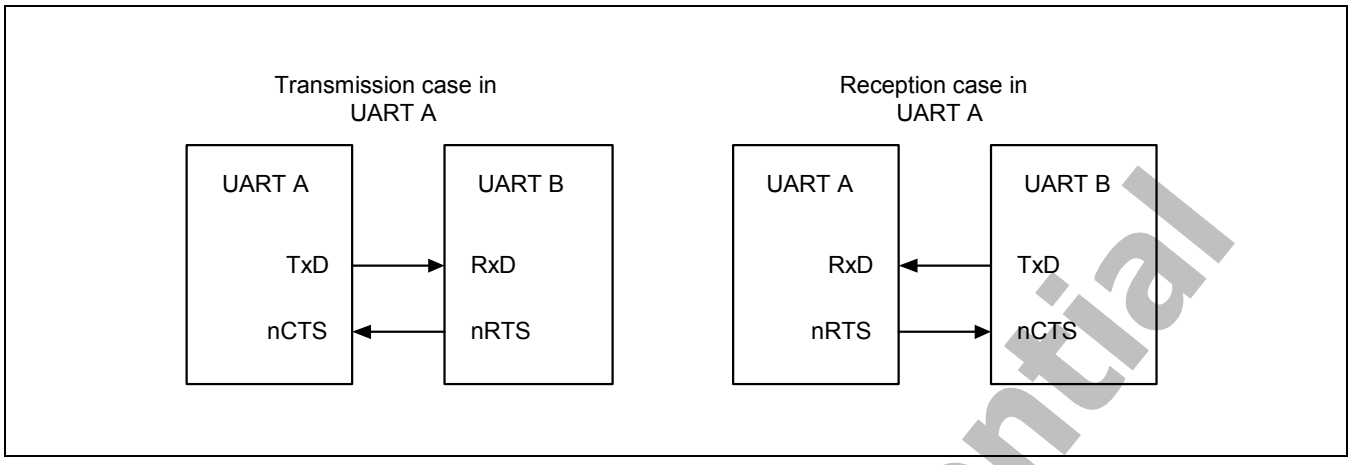

Figure 1-2 UART AFC Interface

1.3.4 EXAMPLE OF NON AUTO-FLOW CONTROL (CONTROLLING NRTS AND NCTS BY SOFTWARE)

1.3.4.1 Rx Operation with FIFO

1. Select the transmit mode (Interrupt or DMA mode).
2. Check the value of Rx FIFO count in UFSTATn register. If the value is less than 16, you must set the value of UMCONn[0] to '1' (activate nRTS). However, if the value equal to or larger than 16, you must set the value to '0' (inactivate nRTS).
3. Repeat the Step 2.

1.3.4.2 Tx Operation with FIFO

1. Select the transmit mode (Interrupt or DMA mode).
2. Check the value of UMSTATn[0]. If the value is '1' (activate nCTS), you must write data to Tx FIFO register.
3. Repeat the Step 2

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1.3.5 TX/RX FIFO TRIGGER LEVEL AND DMA BURST SIZE IN DMA MODE

If Tx/Rx data reaches the Tx/Rx FIFO trigger level of UFCONn register in DMA mode, the DMA transaction starts. A single DMA transaction transfers a data whose size is specified as the DMA burst size of UCONn register, and the DMA transactions are repeated until transferred data size reaches the Tx/Rx FIFO trigger level. Thus, DMA burst size should be less than or equal to Tx/Rx FIFO trigger level. In general, it is recommended to ensure that Tx/Rx FIFO trigger level and DMA burst size matches.

1.3.6 RS-232C INTERFACE

To connect the UART to modem interface (instead of null modem), nRTS, nCTS, nDSR, nDTR, DCD and nRI signals are required. You can control these signals with general I/O ports using software because the AFC does not support the RS-232C interface.

1.3.7 INTERRUPT/DMA REQUEST GENERATION

Each UART in S5PV210 comprises of seven status (Tx/Rx/Error) signals, namely, Overrun error, Parity error, Frame error, Break, Receive buffer data ready, Transmit buffer empty, and Transmit shifter empty. These conditions are indicated by the corresponding UART status register (UTRSTATn/UERSTATn).

The Overrun Error, Parity Error, Frame Error and Break Condition specify the receive error status. If receive-error-status-interrupt-enable bit is set to 1 in the control register (UCONn), the receive error status generates receive-error-status-interrupt. If a receive-error-status-interrupt-request is detected, you can identify the source of interrupt by reading the value of UERSTATn.

If the receiver transfers data of the receive shifter to the receive FIFO register in FIFO mode, and the number of received data is greater than or equal to the Rx FIFO Trigger Level, Rx interrupt is generated if Receive mode in control register (UCONn) is set to 1 (Interrupt request or polling mode).

In Non-FIFO mode, transferring the data of receive shifter to receive holding register causes Rx interrupt in the Interrupt request and polling modes.

If the transmitter transfers data from its transmit FIFO register to transmit shifter and the number of data left in transmit FIFO is less than or equal to the Tx FIFO Trigger Level, Tx interrupt is generated (provided Transmit mode in control register is selected as Interrupt request or polling mode). In Non-FIFO mode, transferring the data from transmit holding register to transmit shifter causes Tx interrupt in the Interrupt request and polling mode.

Remember that the Tx interrupt is always requested if the number of data in the transmit FIFO is smaller than the trigger level. This means that an interrupt is requested as soon as you enable the Tx interrupt, unless you fill the Tx buffer. It is recommended to fill the Tx buffer first and then enable the Tx interrupt.

The interrupt controllers of S5PV210 are of the level-triggered type. You must set the interrupt type as ‘Level’ if you program the UART control registers.

If Receive and Transmit modes in control register are selected as DMAn request mode, then DMAn request occurs instead of Rx or Tx interrupt in the above situation.

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Table 1-1 Interrupts in Connection with FIFO

Type	FIFO Mode	Non-FIFO Mode
Rx interrupt	Generated if Rx FIFO count is greater than or equal to the trigger level of received FIFO. Generated if the number of data in FIFO does not reaches Rx FIFO trigger Level and does not receive any data during 3-word time (receive time out). This interval follows the setting of Word Length bit.	Generated by receive holding register whenever receive buffer becomes full.
Tx interrupt	Generated if Tx FIFO count is less than or equal to the trigger level of transmit FIFO (Tx FIFO trigger Level).	Generated by transmit holding register whenever transmit buffer becomes empty.
Error interrupt	Generated if frame error, parity error, or break signal are detected. Generated if UART receives new data when Rx FIFO is full (overrun error).	Generated by all errors. However if another error occurs at the same time, only one interrupt is generated.

1.3.8 UART ERROR STATUS FIFO

UART contains the error status FIFO besides the Rx FIFO register. The error status FIFO indicates which data, among FIFO registers is received with an error. An error interrupt is issued only if the data containing an error, is ready to read out. To clear the error status FIFO, URXHn with an error and UERSTATn must be read out.

For example, it is assumed that the UART Rx FIFO receives A, B, C, D, and E characters sequentially and the frame error occurs while receiving 'B' and the parity error occurs while receiving 'D'.

The actual UART receive error does not generate any error interrupt, since the character, which was received with an error was not read. The error interrupt occurs if the character is read out.

Time	Sequence Flow	Error Interrupt	Note
#0	If no character is read out	-	
#1	A, B, C, D, and E is received	-	
#2	After A is read out	Frame error (in B) interrupt occurs.	The 'B' has to be read out.
#3	After B is read out	-	
#4	After C is read out	Parity error (in D) interrupt occurs.	The 'D' has to be read out.
#5	After D is read out	-	
#6	After E is read out	-	

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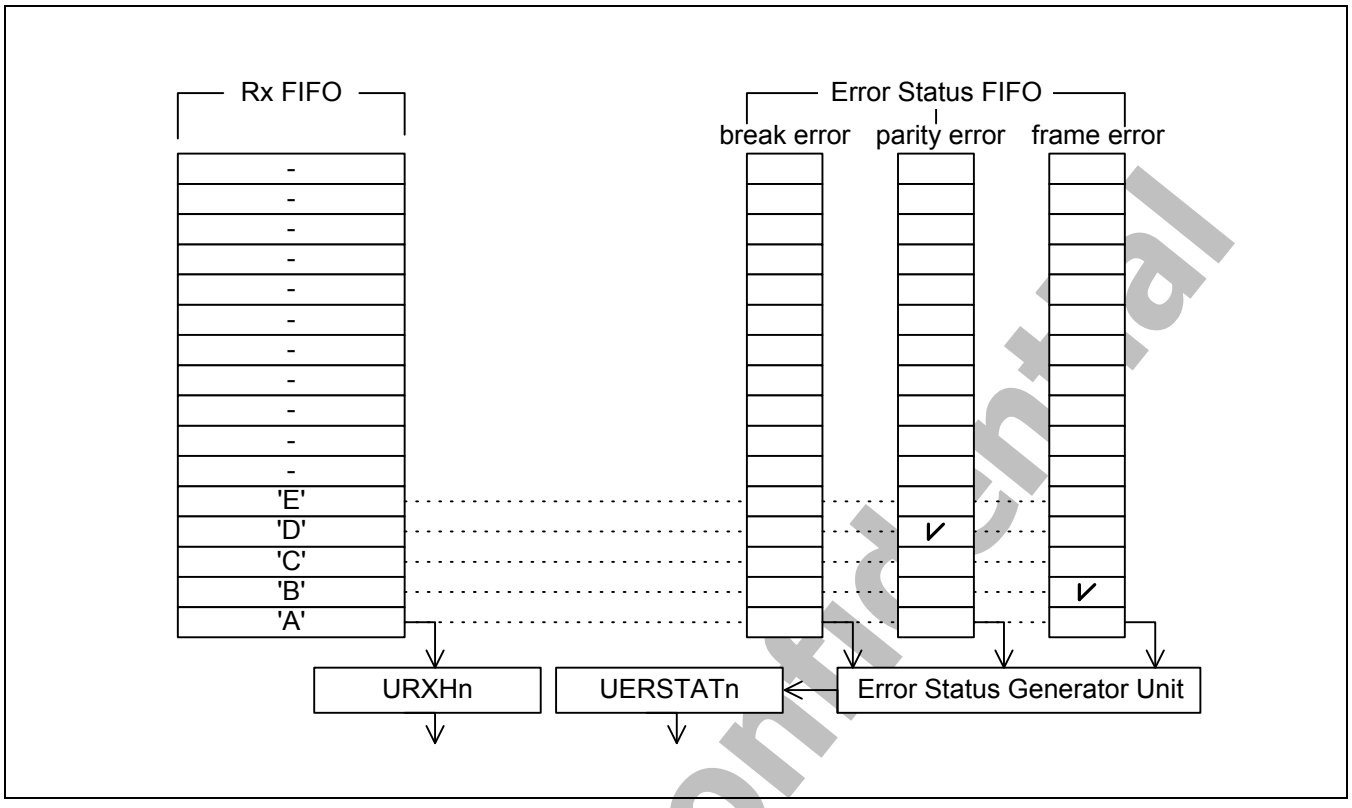

Figure 1-3 UART Receives the Five Characters Including Two Errors

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1.3.8.1 Infra-Red (IR) Mode

The S5PV210 UART block supports both infra-red (IR) transmission and reception. It is selected by setting the Infra-red-mode bit in the UART line control register (ULCONn). *Figure 1-4* illustrates how to implement the IR mode.
In IR transmit mode, the transmit pulse comes out at the rate of 3/16, that is, normal serial transmit rate (if the transmit data bit is 0). In IR receive mode, however, the receiver must detect the 3/16 pulsed period to recognize a 0 value (Refer to the frame timing diagrams shown in *Figure 1-5* and *Figure 1-7*).

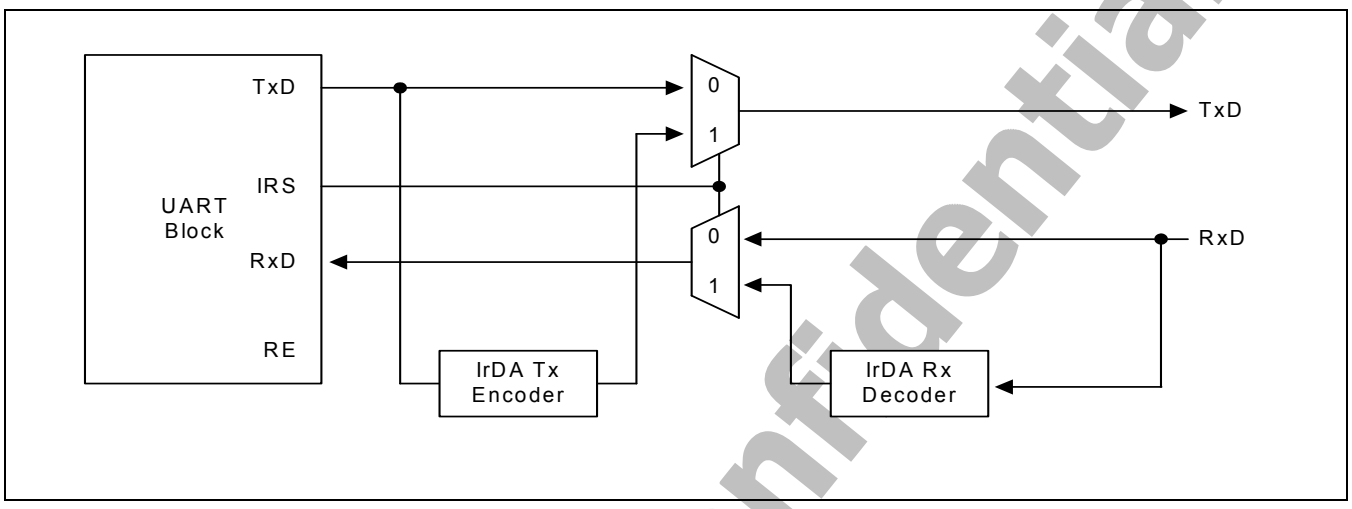

Figure 1-4 IrDA Function Block Diagram

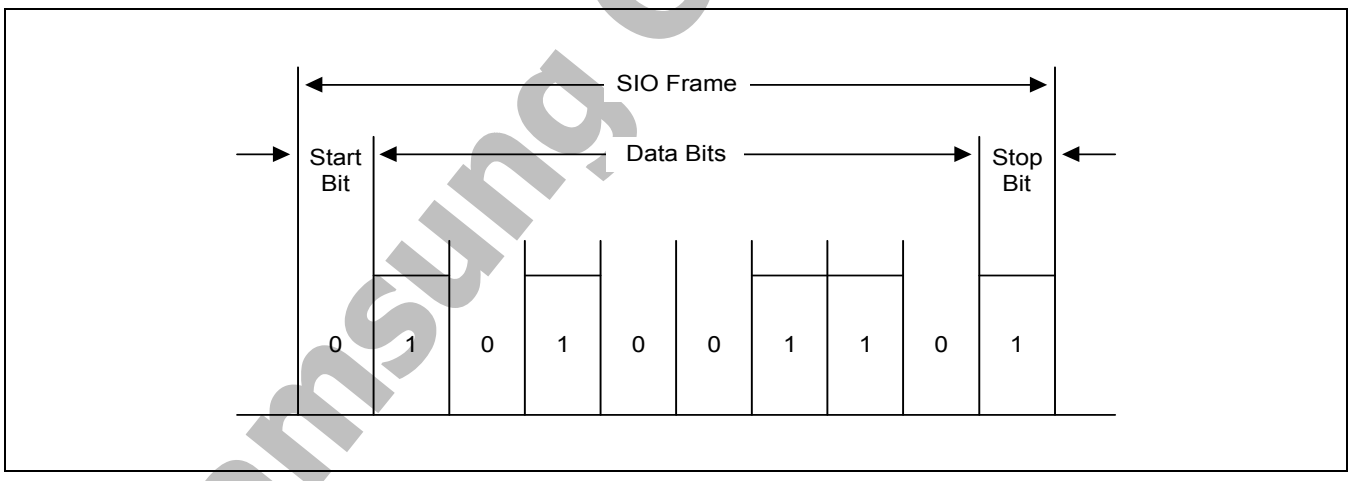

Figure 1-5 Serial I/O Frame Timing Diagram (Normal UART)

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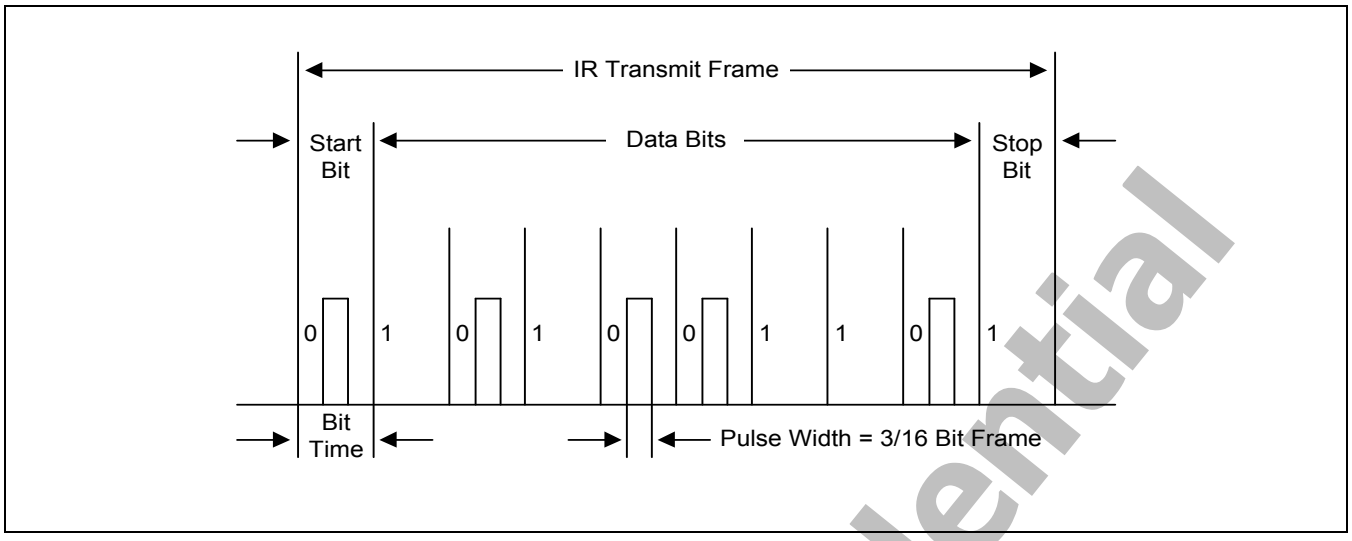

Figure 1-6 Infra-Red Transmit Mode Frame Timing Diagram

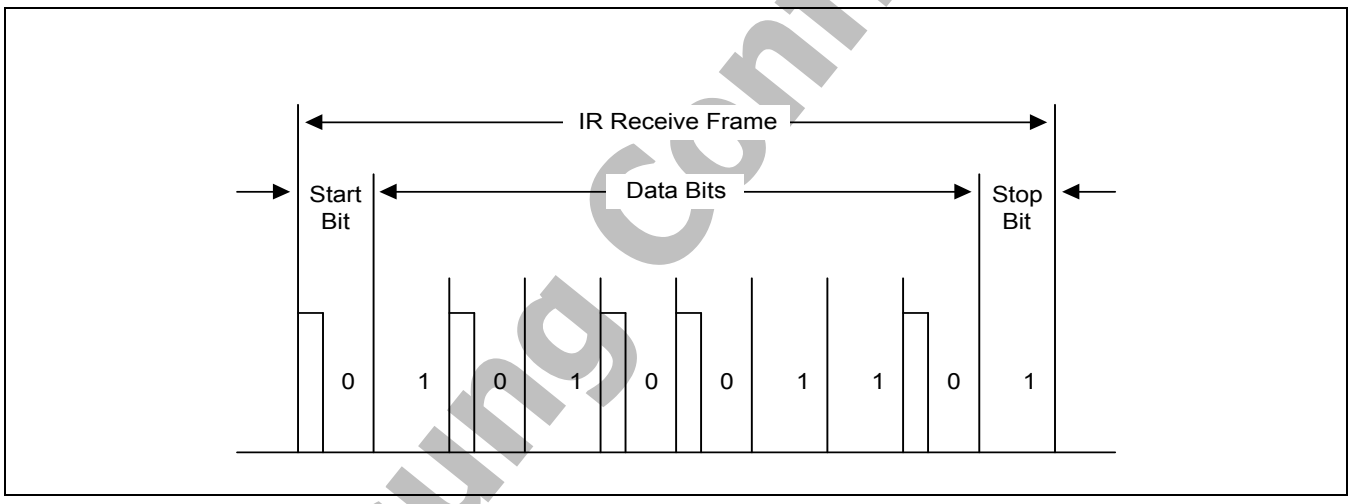

Figure 1-7 Infra-Red Receive Mode Frame Timing Diagram

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1.4 UART INPUT CLOCK DIAGRAM DESCRIPTION

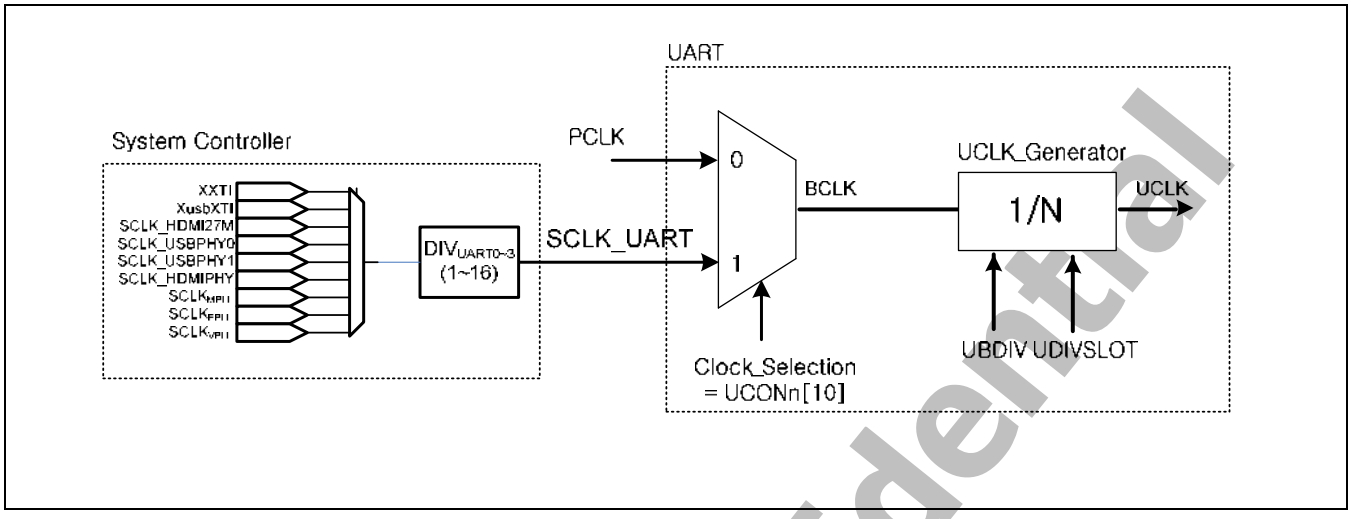

Figure 1-8 Input Clock Diagram for UART

S5PV210 provides UART with a variety of clocks. As described in the *Figure 1-8*, the UART is able to select clocks from PCLK, or SCLK_UART, which is from clock controller. You can also select SCLK_UART from PLLs. To select SCLK_UART, please refer to Section 2-3 Clock Controller.

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1.5 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
UART_0_RXD	Input	Receives Data for UART0	XuRXD[0]	muxed
UART_0_TXD	Output	Transmits Data for UART0	XuTXD[0]	muxed
UART_0_CTSn	Input	Clears to Send(active low) for UART0	XuCTSn[0]	muxed
UART_0_RTSn	Output	Requests to Send(active low) for UART0	XuRTSn[0]	muxed
UART_1_RXD	Input	Receives Data for UART1	XuRXD[1]	muxed
UART_1_TXD	Output	Transmits Data for UART1	XuTXD[1]	muxed
UART_1_CTSn	Input	Clears to Send(active low) for UART1	XuCTSn[1]	muxed
UART_1_RTSn	Output	Requests to Send(active low) for UART1	XuRTSn[1]	muxed
UART_2_RXD	Input	Receives Data for UART2	XuRXD[2]	muxed
UART_2_TXD	Output	Transmits Data for UART2	XuTXD[2]	muxed
UART_2_CTSn	Input	Clears to Send(active low) for UART2	XuRXD[3]	muxed
UART_2_RTSn	Output	Requests to Send(active low) for UART2	XuTXD[3]	muxed
UART_3_RXD	Input	Receives Data for UART3	XuRXD[3]	muxed
UART_3_TXD	Output	Transmits Data for UART3	XuTXD[3]	muxed

NOTE: Type field indicates whether pads are dedicated to the signal or pads are connected to the multiplexed signals. UART external pads are shared with IrDA. In order to use these pads, GPIO must be set before the start of UART. Please refer to Section 2-2 GPIO for exact settings

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1.6 REGISTER DESCRIPTION

1.6.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
ULCON0	0xE290_0000	R/W	Specifies the UART Channel 0 Line Control Register	0x00000000
UCON0	0xE290_0004	R/W	Specifies the UART Channel 0 Control Register	0x00000000
UFCON0	0xE290_0008	R/W	Specifies the UART Channel 0 FIFO Control Register	0x00000000
UMCON0	0xE290_000C	R/W	Specifies the UART Channel 0 Modem Control Register	0x00000000
UTRSTAT0	0xE290_0010	R	Specifies the UART Channel 0 Tx/Rx Status Register	0x00000006
UERSTAT0	0xE290_0014	R	Specifies the UART Channel 0 Rx Error Status Register	0x00000000
UFSTAT0	0xE290_0018	R	Specifies the UART Channel 0 FIFO Status Register	0x00000000
UMSTAT0	0xE290_001C	R	Specifies the UART Channel 0 Modem Status Register	0x00000000
UTXH0	0xE290_0020	W	Specifies the UART Channel 0 Transmit Buffer Register	-
URXH0	0xE290_0024	R	Specifies the UART Channel 0 Receive Buffer Register	0x00000000
UBRDIV0	0xE290_0028	R/W	Specifies the UART Channel 0 Baud Rate Divisor Register	0x00000000
UDIVSLOT0	0xE290_002C	R/W	Specifies the UART Channel 0 Dividing Slot Register	0x00000000
UINTP0	0xE290_0030	R/W	Specifies the UART Channel 0 Interrupt Pending Register	0x00000000
UINTSP0	0xE290_0034	R/W	Specifies the UART Channel 0 Interrupt Source Pending Register	0x00000000
UINTM0	0xE290_0038	R/W	Specifies the UART Channel 0 Interrupt Mask Register	0x00000000
ULCON1	0xE290_0400	R/W	Specifies the UART Channel 1 Line Control Register	0x00000000
UCON1	0xE290_0404	R/W	Specifies the UART Channel 1 Control Register	0x00000000
UFCON1	0xE290_0408	R/W	Specifies the UART Channel 1 FIFO Control Register	0x00000000
UMCON1	0xE290_040C	R/W	Specifies the UART Channel 1 Modem Control Register	0x00000000
UTRSTAT1	0xE290_0410	R	Specifies the UART Channel 1 Tx/Rx Status Register	0x00000006
UERSTAT1	0xE290_0414	R	Specifies the UART Channel 1 Rx Error Status	0x00000000

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Register	Address	R/W	Description	Reset Value
			Register	
UFSTAT1	0xE290_0418	R	Specifies the UART Channel 1 FIFO Status Register	0x00000000
UMSTAT1	0xE290_041C	R	Specifies the UART Channel 1 Modem Status Register	0x00000000
UTXH1	0xE290_0420	W	Specifies the UART Channel 1 Transmit Buffer Register	-
URXH1	0xE290_0424	R	Specifies the UART Channel 1 Receive Buffer Register	0x00000000
UBRDIV1	0xE290_0428	R/W	Specifies the UART Channel 1 Baud Rate Divisor Register	0x00000000
UDIVSLOT1	0xE290_042C	R/W	Specifies the UART Channel 1 Dividing Slot Register	0x00000000
UINTP1	0xE290_0430	R/W	Specifies the UART Channel 1 Interrupt Pending Register	0x00000000
UINTSP1	0xE290_0434	R/W	Specifies the UART Channel 1 Interrupt Source Pending Register	0x00000000
UINTM1	0xE290_0438	R/W	Specifies the UART Channel 1 Interrupt Mask Register	0x00000000
ULCON2	0xE290_0800	R/W	Specifies the UART Channel 2 Line Control Register	0x00000000
UCON2	0xE290_0804	R/W	Specifies the UART Channel 2 Control Register	0x00000000
UFCON2	0xE290_0808	R/W	Specifies the UART Channel 2 FIFO Control Register	0x00000000
UMCON2	0xE290_080C	R/W	Specifies the UART Channel 2 Modem Control Register	0x00000000
UTRSTAT2	0xE290_0810	R	Specifies the UART Channel 2 Tx/Rx Status Register	0x00000006
UERSTAT2	0xE290_0814	R	Specifies the UART Channel 2 Rx Error Status Register	0x00000000
UFSTAT2	0xE290_0818	R	Specifies the UART Channel 2 FIFO Status Register	0x00000000
UMSTAT2	0xE290_081C	R	Specifies the UART Channel 2 Modem Status Register	0x00000000
UTXH2	0xE290_0820	W	Specifies the UART Channel 2 Transmit Buffer Register	-
URXH2	0xE290_0824	R	Specifies the UART Channel 2 Receive Buffer Register	0x00000000
UBRDIV2	0xE290_0828	R/W	Specifies the UART Channel 2 Baud Rate Divisor Register	0x00000000
UDIVSLOT2	0xE290_082C	R/W	Specifies the UART Channel 2 Dividing Slot Register	0x00000000
INTP2	0xE290_0830	R/W	Specifies the UART Channel 2 Interrupt Pending	0x00000000

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Register	Address	R/W	Description	Reset Value
			Register	
UINTSP2	0xE290_0834	R/W	Specifies the UART Channel 2 Interrupt Source Pending Register	0x00000000
UINTM2	0xE290_0838	R/W	Specifies the UART Channel 2 Interrupt Mask Register	0x00000000
ULCON3	0xE290_0C00	R/W	Specifies the UART Channel 3 Line Control Register	0x00000000
UCON3	0xE290_0C04	R/W	Specifies the UART Channel 3 Control Register	0x00000000
UFCON3	0xE290_0C08	R/W	Specifies the UART Channel 3 FIFO Control Register	0x00000000
UMCON3	0xE290_0C0C	R/W	Specifies the UART Channel 3 Modem Control Register	0x00000000
UTRSTAT3	0xE290_0C10	R	Specifies the UART Channel 3 Tx/Rx Status Register	0x00000006
UERSTAT3	0xE290_0C14	R	Specifies the UART Channel 3 Rx Error Status Register	0x00000000
UFSTAT3	0xE290_0C18	R	Specifies the UART Channel 3 FIFO Status Register	0x00000000
UMSTAT3	0xE290_0C1C	R	Specifies the UART Channel 3 Modem Status Register	0x00000000
UTXH3	0xE290_0C20	W	Specifies the UART Channel 3 transmit Buffer Register	-
URXH3	0xE290_0C24	R	Specifies the UART Channel 3 receive Buffer Register	0x00000000
UBRDIV3	0xE290_0C28	R/W	Specifies the UART Channel 3 Baud Rate Divisor Register	0x00000000
UDIVSLOT3	0xE290_0C2C	R/W	Specifies the UART Channel 3 Dividing Slot Register	0x00000000
INTP3	0xE290_0C30	R/W	Specifies the UART Channel 3 Interrupt Pending Register	0x00000000
UINTSP3	0xE290_0C34	R/W	Specifies the UART Channel 3 Interrupt Source Pending Register	0x00000000
UINTM3	0xE290_0C38	R/W	Specifies the UART Channel 3 Interrupt Mask Register	0x00000000

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1.6.1.1 UART Line Control Register

- ULCON0, R/W, Address = 0xE290_0000
- ULCON1, R/W, Address = 0xE290_0400
- ULCON2, R/W, Address = 0xE290_0800
- ULCON3, R/W, Address = 0xE290_0C00

There are four UART line control registers in the UART block, namely, ULCON0, ULCON1, ULCON2, and ULCON3.

ULCONn	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
Infrared Mode	[6]	Determines whether to use the Infrared mode. 0 = Normal mode operation 1 = Infrared Tx/Rx mode	0
Parity Mode	[5:3]	Specifies the type of parity generation to be performed and checking during UART transmit and receive operation. 0xx = No parity 100 = Odd parity 101 = Even parity 110 = Parity forced/ checked as 1 111 = Parity forced/ checked as 0	000
Number of Stop Bit	[2]	Specifies how many stop bits are used to signal end-of-frame signal. 0 = One stop bit per frame 1 = Two stop bit per frame	0
Word Length	[1:0]	Indicates the number of data bits to be transmitted or received per frame. 00 = 5-bit 01 = 6-bit 10 = 7-bit 11 = 8-bit	00

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1.6.1.2 UART Control Register

- UCON0, R/W, Address = 0xE290_0004
- UCON1, R/W, Address = 0xE290_0404
- UCON2, R/W, Address = 0xE290_0804
- UCON3, R/W, Address = 0xE290_0C04

There are four UART control registers in the UART block, namely, UCON0, UCON1, UCON2 and UCON3.

UCONn	Bit	Description	Initial State
Reserved	[31:21]	Reserved	000
Tx DMA Burst Size	[20]	Tx DMA Burst Size 0 = 1 byte (Single) 1 = 4 bytes	0
Reserved	[19:17]	Reserved	000
Rx DMA Burst Size	[16]	Rx DMA Burst Size 0 = 1 byte (Single) 1 = 4 bytes	0
Reserved	[15:11]	Reserved	0000
Clock Selection	[10]	Selects PCLK or SCLK_UART (from Clock Controller) clock for the UART baud rate. 0 = PCLK: DIV_VAL1) = (PCLK / (bps x 16)) –1 1 = SCLK_UART: DIV_VAL1) = (SCLK_UART / (bps x 16)) –1	00
Tx Interrupt Type	[9]	Interrupt request type.(2) 0 = Pulse (Interrupt is requested when the Tx buffer is empty in the Non-FIFO mode or when it reaches Tx FIFO Trigger Level in the FIFO mode.) 1 = Level (Interrupt is requested when Tx buffer is empty in the Non-FIFO mode or when it reaches Tx FIFO Trigger Level in the FIFO mode.)	0
Rx Interrupt Type	[8]	Interrupt request type. (2) 0 = Pulse (Interrupt is requested when instant Rx buffer receives data in the Non-FIFO mode or when it reaches Rx FIFO Trigger Level in the FIFO mode.) 1 = Level (Interrupt is requested when Rx buffer is receiving data in the Non-FIFO mode or when it reaches Rx FIFO Trigger Level in the FIFO mode.)	0
Rx Time Out Enable	[7]	Enables/ Disables Rx time-out interrupts if UART FIFO is enabled. The interrupt is a receive interrupt. 0 = Disables 1 = Enables	0
Rx Error Status Interrupt Enable	[6]	Enables the UART to generate an interrupt upon an exception, such as a break, frame error, parity error, or overrun error during a receive operation. 0 = Does not generate receive error status interrupt. 1 = Generates receive error status interrupt.	0

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UCONn	Bit	Description	Initial State
Loop-back Mode	[5]	Setting loop-back bit to 1 trigger the UART to enter the loop-back mode. This mode is provided for test purposes only. 0 = Normal operation 1 = Loop-back mode	0
Send Break Signal	[4]	Setting this bit trigger the UART to send a break during 1 frame time. This bit is automatically cleared after sending the break signal. 0 = Normal transmit 1 = Sends the break signal	0
Transmit Mode	[3:2]	Determines which function is able to write Tx data to the UART transmit buffer register. 00 = Disables 01 = Interrupt request or polling mode 10 = DMA mode 11 = Reserved	00
Receive Mode	[1:0]	Determines which function is able to read data from UART receive buffer register. 00 = Disables 01 = Interrupt request or polling mode 10 = DMA mode 11 = Reserved	00

NOTE:

1. DIV_VAL = UBRDIVn + (num of 1's in UDIVSLOTn)/16. Refer to 1.6.1.11 UART Channel Baud Rate Division Register and 1.6.1.12 UART Channel Dividing Slot Register
2. S5PV210 use a level-triggered interrupt controller. Therefore, these bits must be set to 1 for every transfer.
3. If the UART does not reach the FIFO trigger level and does not receive data during 3 word time in DMA receive mode with FIFO, the Rx interrupt is generated (receive time out). You must check the FIFO status and read out the rest.

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1.6.1.3 UART FIFO Control Register

- UFCON0, R/W, Address = 0xE290_0008
- UFCON1, R/W, Address = 0xE290_0408
- UFCON2, R/W, Address = 0xE290_0808
- UFCON3, R/W, Address = 0xE290_0C08

There are four UART FIFO control registers in the UART block, namely, UFCON0, UFCON1, UFCON2 and UFCON3.

UFCONn	Bit	Description	Initial State
Reserved	[31:11]	Reserved	0
Tx FIFO Trigger Level	[10:8]	Determines the trigger level of Tx FIFO. If data count of Tx FIFO is less than or equal to the trigger level, Tx interrupt occurs. [Channel 0] 000 = 0 byte 001 = 32 bytes 010 = 64 bytes 011 = 96 bytes 100 = 128 bytes 101 = 160 bytes 110 = 192 bytes 111 = 224 bytes [Channel 1] 000 = 0 byte 001 = 8 bytes 010 = 16 bytes 011 = 24 bytes 100 = 32 bytes 101 = 40 bytes 110 = 48 bytes 111 = 56 bytes [Channel 2, 3] 000 = 0 byte 001 = 2 bytes 010 = 4 bytes 011 = 6 bytes 100 = 8 bytes 101 = 10 bytes 110 = 12 bytes 111 = 14 bytes	000
Reserved	[7]	Reserved	0
Rx FIFO Trigger Level	[6:4]	Determines the trigger level of Rx FIFO. If data count of Rx FIFO is more than or equal to the trigger level, Rx interrupt occurs. [Channel 0] 000 = 32 byte 001 = 64 bytes 010 = 96 bytes 011 = 128 bytes 100 = 160 bytes 101 = 192 bytes 110 = 224 bytes 111 = 256 bytes [Channel 1] 000 = 8 byte 001 = 16 bytes 010 = 24 bytes 011 = 32 bytes 100 = 40 bytes 101 = 48 bytes 110 = 56 bytes 111 = 64 bytes	000

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UFCONn	Bit	Description	Initial State
		[Channel 2, 3] 000 = 2 byte 001 = 4 bytes 010 = 6 bytes 011 = 8 bytes 100 = 10 bytes 101 = 12 bytes 110 = 14 bytes 111 = 16 bytes	
Reserved	[3]	-	0
Tx FIFO Reset	[2]	Auto-clears after resetting FIFO 0 = Normal 1 = Tx FIFO reset	0
Rx FIFO Reset	[1]	Auto-clears after resetting FIFO 0 = Normal 1 = Rx FIFO reset	0
FIFO Enable	[0]	0 = Disables 1 = Enables	0

NOTE: If the UART does not reach the FIFO trigger level and does not receive data during 3 word time in DMA receive mode with FIFO, the Rx interrupt will be generated (receive time out). You must check the FIFO status and read out the rest

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1.6.1.4 UART Modem Control Register

- UMCON0, R/W, Address = 0xE290_000C
- UMCON1, R/W, Address = 0xE290_040C
- UMCON2, R/W, Address = 0xE290_080C
- Reserved (Address = 0xE290_0C0C)

There are three UART MODEM control registers in the UART block, namely, UMCON0, UMCON1 and UMCON2.

UMCONn	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
RTS trigger Level	[7:5]	Determines the trigger level of Rx FIFO to control nRTS signal. If AFC bit is enabled and Rx FIFO have bytes that are greater than or equal to the trigger level, nRTS signal is deactivated. [Channel 0] 000 = 255 bytes 001 = 224 bytes 010 = 192 bytes 011 = 160 bytes 100 = 128 bytes 101 = 96 bytes 110 = 64 bytes 111 = 32 bytes [Channel 1] 000 = 63 bytes 001 = 56 bytes 010 = 48 bytes 011 = 40 bytes 100 = 32 bytes 101 = 24 bytes 110 = 16 bytes 111 = 8 bytes [Channel 2] 000 = 15 bytes 001 = 14 bytes 010 = 12 bytes 011 = 10 bytes 100 = 8 bytes 101 = 6 bytes 110 = 4 bytes 111 = 2 bytes	000
Auto Flow Control (AFC)	[4]	0 = Disables 1 = Enables	0
Modem Interrupt Enable	[3]	0 = Disables 1 = Enables	0
Reserved	[2:1]	These bits must be 0	00
Request to Send	[0]	If AFC bit is enabled, this value will be ignored. In this case the S5PV210 controls nRTS signals automatically. If AFC bit is disabled, the software must control nRTS signal. 0 = 'H' level (Inactivate nRTS) 1 = 'L' level (Activate nRTS)	0

NOTE: UART 2 supports AFC function, if nRxD3 and nTxD3 are set as nRTS2 and nCTS2 by GPA1CON. UART 3 does not support AFC function, because the S5PV210 has no nRTS3 and nCTS3.

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1.6.1.5 UART Tx/Rx Status Register

- UTRSTAT0, R, Address = 0xE290_0010
- UTRSTAT1, R, Address = 0xE290_0410
- UTRSTAT2, R, Address = 0xE290_0810
- UTRSTAT3, R, Address = 0xE290_0C10

There are four UART Tx/Rx status registers in the UART block, namely, UTRSTAT0, UTRSTAT1, UTRSTAT2 and UTRSTAT3.

UTRSTATn	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
Transmitter empty	[2]	This bit is automatically set to 1 if the transmit buffer register has no valid data to transmit, and the transmit shift register is empty. 0 = Not empty 1 = Transmitter (which includes transmit buffer and shifter register) empty	1
Transmit buffer empty	[1]	This bit is automatically set to 1 if transmit buffer register is empty. 0 = Buffer register is not empty 1 = Buffer register is empty (In Non-FIFO mode, Interrupt or DMA is requested. In FIFO mode, Interrupt or DMA is requested, if Tx FIFO Trigger Level is set to 00 (Empty)) If UART uses FIFO, check Tx FIFO Count bits and Tx FIFO Full bit in UFSTAT register instead of this bit.	1
Receive buffer data ready	[0]	This bit is automatically set to 1 if receive buffer register contains valid data, received over the RXDn port. 0 = Buffer register is empty 1 = Buffer register has a received data (In Non-FIFO mode, Interrupt or DMA is requested) If UART uses the FIFO, check Rx FIFO Count bits and Rx FIFO Full bit in UFSTAT register instead of this bit.	0

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1.6.1.6 UART Error Status Register

- UERSTAT0, R, Address = 0xE290_0014
- UERSTAT1, R, Address = 0xE290_0414
- UERSTAT2, R, Address = 0xE290_0814
- UERSTAT3, R, Address = 0xE290_0C14

There are four UART Rx error status registers in the UART block, namely, UERSTAT0, UERSTAT1, UERSTAT2 and UERSTAT3.

UERSTATn	Bit	Description	Initial State
Reserved	[31:4]	Reserved	0
Break Detect	[3]	This bit is automatically set to 1 to indicate that a break signal has been received. 0 = No break signal is received 1 = Break signal is received (Interrupt is requested.)	0
Frame Error	[2]	This bit is automatically set to 1 if a frame error occurs during the receive operation. 0 = No frame error occurs during the receive operation 1 = Frame error occurs (Interrupt is requested.) during the receive operation	0
Parity Error	[1]	This bit is automatically set to 1 if a parity error occurs during the receive operation. 0 = No parity error occurs during receive the receive operation 1 = Parity error occurs (Interrupt is requested.) the receive operation	0
Overrun Error	[0]	This bit is automatically set to 1 automatically if an overrun error occurs during the receive operation. 0 = No overrun error occurs during the receive operation 1 = Overrun error occurs (Interrupt is requested.) during the receive operation	0

NOTE: These bits (UERSATn[3:0]) are automatically cleared to 0 if UART error status register is read

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1.6.1.7 Uart FIFO Status Register

- UFSTAT0, R, Address = 0xE290_0018
- UFSTAT1, R, Address = 0xE290_0418
- UFSTAT2, R, Address = 0xE290_0818

UFSTAT3, R, Address = 0xE290_0C18 There are four UART FIFO status registers in the UART block, namely, UFSTAT0, UFSTAT1, UFSTAT2 and UFSTAT3

UFSTATn	Bit	Description	Initial State
Reserved	[31:25]	Reserved	0
Tx FIFO Full	[24]	This bit is automatically set to 1 if the transmitted FIFO is full during transmit operation 0 = Not full 1 = Full	0
Tx FIFO Count	[23:16]	Number of data in Tx FIFO	0
Reserved	[15:10]	-	0
Rx FIFO Error	[9]	This bit is set to 1 if Rx FIFO contains invalid data which results from frame error, parity error, or break signal.	0
Rx FIFO Full	[8]	This bit is automatically set to 1 if the received FIFO is full during receive operation 0 = Not full 1 = Full	0
Rx FIFO Count	[7:0]	Number of data in Rx FIFO	0

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1.6.1.8 Uart Modem Status Register

- UMSTAT0, R, Address = 0xE290_001C
- UMSTAT1, R, Address = 0xE290_041C
- UMSTAT2, R, Address = 0xE290_081C
- Reserved, Address = 0xE290_0C1C

There are three UART modem status registers in the UART block, namely, UMSTAT0, UMSTAT1 and UMSTAT2.

UMSTAT0	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
Delta CTS	[4]	This bit indicates that the nCTS input to the S5PV210 has changed its state since the last time it was read by CPU. (Refer *Figure 1-9*) 0 = Has not changed 1 = Has changed	0
Reserved	[3:1]	Reserved	00
Clear to Send	[0]	0 = CTS signal is not activated (nCTS pin is high) 1 = CTS signal is activated (nCTS pin is low)	0

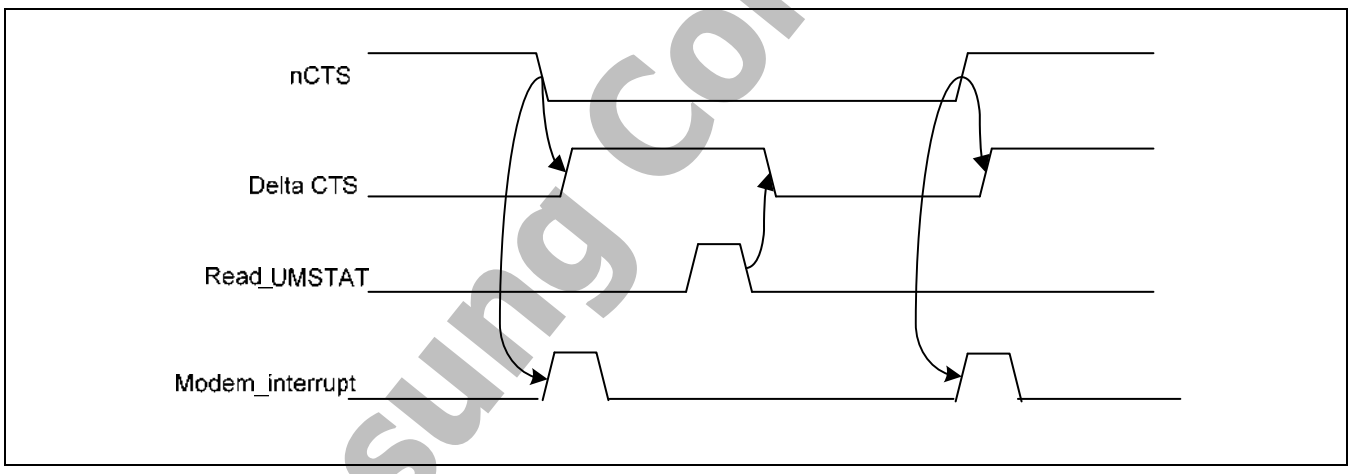

Figure 1-9 nCTS and Delta CTS Timing Diagram

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1.6.1.9 UART Transmit Buffer Register (Holding Register & FIFO Register)

- UTXH0, W, Address = 0xE290_0020
- UTXH1, W, Address = 0xE290_0420
- UTXH2, W, Address = 0xE290_0820
- UTXH3, W, Address = 0xE290_0C20

There are four UART transmit buffer registers in the UART block, namely, UTXH0, UTXH1, UTXH2 and UTXH3. UTXHn contains 8-bit data for transmission data.

UTXHn	Bit	Description	Initial State
Reserved	[31:8]	Reserved	-
UTXHn	[7:0]	Transmit data for UARTn	-

1.6.1.10 UART Recive Buffer Register (Holding Register & FIFO Register)

- URXH0, R, Address = 0xE290_0024
- URXH1, R, Address = 0xE290_0424
- URXH2, R, Address = 0xE290_0824
- URXH3, R, Address = 0xE290_0C24

There are four UART receive buffer registers in the UART block, namely, URXH0, URXH1, URXH2 and URXH3. URXHn contains 8-bit data for received data.

URXHn	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
URXHn	[7:0]	Receive data for UARTn	0x00

NOTE: If an overrun error occurs, the URXHn must be read. If not, the next received data makes an overrun error, even though the overrun bit of UERSTATn had been cleared.

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1.6.1.11 UART Channel Baud Rate Division Register

- UBRDIV0, R/W, Address = 0xE290_0028
- UBRDIV1, R/W, Address = 0xE290_0428
- UBRDIV2, R/W, Address = 0xE290_0828
- UBRDIV3, R/W, Address = 0xE290_0C28

UBRDIV n	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
UBRDIVn	[15:0]	Baud rate division value (When UART clock source is PCLK, UBRDIVn must be more than 0 (UBRDIVn >0))	0x0000

NOTE: If UBRDIV value is 0, UART baudrate is not affected by UDIVSLOT value.

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1.6.1.12 UART Channel Dividing Slot Register

- UDIVSLOT0, R/W, Address = 0xE290_002C
- UDIVSLOT1, R/W, Address = 0xE290_042C
- UDIVSLOT2, R/W, Address = 0xE290_082C
- UDIVSLOT3, R/W, Address = 0xE290_0C2C

UDIVSLOT n	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
UDIVSLOTn	[15:0]	Select the slot where clock generator divide clock source	0x0000

1. **UART Baud Rate Configuration**
   There are four UART baud rate divisor registers in the UART block, namely, UBRDIV0, UBRDIV1, UBRDIV2 and UBRDIV3.
   The value stored in the baud rate divisor register (UBRDIVn) and dividing slot register(UDIVSLOTn) is used to determine the serial Tx/Rx clock rate (baud rate) as follows:

   DIV_VAL = UBRDIVn + (num of 1's in UDIVSLOTn)/16
   DIV_VAL = (PCLK / (bps x 16)) –1
   or
   DIV_VAL = (SCLK_UART / (bps x 16)) –1

   Where, the divisor should be from 1 to (216-1).

   Using UDIVSLOT, you can generate the baud rate more accurately.

   For example, if the baud-rate is 115200 bps and SCLK_UART is 40 MHz, UBRDIVn and UDIVSLOTn are:

   DIV_VAL = (40000000 / (115200 x 16)) -1
   = 21.7 -1
   = 20.7

   UBRDIVn = 20 (integer part of DIV_VAL)
   (num of 1's in UDIVSLOTn)/16 = 0.7
   then, (num of 1's in UDIVSLOTn) = 11
   so, UDIVSLOTn can be 16'b1110_1110_1110_1010 or 16'b0111_0111_0111_0101, etc.

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It is recommended to select UDIVSLOTn as described in the following table:

Num of 1's	UDIVSLOTn	Num of 1's	UDIVSLOTn
0	0x0000(0000_0000_0000_0000b)	8	0x5555(0101_0101_0101_0101b)
1	0x0080(0000_0000_0000_1000b)	9	0xD555(1101_0101_0101_0101b)
2	0x0808(0000_1000_0000_1000b)	10	0xD5D5(1101_0101_1101_0101b)
3	0x0888(0000_1000_1000_1000b)	11	0xDDD5(1101_1101_1101_0101b)
4	0x2222(0010_0010_0010_0010b)	12	0xDDDD(1101_1101_1101_1101b)
5	0x4924(0100_1001_0010_0100b)	13	0xDFDD(1101_1111_1101_1101b)
6	0x4A52(0100_1010_0101_0010b)	14	0xDFDF(1101_1111_1101_1111b)
7	0x54AA(0101_0100_1010_1010b)	15	0xFFDF(1111_1111_1101_1111b)

2. Baud Rate Error Tolerance

UART Frame error should be less than 1.87%(3/160)

tUPCLK = (UBRDIVn + 1) x 16 x 1Frame / (PCLK or SCLK_UART) tUPCLK: Real UART Clock
tEXTUARTCLK = 1Frame / baud-rate tEXTUARTCLK: Ideal UART Clock

UART error = (tUPCLK – tEXTUARTCLK) / tEXTUARTCLK x 100%

1Frame = start bit + data bit + parity bit + stop bit.

3. UART Clock and PCLK Relation

There is a constraint on the ratio of clock frequencies for PCLK to UARTCLK.

The frequency of UARTCLK must be no more than 5.5/3 times faster than the frequency of PCLK:

FUARTCLK <= 5.5/3 X FPCLK **FUARTCLK = baudrate x 16**

This allows sufficient time to write the received data to the receive FIFO

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1.6.1.13 UART Interrupt Pending Register

- UINTP0, R/W, Address = 0xE290_0030
- UINTP1, R/W, Address = 0xE290_0430
- UINTP2, R/W, Address = 0xE290_0830
- UINTP3, R/W, Address = 0xE290_0C30

Interrupt pending register contains the information of the interrupts that are generated.

UINTPn	Bit	Description	Initial State
Reserved	[31:4]	Reserved	0
MODEM	[3]	Generates Modem interrupt.	0
TXD	[2]	Generates Transmit interrupt.	0
ERROR	[1]	Generates Error interrupt.	0
RXD	[0]	Generates Receive interrupt.	0

If one of above 4 bits is logical high ('1'), each UART channel generates interrupt.

This register must be cleared in the interrupt service routine after clearing interrupt pending register in Interrupt Controller (INTC). Clear specific bits of UINTP register by writing 1's to the bits that you want to clear.

1.6.1.14 UART Interrupt Source Pending Register

- UINTSP0, R/W, Address = 0xE290_0034
- UINTSP1, R/W, Address = 0xE290_0434
- UINTSP2, R/W, Address = 0xE290_0834
- UINTSP3, R/W, Address = 0xE290_0C34

Interrupt Source Pending Register contains the information of the interrupt that are generated regardless of the value of Interrupt Mask Register

UINTSPn	Bit	Description	Initial State
Reserved	[31:4]	Reserved	0
MODEM	[3]	Generates Modem interrupt.	0
TXD	[2]	Generates Transmit interrupt.	0
ERROR	[1]	Generates Error interrupt.	0
RXD	[0]	Generates Receive interrupt.	0

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1.6.1.15 UART Interrupt Mask Register

- UINTM0, R/W, Address = 0xE290_0038
- UINTM1, R/W, Address = 0xE290_0438
- UINTM2, R/W, Address = 0xE290_0838
- UINTM3, R/W, Address = 0xE290_0C38

Interrupt mask register contains the information about which interrupt source is masked. If a specific bit is set to 1, interrupt request signal to the Interrupt Controller is not generated even though corresponding interrupt is generated. (**Note:** Even in such a case, the corresponding bit of UINTSPn register is set to 1). If the mask bit is 0, the interrupt requests are serviced from the corresponding interrupt source.

UINTMn	Bit	Description	Initial State
Reserved	[31:4]	Reserved	0
MODEM	[3]	Mask Modem interrupt.	0
TXD	[2]	Mask Transmit interrupt.	0
ERROR	[1]	Mask Error interrupt.	0
RXD	[0]	Mask Receive interrupt.	0

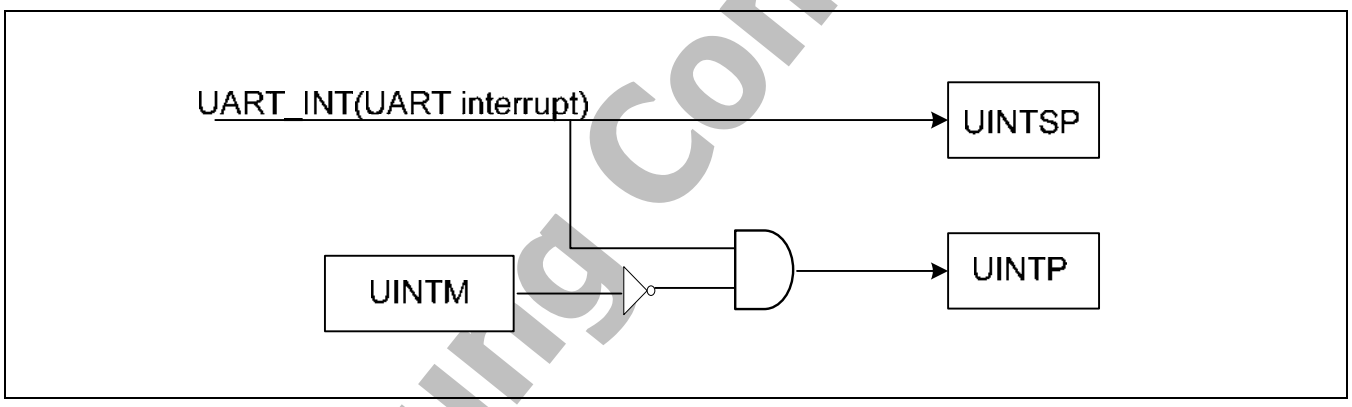

Figure 1-10 Block diagram of UINTSP, UINTP and UINTM

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2 IIC-BUS INTERFACE

2.1 OVERVIEW OF IIC-BUS INTERFACE

The S5PV210 RISC microprocessor supports four multi-master I^2C bus serial interfaces. To carry information between bus masters and peripheral devices connected to the I^2C bus, a dedicated Serial Data Line (SDA) and an Serial Clock Line (SCL) is used. Both SDA and SCL lines are bi-directional.

In multi-master I^2C-bus mode, multiple S5PV210 RISC microprocessors receive or transmit serial data to or from slave devices. The master S5PV210 initiates and terminates a data transfer over the I^2C bus. The I^2C bus in the S5PV210 uses a standard bus arbitration procedure.

To control multi-master I^2C-bus operations, values must be written to the following registers:

- Multi-master I^2C-bus control register- I2CCON
- Multi-master I^2C-bus control/status register- I2CSTAT
- Multi-master I^2C-bus Tx/Rx data shift register- I2CDS
- Multi-master I^2C-bus address register- I2CADD

If the I^2C-bus is free, both SDA and SCL lines should be both at High level. A High-to-Low transition of SDA initiates a Start condition. A Low-to-High transition of SDA initiates a Stop condition while SCL remains steady at High Level.

The master device always generates Start and Stop conditions. First 7-bit address value in the data byte that is transferred via SDA line after the Start condition has been initiated, can determine the slave device which the bus master device has selected. The 8th bit determines the direction of the transfer (read or write).

Every data byte put onto the SDA line should be eight bits in total. There is no limit to send or receive bytes during the bus transfer operation. Data is always sent from most-significant bit (MSB) first, and every byte should be immediately followed by acknowledge (ACK) bit.

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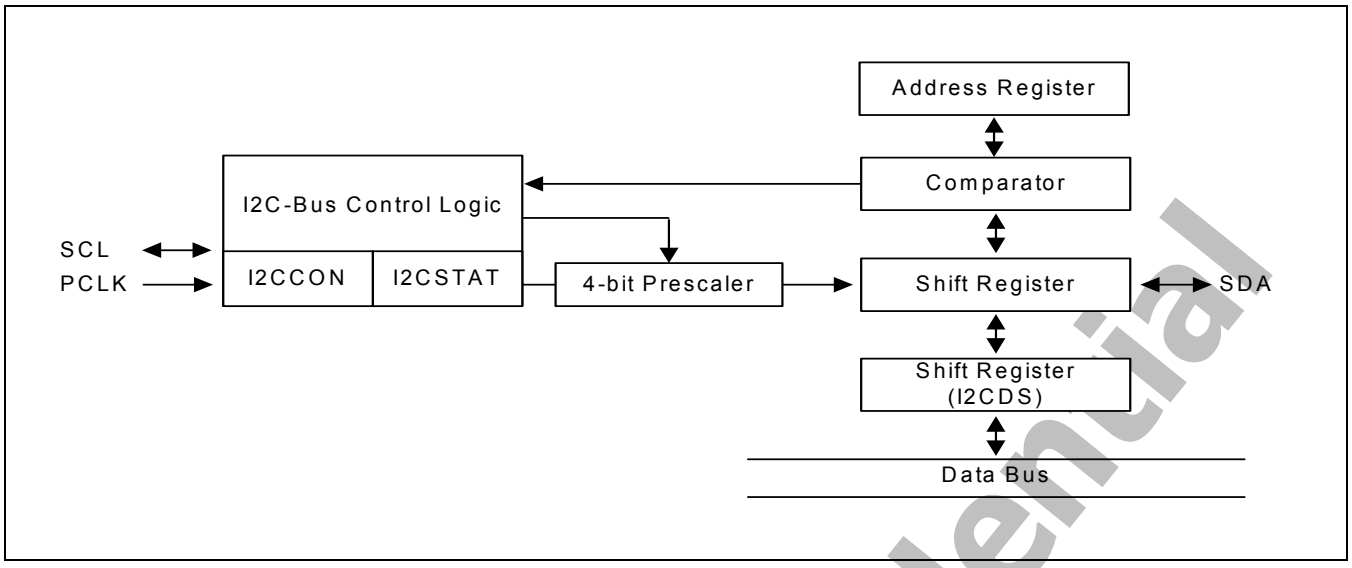

Figure 2-1 I²C-Bus Block Diagram

2.2 KEY FEATURES OF IIC-BUS INTEFACE

- Four channel Multi-Master, Slave I²C BUS interfaces
  (One channel for HDMI PHY is internally connected. Three channels can be used for general purpose. However, if the user wants to use HDMI, it is recommended to allocate one channel for HDMI use only among three channels)
- 7-bit addressing mode
- Serial, 8-bit oriented, and bidirectional data transfer
- Supports up to 100kbit/s in the Standard mode
- Supports up to 400kbit/s in the Fast mode.
- Supports master transmit, master receive, slave transmit and slave receive operation
- Supports interrupt or polling events.

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2.3 I²C-BUS INTERFACE OPERATION

The S5PV210 I²C-bus interface has four operation modes, namely:

- Master Transmitter Mode
- Master Receive Mode
- Slave Transmitter Mode
- Slave Receive Mode

The functional relationships among these operating modes are described below.

2.3.1 START AND STOP CONDITIONS

If the I²C-bus interface is inactive, it is usually in Slave mode. In other words, the interface should be in Slave mode before detecting a Start condition on the SDA line (a Start condition is initiated with a High-to-Low transition of the SDA line while the clock signal of SCL is High). If the interface state is changed to Master mode, SDA line initiates data transfer and generates SCL signal.

A Start condition transfers one-byte serial data via SDA line, and a Stop condition terminates the data transfer. A Stop condition is a Low-to-High transition of the SDA line while SCL is High. The master generates Start and Stop conditions. The I²C-bus gets busy if a Start condition is generated. On the other hand, a Stop condition frees the I²C-bus.

If a master initiates a Start condition, it should send a slave address to notify the slave device. One byte of address field consists of a 7-bit address and a 1-bit transfer direction indicator (that shows write or read).
If bit 8 is 0, it indicates a write operation (Transmit Operation); if bit 8 is 1, it indicates a request for data read (Receive Operation).

The master transmits Stop condition to complete the transfer operation. If the master wants to continue the data transmission to the bus, it should generate another Start condition as well as a slave address. In this way, the read-write operation is performed in various formats.

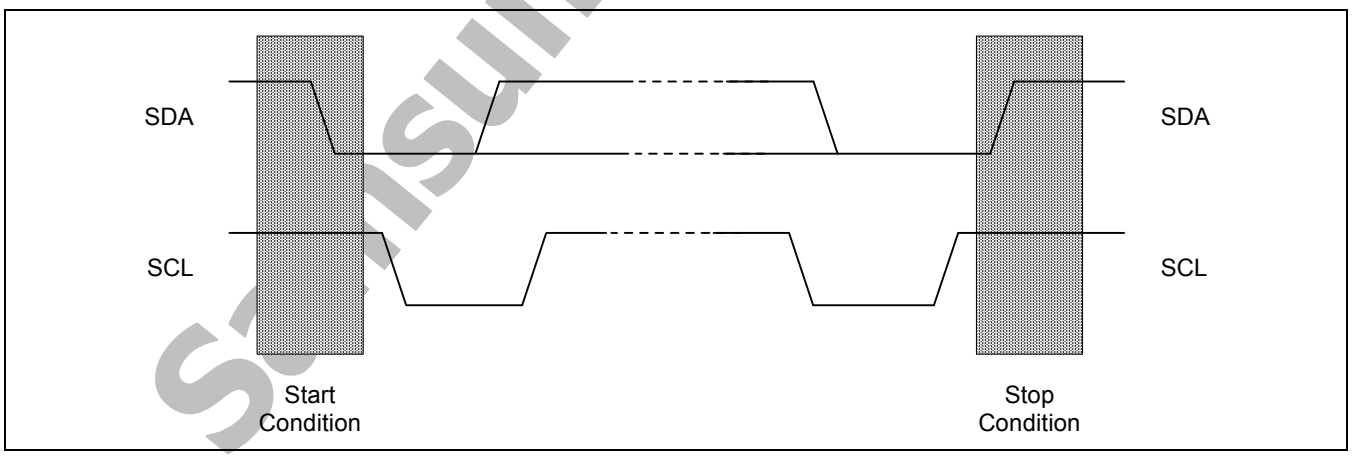

Figure 2-2 Start and Stop Condition

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2.3.2 DATA TRANSFER FORMAT

Every byte placed on the SDA line should be eight bits in length. There is no limit to transmit bytes per transfer. The first byte following a Start condition should have the address field. If the I²C-bus is operating in Master mode, master transmits the address field. Each byte should be followed by an acknowledgement (ACK) bit. The MSB bit of the serial data and addresses are sent first.

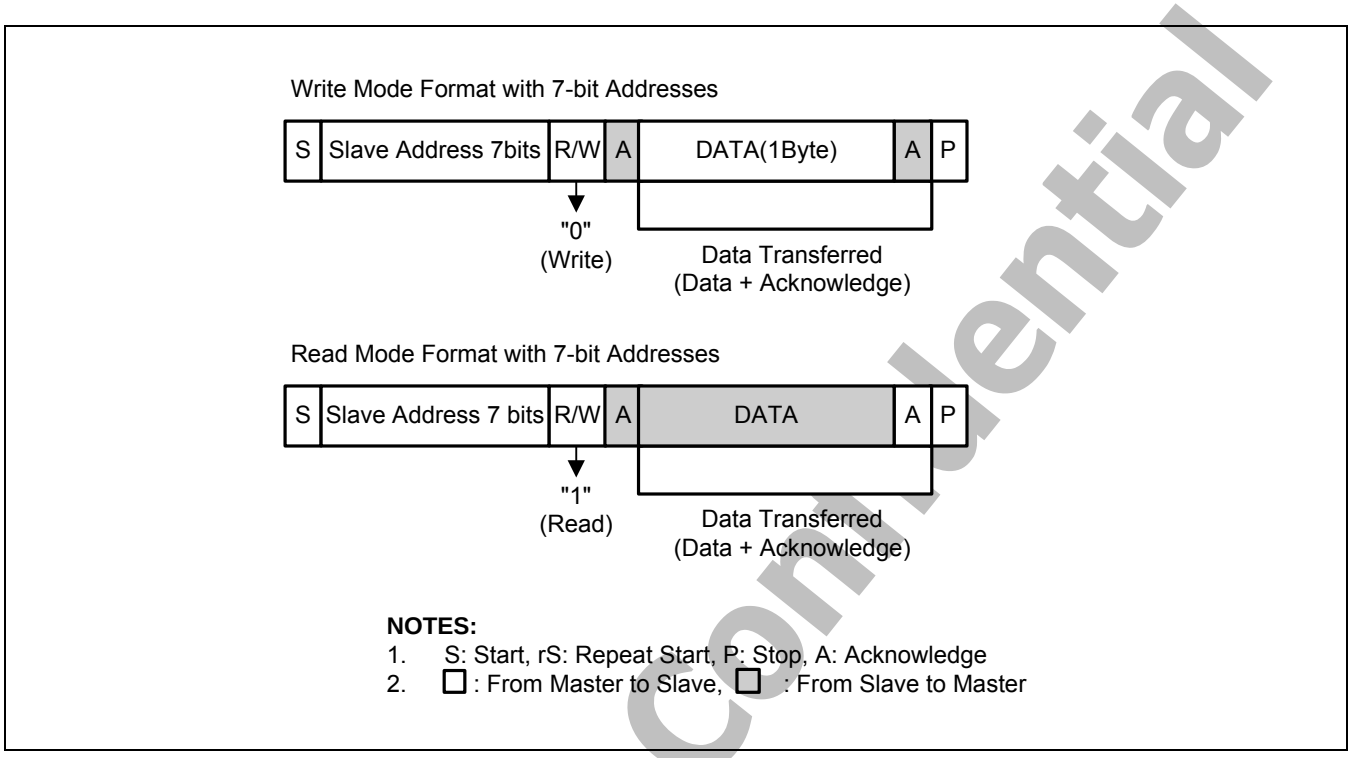

Figure 2-3 I²C-Bus Interface Data Format

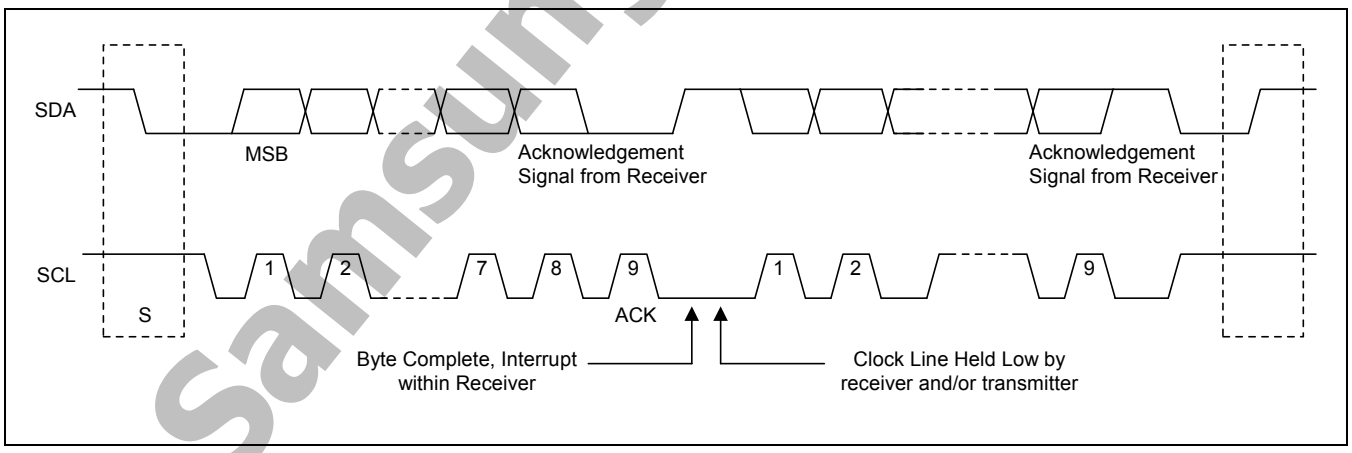

Figure 2-4 Data Transfer on the I²C-Bus

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2.3.3 ACK SIGNAL TRANSMISSION

To complete a one-byte transfer operation, the receiver sends an ACK bit to the transmitter. The ACK pulse occurs at the ninth clock of the SCL line. Eight clocks are required for the one-byte data transfer. The master generates clock pulse required to transmit the ACK bit.

The transmitter sets the SDA line to High to release the SDA line if the ACK clock pulse is received. The receiver drives the SDA line Low during the ACK clock pulse so that the SDA keeps Low during the High period of the ninth SCL pulse. The software (I2CSTAT) enables or disables ACK bit transmit function. However, the ACK pulse on the ninth clock of SCL is required to complete the one-byte data transfer operation.

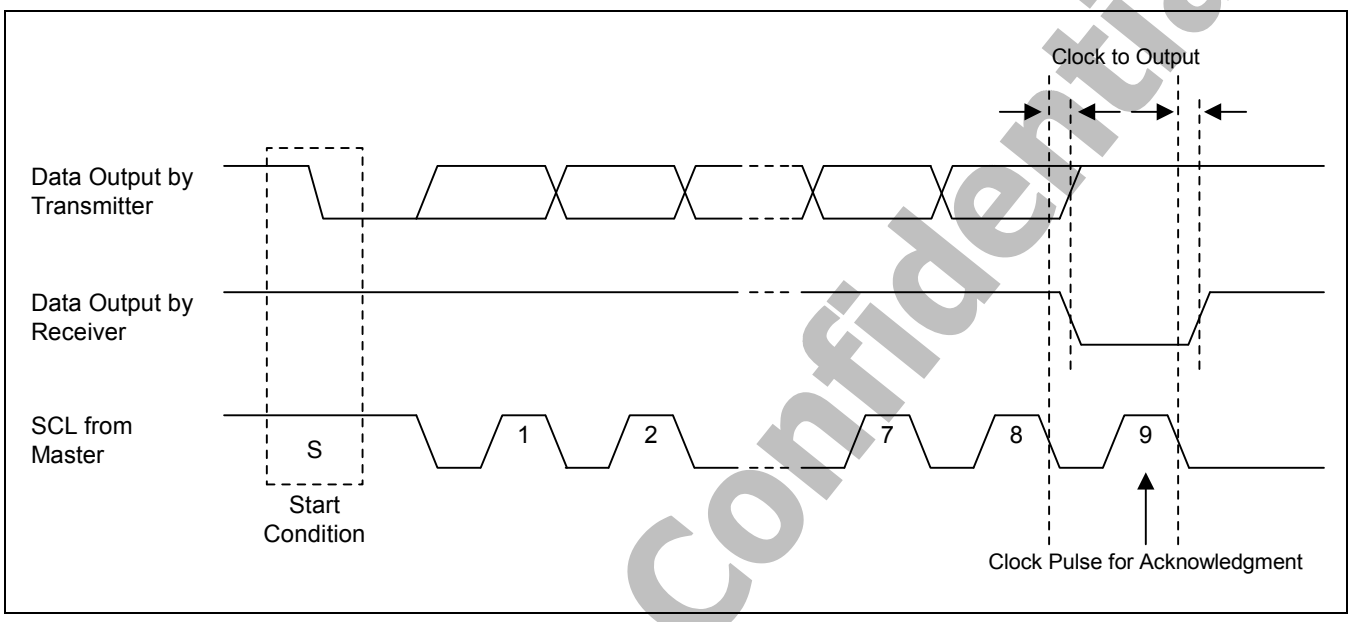

Figure 2-5 Acknowledge on the I2C-Bus

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2.3.4 READ-WRITE OPERATION

In data is transmitted in Transmitter mode, the I^{2}C-bus interface waits until I^{2}C-bus Data Shift (I2CDS) register receives the new data. Before the new data is written to the register, the SCL line is held low. The line is only released after the data has been written. S5PV210 holds the interrupt to identify the completion of current data transfer. After the CPU receives the interrupt request, it writes new data to the I2CDS register again.

If data is received in Receive mode, the I^{2}C-bus interface waits until I2CDS register is read. Before the new data is read out, the SCL line is held low. The line is only released after the data has been read. S5PV210 holds the interrupt to identify the completion of new data reception. After the CPU receives the interrupt request, it reads the data from the I2CDS register.

2.3.5 BUS ARBITRATION PROCEDURES

Arbitration takes place on the SDA line to prevent the contention on the bus between two masters. If a master with a SDA High level detects other master with a SDA active Low level, it does not initiate a data transfer because the current level on the bus does not correspond to its own. The arbitration procedure extends until the SDA line turns High.

If the masters lower the SDA line simultaneously, each master evaluates whether the mastership is allocated itself or not. For the purpose of evaluation each master detects the address bits. While each master generates the slave address, it detects the address bit on the SDA line because the SDA line is likely to get Low rather than high.

Assume that one master generates a Low as first address bit, while the other master is maintaining High. In this case, both masters detect Low on the bus because the Low status is superior to the High status in power. If this happens, Low (as the first bit of address) generating master gets the mastership while High (as the first bit of address) generating master withdraws the mastership. If both masters generate Low as the first bit of address, there is arbitration for the second address bit again. This arbitration continues to the end of last address bit.

2.3.6 ABORT CONDITIONS

If a slave receiver cannot acknowledge the confirmation of the slave address, it holds the level of the SDA line High. In this case, the master generates a Stop condition and cancels the transfer.

If a master receiver is involved in the aborted transfer, it signals the end of slave transmit operation by canceling the generation of an ACK after the last data byte received from the slave. The slave transmitter releases the SDA to allow a master to generate a Stop condition.

2.3.7 CONFIGURING I^{2}C-BUS

To control the frequency of the serial clock (SCL), the 4-bit prescaler value is programmed in the I2CCON register. The I^{2}C-bus interface address is stored in the I^{2}C-bus address (I2CADD) register (By default, the I^{2}C-bus interface address has an unknown value).

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2.3.8 FLOWCHARTS OF OPERATIONS IN EACH MODE

Following steps must be executed before any I^2C Tx/Rx operations:

1. If required, write own slave address on I2CADD register.
2. Set I2CCON register.
   a) Enable interrupt
   b) Define SCL period
3. Set I2CSTAT to enable Serial Output

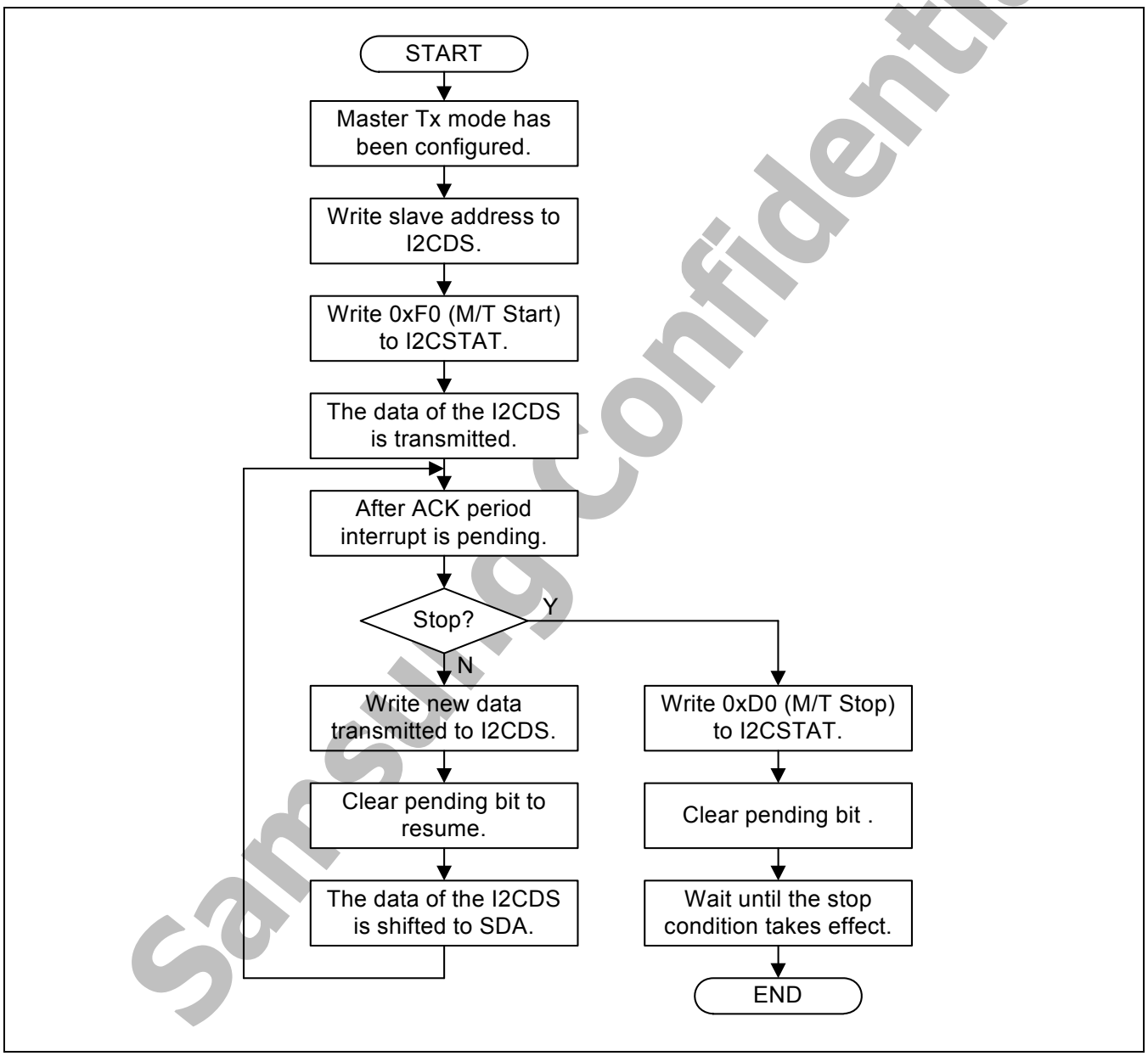

Figure 2-6 Operations for Master/Transmitter Mode

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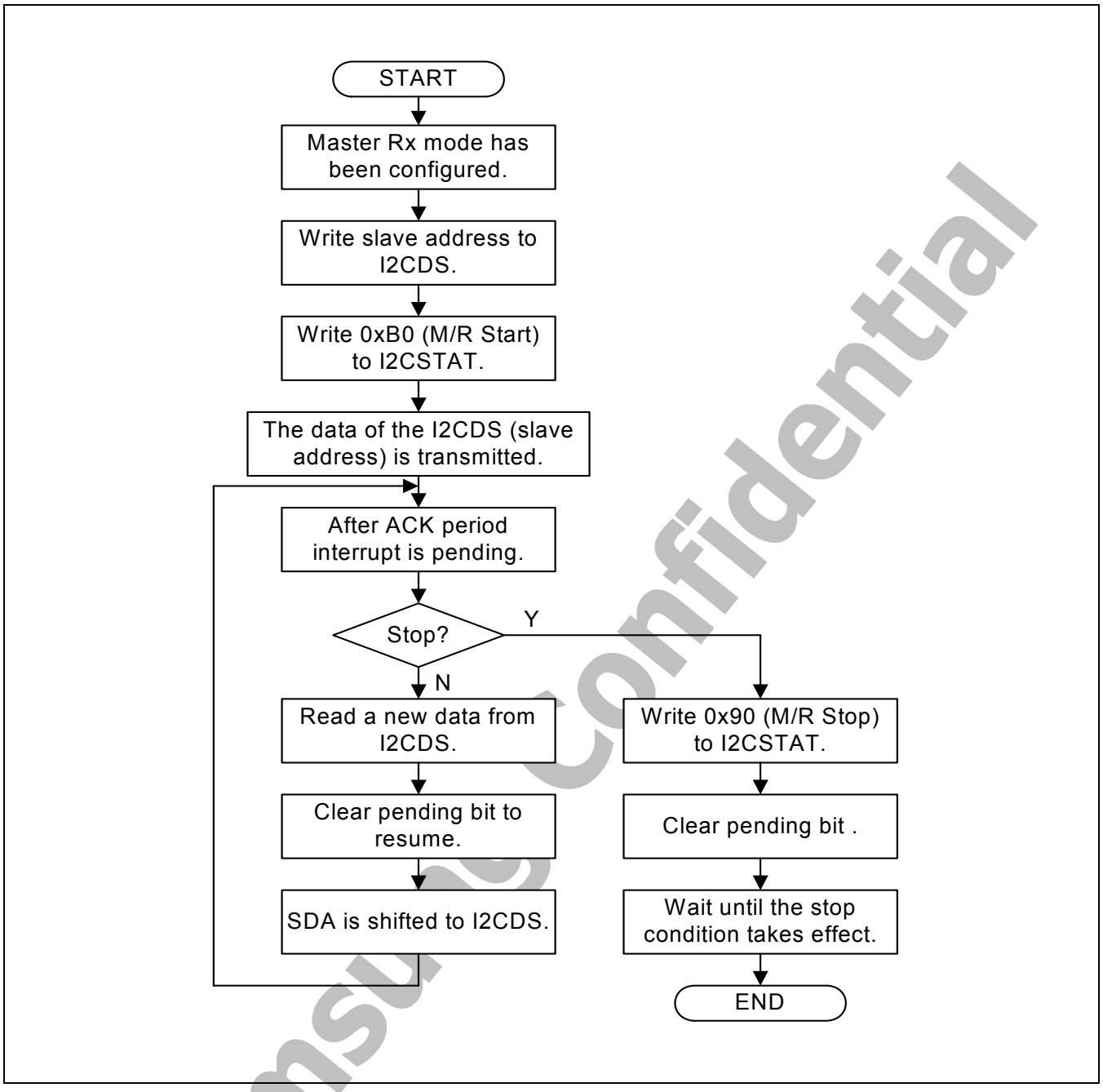

Figure 2-7 Operations for Master/ Receiver Mode

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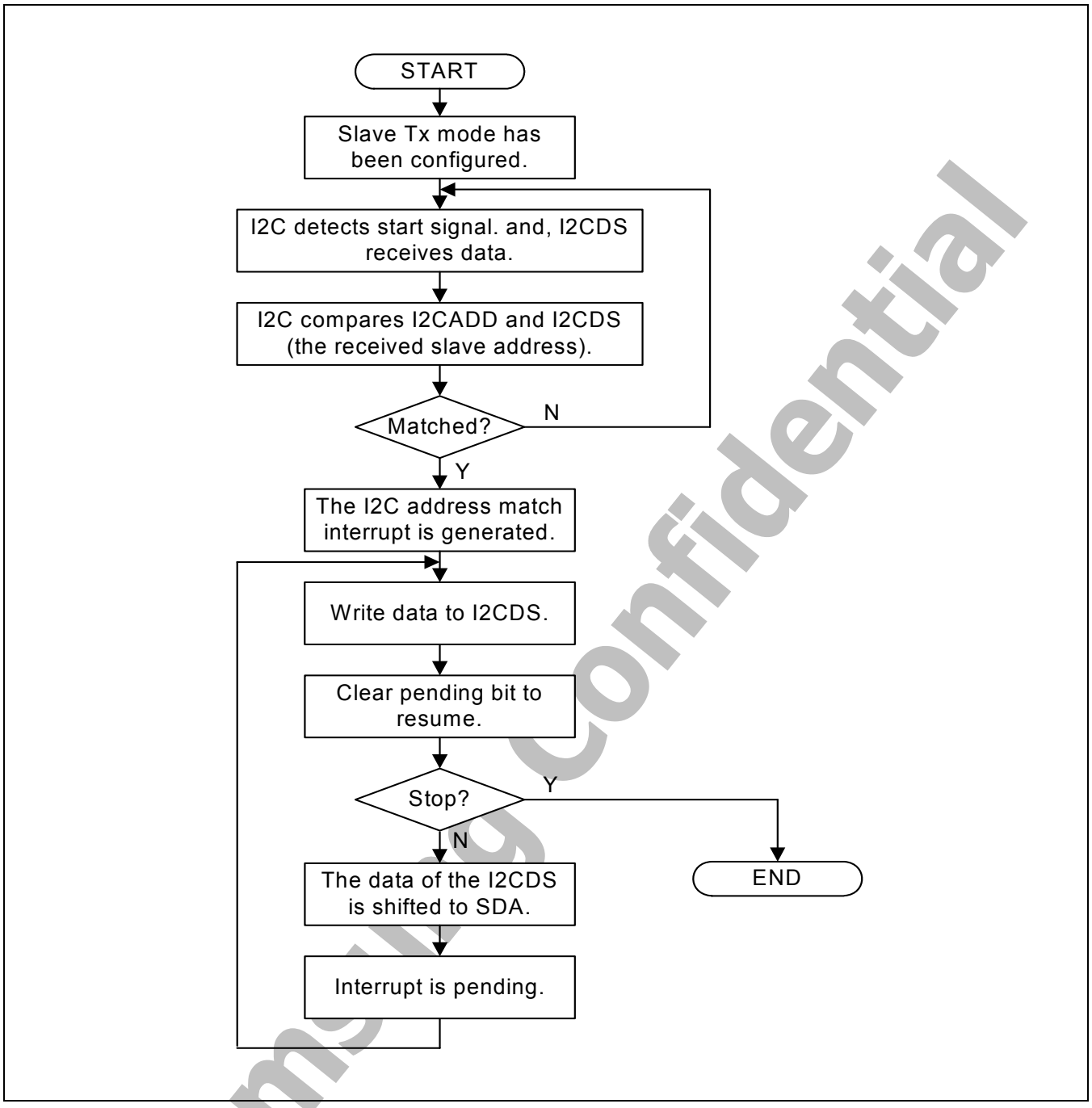

Figure 2-8 Operations for Slave/ Transmitter Mode

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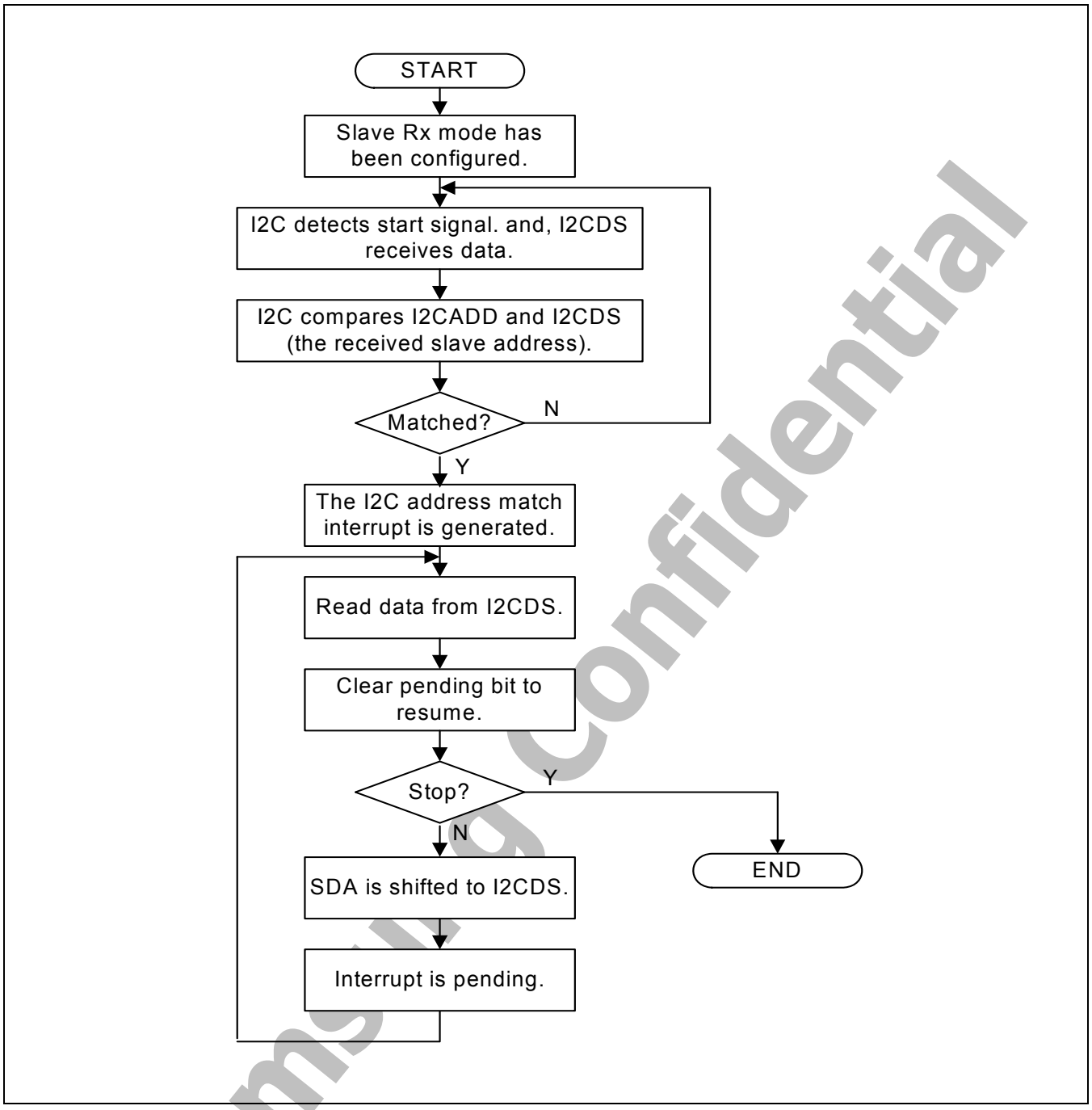

Figure 2-9 Operations for Slave/Receiver Mode

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2.4 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
I2C0_SCL	Input/Output	I^2C-Bus Interface0 Serial Clock Line	Xi2c0SCL	muxed
I2C0_SDA	Input/Output	I^2C-Bus Interface0 Serial Data Line	Xi2c0SDA	muxed
I2C2_SCL	Input/Output	I^2C-BUS Interface2 Serial Clock Line	Xi2c2SCL	muxed
I2C2_SDA	Input/Output	I^2C-BUS Interface2 Serial Data Line	Xi2c2SDA	muxed
I2C_HDMI_DDC_SCL	Input/Output	I^2C-BUS Interface for HDMI DDC Serial Clock Line	Xi2c1SCL	muxed
I2C_HDMI_DDC_SDA	Input/Output	I^2C-BUS Interface for HDMI DDC Serial Data Line	Xi2c1SDA	muxed

NOTE: I^2C-BUS Interface for HDMI PHY is internally connected.

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2.5 REGISTER DESCRIPTION

2.5.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
I2CCON0	0xE180_0000	R/W	Specifies the I2C-Bus Interface0 control register	0x0X
I2CSTAT0	0xE180_0004	R/W	Specifies the I2C-Bus Interface0 control/status register	0x00
I2CADD0	0xE180_0008	R/W	Specifies the I2C-Bus Interface0address register	0xXX
I2CDS0	0xE180_000C	R/W	Specifies the I2C-Bus Interface0transmit/receive data shift register	0xXX
I2CLC0	0xE180_0010	R/W	Specifies the I2C-Bus Interface0multi-master line control register	0x00
I2CCON2	0xE1A0_0000	R/W	Specifies the I2C-Bus Interface2 control register	0x0X
I2CSTAT2	0xE1A0_0004	R/W	Specifies the I2C-Bus Interface2 control/status register	0x00
I2CADD2	0xE1A0_0008	R/W	Specifies the I2C-Bus Interface2 address register	0xXX
I2CDS2	0xE1A0_000C	R/W	Specifies the I2C-Bus Interface2 transmit/receive data shift register	0xXX
I2CLC2	0xE1A0_0010	R/W	Specifies the I2C-Bus Interface2 multi-master line control register	0x00
I2CCON_HDMI_DDC	0xFAB0_0000	R/W	Specifies the I2C-Bus Interface for HDMI DDC control register	0x0X
I2CSTAT_HDMI_DDC	0xFAB0_0004	R/W	Specifies the I2C-Bus Interface for HDMI DDC control/status register	0x00
I2CADD_HDMI_DDC	0xFAB0_0008	R/W	Specifies the I2C-Bus Interface for HDMI DDC address register	0xXX
I2CDS_HDMI_DDC	0xFAB0_000C	R/W	Specifies the I2C-Bus Interface for HDMI DDC transmit/receive data shift register	0xXX
I2CLC_HDMI_DDC	0xFAB0_0010	R/W	Specifies the I2C-Bus Interface for HDMI DDC multi-master line control register	0x00
I2CCON_HDMI_PHY	0xFA90_0000	R/W	Specifies the I2C-Bus Interface for HDMI PHY control register	0x0X
I2CSTAT_HDMI_PHY	0xFA90_0004	R/W	Specifies the I2C-Bus Interface for HDMI PHY control/status register	0x00
I2CADD_HDMI_PHY	0xFA90_0008	R/W	Specifies the I2C-Bus Interface for HDMI PHY address register	0xXX
I2CDS_HDMI_PHY	0xFA90_000C	R/W	Specifies the I2C-Bus Interface for HDMI PHY transmit/receive data shift register	0xXX
I2CLC_HDMI_PHY	0xFA90_0010	R/W	Specifies the I2C-Bus Interface for HDMI PHY multi-master line control register	0x00

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2.5.1.1 MULTI-MASTER I²C-Bus Control Register

- I2CCON0, R/W, Address = 0xE180_0000
- I2CCON2, R/W, Address = 0xE1A0_0000
- I2CCON_HDMI_DDC, R/W, Address = 0xFAB0_0000
- I2CCON_HDMI_PHY, R/W, Address = 0xFA90_0000

I2CCON	Bit	Description	Initial State
Acknowledge generation (1)	[7]	I²C-bus acknowledge enable bit. 0 = Disables 1 = Enables In Tx mode, the I2CSDA is free in the ACK time. In Rx mode, the I2CSDA is L in the ACK time.	0
Tx clock source selection	[6]	Source clock of I2C-bus transmit clock prescaler selection bit. 0 = I2CCLK = fPCLK /16 1 = I2CCLK = fPCLK /512	0
Tx/Rx Interrupt (5)	[5]	I²C-Bus Tx/Rx interrupt enable/ disable bit. 0 = Disables 1 = Enables	0
Interrupt pending flag (2) (3)	[4]	I²C-bus Tx/Rx interrupt pending flag. This bit cannot be written to 1. If this bit is read as 1, the I2CSCL is tied to L and the I²C is stopped. To resume the operation, clear this bit as 0. 0 = 1) No interrupt is pending (If read). 2) Clear pending condition and Resume the operation (If write). 1 = 1) Interrupt is pending (If read) 2) N/A (If write)	0
Transmit clock value (4)	[3:0]	I²C-Bus transmit clock prescaler. I²C-Bus transmit clock frequency is determined by this 4-bit prescaler value, according to the following formula: Tx clock = I2CCLK/(I2CCON[3:0]+1).	Undefined

NOTE:

1 Interfacing with EEPROM, the ACK generation may be disabled before reading the last data to generate the STOP condition in Rx mode.

2. An I²C-bus interrupt occurs if 1) if a 1-byte transmit or receive operation is complete. In other words, ack period is finished. 2) A general call or a slave address match occurs, 3) Bus arbitration fails.
3. To adjust the setup time of SDA before SCL rising edge, I2CDS has to be written before clearing the I²C interrupt pending bit.
4. I2CCLK is determined by I2CCON[6].
   Tx clock can vary by SCL transition time. If I2CCON[6]=0, I2CCON[3:0]=0x0 or 0x1 is not available.
5. If the I2CCON[5]=0, I2CCON[4] does not operate correctly.
   Therefore, It is recommended to set I2CCON[5]=1, even if you do not use the I²C interrupt.

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2.5.1.2 MULTI-MASTER I²C-Bus Control/Status Register

- I2CSTAT0, R/W, Address = 0xE180_0004
- I2CSTAT2, R/W, Address = 0xE1A0_0004
- I2CSTAT_HDMI_DDC, R/W, Address = 0xFAB0_0004
- I2CSTAT_HDMI_PHY, R/W, Address = 0xFA90_0004

I2CSTAT	Bit	Description	Initial State
Mode selection	[7:6]	I²C-bus master/ slave Tx/Rx mode select bits. 00 = Slave receive mode 01 = Slave transmit mode 10 = Master receive mode 11 = Master transmit mode	00
Busy signal status / START STOP condition	[5]	I²C-Bus busy signal status bit. 0 = read) Not busy (If read) write) STOP signal generation 1 = read) Busy (If read) write) START signal generation. The data in I2CDS is transferred automatically just after the start signal.	0
Serial output	[4]	I²C-bus data output enable/ disable bit. 0 = Disables Rx/Tx, 1 = Enables Rx/Tx	0
Arbitration status flag	[3]	I²C-bus arbitration procedure status flag bit. 0 = Bus arbitration successful 1 = Bus arbitration failed during serial I/O	0
Address-as-slave status flag	[2]	I²C-bus address-as-slave status flag bit. 0 = Cleared when START/STOP condition was detected 1 = Received slave address matches the address value in the I2CADD	0
Address zero status flag	[1]	I²C-bus address zero status flag bit. 0 = Cleared if START/ STOP condition is detected 1 = Received slave address is 00000000b.	0
Last-received bit status flag	[0]	I²C-bus last-received bit status flag bit. 0 = Last-received bit is 0 (ACK was received). 1 = Last-received bit is 1 (ACK was not received).	0

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2.5.1.3 MULTI-MASTER I²C-Bus Address Register

- I2CADD0, R/W, Address = 0xE180_0008
- I2CADD2, R/W, Address = 0xE1A0_0008
- I2CADD_HDMI_DDC, R/W, Address = 0xFAB0_0008
- I2CADD_HDMI_PHY, R/W, Address = 0xFA90_0008

I2CADD	Bit	Description	Initial State
Slave address	[7:0]	7-bit slave address, latched from the I²C-bus. If serial output enable = 0 in the I2CSTAT, I2CADD is write-enabled. The I2CADD value is read any time, regardless of the current serial output enable bit (I2CSTAT) setting. Slave address: [7:1] Not mapped : [0]	Undefined

2.5.1.4 MULTI-MASTER I²C-Bus Transmit/Receive Data Shift Register

- I2CDS0, R/W, Address = 0xE180_000C
- I2CDS2, R/W, Address = 0xE1A0_000C
- I2CDS_HDMI_DDC, R/W, Address = 0xFAB0_000C
- I2CDS_HDMI_PHY, R/W, Address = 0xFA90_000C

I2CDS	Bit	Description	Initial State
Data shift	[7:0]	8-bit data shift register for I²C-bus Tx/Rx operation. If serial output enable = 1 in the I2CSTAT, I2CDS is write-enabled. The I2CDS value is read any time, regardless of the current serial output enable bit (I2CSTAT) setting.	Undefined

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2.5.1.5 MULTI-MASTER I²C-Bus Line Control Register

- I2CLC0, R/W, Address = 0xE180_0010
- I2CLC2, R/W, Address = 0xE1A0_0010
- I2CLC_HDMI_DDC, R/W, Address = 0xFAB0_0010
- I2CLC_HDMI_PHY, R/W, Address = 0xFA90_0010

I2CLC	Bit	Description	Initial State
Filter enable	[2]	I²C-bus filter enable bit. If SDA port is operating as input, this bit should be High. This filter prevents error caused by glitch between two PCLK clock. 0 = Disables Filter 1 = Enables Filter	0
SDA output delay	[1:0]	I²C-Bus SDA line delay length selection bits. SDA line is delayed as following clock time(PCLK) 00 = 0 clocks 01 = 5 clocks 10 = 10 clocks 11 = 15 clocks	00

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3 SERIAL PERIPHERAL INTERFACE

3.1 OVERVIEW OF SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) in S5PV210 transfers serial data using various peripherals. SPI includes two 8, 16, 32-bit shift registers to transmit and receive data. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). SPI supports the protocols for National Semiconductor Microwire and Motorola Serial Peripheral Interface.

3.2 KEY FEATURES OF SERIAL PERIPHERAL INTERFACE

The features of SPI include:

- Full duplex
- 8/16/32-bit shift register for TX/RX
- 8-bit Prescaler logic
- 2 clock sources: PCLK and SPI_EXT_CLK from SYSCON
- Supports 8-bit/16-bit/32-bit bus interface
- Supports the Motorola SPI protocol and National Semiconductor Microwire
- Two independent 32-bits wide transmit and receive FIFOs: depth 64 in port 0 and depth 16 in port 1
- Master-mode and Slave-mode
- Receive-without-transmit operation
- Tx/Rx maximum frequency at up to 50MHz

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3.2.1 OPERATION OF SERIAL PERIPHERAL INTERFACE

The SPI transfers 1-bit serial data between S5PV210 and external device. The SPI in S5PV210 supports the CPU or DMA to transmit or receive FIFOs separately and to transfer data in both directions simultaneously. SPI has two channels, TX channel and RX channel. TX channel has the path from Tx FIFO to external device. RX channel has the path from external device to RX FIFO.

CPU (or DMA) must write data on the register SPI_TX_DATA, to write data in FIFO. Data on the register are automatically moved to Tx FIFOs. To read data from Rx FIFOs, CPU (or DMA) must access the register SPI_RX_DATA and data are automatically sent to the SPI_RX_DATA register.

3.2.1.1 Operation Mode

SPI has two modes, namely, master and slave mode. In master mode, SPICLK is generated and transmitted to external device. XspiCS#, which is the signal to select slave, indicates data valid when XspiCS# is low level. XspiCS# must be set low before packets are transmitted or received.

3.2.1.2 FIFO Access

The SPI supports CPU access and DMA access to FIFOs. Data size of CPU access and DMA access to FIFOs are selected either from 8-bit, 16-bit, or 32-bit data. If 8-bit data size is selected, valid bits are from 0 bit to 7 bit. User can define the trigger threshold to raise interrupt to CPU. The trigger level of each FIFO in port 0 is set by 4 bytes step from 0 byte to 252 bytes, and that of each FIFO in port 1 is set by 1 byte step from 0 byte to 63 bytes. TxDMAOn or RxDMAOn bit of SPI_MODE_CFG register must be set to use DMA access. DMA access supports only single transfer and 4-burst transfer. In TX FIFO, DMA request signal is high until TX FIFO is full. In RX FIFO, DMA request signal is high if FIFO is not empty.

3.2.1.3 Trailing Bytes in the Rx FIFO

If the number of samples in Rx FIFO is less than the threshold value in INT mode or DMA 4 burst mode and no additional data is received, the remaining bytes are called trailing bytes. To remove these bytes in RX FIFO, internal timer and interrupt signal are used. The value of internal timer is set up to 1024 clocks based on APB BUS clock. When timer value is zero, interrupt signal occurs and CPU can remove trailing bytes in FIFO.

3.2.1.4 Packet Number Control

SPI controls the number of packets to be received in master mode. Set SFR (PACKET_CNT_REG) to receive any number of packets. SPI stops generating SPICLK if the number of packets is the same as PACKET_CNT_REG. It is mandatory to follow software or hardware reset before this function is reloaded. (Software reset can clear all registers except special function registers, but hardware reset clears all registers.)

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3.2.1.5 Chip Select Control

Chip select XspiCS# is active low signal. In other words, a chip is selected when XspiCS# input is 0.

XspiCS# can be controlled automatically or manually.

When you use manual control mode, AUTO_N_MANUAL must be cleared (Default value is 0). XspiCS# level is controlled by NSSOUT bit.

When you use auto control mode, AUTO_N_MANUAL must be set as 1. XspiCS toggled between packet and packet automatically. Inactive period of XspiCS is controlled by NCS_TIME_COUNT. NSSOUT is not available at this time.

3.2.1.6 High Speed Operation as Slave

S5PV210 SPI supports Tx/Rx operations upto 50MHz, but there is a limitation. When S5PV210 SPI works as a slave, it consumes large delay over than 15ns in worst operating condition. Such a large delay can cause setup violation at SPI master device. To overcome the problem, S5PV210 SPI provides fast slave Tx mode by setting 1 to HIGH_SPEED bit of CH_CFG register. In that mode, MISO output delay is reduced by half cycle, so that the SPI master device has more setup margin.
However, the fast slave Tx mode can be used only when CPHA = 0.

3.2.1.7 FeedBack Clock Selection

Under SPI protocol spec, SPI master should capture the input data launched by slave (MISO) with its internal SPICLK. If SPI runs at high operating frequency such as 50MHz, it is difficult to capture the MISO input because the required arrival time of MISO, which is an half cycle period in S5PV210, is shorter than the arrival time of MISO that consists of SPICLK output delay of SPI master, MISO output delay of SPI slave, and MISO input delay of SPI master. To overcome the problem, S5PV210 SPI provides 3 feedback clocks that are phase-delayed clock of internal SPICLK.

A selection of feedback clock depends on MISO output delay of SPI slave. To capture MISO data correctly, it is selected the feedback clock that satisfies the following constraint.

$$t_{SPIMIS}(s) < t_{period}/2 - t_{SPISOD}$$

* $t_{SPIMIS}(s)$: *MISO input setup time of SPI master on a given feedback clock selection 's'*
* t_{SPISOD}: *MISO output delay of SPI slave*
* t_{period} : *SPICLK cycle period*

If multiple feedback clocks meet the constraint, the feedback clock with smallest phase delay should be selected.

It is because a feedback clock with large phase delay may capture data of next cycle.

For example of S5PV210 SPI CH1 with master configuration of 50MHz operating frequency, 1.8V external voltage and 15pF load, 270 degree phase-delayed feedback clock should be used if the MISO output delay of SPI slave is assumed as 11ns ($t_{SPIMIS}(s) < 10ns - 11ns = -1ns$).

If the operating clock frequency is 33MHz and other conditions are the same as the previous example, it is better to use 180 degree phase-delayed feedback clock ($t_{SPIMIS}(s) < 15ns - 11ns = 4ns$).

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3.2.1.8 SPI Transfer Format

The S5PV210 supports four different formats for data transfer. *Figure 3-1* describes four waveforms for SPICLK.

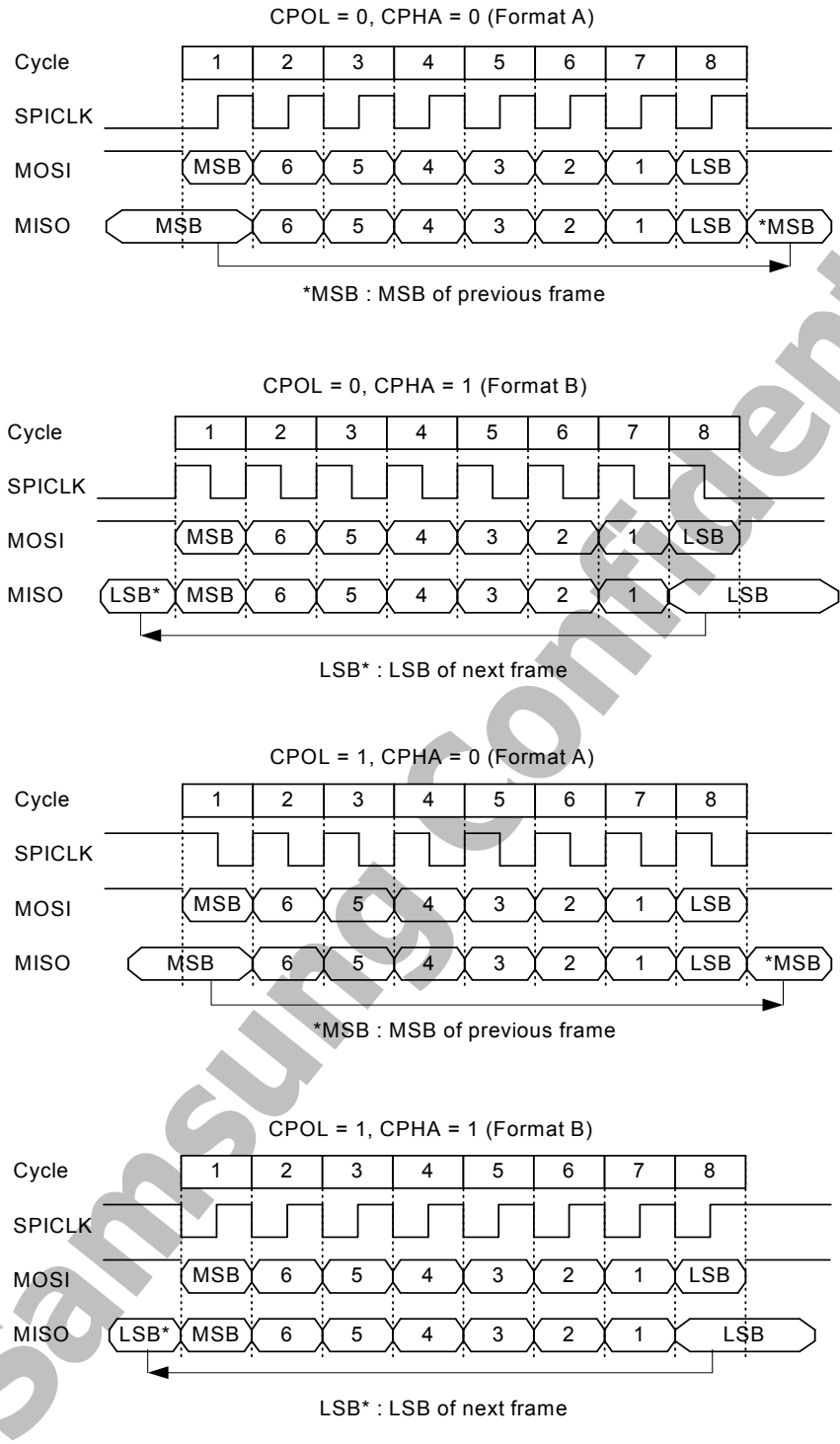

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Figure 3-1 SPI Transfer Format

3.3 IO DESCRIPTION

The following table lists the external signals between the SPI and external device. The unused SPI ports are used as General Purpose I/O ports. Refer to “General Purpose I/O” chapter for more information.

Signal	I/O	Description	Pad	Type
SPI_0_CLK SPI_1_CLK	In/Out	XspiCLK is the serial clock used to control time of data transfer. Out, when used as master In, when used as slave	XspiCLK[0] XspiCLK[1]	muxed
SPI_0_MISO SPI_1_MISO	In/Out	This port is the input port in Master mode. Input mode is used to get data from slave output port. Data are transmitted to master through this port in slave mode. Out, when used as slave In, when used as master	XspiMISO[0] XspiMISO[1]	muxed
SPI_0_MOSI SPI_1_MOSI	In/Out	This port is the output port in Master mode. This port is used to transfer data from master output port. Data are received from master through this port in slave mode. Out, when used as master In, when used as slave	XspiMOSI[0] XspiMOSI[1]	muxed
SPI_0_nSS SPI_1_nSS	In/Out	Slave selection signal. All data TX/RX sequences are executed if XspiCS is low. Out, when used as master In, when used as slave	XspiCSn[0] XspiCSn[1]	muxed

NOTE: Type field indicates whether pads are dedicated to the signal or pads are connected to the multiplexed signals.

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3.4 REGISTER DESCRIPTION

3.4.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
CH_CFG0	0xE1300000	R/W	Specifies the SPI Port 0 Configuration Register	0x0
CLK_CFG0	0xE1300004	R/W	Specifies the SPI Port 0 Clock Configuration Register	0x0
MODE_CFG0	0xE1300008	R/W	Specifies the SPI Port 0 FIFO Control Register	0x0
CS_REG0	0xE130000C	R/W	Specifies the SPI Port 0 Slave Selection Control Register	0x1
SPI_INT_EN0	0xE1300010	R/W	Specifies the SPI Port 0 Interrupt Enable Register	0x0
SPI_STATUS0	0xE1300014	R	Specifies the SPI Port 0 Status Register	0x0
SPI_TX_DATA0	0xE1300018	W	Specifies the SPI Port 0 TX Data Register	0x0
SPI_RX_DATA0	0xE130001C	R	Specifies the SPI Port 0 RX Data Register	0x0
PACKET_CNT_REG0	0xE1300020	R/W	Specifies the SPI Port 0 Packet Count Register	0x0
PENDING_CLR_REG0	0xE1300024	R/W	Specifies the SPI Port 0 Interrupt Pending Clear Register	0x0
SWAP_CFG0	0xE1300028	R/W	Specifies the SPI Port 0 Swap Config Register	0x0
FB_CLK_SEL0	0xE130002C	R/W	Specifies the SPI Port 0 Feedback Clock Selection Register	0x0
CH_CFG1	0xE1400000	R/W	Specifies the SPI Port 1 Configuration Register	0x0
CLK_CFG1	0xE1400004	R/W	Specifies the SPI Port 1 Clock Configuration Register	0x0
MODE_CFG1	0xE1400008	R/W	Specifies the SPI Port 1 SPI FIFO Control Register	0x0
CS_REG1	0xE140000C	R/W	Specifies the SPI Port 1 Slave Selection Control Register	0x1
SPI_INT_EN1	0xE1400010	R/W	Specifies the SPI Port 1 Interrupt Enable Register	0x0
SPI_STATUS1	0xE1400014	R	Specifies the SPI Port 1 Status Register	0x0
SPI_TX_DATA1	0xE1400018	W	Specifies the SPI Port 1 TX Data Register	0x0
SPI_RX_DATA1	0xE140001C	R	Specifies the SPI Port 1 RX Data Register	0x0
PACKET_CNT_REG1	0xE1400020	R/W	Specifies the SPI Port 1 Packet Count Register	0x0
PENDING_CLR_REG1	0xE1400024	R/W	Specifies the SPI Port 1 Interrupt Pending Clear Register	0x0
SWAP_CFG1	0xE1400028	R/W	Specifies the SPI Port 1 Swap Config	0x0

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Register	Address	R/W	Description	Reset Value
			Register	
FB_CLK_SEL1	0xE140002C	R/W	Specifies the SPI Port 1 Feedback Clock Selection Register	0x0

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3.4.1.1 Setting Sequence of Special Function Register

Steps to set Special Function Register (nCS manual mode):

1. Set Transfer Type. (CPOL & CPHA set)
2. Set Feedback Clock Selection register.
3. Set Clock configuration register.
4. Set SPI MODE configuration register.
5. Set SPI INT_EN register.
6. Set PACKET_CNT_REG register if necessary.
7. Set Tx or Rx Channel on.
8. Set nSSout low to start Tx or Rx operation.
   a. Set nSSout Bit to low, then start TX data writing.
   b. If auto chip selection bit is set, nSSout is controlled automatically.

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3.4.2 SPECIAL FUNCTION REGISTER

3.4.2.1 SPI Configuration Register

- CH_CFG0, R/W, Address = 0xE130_0000
- CH_CFG1, R/W, Address = 0xE140_0000

CH_CFGn	Bit	Description	Initial State
HIGH_SPEED_EN	[6]	Slave TX output time control bit. If this bit is enabled, slave TX output time is reduced as much as half period of SPICLKout period. **NOTE:** This bit is valid only in CPHA 0. 0 = Disables 1 = Enables	0
SW_RST	[5]	Software reset. The following registers and bits are cleared by this bit. Rx/Tx FIFO Data, SPI_STATUS Once reset, this bit must be clear manually. 0 = Inactive 1 = Active	0
SLAVE	[4]	Whether SPI Channel is Master or Slave 0 = Master 1 = Slave	0
CPOL	[3]	Determines whether active high or active low clock 0 = Active High 1 = Active Low	0
CPHA	[2]	Select one of the two fundamentally different transfer format 0 = Format A 1 = Format B	0
RX_CH_ON	[1]	SPI Rx Channel On 0 = Channel Off 1 = Channel On	0
TX_CH_ON	[0]	SPI Tx Channel On 0 = Channel Off 1 = Channel On	0

NOTE: SPI controller should reset when

1. Reconfiguration SPI registers.
2. Error interrupt occurred.

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3.4.2.2 Clock Configuration Register

- CLK_CFG0, R/W, Address = 0xE130_0004
- CLK_CFG1, R/W, Address = 0xE140_0004

CLK_CFGn	Bit	Description	Initial State
SPI_CLKSEL	[9]	Clock source selection to generate SPI clock-out 0 = PCLK 1 = SPI_EXT_CLK	0
ENCLK	[8]	Clock enable/ disable 0 = Disable 1 = Enable	0
SPI_SCALER	[7:0]	SPI clock-out division rate SPI clock-out = Clock source / (2 x (Prescaler value +1))	0

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3.4.2.3 SPI FIFO Control Register

- MODE_CFG0, R/W, Address = 0xE130_0008
- MODE_CFG1, R/W, Address = 0xE140_0008

MODE_CFGn	Bit	Description	Initial State
CH_WIDTH	[30:29]	00 = Byte 01 = Halfword 10 = Word 11 = Reserved	0
TRAILING_CNT	[28:19]	Count value from writing the last data in RX FIFO to flush trailing bytes in FIFO	0
BUS_WIDTH	[18:17]	00 = Byte 01 = Halfword 10 = Word 11 = Reserved	0
RX_RDY_LVL	[16:11]	Rx FIFO trigger level in INT mode. Port 0: trigger level (bytes) = 4 x N Port 1: trigger level (bytes) = N (N = value of RX_RDY_LVL field)	0
TX_RDY_LVL	[10:5]	Tx FIFO trigger level in INT mode. Port 0: trigger level (bytes) = 4 x N Port 1: trigger level (bytes) = N (N = value of TX_RDY_LVL field)	0
Reserved	[4:3]	Reserved	-
RX_DMA_SW	[2]	Rx DMA mode enable/disable 0 = Disables DMA Mode 1 = Enables DMA Mode	0
TX_DMA_SW	[1]	Tx DMA mode on/off 0 = Disables DMA Mode 1 = Enables DMA Mode	0
DMA_TYPE	[0]	DMA transfer type, single or 4 busts. 0 = Single 1 = 4 burst DMA transfer size must be set as the same size in SPI DMA.	0

NOTE:

1. CH_WIDTH is shift-register width.
2. BUS_WIDTH is SPI FIFO width, transfer data size should be aligned at BUS_WIDTH.
3. CH_WIDTH must be smaller than BUS_WIDTH or same.

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3.4.2.4 Slave Selection Signal Control Signal

- CS_REG0, R/W, Address = 0xE130_000C
- CS_REG1, R/W, Address = 0xE140_000C

CS_REGn	Bit	Description	Initial State
NCS_TIME_COUNT	[9:4]	NSSOUT inactive time = ((nCS_time_count+3)/2) x SPICLKout	0
Reserved	[3:2]	Reserved	-
AUTO_N_MANUAL	[1]	Chip select toggle manual or auto selection 0 = Manual 1 = Auto	0
NSSOUT	[0]	Slave selection signal (manual only) 0 = Active 1 = Inactive	1

If AUTO_N_MANUAL is set, NSSOUT is controlled by SPI controller and data transfer is not performed continuously.

- Unit data size depends on CH_WIDTH.

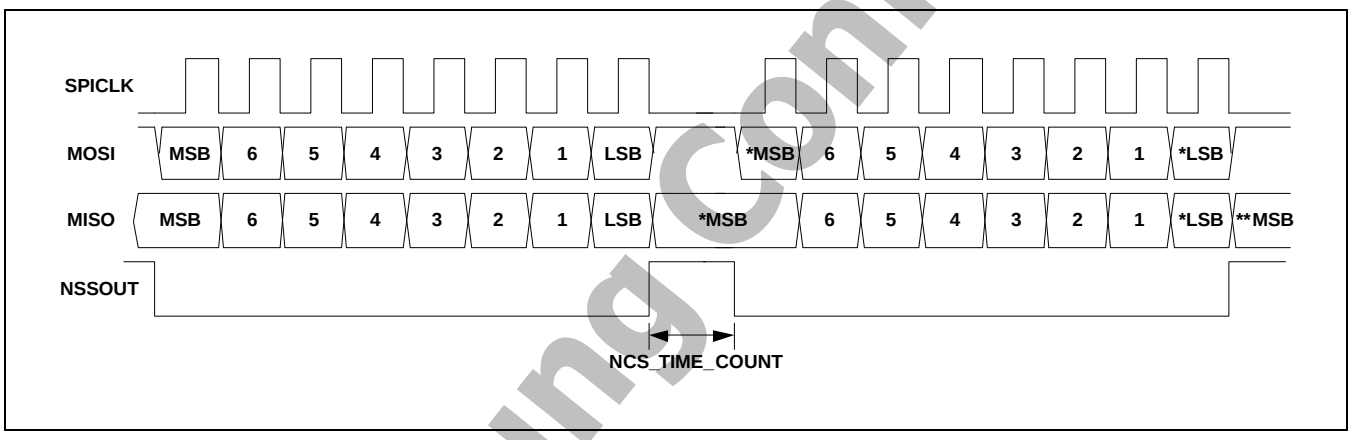

Figure 3-2 Auto Chip Select Mode Waveform (CPOL=0, CPHA=0, CH_WIDTH=Byte)

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3.4.2.5 SPI Interrupt Enable Register

- SPI_INT_EN0, R/W, Address = 0xE130_0010
- SPI_INT_EN1, R/W, Address = 0xE140_0010

SPI_INT_ENn	Bit	Description	Initial State
INT_EN_TRAILING	[6]	Interrupt Enable for trailing count to be 0 0 = Disables 1 = Enables	0
INT_EN_RX_OVERRUN	[5]	Interrupt Enable for RxOverrun 0 = Disables 1 = Enables	0
INT_EN_RX_UNDERRUN	[4]	Interrupt Enable for RxUnderrun 0 = Disables 1 = Enables	0
INT_EN_TX_OVERRUN	[3]	Interrupt Enable for TxOverrun 0 = Disables 1 = Enables	0
INT_EN_TX_UNDERRUN	[2]	Interrupt Enable for TxUnderrun. In slave mode, this bit must be clear first after turning on slave TX path. 0 = Disables 1 = Enables	0
INT_EN_RX_FIFO_RDY	[1]	Interrupt Enable for RxFifoRdy (INT mode) 0 = Disables 1 = Enables	0
INT_EN_TX_FIFO_RDY	[0]	Interrupt Enable for TxFifoRdy (INT mode) 0 = Disables 1 =Enables	0

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3.4.2.6 SPI Status Register

- SPI_STATUS0, R, Address = 0xE130_0014
- SPI_STATUS1, R, Address = 0xE140_0014

SPI_STATUSn	Bit	Description	Initial State
TX_DONE	[25]	Indication of transfer done in Shift register(master mode only) 0 = All case except blow case 1 = If Tx FIFO and shift register are empty	0
TRAILING_BYTE	[24]	Indication that trailing count is 0	0
RX_FIFO_LVL	[23:15]	Data level in Rx FIFO 0 ~ 256 bytes in port 0 0 ~ 64 bytes in port	0
TX_FIFO_LVL	[14:6]	Data level in Tx FIFO 0 ~ 256 bytes in port 0 0 ~ 64 bytes in port	0
RX_OVERRUN	[5]	Rx FIFO overrun error 0 = No Error 1 = Overrun Error	0
RX_UNDERRUN	[4]	Rx FIFO underrun error 0 = No Error, 1 = Underrun Error	0
TX_OVERRUN	[3]	Tx FIFO overrun error 0 = No Error 1 = Overrun Error	0
TX_UNDERRUN	[2]	Tx FIFO underrun error Tx FIFO underrun error is occurred if TX FIFO is empty in slave mode.(no empty state in slave Tx mode) 0 = No Error 1 = Underrun Error	0
RX_FIFO_RDY	[1]	0 = Data in FIFO less than trigger level 1 = Data in FIFO more than trigger level	0
TX_FIFO_RDY	[0]	0 = Data in FIFO more than trigger level 1 = Data in FIFO less than trigger level	0

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3.4.2.7 SPI TX Data Register

- SPI_TX_DATA, W, Address = 0xE130_0018
- SPI_TX_DATA, W, Address = 0xE140_0018

SPI_TX_DATAn	Bit	Description	Initial State
TX_DATA	[31:0]	This field contains the data to be transmitted over the SPI channel.	0

3.4.2.8 SPI RX Data Register

- SPI_RX_DATA0, R, Address = 0xE130_001C
- SPI_RX_DATA1, R, Address = 0xE140_001C

SPI_RX_DATAn	Bit	Description	Initial State
RX_DATA	[31:0]	This field contains the data to be received over the SPI channel.	0

3.4.2.9 Packet Count Register

- PACKET_CNT_REG0, R/W, Address = 0xE130_0020
- PACKET_CNT_REG1, R/W, Address = 0xE140_0020

PACKET_CNT_REGn	Bit	Description	Initial State
PACKET_CNT_EN	[16]	Enable bit for packet count 0 = Disable 1 = Enable	0
COUNT_VALUE	[15:0]	Packet count value	0

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3.4.2.10 Status Pending Clear Register

- PENDING_CLR_REG0, R/W, Address = 0xE130_0024
- PENDING_CLR_REG1, R/W, Address = 0xE140_0024

PENDING_CLR_REGn	Bit	Description	Initial State
TX_UNDERRUN_CLR	[4]	TX underrun pending clear bit 0 = Non-Clear 1 = Clear	0
TX_OVERRUN_CLR	[3]	TX overrun pending clear bit 0 = Non-Clear 1 = Clear	0
RX_UNDERRUN_CLR	[2]	RX underrun pending clear bit 0 = Non-clear 1 = Clear	0
RX_OVERRUN_CLR	[1]	RX overrun pending clear bit 0 = Non-Clear 1 = Clear	0
TRAILING_CLR	[0]	Trailing pending clear bit 0 = Non-Clear 1 = Clear	0

NOTE: After error interrupt pending clear, SPI controller should be reset.
Error interrupt list: Tx underrun, Tx overrun, Rx underrun, Rx overrun

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3.4.2.11 SWAP Config Register

- SWAP_CFG_REG0, R/W, Address = 0xE130_0028
- SWAP_CFG_REG1, R/W, Address = 0xE140_0028

SWAP_CFGn	Bit	Description	Initial State
RX_HWORD_SWAP	[7]	0 = Off 1 = Swap	0
RX_BYTE_SWAP	[6]	0 = Off 1 = Swap	0
RX_BIT_SWAP	[5]	0 = Off 1 = Swap	0
RX_SWAP_EN	[4]	Swap enable 0 = Normal 1 = Swap	0
TX_HWORD_SWAP	[3]	0 = Off 1 = Swap	0
TX_BYTE_SWAP	[2]	0 = Off 1 = Swap	0
TX_BIT_SWAP	[1]	0 = Off 1 = Swap	0
TX_SWAP_EN	[0]	Swap enable 0 = Normal 1 = Swap	0

NOTE: Data size must be larger than swap size.

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3.4.2.12 FeedBack Clock Selection Register

- FB_CLK_SEL_REG0, R/W, Address = 0xE130_002C
- FB_CLK_SEL_REG1, R/W, Address = 0xE140_002C

FB_CLK_SELn	Bit	Description	Initial State
FB_CLK_SEL	[1:0]	In master mode, SPI uses a clock which is feedback from the SPICLK. The feedback clock is intended to capture safely the slave TX signal which can be lagged if slave device is very far. There are four kinds of feedback clocks which experience different path delays. This register selects which one is to be used. Note that this register value is meaningless when SPI operates in slave mode. 00 = SPICLK bypass (do not use feedback clock) 01 = A feedback clock with 90 degree phase lagging 10 = A feedback clock with 180 degree phase lagging 11 = A feedback clock with 270 degree phase lagging **NOTE:** 90 degree phase lagging means 5ns delay in 50MHz operating frequency.	0x0

3.4.2.13 PAD Driving Strength

PAD driving strength of SPI is controlled by setting drive strength control register in GPIO. SPI related SFR is GPBDRV_SR (for SPI channel 0, 1).

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4 USB 2.0 HOST CONTROLLER

4.1 OVERVIEW OF USB 2.0 HOST CONTROLLER

S5PV210 supports a single port USB host interface. The key features of this interface include:

- Complies with Enhanced HCI (EHCI) Rev 1.0a and Open HCI (OHCI) Rev1.0 specifications (Both EHCI and OHCI compatible).
- Complies with USB Rev 2.0 specification.
- Complies with USB Rev 1.1 specification.
- Supports high-speed (480 Mbps transfer) peripherals.
- Supports power management features, such as:
  - Full Suspend/ Resume functionality, including Remote Wakeup
  - Over-current protection on ports hooks for master clock suspension

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4.2 BLOCK DIAGRAM OF USB SYSTEM AND USB 2.0 HOST CONTROLLER

USB HOST 2.0 controller is composed of two independent blocks, namely, USB HOST 2.0 controller and USB PHY Controller. Each of these blocks has an AHB Slave interface that provides the microcontroller with read and write access to the Control and Status Registers (CSRs). The HOST Link has an AHB Master to enable the link to transfer data on the AHB.

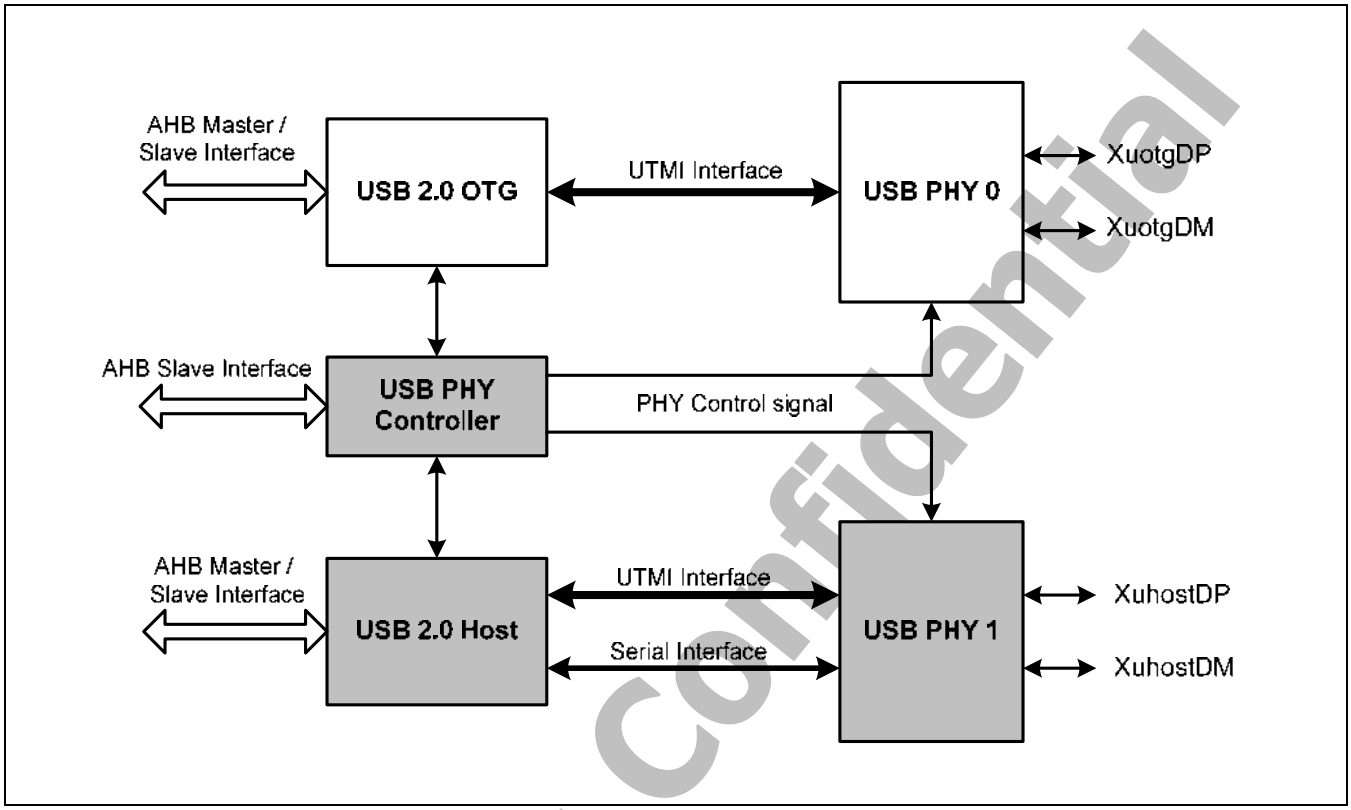

Figure 4-1 USB System Block Diagram

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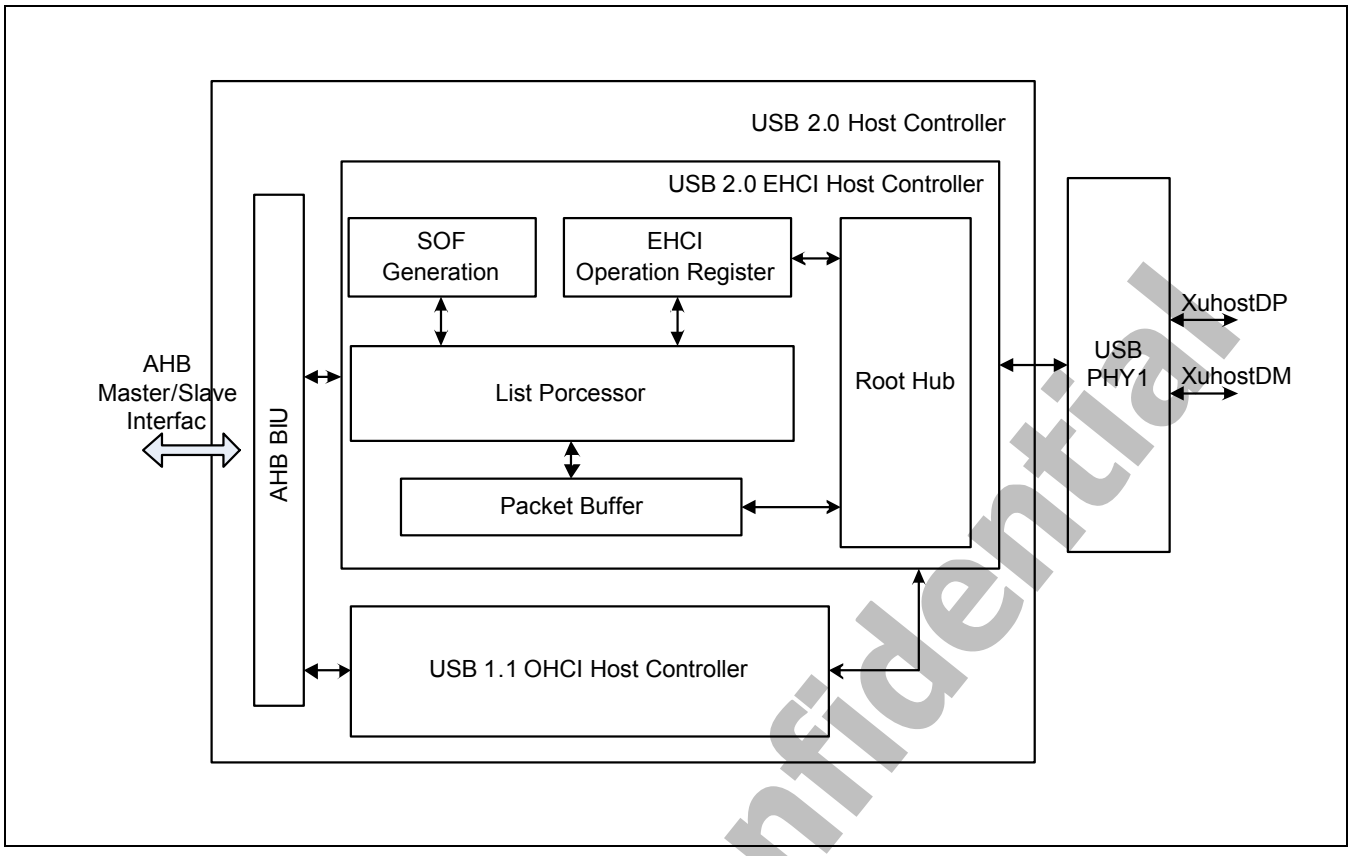

Figure 4-2 USB 2.0 Host Controller Block Diagram

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4.3 REGISTER DESCRIPTION

4.3.1 REGISTER MAP

The USB host controller in S5PV210X complies with both EHCI Rev 1.0a and OHCI Rev 1.0 specification. For more information, Refer to EHCI 1.0a and OHCI 1.0 specification.

Register	Address	R/W	Description	Reset Value
Implemented Capability Registers for USB Host Controller				
HCCPBASE	0xEC20_0000	R	Specifies the Capability and Interface Version Number Register.	0x01000010
HCSPARAMS	0xEC20_0004	R	Specifies the Structural Parameter	0x00001111
HCCPARAMS	0xEC20_0008	R	Specifies the Capability Parameter	0x0000A010
Implemented Operational for USB Host Controller				
USBCMD	0xEC20_0010	R/W	Specifies the USB Command.	0x00080000
USBSTS	0xEC20_0014	R/W	Specifies the USB Status.	0x00001000
USBINTR	0xEC20_0018	R/W	Enables the USB Interrupt.	0x00000000
FRINDEX	0xEC20_001C	R/W	Specifies the USB Frame Index.	0x00000000
CTRLDSSEGMENT	0xEC20_0020	R/W	Specifies the 4G Segment Selector.	0x00000000
PERIODICLISTBASE	0xEC20_0024	R/W	Specifies the Periodic Frame List Base Address Register.	0x00000000
ASYNCLISTADDR	0xEC20_0028	R/W	Specifies the Asynchronous List Address.	0x00000000
Implemented Auxiliary Registers for USB Host Controller				
CONFIGFLAG	0xEC20_0050	R/W	Specifies the Configured Flag Register	0x00000000
Port Status/Control	0xEC20_0054	R/W	Specifies the Port Status and Control Register	0x00002000
Implemented Specific Registers				
INSNREG00	0xEC20_0090	R/W	Specifies the Programmable Microframe Base Value.	0x00000000
INSNREG01	0xEC20_0094	R/W	Specifies the Programmable Packet Buffer OUT/IN Thresholds.	0x00400040
INSNREG02	0xEC20_0098	R/W	Specifies the Programmable Packet Buffer Depth.	0x00000100
INSNREG03	0xEC20_009C	R/W	Transfers Break Memory.	0x00000000
INSNREG04	0xEC20_00A0	R/W	Used for debug only.	0x00000000
INSNREG05	0xEC20_00A4	R/W	Used for UTMI Configuration.	0x00001000
INSNREG06	0xEC20_00A8	R/W	AHB Error Status	0x00000000
INSNREG07	0xEC20_00AC	R/W	AHB Master Error Address	0x00000000
OHCI Registers for USB Host Controller				
HcRevision	0xEC30_0000	R	Specifies the USB Host Controller Revision Register.	0x0000_0110

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Register	Address	R/W	Description	Reset Value
HcControl	0xEC30_0004	R/W	Specifies the USB Host Controller Control Register.	0x0000_0000
HcCommonStatus	0xEC30_0008	R/W	Specifies the USB Host Controller Command Status Register.	0x0000_0000
HcInterruptStatus	0xEC30_000C	R/W	Specifies the USB Host Controller Interrupt Status Register.	0x0000_0000
HcInterruptEnable	0xEC30_0010	R/W	Specifies the USB Host Controller Interrupt Enable Register.	0x0000_0000
HcInterruptDisable	0xEC30_0014	R/W	Specifies the USB Host Controller Interrupt Disable Register.	0x0000_0000
HcHCCA	0xEC30_0018	R/W	Specifies the USB Host Controller HCCA Register.	0x0000_0000
HcPeriodCuttentED	0xEC30_001C	R	Specifies the USB Host Controller Period Current ED Register	0x0000_0000
HcControlHeadED	0xEC30_0020	R/W	Specifies the USB Host Controller Control Head ED Register.	0x0000_0000
HcControlCurrentED	0xEC30_0024	R/W	Specifies the USB Host Controller Control Current ED Register.	0x0000_0000
HcBulkHeadED	0xEC30_0028	R/W	Specifies the USB Host Controller Bulk Head ED Register.	0x0000_0000
HcBulkCurrentED	0xEC30_002C	R/W	Specifies the USB Host Controller Bulk Current ED Register	0x0000_0000
HcDoneHead	0xEC30_0030	R	Specifies the USB Host Controller Done Head Register.	0x0000_0000
HcRmInterval	0xEC30_0034	R/W	Specifies the USB Host Controller FmInterval Register.	0x0000_2EDF
HcFmRemaining	0xEC30_0038	R	Specifies the USB Host Controller Frame Remaining Register.	0x0000_0000
HcFmNumber	0xEC30_003C	R	Specifies the USB Host Controller Frame Number Register.	0x0000_0000
HcPeriodicStart	0xEC30_0040	R/W	Specifies the USB Host Controller Periodic Start Register.	0x0000_0000
HcLSThreshold	0xEC30_0044	R/W	Specifies the USB Host Controller Low-Speed Threshold Register.	0x0000_0628
HcRhDescriptorA	0xEC30_0048	R/W	Specifies the USB Host Controller Root Hub Descriptor A Register.	0x0200_0001
HcRhDescriptorB	0xEC30_004C	R/W	Specifies the USB Host Controller Root Hub Descriptor B Register.	0x0000_0000
HcRhStatus	0xEC30_0050	R/W	Specifies the USB Host Controller Root Hub Status Register.	0x0000_0000
HcRhPortStatus	0xEC30_0054	R/W	Specifies the USB Host Controller Root Hub Port Status Register.	0x0000_0000

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4.3.2 IMPLEMENTED SPECIFIC REGISTERS

Specific registers allow you to program configurable registers such as the Packet Buffer Depth, Break Memory Transfer, Frame Length, and UTMI Control and Status Registers Access.

4.3.2.1 Programmable Microframe Base Value (INSNREG00, R/W, Address = 0xEC20_0090)

INSNREG00	Bit	Description	Initial State
Reserved	[31:20]	-	0x00000000
-	[19]	Enables the AHB master interface to utilize burst INCR16 when appropriate. • 1'b1 = Use INCR16 when appropriate • 1'b0 = Do not use INCR16:use other enabled INCRX bursts or unspecified length burst INCR	-
-	[18]	Enables the AHB master interface to utilize burst INCR8 when appropriate. • 1'b1 = Use INCR8 when appropriate • 1'b0 = Do not use INCR8:use other enabled INCRX bursts or unspecified length burst INCR	-
-	[17]	Enables the AHB master interface to utilize burst INCR4 when appropriate. • 1'b1 = Use INCR4 when appropriate • 1'b0 = Do not use INCR4:use other enabled INCRX bursts or unspecified length burst INCR	-
-	[16]	Forces AHB master to start INCR4/8/16 bursts only on burst boundaries. AHB requires that double word width burst be addressed aligned only the double word boundary • 1'b1 = Start INCRX burst only on burst x-aligned addresses • 1'b0 = Normal AHB operation, start bursts on any double word boundary	-
-	[15]	When the OHCI clocks are suspended, the system has to assert this signal to start the clocks(12 and 48 MHz). This should be deasserted after the clocks are started and before the host is suspended again (Host is suspended means HCFS =SUSPEND or all the OHCI ports are suspended).	-
-	[14]	• 1'b1 = If the USB port is owned by OHCI, the signal utmi_suspend_o_n reflects the status of the USB port(suspended or not suspended) • 1'b0 = If the USB port is owned by OHCI, - utmi_suspend_o_n asserts(0) if all the OHCI ports are suspended or if the OHCI is in global suspend state(HCFS=USBSUSOPEND) - utmi_susend_o_n deasserts(1) if any of the OHCI ports are not suspended and OHCI is not in global suspend.	-
Reserved	[13]	-	
-	[12:1]	Changes the microframe length value (default is microframe SOF = 125us) to reduce the simulation time. This value is used as 1-microframe counter with word interface (16-bits).	-

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INSNREG00	Bit	Description	Initial State
-	[0]	Writing 1'b1 enables the microframe length value field of this register.	-

4.3.2.2 Programmable Packet Buffer OUT/IN Thresholds (INSNREG01, R/W, Address = 0xEC20_0094)

INSNREG01	Bit	Description	Initial State
	[31:0]	[31:16] OUT Threshold [15:0] IN Threshold Specifies the number of DWORDs (32-bit entries). The OUT threshold is used to start the USB transfer as soon as the OUT threshold amount of data is fetched from system memory. It is also used to disconnect the data fetch if the threshold amount of space is not available in the Packet Buffer. The IN threshold is used to start the memory transfer as soon as the IN threshold amount of data is available in the Packet Buffer. It is also used to disconnect the data write if the threshold amount of data is not available in the Packet Buffer. For INCRX configurations, the minimum threshold amount that can be programmed is the highest possible INCRX burst value. The minimum OUT and IN threshold amount that can be programmed through INSN registers is 16 bytes. OUT and IN threshold values can be equal to the packet buffer depth. The default value of thresholds is 256 bytes IN and OUT thresholds.	0x00400040

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4.3.2.3 Programmable Packet Buffer Depth (INSNREG02, R/W, Address = 0xEC20_0098)

INSNREG02	Bit	Description	Initial State
-	[31:0]	Specifies the number of DWORDs (32-bit entries).	0x00000100

4.3.2.4 Break Memory Transfer (INSNREG03, R/W, Address = 0xEC20_009C)

INSNREG03	Bit	Description	Initial State
Reserved	[31:13]	-	0x00000000
-	[12:10]	Tx-Tx turnaround Delay Add on This field specifies the extra delays in phy_clks to be added to the "Transmit to Transmit turnaround delay" value maintained in the core. The default value of this register field is 0.	-
-	[9]	Periodic Frame List Fetch Setting this bit will force the host controller to fetch the periodic frame list in every microframe of a frame.	-
-	[8:1]	Time-Available Offset. This value indicates the additional number of bytes to be accommodated for the time-available calculation.	-
-	[0]	Specifies Break Memory Transfer. Used in conjunction with INSNREG01 to enable/disable breaking memory transactions into chunks once the OUT/IN threshold value is reached. • 1'b1 = Enables this function • 1'b0 = Disables this function	-

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4.3.2.5 Used for Debug Only (INSNREG04, R/W, Address = 0xEC20_00A0)

INSNREG04	Bit	Description	Initial State
Reserved	[31:6]	-	0x00000000
-	[5]	Used only for debug purposes. • 1'b0 = by default, the automatic feature is enabled. The Suspend signal is deasserted when run/stop is reset by software, but the hchalted bit is not yet set. • 1'b1 = Disables the automatic feature, which takes all ports out of suspend when software clears the run/stop bit. This is for backward compatibility.	-
-	[4]	• 1’b0 = Enables NAK reload fix. • 1’b1 = Disables NAK reload fix. Reset value is 1’b0. Attribute is R/W.	-
Reserved.	[3]	-	-
-	[2]	1’b1 = Scales down port enumeration time.	-
-	[1]	1’b1 = Makes the HCCPARAMS register writable.	-
-	[0]	1’b1 = Makes the HCSPARAMS register writable.	-

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4.3.2.6 UTMI Configuration (INSNREG05, R/W, Address = 0xEC20_00A4)

INSNREG05	Bit	Description	Initial State
Reserved	[31:18]	-	0x00001000
-	[17]	Specifies VBusy (Software RO). The hardware indicates that a write to this register has occurred and the hardware is processing the operation defined by the data written. When the processing is finished, this bit is cleared	-
-	[16:13]	Specifies VPort (Software R/W).	-
-	[12]	Specifies VControlLoadM. • 1'b0 = Load • 1'b1 = NOP, (Software R/W)	-
-	[11:8]	Specifies VControl (Software R/W).	-
-	[7:0]	Specifies VStatus (Software RO).	-

4.3.2.7 AHB Error Status (INSNREG06, R/W, Address = 0xEC20_00A8)

INSNREG05	Bit	Description	Initial State
	[31]	AHB Error Captured Indicator that an AHB error was encountered and values were captured. To clear this field the application must write a 0 to it.	0x00000000
Reserved	[30:12]	-	-
-	[11:9]	HBURST value of the control phase at which the AHB error occurred.	-
-	[8:4]	Number of beats expected in the burst at which the AHB error occurred. Valid values are 0 to 16	-
-	[3:0]	Number of successfully-completed beats in the current burst before the AHB error occurred.	-

4.3.2.8 AHB Master Error Address (INSNREG07, R/W, Address = 0xEC20_00AC)

INSNREG05	Bit	Description	Initial State
	[31:0]	AHB Master Error Address AHB address of the control phase at which the AHB error occurred.	0x00000000

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5 USB2.0 HS OTG

5.1 OVERVIEW OF USB2.0 HS OTG

Samsung USB On-The-Go (OTG) is a Dual-Role Device (DRD) controller, which supports both device and host functions. It is fully compliant with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a. It supports high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps, Host only) transfers. HS OTG can be configured as a Host-only or Device-only controller.

5.2 KEY FEATURES OF USB2.0 HS OTG

The USB2.0 HS OTG features include:

- Complies with the On-The-Go Supplement to the USB 2.0 Specification (Revision 1.0a)
- Operates in High-Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed (1.5 Mbps, Host only) modes
- Supports UTMI+ Level 3 interface (Revision 1.0)
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- Supports only 32-bit data on the AHB
- 1 Control Endpoint 0 for control transfer
- 15 Device Mode programmable Endpoints
  - Programmable endpoint type: Bulk, Isochronous, or Interrupt
  - Programmable IN/ OUT direction
- Supports 16 Host channels
- Supports packet-based, dynamic FIFO memory allocation of 7936depths (35-bit width)

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5.3 BLOCK DIAGRAM OF USB2.0 HS OTG

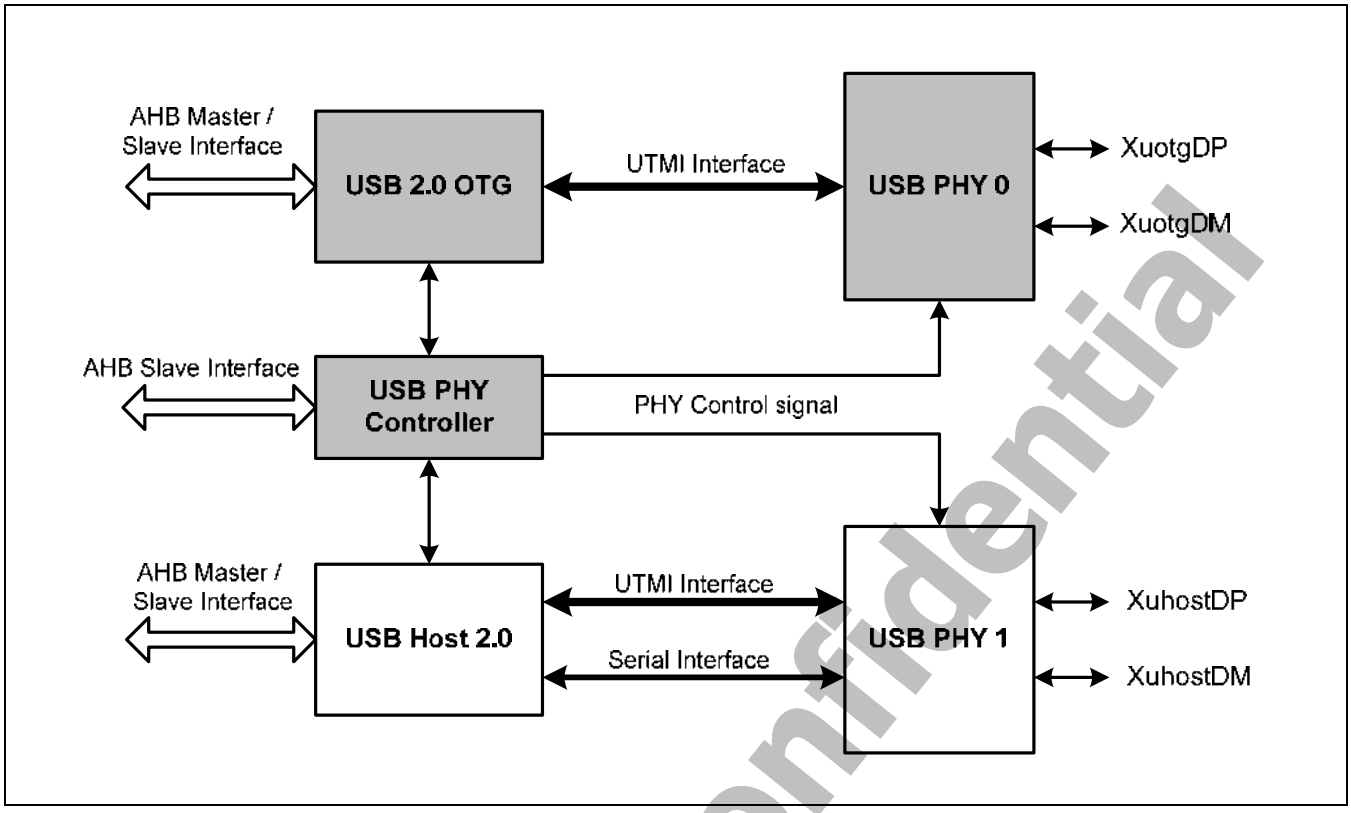

Figure 5-1 System Level Block Diagram

USB HS OTG controller is composed of two independent blocks, namely, USB 2.0 OTG and USB PHY Controller. Each of these blocks has an AHB Slave interface that provides the microcontroller with read and write access to the Control and Status Registers (CSRs). The OTG Link has an AHB Master to enable the link to transfer data on the AHB.

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5.4 MODES OF OPERATION

The end user application operates the Link in either DMA or Slave mode. It cannot operate the USB OTG controller using DMA and Slave modes simultaneously.

5.4.1 DMA MODE

USB OTG host uses the AHB Master interface to transmit packet data to be fetched (AHB to USB) and receive data update (USB to AHB). The AHB master uses programmed DMA address (HCDMAn register in Host mode and DIEPDMAn/ DOEPDMAn register in Device mode) to access the data buffers.

5.4.2 SLAVE MODE

USB OTG can operate in either transaction-level or pipelined transaction-level. The application handles one data packet at a time per channel / endpoint in transaction-level operations. In pipelined transaction-level operation, the application programs the OTG to perform multiple transactions. The advantage of pipelined operation is that the application is not interrupted based on packet.

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5.5 POWER MANAGEMENT UNIT SETTING

A register in Power Management Unit has to be set for USB to work appropriately. For more information, refer to Power Management Unit.

USB_CONTROL	Bit	Description	R/W	Initial State
ENABLE 1	[1]	Enables USB PHY1 0 = Disables 1 = Enables This bit must be set before USB PHY1 is used	R/W	1'b0
ENABLE 0	[0]	Enables USB PHY0 0 = Disables 1 = Enables This bit must be set before USB PHY0 is used.	R/W	1'b0

The USB_CONTROL register (based on the address E010_E80Ch) is guided to be set differently depending on the following system operation mode:

5.5.1 NORMAL MODE

Reset Value of ENABLE is 1'b0. To start USB transaction set this value to 1'b1.

In Normal Mode, power to USB PHY is switched off if USB OTG function is not used.

5.5.2 STOP/DEEP STOP/SLEEP MODE

In STOP/DEEP STOP/SLEEP MODE operation modes, USB PHY power is switched off.

Therefore, to prevent unwanted leakage current, ENABLE must be set to 1'b0 before entering these modes.

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5.6 REGISTER MAP

5.6.1 OVERVIEW OF REGISTER MAP

To control and observe the OTG PHY, access the USB PHY control registers based on the address EC10_0000h.

The OTG Link Core registers is based on the address EC00_0000h, which is classified as follows:

- Core Global Registers
- Host Mode Registers
  - Host Global Registers
  - Host Port CSRs
  - Host Channel-Specific Registers
- Device Mode Registers
  - Device Global Registers
  - Device Endpoint-Specific Registers

The Core Global and Host Port control and status registers are accessed in both Host and Device modes. If the OTG Link operates in either Device or Host mode, the application must not access registers from other modes. If an unauthorized access occurs, a Mode Mismatch interrupt is generated and value is reflected in the Core Interrupt register. If the core switches from one mode to another, reprogram the registers in the new mode of operation to match state after a power-on reset.

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5.6.2 OTG LINK CSR MEMORY MAP

Figure 5-2 shows the OTG link CSR address map. Host and Device mode registers occupy different addresses. All registers are implemented in the AHB Clock domain.

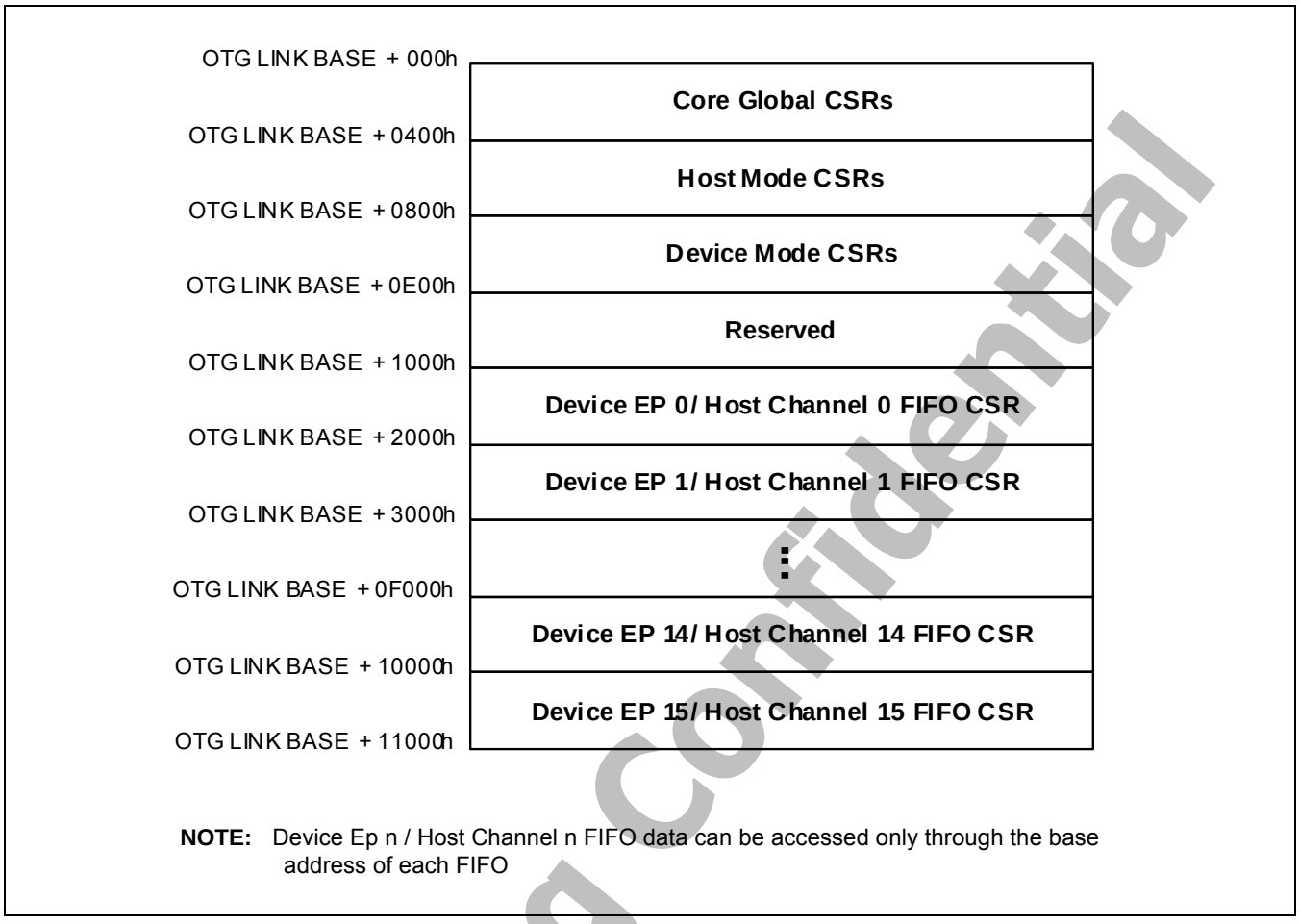

Figure 5-2 OTG Link CSR Memory Map

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5.6.3 OTG FIFO ADDRESS MAPPING

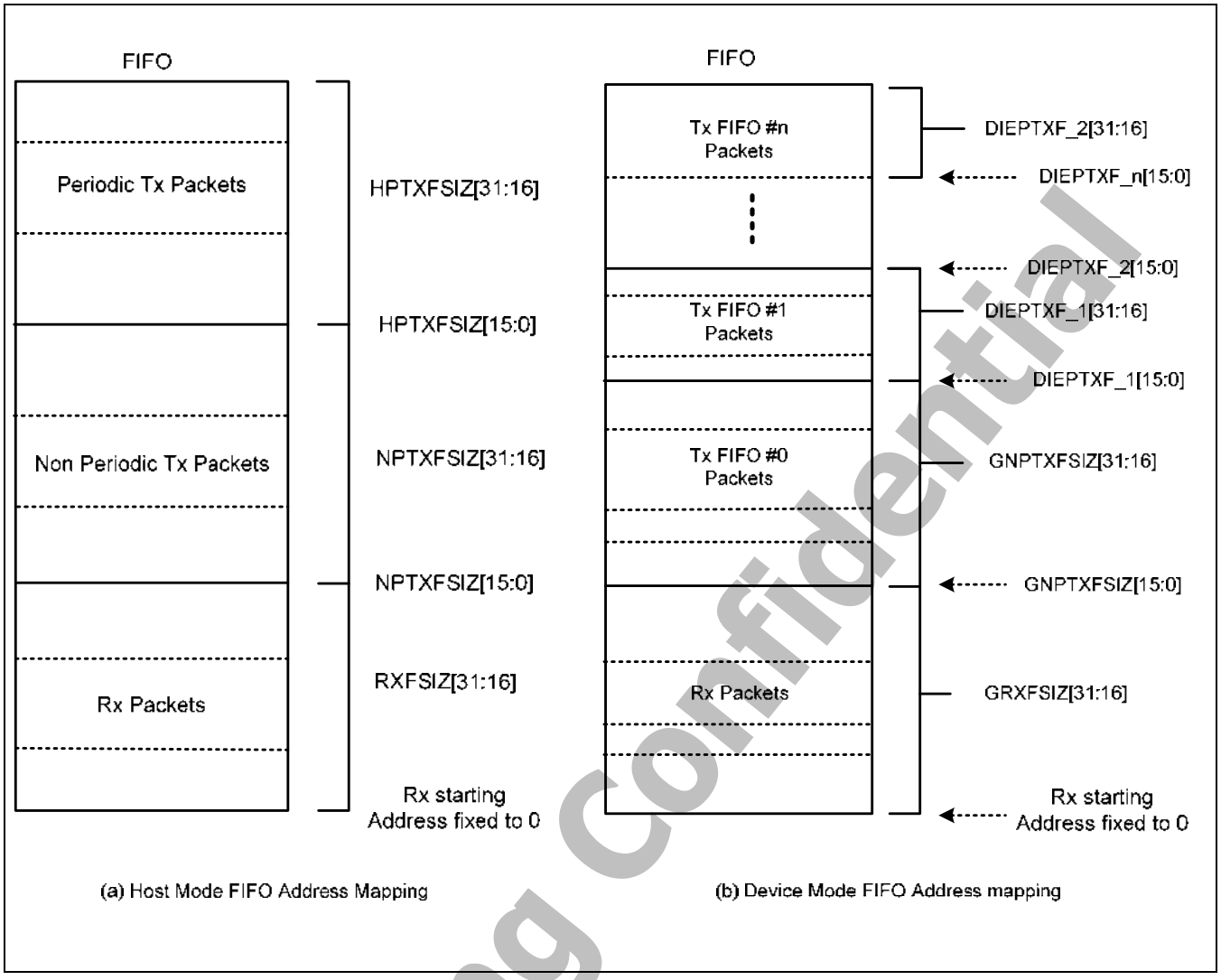

Figure 5-3 OTG FIFO Mapping

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Figure 5-3 shows the OTG FIFO Address Mapping. The following registers must be programmed as follows;

In Host Mode

- RXFSIZ[31:16] = OTG_RX_DFIFO_DEPTH
- NPTXFSIZ[15:0] = OTG_RX_DFIFO_DEPTH
- NPTXFSIZ[31:16] = OTG_TX_HNPERIO_DFIFO_DEPTH
- HPTXFSIZ[15:0] = OTG_RX_DFIFO_DEPTH + OTG_TX_HNPERIO_DFIFO_DEPTH
- HPTXFSIZ[31:16] = OTG_TX_HPERIO_DFIFO_DEPTH

In Device Mode

- RXFSIZ[31:16] = OTG_RX _DFIFO_ DEPTH
- NPTXFSIZ[15:0] = OTG_RX_ DFIFO_ DEPTH
- NPTXFSIZ[31:16] = OTG_TX_DINEP_DFIFO_DEPTH_0
- DIEPTXF_1[15:0] = OTG_RX_DFIFO_DEPTH + OTG_TX_DINEP_DFIFP_DEPTH_0
- DIEPTXF_1[31:16] = OTG_TX_DINEP_DFIFO_DEPTH_1
- DEIPTXF_2[15:0] = DIEPTXF_1[15:0] + OTG_TX_DINEP_DFIFO_DEPTH_1
- DIEPTXF_2[31:16] = OTG_TX_DINEP_DFIFO_DEPTH_2

NOTE: When the device is operating in non Scatter Gather Internal DMA mode, the last locations of the SPRAM are used to store the DMAADDR values of each Endpoint (1 Location per Endpoint). When the device is operating in Scatter Gather, then the last locations of the SPRAM store the Base Descriptor address, Current Descriptor address, Current Buffer address, and status word (DWORD-32bits information for each endpoint direction (4 locations per Endpoint .If an endpoint is bidirectional then 4 will be used for IN and another 4 for OUT).

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5.6.4 APPLICATION ACCESS TO THE CSRS

The Access column of each register description that follows specifies how the application and the core access the register fields of the CSRs. The following conventions are used.

Read Only	R	The application has permission to read the Register field. Writes to read-only fields have no effect.
Write Only	W	The application has permission to write in the Register field.
READ and Write	R/ W	The application has permission to read and writes in the Register field. The application sets this field by writing 1’b1 and clears it by writing 1’b0.
Read, Write, and Self Clear	R/ W_SC	Register field is read and written by the application (Read and Write), and is cleared to 1'b0 by the core (Self Clear). The conditions under which the core clears this field are explained in detail in the field's description.
Read, Write, Self Set, and Self Clear	R/ W_SS_SC	Register field is read and written by the application (Read and Write), set to 1'b1 by the core on certain USB events (Self Set), and cleared to 1'b0 by the core (Self Clear).
Read, Self set, and Write Clear	R/ SS_WC	Register field is read by the application (Read), set to 1'b1 by the core on certain internal or USB or AHB event (Self Set), and cleared to 1'b0 by the application with a register write of 1'b1 (Write Clear). A register write of 1'b0 has no effect on this field.
Read, Write Set, and Self Clear	R/ WS_SC	Register field is read by the application (Read), set to 1'b1 by the application with a register write of 1'b1 (Write Set), and is cleared to 1'b0 by the core (Self Clear). The application cannot clear this type of field, and a register write of 1'b0 to this bit has no effect on this field.
Read, Self set, and Self Clear or Write Clear	R/ SS_SC_WC	Register field is read by the application (Read), set to 1'b1 by the core on certain internal or USB or AHB events (Self Set), and cleared to 1'b0 either by the core itself (Self Clear) or by the application with a register write of 1'b1 (Write Clear). A register write of 1’b0 to this bit has no effect on this field.

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5.7 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
XuotgDP	Input/ Output	Data Plus Signal from the USB Cable	XuotgDP	Dedicated
XuotgDM	Input/ Output	Data Minus Signal from the USB Cable	XuotgDM	Dedicated
XusbXTI	Input	Crystal Oscillator XI	XusbXTI	Dedicated
XusbXTO	Output	Crystal Oscillator XO	XusbXTO	Dedicated
XuotgREXT	Input/ Output	Connection to the External 44.2Ω (±1%) register	XuotgREXT	Dedicated
XuotgVBUS	Input/ Output	USB mini-Receptacle VBUS	XuotgVBUS	Dedicated
XuotgID	Input	USB mini-Receptacle Identifier	XuotgID	Dedicated
XuotgDRVVBUS	Output	Off-Chip Charge Pump Enable	XuotgDRVVBUS	Dedicated

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5.8 REGISTER DESCRIPTION

5.8.1 REGISTER MAP

Table 5-1 Register Summary of HS USB PHY Controller

Register	Address	R/W	Description	Reset Value
USB PHY Control Registers				
UPHYPWR	0xEC10_0000	R/W	Specifies the USB PHY Power Control Register	0x0000_01F9
UPHYCLK	0xEC10_0004	R/W	Specifies the USB PHY Clock Control Register	0x0000_0000
URSTCON	0xEC10_0008	R/W	Specifies the USB Reset Control Register	0x0000_0009
UPHYTUNE1	0xEC10_0020	R/W	Specifies the USB PHY1 Tuning Register	0x0009_19B3
UPHYTUNE0	0xEC10_0024	R/W	Specifies the USB PHY0 Tuning Register	0x0009_19B3
OTG LINK Core Registers (Core Global Registers)				
GOTGCTL	0xEC00_0000	R/W	Specifies the OTG Control and Status Register	0x0001_0000
GOTGINT	0xEC00_0004	R/W	Specifies the OTG Interrupt Register	0x0000_0000
GAHBCFG	0xEC00_0008	R/W	Specifies the Core AHB Configuration Register	0x0000_0000
GUSBCFG	0xEC00_000C	R/W	Specifies the Core USB Configuration Register	0x0000_1408
GRSTCTL	0xEC00_0010	R/W	Specifies the Core Reset Register	0x8000_0000
GINTSTS	0xEC00_0014	R/W	Specifies the Core Interrupt Register	0x0400_0020
GINTMSK	0xEC00_0018	R/W	Specifies the Core Interrupt Mask Register	0x0000_0000
GRXSTSR	0xEC00_001C	R	Specifies the Receive Status Debug Read Register	-
GRXSTSP	0xEC00_0020	R	Specifies the Receive Status Read/Pop Register	-
GRXFSIZ	0xEC00_0024	R/W	Specifies the Receive FIFO Size Register	0x0000_1F00
GNPTXFSIZ	0xEC00_0028	R/W	Specifies the Non-Periodic Transmit FIFO Size Register	0x1F00_1F00
GNPTXSTS	0xEC00_002C	R	Specifies the Non-Periodic Transmit FIFO/Queue Status Register	0x0008_1F00
GLPMCFG	0xEC00_0054	R/W	Specifies the Core LPM configuration Register	0x0000_0000
HPTXFSIZ	0xEC00_0100	R/W	Specifies the Host Periodic Transmit FIFO Size Register	0x0300_5A00
DIEPTXF1	0xEC00_0104	R/W	Specifies the Device IN Endpoint Transmit FIFO-1 Size Register	0x0300_2200
DIEPTXF2	0xEC00_0108	R/W	Specifies the Device IN Endpoint Transmit FIFO-2 Size Register	0x0300_2500
DIEPTXF3	0xEC00_010C	R/W	Specifies the Device IN Endpoint Transmit FIFO-3 Size Register	0x0300_2800
DIEPTXF4	0xEC00_0110	R/W	Specifies the Device IN Endpoint Transmit FIFO-4 Size Register	0x0300_2B00
DIEPTXF5	0xEC00_0114	R/W	Specifies the Device IN Endpoint Transmit FIFO-5 Size Register	0x0300_2E00
DIEPTXF6	0xEC00_0118	R/W	Specifies the Device IN Endpoint Transmit FIFO-6	0x0300_3100

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Register	Address	R/W	Description	Reset Value
			Size Register	
DIEPTXF7	0xEC00_011C	R/W	Specifies the Device IN Endpoint Transmit FIFO-7 Size Register	0x0300_3400
DIEPTXF8	0xEC00_0120	R/W	Specifies the Device IN Endpoint Transmit FIFO-8 Size Register	0x0300_3700
DIEPTXF9	0xEC00_0124	R/W	Specifies the Device IN Endpoint Transmit FIFO-9 Size Register	0x0300_3A00
DIEPTXF10	0xEC00_0128	R/W	Specifies the Device IN Endpoint Transmit FIFO-10 Size Register	0x0300_3D00
DIEPTXF11	0xEC00_012C	R/W	Specifies the Device IN Endpoint Transmit FIFO-11 Size Register	0x0300_4000
DIEPTXF12	0xEC00_0130	R/W	Specifies the Device IN Endpoint Transmit FIFO-12 Size Register	0x0300_4300
DIEPTXF13	0xEC00_0134	R/W	Specifies the Device IN Endpoint Transmit FIFO-13 Size Register	0x0300_4600
DIEPTXF14	0xEC00_0138	R/W	Specifies the Device IN Endpoint Transmit FIFO-14 Size Register	0x0300_4900
DIEPTXF15	0xEC00_013C	R/W	Specifies the Device IN Endpoint Transmit FIFO-15 Size Register	0x0300_4C00
Host Mode Registers (Host Global Registers)				
HCFG	0xEC00_0400	R/W	Specifies the Host Configuration Register	0x0020_0000
HFIR	0xEC00_0404	R/W	Specifies the Host Frame Interval Register	0x0000_0B8F
HFNUM	0xEC00_0408	R	Specifies the Host Frame Number/Frame Time Remaining Register	0x0000_0000
HPTXSTS	0xEC00_0410	R	Specifies the Host Periodic Transmit FIFO/Queue Status Register	0x0008_0300
HAINT	0xEC00_0414	R	Specifies the Host All Channels Interrupt Register	0x0000_0000
HAINTMSK	0xEC00_0418	R/W	Specifies the Host All Channels Interrupt Mask Register	0x0000_0000
Host Mode Registers (Host Port Control and Status Registers)				
HPRT	0xEC00_0440	R/W	Specifies the Host Port Control and Status Register	0x0000_0000
Host Mode Registers (Host Channel-Specific Registers)				
HCCHAR0	0xEC00_0500	R/W	Specifies the Host Channel 0 Characteristics Register	0x0000_0000
HCSPLT0	0xEC00_0504	R/W	Specifies the Host Channel 0 Spilt Control Register	0x0000_0000
HCINT0	0xEC00_0508	R/W	Specifies the Host Channel 0 Interrupt Register	0x0000_0000
HCINTMSK0	0xEC00_050C	R/W	Specifies the Host Channel 0 Interrupt Mask Register	0x0000_0000
HCTSIZ0	0xEC00_0510	R/W	Specifies the Host Channel 0 Transfer Size Register	0x0000_0000
HCDMA0	0xEC00_0514	R/W	Specifies the Host Channel 0 DMA Address	0x0000_0000

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Register	Address	R/W	Description	Reset Value
			Register	
HCCHAR1	0xEC00_0520	R/W	Specifies the Host Channel 1 Characteristics Register	0x0000_0000
HCSPLT1	0xEC00_0524	R/W	Specifies the Host Channel 1 Spilt Control Register	0x0000_0000
HCINT1	0xEC00_0528	R/W	Specifies the Host Channel 1 Interrupt Register	0x0000_0000
HCINTMSK1	0xEC00_052C	R/W	Specifies the Host Channel 1 Interrupt Mask Register	0x0000_0000
HCTSIZ1	0xEC00_0530	R/W	Specifies the Host Channel 1 Transfer Size Register	0x0000_0000
HCDMA1	0xEC00_0534	R/W	Specifies the Host Channel 1 DMA Address Register	0x0000_0000
HCCHAR2	0xEC00_0540	R/W	Specifies the Host Channel 2 Characteristics Register	0x0000_0000
HCSPLT2	0xEC00_0544	R/W	Specifies the Host Channel 2 Spilt Control Register	0x0000_0000
HCINT2	0xEC00_0548	R/W	Specifies the Host Channel 2 Interrupt Register	0x0000_0000
HCINTMSK2	0xEC00_054C	R/W	Specifies the Host Channel 2 Interrupt Mask Register	0x0000_0000
HCTSIZ2	0xEC00_0550	R/W	Specifies the Host Channel 2 Transfer Size Register	0x0000_0000
HCDMA2	0xEC00_0554	R/W	Specifies the Host Channel 2 DMA Address Register	0x0000_0000
HCCHAR3	0xEC00_0560	R/W	Specifies the Host Channel 3 Characteristics Register	0x0000_0000
HCSPLT3	0xEC00_0564	R/W	Specifies the Host Channel 3 Spilt Control Register	0x0000_0000
HCINT3	0xEC00_0568	R/W	Specifies the Host Channel 3 Interrupt Register	0x0000_0000
HCINTMSK3	0xEC00_056C	R/W	Specifies the Host Channel 3 Interrupt Mask Register	0x0000_0000
HCTSIZ3	0xEC00_0570	R/W	Specifies the Host Channel 3 Transfer Size Register	0x0000_0000
HCDMA3	0xEC00_0574	R/W	Specifies the Host Channel 3 DMA Address Register	0x0000_0000
HCCHAR4	0xEC00_0580	R/W	Specifies the Host Channel 4 Characteristics Register	0x0000_0000
HCSPLT4	0xEC00_0584	R/W	Specifies the Host Channel 4 Spilt Control Register	0x0000_0000
HCINT4	0xEC00_0588	R/W	Specifies the Host Channel 4 Interrupt Register	0x0000_0000
HCINTMSK4	0xEC00_058C	R/W	Specifies the Host Channel 4 Interrupt Mask Register	0x0000_0000
HCTSIZ4	0xEC00_0580	R/W	Specifies the Host Channel 4 Transfer Size Register	0x0000_0000
HCDMA4	0xEC00_0584	R/W	Specifies the Host Channel 4 DMA Address Register	0x0000_0000

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Register	Address	R/W	Description	Reset Value
HCCHAR5	0xEC00_05A0	R/W	Specifies the Host Channel 5 Characteristics Register	0x0000_0000
HCSPLT5	0xEC00_05A4	R/W	Specifies the Host Channel 5 Spilt Control Register	0x0000_0000
HCINT5	0xEC00_05A8	R/W	Specifies the Host Channel 5 Interrupt Register	0x0000_0000
HCINTMSK5	0xEC00_05AC	R/W	Specifies the Host Channel 5 Interrupt Mask Register	0x0000_0000
HCTSIZ5	0xEC00_05B0	R/W	Specifies the Host Channel 5 Transfer Size Register	0x0000_0000
HCDMA5	0xEC00_05B4	R/W	Specifies the Host Channel 5 DMA Address Register	0x0000_0000
HCCHAR6	0xEC00_05C0	R/W	Specifies the Host Channel 6 Characteristics Register	0x0000_0000
HCSPLT6	0xEC00_05C4	R/W	Specifies the Host Channel 6 Spilt Control Register	0x0000_0000
HCINT6	0xEC00_05C8	R/W	Specifies the Host Channel 6 Interrupt Register	0x0000_0000
HCINTMSK6	0xEC00_05CC	R/W	Specifies the Host Channel 6 Interrupt Mask Register	0x0000_0000
HCTSIZ6	0xEC00_05D0	R/W	Specifies the Host Channel 6 Transfer Size Register	0x0000_0000
HCDMA6	0xEC00_05D4	R/W	Specifies the Host Channel 6 DMA Address Register	0x0000_0000
HCCHAR7	0xEC00_05E0	R/W	Specifies the Host Channel 7 Characteristics Register	0x0000_0000
HCSPLT7	0xEC00_05E4	R/W	Specifies the Host Channel 7 Spilt Control Register	0x0000_0000
HCINT7	0xEC00_05E8	R/W	Specifies the Host Channel 7 Interrupt Register	0x0000_0000
HCINTMSK7	0xEC00_05EC	R/W	Specifies the Host Channel 7 Interrupt Mask Register	0x0000_0000
HCTSIZ7	0xEC00_05F0	R/W	Specifies the Host Channel 7 Transfer Size Register	0x0000_0000
HCDMA7	0xEC00_05F4	R/W	Specifies the Host Channel 7 DMA Address Register	0x0000_0000
HCCHAR8	0xEC00_0600	R/W	Specifies the Host Channel 8 Characteristics Register	0x0000_0000
HCSPLT8	0xEC00_0604	R/W	Specifies the Host Channel 8 Spilt Control Register	0x0000_0000
HCINT8	0xEC00_0608	R/W	Specifies the Host Channel 8 Interrupt Register	0x0000_0000
HCINTMSK8	0xEC00_060C	R/W	Specifies the Host Channel 8 Interrupt Mask Register	0x0000_0000
HCTSIZ8	0xEC00_0610	R/W	Specifies the Host Channel 8 Transfer Size Register	0x0000_0000
HCDMA8	0xEC00_0614	R/W	Specifies the Host Channel 8 DMA Address Register	0x0000_0000
HCCHAR9	0xEC00_0620	R/W	Specifies the Host Channel 9 Characteristics	0x0000_0000

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Register	Address	R/W	Description	Reset Value
			Register	
HCSPLT9	0xEC00_0624	R/W	Specifies the Host Channel 9 Spilt Control Register	0x0000_0000
HCINT9	0xEC00_0628	R/W	Specifies the Host Channel 9 Interrupt Register	0x0000_0000
HCINTMSK9	0xEC00_062C	R/W	Specifies the Host Channel 9 Interrupt Mask Register	0x0000_0000
HCTSIZ9	0xEC00_0630	R/W	Specifies the Host Channel 9 Transfer Size Register	0x0000_0000
HCDMA9	0xEC00_0634	R/W	Specifies the Host Channel 9 DMA Address Register	0x0000_0000
HCCHAR10	0xEC00_0640	R/W	Specifies the Host Channel 10 Characteristics Register	0x0000_0000
HCSPLT10	0xEC00_0644	R/W	Specifies the Host Channel 10 Spilt Control Register	0x0000_0000
HCINT10	0xEC00_0648	R/W	Specifies the Host Channel 10 Interrupt Register	0x0000_0000
HCINTMSK10	0xEC00_064C	R/W	Specifies the Host Channel 10 Interrupt Mask Register	0x0000_0000
HCTSIZ10	0xEC00_0650	R/W	Specifies the Host Channel 10 Transfer Size Register	0x0000_0000
HCDMA10	0xEC00_0654	R/W	Specifies the Host Channel 10 DMA Address Register	0x0000_0000
HCCHAR11	0xEC00_0660	R/W	Specifies the Host Channel 11 Characteristics Register	0x0000_0000
HCSPLT11	0xEC00_0664	R/W	Specifies the Host Channel 11 Spilt Control Register	0x0000_0000
HCINT11	0xEC00_0668	R/W	Specifies the Host Channel 11 Interrupt Register	0x0000_0000
HCINTMSK11	0xEC00_066C	R/W	Specifies the Host Channel 11 Interrupt Mask Register	0x0000_0000
HCTSIZ11	0xEC00_0670	R/W	Specifies the Host Channel 11 Transfer Size Register	0x0000_0000
HCDMA11	0xEC00_0674	R/W	Specifies the Host Channel 11 DMA Address Register	0x0000_0000
HCCHAR12	0xEC00_0680	R/W	Specifies the Host Channel 12 Characteristics Register	0x0000_0000
HCSPLT12	0xEC00_0684	R/W	Specifies the Host Channel 12 Spilt Control Register	0x0000_0000
HCINT12	0xEC00_0688	R/W	Specifies the Host Channel 12 Interrupt Register	0x0000_0000
HCINTMSK12	0xEC00_068C	R/W	Specifies the Host Channel 12 Interrupt Mask Register	0x0000_0000
HCTSIZ12	0xEC00_0690	R/W	Specifies the Host Channel 12 Transfer Size Register	0x0000_0000
HCDMA12	0xEC00_0694	R/W	Specifies the Host Channel 12 DMA Address Register	0x0000_0000

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Register	Address	R/W	Description	Reset Value
HCCHAR13	0xEC00_06A0	R/W	Specifies the Host Channel 13 Characteristics Register	0x0000_0000
HCSPLT13	0xEC00_06A4	R/W	Specifies the Host Channel 13 Spilt Control Register	0x0000_0000
HCINT13	0xEC00_06A8	R/W	Specifies the Host Channel 13 Interrupt Register	0x0000_0000
HCINTMSK13	0xEC00_06AC	R/W	Specifies the Host Channel 13 Interrupt Mask Register	0x0000_0000
HCTSIZ13	0xEC00_06B0	R/W	Specifies the Host Channel 13 Transfer Size Register	0x0000_0000
HCDMA13	0xEC00_06B4	R/W	Specifies the Host Channel 13 DMA Address Register	0x0000_0000
HCCHAR14	0xEC00_06C0	R/W	Specifies the Host Channel 14 Characteristics Register	0x0000_0000
HCSPLT14	0xEC00_06C4	R/W	Specifies the Host Channel 14 Spilt Control Register	0x0000_0000
HCINT14	0xEC00_06C8	R/W	Specifies the Host Channel 14 Interrupt Register	0x0000_0000
HCINTMSK14	0xEC00_06CC	R/W	Specifies the Host Channel 14 Interrupt Mask Register	0x0000_0000
HCTSIZ14	0xEC00_06D0	R/W	Specifies the Host Channel 14 Transfer Size Register	0x0000_0000
HCDMA14	0xEC00_06D4	R/W	Specifies the Host Channel 14 DMA Address Register	0x0000_0000
HCCHAR15	0xEC00_06E0	R/W	Specifies the Host Channel 15 Characteristics Register	0x0000_0000
HCSPLT15	0xEC00_06E4	R/W	Specifies the Host Channel 15 Spilt Control Register	0x0000_0000
HCINT15	0xEC00_06E8	R/W	Specifies the Host Channel 15 Interrupt Register	0x0000_0000
HCINTMSK15	0xEC00_06EC	R/W	Specifies the Host Channel 15 Interrupt Mask Register	0x0000_0000
HCTSIZ15	0xEC00_06F0	R/W	Specifies the Host Channel 15 Transfer Size Register	0x0000_0000
HCDMA15	0xEC00_06F4	R/W	Specifies the Host Channel 15 DMA Address Register	0x0000_0000
Device Mode Registers (Device Global Registers)				
DCFG	0xEC00_0800	R/W	Specifies the Device Configuration Register	0x0820_0000
DCTL	0xEC00_0804	R/W	Specifies the Device Control Register	0x0000_0000
DSTS	0xEC00_0808	R	Specifies the Device Status Register	0x0000_0002
DIEPMSK	0xEC00_0810	R/W	Specifies the Device IN Endpoint Common Interrupt Mask Register	0x0000_0000
DOEPMSK	0xEC00_0814	R/W	Specifies the Device OUT Endpoint Common Interrupt Mask Register	0x0000_0000

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Register	Address	R/W	Description	Reset Value
DAINT	0xEC00_0818	R	Specifies the Device ALL Endpoints Interrupt Register	0x0000_0000
DAINTMSK	0xEC00_081C	R/W	Specifies the Device ALL Endpoints Interrupt Mask Register	0x0000_0000
DVBUSDIS	0xEC00_0828	R/W	Specifies the Device VBUS Discharge Time Register	0x0000_0B8F
DVBUSPULSE	0xEC00_082C	R/W	Specifies the Device VBUS Pulsing Time Register	0x0000_02C6
DTHRCTL	0xEC00_0830	R/W	Specifies the Device Threshold Control Register	0x0C10_0020
DIEPEMPMSK	0xEC00_0834	R/W	Specifies the Device IN Endpoint FIFO EMPTY Interrupt Mask Register	0x0000_0000
Device Mode Registers (Device Logical IN Endpoint-Specific Registers)				
DIEPCTL0	0xEC00_0900	R/W	Specifies the Device Control IN Endpoint 0 Control Register	0x0000_8000
DIEPINT0	0xEC00_0908	R/W	Specifies the Device IN Endpoint 0 Interrupt Register	0x0000_0000
DIEPTSIZ0	0xEC00_0910	R/W	Specifies the Device IN Endpoint 0 Transfer Size Register	0x0000_0000
DIEPDMA0	0xEC00_0914	R/W	Specifies the Device IN Endpoint 0 DMA Address Register	0x0000_0000
DTXFSTS0	0xEC00_0918	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB0	0xEC00_091C	R	Specifies the Device IN Endpoint 0 DMA Buffer Address Register	0x0000_0000
DIEPCTL1	0xEC00_0920	R/W	Specifies the Device Control IN Endpoint 1 Control Register	0x0000_0000
DIEPINT1	0xEC00_0928	R/W	Specifies the Device IN Endpoint 1 Interrupt Register	0x0000_0080
DIEPTSIZ1	0xEC00_0930	R/W	Specifies the Device IN Endpoint 1 Transfer Size Register	0x0000_0000
DIEPDMA1	0xEC00_0934	R/W	Specifies the Device IN Endpoint 1 DMA Address Register	0x0000_0000
DTXFSTS1	0xEC00_0938	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB1	0xEC00_093C	R	Specifies the Device IN Endpoint 1 DMA Buffer Address Register	0x0000_0000
DIEPCTL2	0xEC00_0940	R/W	Specifies the Device Control IN Endpoint 2 Control Register	0x0000_0000
DIEPINT2	0xEC00_0948	R/W	Specifies the Device IN Endpoint 2 Interrupt Register	0x0000_0080
DIEPTSIZ2	0xEC00_0950	R/W	Specifies the Device IN Endpoint 2 Transfer Size Register	0x0000_0000
DIEPDMA2	0xEC00_0954	R/W	Specifies the Device IN Endpoint 2 DMA Address	0x0000_0000

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Register	Address	R/W	Description	Reset Value
			Register	
DTXFSTS2	0xEC00_0958	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB2	0xEC00_095C	R	Specifies the Device IN Endpoint 2 DMA Buffer Address Register	0x0000_0000
DIEPCTL3	0xEC00_0960	R/W	Specifies the Device Control IN Endpoint 3 Control Register	0x0000_0000
DIEPINT3	0xEC00_0968	R/W	Specifies the Device IN Endpoint 3 Interrupt Register	0x0000_0080
DIEPTSIZ3	0xEC00_0970	R/W	Specifies the Device IN Endpoint 3 Transfer Size Register	0x0000_0000
DIEPDMA3	0xEC00_0974	R/W	Specifies the Device IN Endpoint 3 DMA Address Register	0x0000_0000
DTXFSTS3	0xEC00_0978	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB3	0xEC00_097C	R	Specifies the Device IN Endpoint 3 DMA Buffer Address Register	0x0000_0000
DIEPCTL4	0xEC00_0980	R/W	Specifies the Device Control IN Endpoint 4 Control Register	0x0000_0000
DIEPINT4	0xEC00_0988	R/W	Specifies the Device IN Endpoint 4 Interrupt Register	0x0000_0080
DIEPTSIZ4	0xEC00_0990	R/W	Specifies the Device IN Endpoint 4 Transfer Size Register	0x0000_0000
DIEPDMA4	0xEC00_0994	R/W	Specifies the Device IN Endpoint 4 DMA Address Register	0x0000_0000
DTXFSTS4	0xEC00_0998	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB4	0xEC00_099C	R	Specifies the Device IN Endpoint 4 DMA Buffer Address Register	0x0000_0000
DIEPCTL5	0xEC00_09A0	R/W	Specifies the Device Control IN Endpoint 5 Control Register	0x0000_0000
DIEPINT5	0xEC00_09A8	R/W	Specifies the Device IN Endpoint 5 Interrupt Register	0x0000_0080
DIEPTSIZ5	0xEC00_09B0	R/W	Specifies the Device IN Endpoint 5 Transfer Size Register	0x0000_0000
DIEPDMA5	0xEC00_09B4	R/W	Specifies the Device IN Endpoint 5 DMA Address Register	0x0000_0000
DTXFSTS5	0xEC00_09B8	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB5	0xEC00_09BC	R	Specifies the Device IN Endpoint 5 DMA Buffer Address Register	0x0000_0000
DIEPCTL6	0xEC00_09C0	R/W	Specifies the Device Control IN Endpoint 6 Control Register	0x0000_0000

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Register	Address	R/W	Description	Reset Value
DIEPINT6	0xEC00_09C8	R/W	Specifies the Device IN Endpoint 6 Interrupt Register	0x0000_0080
DIEPTSIZ6	0xEC00_09D0	R/W	Specifies the Device IN Endpoint 6 Transfer Size Register	0x0000_0000
DIEPDMA6	0xEC00_09D4	R/W	Specifies the Device IN Endpoint 6 DMA Address Register	0x0000_0000
DTXFSTS6	0xEC00_09D8	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB6	0xEC00_09DC	R	Specifies the Device IN Endpoint 6 DMA Buffer Address Register	0x0000_0000
DIEPCTL7	0xEC00_09E0	R/W	Specifies the Device Control IN Endpoint 7 Control Register	0x0000_0000
DIEPINT7	0xEC00_09E8	R/W	Specifies the Device IN Endpoint 7 Interrupt Register	0x0000_0080
DIEPTSIZ7	0xEC00_09F0	R/W	Specifies the Device IN Endpoint 7 Transfer Size Register	0x0000_0000
DIEPDMA7	0xEC00_09F4	R/W	Specifies the Device IN Endpoint 7 DMA Address Register	0x0000_0000
DTXFSTS7	0xEC00_09F8	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB7	0xEC00_09FC	R	Specifies the Device IN Endpoint 7 DMA Buffer Address Register	0x0000_0000
DIEPCTL8	0xEC00_0A00	R/W	Specifies the Device Control IN Endpoint 8 Control Register	0x0000_0000
DIEPINT8	0xEC00_0A08	R/W	Specifies the Device IN Endpoint 8 Interrupt Register	0x0000_0080
DIEPTSIZ8	0xEC00_0A10	R/W	Specifies the Device IN Endpoint 8 Transfer Size Register	0x0000_0000
DIEPDMA8	0xEC00_0A14	R/W	Specifies the Device IN Endpoint 8 DMA Address Register	0x0000_0000
DTXFSTS8	0xEC00_0A18	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB8	0xEC00_0A1C	R	Specifies the Device IN Endpoint 8 DMA Buffer Address Register	0x0000_0000
DIEPCTL9	0xEC00_0A20	R/W	Specifies the Device Control IN Endpoint 9 Control Register	0x0000_0000
DIEPINT9	0xEC00_0A28	R/W	Specifies the Device IN Endpoint 9 Interrupt Register	0x0000_0080
DIEPTSIZ9	0xEC00_0A30	R/W	Specifies the Device IN Endpoint 9 Transfer Size Register	0x0000_0000
DIEPDMA9	0xEC00_0A34	R/W	Specifies the Device IN Endpoint 9 DMA Address Register	0x0000_0000
DTXFSTS9	0xEC00_0A38	R	Specifies the Device IN Endpoint Transmit FIFO	0x0000_0100

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Register	Address	R/W	Description	Reset Value
			Status Register	
DIEPDMAB9	0xEC00_0A3C	R	Specifies the Device IN Endpoint 9 DMA Buffer Address Register	0x0000_0000
DIEPCTL10	0xEC00_0A40	R/W	Specifies the Device Control IN Endpoint 10 Control Register	0x0000_0000
DIEPINT10	0xEC00_0A48	R/W	Specifies the Device IN Endpoint 10 Interrupt Register	0x0000_0080
DIEPTSIZ10	0xEC00_0A50	R/W	Specifies the Device IN Endpoint 10 Transfer Size Register	0x0000_0000
DIEPDMA10	0xEC00_0A54	R/W	Specifies the Device IN Endpoint 10 DMA Address Register	0x0000_0000
DTXFSTS10	0xEC00_0A58	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB10	0xEC00_0A5C	R	Specifies the Device IN Endpoint 10 DMA Buffer Address Register	0x0000_0000
DIEPCTL11	0xEC00_0A60	R/W	Specifies the Device Control IN Endpoint 11 Control Register	0x0000_0000
DIEPINT11	0xEC00_0A68	R/W	Specifies the Device IN Endpoint 11 Interrupt Register	0x0000_0080
DIEPTSIZ11	0xEC00_0A70	R/W	Specifies the Device IN Endpoint 11 Transfer Size Register	0x0000_0000
DIEPDMA11	0xEC00_0A74	R/W	Specifies the Device IN Endpoint 11 DMA Address Register	0x0000_0000
DTXFSTS11	0xEC00_0A78	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB11	0xEC00_0A7C	R	Specifies the Device IN Endpoint 11 DMA Buffer Address Register	0x0000_0000
DIEPCTL12	0xEC00_0A80	R/W	Specifies the Device Control IN Endpoint 12 Control Register	0x0000_0000
DIEPINT12	0xEC00_0A88	R/W	Specifies the Device IN Endpoint 12 Interrupt Register	0x0000_0080
DIEPTSIZ12	0xEC00_0A90	R/W	Specifies the Device IN Endpoint 12 Transfer Size Register	0x0000_0000
DIEPDMA12	0xEC00_0A94	R/W	Specifies the Device IN Endpoint 12 DMA Address Register	0x0000_0000
DTXFSTS12	0xEC00_0A98	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB12	0xEC00_0A9C	R	Specifies the Device IN Endpoint 12 DMA Buffer Address Register	0x0000_0000
DIEPCTL13	0xEC00_0AA0	R/W	Specifies the Device Control IN Endpoint 13 Control Register	0x0000_0000
DIEPINT13	0xEC00_0AA8	R/W	Specifies the Device IN Endpoint 13 Interrupt Register	0x0000_0080

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Register	Address	R/W	Description	Reset Value
DIEPTSIZ13	0xEC00_0AB0	R/W	Specifies the Device IN Endpoint 13 Transfer Size Register	0x0000_0000
DIEPDMA13	0xEC00_0AB4	R/W	Specifies the Device IN Endpoint 13 DMA Address Register	0x0000_0000
DTXFSTS13	0xEC00_0AB8	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB13	0xEC00_0ABC	R	Specifies the Device IN Endpoint 13 DMA Buffer Address Register	0x0000_0000
DIEPCTL14	0xEC00_0AC0	R/W	Specifies the Device Control IN Endpoint 14 Control Register	0x0000_0000
DIEPINT14	0xEC00_0AC8	R/W	Specifies the Device IN Endpoint 14 Interrupt Register	0x0000_0080
DIEPTSIZ14	0xEC00_0AD0	R/W	Specifies the Device IN Endpoint 14 Transfer Size Register	0x0000_0000
DIEPDMA14	0xEC00_0AD4	R/W	Specifies the Device IN Endpoint 14 DMA Address Register	0x0000_0000
DTXFSTS14	0xEC00_0AD8	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB14	0xEC00_0ADC	R	Specifies the Device IN Endpoint 14 DMA Buffer Address Register	0x0000_0000
DIEPCTL15	0xEC00_0AE0	R/W	Specifies the Device Control IN Endpoint 15 Control Register	0x0000_0000
DIEPINT15	0xEC00_0AE8	R/W	Specifies the Device IN Endpoint 15 Interrupt Register	0x0000_0080
DIEPTSIZ15	0xEC00_0AF0	R/W	Specifies the Device IN Endpoint 15 Transfer Size Register	0x0000_0000
DIEPDMA15	0xEC00_0AF4	R/W	Specifies the Device IN Endpoint 15 DMA Address Register	0x0000_0000
DTXFSTS15	0xEC00_0AF8	R	Specifies the Device IN Endpoint Transmit FIFO Status Register	0x0000_0100
DIEPDMAB15	0xEC00_0AFC	R	Specifies the Device IN Endpoint 15 DMA Buffer Address Register	0x0000_0000
Device Mode Registers (Device Logical OUT Endpoint-Specific Registers)				
DOEPCTL0	0xEC00_0B00	R/W	Specifies the Device Control OUT Endpoint 0 Control Register	0x0000_8000
DOEPINT0	0xEC00_0B08	R/W	Specifies the Device OUT Endpoint 0 Interrupt Register	0x0000_0000
DOEPTSIZ0	0xEC00_0B10	R/W	Specifies the Device OUT Endpoint 0 Transfer Size Register	0x0000_0000
DOEPDMA0	0xEC00_0B14	R/W	Specifies the Device OUT Endpoint 0 DMA Address Register	0x0000_0000
DOEPDMAB0	0xEC00_0B1C	R	Specifies the Device OUT Endpoint 0 DMA Buffer Address Register	0x0000_0000

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Register	Address	R/W	Description	Reset Value
DOEPCTL1	0xEC00_0B20	R/W	Specifies the Device Control OUT Endpoint 1 Control Register	0x0000_0000
DOEPINT1	0xEC00_0B28	R/W	Specifies the Device OUT Endpoint 1 Interrupt Register	0x0000_0000
DOEPTSIZ1	0xEC00_0B30	R/W	Specifies the Device OUT Endpoint 1 Transfer Size Register	0x0000_0000
DOEPDMA1	0xEC00_0B34	R/W	Specifies the Device OUT Endpoint 1 DMA Address Register	0x0000_0000
DOEPDMAB1	0xEC00_0B3C	R	Specifies the Device OUT Endpoint 1 DMA Buffer Address Register	0x0000_0000
DOEPCTL2	0xEC00_0B40	R/W	Specifies the Device Control OUT Endpoint 2 Control Register	0x0000_0000
DOEPINT2	0xEC00_0B48	R/W	Specifies the Device OUT Endpoint 2 Interrupt Register	0x0000_0000
DOEPTSIZ2	0xEC00_0B50	R/W	Specifies the Device OUT Endpoint 2 Transfer Size Register	0x0000_0000
DOEPDMA2	0xEC00_0B54	R/W	Specifies the Device OUT Endpoint 2 DMA Address Register	0x0000_0000
DOEPDMAB2	0xEC00_0B5C	R	Specifies the Device OUT Endpoint 2 DMA Buffer Address Register	0x0000_0000
DOEPCTL3	0xEC00_0B60	R/W	Specifies the Device Control OUT Endpoint 3 Control Register	0x0000_0000
DOEPINT3	0xEC00_0B68	R/W	Specifies the Device OUT Endpoint 3 Interrupt Register	0x0000_0000
DOEPTSIZ3	0xEC00_0B70	R/W	Specifies the Device OUT Endpoint 3 Transfer Size Register	0x0000_0000
DOEPDMA3	0xEC00_0B74	R/W	Specifies the Device OUT Endpoint 3 DMA Address Register	0x0000_0000
DOEPDMAB3	0xEC00_0B7C	R	Specifies the Device OUT Endpoint 3 DMA Buffer Address Register	0x0000_0000
DOEPCTL4	0xEC00_0B80	R/W	Specifies the Device Control OUT Endpoint 4 Control Register	0x0000_0000
DOEPINT4	0xEC00_0B88	R/W	Specifies the Device OUT Endpoint 4 Interrupt Register	0x0000_0000
DOEPTSIZ4	0xEC00_0B90	R/W	Specifies the Device OUT Endpoint 4 Transfer Size Register	0x0000_0000
DOEPDMA4	0xEC00_0B94	R/W	Specifies the Device OUT Endpoint 4 DMA Address Register	0x0000_0000
DOEPDMAB4	DOEPDMAB4	R	Specifies the Device OUT Endpoint 4 DMA Buffer Address Register	0x0000_0000
DOEPCTL5	0xEC00_0BA0	R/W	Specifies the Device Control OUT Endpoint 5 Control Register	0x0000_0000
DOEPINT5	0xEC00_0BA8	R/W	Specifies the Device OUT Endpoint 5 Interrupt	0x0000_0000

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Register	Address	R/W	Description	Reset Value
			Register	
DOEPTSIZ5	0xEC00_0BB0	R/W	Specifies the Device OUT Endpoint 5 Transfer Size Register	0x0000_0000
DOEPDMA5	0xEC00_0BB4	R/W	Specifies the Device OUT Endpoint 5 DMA Address Register	0x0000_0000
DOEPDMAB5	0xEC00_0BBC	R	Specifies the Device OUT Endpoint 5 DMA Buffer Address Register	0x0000_0000
DOEPCTL6	0xEC00_0BC0	R/W	Specifies the Device Control OUT Endpoint 6 Control Register	0x0000_0000
DOEPINT6	0xEC00_0BC8	R/W	Specifies the Device OUT Endpoint 6 Interrupt Register	0x0000_0000
DOEPTSIZ6	0xEC00_0BD0	R/W	Specifies the Device OUT Endpoint 6 Transfer Size Register	0x0000_0000
DOEPDMA6	0xEC00_0BD4	R/W	Specifies the Device OUT Endpoint 6 DMA Address Register	0x0000_0000
DOEPDMAB6	0xEC00_0BDC	R	Specifies the Device OUT Endpoint 6 DMA Buffer Address Register	0x0000_0000
DOEPCTL7	0xEC00_0BE0	R/W	Specifies the Device Control OUT Endpoint 7 Control Register	0x0000_0000
DOEPINT7	0xEC00_0BE8	R/W	Specifies the Device OUT Endpoint 7 Interrupt Register	0x0000_0000
DOEPTSIZ7	0xEC00_0BF0	R/W	Specifies the Device OUT Endpoint 7 Transfer Size Register	0x0000_0000
DOEPDMA7	0xEC00_0BF4	R/W	Specifies the Device OUT Endpoint 7 DMA Address Register	0x0000_0000
DOEPDMAB7	0xEC00_0BFC	R	Specifies the Device OUT Endpoint 7 DMA Buffer Address Register	0x0000_0000
DOEPCTL8	0xEC00_0C00	R/W	Specifies the Device Control OUT Endpoint 8 Control Register	0x0000_0000
DOEPINT8	0xEC00_0C08	R/W	Specifies the Device OUT Endpoint 8 Interrupt Register	0x0000_0000
DOEPTSIZ8	0xEC00_0C10	R/W	Specifies the Device OUT Endpoint 8 Transfer Size Register	0x0000_0000
DOEPDMA8	0xEC00_0C14	R/W	Specifies the Device OUT Endpoint 8 DMA Address Register	0x0000_0000
DOEPDMAB8	0xEC00_0C1C	R	Specifies the Device OUT Endpoint 8 DMA Buffer Address Register	0x0000_0000
DOEPCTL9	0xEC00_0C20	R/W	Specifies the Device Control OUT Endpoint 9 Control Register	0x0000_0000
DOEPINT9	0xEC00_0C28	R/W	Specifies the Device OUT Endpoint 9 Interrupt Register	0x0000_0000
DOEPTSIZ9	0xEC00_0C30	R/W	Specifies the Device OUT Endpoint 9 Transfer Size Register	0x0000_0000

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Register	Address	R/W	Description	Reset Value
DOEPDMA9	0xEC00_0C34	R/W	Specifies the Device OUT Endpoint 9 DMA Address Register	0x0000_0000
DOEPDMAB9	0xEC00_0C31C	R	Specifies the Device OUT Endpoint 9 DMA Buffer Address Register	0x0000_0000
DOEPCTL10	0xEC00_0C40	R/W	Specifies the Device Control OUT Endpoint 10 Control Register	0x0000_0000
DOEPINT10	0xEC00_0C48	R/W	Specifies the Device OUT Endpoint 10 Interrupt Register	0x0000_0000
DOEPTSIZ10	0xEC00_0C50	R/W	Specifies the Device OUT Endpoint 10 Transfer Size Register	0x0000_0000
DOEPDMA10	0xEC00_0C54	R/W	Specifies the Device OUT Endpoint 10 DMA Address Register	0x0000_0000
DOEPDMAB10	0xEC00_0C5C	R	Specifies the Device OUT Endpoint 10 DMA Buffer Address Register	0x0000_0000
DOEPCTL11	0xEC00_0C60	R/W	Specifies the Device Control OUT Endpoint 11 Control Register	0x0000_0000
DOEPINT11	0xEC00_0C68	R/W	Specifies the Device OUT Endpoint 11 Interrupt Register	0x0000_0000
DOEPTSIZ11	0xEC00_0C70	R/W	Specifies the Device OUT Endpoint 11 Transfer Size Register	0x0000_0000
DOEPDMA11	0xEC00_0C74	R/W	Specifies the Device OUT Endpoint 11 DMA Address Register	0x0000_0000
DOEPDMAB11	0xEC00_0C7C	R	Specifies the Device OUT Endpoint 11 DMA Buffer Address Register	0x0000_0000
DOEPCTL12	0xEC00_0C80	R/W	Specifies the Device Control OUT Endpoint 12 Control Register	0x0000_0000
DOEPINT12	0xEC00_0C88	R/W	Specifies the Device OUT Endpoint 12 Interrupt Register	0x0000_0000
DOEPTSIZ12	0xEC00_0C90	R/W	Specifies the Device OUT Endpoint 12 Transfer Size Register	0x0000_0000
DOEPDMA12	0xEC00_0C94	R/W	Specifies the Device OUT Endpoint 12 DMA Address Register	0x0000_0000
DOEPDMAB12	0xEC00_0C9C	R	Specifies the Device OUT Endpoint 12 DMA Buffer Address Register	0x0000_0000
DOEPCTL13	0xEC00_0CA0	R/W	Specifies the Device Control OUT Endpoint 13 Control Register	0x0000_0000
DOEPINT13	0xEC00_0CA8	R/W	Specifies the Device OUT Endpoint 13 Interrupt Register	0x0000_0000
DOEPTSIZ13	0xEC00_0CB0	R/W	Specifies the Device OUT Endpoint 13 Transfer Size Register	0x0000_0000
DOEPDMA13	0xEC00_0CB4	R/W	Specifies the Device OUT Endpoint 13 DMA Address Register	0x0000_0000
DOEPDMAB13	0xEC00_0CBC	R	Specifies the Device OUT Endpoint 13 DMA Buffer	0x0000_0000

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Register	Address	R/W	Description	Reset Value
			Address Register	
DOEPCTL14	0xEC00_0CC0	R/W	Specifies the Device Control OUT Endpoint 14 Control Register	0x0000_0000
DOEPINT14	0xEC00_0CC8	R/W	Specifies the Device OUT Endpoint 14 Interrupt Register	0x0000_0000
DOEPTSIZ14	0xEC00_0CD0	R/W	Specifies the Device OUT Endpoint 14 Transfer Size Register	0x0000_0000
DOEPDMA14	0xEC00_0CD4	R/W	Specifies the Device OUT Endpoint 14 DMA Address Register	0x0000_0000
DOEPDMAB14	0xEC00_0CDC	R	Specifies the Device OUT Endpoint 14 DMA Buffer Address Register	0x0000_0000
DOEPCTL15	0xEC00_0CE0	R/W	Specifies the Device Control OUT Endpoint 15 Control Register	0x0000_0000
DOEPINT15	0xEC00_0CE8	R/W	Specifies the Device OUT Endpoint 15 Interrupt Register	0x0000_0000
DOEPTSIZ15	0xEC00_0CF0	R/W	Specifies the Device OUT Endpoint 15 Transfer Size Register	0x0000_0000
DOEPDMA15	0xEC00_0CF4	R/W	Specifies the Device OUT Endpoint 15 DMA Address Register	0x0000_0000
DOEPDMAB15	0xEC00_0CFC	R	Specifies the Device OUT Endpoint 15 DMA Buffer Address Register	0x0000_0000

NOTE: All HS OTG Controller registers are accessible by word unit with STR/ LDR instructions.

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5.8.2 USB PHY CONTROL REGISTERS

5.8.2.1 USB PHY Power Control Register (UPHYPWR, R/W, Address = 0xEC10_0000)

UPHYPWR	Bit	Description	R/W	Initial State
Reserved	[31:9]	-	-	23'b0
Reserved	[8]	Reserved, but should be 0x1	-	1'b1
Analog _powerdown1	[7]	USBPHY1, Analog block power down • 1'b0: Analog block power up (Normal Operation) • 1'b1: Analog block power down	R/W	1'b1
force_suspend1	[6]	USBPHY1, Apply Suspend signal to save power • 1'b0: Disables (Normal Operation) • 1'b1: Enables	R/W	1'b1
Reserved	[5]	Reserved, but should be 0x1	-	1'b1
otg_disable_0	[4]	USBPHY0, OTG block power down • 1'b0: OTG block power up • 1'b1: OTG block power down If the application does not use OTG functionality, you can set this input high to save power.	-	1'b1
Analog _powerdown_0	[3]	USBPHY0, Analog block power down • 1'b0: Analog block power up (Normal Operation) • 1'b1: Analog block power down	R/W	1'b1
Reserved	[2:1]	-	-	2b'0
force_suspend_0	[0]	USBPHY0, Apply Suspend signal for to save power save • 1'b0: Disables (Normal Operation) • 1'b1: Enables	R/W	1'b1

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5.8.2.2 USB PHY Clock Control Register (UPHYCLK, R/W, Address = 0xEC10_0004)

UPHYCLK	Bit	Description	R/W	Initial State
Reserved	[31:7]	-	-	25'h0
common_on_n1	[7]	USBPHY1, Force XO, Bias, Bandgap, and PLL to Remain Powered During a Suspend This bit controls the power-down signals of sub-blocks in the Common block if the USB PHY1 is suspended. • 1'b0: 48MHz clock on clk48m_ohci is available at all times, except in Suspend mode. • 1'b1: 48MHz clock on clk48m_ohci is available at all times, even in Suspend mode.	R/W	1'b0
Reserved	[6:5]	-	-	
common_on_n0	[4]	USBPHY0, Force XO, Bias, Bandgap, and PLL to Remain Powered During a Suspend This bit controls the power-down signals of sub-blocks in the Common block if the USB PHY0 is suspended. • 1'b0: 48MHz clock on clk48m_ohci is available at all times, except in Suspend mode. • 1'b1: 48MHz clock on clk48m_ohci is available at all times, even in Suspend mode.	R/W	1'b0
Reserved	[3]	-	-	1'b0
id_pullup0	[2]	USBPHY0, Analog ID Input Sample Enable • 1'b0: id_dig disable. • 1'b1: id_dig enable. (The id_dig output is valid, and within 20ms, id_dig must indicate the type of plug connected.)	R/W	1'b0
clk_sel	[1:0]	USBPHY0 &1 Reference Clock Frequency Select for PLL • 2'b00: 48MHz • 2'b01: Reserved • 2'b10: 12MHz • 2'b11: 24MHz	R/W	2'b00

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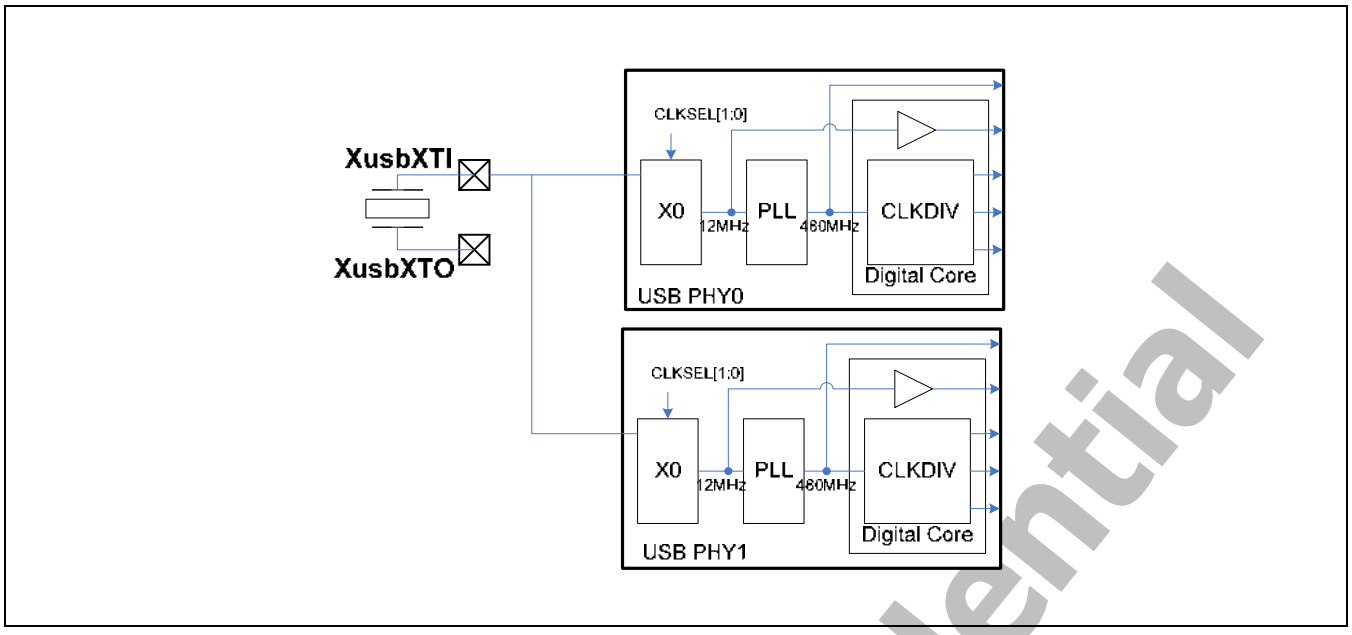

Figure 5-4 USB PHY Clock Path

5.8.2.3 USB Reset Control Register (URSTCON, R/W, Address = 0xEC10_0008)

URSTCON	Bit	Description	R/W	Initial State
Reserved	[31:5]	-	-	29'h0
host_sw_rst	[4]	USB Host LINK S/W Reset	R/W	1'b0
phy_sw_rst1	[3]	USB PHY1, USB Host LINK S/W Reset The phy1_sw_rst signal must by asserted for at least 10us	R/W	1'b1
phylnk_sw_rst	[2]	OTG Link Core phy_clock domain S/W Reset	R/W	1'b0
link_sw_rst	[1]	OTG Link Core hclk domain S/W Reset	R/W	1'b0
phy_sw_rst0	[0]	USBPHY0 , LINK 2.0 S/W Reset The phy_sw_rst0 signal must be asserted for at least 10us	R/W	1'b1

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5.8.2.4 PHY Tune Register (PHY_TUNE, R/W, Address = 0xEC10_0020, 0xEC10_0024)

Caution: USB PHY1:0XEC10_0020, USB PHY0: 0XEC10_0024

UPHYTUNE0, 1	Bit	Description	R/W	Initial State
Reserved	[31:21]	-	-	11'h0
Reserved	[20:17]	Reserved, but should be 4’b0100	-	4'b0100
Otgtune	[16:14]	VBUS Valid Threshold Adjustment. This bit adjusts the voltage level for the VBUS Valid threshold in USBPHY-n. • 111: Reserved • 110: Reserved • 101: Reserved • 100: Design default • 011: Reserved • 010: Reserved • 001: Reserved • 000: -6%	R/W	3'b100
Reserved	[13:0]	Reserved, but should be 0x19B3	-	14’h19B3

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5.8.3 OTG LINK CORE REGISTERS (OTG GLOBAL REGISTERS)

These registers are available in both Host and Device modes, and not required to be reprogrammed to switch between these modes.

5.8.3.1 OTG Control and Status Register (GOTGCTL, R/W, Address = 0xEC00_0000)

The OTG Control and Status register controls the behavior and reflects the status of the core's OTG function.

GOTGCTL	Bit	Description	R/W	Initial State
Reserved	[31:20]	-	-	12'h0
BSesVld	[19]	B-Session Valid Indicates the Device mode transceiver status. • 1'b0: B-session is not valid • 1'b1: B-session is valid	R	1'b0
ASesVld	[18]	A-Session Valid Indicates the Host mode transceiver status. • 1'b0: A-session is not valid • 1'b1: A-session is valid	R	1'b0
DbncTime	[17]	Long/ Short Debounce Time Indicates the Debounce time of a detected connection. • 1'b0: Long Debounce time, used for physical connections • 1'b1: Short Debounce time, used for soft connections	R	1'b0
ConIDSts	[16]	Connector ID Status Indicates the connector ID status. • 1'b0: The OTG core is in A-device mode • 1'b1: The OTG core is in B-device mode	R	1'b1
Reserved	[15:12]	-	-	4'h0
DevHNPEn	[11]	Device HNP Enable The application sets the bit if it successfully receives a SetFeature. • 1'b0: HNP is not enabled in the application • 1'b1: HNP is enabled in the application	R/W	1'b0
HstSet HNPEn	[10]	Host Set HNP Enable The application sets this bit if it has successfully enabled HNP on the connected device. • 1'b0: Host Set HNP is not enabled • 1'b1: Host Set HNP is enabled	R/W	1'b0
HNPReq	[9]	HNP Request The application sets this bit to initiate an HNP request to the connected USB host. The core clears this bit if the HstNegSucStsChng bit is cleared. • 1'b0: No HNP request • 1'b1: HNP request	R/W	1'b0

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GOTGCTL	Bit	Description	R/W	Initial State
HstNegScs	[8]	Host Negotiation Success The core sets this bit if host negotiation is successful. The core clears this bit if the HNP Request (HNPReq) bit in this register is set. • 1'b0: Host negotiation failure • 1'b1: Host negotiation success	R	1'b0
Reserved	[7:2]	-	-	6'h0
SesReq	[1]	Session Request The application sets this bit to initiate a session request on the USB. The core clears this bit if the HstNegSucStsChng bit is cleared. • 1'b0: No session request • 1'b1: Session request	R/W	1'b0
SesReqScs	[0]	Session Request Success The core sets this bit if a session request initiation is successful. • 1'b0: Session request failure • 1'b1: Session request success	R	1'b0

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5.8.3.2 OTG Interrupt Register (GOTGINT, R/W, Address = 0xEC00_0004)

The application reads this register at the time of OTG interrupt. To clear the OTG interrupt, application clears the bits in this register.

GOTGINT	Bit	Description	R/W	Initial State
Reserved	[31:20]	-	-	12'h0
DbnceDone	[19]	Debounce Done The core sets this bit if the debounce is complete after the device connects. This bit is valid if the HNP Capable or SRP Capable bit is set in the Core USB Configuration register.	R_SS_WC	1'b0
ADev TOUTChg	[18]	A-Device Timeout Change The core sets this bit to indicate that the A-device has timed out while waiting for the B-device to connect.	R_SS_WC	1'b0
HstNegDet	[17]	Host Negotiation Detected. The core sets this bit if it detects a host negotiation request on the USB.	R_SS_WC	1'b0
Reserved	[16:10]	-	-	7'h0
HstnegSuc StsChng	[9]	Host Negotiation Success Status Change The core sets this bit on the success or failure of a USB host negotiation request.	R_SS_WC	1'b0
SesReq SucStsChng	[8]	Session Request Success Status Change The core sets this bit on the success or failure of a session request.	R_SS_WC	1'b0
Reserved	[7:3]	-	-	5'h0
SesEndDet	[2]	Session End Detected The core sets this bit if the b_valid signal is deasserted.	R_SS_WC	1'b0
Reserved	[1:0]	-	-	2'h0

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5.8.3.3 OTG AHB Configuration Register (GAHBCFG, R/W, Address = 0xEC00_0008)

This register configures the core after power-on or a change in mode of operation. This register mainly contains AHB system-related configuration parameters. Do not change this register after the initial programming. The application must program this register before starting any transactions on either the AHB or the USB.

GAHBCFG	Bit	Description	R/W	Initial State
Reserved	[31:9]	-	-	23'h0
PTxFEmpLvl	[8]	Periodic TxFIFO Empty Level Indicates if the Periodic TxFIFO Empty Interrupt bit in the Core Interrupt registers (GINTSTS.PTxFEmp) is triggered. This bit is used only in Slave mode. • 1'b0: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is half empty • 1'b1: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is completely empty	R/W	1'b0
NPTxFEmp Lvl	[7]	Non-Periodic TxFIFO Empty Level This bit is used only in Slave mode. This bit indicates when IN endpoint Transmit FIFO empty interrupt (DIEPINTn.TxFEmp)is triggered. • 1'b0: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is half empty • 1'b1: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is completely empty	R/W	1'b0
Reserved	[6]	-	-	1'b0
DMAEn	[5]	DMA Enable • 1'b0: Core operates in Slave mode • 1'b1: Core operates in a DMA mode	R/W	1'b0
HBstLen	[4:1]	Burst Length/vType Internal DMA Mode – AHB Master burst type: • 4'b0000: Single • 4'b0001: INCR • 4'b0011: INCR4 • 4'b0101: INCR8 • 4'b0111: INCR16 • Others: Reserved	R/W	4'b0
GlblIntrMsk	[0]	Global Interrupt Mask The application uses this bit to mask or unmask the interrupt line assertion. Irrespective of this bit's setting, the interrupt status registers are updated by the core • 1'b0: Mask the interrupt assertion to the application • 1'b1: Unmask the interrupt assertion to the application	R/W	1'b0

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5.8.3.4 OTG USB Configuration Register (GUSBCFG, R/W, Address = 0xEC00_000C)

This register configures the core after power-on or a changing to Host mode or Device mode. It contains USB and USB-PHY related configuration parameters. The application must program this register before starting any transactions on either the AHB or the USB. Do not make changes to this register after the initial programming.

GUSBCFG	Bit	Description	R/W	Initial State
Reserved	[31]	-	-	1'h0
ForceDevMode	[30]	Force Device Mode Writing a 1 to this bit forces the core to device mode irrespective of utmiotg_iddig input pin. • 1'b0: Normal Mode • 1'b1: Force Device Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect.	R/W	1'b0
ForceHstMode	[29]	Force Host Mode Writing a 1 to this bit forces the core to host mode irrespective of utmiotg_iddig input pin. • 1'b0: Normal Mode • 1'b1: Force Host Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect..	R/W	1'b0
Reserved	[28:14]	-	-	15'h0
USBTrdTim	[13:10]	USB Turnaround Time Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). This must be programmed to • 4'h5: When the MAC interface is 16-bit UTMI+. • 4'h9: When the MAC interface is 8-bit UTMI+. Note: The values above are calculated for the minimum AHB frequency of 30 MHz. USB turnaround time is critical for certification where long cables and 5-Hubs are used, so if you need the AHB to run at less than 30 MHz, and if USB turnaround time is not critical, these bits can be programmed to a larger value.	R/W	4'h5
HNPCap	[9]	HNP - Capable The application uses this bit to control the OTG controller HNP capabilities. • 1'b0: HNP capability is not enabled • 1'b1: HNP capability is enabled	R/W	1'b0
SRPCap	[8]	SRP - Capable The application uses this bit to control the OTG core's SRP capabilities. • 1'b0: SRP capability is not enabled • 1'b1: SRP capability is enabled	R/W	1'b0
Reserved	[7:4]	-	-	4'h0

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GUSBCFG	Bit	Description	R/W	Initial State
PHYIf	[3]	PHY Interface The application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. Only 16-bit interface is supported. This bit must be set to 1. • 1'b0: 8 bits • 1'b1: 16 bits	R/W	1'b1
TOutCal	[2:0]	HS/ FS Timeout Calibration Set this bit to 3'h7.	R/W	3'h0

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5.8.3.5 Core Reset Register (GRSTCTL, R/W, Address = 0xEC00_0010)

The application uses this register to reset various hardware features inside the core.

GRSTCTL	Bit	Description	R/W	Initial State
AHBIdle	[31]	AHB Master Idle Indicates that the AHB Master State Machine is in the IDLE condition.	R	1'b1
DMAReq	[30]	DMA Request Signal Indicates that the DMA request is in progress. Used for debug.	R	1'b0
Reserved	[29:11]	-	-	19'h0
TxFNum	[10:6]	TxFIFO Number This is the FIFO number. Use TxFIFO Flush bit to flush FIFO number. This field must not be changed until the core clears the TxFIFO Flush bit. • 5'h0: Non-periodic TxFIFO flush in Host mode. Tx FIFO 0 flush in device mode. • 5'h1: Periodic TxFIFO flush in Host mode. TXFIFO 1 flush in device. • 5'h2: TXFIFO 2 flush in device mode … • 5'hF: Periodic TxFIFO 15 flush in Device mode • 5'h10: Flush all the transmit FIFOs in device or host mode	R/W	5'h0
TxFFlsh	[5]	TxFIFO Flush This bit selectively flushes a single or all transmit FIFOs, but cannot flush if the core is in the middle of a transaction. The application must only write this bit after checking that the core is neither writing to the TxFIFO nor reading from the TxFIFO. The application must wait until the core clears this bit before performing any operations. This bit takes 8 clocks to clear.	R_WS_SC	1'b0
RxFFlsh	[4]	RxFIFO Flush The application flushes the entire RxFIFO using this bit, but must first ensure that the core is not in the middle of a transaction. The application must only write to this bit after checking that the core is neither reading from the RxFIFO nor writing to the RxFIFO. The application must wait until the bit is cleared before performing any other operations. This bit takes 8 clocks to clear.	R_WS_SC	1'b0
INTknQFlsh	[3]	IN Token Sequence Learning Queue Flush The application writes this bit to flush the IN Token Sequence Learning Queue.	R_WS_SC	1'b0
FrmCntrRst	[2]	Host Frame Counter Reset The application writes this bit to reset the (micro) frame number counter inside the core. If the (micro) frame counter is reset, the subsequent SOF sent out by the core will have a (micro) frame number of 0.	R_WS_SC	1'b0

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GRSTCTL	Bit	Description	R/W	Initial State
HSftRst	[1]	HClk Soft Reset The application uses this bit to flush the control logic in the AHB Clock domain. Only AHB Clock Domain pipelines are reset. • FIFOs are not flushed with this bit. • All state machines in the AHB clock domain are reset to the Idle state after terminating the transactions on the AHB, following the protocol. • CSR control bits used by the AHB clock domain state machines are cleared. • To clear this interrupt, status mask bits that control the interrupt status and are generated by the AHB clock domain state machine are cleared. • Because interrupt status bits are not cleared, the application can get the status of any core events that occurred after it set this bit. This is a self-clearing bit that the core clears after all necessary logic is reset in the core. This can take several clocks, depending on the core's current state	R_WS_SC	1'b0
CSftRst	[0]	Core Soft Reset Resets the hclk and phy_clock domains as follows: • Clears the interrupts and all the CSR registers except the following register bits: - HCFG.FSLSPclkSel - DCFG.DevSpd • All module state machines (except the AHB Slave Unit) are reset to the IDLE state, and all the transmit FIFOs and the receive FIFO are flushed. • Any transactions on the AHB Master are terminated as soon as possible, after gracefully completing the last data phase of an AHB transfer. Any transactions on the USB are terminated immediately. The application can write to this bit any time it wants to reset the core. This is a self-clearing bit and the core clears this bit after all the necessary logic is reset in the core, which may take several clocks, depending on the current state of the core. Once this bit is cleared software must wait at least 3 PHY clocks before accessing the PHY domain. Software must also check that bit 31 of this register is 1 (AHB Master is IDLE) before starting any operation. Typically software reset is used during software development and if you dynamically change the PHY selection bits in the USB configuration registers listed above. If you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain has to be reset for proper operation.	R_WS_SC	1'b0

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5.8.3.6 Core Interrupt Register (GINTSTS, R/W, Address = 0xEC00_0014)

This register interrupts the application for system-level events in the current mode of operation (Device mode or Host mode).

GINTSTS	Bit	Description	R/W	Initial State
WkUpInt	[31]	Resume/ Remote Wakeup Detected Interrupt In Device mode, this interrupt is asserted if a resume is detected on the USB. In Host mode, this interrupt is asserted if a remote wakeup is detected on the USB.	R_SS_WC	1'b0
SessReqInt	[30]	Session Request/ New Session Detected Interrupt In Host mode, this interrupt is asserted if a session request is detected from the device. In Device mode, this interrupt is asserted if the b_valid signal goes high.	R_SS_WC	1'b0
DisconnInt	[29]	Disconnect Detected Interrupt Asserted when a device disconnect is detected.	R_SS_WC	1'b0
ConIDSts Chng	[28]	Connector ID Status Change The core sets this bit if there is a change in connector ID status.	R_SS_WC	1'b0
LPM_Int	[27]	LPM Transaction Received Interrupt The core asserts this interrupt the device receives an LPM transaction with a non-ERRORed response. The interrupt is asserted in Host mode when the device responds to an LPM token with a non-ERRORed response. or when the host core has completed LPM transactions for the programmed number of times (GLPMCFG.RetryCnt). This field is valid only if OTG_ENABLE_LPM is set to 1 and the Global Core LPM Configuration register's LPM-Capable (LPMCap) field is set to 1.	R_SS_WC	1'b0
PTxFEmp	[26]	Periodic TxFIFO Empty Asserted if the Periodic Transmit FIFO is either half or completely empty and there is space for at least one entry to be written in the Periodic Request Queue. The half or completely empty status is determined by the Periodic TxFIFO Empty Level bit in the Core AHB Configuration register.(GAHBCFG.PTFEmpLvl)	R	1'b1
HChInt	[25]	Host Channels Interrupt The core sets this bit to indicate that an interrupt is pending on one of the channels of the core (in Host mode). The application must read the Host All Channels Interrupt (HAINT) register to determine the exact number of the channel on which the interrupt occurred, and then read the corresponding Host Channel-n Interrupt (HCINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the HCINTn register to clear this bit.	R	1'b0
PrtInt	[24]	Host Port Interrupt The core sets this bit to indicate a change in port status of one of the OTG core ports in Host mode. The application must read the Host Port Control and Status (HPRT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the Host Port Control and Status register to clear this bit.	R	1'b0

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GINTSTS	Bit	Description	R/W	Initial State
Reserved	[23]	-	-	1'b0
FetSusp	[22]	Data Fetch Suspended. This interrupt is valid only in DMA mode. This interrupt indicates that the core has stopped fetching data for IN endpoints due to the unavailability of TxFIFO space or Request Queue space. This interrupt is used by the application for an endpoint mismatch algorithm For example, after detecting an endpoint mismatch, the application: • Sets a global non-periodic IN NAK handshake • Disables In endpoints • Flushes the FIFO • Determines the token sequence from the IN Token Sequence Learning Queue • Re-enables the endpoints • Clears the global non-periodic IN NAK handshake If the global non-periodic IN NAK is cleared, the core has not yet fetched data for the IN endpoint, and the IN token received: the core generates an “IN token received when FIFO empty” interrupt. The OTG then sends the host a NAK response. To avoid this scenario, the application checks the GINSTS. FetSusp interrupt, which ensures that the FIFO is full before clearing a global NAK handshake. Alternatively, the application masks the “IN token received when FIFO empty” interrupt if clearing a global IN NAK handshake.	R_SS_WC	1'b0
incompIP	[21]	Incomplete Periodic Transfer. In Host mode, the core sets this interrupt bit if there are incomplete periodic transactions still pending which are scheduled for the current microframe.	R_SS_WC	1'b0
incompl SOOUT		Incomplete Isochronous OUT Transfer. The Device mode, the core sets this interrupt to indicate that there is at least one isochronous OUT endpoint on which the transfer is not complete in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register.	-	-
Incompl SOIN	[20]	Incomplete Isochronous IN Transfer (incompISOIN) The core sets this interrupt to indicate that there is at least one isochronous IN endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register. Note: This interrupt is not asserted in Scatter/Gather DMA mode.	R_SS_WC	1'b0

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GINTSTS	Bit	Description	R/W	Initial State
OEPInt	[19]	OUT Endpoints Interrupt (OEPInt) The core sets this bit to indicate that an interrupt is pending on one of the OUT endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the OUT endpoint on which the interrupt occurred, and then read the corresponding Device OUT Endpoint-n Interrupt (DOEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DOEPINTn register to clear this bit.	R	1'b0
IEPInt	[18]	IN Endpoints Interrupt (IEPInt) The core sets this bit to indicate that an interrupt is pending on one of the IN endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the IN endpoint on which the interrupt occurred, and then read the corresponding Device IN Endpoint-n Interrupt (DIEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DIEPINTn register to clear this bit.	R	1'b0
Reserved	[17:16]	-	-	2'b0
EOPF	[15]	End of Periodic Frame Interrupt Indicates that the period specified in the Periodic Frame Interval field of the Device Configuration register (DCFG.PerFrInt) has been reached in the current microframe.	R_SS_WC	1'b0
ISOutDrop	[14]	Isochronous OUT Packet Dropped Interrupt The core sets this bit if it fails to write an isochronous OUT packet into the RxFIFO because the RxFIFO does not have enough space to accommodate a maximum packet size packet for the isochronous OUT endpoint.	R_SS_WC	1'b0
EnumDone	[13]	Enumeration Done The core sets this bit to indicate that speed enumeration is complete. The application must read the Device Status (DSTS) register to obtain the enumerated speed.	R_SS_WC	1'b0
USBRst	[12]	USB Reset The core sets this bit to indicate that a reset is detected on the USB.	R_SS_WC	1'b0
USBSusp	[11]	USB Suspend The core sets this bit to indicate that a suspend state was detected on the USB. The core enters the Suspended state if there is no activity on the line_state signal for an extended period of time.	R_SS_WC	1'b0
ErlySusp	[10]	Early Suspend The core sets this bit to indicate that an Idle state has been detected on the USB for 3 ms.	R_SS_WC	1'b0
Reserved	[9:8]	-	-	2'b0

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GINTSTS	Bit	Description	R/W	Initial State
GOUTNak Eff	[7]	Global OUT NAK Effective Indicates that the Set Global OUT NAK bit in the Device Control register (DCTL.SGOUTNak), set by the application, has taken effect in the core. This bit can be cleared by writing the Clear Global OUT NAK bit in the Device Control register (DCTL.CGOUTNak).	R	1'b0
GINNakEff	[6]	Global IN Non-periodic NAK Effective Indicates that the Set Global Non-periodic IN NAK bit in the Device Control register (DCTL.SGNPInNak), set by the application, has taken effect in the core. That is, the core has sampled the Global IN NAK bit set by the application. This bit can be cleared by clearing the Clear Global Non-periodic IN NAK bit in the Device Control register (DCTL.CGNPInNak). This interrupt does not necessarily mean that a NAK handshake is sent out on the USB. The STALL bit takes precedence over the NAK bit.	R	1'b0
NPTxFEmp	[5]	Non-periodic TxFIFO Empty This interrupt is valid only when OTG_EN_DED_TX_FIFO = 0. This interrupt is asserted when the Non-periodic TxFIFO is either half or completely empty, and there is space for at least one entry to be written to the Non-periodic Transmit Request Queue. The half or completely empty status is determined by the Non-periodic TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl).	R	1'b1
RxFLvl	[4]	RxFIFO Non-Empty Indicates that there is at least one packet pending to be read from the RxFIFO.	R	1'b0
Sof	[3]	Start of (micro) Frame In Host mode, the core sets this bit to indicate that an SOF (FS), micro-SOF (HS), or Keep-Alive (LS) is transmitted on the USB. The application must write a 1 to this bit to clear the interrupt. In Device mode, in the core sets this bit to indicate that an SOF token has been received on the USB. The application can read the Device Status register to get the current (micro) frame number. This interrupt is seen only when the core is operating at either HS or FS.	R_SS_WC	1'b0
OTGInt	[2]	OTG Interrupt The core sets this bit to indicate an OTG protocol event. The application must read the OTG Interrupt Status (GOTGINT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the GOTGINT register to clear this bit.	R	1'b0
ModeMis	[1]	Mode Mismatch Interrupt The core sets this bit if the application is trying to access: • A Host mode register, if the core is operating in Device mode • A Device mode register, if the core is operating in Host mode	R_SS_WC	1'b0

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GINTSTS	Bit	Description	R/W	Initial State
CurMod	[0]	Current Mode Of Operation Indicates the current mode of operation. • 1'b0: Device mode • 1'b1: Host mode	R	1'b0

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5.8.3.7 Core Interrupt Mask Register (GINTMSK, R/W, Address = 0xEC00_0018)

This register works with the Core Interrupt register to interrupt the application. If an interrupt bit is masked, the interrupt associated with that bit will not be generated. However, the Core Interrupt (GINTSTS) register bit corresponding to that interrupt will still be set.

- Mask interrupt: 1'b0
- Unmask interrupt: 1'b1

GINTMSK	Bit	Description	R/W	Initial State
WkUpIntMsk	[31]	Resume/ Remote Wakeup Detected Interrupt Mask	R/W	1'b0
SessReqIntMsk	[30]	Session Request/ New Session Detected Interrupt Mask	R/W	1'b0
DisconnIntMsk	[29]	Disconnect Detected Interrupt Mask	R/W	1'b0
ConIDStsChngMsk	[28]	Connector ID Status Change Mask	R/W	1'b0
LPM_IntMsk	[27]	LPM Transaction Received Interrupt Mask	R/W	1'b0
PTxFEmpMsk	[26]	Periodic TxFIFO Empty Mask	R/W	1'b0
HChIntMsk	[25]	Host Channels Interrupt Mask	R/W	1'b0
PrtIntMsk	[24]	Host Port Interrupt Mask	R/W	1'b0
Reserved	[23]	-	-	1'b0
FetSuspMsk	[22]	Data Fetch Suspended Mask	R/W	1'b0
incomplPMsk incompISOOUTMsk	[21]	Incomplete Periodic Transfer Mask	R/W	1'b0
		Incomplete Isochronous OUT Transfer Mask	-	
incompISOINMsk	[20]	Incomplete Isochronous IN Transfer Mask	R/W	1'b0
OEPIntMsk	[19]	OUT Endpoints Interrupt Mask	R/W	1'b0
INEPIntMsk	[18]	IN Endpoints Interrupt Mask	R/W	1'b0
Reserved	[17]	-	-	1'b0
Reserved	[16]	-	-	1'b0
EOPFMsk	[15]	End of Periodic Frame Interrupt Mask	R/W	1'b0
ISOOutDropMsk	[14]	Isochronous OUT Packet Dropped Interrupt Mask	R/W	1'b0
EnumDoneMsk	[13]	Enumeration Done Mask	R/W	1'b0
USBRstMsk	[12]	USB Reset Mask	R/W	1'b0
USBSuspMsk	[11]	USB Suspend Mask	R/W	1'b0
ErlySuspMsk	[10]	Early Suspend Mask	R/W	1'b0
Reserved	[9]	-	-	1'b0
Reserved	[8]	-	-	1'b0
GOUTNakEffMsk	[7]	Global OUT NAK Effective Mask	R/W	1'b0
GINNakEffMsk	[6]	Global Non-Periodic IN NAK Effective Mask	R/W	1'b0
NPTxFEmpMsk	[5]	Non-Periodic TxFIFO Empty Mask	R/W	1'b0
RxFLvlMsk	[4]	Receive FIFO Non-Empty Mask	R/W	1'b0
SofMsk	[3]	Start of (micro)Frame Mask	R/W	1'b0

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GINTMSK	Bit	Description	R/W	Initial State
OTGIntMsk	[2]	OTG Interrupt Mask	R/W	1'b0
ModeMisMsk	[1]	Mode Mismatch Interrupt Mask	R/W	1'b0
Reserved	[0]	-	-	1'b0

5.8.3.8 Receive Status Debug Read/Status Read and Pop Registers (GRXSTSR/GRXSTSP)

A read to the Receive Status Debug Read register returns the contents of the top of the Receive FIFO. A read to the Receive Status Read and Pop register additionally pops the top data entry out of the RxFIFO.

The receive status contents must be interpreted differently in Host and Device modes. The core ignores the receive status pop/ read if the receive FIFO is empty and returns a value of 32'h0000_0000. The application must only pop the Receive Status FIFO if the Receive FIFO Non-Empty bit of the Core Interrupt register (GINTSTS.RxFLvl) is asserted.

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5.8.3.9 Host Mode Receive Status Debug Read/Status Read and Pop Registers (GRXSTSR/GRXSTSP, R, Address = 0xEC00_001C, 0xEC00_0020)

GRXSTSR/ GRXSTSP	Bit	Description	R/W	Initial State
Reserved	[31:21]	-	-	-
PktSts	[20:17]	Packet Status Indicates the status of the received packet. • 4'b0010: IN data packet received • 4'b0011: IN transfer completed (triggers an interrupt) • 4'b0101: Data toggle error (triggers an interrupt) • 4'b0111: Channel halted (triggers an interrupt) • others: Reserved	R	-
DPID	[16:15]	Data PID Indicates the Data PID of the received packet. • 2'b00: DATA0 • 2'b10: DATA1 • 2'b01: DATA2 • 2'b11: MDATA	R	-
BCnt	[14:4]	Byte Count Indicates the byte count of the received IN data packet.	R	-
ChNum	[3:0]	Channel number Indicates the channel number to which the current received packet belongs.	R	-

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5.8.3.10 Device Mode Receive Status Debug Read/Status Read and Pop Registers (GRXSTSR/GRXSTSP, R, Address = 0xEC00_001C, 0xEC00_0020)

GRXSTSR/ GRXSTSP	Bit	Description	R/W	Initial State
Reserved	[31:25]	-	-	7'h3F
FN	[24:21]	Frame Number This is the least significant 4 bits of the (micro) frame number in which the packet is received on the USB. This field is supported if isochronous OUT endpoints are supported.	R	4'hF
PktSts	[20:17]	Packet Status Indicates the status of the received packet. • 4'b0001: Global OUT NAK (triggers an interrupt) • 4'b0010: OUT data packet received • 4'b0011: OUT transfer completed (triggers an interrupt) • 4'b0100: SETUP transaction completed (triggers an interrupt) • 4'b0110: SETUP data packet received • others: Reserved	R	4'b1111
DPID	[16:15]	Data PID Indicates the Data PID of the received OUT data packet. • 2'b00: DATA0 • 2'b10: DATA1 • 2'b01: DATA2 • 2'b11: MDATA	R	2'b11
BCnt	[14:4]	Byte Count Indicates the byte count of the received data packet.	R	11'h3FF
EPNum	[3:0]	Endpoint number Indicates the endpoint number to which the current received packet belongs.	R	4'hF

5.8.3.11 Receive FIFO Size Register (GRXFSIZ, R/W, Address = 0xEC00_0024)

The application programs the RAM size that must be allocated to the RxFIFO.

GRXFSIZ	Bit	Description	R/W	Initial State
Reserved	[31:16]	-	-	16'h0
RxFDep	[15:0]	RxFIFO Depth This value is in terms of 32-bit words. • Minimum value is 16 • Maximum value is 7936 The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth. A new value must be written to this field. Programmed values must not exceed the power-on value set.	R/W	16'h1F00

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5.8.3.12 Non-Periodic Transmit FIFO Size Register (GNPTXFSIZ, R/W, Address = 0xEC00_0028)

The application programs the RAM size and the memory start address for the Non-Periodic TxFIFO.

GNPTXFSIZ	Bit	Description	R/W	Initial State
NPTxFDep	[31:16]	Non-Periodic TxFIFO Depth (For host mode) This value is in terms of 32-bit words. • Minimum value is 16 • Maximum value is 7936 The power-on reset value of this register is specified as the Largest Non-Periodic Tx Data FIFO Depth (7936). A new value must be written to this field. Programmed values must not exceed the power-on value set.	R/W	16'h1F00
INEPTxF0Dep		IN Endpoint TxFIFO 0 Depth (For Device mode) This value is in terms of 32-bit words. • Minimum value is 16 • Maximum value is 7936		
NPTxFStAddr	[15:0]	Non-Periodic Transmit Start Address (For host mode) This field contains the memory start address for Non-Periodic Transmit FIFO RAM. The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth (7936). A new value must be written to this field. Programmed values must not exceed the power-on value set.	R/W	16'h1F00
INEPTxF0StAddr		IN Endpoint FIFO0 Transmit RAM Start Address (For Device mode) This field contains the memory start address for IN Endpoint Transmit FIFO# 0		

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5.8.3.13 Non-Periodic Transmit FIFO/Queue Status Register (GNPTXSTS, R, Address = 0xEC00_002C)

This read-only register contains the free space information for the Non-Periodic TxFIFO and the Non-Periodic Transmit Request Queue.

GNPTXSTS	Bit	Description	R/W	Initial State
Reserved	[31]	-	-	1'b0
NPTxQTop	[30:24]	Top of the Non-Periodic Transmit Request Queue. Entry in the Non-Periodic Tx Request Queue that is currently being processed by the MAC. • Bits[30:27]: Channel/ endpoint number • Bits[26:25]: • 2'b00: IN/ OUT token • 2'b01: Zero-length transmit packet (device IN/host OUT) • 2'b10: PING/CSPLIT token • 2'b11: Channel halt command • Bit[24]: Terminate (last entry for selected channel/ endpoint)	R	7'h0
NPTxQSpcAvail	[23:16]	Non-Periodic Transmit Request Queue Space Available. Indicates the amount of free space available in the Non-Periodic Transmit Request Queue. This queue holds both IN and OUT requests in Host mode. Device mode has only IN requests. • 8'h0: Non-Periodic Transmit Request Queue is full • 8'h1: 1 location available • 8'h2: 2 locations available • n: n locations available(0≤n≤8) • Others: Reserved	R	8'h08
NPTxFSpcAvail	[15:0]	Non-Periodic TxFIFO Space Available Indicates the amount of free space available in the Non-Periodic TxFIFO. Values are in terms of 32-bit words. • 16'h0: Non-Periodic TxFIFO is full • 16'h1: 1 word available • 16'h2: 2 words available • 16'hn: n words available (where 0 ≤ n ≤ 32768) • 16'h8000: 32768 words available • Others: Reserved	R	16'h1F00

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5.8.3.14 Core LPM Configuration Register (GLPMCFG, R/W, Address = 0xEC00_0054)

This register controls the operation of the core's LPM and HSIC capabilities. It also contains status bits pertaining to these features.

GLPMCFG	Bit	Description	R/W	Initial State
Reserved	[31:28]	-	-	4'b0
LPM_RetryCnt_Sts	[27:25]	Number of LPM host retries remaining to be transmitted for the current LPM sequence.	R	3'b0
SndLPM	[24]	When the application software sets this bit, an LPM transaction containing two tokens, EXT and LPM, is sent. The hardware clears this bit once a valid response (STALL, NYET, or ACK) is received from the device or the core has finished transmitting the programmed number of LPM retries. Note: This bit must only be set when the host is connected to a local port.	R_WS_SC	1'b0
LPM_Retry_Cnt	[23:21]	When the device gives an ERROR response, this is the number of additional LPM retries that the host performs until a valid device response (STALL, NYET, or ACK) is received.	R/W	3'b0
LPM_Chnl_Indx	[20:17]	The channel number on which the LPM transaction must be applied while sending an LPM transaction to the local device. Based on the LPM channel index, the core automatically inserts the device address and endpoint number programmed in the corresponding channel into the LPM transaction.	R/W	4'b0
L1ResumeOK	[16]	Indicates that the application or host can start a resume from the Sleep state. This bit is valid in the LPM Sleep (L1) state. It is set in Sleep mode after a delay of 50 µs (TL1Residency). The bit is reset when SlpSts is 0 • 1'b1: The application/core can start resume from the Sleep state • 1'b0: The application/core cannot start resume from the Sleep state	R	1'b0
SlpSts	[15]	Host Mode: The host transitions to the Sleep (L1) state as a side-effect of a successful LPM transaction by the core to the local port with an ACK response from the device. The read value of this bit reflects the port's current sleep status. The core clears this bit after: • The core detects a remote L1 Wakeup signal; • The application sets the Port Reset bit or the Port L1Resume bit in the HPRT register; or • The application sets the L1Resume/ Remote Wakeup Detected Interrupt bit or Disconnect Detected Interrupt bit in the Core Interrupt register (GINTSTS.L1WkUpInt or GINTSTS.DisconnInt, respectively).	R	1'b0
		Device Mode: This bit is set as long as a Sleep condition is present on the USB bus. The core enters the Sleep state when an ACK response is sent to an LPM transaction and the timer TL1TokenRetry. has expired. To stop the PHY		

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GLPMCFG	Bit	Description	R/W	Initial State
		clock, the application must set the Port Clock Stop bit, which asserts the PHY's Suspend input pin. The application must rely on SlpSts and not ACK in CoreL1Res to confirm transition into sleep. The core comes out of sleep: • When there is any activity on the USB line_state • When the application writes to the Remote Wakeup Signaling bit in the Device Control register (DCTL.RmtWkUpSig) or when the application resets or soft-disconnects the device.		
CoreL1Res	[14:13]	Host Mode: The handshake response received from the local device for LPM transaction • 11: ACK • 10: NYET • 01: STALL • 00: ERROR (No handshake response) Device Mode: The core's response to the received LPM transaction is reflected in these two bits.	R	2'b0
HIRD_Thres	[12:8]	Host Mode: The core asserts L1SuspendM to put the PHY into Deep Low-Power mode in L1 when HIRD_Thres[4] is set to 1'b1. HIRD_Thres[3:0] specifies the time for which resume signaling is to be reflected by the host (TL1HubDrvResume2) on the USB when it detects device-initiated resume. HIRD_Thres must not be programmed with a value greater than 4'b1100 in Host mode, because this exceeds maximum TL1HubDrvResume2. Host mode resume Sl. No HIRD_Thres[3:0] signaling time (µ s) 1 4'b0000 60 2 4'b0001 135 3 4'b0010 210 4 4'b0011 285 5 4'b0100 360 6 4'b0101 435 7 4'b0110 510 8 4'b0111 585 9 4'b1000 660 10 4'b1001 735 11 4'b1010 810 12 4'b1011 885 13 4'b1100 960 14 4'b1101 invalid 15 4'b1110 invalid 16 4'b1111 invalid	R/W	5'b0

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GLPMCFG	Bit	Description	R/W	Initial State
EnblSlpM	[7]	For UTMI+ interface: The application uses this bit to control utmi_sleep_n assertion to the PHY in the L1 state. For the host, this bit is valid only in Local Device mode. • 1'b0: utmi_sleep_n assertion from the core is not transferred to the external PHY. • 1'b1: utmi_sleep_n assertion from the core is transferred to the external PHY when utmi_l1_suspend_n cannot be asserted.	R/W	1'b0
bRemoteWake	[6]	Host Mode: The remote wakeup value to be sent in the LPM transaction's wIndex field.	R/W	1'b0
		Device Mode: This field is updated with the received bRemoteWake LPM token's bmAttribute when an ACK/NYET/STALL response is sent to an LPM transaction.	R	1'b0
HIRD	[5:2]	Host Mode: The value of HIRD to be sent in an LPM transaction. This value is also used to initiate resume for a duration TL1HubDrvResume1 for host initiated resume	R/W	4'b0
AppL1Res	[1]	Handshake response to LPM token pre-programmed by device application software. The response depends on GLPMCFG.LPMCap. If GLPMCFG.LPMCap is 1'b0, the core always responds with a NYET. If GLPMCFG.LPMCap is 1'b1, the core responds as follows: • 1: ACK Even though an ACK is pre-programmed, the core responds with an ACK only on a successful LPM transaction. The LPM transaction is successful if: - There are no PID/CRC5 errors in both the EXT token and the LPM token (else ERROR) - A valid bLinkState = 0001B (L1) is received in the LPM transaction (else STALL) - No data is pending in the Transmit queue (else NYET) • 0: NYET The pre-programmed software bit is overridden for response to LPM token when: - The received bLinkState is not L1 (STALL response) - An error is detected in either of the LPM token packets due to corruption (ERROR response).	R	1'b0
LPMCap	[0]	LPM-Capable (LPMCap) The application uses this bit to control the DWC_otg core LPM capabilities. If the core operates as a non-LPM-capable host, it cannot request the connected device/hub to activate LPM mode. If the core operates as a non-LPM-capable device, it cannot respond to any LPM transactions. • 1'b0: LPM capability is not enabled. • 1'b1: LPM capability is enabled. Otherwise, reads return 0.	R/W	1'b0

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5.8.3.15 Host Periodic Transmit FIFO Size Register (HPTXFSIZ, R/W, Address = 0xEC00_0100)

This register holds the size and the memory start address of the Periodic TxFIFO.

HPTXFSIZ	Bit	Description	R/W	Initial State
PTxFSize	[31:16]	Host Periodic TxFIFO Depth This value is in terms of 32-bit words • Minimum value is 16 • Maximum value is 7936 A new value must be written to this field. Programmed values must not exceed the Maximum value.	R/W	16'h0300
PTxFStAddr	[15:0]	Host Periodic TxFIFO Start Address. The power-on reset value of this register is the sum of the Largest Rx Data FIFO Depth and Largest Non-periodic Tx Data FIFO Depth If you have programmed new values for the RxFIFO or Non-Periodic TxFIFO, write their sum in this field. Programmed values must not exceed the power-on value.	R/W	16'h5A00

5.8.3.16 Device IN Endpoint Transmit FIFO-n Size Register (DIEPTXFn, R/W, Address = 0xEC00_0104 + (n-1)*04h)

FIFO_number: $1 \leq n \leq 15$

This register holds the memory start address of IN endpoint TxFIFOs to implement in Device mode. Each FIFO holds the data for one IN endpoint FIFOs. This register is repeated for IN endpoint FIFO instantiated.

DIEPTXFn	Bit	Description	R/W	Initial State
INEPnTxFDep	[31:16]	IN Endpoint TxFIFO Depth (INEPnTxFDep) This value is in terms of 32-bit words • Minimum value is 4 • Maximum value is 768 The Power-on reset value of this registeris specified as the Largest IN Endpoint FIFO number Depth. It can be write a new value in this field.	R/W	User selected
INEPnTxFStAddr	[15:0]	IN Endpoint FIFOn Transmit RAM Start Address This field contains the memory start address for IN endpoint Transmit FIFOn. The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth. You have programmed a new value for RxFIFO depth, you can write that value in this field. Programmed values must not exceed the power-on value.	R/W	User selected

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5.8.4 HOST MODE REGISTERS (HOST GLOBAL REGISTERS)

These registers affect the operation of the core in the Host mode. Host mode registers must not be accessed in Device mode, as the results are undefined. Host Mode registers are categorized as follows:

- Host Global registers
- Host Port Control and Status registers
- Host Channel-Specific registers

5.8.4.1 Host Configuration Register (HCFG, R/W, Address = 0xEC00_0400)

This register configures the core after power-on. Do not make changes to this register after initializing the host.

HCFG	Bit	Description	R/W	Initial State
Reserved	[31:3]	-	-	29'h0040000
FSLSSupp	[2]	FS- and LS- Only Support The application uses this bit to control the core's enumeration speed. Using this bit, the application makes the core enumerate as a FS host, even if the connected device supports HS traffic. Do not make changes to this field after initial programming. • 1'b0: HS/FS/LS, based on the maximum speed supported by the connected device • 1'b1: FS/LS -only, even if the connected device can support HS	R/W	1'b0
FSLSPclkSel	[1:0]	FS/ LS PHY Clock Select If the core is in FS Host mode • 2'b00: PHY clock is 30/60 MHz • 2'b01: PHY clock is 48 MHz • Others: Reserved If the core is in LS Host mode • 2'b00: PHY clock is 30/60 MHz • 2'b01: PHY clock is 48 MHz • 2'b10: PHY clock is 6 MHz • 2'b11: Reserved	R/W	2'b0

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5.8.4.2 Host Frame Interval Register (HFIR, R/W, Address = 0xEC00_0404)

This register stores the frame interval information for the current speed to which the core has enumerated

HFNUM	Bit	Description	R/W	Initial State
Reserved	[31:16]	-	-	16'h0
FrInt	[15:0]	Frame Interval The value that the application programs to this field specifies the interval between two consecutive SOFs (FS) or micro- SOFs (HS) or Keep-Alive tokens (HS). This field contains the number of PHY clocks that constitute the required frame interval. The default value set in this field for a FS operation if the PHY clock frequency is 60 MHz. The application can write a value to this register only after the Port Enable bit of the Host Port Control and Status register (HPRT.PrtEnaPort) has been set. If no value is programmed, the core calculates the value based on the PHY clock specified in the FS/ LS PHY Clock Select field of the Host Configuration register (HCFG.FSLSPclkSel). Do not change the value of this field after the initial configuration. • 125 µs * (PHY clock frequency for HS) • 1 ms * (PHY clock frequency for FS/LS)	R/W	16'h0B8F

5.8.4.3 Host Frame Number/Frame Time Remaining Register (HFNUM, R, Address = 0xEC00_0408)

This register indicates the current frame number. It also indicates the time remaining in the current frame.

HFNUM	Bit	Description	R/W	Initial State
FrRem	[31:16]	Frame Time Remaining Indicates the amount of time remaining in the current microframe (HS) or frame (FS/ LS), in terms of PHY clocks. This field decrements on each PHY clock. If it reaches zero, this field is reloaded with the value in the Frame Interval register and a new SOF is transmitted on the USB.	R	16'h0
FrNum	[15:0]	Frame Number This field increment if a new SOF is transmitted on the USB, and is reset to 0 if it reaches 16'h3FFF.	R	16'h0

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5.8.4.4 Host Periodic Transmit FIFO/QUEUE Status Register (HPTXSTS, R, Address = 0xEC00_0410)

This read-only register contains the free space information for the Periodic TxFIFO and the Periodic Transmit Request Queue.

HPTXSTS	Bit	Description	R/W	Initial State
PTxQTop	[31:24]	Top of the Periodic Transmit Request Queue This indicates the entry in the Periodic Tx Request Queue that is currently being processes by the MAC. This register is used for debugging. • Bit [31]: Odd/Even (micro)frame - 1'b0: send in even (micro)frame - 1'b1: send in odd (micro)frame • Bits [30:27]: Channel/endpoint number • Bits [26:25]: Type -2'b00: IN/OUT -2'b01: Zero-length packet -2'b10: CSPLIT -2'b11: Disable channel command • Bit[24]: Terminate	R	8'h0
PTxQSpcAvail	[23:16]	Periodic Transmit Request Queue Space Available Indicates the number of free locations available to be written in the Periodic Transmit Request Queue. This queue holds both IN and OUT requests. • 8'h0: Periodic Transmit Request Queue is full • 8'h1: 1 location available • 8'h2: 2 location available • n: n locations available ($0 \le n \le 8$) • Others: Reserved	R	8'h8
PTxFSpcAvail	[15:0]	Periodic Transmit Data FIFO Space Available Indicates the number of free locations available to be written to in the Periodic TxFIFO. Values are in terms of 32-bit words • 16'h0: Periodic TxFIFO is full • 16'h1: 1 word available • 16'h2: 2 words available • n: n words available ($0 \le n \le 8$) • Others: Reserved	R	16'h0300

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5.8.4.5 Host All Channels Interrupt Register (HAINT, R, Address = 0xEC00_0414)

If a significant event occurs on a channel, the Host All Channels Interrupt register interrupts the application using the Host Channels Interrupt bit of the Core Interrupt register. There is one interrupt bit per channel, up to a maximum of 16 bits. Bits in this register are set and cleared if the application sets and clears bits in the corresponding Host Channel-n Interrupt register.

HAINT	Bit	Description	R/W	Initial State
Reserved	[31:16]	-	-	16'h0
HAINT	[15:0]	Channel Interrupts One bit per channel: Bit 0 for Channel 0, bit 15 for Channel 15	R	16'h0

5.8.4.6 Host All Channels Interrupt Mask Register (HAINTMSK, R/W, Address = 0xEC00_0418)

The Host All Channel Interrupt Mask register works with the Host All Channel Interrupt register to interrupt the application if an event occurs on a channel. There is one interrupt mask bit per channel, up to a maximum of 16 bits.

- Msk interrupt: 1'b0
- Unmask interrupt: 1'b0

HAINTMSK	Bit	Description	R/W	Initial State
Reserved	[31:16]	-	-	16'h0
HAINTMsk	[15:0]	Channel Interrupt Mask One bit per channel: Bit 0 for Channel 0, bit 15 for Channel 15	R/W	16'h0

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5.8.5 HOST MODE REGISTERS (**HOST PORT CONTROL AND STATUS REGISTERS)**

5.8.5.1 Host Port Control and Status Register (HPRT, R/W, Address = 0xEC00_0440)

This register is available only in Host mode. Currently, the OTG Host supports only one port. A single register holds USB port-related information such as USB reset, enable, suspend, resume, connect status, and test mode for each port. On a Port Interrupt, the application must read this register and clear the bit that caused the interrupt. For the R_SS_WC bits, the application must write a 1 to the bit to clear the interrupt

HPRT	Bit	Description	R/W	Initial State
Reserved	[31:19]	-	-	13'h0
PrtSpd	[18:17]	Port Speed Indicates the speed of the device attached to this port. • 2'b00: High speed • 2'b01: Full speed • 2'b10: Low speed • 2'b11: Reserved	R	2'b0
PrtTstCtl	[16:13]	Port Test Control The application writes a nonzero value to this field to put the port into a Test mode, and the corresponding pattern is signaled on the port. • 4'b0000: Test mode disabled • 4'b0001: Test_J mode • 4'b0010: Test_K mode • 4'b0011: Test_SE0_NAK mode • 4'b0100: Test_Packet mode • 4'b0101: Test_Force_Enable • Others: Reserved	R/W	4'h0
PrtPwr	[12]	Port Power The application uses this field to control power to this port, and the core clears this bit on an overcurrent condition. • 1'b0: Power off • 1'b1: Power on	R_W_SC	1'b0
PrtLnSts	[11:10]	Port Line Status Indicates the current logic level USB data lines • Bit [10]: Logic level of D– • Bit [11]: Logic level of D+	R	2'b0
Reserved	[9]	-	-	1'b0

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HPRT	Bit	Description	R/W	Initial State
PrtRst	[8]	Port Reset If the application sets this bit, a reset sequence is started on this port. The application must time the reset period and clear this bit after the reset sequence is complete. • 1'b0: Port not in reset • 1'b1: Port in reset The application must leave this bit set for at least a minimum duration mentioned below to start a reset on the port. The application can leave it set for another 10ms in addition to the required minimum duration, before clearing the bit, even though there is no maximum limit set by the USB standard. • High speed: 50 ms • Full speed/Low speed: 10ms	R/W	1'b0
prtSusp	[7]	Port Suspend The application sets this bit to put this port in Suspend mode. The core stops sending SOFs if this is set. To stop the PHY clock, the application must set the Port Clock Stop bit, which asserts the suspend input pin of the PHY. The read value of this bit reflects the current suspend status of the port. This bit is cleared by the core after a remote wakeup signal is detected or the application sets the Port Reset bit or Port Resume bit in this register or the Resume/Remote Wakeup Detected Interrupt bit or Disconnect Detected Interrupt bit in the Core Interrupt register. • 1'b0: Port not in Suspend mode • 1'b1: Port in Suspend mode	R_WS_SC	1'b0
PrtRes	[6]	Port Resume The application sets this bit to drive resume signaling on the port. The core continues to drive the resume signal until the application clears this bit. If the core detects a USB remote wakeup sequence, as indicated by the Port Resume/ Remote Wakeup Detected Interrupt bit of the Core Interrupt register, the core starts driving resume signaling without application intervention and clears this bit if it detects a disconnect condition. The read value of this bit indicates whether the core is currently driving resume signaling. • 1'b0: No resume driven • 1'b1: Resume driven	R_W_SS_SC	1'b0
PrtOvr CurrChng	[5]	Port Overcurrent Change The core sets this bit if the status of the Port Overcurrent Active bit (bit 4) in this register changes.	R_SS_WC	1'b0
PrtOvr CurrAct	[4]	Port Overcurrent Active Indicates the overcurrent condition of the port. • 1'b0: No overcurrent condition • 1'b1: Overcurrent condition	R	1'b0

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HPRT	Bit	Description	R/W	Initial State
PrtEnChng	[3]	Port Enable/Disable Change The core sets this bit if the status of the Port Enable bit [2] of this register changes.	R_SS_WC	1'b0
PrtEna	[2]	Port Enable A port is enabled by the core after a reset sequence, and is disabled by an overcurrent condition, a disconnect condition, or by the application clearing this bit. The application cannot set this bit by a register write. It clears it to disable the port. This bit does not trigger any interrupt to the application. • 1'b0: Port disabled • 1'b1: Port enabled	R_SS_SC_WC	1'b0
PrtConn Det	[1]	Port Connect Detected The core sets this bit if a device connection is detected to trigger an interrupt to the application using the Host Port Interrupt bit of the Core Interrupt register. The application must write a 1 to this bit to clear the interrupt.	R_SS_WC	1'b0
PrtConnSts	[0]	Port Connect Status • 1'b0: No device is attached to the port • 1'b1: A device is attached to the port	R	1'b0

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5.8.6 HOST MODE REGISTERS (HOST CHANNEL-SPECIFIC REGISTERS)

5.8.6.1 Host Channel-n Characteristics Register (HCCHARn, R/W, Address = 0xEC00_0500+n*20h)

Channel_number: 0 ≤ n ≤ 15

HCCHARn	Bit	Description	R/W	Initial State
ChEna	[31]	Channel Enable This field is set by the application and cleared by the OTG host. • 1'b0: Disables Channel • 1'b1: Enables Channel	R_WS_SC	1'b0
ChDis	[30]	Channel Disable The application sets this bit to stop transmitting/ receiving data on a channel, even before the transfer for that channel is complete. The application must wait for the Channel Disabled interrupt before treating the channel as disabled.	R_WS_SC	1'b0
OddFrm	[29]	Odd Frame This field is set (reset) by the application to indicate that the OTG host must perform a transfer in an odd (micro) frame. This field is applicable for only periodic transactions. • 1'b0: Even (micro)frame • 1'b1: Odd (micro)frame	R/W	1'b0
DevAddr	[28:22]	Device Address This field selects the specific device serving as the data source or sink.	R/W	7'h0
MC/EC	[21:20]	Multi Count/Error Count If the Split Enable bit of the Host Channel-n Split Control register is reset (1'b0), this field indicates to the host the number of transactions that must be executed per microframe for this endpoint. • 2'b00: Reserved • 2'b01: 1 transaction • 2'b10: 2 transactions to be issued for this endpoint per microframe • 2'b11: 3 transactions to be issued for this endpoint per microframe If HCSPLTn.SpltEna is set, this field indicates the number of immediate retries to be performed for a periodic split transactions on transaction errors. This field must be set to at least 2'b01.	R/W	2'b0
EPType	[19:18]	Endpoint Type Indicates the transfer type selected. • 2'b00: Control • 2'b01: Isochronous • 2'b10: Bulk • 2'b11: Interrupt	R/W	2'b0
LSpdDev	[17]	Low-Speed Device This field is set by the application to indicate that this channel is communicating to a low-speed device.	R/W	1'b0
Reserved	[16]	-	-	1'b0

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HCCHARn	Bit	Description	R/W	Initial State
EPDir	[15]	Endpoint Direction Endpoint Type Indicates the transfer type selected. • 1'b0: Out • 1'b1: In	R/W	1'b0
EPNum	[14:11]	Endpoint Number Indicates the endpoint number on the device serving as the data source or sink.	R/W	4'h0
MPS	[10:0]	Maximum Packet Size Indicates the maximum packet size of the associated endpoint.	R/W	11'h0

5.8.6.2 Host Channel-n Split Register (HCSPLTn, R/W, Address = 0xEC00_0504+n*20h)

Channel_number: $0 \leq n \leq 15$

HCSPLTn	Bit	Description	R/W	Initial State
SpltEna	[31]	Split Enable The application sets this field to indicate that this channel is enabled to perform split transactions.	R/W	1'b0
Reserved	[30:17]	-	-	14'h0
CompSplt	[16]	Do Complete Split The application sets this field to request the OTG host to perform a complete split transaction.	R/W	1'b0
XactPos	[15:14]	Transaction Position This field is used to determine whether to send all, first, middle, or last payloads with each OUT transaction. • 2'b11: All. This is the entire data payload is of this transaction. • 2'b10: Begin. This is the first data payload of this transaction. • 2'b00: Mid. This is the middle payload of this transaction. • 2'b01: End. This is the last payload of this transaction.	R/W	2'h0
HubAddr	[13:7]	Hub Address This field holds the device address of the transaction translator's hub.	R/W	7'h0
PrtAddr	[6:0]	Port Address This field is the port number of the recipient transaction translator.	R/W	7'h0

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5.8.6.3 Host Channel-n Interrupt Register (HCINTn, R/W, Address = 0xEC00_0508+n*20h)

Channel_number: 0 ≤ n ≤ 15

This register indicates the status of a channel with respect to USB- and AHB-related events. The application must read this register if the Host Channels Interrupt bit of the Core Interrupt register is set. Before the application reads this register, it must first read the Host All Channels Interrupt register to get the exact channel number for the Host Channel-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the HAINT and GINTSTS registers.

HCINTn	Bit	Description	R/W	Initial State
Reserved	[31:11]	-	-	21'h0
DataTglErr	[10]	Data Toggle Error	R_SS_WC	1'b0
FrmOvrun	[9]	Frame Overrun	R_SS_WC	1'b0
BblErr	[8]	Babble Error	R_SS_WC	1'b0
XactErr	[7]	Transaction Error	R_SS_WC	1'b0
NYET	[6]	NYET Response Received Interrupt	R_SS_WC	1'b0
ACK	[5]	ACK Response Received Interrupt	R_SS_WC	1'b0
NAK	[4]	NAK Response Received Interrupt	R_SS_WC	1'b0
STALL	[3]	STALL Response Received Interrupt	R_SS_WC	1'b0
AHBErr	[2]	AHB Error This is generated only in Internal DMA mode if there is an AHB error during AHB read/ writes. The application reads the corresponding channel's DMA address register to get the error address.	R_SS_WC	1'b0
ChHltd	[1]	Channel Halted Indicates the incomplete transfer either because of any USB transaction error or in response to disable request by the application.	R_SS_WC	1'b0
XferCompl	[0]	Transfer Completed Transfer completed normally without any errors.	R_SS_WC	1'b0

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5.8.6.4 Host Channel-n Interrupt Mask Register (HCINTMSKn, R/W, Address = 0xEC00_050C+n*20h)

Channel_number: 0 ≤ n ≤ 15

This register reflects the mask for each channel status described in the previous section.

- Mask interrupt : 1'b0
- Unmask interrupt : 1'b1

HCINTMSKn	Bit	Description	R/W	Initial State
Reserved	[31:11]	-	-	21'h0
DataTglErrMsk	[10]	Data Toggle Error Mask	R/W	1'b0
FrmOvrunMsk	[9]	Frame Overrun Mask	R/W	1'b0
BblErrMsk	[8]	Babble Error Mask	R/W	1'b0
XactErrMsk	[7]	Transaction Error Mask	R/W	1'b0
NyetMsk	[6]	NYET Response Received Interrupt Mask	R/W	1'b0
AckMsk	[5]	ACK Response Received Interrupt Mask	R/W	1'b0
NakMsk	[4]	NAK Response Received Interrupt Mask	R/W	1'b0
StallMsk	[3]	STALL Response Received Interrupt Mask	R/W	1'b0
AHBErrMsk	[2]	AHB Error Mask	R/W	1'b0
ChHltdMsk	[1]	Channel Halted Mask	R/W	1'b0
XferComplMsk	[0]	Transfer Completed Mask	R/W	1'b0

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5.8.6.5 Host Channel-n Transfer Size Register (HCTSIZn, R/W, Address = 0xEC00_0510+n*20h)

Channel_number: 0 ≤ n ≤ 15

HCTSIZn	Bit	Description	R/W	Initial State
DoPng	[31]	Do Ping Setting this field to 1 directs the host to do PING protocol.	R/W	1'h0
Pid	[30:29]	PID The application programs this field with the type of PID to use for the initial transaction. The host maintains this field for the rest of the transfer. • 2'b00: DATA0 • 2'b01: DATA1 • 2'b10: DATA2 • 2'b11: MDATA (non-control)/ SETUP(control)	R/W	2'b0
PktCnt	[28:19]	Packet Count This field is programmed by the application with the expected number of packets to be transmitted (OUT) or received (IN). The host decrements this count on every successful transmission or reception of an OUT/ IN packet. Once this count reaches zero, the application is interrupted to indicate normal completion.	R/W	10'b0
XferSize	[18:0]	Transfer Size For an OUT, this field is the number of data bytes the host sends during the transfer. For an IN, this field is the buffer size that the application has reserved for the transfer. The application is expected to program this field as an integer multiple of the maximum packet size for IN transactions.	R/W	19'b0

NOTE: Transfer Size for a Host Channel must equal [Packet Count * Max Packet Size] for accurate data transfer.

5.8.6.6 Host Channel-n DMA Address Register (HCDMAn, R/W, Address = 0xEC00_0514+n*20h)

Channel_number: 0 ≤ n ≤ 15

This register is used by the OTG host in the internal DMA mode to maintain the buffer pointer for IN/ OUT transactions.

HCDMAn	Bit	Description	R/W	Initial State
DMAAddr	[31:0]	DMA Address This field holds the start address in the external memory from which the data for the endpoint must be fetched or to which it must be stored. This register is incremented on every AHB transaction.	R/W	32'h0

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5.8.7 DEVICE MODE REGISTERS (DEVICE GLOBAL REGISTERS)

These registers are visible only in Device mode and must not be accessed in Host mode, as the results are unknown. Some of them affect all the endpoints uniformly, while others affect only a specific endpoint. Device Mode registers fall into two categories:

- Device Global registers
- Device logical endpoint-specific registers

5.8.7.1 Device Configuration Register (DCFG, R/W, Address = 0xEC00_0800)

This register configures the core after power-on or after certain control commands or enumeration. Do not make changes to this register after initial programming.

DCFG	Bit	Description	R/W	Initial State
ResValid	[31:26]	Resume Validation Period This field controls the period when the core resumes from a suspend. When this bit is set, the core counts for the ResValid number of clock cycles to detect a valid resume. This field is effective only when DCFG.Ena32KHzSusp is set	R/W	6'h2
PerSchIntvl	[25:24]	Periodic Scheduling Interval PerSchIntvl must be programmed only for Scatter/Gather DMA mode. This field specifies the amount of time the Internal DMA engine must allocate for fetching periodic IN endpoint data. Based on the number of periodic endpoints, this value must be specified as 25, 50 or 75% of (micro) frame. • When any periodic endpoints are active, the internal DMA engine allocates the specified amount of time in fetching periodic IN endpoint data • When no periodic endpoints are active, then the internal DMA engine services non-periodic endpoints, ignoring this field. • After the specified time within a (micro)frame, the DMA switches to fetching for non-periodic endpoints. • 2'b00: 25% of (micro)frame. • 2'b01: 50% of (micro)frame. • 2'b10: 75% of (micro)frame. • 2'b11: Reserved.	R/W	2’b00
DescDMA	[23]	Enable Scatter/gather DMA in device mode. This bit must be modified only once after a reset. The following combinations are available for programming: • GAHBCFG.DMAEn=0,DCFG.DescDMA=0 => Slave mode • GAHBCFG.DMAEn=0,DCFG.DescDMA=1 => Invalid • GAHBCFG.DMAEn=1,DCFG.DescDMA=0 => Buffered DMA mode • GAHBCFG.DMAEn=1,DCFG.DescDMA=1 => Scatter/Gather DMA mode	R/W	1’b0
Reserved	[22:13]	-	-	10'h100

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DCFG	Bit	Description	R/W	Initial State
PerFrInt	[12:11]	Periodic Frame Interval Indicates the time within a (micro) frame at which the application must be notified using the End Of Periodic Frame Interrupt. This can be used to determine if all the isochronous traffic for that (micro) frame is complete. • 2'b00: 80% of the (micro) frame interval • 2'b01: 85% • 2'b10: 90% • 2'b11: 95%	R/W	2'h0
DevAddr	[10:4]	Device Address The application must program this field after every SetAddress control command.	R/W	7'h0
Reserved	[3]	-	-	1'b0
NZSts OUTHShk	[2]	Non-Zero-Length Status OUT Handshake The application uses this field to select the handshake that the core sends on receiving a nonzero-length data packet during the OUT transaction of a control transfer's Status stage. • 1'b0: Sends a STALL handshake on a nonzero-length status OUT transaction and do not send the received OUT packet to the application. • 1'b1: Sends the received OUT packet to the application and send a handshake based on the NAK and STALL bits for the endpoint in the Device Endpoint Control register.	R/W	1'b0
DevSpd	[1:0]	Device Speed. Indicates the speed at which the application requires the core to enumerate, or the maximum speed the application supports. However the actual bus speed is determined only after the chirp sequence is complete, and is based on the speed of the USB host to which the core is connected. • 2'b00: High speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) • 2'b01: Full speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) • 2'b10: Low speed (USB 1.1 transceiver clock is 6 MHz). If you select 6 MHz LS mode, you must do a soft reset. • 2'b11: Full speed (USB 1.1 transceiver clock is 48 MHz).	R/W	2'b0

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5.8.7.2 Device Control Register (DCTL, R/W, Address = 0xEC00_0804)

DCTL	Bit	Description	R/W	Initial State
Reserved	[31:17]	-	-	15'h0
NakOnBable	[16]	Set NAK automatically on babble (NakOnBble). The core sets NAK automatically for the endpoint on which babble is received	R/W	1'b0
IgnrFrmNum	[15]	Ignore frame number for Isochronous end points Do NOT program IgnrFrmNum bit to 1'b1 when the core is operating in threshold mode. This feature is not applicable to High Speed, High bandwidth transfers. When this bit is enabled, there must be only one packet per descriptor. • 0: The core transmits the packets only in the frame number in which they are intended to be transmitted. • 1: The core ignores the frame number, sending packets immediately as the packets are ready. When Scatter/Gather DMA mode is disabled, this field is reserved, and reads 1'b0. • In Scatter/Gather DMA mode, if this bit is enabled, the packets are not flushed when a ISOC IN token is received for an elapsed frame.	R/W	1'b0
GMC	[14:13]	Global Multi Count. GMC must be programmed only once after initialization. Applicable only for Scatter/Gather DMA mode. This indicates the number of packets to be serviced for that end point before moving to the next end point. It is only for non-periodic end points. • 2'b00: Invalid. • 2'b01: 1 packet. • 2'b10: 2 packets. • 2'b11: 3 packets. When Scatter/Gather DMA mode is disabled, this field is reserved. And reads 2'b00.	R/W	2'b01
Reserved	[12]	-	-	-
PWROnPrgDone	[11]	Power-On Programming Done The application uses this bit to indicate that register programming is complete after a wake-up from Power Down mode.	R/W	1'b0
CGOUTNak	[10]	Clear Global OUT NAK A write to this field clears the Global OUT NAK.	W	1'b0
SGOUTNak	[9]	Set Global OUT NAK A write to this field sets the Global OUT NAK. The application uses this bit to send a NAK handshake on all OUT endpoints. The application must set this bit after making sure that the Global OUT NAK Effective bit in Core Interrupt Register is cleared.	W	1'b0

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DCTL	Bit	Description	R/W	Initial State
CGNPInNAK	[8]	Clear Global Non-Periodic IN NAK A write to this field clears the Global Non-Periodic IN NAK.	W	1'b0
SGNPInNAK	[7]	Set Global Non-Periodic IN NAK A write to this field sets the Global Non-Periodic IN NAK. The application uses this bit to send a NAK handshake on all non-periodic IN endpoints. The core sets this bit if a timeout condition is detected on a non-periodic endpoint. The application must set this bit only after making sure that the Global IN NAK Effective bit in the Core Interrupt Register is cleared.	W	1'b0
TstCtl	[6:4]	Test Control • 3'b000: Test mode disabled • 3'b001: Test_J mode • 3'b010: Test_K mode • 3'b011: Test_SE0_NAK mode • 3'b100: Test_Packet mode • 3'b101: Test_Force_Enable • Others: Reserved	R/W	3'b0
GOUTNakSts	[3]	Global OUT NAK Status • 1'b0: A handshake is sent based on the FIFO Status and the NAK and STALL bit settings. • 1'b1: No data is written to the RxFIFO, irrespective of space availability. Sends a NAK handshake on all packets, except on SETUP transactions. All isochronous OUT packets are dropped.	R	1'b0
GNPINNakSts	[2]	Global Non-Periodic IN NAK Status • 1'b0: A handshake is sent based on the data availability in the transmit FIFO. • 1'b1: A NAK handshake is sent out on all non-periodic IN endpoints, irrespective of the data availability in the transmit FIFO.	R	1'b0
SftDiscon	[1]	Soft Disconnect The application uses this bit to signal the OTG core to do a soft disconnect. As long as this bit is set, the host does not see that the device is connected, and the device will not receive signals on the USB. The core stays in the disconnected state until the application clears this bit. • 1'b0: Normal operation. If this bit is cleared after a soft disconnect, the core drives the opmode signal on the UTMI+ to 2'b00, which generates a device connect event to the USB host. If the device is reconnected, the USB host restarts device enumeration. • 1'b1: The core drives the opmode signal on the UTMI+ to 2'b01, which generates a device disconnect event to the USB host.	R/W	1'b0

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DCTL	Bit	Description	R/W	Initial State
RmtWkUpSig	[0]	Remote Wakeup Signaling If the application sets this bit, the core initiates remote signaling to wake up the USB host. The application must set this bit to instruct the core to exit the Suspend state. As specified in the USB 2.0 specification, the application must clear this bit 1-15ms after setting it.	R/W	1'b0

The following table lists the minimum duration under various conditions for which the SoftDisconnect bit must be set for the USB host to detect a device disconnect. To accommodate clock jitter, it is recommended that the application add some extra delay to the specified minimum duration.

Operating Speed	Device state	Minimum Duration
High speed	Suspended	1ms + 2.5μs
High speed	Idle	3ms + 2.. μs
High speed	Not Idle or Suspended (Performing transactions)	125μs
Full speed/ Low speed	Suspended	1ms + 2.5μs
Full speed/ Low speed	Idle	2.5μs
Full speed/ Low speed	Not Idle or Suspended (Performing transactions)	2.5μs

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5.8.7.3 Device Status Register (DSTS, R, Address = 0xEC00_0808)

This register indicates the status of the core with respect to USB-related events. It must be read on interrupts from Device ALL Interrupts (DAINT) register.

DSTS	Bit	Description	R/W	Initial State
Reserved	[31:22]	-	-	10'h0
SOFFN	[21:8]	Frame or Microframe Number of the Received SOF If the core is operating at high speed; this field contains a microframe number. If the core is operating at full or low speed, this field contains a frame number.	R	14'h0
Reserved	[7:4]	-	-	4'h0
ErrticErr	[3]	Erratic Error The core sets this bit to report any erratic errors seen on the UTMI+. Due to erratic errors, the OTG core goes into Suspended state and an interrupt is generated to the application with Early Suspend bit of the Core Interrupt register. If the early suspend is asserted due to an erratic error, the application performs a soft disconnect recover.	R	1'b0
EnumSpd	[2:1]	Enumerated Speed Indicates the speed at which the OTG core has come up after speed detection through a chirp sequence. • 2'b00: High speed (PHY clock is 30 MHz) • 2'b01: Full speed (PHY clock is 30 MHz) • 2'b10: Low speed (PHY clock is 6 MHz). • 2'b11: Full speed (PHY clock is 48 MHz). Low speed is not supported for devices using a UTMI+ PHY.	R	2'b01
SuspSts	[0]	Suspend Status In device mode, this bit is set as long as a Suspend condition is detected on the USB. The core enters the Suspended state if there is no activity on the line_state signal for an extended period of time. The core comes out of the suspend: • If there is any activity on the line_state signal • If the application writes to the Remote Wakeup Signaling bit in the Device Control register.	R	1'b0

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5.8.7.4 Device IN Endpoint Common Interrupt Mask Register (DIEPMSK, R/W, Address = 0xEC00_0810)

This register works with each of the Device IN Endpoint Interrupt registers for all endpoints to generate an interrupt per IN endpoint. The IN endpoint interrupt for a specific status in the DIEPINTn register is masked by writing to the corresponding bit in this register. Status bits are masked by default.

- Mask interrupt: 1'b0
- Unmask interrupt: 1'b1

DIEPMSK	Bit	Description	R/W	Initial State
Reserved	[31:10]	-	-	22'h0
BNAInIntrMsk	[9]	BNA interrupt Mask	R/W	1’b0
TxfifoUndrnMsk	[8]	Fifo Underrun Mask	R/W	1’b0
Reserved	[7]	-	-	1'b0
INEPNakEffMsk	[6]	IN Endpoint NAK Effective Mask	R/W	1'b0
Reserved	[5]	-	-	1'b0
INTknTXFEmpMsk	[4]	IN Token received with TxFIFO Empty mask	R/W	1'b0
TimeOUTMsk	[3]	Timeout Condition Mask	R/W	1'b0
AHBErrMsk	[2]	AHB Error Mask	R/W	1'b0
EPDisbldMsk	[1]	Endpoint Disabled Interrupt Mask	R/W	1'b0
XferComplMsk	[0]	Transfer Completed Interrupt Mask	R/W	1'b0

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5.8.7.5 Device OUT Endpoint Common Interrupt Mask Register (DOEPMSK, R/W, Address = 0xEC00_0814)

This register works with each of the Device OUT Endpoint Interrupt registers for all endpoints to generate an interrupt per OUT endpoint. The OUT endpoint interrupts for a specific status in the DOEPINTn register is masked by writing to the corresponding bit in this register. Status bits are masked by default.

- Mask interrupt: 1'b0
- Unmask interrupt: 1'b1

DOEPMSK	Bit	Description	R/W	Initial State
Reserved	[31:10]	-	-	22'h0
BnaOutIntrMsk	[9]	BNA interrupt Mask	R/W	1'b0
OutPktErrMsk	[8]	OUT Packet Error Mask	R/W	1'b0
Reserved	[7]	-	-	-
Back2BackSETup	[6]	Back-to-Back SETUP Packets Received Mask Applies to control OUT endpoints only.	R/W	1'b0
Reserved	[5]	-	-	1'b0
OUTTknEPdisMsk	[4]	OUT Token Received When Endpoint Disabled Applies to control OUT endpoints only.	R/W	1'b0
SetUPMsk	[3]	SETUP Phase Done Mask Applies to control endpoints only.	R/W	1'b0
AHBErrMsk	[2]	AHB Error	R/W	1'b0
EPDisbldMsk	[1]	Endpoint Disabled Interrupt Mask	R/W	1'b0
XferComplMsk	[0]	Transfer Completed Interrupt Mask	R/W	1'b0

5.8.7.6 Device ALL Endpoints Interrupt Register (DAINT, R, Address = 0xEC00_0818)

If a significant event occurs on an endpoint, a Device All Endpoints Interrupt register interrupts the application using the Device OUT Endpoints Interrupt bit or Device IN Endpoints Interrupt bit of the Core Interrupt register. There is one interrupt bit per endpoint, up to a maximum of 16 bits for OUT endpoints and 16 bits for IN endpoints. For a bidirectional endpoint, the corresponding IN and OUT interrupt bits are used. Bits in this register are set and cleared if the application sets and clears bits in the corresponding Device Endpoint – n Interrupt register.

DAINT	Bit	Description	R/W	Initial State
OutEPInt	[31:16]	OUT Endpoint Interrupt Bits One bit per OUT endpoint : Bit 16 for OUT endpoint 0, bit 31 for OUT endpoint 15	R	16'h0
InEpInt	[15:0]	IN Endpoint Interrupt Bits One bit per IN endpoint : Bit 0 for IN endpoint 0, bit 15 for endpoint 15	R	16'h0

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5.8.7.7 Device ALL Endpoints Interrupt Mask Register (DAINTMSK, R/W, Address = 0xEC00_081C)

The Device Endpoint Interrupt Mask register works with the Device Endpoint Interrupt register to interrupt the application if an event occurs on a device endpoint. However, the Device all Endpoints Interrupt register bit corresponding to that interrupt remains set.

- Mask interrupt: 1'b0
- Unmask interrupt: 1'b1

DAINTMSK	Bit	Description	R/W	Initial State
OutEPMsk	[31:16]	OUT EP Interrupt Mask Bits One bit per OUT endpoint : Bit 16 for OUT EP 0, bit 31 for OUT EP 15	R/W	16'h0
InEpMsk	[15:0]	IN EP Interrupt Mask Bits One bit per IN endpoint : Bit 0 for IN EP 0, bit 15 for IN EP 15	R/W	16'h0

5.8.7.8 Device VBUS Discharge Time Register (DVBUSDIS, R/W, Address = 0xEC00_0828)

This register specifies the VBUS discharge time after VBUS pulsing during SRP.

DVBUSDIS	Bit	Description	R/W	Initial State
Reserved	[31:16]	-	-	16'h0
DVBUSDis	[15:0]	Device VBUS Discharge Time Specifies the VBUS discharge time after VBUS pulsing during SRP. This value equals : VBUS discharge time in PHY clocks /1,024	R/W	16'h0B8F

5.8.7.9 Device VBUS Pulsing Time Register (DVBUSPULSE, R/W, Address = 0xEC00_082C)

This register specifies the VBUS discharge time during SRP.

DVBUSPULSE	Bit	Description	R/W	Initial State
Reserved	[31:12]	-	-	16'h0
DVBUSPulse	[11:0]	Device VBUS Pulsing Time Specifies the VBUS pulsing time during SRP. This value equals : VBUS pulse time in PHY clocks /1,024	R/W	12'h02C6

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5.8.7.10 Device Threshold Control Register (DTHRCTL, R/W, Address = 0xEC00_0830)

Thresholding is not supported in Slave mode and so this register must not be programmed in Slave mode.

DTHRCTL	Bit	Description	R/W	Initial State
Reserved	[31:28]	-	-	4'h0
ArbPrkEn	[27]	Arbiter Parking Enable. This bit controls internal DMA arbiter parking for IN endpoints. When thresholding is enabled and this bit is set to one, then the arbiter parks on the IN endpoint for which there is a token received on the USB. This is done to avoid getting into underrun conditions. By default the parking is enabled.	R/W	1'b1
Reserved	[26]	-	-	-
RxThrLen	[25:17]	Receive Threshold Length This field specifies Receive thresholding size in DWORDS. This field also specifies the amount of data received on the USB before the core can start transmitting on the AHB. The threshold length has to be at least eight DWORDS. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen).	R/W	9'h8
RxThrEn	[16]	Receive Threshold Enable When this bit is set, the core enables thresholding in the receive direction.	R/W	1'b0
Reserved	[15:13]	-	-	-
AHBThrRatio	[12:11]	AHB Threshold Ratio (AHBThrRatio) These bits define the ratio between the AHB threshold and the MAC threshold for the transmit path only. The AHB threshold always remains less than or equal to the USB threshold, because this does not increase overhead. Both the AHB and the MAC threshold must be DWORD-aligned. If the AHB threshold value is not DWORD-aligned after AHBThrRatio is calculated (based on the application's programming of the MAC threshold and AHBThrRatio), the core automatically aligns to the next lower DWORD value. When programming the TxThrLen and AHBThrRatio, the application must ensure that the minimum AHB threshold value does not go below 8 DWORDS to meet the USB turnaround time requirements. • 2'b00: AHB threshold = MAC threshold • 2'b01: AHB threshold = MAC threshold / 2 • 2'b10: AHB threshold = MAC threshold / 4 • 2'b11: AHB threshold = MAC threshold / 8	R/W	2'h0
TxThrLen	[10:2]	Transmit Threshold Length This field specifies Transmit thresholding size in DWORDS. This field specifies the amount of data in bytes to be in the corresponding endpoint transmit FIFO, before the core can start transmit on the USB. The threshold length has to be at least eight DWORDS. This field controls both isochronous and non-isochronous IN endpoint thresholds.	R/W	9'h8

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DTHRCTL	Bit	Description	R/W	Initial State
		The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen).		
ISOThrEn	[1]	ISO IN Endpoints Threshold Enable When this bit is set, the core enables thresholding for isochronous IN endpoints	R/W	1'b0
NonISOThrEn	[0]	Non-ISO IN Endpoints Threshold Enable When this bit is set, the core enables thresholding for Non Isochronous IN endpoints.	R/W	1'b0

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5.8.7.11 Device IN Endpoint FIFO Empty Interrupt Mask Register (DIEPEMPMSK, R/W, Address = 0xEC00_0834)

This register is used to control the IN endpoint FIFO empty interrupt generation (DIEPINTn.TxfEmp).

- Mask interrupt: 1'b0
- Unmask interrupt: 1'b1

DVBUSPULSE	Bit	Description	R/W	Initial State
Reserved	[31:16]	-	-	16'h0
InEpTxfEmpMsk	[15:0]	IN EP Tx FIFO Empty Interrupt Mask Bits These bits acts as mask bits for DIEPINTn. TxFEmp interrupt One bit per IN Endpoint: Bit 0 for IN EP 0, bit 15 for IN EP 15	R/W	16'h0

5.8.7.12 Device Logical Endpoint-Specific Registers

A logical endpoint is unidirectional: it is either IN or OUT. To represent a bidirectional endpoint, two logical endpoints are required, one for the IN direction and the other for the OUT direction. This is also true for control endpoints. The registers and register fields described in this section may pertain to IN or OUT endpoints, or both, or specific endpoint types are noted.

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5.8.7.13 Device Control IN Endpoint 0 Control Register (DIEPCTL0, R/W, Address = 0xEC00_0900)

This section describes the Control IN Endpoint 0 Control register. Nonzero control endpoints use registers for endpoints 1-15.

DIEPCTL0	Bit	Description	R/W	Initial State
EPEna	[31]	Endpoint Enable Indicates that data is ready to be transmitted on the endpoint. The core clears this bit before setting any of the following interrupts on this endpoint. • Endpoint Disabled • Transfer Completed	R_WS_SC	1'b0
EPDis	[30]	Endpoint Disable The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.	R_WS_SC	1'b0
Reserved	[29:28]	-	-	2'b0
SetNAK	[27]	Set NAK A write to this bit sets the NAK bit for the endpoint. Using this bit, the application controls the transmission of NAK handshakes on an endpoint. The core also sets this bit for an endpoint after a SETUP packet is received on that endpoint.	W	1'b0
CNAK	[26]	Clear NAK A write to this bit clears the NAK bit for the endpoint.	W	1'b0
TxFNum	[25:22]	TxFIFO Number This value is set to the FIFO number that is assigned to IN Endpoint 0.	R	4'h0
Stall	[21]	STALL Handshake The application sets this bit, and the core clears it, if a SETUP token is received for this endpoint. If a NAK bit, Global Non-Periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority.	R_WS_SC	1'b0
Reserved	[20]	-	-	1'b0
EPType	[19:18]	Endpoint Type Hardcoded to 00 for control	R	2'h0

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DIEPCTL0	Bit	Description	R/W	Initial State
NAKsts	[17]	NAK Status Indicates the following: • 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status • 1'b1: The core is transmitting NAK handshakes on this endpoint If this bit is set, either by the application or core, the core stops transmitting data, even if there is data available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	R	1'b0
Reserved	[16]	-	-	1'b0
USBActEP	[15]	USB Active Endpoint This bit is always set to 1, indicating that control endpoint 0 is always active in all configurations and interfaces.	R	1'b1
Reserved	[14:2]	-	-	13'h0
MPS	[1:0]	Maximum Packet Size Applies to IN and OUT endpoints. The application must program this field with the maximum packet size for the current logical endpoint. • 2'b00: 64 bytes • 2'b01: 32 bytes • 2'b10: 16 bytes • 2'b11: 8 bytes	R/W	2'h0

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5.8.7.14 Device Control OUT Endpoint 0 Control Register (DOEPCTL0, R/W, Address =0xEC00_0B00)

This section describes the Control OUT Endpoint 0 Control register. Nonzero control endpoints use registers for endpoints 1-15.

DOEPCTL0	Bit	Description	R/W	Initial State
EPEna	[31]	Endpoint Enable When Scatter/Gather DMA mode is enabled, for OUT endpoints this bit indicates that the descriptor structure and data buffer to receive data is setup. • When Scatter/Gather DMA mode is disabled—(such as for buffer-pointer based DMA mode)—this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: • SETUP Phase Done • Endpoint Disabled • Transfer Completed **Note:** In DMA mode, this bit must be set for the core to transfer SETUP data packets into memory.	R_WS_SC	1'b0
EPDis	[30]	Endpoint Disable The application cannot disable control OUT endpoint 0.	R	1'b0
Reserved	[29:28]	-	-	2'b0
SetNAK	[27]	Set NAK A write to this bit sets the NAK bit for the endpoint. Using this bit, the application controls the transmission of NAK handshakes on an endpoint. The core sets this bit on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.	W	1'b0
CNAK	[26]	Clear NAK A write to this bit clears the NAK bit for the endpoint.	W	1'b0
Reserved	[25:22]	-	-	4'h0
Stall	[21]	STALL Handshake The application sets this bit, and the core clears it, if a SETUP token is received for this endpoint. If a NAK bit or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	R_WS_SC	1'b0
Snp	[20]	Snoop Mode This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.	R/W	1'b0
EPType	[19:18]	Endpoint Type Hardcoded to 2'b00 for control.	R	2'h0

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DOEPCTL0	Bit	Description	R/W	Initial State
NAKsts	[17]	NAK Status Indicates the following: • 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status • 1'b1: The core is transmitting NAK handshakes on this endpoint If application or the core sets this bit, the core stops receiving data, even if there is space in the RxFIFO to accommodate the incoming packet. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake	R	1'b0
Reserved	[16]	-	-	1'b0
USBActEP	[15]	USB Active Endpoint This bit is always set to 1, indicating that a control endpoint 0 is always active in all configurations and interfaces.	R	1'b1
Reserved	[14:2]	-	-	13'h0
MPS	[1:0]	Maximum Packet Size The maximum packet size for control OUT endpoint 0 is the same as what is programmed in control IN Endpoint 0. • 2'b00: 64 bytes • 2'b01: 32 bytes • 2'b10: 16 bytes • 2'b11: 8 bytes	R	2'h0

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5.8.7.15 Device Endpoint-n Control Register (DIEPCTLn/DOEPCTLn, R/W, Address = 0xEC00_0900+ n*20h, 0xEC00_0B00+ n*20h)

Endpoint_number:1 ≤ n ≤ 15

The application uses this register to control the behavior of each logical endpoint other than endpoint 0.

DIEPCTLn/ DOEPCTLn	Bit	Description	R/W	Initial State
EPEna	[31]	Endpoint Enable Applies to IN and OUT endpoints. • When Scatter/Gather DMA mode is enabled, • For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. • For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. • When Scatter/Gather DMA mode is enabled—such as for buffer-pointer based DMA mode: - For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. - For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: • SETUP Phase Done • Endpoint Disabled • Transfer Completed **Note:** For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.	R_WS _SC	1'b0
EPDis	[30]	Endpoint Disable Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.	R_WS _SC	1'b0
SetD1PID	[29]	Set DATA1 PID Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. This field is applicable both for Scatter/Gather DMA mode and non- Scatter/Gather DMA mode.	W	1'b0
SetOddFr		Set Odd (micro) frame Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro) frame (EO_FrNum) field to odd (micro) frame. This field is not applicable for Scatter/Gather DMA mode.		
SetD0PID	[28]	Set DATA0 PID Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to	W	1'b0

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DIEPCTLn/ DOEPCTLn	Bit	Description	R/W	Initial State
SetEvenFr		DATA0. This field is applicable both for Scatter/Gather DMA mode and non- Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro) frame (SetEvenFr) Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro) frame (EO_FrNum) field to even (micro) frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure.		
SNAK	[27]	Set NAK Applies to IN and OUT endpoints. A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for OUT endpoints on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.	W	1'b0
CNAK	[26]	Clear NAK Applies to IN and OUT endpoints. A write to this bit clears the NAK bit for the endpoint.	W	1'b0
TxFNum	[25:22]	TxFIFO Number These bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints.	R/W	4'h0
Stall	[21]	STALL Handshake Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	R/W R_WS_SC	1'b0
Snp	[20]	Snoop Mode Applies to OUT endpoints only. This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.	R/W	1'b0
EPType	[19:18]	Endpoint Type Applies to IN and OUT endpoints. This is the transfer type supported by this logical endpoint. • 2'b00: Control	R	2'h0

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DIEPCTLn/ DOEPCTLn	Bit	Description	R/W	Initial State
		• 2'b01: Isochronous • 2'b10: Bulk • 2'b11: Interrupt		
NAKsts	[17]	NAK Status Applies to IN and OUT endpoints. Indicates the following: • 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. • 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: • The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. • For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. • For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	R	1'b0
DPID	[16]	Endpoint Data PID Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. • 1'b0: DATA0 • 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non- Scatter/Gather DMA mode.	R	1'b0
EO_FrNum		Even/ Odd (Micro) Frame In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro) frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro) frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. • 1'b0: Even (micro) frame • 1'b1: Odd (micro) frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure.		
USBActEP	[15]	USB Active Endpoint Applies to IN and OUT endpoints. Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application	R_W_ SC	1'b0

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DIEPCTLn/ DOEPCTLn	Bit	Description	R/W	Initial State
		must program endpoint registers accordingly and set this bit.		
Reserved	[14:11]	-	R/W	4'h0
MPS	[10:0]	Maximum Packet Size Applies to IN and OUT endpoints. The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes.	R/W	11'h0

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5.8.7.16 Device Endpoint-n Interrupt Register (DIEPINTn/DOEPINTn, R/W, Address = 0xEC00_0908 +n*20h, 0xEC00_0B08 +n*20h)

Endpoint_number: $0 \leq n \leq 15$

This register indicates the status of an endpoint with respect to USB- and AHB-related events. The application must read this register if the OUT Endpoints Interrupt bit or IN Endpoints Interrupt bit of the Core Interrupt register is set. Before the application reads this register, it must first read the Device All Endpoints Interrupt (DAINT) register to get the exact endpoint number for the Device Endpoint-n Interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the DAINT and GINTSTS registers.

DIEPINTn/ DOEPINTn	Bit	Description	R/W	Initial State
EPEna	[31:15]	Reserved	-	17'h0
NYETIntrpt	[14]	NYET interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint.	R_SS_WC	1'b0
NAKIntrpt	[13]	NAK interrupt (NAKIntrpt) The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo.	R_SS_WC	1'b0
BbleErrIntrpt	[12]	BbleErr (Babble Error) interrupt (BbleErrIntrpt) The core generates this interrupt when babble is received for the endpoint.	R_SS_WC	1'b0
Packet Dropped Status	[11]	PktDrpSts (Packet Dropped Status) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.	R_SS_WC	1'b0
Reserved	[10]	-	-	-
BNAIntr	[9]	Buffer Not Available Interrupt This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done	R_SS_WC	
TxfifoUndrn	[8]	Fifo Underrun Applies to IN endpoints Only This bit is valid only when thresholding is enabled. The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint.	R_SS_WC	1'b0
OutPktErr		OUT Packet Error Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet.		

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DIEPINTn/ DOEPINTn	Bit	Description	R/W	Initial State
TxFEmp	[7]	Transmit FIFO Empty This bit is valid only for IN Endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)).		
INEPNakEff	[6]	IN Endpoint NAK Effective Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCTLn.CNAK. This interrupt indicates that the core has sampled the NAK bit set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit.	R	1'b0
Back2Back SETup		Back-to-Back SETUP Packets Receive Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. For information about handling this interrupt,	R/W	
INTknEPMis	[5]	IN Token Received with EP Mismatch Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received.	R_SS_WC	1'b0
StsPhseRcvd		Status Phase Received For Control Write This interrupt is valid only for Control OUT endpoints and only in Scatter Gather DMA mode. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in case of Scatter Gather DMA mode.		
INTknTXFEmp	[4]	IN Token Received When TxFIFO is Empty Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received.	R_SS_WC	1'b0

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DIEPINTn/ DOEPINTn	Bit	Description	R/W	Initial State
OUTTknEPdis		OUT Token Received When Endpoint Disabled Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received.		
TimeOUT	[3]	Timeout Condition • In dedicated FIFO mode, applies only to Control IN endpoints. • In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint.	R_SS_WC	1'b0
SetUp		SETUP Phase Done Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet.	-	
AHBErr	[2]	AHB Error Applies to IN and OUT endpoints. This is generated only in Internal DMA mode if there is an AHB error during an AHB read/write. The application reads the corresponding endpoint DMA address register to get the error address.	R_SS_WC	1'b0
EPDisbld	[1]	Endpoint Disabled Interrupt Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.	R_SS_WC	1'b0
XferCompl	[0]	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. • When Scatter/Gather DMA mode is enabled • For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. • For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. • When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.	R_SS_WC	1'b0

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5.8.7.17 Device Endpoint 0 Transfer Size Register (DIEPTSIZ0, R/W, Address = 0xEC00_0910)

The application must modify this register before enabling endpoint 0. Once endpoint 0 is enabled using Endpoint Enable bit of the Device Control Endpoint 0 Control registers (DIEPCTL0.EPEna/DOEPCTL0.EPEna), the core modifies this register. The application can only read this register once the core has cleared the Endpoint Enable bit.

Nonzero endpoints use the registers for endpoints 1-15.
When Scatter/Gather DMA mode is enabled, this register must not be programmed by the application. If the application reads this register when Scatter/Gather DMA mode is enabled, the core returns all zeros.

DIEPTSIZ0	Bit	Description	R/W	Initial State
Reserved	[31:21]	-	-	11'h0
PktCnt	[20:19]	Packet Count Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This field is decremented every time a packet is read from the TxFIFO.	R/W	2'b0
Reserved	[18:7]	-	-	12'h0
XferSize	[6:0]	Transfer Size Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO.	R/W	7'h0

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5.8.7.18 Device OUT Endpoint 0 Transfer Size Register (DOEPTSIZ0, R/W, Address = 0xEC00_0B10)

DOEPTSIZ0	Bit	Description	R/W	Initial State
Reserved	[31]	-	-	1'b0
SUPCnt	[30:29]	SETUP Packet Count This field specifies the number of back-to-back SETUP data packets the endpoint can receive. • 2'b01: 1 packet • 2'b10: 2 packets • 2'b11: 3 packets	R/W	2'h0
Reserved	[28:21]	-	-	9'h0
PktCnt	[20:19]	Packet Count This field is decremented to zero after a packet is written into the RxFIFO.	R/W	2'b0
Reserved	[18:7]	-	-	12'h0
XferSize	[6:0]	Transfer Size Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from RxFIFO and written to the external memory.	R/W	7'h0

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5.8.7.19 Device Endpoint-n Transfer Size Register (DIEPTSIZn/DOEPTSIZn, R/W, Address = 0xEC00_0910 +n*20h, 0xEC00_0B10 +n*20h)

Endpoint_number: 1 ≤ n ≤ 15

The application must modify this register before enabling the endpoint. Once the endpoint is enabled using Endpoint Enable bit of the Device Endpoint-n Control registers (DIEPCTLn.EPEna/DOEPCTLn.EPEna), the core modifies this register. The application can only read this register once the core has cleared the Endpoint Enable bit. This register is used only for endpoints other than Endpoint 0.
When Scatter/Gather DMA mode is enabled, this register must not be programmed by the application. If the application reads this register when Scatter/Gather DMA mode is enabled, the core returns all zeros

DIEPTSIZn/ DOEPTSIZn	Bit	Description	R/W	Initial State
Reserved	[31]	-	-	1'b0
MC	[30:29]	Multi Count Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. • 2'b01: 1 packet • 2'b10: 2 packets • 2'b11: 3 packets	R/W	2'b0
RxDPID		For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetch for an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp).	R	
SUPCnt		Received Data PID Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. • 2'b00: DATA0 • 2'b01: DATA1 • 2'b10: DATA2 • 2'b11: MDATA	R	
		SETUP Packet Count Applies to control OUT Endpoints only. This field specifies the number of back-to-back SETUP data packets the endpoint can receive. • 2'b01: 1 packet • 2'b10: 2 packets • 2'b11: 3 packets	R/W	
PktCnt	[28:19]	Packet Count Indicates the total number of USB packets that constitute the Transfer Size amount of data for this endpoint. • IN Endpoints: This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. • OUT Endpoints: This field is decremented every time a packet (maximum size or short packet) is written to the RxFIFO.	R/W	10'h0

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DIEPTSIZn/ DOEPTSIZn	Bit	Description	R/W	Initial State
XferSize	[18:0]	Transfer Size This field contains the transfer size in bytes for the current endpoint. The core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. • IN Endpoints: The core decrements this field every time a packet from the external memory is written to the TxFIFO. • OUT Endpoints: The core decrements this field every time a packet is read from the RxFIFO and written to the external memory.	R/W	19'h0

5.8.7.20 Device Endpoint-n DMA Address (DIEPDMAn/DOEPDMAn, R/W, Address = 0xEC00_0914 +n*20h, 0xEC00_0B14 +n*20h)

Endpoint_number : $0 \leq n \leq 15$

The starting DMA address must be DWORD-aligned.

DIEPDMAn/ DOEPDMAn	Bit	Description	R/W	Initial State
DMAAddr	[31:0]	DMA Address Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. • When Scatter/Gather DMA mode is not enabled, When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list.	R/W	32'h0

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5.8.7.21 Device IN Endpoint Transmit FIFO Status (DTXFSTSn, R/W, Address = 0xEC00_0918 +n*20h)

Endpoint_number: 0 ≤ n ≤ 15

This read-only register contains the free space information for the Device IN endpoint TxFIFO

DTXFSTSn	Bit	Description	R/W	Initial State
Reserved	[31:16]	-		16'h0
INEPTxFSpcAvail	[15:0]	IN Endpoint TxFIFO Space Avail Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. • 16'h0: Endpoint TxFIFO is full • 16'h1: 1 word available • 16'h2: 2 words available • 16'hn: n words available (where 0 ≤ n ≤ 32,768) • 16'h8000: 32,768 words available • Others: Reserved	R	16'h100

5.8.7.22 Device Endpoint-n DMA Buffer Address Register (DIEPDMABn/DOEPDMABn, R/W, Address = 0xEC00_091C +n*20h, 0xEC00_B1C +n*20h)

Endpoint_number: 0 ≤ n ≤ 15

These fields are present only in case of Scatter/Gather DMA.

DIEPDMABn/DOEPDMABn	Bit	Description	R/W	Initial State
DMABufferAddr	[31:0]	DMA Buffer Address Holds the current buffer address. This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved.	R	32'h0

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6 MODEM INTERFACE

6.1 OVERVIEW OF MODEM INTERFACE

This chapter defines the interface between the Base-band Modem (like MSM) and the Application Processor to facilitate data-exchange between these two devices. To facilitate data-exchange, S5PV210 include a dual-ported SRAM buffer (on-chip). To access SRAM buffer, the Modem chip uses a typical asynchronous-SRAM interface.

The size of the SRAM buffer is 16 KB. This specification specifies a few pre-defined special addressees for the buffer status and interrupts requests.

Modem chip writes data in the data buffer (Internal dual port SRAM buffer) and request interrupt to AP. When the interrupt is asserted, AP reads data in data buffer, and then clears the interrupt. In the same manner, AP writes data in the data buffer and then asserts interrupt to modem chip to notify.

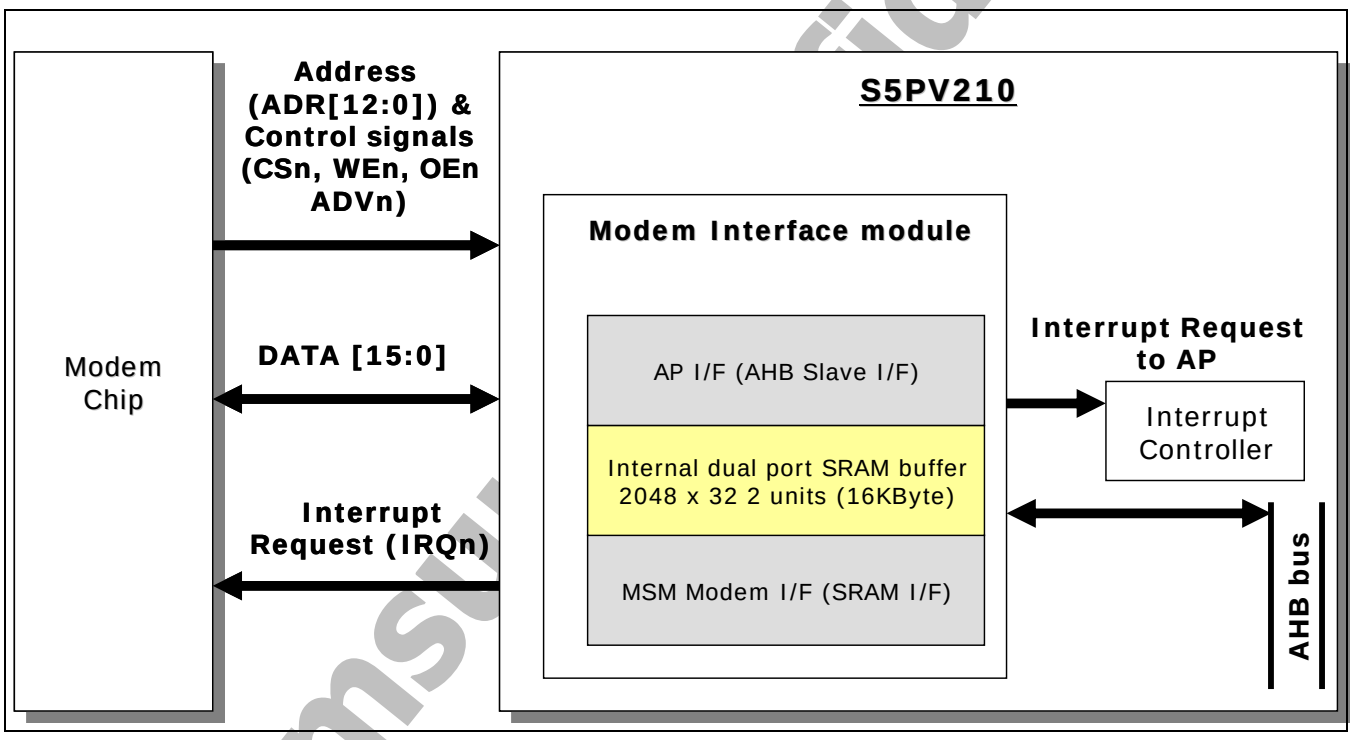

Figure 6-1 Interface with the Modem Chip and the MODEM I/F Block Diagram

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6.2 KEY FEATURES OF MODEM INTERFACE

- Asynchronous SRAM interface style interface
- Supports both Standard mode and Address Muxed mode
- Supports 16-bit parallel bus for data transfer
- Supports 16 KB internal dual-port SRAM buffer
- Supports Interrupt request for data exchange
- Programmable interrupt port address
- Supports DMA for data transfer without intervention of CPU

6.3 INTERRUPT PORTS

If the Modem chip or AP accesses the interrupt-port (predefined special addresses) interrupts are requested or cleared. The S5PV210 configures the special address and the default address-map is described in the *Table 6-1*.

Table 6-1 Interrupt Request and Clear Conditions

Interrupt	An Interrupt is requested, when	Interrupt is cleared, when
To AP	Modem chip writes at least 1 to 0x1FFF through ADR.	AP writes at least 1 to MSMINTCLR register in MODEM IF (2).
To Modem	AP writes 1 to 0xED00_3FFC through internal-chip AHB bus.	Modem chip writes 1 to the bits at 0x1FFE through ADR.

NOTE:

1. There are two address views for MODEMIF, namely, MSM address (ADR) for MODEM chip, and AHB address for S5PV210. AHB address is twice the size of ADR. For example, 0x3FFC at AHB bus is 0x1FFE at ADR. helps you to understand it.
   This is default value. To change the value use SFR (INT2AP and INT2MSM).
2. Modem interface block has one Interrupt Clear Registers; MSMINTCLR. Modem interface block generates level type interrupt request and is sustained until the S5PV210 clears the interrupt clear registers by writing any value to the registers.

Modem chip or S5PV210 reads the data that indicates what event occurred, namely, data transfer requested, data transfer done, special command issued, etc. – from interrupt port address. That data format should be defined for communication between the modem chip and S5PV210.

6.3.1 WAKEUP

* S5PV210 MODEM_IF does not support Wakeup Interrupt mode

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6.4 ADDRESS MAPPING

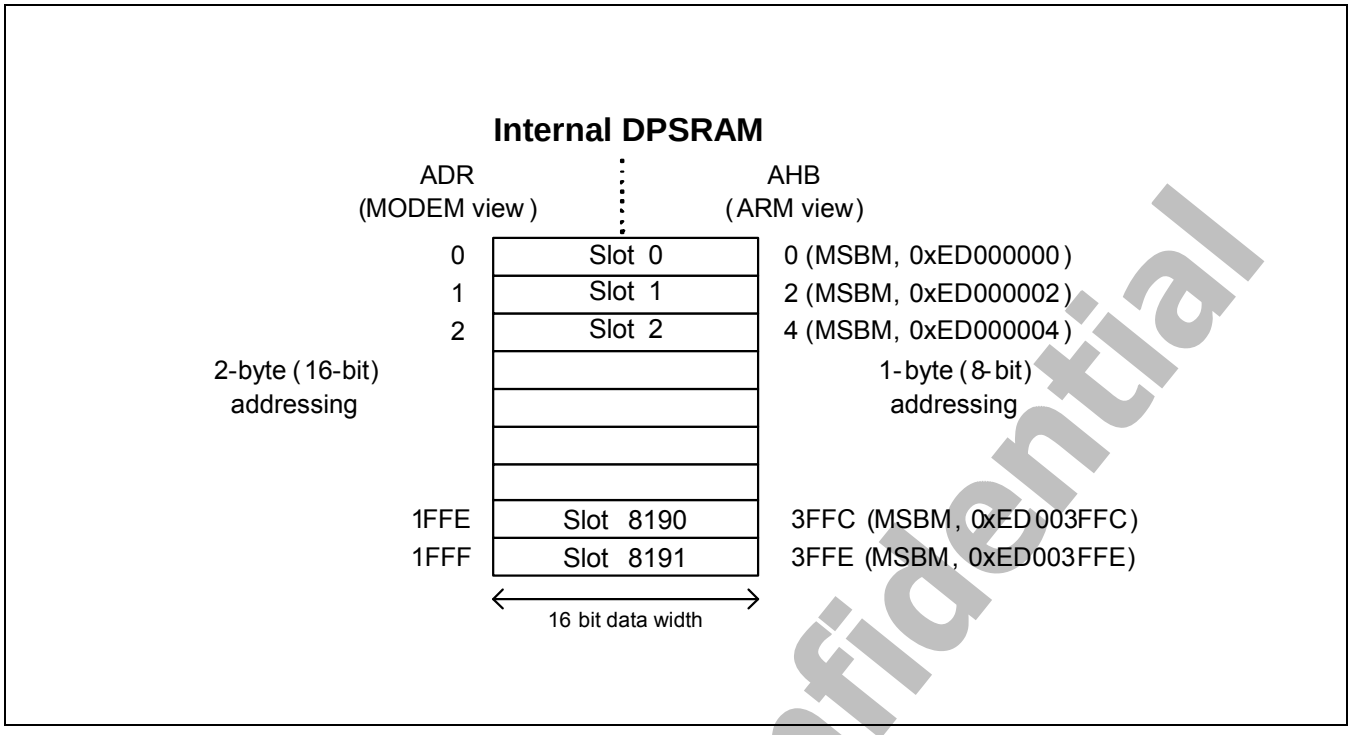

Figure 6-2 MODEM I/F Address Mapping

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6.5 TIMING DIAGRAM

6.5.1 STANDARD MODE WRITE, READ TIMING

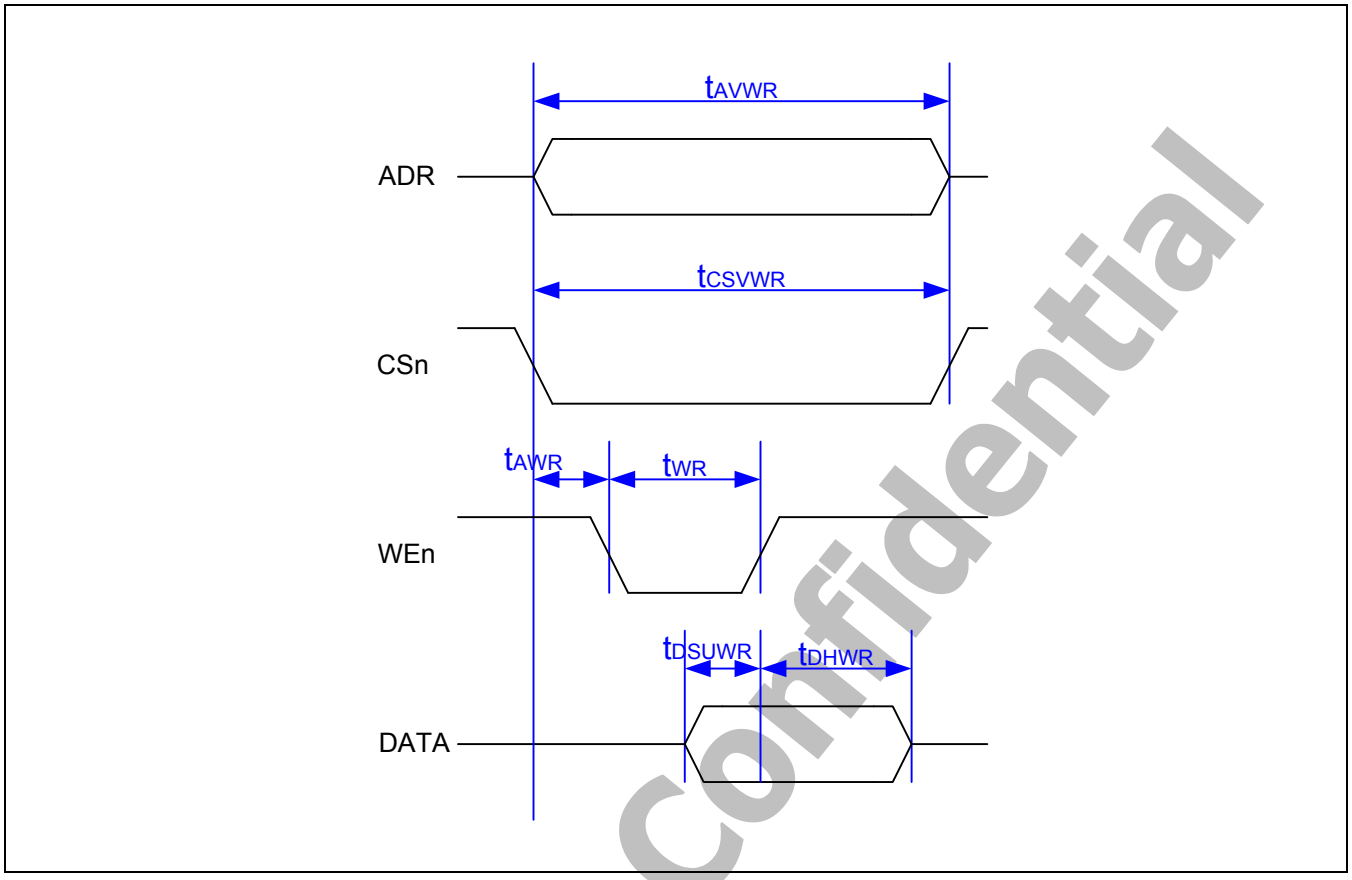

Figure 6-3 Modem Interface Write Timing Diagram (Standard Mode)

Table 6-2 Modem Interface Write Timing (Standard Mode)

Parameter	Description	Min (ns)	Max (ns)	Notes
t_{AVWR}	Address valid to address invalid	16 ns	-	-
t_{CSVWR}	Chip select active	16 ns	-	-
t_{AWR}	Address valid to write active	4 ns	-	-
t_{WR}	Write active	8 ns	-	-
t_{DSUWR}	Write data setup	8 ns	-	-
t_{DHWR}	Write data hold	4 ns	-	-

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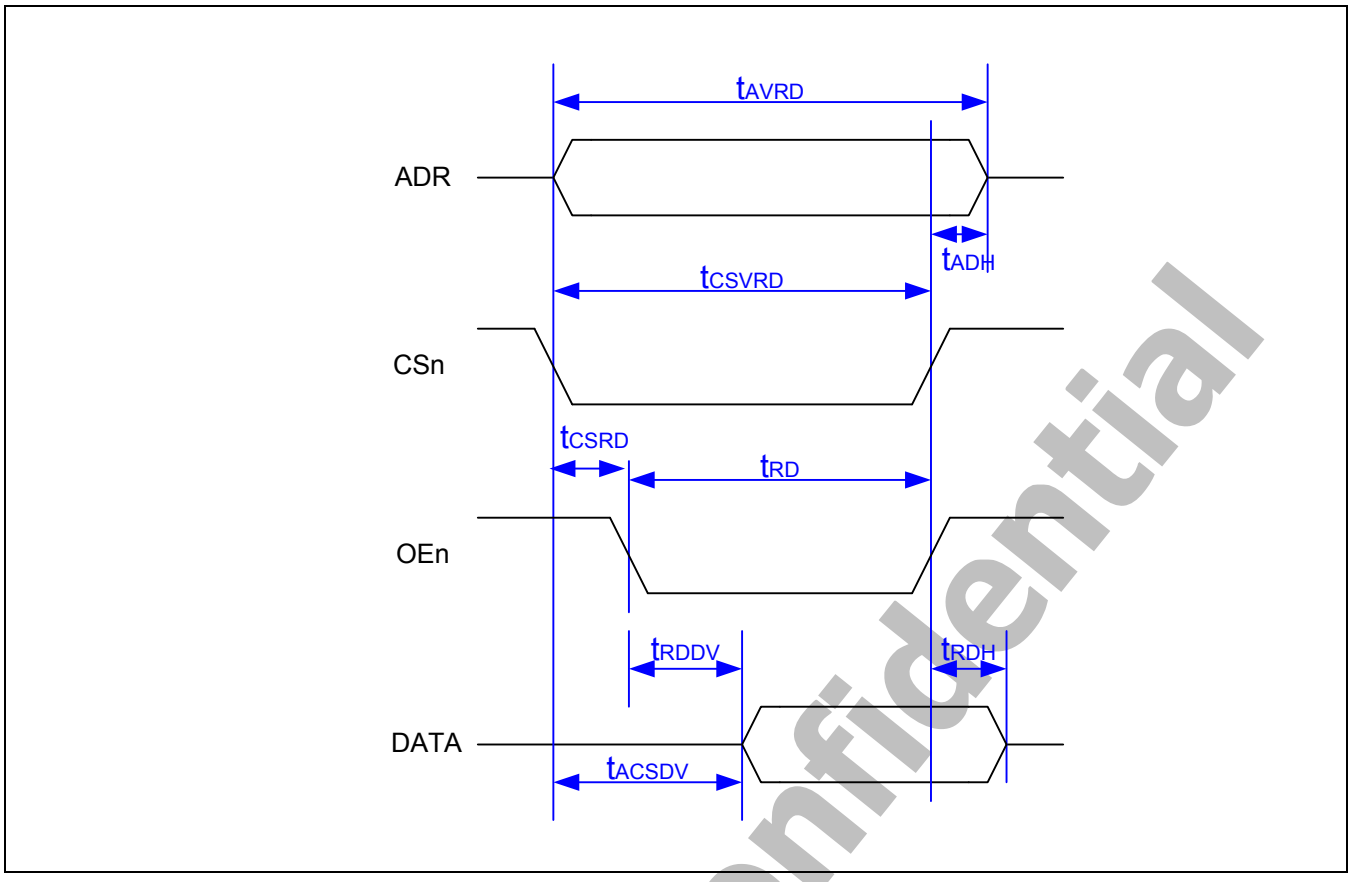

Figure 6-4 Modem Interface Read Timing Diagram (Standard Mode)

Table 6-3 Modem Interface Read Timing (Standard Mode)

Parameter	Description	Min (ns)	Max (ns)	Notes
t_{AVRD}	Address valid to address invalid	50 ns	-	-
t_{ADH}	Address hold	0 ns	-	-
t_{CSVRD}	Chip select active	50 ns	-	-
t_{CSRD}	Chip select active to read active	14 ns	-	-
t_{RD}	Read active	36 ns	-	-
t_{RDDV}	Read active to data valid	-	35 ns	-
t_{RDH}	Read data hold	6 ns	-	-
t_{ACSDV}	Address and chip select active to data valid	-	49 ns	-

NOTE: Output load is 30pF in room temperature (25 Degree)

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6.5.2 ADDRESS MUXED MODE WRITE, READ TIMING

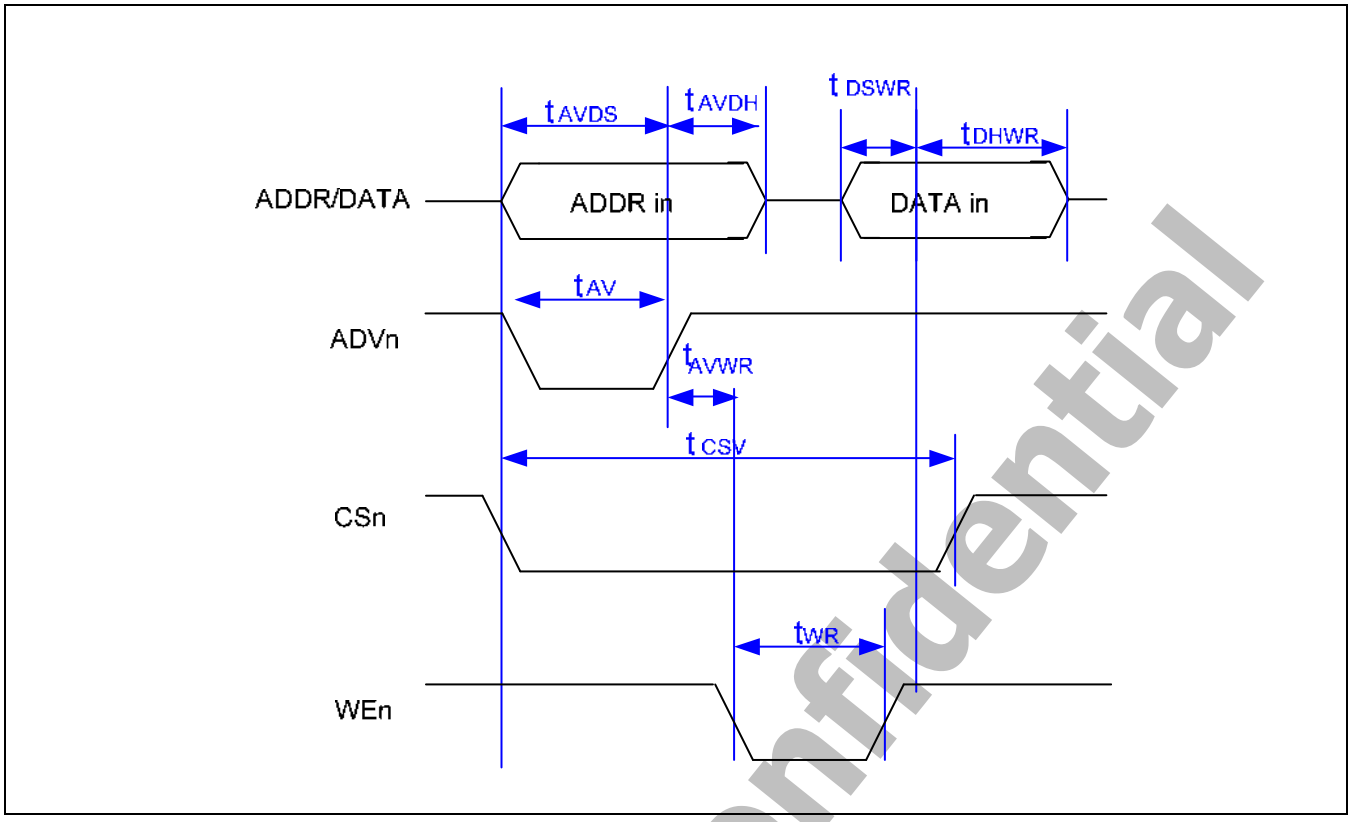

Figure 6-5 Modem Interface Write Timing Diagram (Address Muxed mode)

Table 6-4 Modem Interface Write Timing (Address Muxed mode)

Parameter	Description	Min (ns)	Max (ns)	Notes
t_{AVDS}	Address valid setup	15 ns	-	-
t_{AVDH}	Address valid hold	5 ns	-	-
t_{AV}	Address valid duration	15 ns	-	-
t_{AVWR}	Address valid to write enable	0 ns	-	-
t_{CSV}	Chip select duration	20 ns	-	-
t_{WR}	Write enable duration	5 ns	-	-
t_{DSWR}	Write data setup	8 ns	-	-
t_{DHWR}	Write data hold	4 ns	-	-

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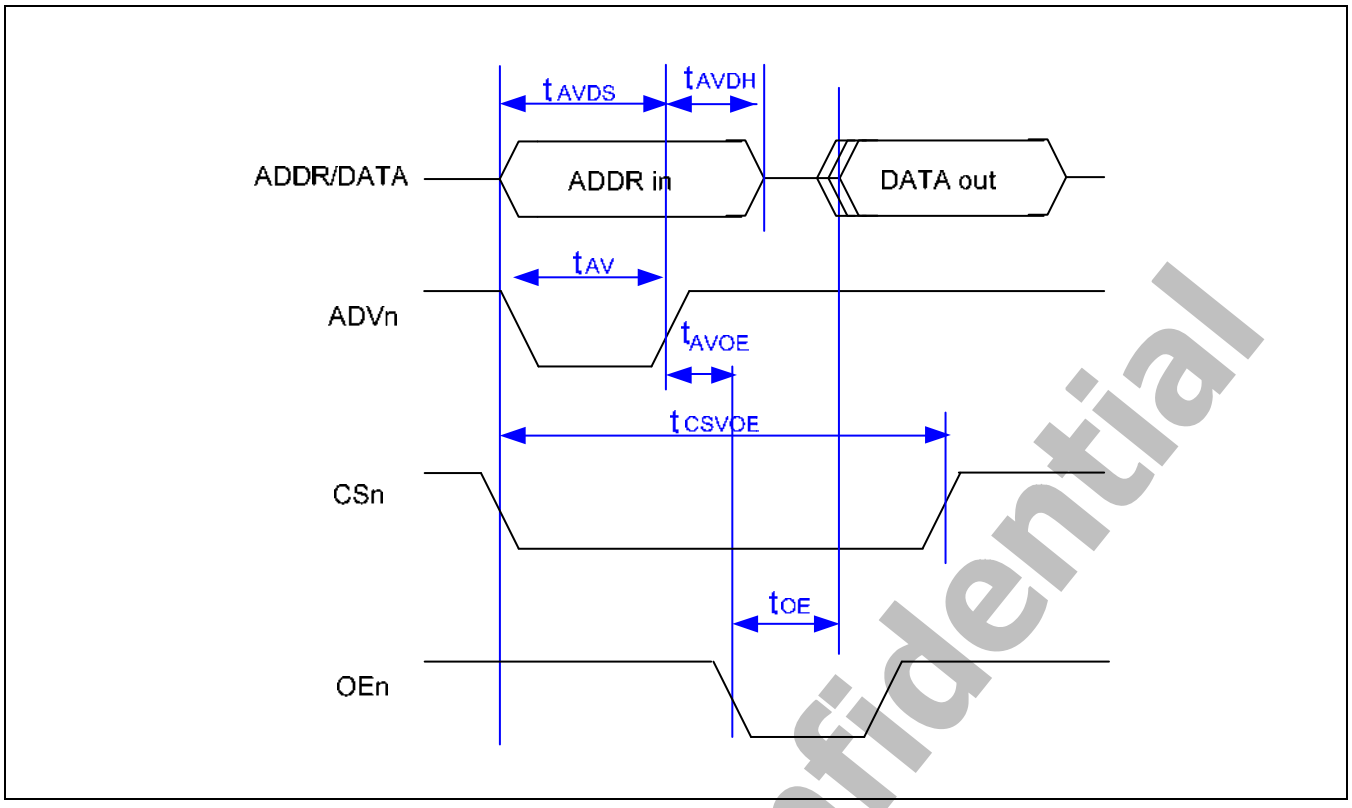

Figure 6-6 Modem Interface Read Timing Diagram (Address Muxed mode)

Table 6-5 Modem Interface Read Timing (Address Muxed mode)

Parameter	Description	Min (ns)	Max (ns)	Notes
t_{AVDS}	Address valid setup	15 ns	-	-
t_{AVDH}	Address valid hold	5 ns	-	-
t_{AV}	Address valid duration	15 ns	-	-
t_{AVOE}	Address valid to read enable	5 ns	-	-
t_{CSVOE}	Chip select duration (Read mode)	45 ns	-	-
t_{OE}	Output enable(Read Active) to data valid	-	35 ns	-

NOTE: Output load is 30pF in room temperature (25 Degree)

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6.6 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
ADR[12:0]	Input	Address from MODEM Chip	XmsmADDR[12:0]	muxed
CSn	Input	Chip Select Signal from MODEM Chip	XmsmCSn	muxed
WEn	Input	Write Enable Signal from MODEM Chip	XmsmWEn	muxed
OEn	Input	Read Enable Signal from MODEM Chip	XmsmRn	muxed
DATA[15:0]	In/Out	Data from/to MODEM Chip	XmsmDATA[15:0]	muxed
IRQn	Output	Interrupt Request to MODEM Chip	XmsmIRQn	muxed
ADVn	Input	Address Valid from MODEM Chip (Only Address Muxed mode)	XmsmADVn	muxed

NOTE: Type field indicates whether pads are dedicated to the signal or pads are connected to the multiplexed signals.

6.7 SOFTWARE INTERFACE AND REGISTERS

This modem interface provides a generic data-exchange method. This interface does not implement any other complex features except for the interrupt-request/ clear such as automatic FIFO managements, and so on. The software should be responsible for required functionalities for the data exchange between the modem chip and the S5PV210, namely, data exchange protocol, data buffer managements, and so on.

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6.8 REGISTER DESCRIPTION

6.8.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
MSBM	0xED00_0000 ~ 0xED00_3FFC	R/W	Specifies the MODEM I/F SRAM Buffer Memory (AP side)	-
INT2AP	0xED00_8000	R/W	Specifies the Interrupt Request to AP Register	0x00003FFE
INT2MSM	0xED00_8004	R/W	Specifies the Interrupt Request to MSM Modem Register	0x00003FFC
MIFCON	0xED00_8008	R/W	Specifies the Modem Interface Control Register	0x00100008
MIFPCON	0xED00_800C	R/W	Specifies the Modem Interface Port Control register	0x00000000
MSMINTCLR	0xED00_8010	W	Specifies the MSM Modem Interface Pending Interrupt Request Clear	-
DMA_TX_ADR	0xED00_8014	R/W	Specifies the DMA TX Request Address Register	0x17FE_13FE
DMA_RX_ADR	0xED00_8018	R/W	Specifies the DMA RX Request Address Register	0x1FFE_1BFE

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6.8.1.1 Interrupt Request to AP Register (INT2AP, R/W, Address = 0xED00_8000)

INT2AP	Bit	Description	Initial State
Reserved	[31:14]	Reserved	0
INT2AP_ADR	[13:0]	Modem interface requests the interrupt to S5PV210 if modem chip writes this address. Interrupt controller of S5PV210 and write access to the MSMINTCLR register clears this interrupt.	0x3FFE

6.8.1.2 Interrupt Request to Modem Register (INT2MSM, R/W, Address = 0xED00_8004)

INT2MSM	Bit	Description	Initial State
Reserved	[31:14]	Reserved	0
INT2MSM_ADR	[13:0]	Modem interface (in this module) requests the interrupt to modem chip if AP writes this address and clears the interrupt if modem chip write 1 to the corresponding bit field.	0x3FFC

NOTE: It is recommended that S5PV210 write data with half-word access on the interrupt port because S5PV210 overwrites the data in INT2AP if there are INT2AP and INT2MSM sharing the same word.

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6.8.1.3 Modem Interface Control Register (MIFCON, R/W, Address = 0xED00_8008)

MIFCON	Bit	Description	Initial State
Reserved	[31:21]	-	0
Fixed	[20]	Should write as 1	1
DMARXREQEN_1	[19]	Enables MSM Write DMA Request (RX 1) to AP (DMA Controller)	0
DMARXREQEN_0	[18]	Enables MSM Write DMA Request (RX 0) to AP (DMA Controller)	0
DMATXREQEN_1	[17]	Enables MSM Read DMA Request (TX 1) to AP (DMA Controller)	0
DMATXREQEN_0	[16]	Enables MSM Read DMA Request (TX 0) to AP (DMA Controller)	0
Reserved	[15:4]	-	0
INT2MSMEN	[3]	Enables Interrupt to MSM (Modem) : MSM_nIRQ is interrupt signal enable. 0 = Disables 1 = Enables	1
INT2APEN	[2]	Enables MSM (Modem) write interrupt to AP 0 = Disable s 1 = Enables	0
Reserved	[1]	Reserved	0
Fixed	[0]	Fixed to 0	0

6.8.1.4 Modem Interface Port Control Register (MIFPCON, R/W, Address = 0xED00_800C)

MIFPCON	Bit	Description	Initial State
Reserved	[31:7]	-	0
ADM_MODE	[6]	Address Muxed mode selection 0 = Disables 1 = Enables	0
Reserved	[5]	Fixed to 0	0
INT2M_LEVEL	[4]	Fixed to 0	0
Fixed	[3:0]	Fixed to 0	0

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6.8.1.5 MSM Interrupt Clear Register (MSMINTCLR, W, Address = 0xED00_8010)

MSMINTCLR	Bit	Description	Initial State
MSMINTCLR	[31:0]	Write access to this register with any data will clear the interrupt pending register of MSM modem interface.	-

NOTE: The interrupt controllers of S5PV210 receive level-triggered type interrupt requests. Therefore, interrupt requests from MSM interface are maintained until the interrupt service routine clears the interrupt pending register by writing any data into this register.

6.8.1.6 DMA Request TX Address Register used at Direct Mode (DMAREQ_TX_ADR, R/W, Address = 0xED00_8014)

INT2AP	Bit	Description	Initial State
Reserved	[31:30]	Reserved	0
DMA_TX_ADR_1	[29:16]	Modem interface requests the DMA to AP (DMA Controller) if modem chip reads this address. Source: DMA_MSM_Req[1]	0x17FE
Reserved	[15:14]	Reserved	0
DMA_TX_ADR_0	[13:0]	Modem interface requests the DMA to AP (DMA Controller) if modem chip reads this address. Source: DMA_MSM_Req[0]	0x13FE

6.8.1.7 DMA Request RX Address Register used at Direct Mode (DMAREQ_RX_ADR, R/W, Address = 0xED00_8018)

INT2AP	Bit	Description	Initial State
Reserved	[31:30]	Reserved	0
DMA_RX_ADR_1	[29:16]	Modem interface requests the DMA to AP (DMA Controller) if modem chip writes this address. Source: DMA_MSM_Req[3]	0x1FFE
Reserved	[15:14]	Reserved	0
DMA_RX_ADR_0	[13:0]	Modem interface requests the DMA to AP (DMA Controller) if modem chip writes this address. Source: DMA_MSM_Req[2]	0x1BFE

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7 SD/MMC CONTROLLER

This chapter describes the Secure Digital (SD/ SDIO), MultiMediaCard (MMC), CE-ATA host controller and related registers supported by S5PV210 RISC microprocessor.

7.1 OVERVIEW OF SD/ MMC CONTROLLER

The SD/ MMC host controller is a combo host for Secure Digital card and MultiMediaCard. This host controller is based on SD Association's (SDA) Host Standard Specification.

The SD/ MMC host controller is a interface between system and SD/MMC. The performance of this host is very powerful, as clock rate is 52-MHz and access 8-bit data pin simultaneously.

7.2 KEY FEATURES OF SD/ MMC CONTROLLER

The High-Speed MMC controller supports:

- SD Standard Host Specification Version 2.0 standard
- SD Memory Card Specification Version 2.0 / High Speed MMC Specification Version 4.3 standard
- SDIO Card Specification Version 1.0 standard
- 512 bytes FIFO for data Tx/ Rx
- CPU Interface and DMA data transfer mode
- 1-bit / 4-bit / 8-bit mode switch
- 8-bit 2 channel, or 4-bit 4 channel
- Auto CMD12
- Suspend/ Resume
- Read Wait operation
- Card Interrupt
- CE-ATA mode

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7.3 BLOCK DIAGRAM OF SD/ MMC CONTROLLER

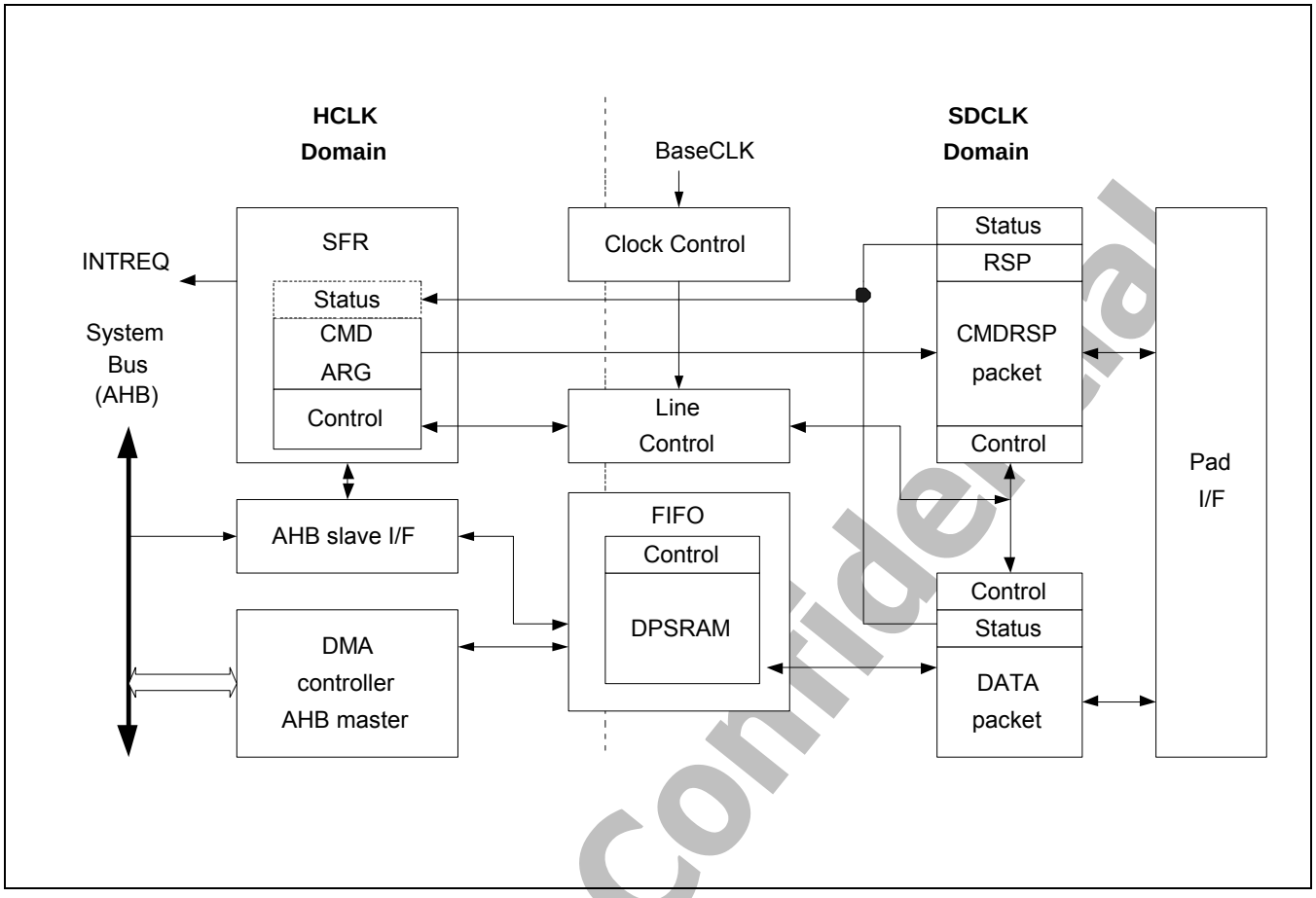

Figure 7-1 SDMMC Clock Domain

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7.4 OPERATION SEQUENCE

This section defines basic operation flow chart divided into several sub sequences. "Wait for interrupts" is used in the flow chart. This means the Host Driver waits until specified interrupts are asserted. If already asserted, then follow the next step in the flow chart. Timeout checking is only available when interrupt is not generated. and it is not described in the flow chart.

7.4.1 SD CARD DETECTION SEQUENCE

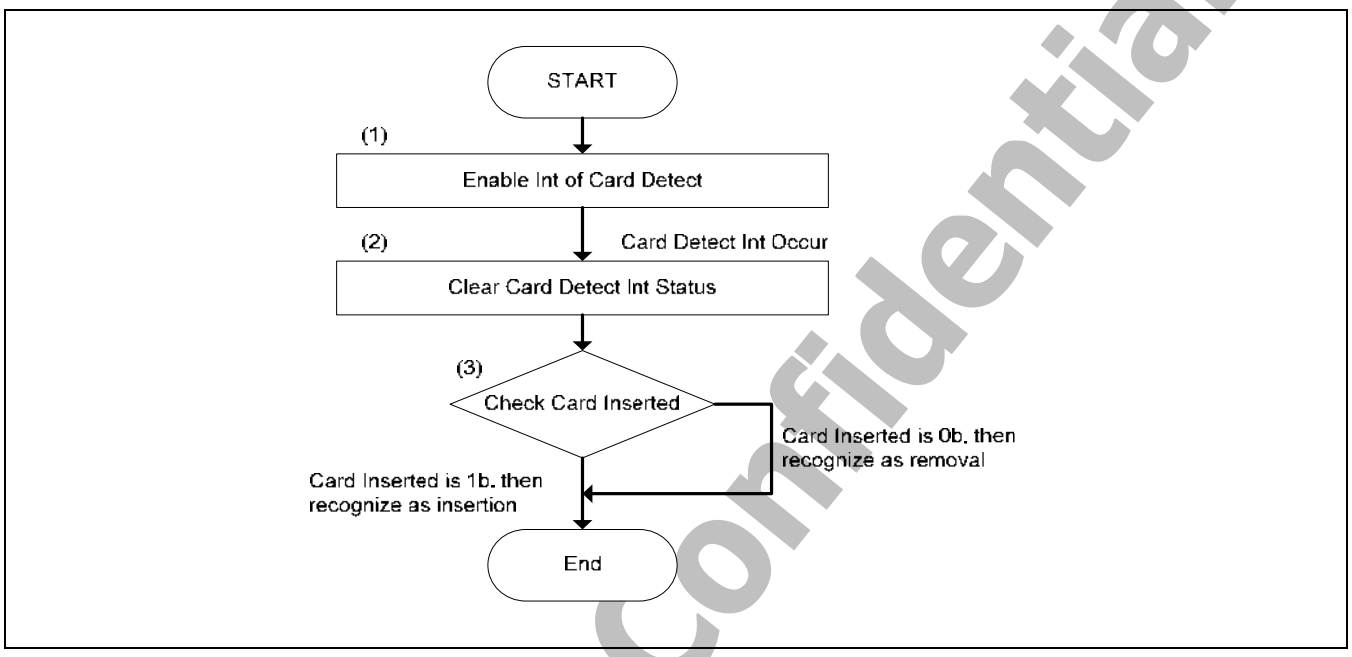

Figure 7-2 SD Card Detect Sequence

The flow chart to detect a SD card is shown in *Figure 7-2.* The steps to detect SD card:

1. To enable interrupt for card detection, write 1 to the following bits:
   Card Insertion Status Enable (ENSTACARDNS) in the Normal Interrupt Status Enable register
   Card Insertion Signal Enable (ENSIGCARDNS) in the Normal Interrupt Signal Enable register
   Card Removal Status Enable (ENSTACARDREM) in the Normal Interrupt Status Enable register
   Card Removal Signal Enable (ENSIGCARDREM) in the Normal Interrupt Signal Enable register

2. If Host Driver detects the card insertion or removal, it clears the interrupt statuses. If Card Insertion interrupt (STACARDINS) is generated, write 1 to Card Insertion in the Normal Interrupt Status register. If Card Removal interrupt (STACARDREM) is generated, write 1 to Card Removal in the Normal Interrupt Status register.

3. Check Card Inserted in the Present State register. If Card Inserted (INSCARD) is 1, the Host Driver supplies power and clock to the SD card. If Card Inserted is 0, it stops the executing process of the Host Driver.

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7.4.2 SD CLOCK SUPPLY SEQUENCE

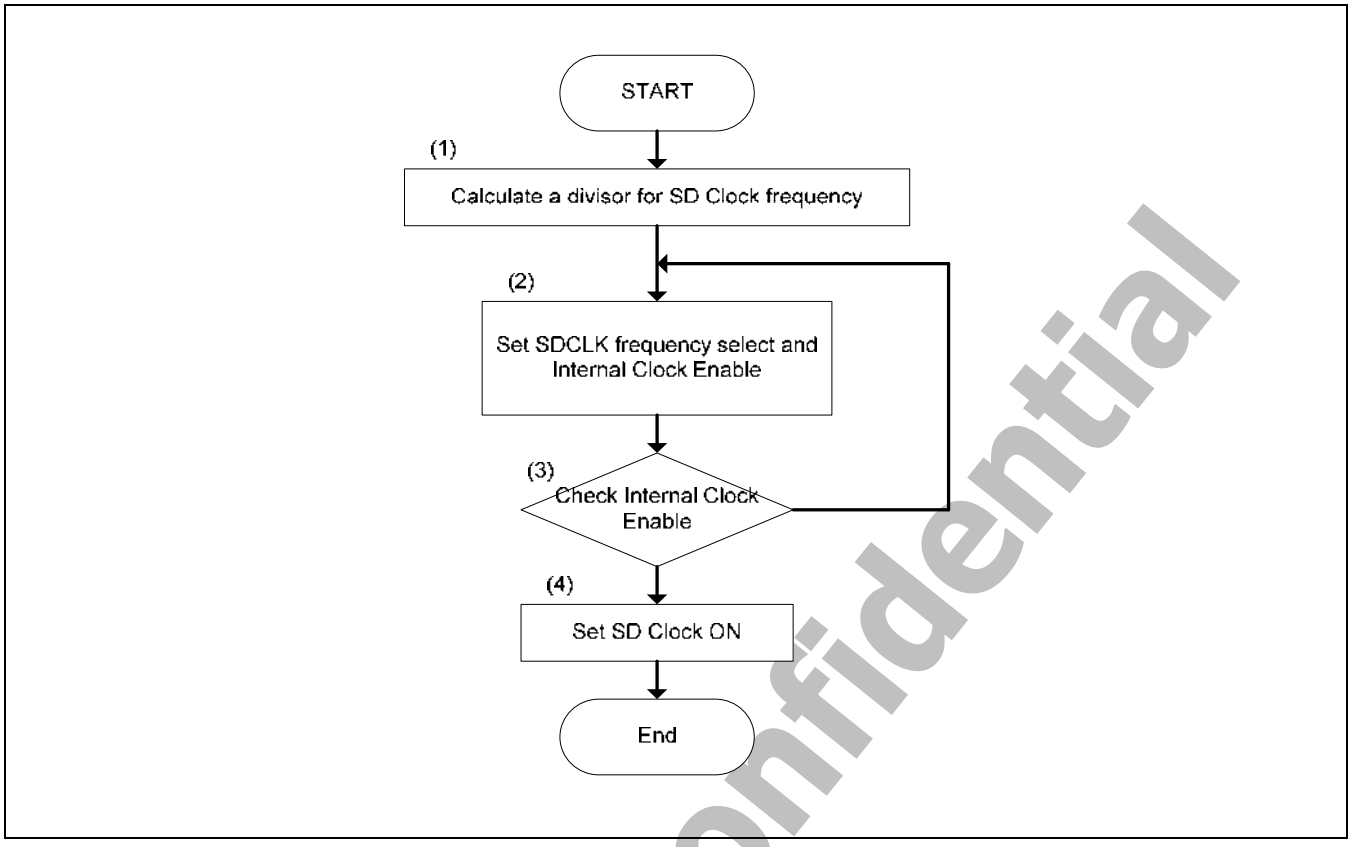

Figure 7-3 SD Clock Supply Sequence

The sequence to set SD Clock to a SD card is shown in *Figure 7-3*. The clock is enabled before one of the following actions:

- a) Issuing a SD command
- b) Detect an interrupt from a SD card in 4-bit mode.

The steps to set SD Clock to a SD card:

1. Calculate a divisor to determine SD Clock frequency for SD Clock by reading Base Clock Frequency. Refer to clock control register (9.15).
2. Set Internal Clock Enable (ENINTCLK) and SDCLK Frequency Select in the Clock Control register in accordance with the calculated result of step (1).
3. Check Internal Clock Stable (STBLINTCLK) in the Clock Control register. Repeat this step until Clock Stable is 1.
4. Set SD Clock Enable (ENSDCLK) in the Clock Control register to 1. After ENSDCLK is set, the Host Controller starts SD Clock.

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7.4.3 SD CLOCK STOP SEQUENCE

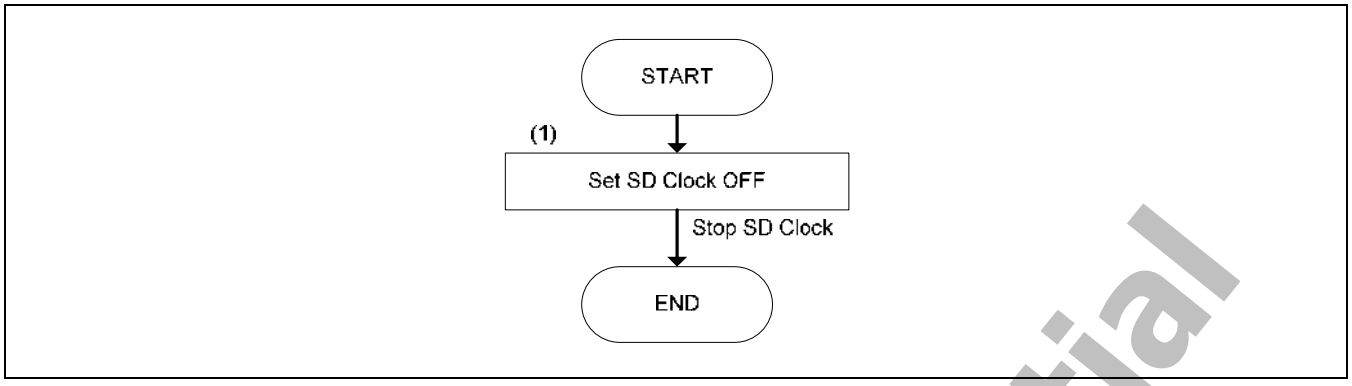

Figure 7-4 SD Clock Stop Sequence

The flow chart to stop the SD Clock is shown in *Figure 7-4* The Host Driver does not stop the SD Clock if a SD transaction takes place on the SD Bus -- namely, either Command Inhibit (DAT) or Command Inhibit (CMD) in the Present State register is set to 1.

1. Set SD Clock Enable (ENSDCLK) in the Clock Control register to 0. After ENSDCLK is set, the Host Controller stops SD Clock.

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7.4.4 SD CLOCK FREQUENCY CHANGE SEQUENCE

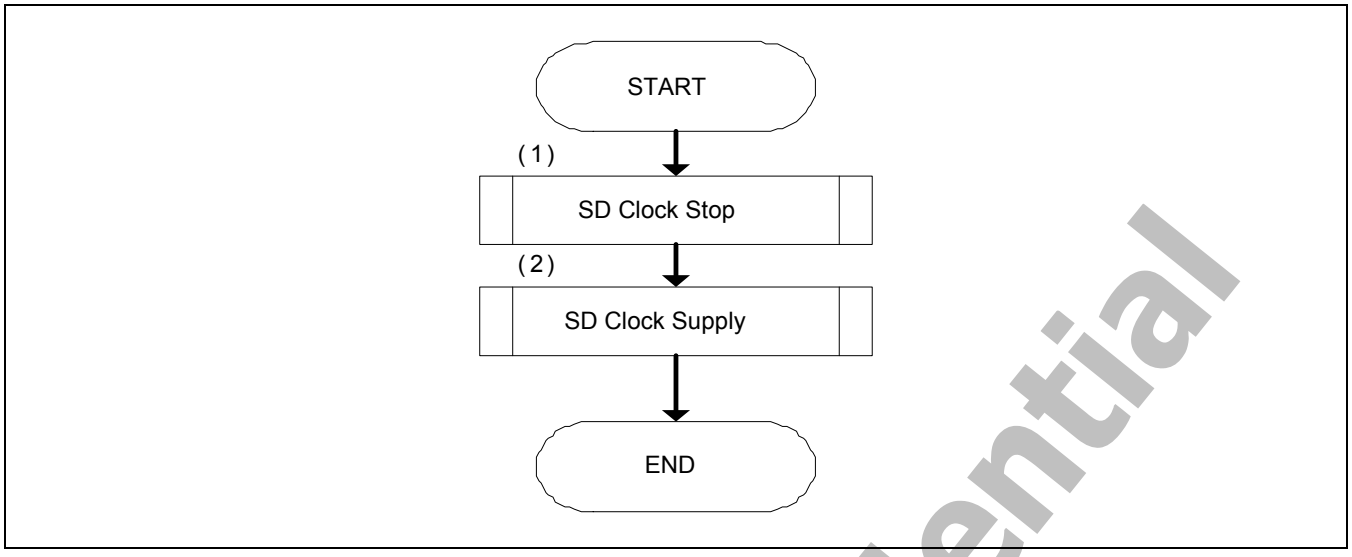

Figure 7-5 SD Clock Frequency Change Sequence

The sequence to change SD Clock frequency is shown in *Figure 7-5*. If SD Clock is still off, skip step (1).

The steps to change SD Clock frequency:

1. Perform SD Clock Stop Sequence. Refer to *7.4.2 SD Clock Supply Sequence.*
2. Perform SD Clock Supply Sequence. Refer to *7.4.3 SD Clock Stop Sequence*.

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7.4.5 SD BUS POWER CONTROL SEQUENCE

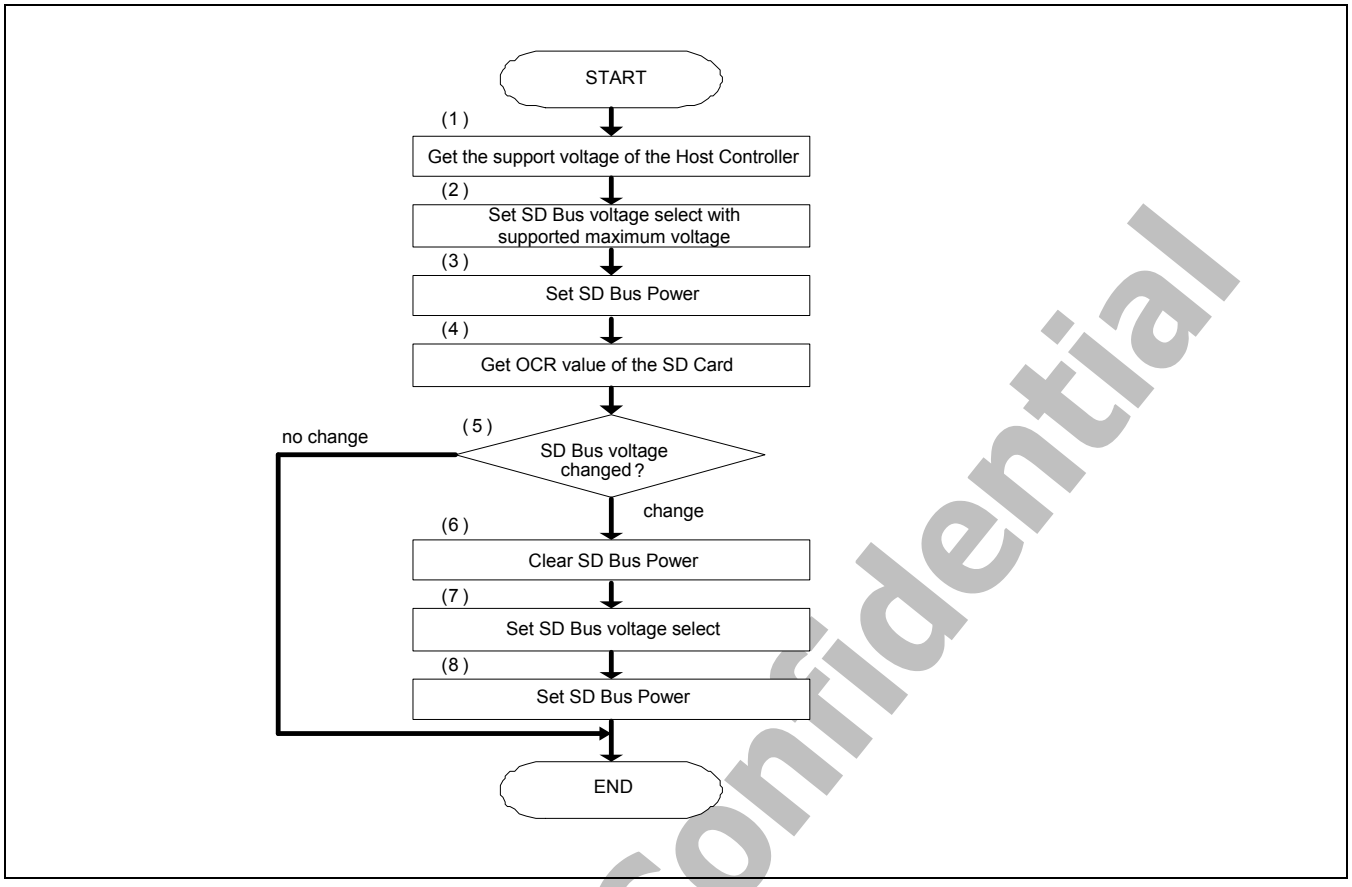

Figure 7-6 SD Bus Power Control Sequence

The sequence to control SD Bus Power is shown in *Figure 7-6*. Steps to control SD Bus Power:

1. To get the support voltage of the Host Controller, read the Capabilities register.
2. Set SD Bus Voltage Select in external power regulator (optional) with maximum voltage that the Host Controller supports.
3. Set SD Bus Power (PWRON) in the Power Control register to 1.
4. Get the OCR value of all function internal of SD card.
5. Judge whether SD Bus voltage must be changed or not. If SD Bus voltage must be changed, continue with step (6). If SD Bus voltage is not to be changed, go to 'End'.
6. Set SD Bus Power in the Power Control register to 0 for clearing this bit. The card requires voltage rising from 0 volt to detect it correctly. The Host Driver sets SD Bus Voltage Select to clear SD Bus Power before changing voltage.
7. Set SD Bus Voltage Select (SELPWRLVL) in the Power Control register.
8. Set SD Bus Power (PWRON) in the Power Control register to 1.

NOTE: Step (2) and step (3) can be executed at same time. Also, step (7) and step (8) can be executed at same time.

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7.4.6 CHANGE BUS WIDTH SEQUENCE

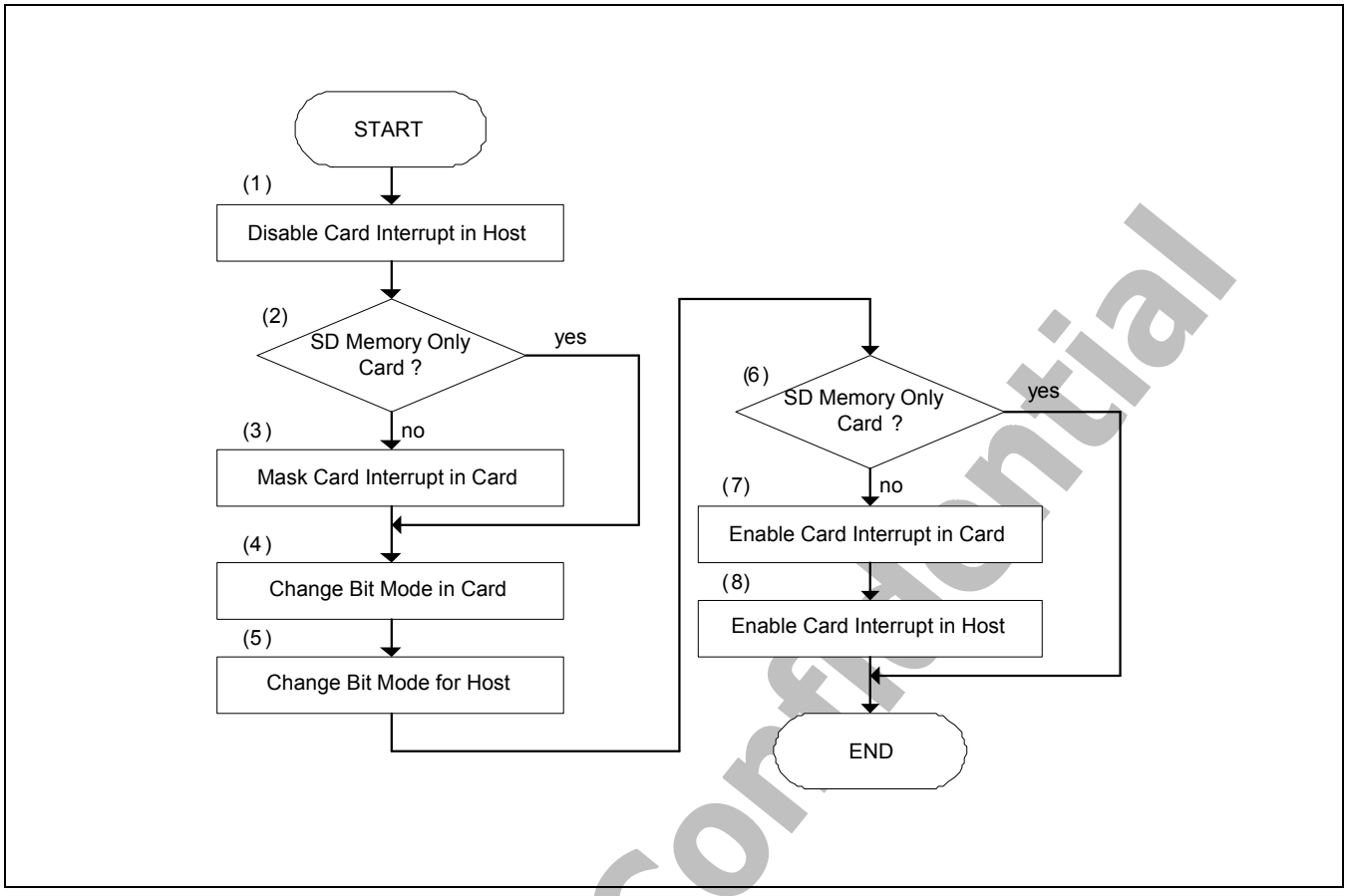

Figure 7-7 Change Bus Width Sequence

The sequence to change bit mode on SD Bus is shown in *Figure 7-7* . Steps to change bit mode on SD Bus:

1. To mask incorrect interrupts that may occur while changing the bus width, Set Card Interrupt Status Enable (STACARDINT) in the Normal Interrupt Status Enable register to 0.
2. If SD memory card is used, go to step (4). In case of other card, go to step (3).
3. Use CMD52 to set "IENM" of the CCCR in a SDIO or SD combo card to 0.
4. Change the bit mode for a SD card. To change SD memory card bus width by ACMD6 (Set bus width) and SDIO card bus width set Bus Width of Bus Interface Control register in CCCR.
5. If you want to change to 4-bit mode, set Data Transfer Width (WIDE4) to 1 in the Host Control register. In another case (1-bit mode), set this bit to 0.
6. If SD memory card is used, go to 'End'. In case of other card, go to step (7).
7. Set "IENM" of the CCCR in a SDIO or SD combo card to 1 by CMD52.
8. Set Card Interrupt Status Enable to 1 in the Normal Interrupt Status Enable register.

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7.4.7 TIMEOUT SETTING FOR DAT LINE

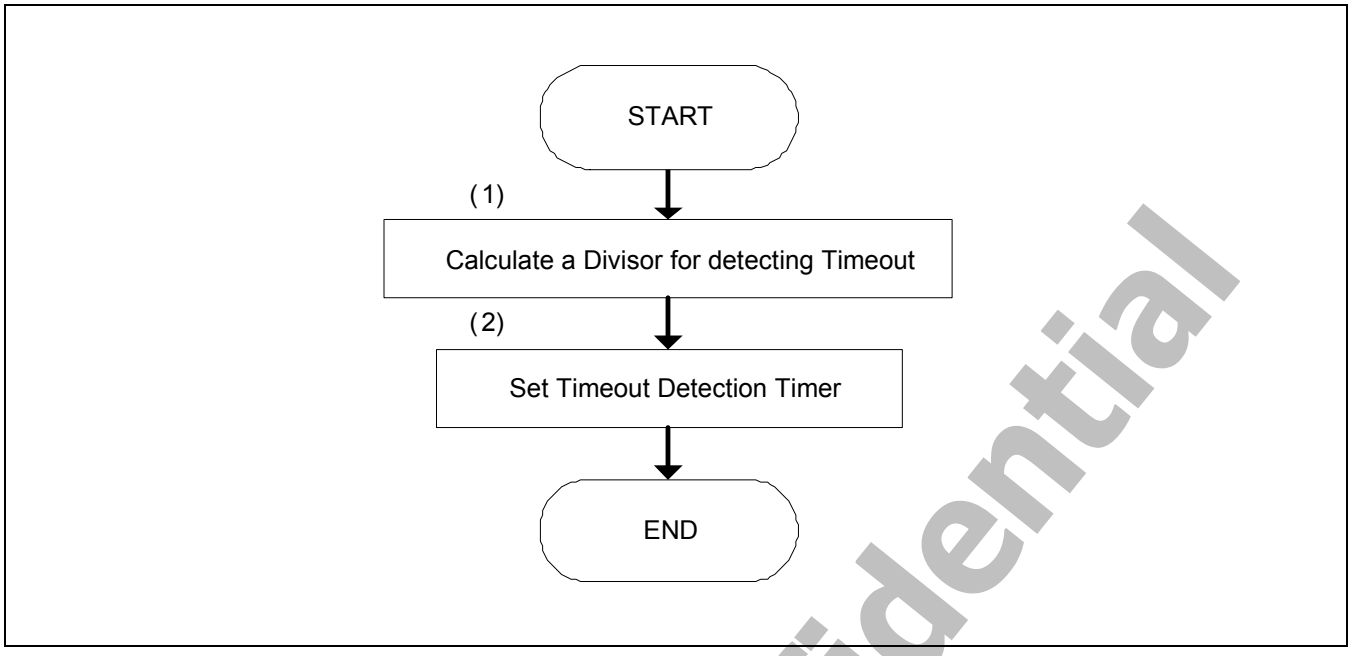

Figure 7-8 Timeout Setting Sequence

In order to detect timeout errors on DAT line, the Host Driver executes the following two steps before any SD transaction.

1. To calculate a divisor for detecting timeout, refer to Timeout Control Register (9.16).
2. (Set Data Timeout Counter Value (TIMEOUTCON) in the Timeout Control register in accordance with the value of step (1).

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7.4.8 SD TRANSACTION GENERATION

This section describes the sequence to generate and control various kinds of SD transactions. SD transactions are classified into three cases, namely:

1. Transactions that do not use the DAT line.
2. Transactions that use the DAT line for the busy signal.
3. Transactions that use the DAT line for transferring data.

In this specification the first and the second case's transactions are classified as "Transaction Control without Data Transfer using DAT Line", the third case's transaction is classified as "Transaction Control with Data Transfer using DAT Line".

Refer to the specifications below for the detailed specifications on the SD Command itself:

- SD Memory Card Specification Part 1
  PHYSICAL LAYER SPECIFICATION Version 1.01
- SD Card Specification PART E1
  Secure Digital Input/Output (SDIO) Specification Version 1.00

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7.4.9 SD COMMAND ISSUE SEQUENCE

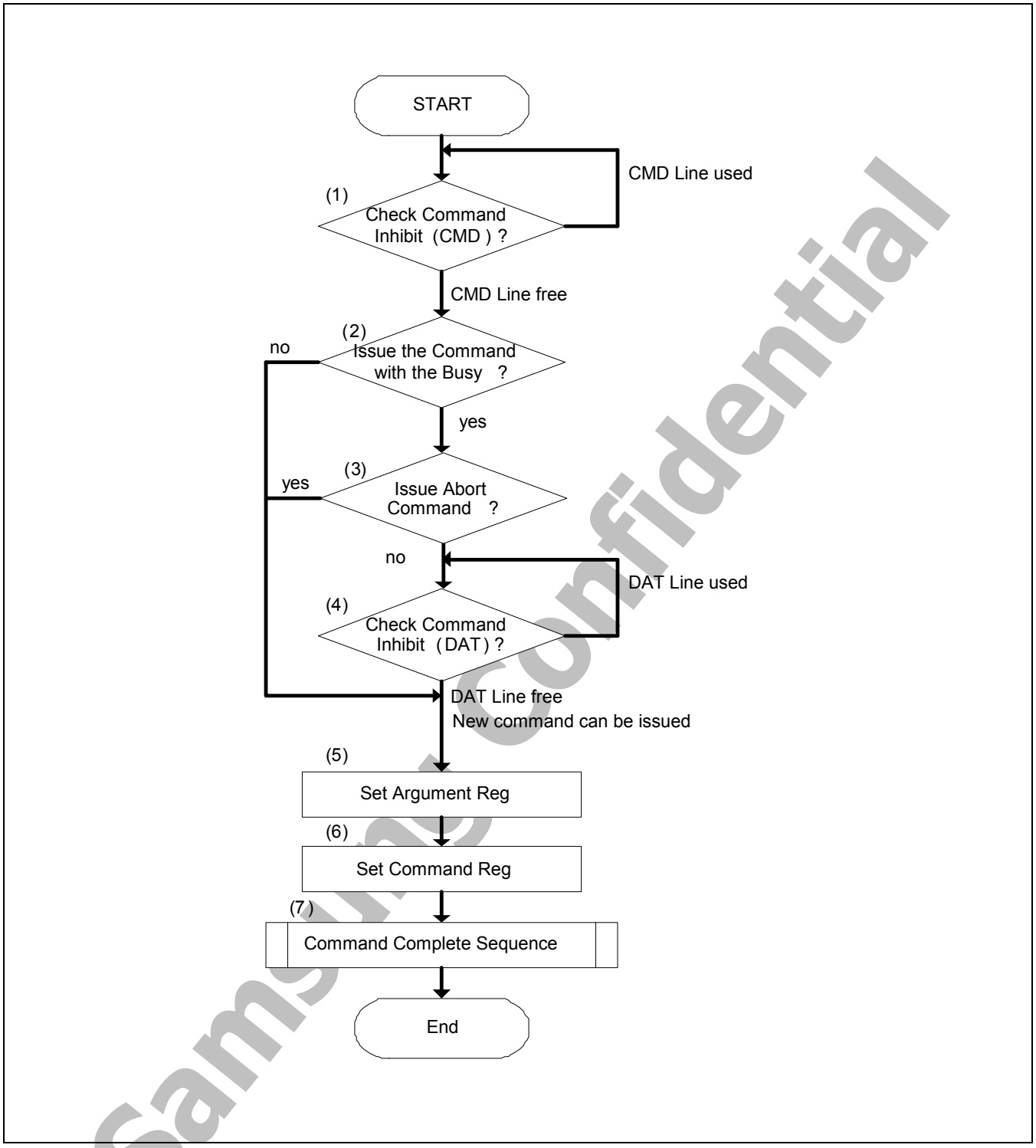

Figure 7-9 Timeout Setting Sequence

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Steps to set Timeout:

1. Check Command Inhibit (CMD) in the Present State register. Repeat this step until Command Inhibit (CMD) is 0. If Command Inhibit (CMD) is 1, the Host Driver does not issue a SD Command.
2. If the Host Driver issues a SD Command with busy signal, go to step (3). If without busy signal, go to step (5).
3. If the Host Driver issues an abort command, go to step (5). If no abort command is issued, go to step (4).
4. Check Command Inhibit (DAT) in the Present State register. Repeat this step until Command Inhibit (DAT) is 0.
5. Set the value corresponding to the issued command in the Argument register.
6. Set the value corresponding to the issued command in the Command register.

NOTE: If the upper byte is written in the Command register, it issues a SD command.

7. Perform Command Complete Sequence

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7.4.10 COMMAND COMPLETE SEQUENCE

The sequence to complete the SD Command is shown in *Figure 7-7*, *Figure 7-8*, *Figure 7-9* and *Figure 7-10*. The following errors can occur during this sequence: Command Index/ End bit/ CRC/ Timeout Error.

Steps to complete the SD command:

1. Wait for the Command Complete Interrupt. If the Command Complete Interrupt occurs, go to step (2).
2. Write 1 to Command Complete (STACMDCMPLT) in the Normal Interrupt Status register to clear this bit.
3. Read the Response register and get necessary information in accordance with the issued command.
4. Judge whether the command uses the Transfer Complete Interrupt or not. If it uses Transfer Complete, proceed with step (5). If not, go to step (7).
5. Wait for the Transfer Complete Interrupt. If the Transfer Complete Interrupt occurs, go to step (6).
6. Write 1 to Transfer Complete (STATRANCMPLT) in the Normal Interrupt Status register to clear this bit.
7. Check for errors in Response Data. If there is no error, proceed with step (8). If there is an error, go to step (9).
8. Return Status of "No Error".
9. Return Status of "Response Contents Error".

NOTE:

1. While waiting for the Transfer Complete interrupt, the Host Driver issues commands that do not use the busy signal.
2. The Host Driver monitors Transfer Complete to judge the Auto CMD12 (Stop Command) complete.
3. If the last block of un-protected area is read using memory multiple blocks read command (CMD18), OUT_OF_RANGE error may occur even if the sequence is correct. The Host Driver must ignore this error. This error appears in the response of Auto CMD12 or in the response of the next memory command.

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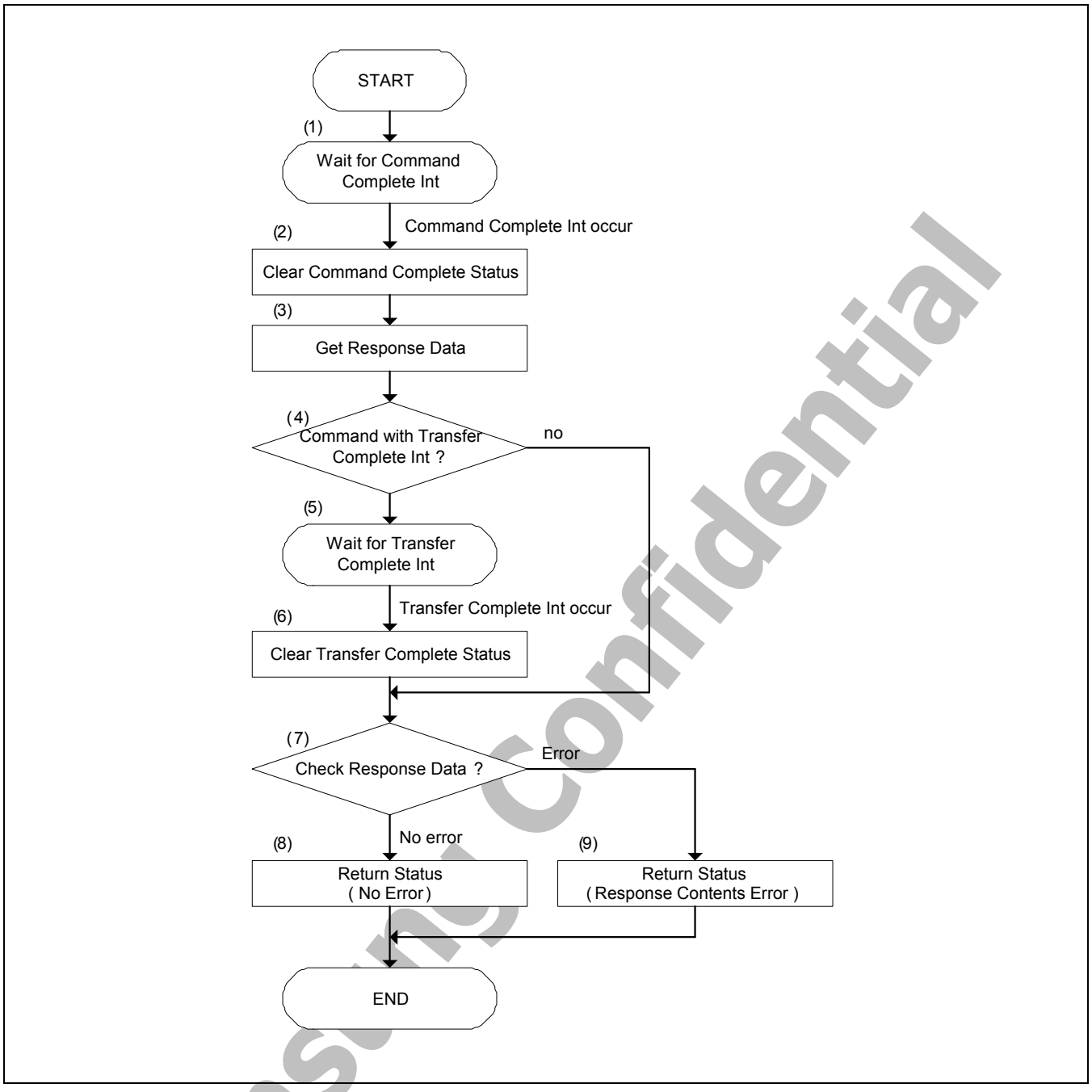

Figure 7-10 Command Complete Sequence

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7.4.11 TRANSACTION CONTROL WITH DATA TRANSFER USING DAT LINE

Depending on whether DMA (optional) is used or not, there are two execution methods. The sequence without using DMA is shown in *Figure 7-11* and the sequence using DMA is shown in *Figure 7-12*.

In addition, the sequences for SD transfers are basically classified according to how the number of blocks is specified. The three kinds of classification are as follows:

1. Single Block Transfer:
   The number of blocks is specified to the Host Controller before the transfer. The number of blocks specified is always one.

2. Multiple Block Transfer:
   The number of blocks is specified to the Host Controller before the transfer. The number of blocks specified is one or more.

3. Infinite Block Transfer:
   The number of blocks is not specified to the Host Controller before the transfer. This transfer is continued until an abort transaction is executed. This abort transaction is performed by CMD12 (Stop Command) in the case of a SD memory card and by CMD52 (IO_RW_DIRECT) in the case of a SDIO card.

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7.4.12 SEQUENCE WITHOUT USING DMA

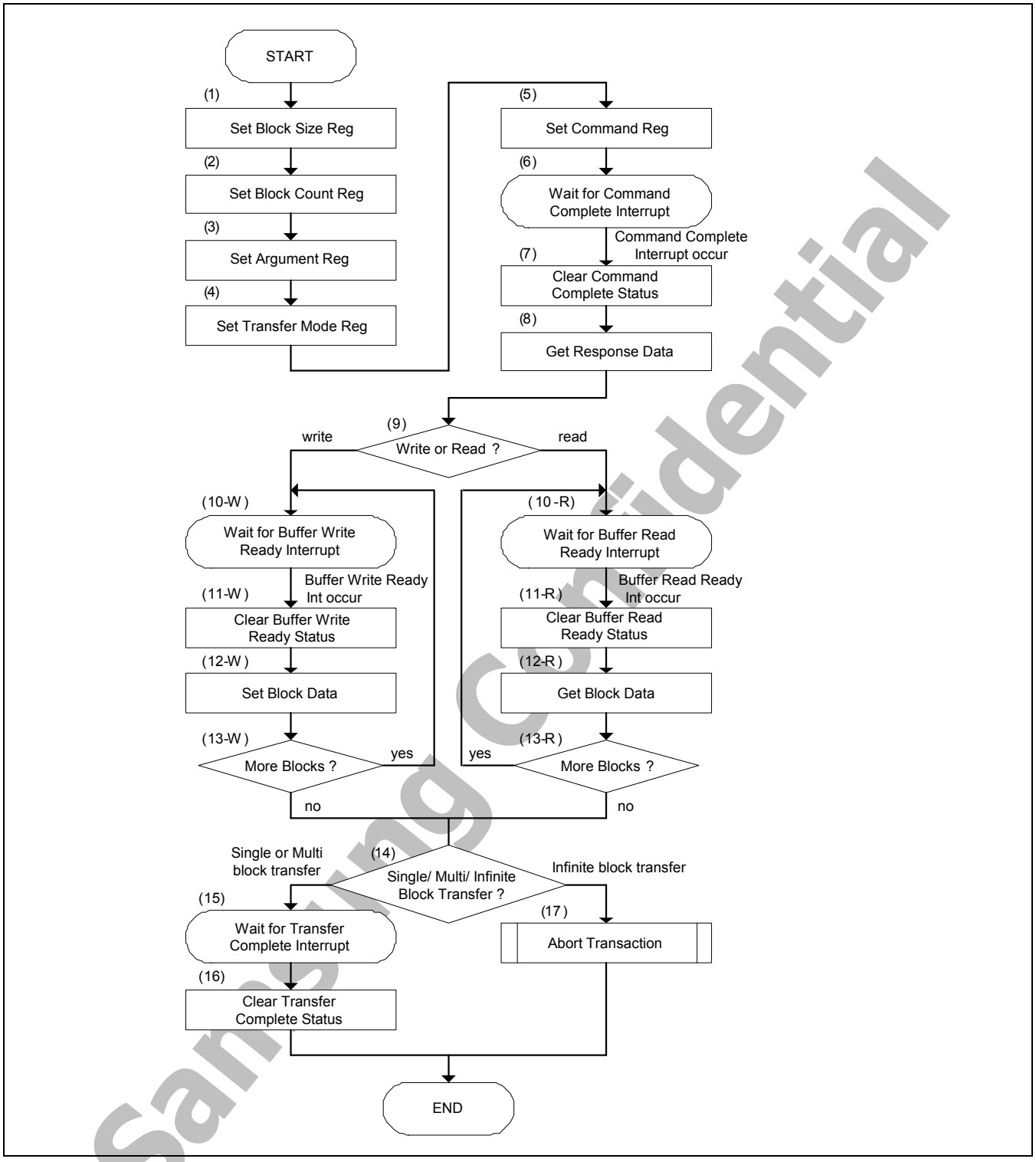

Figure 7-11 Transaction Control with Data Transfer Using DAT Line Sequence (Not using DMA)

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1. Set the value corresponding to the executed data byte length of one block to Block Size register.
2. Set the value corresponding to the executed data block count to Block Count register.
3. Set the value corresponding to the issued command to Argument register.
4. Set the value to Multi / Single Block Select and Block Count Enable. At this time, set the value corresponding to the issued command to Data Transfer Direction, Auto CMD12 Enable and DMA Enable.
5. Set the value corresponding to the issued command to Command register.

NOTE: If the upper byte is written in the Command register, it issues a SD command

6. Wait for the Command Complete Interrupt.
7. Write 1 to the Command Complete (STACMDCMPLT) in the Normal Interrupt Status register to clear this bit.
8. Read Response register and get necessary information in accordance with the issued command.
9. If this sequence is for write to a card, proceed to step (10-W). If read from a card, go to step (10-R).
10. (10-W) Wait for Buffer Write Ready Interrupt.
11. (11-W) Write 1 to the Buffer Write Ready (STABUFWTRDY) in the Normal Interrupt Status register to clear this bit.
12. (12-W) Write block data (in according to the number of bytes specified at the step (1)) to Buffer Data Port register.
13. (13-W) Repeat until all blocks are sent and then go to step (14).
14. (10-R) Wait for the Buffer Read Ready Interrupt.
15. (11-R) Write 1 to the Buffer Read Ready (STABUFRDRDY) in the Normal Interrupt Status register to clear this bit.
16. (12-R) Read block data (in according to the number of bytes specified at the step (1)) from the Buffer Data Port register.
17. (13-R) Repeat until all blocks are received and proceed to step (14).
18. (14) If this sequence is for Single or Multiple Block Transfer, proceed to step (15). In case of Infinite Block Transfer, go to step (17).
19. (15) Wait for Transfer Complete Interrupt.
20. (16)Write 1 to the Transfer Complete (STATRANCMPLT) in the Normal Interrupt Status register to clear this bit.
21. (17)Perform the sequence for Abort Transaction.

NOTE: Step (1) and Step (2) can be executed at same time. Step (4) and Step (5) can be executed at same time

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7.4.13 SEQUENCE USING DMA

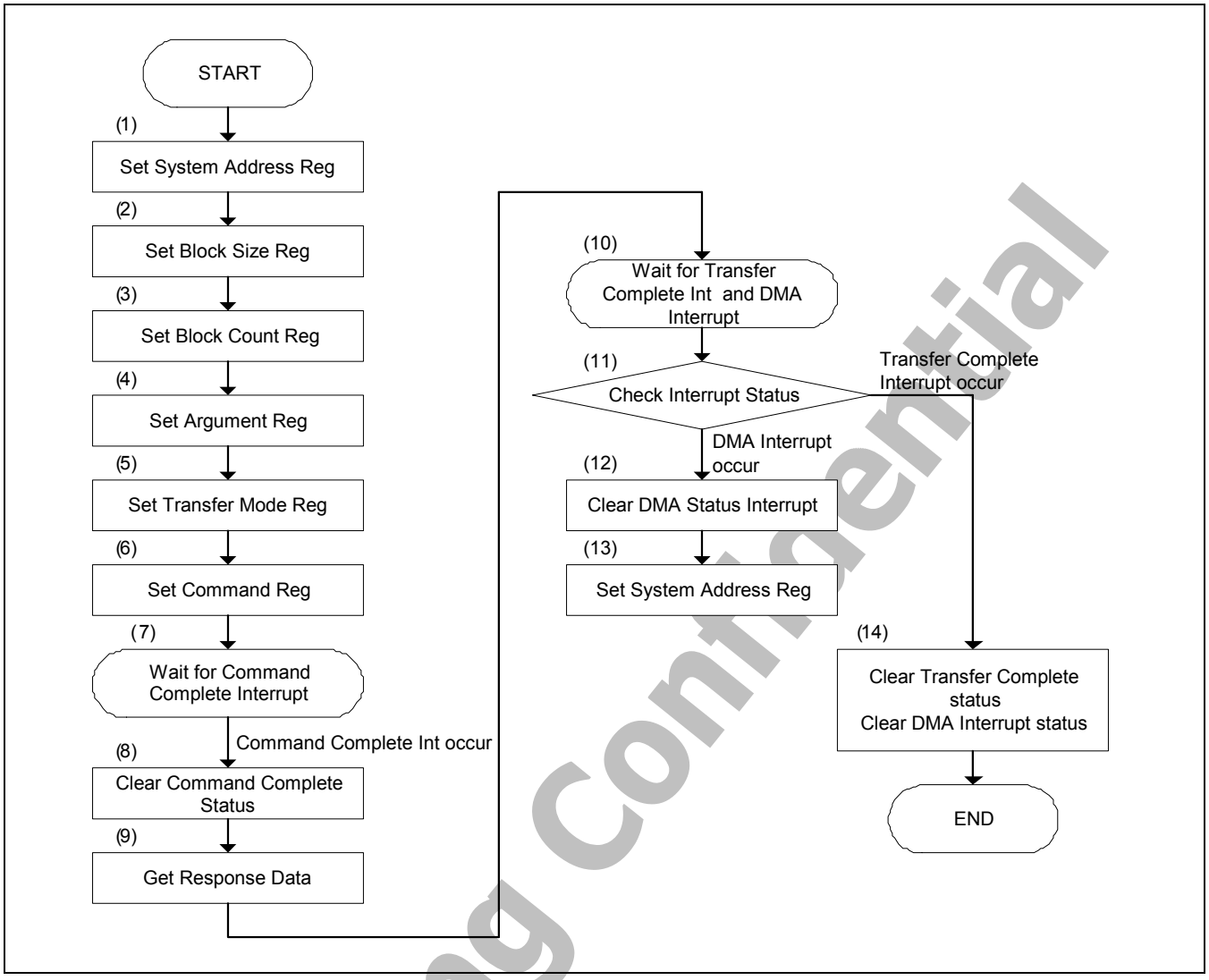

Figure 7-12 Transaction Control with Data Transfer Using DAT Line Sequence (Using DMA)

1. Set the system address for DMA in the System Address register.
2. Set the value corresponding to the executed data byte length of one block in the Block Size register.
3. Set the value corresponding to the executed data block count in the Block Count register (BLKCNT).
4. Set the value corresponding to the issued command in the Argument register (ARGUMENT).
5. Set the values for Multi / Single Block Select and Block Count Enable.

At this time, set the value corresponding to the issued command for Data Transfer Direction, Auto CMD12 Enable and DMA Enable.

6. Set the value corresponding to the issued command in the Command register (CMDREG).

NOTE: If the upper byte is written in the Command register, it issues a SD command and DMA is operated.

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7. Wait for the Command Complete Interrupt.
8. Write 1 to the Command Complete (STACMDCMPLT) in the Normal Interrupt Status register to clear this bit.
9. Read Response register and get necessary information in accordance with the issued command.
10. Wait for the Transfer Complete Interrupt and DMA Interrupt.
11. If Transfer Complete (STATRANCMPLT) is set 1, go to Step (14) else if DMA Interrupt is set to 1; proceed to Step (12). Transfer Complete is higher priority than DMA Interrupt.
12. Write 1 to the DMA Interrupt in the Normal Interrupt Status register to clear this bit.
13. Set the next system address of the next data position to the System Address register and go to Step (10).
14. Write 1 to the Transfer Complete and DMA Interrupt in the Normal Interrupt Status register to clear this bit.

NOTE: Step (2) and Step (3) can be executed simultaneously. Step (5) and Step (6) can also be executed simultaneously.

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7.5 ABORT TRANSACTION

To perform Abort transaction issue CMD12 (Stop Command) for a SD memory and issue CMD52 for a SDIO card. There are two cases where the Host Driver needs to issue an Abort Transaction. The first case is if the Host Driver stops Infinite Block Transfers. The second case is if the Host Driver stops transfers while a Multiple Block Transfer is executing.

There are two ways to issue an Abort Command, namely, asynchronous abort and synchronous abort.

In an asynchronous abort sequence, the Host Driver issues an Abort Command at anytime unless Command Inhibit (CMD) in the Present State register is set to 1.

In a synchronous abort, the Host Driver issues an Abort Command after the data transfer stopped by using Stop At Block Gap Request in the Block Gap Control register.

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7.6 DMA TRANSACTION

DMA allows a peripheral to read and write memory without intervention from the CPU. DMA executes one SD command transaction. Host Controllers that support DMA supports both single block and multiple block transfers.

The System Address register points to the first data address, and data is then accessed sequentially from that address. Host Controller registers remains accessible for issuing non-DAT line commands during a DMA transfer. The result of a DMA transfer is same regardless of the system bus transaction method. DMA does not support infinite transfers.

DMA transfers are stopped and restarted using control bits in the Block Gap Control register. If the Stop At Block Gap Request is set, DMA transfers is suspended. If the Continue Request is set or a Resume Command is issued, DMA continues to execute transfers. Refer to the Block Gap Control register for details. If SD Bus errors occur, SD Bus transfers and DMA transfers are stopped. Setting the Software Reset for DAT Line in the Software Reset register aborts DMA transfers.

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7.7 ADMA (ADVANCED DMA)

In the SD Host Controller Standard Specification Version 2.00, new DMA transfer algorithm called ADMA (Advanced DMA) is defined. The DMA algorithm defined in the SD Host Controller Standard Specification Version 1.00 is called SDMA (Single Operation DMA). SDMA had disadvantage that DMA Interrupt generated at every page boundary disturbs CPU to reprogram the new system address. This SDMA algorithm forms a performance bottleneck by interruption at every page boundary. ADMA adopts scatter gather DMA algorithm so that higher data transfer speed is available. The Host Driver can program a list of data transfers between system memory and SD card to the Descriptor Table before executing ADMA. It enables ADMA to operate without interrupting the Host Driver. Furthermore, ADMA can support not only 32-bit system memory addressing but also 64-bit system memory addressing. The 32-bit system memory addressing uses lower 32-bit field of 64-bit address registers. Support of SDMA and ADMA are optional for the Host Controller. ADMA improves the restriction so that data of any location and any size can be transferred in system memory. The format of Descriptor Table is different between them. The Host Controller Specification Ver2.00 defines ADMA as standard ADMA.

7.7.1 BLOCK DIAGRAM OF ADMA

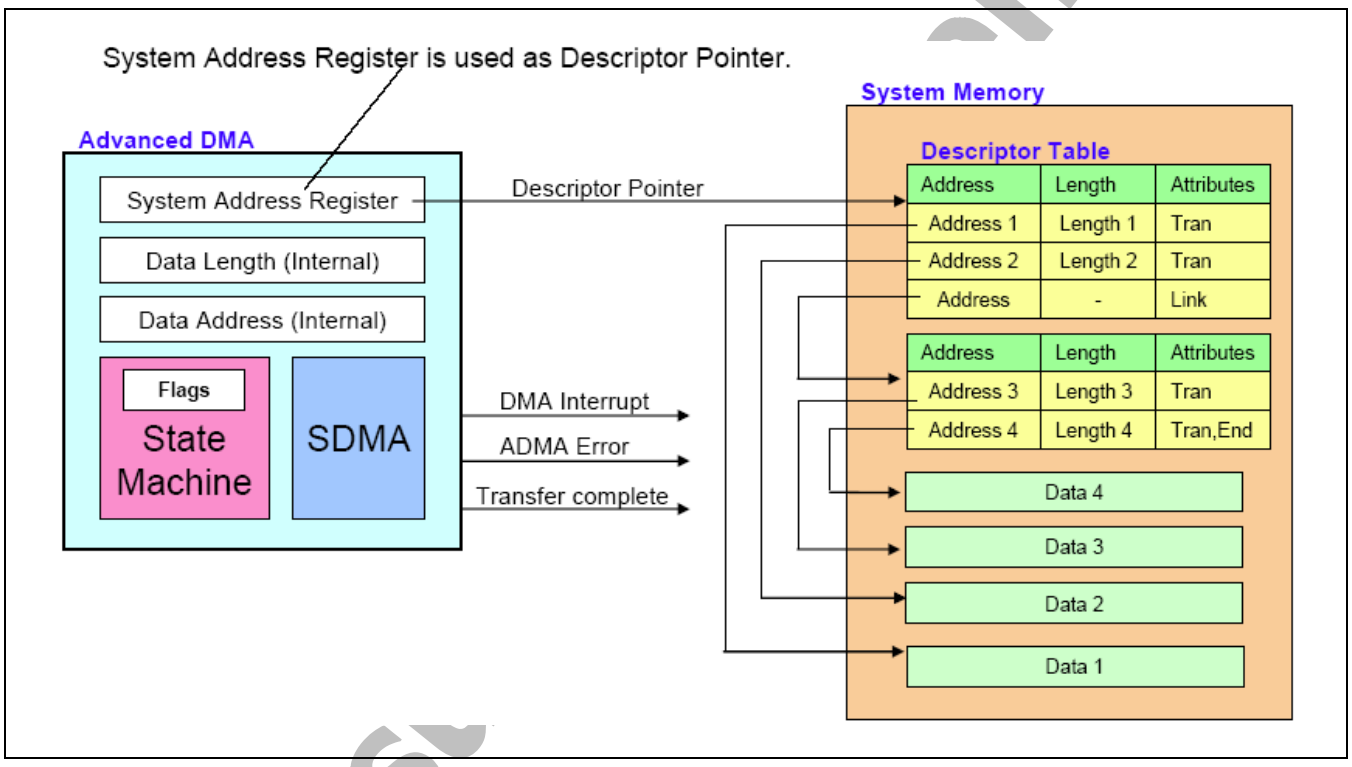

Figure 7-13 Block Diagram of ADMA

Figure 7-13 shows block diagram of ADMA. The Descriptor Table is created in system memory by the Host Driver. 32-bit Address Descriptor Table is used for the system with 32-bit addressing and 64-bit Address Descriptor Table is used for the system with 64-bit addressing. Each descriptor line (one executable unit) consists of address, length and attribute field. The attribute specifies operation of the descriptor line. ADMA includes SDMA, State Machine and Registers circuits. ADMA does not use 32-bit SDMA System Address Register (offset 0) but uses the 64-bit Advanced DMA System Address register (offset 058h) for descriptor pointer. Writing Command register triggers off ADMA transfer. ADMA fetches one descriptor line and execute. This procedure is repeated until end of descriptor is found (End=1 in attribute).

7.7.2 EXAMPLE OF ADMA PROGRAMMING

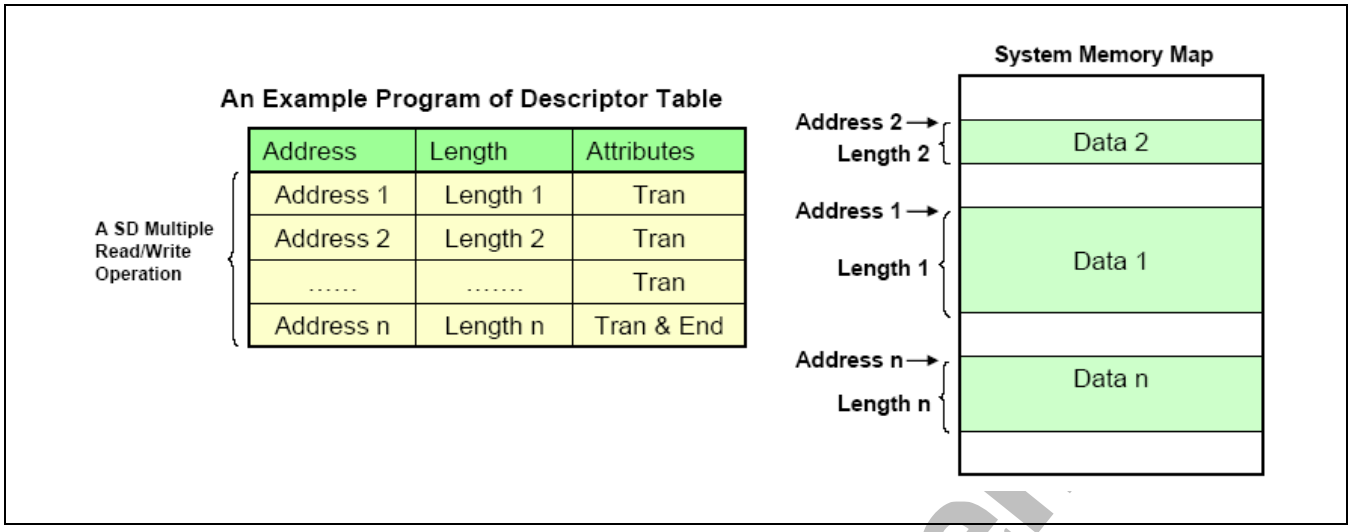

Figure 7-14 Example of ADMA Data Transfer

Figure 7-14 shows a typical ADMA descriptor program. The data area is sliced in various lengths and each slice is placed somewhere in system memory. The Host Driver describes the Descriptor Table with set of address, length and attributes. Each sliced data is transferred in turns as programmed in descriptor.

7.7.3 DATA ADDRESS AND DATA LENGTH REQUIREMENTS

There are 3 requirements to program descriptor. The minimum unit of address is 4byte.

The maximum data length of each descriptor line is less than 64KB.

Total Length = Length 1 + Length 2 + Length 3 + ... + Length n

= multiple of Block Size If total length of a descriptor were not multiple of block size, ADMA transfer might not be terminated. In this case, the transfer should be aborted by data timeout. Block Count register is defined as 16-bit register and it limits the maximum of 65535 blocks transfer. If ADMA operation is less than or equal 65535 blocks transfer, Block Count register can be used. In this case, total length of Descriptor Table shall be equivalent to multiply block size and block count. If ADMA operation is more than 65535 blocks transfer, Block Count register shall be disabled by setting 0 to Block Count Enable in the Transfer Mode Register. In this case, length of data transfer is not designated by block count but Descriptor Table. Therefore, the timing of detecting the last block on SD bus may be different and it affects the control of Read Transfer Active, Write Transfer Active and DAT line Active in the Present State register. In case of read operation, several blocks may be read more than required. The Host Driver shall ignore out of range error if the read operation is for the last block of memory area.

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7.7.4 DESCRIPTOR TABLE

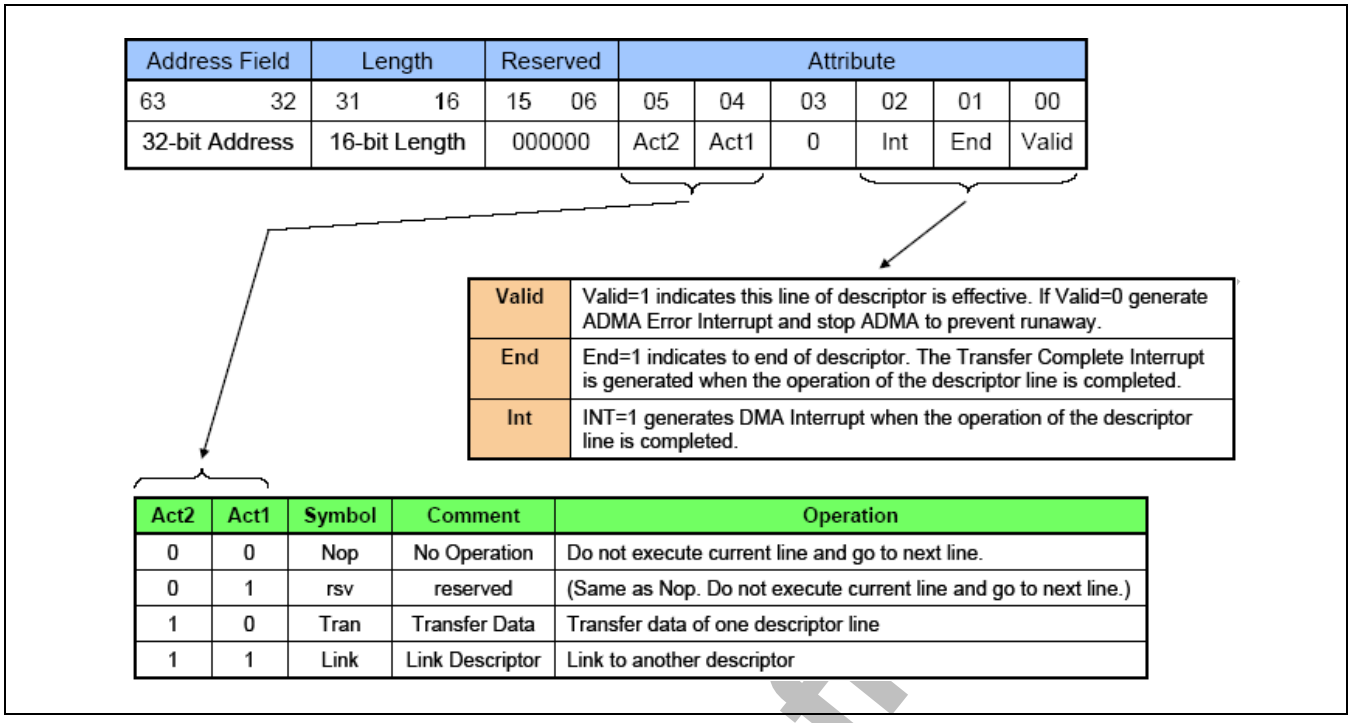

Figure 7-15 32-bit Address Descriptor Table

Figure 7-15 shows the definition of 32-bit Address Descriptor Table. One descriptor line consumes 64-bit (8-byte) memory space. Attribute is used to control descriptor. 3 action symbols are specified. "Nop" operation skips current descriptor line and fetches next one. "Tran" operation transfers data designated by address and length field. "Link" operation is used to connect separated two descriptors. The address field of link points to next Descriptor Table. The combination of Act2=0 and Act1=1 is reserved and defined the same operation as Nop. A future version of controller may use this field and redefine a new operation. 32-bit address is stored in the lower 32-bit of 64-bit address registers. Address field shall be set on 32-bit boundary (Lower 2-bit is always set to 0) for 32-bit address descriptor table. *Table 7-1* shows the definition of length field in the Descriptor Table.

Table 7-1 ADMA Length Field

Length Field	Value of Length
0000h	65536 bytes
0001h	1 byte
0002h	2 bytes
……	……
FFFFh	65535 bytes

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7.7.5 ADMA STATES

Figure 7-16 shows state diagram of ADMA. Four states are defined, namely, Fetch Descriptor state, Change Address state, Transfer Data state, and Stop ADMA state. Operation of each state is explained in *Table 7-2*.

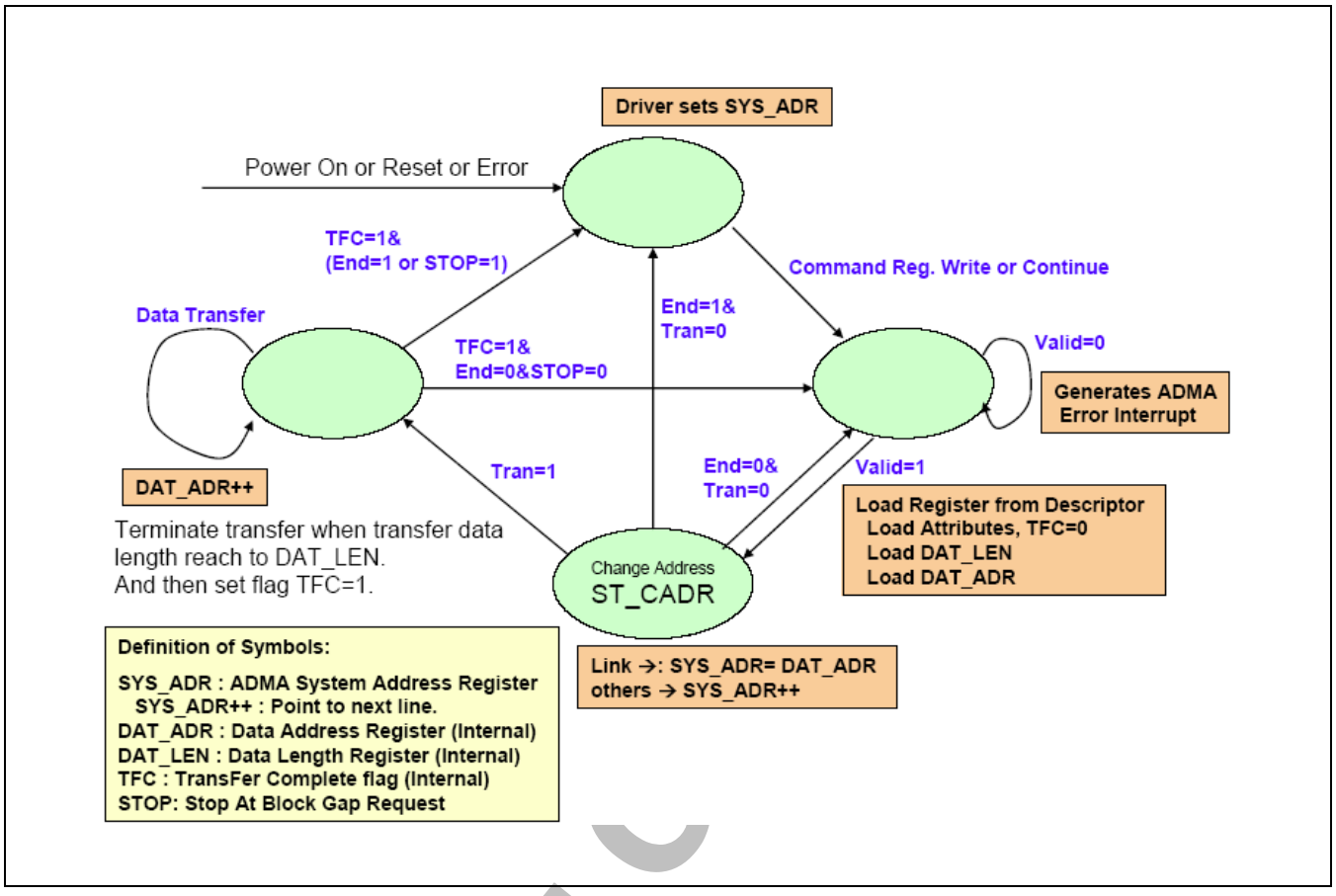

Figure 7-16 State Diagram of the ADMA

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Table 7-2 ADMA States

State Name	Operation
ST_FDS (Fetch Descriptor)	ADMA fetches a descriptor line and set parameters in internal registers. Next go to ST_CADR state.
ST_CADR (Change Address)	Link operation loads another Descriptor address to ADMA System Address register. In other operations, ADMA System Address register is incremented to point next descriptor line. If End=0, go to ST_TFR state. ADMA shall not be stopped at this state even if some errors occur.
ST_TFR (Transfer Data)	Data transfer of one descriptor line is executed between system memory and SD card. If data transfer continues (End=0) go to ST_FDS state. If data transfer completes, go to ST_STOP state.
ST_STOP (Stop DMA)	ADMA stays in this state in following cases: (1) After Power on reset or software reset. (2) All descriptor data transfers are completed If a new ADMA operation is started by writing Command register, go to ST_FDS state.

ADMA does not support suspend / resume function but stop and continue are available. When the Stop at Block Gap Request in the Block Gap Control register is set during the ADMA operation, the Block Gap Event Interrupt is generated when ADMA is stopped at block gap. The Host Controller shall stop ADMA read operation by using Read Wait or stopping SD Clock. While stopping ADMA, SD commands cannot be issued. (In case of Host Controller version 1.00, the Stop at Block Gap Request can be set only when the card supports the Read Wait.)

Error occurrence during ADMA transfer can stop ADMA operation and generates ADMA Error Interrupt. The ADMA Error State field in the ADMA Error Status register holds state of ADMA stopped. The host driver can identify error descriptor location by following method.

If ADMA stopped at ST_FDS state, the ADMA System Address Register points the error descriptor line. If ADMA stopped at ST_TFR or ST_STOP state, the ADMA System Address Register points the next location of error descriptor line. By this reason, ADMA2 shall not stop at ST_CADR state.

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7.8 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
SD_0_CLK	OUTPUT	Clock for SDMMC0	Xmmc0CLK	muxed
SD_0_CMD	IN/OUT	Command for SDMMC0	Xmmc0CMD	muxed
SD_0_DATA[0]	IN/OUT	Data for SDMMC0	Xmmc0DATA[0]	muxed
SD_0_DATA[1]	IN/OUT	Data for SDMMC0	Xmmc0DATA[1]	muxed
SD_0_DATA[2]	IN/OUT	Data for SDMMC0	Xmmc0DATA[2]	muxed
SD_0_DATA[3]	IN/OUT	Data for SDMMC0	Xmmc0DATA[3]	muxed
SD_0_DATA[4]	IN/OUT	Data for SDMMC0	Xmmc1DATA[0]	muxed
SD_0_DATA[5]	IN/OUT	Data for SDMMC0	Xmmc1DATA[1]	muxed
SD_0_DATA[6]	IN/OUT	Data for SDMMC0	Xmmc1DATA[2]	muxed
SD_0_DATA[7]	IN/OUT	Data for SDMMC0	Xmmc1DATA[3]	muxed
SD_0_CDn	INPUT	Card Detect for SDMMC0	Xmmc0CDn	muxed
SD_1_CLK	OUTPUT	Clock for SDMMC1	Xmmc1CLK	muxed
SD_1_CMD	IN/OUT	Command for SDMMC1	Xmmc1CMD	muxed
SD_1_DATA[0]	IN/OUT	Data for SDMMC1	Xmmc1DATA[0]	muxed
SD_1_DATA[1]	IN/OUT	Data for SDMMC1	Xmmc1DATA[1]	muxed
SD_1_DATA[2]	IN/OUT	Data for SDMMC1	Xmmc1DATA[2]	muxed
SD_1_DATA[3]	IN/OUT	Data for SDMMC1	Xmmc1DATA[3]	muxed
SD_1_CDn	INPUT	Card Detect for SDMMC1	Xmmc1CDn	muxed
SD_2_CLK	OUTPUT	Clock for SDMMC2	Xmmc2CLK	muxed
SD_2_CMD	IN/OUT	Command for SDMMC2	Xmmc2CMD	muxed
SD_2_DATA[0]	IN/OUT	Data for SDMMC2	Xmmc2DATA[0]	muxed
SD_2_DATA[1]	IN/OUT	Data for SDMMC2	Xmmc2DATA[1]	muxed
SD_2_DATA[2]	IN/OUT	Data for SDMMC2	Xmmc2DATA[2]	muxed
SD_2_DATA[3]	IN/OUT	Data for SDMMC2	Xmmc2DATA[3]	muxed
SD_2_DATA[4]	IN/OUT	Data for SDMMC2	Xmmc3DATA[0]	muxed
SD_2_DATA[5]	IN/OUT	Data for SDMMC2	Xmmc3DATA[1]	muxed
SD_2_DATA[6]	IN/OUT	Data for SDMMC2	Xmmc3DATA[2]	muxed
SD_2_DATA[7]	IN/OUT	Data for SDMMC2	Xmmc3DATA[3]	muxed
SD_2_CDn	INPUT	Card Detect for SDMMC2	Xmmc2CDn	muxed
SD_3_CLK	OUTPUT	Clock for SDMMC3	Xmmc3CLK	muxed
SD_3_CMD	IN/OUT	Command for SDMMC3	Xmmc3CMD	muxed
SD_3_DATA[0]	IN/OUT	Data for SDMMC3	Xmmc3DATA[0]	muxed
SD_3_DATA[1]	IN/OUT	Data for SDMMC3	Xmmc3DATA[1]	muxed
SD_3_DATA[2]	IN/OUT	Data for SDMMC3	Xmmc3DATA[2]	muxed
SD_3_DATA[3]	IN/OUT	Data for SDMMC3	Xmmc3DATA[3]	muxed

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Signal	I/O	Description	Pad	Type
SD_3_CDn	INPUT	Card Detect for SDMMC3	Xmmc3CDn	muxed

NOTE: SDMMC external pads are shared with CAMIF or SPI. In order to use these pads for SDMMC, set the GPIO before the SDMMC started. Refer to the GPIO chapter for correct GPIO settings.

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7.9 REGISTER DESCRIPTION

7.9.1 REGISTER MAP

Configuration register fields are assigned to one of the attributes described below:

Register	Address	R/W	Description	Reset Value
SDMASYSAD0	0xEB00_0000	R/W	SDMA System Address register (Channel 0)	0x0
BLKSIZE0	0xEB00_0004	R/W	Host DMA Buffer Boundary and Transfer Block Size Register (Channel 0)	0x0
BLKCNT0	0xEB00_0006	R/W	Blocks count for current transfer (channel 0)	0x0
ARGUMENT0	0xEB00_0008	R/W	Command Argument Register (Channel 0)	0x0
TRNMOD0	0xEB00_000C	R/W	Transfer Mode Setting Register (Channel 0)	0x0
CMDREG0	0xEB00_000E	R/W	Command Register (Channel 0)	0x0
RSPREG0_0	0xEB00_0010	ROC	Response Register 0 (Channel 0)	0x0
RSPREG1_0	0xEB00_0014	ROC	Response Register 1 (Channel 0)	0x0
RSPREG2_0	0xEB00_0018	ROC	Response Register 2 (Channel 0)	0x0
RSPREG3_0	0xEB00_001C	ROC	Response Register 3 (Channel 0)	0x0
BDATA0	0xEB00_0020	R/W	Buffer Data Register (Channel 0)	0x0
PRNSTS0	0xEB00_0024	R/ROC	Present State Register (Channel 0)	0x000A0000
HOSTCTL0	0xEB00_0028	R/W	Present State Register (Channel 0)	0x0
PWRCON0	0xEB00_0029	R/W	Present State Register (Channel 0)	0x0
BLKGAP0	0xEB00_002A	R/W	Block Gap Control Register (Channel 0)	0x0
WAKCON0	0xEB00_002B	R/W	Wakeup Control Register (Channel 0)	0x0
CLKCON0	0xEB00_002C	R/W	Command Register (Channel 0)	0x0
TIMEOUTCON0	0xEB00_002E	R/W	Timeout Control Register (Channel 0)	0x0
SWRST0	0xEB00_002F	R/W	Software Reset Register (Channel 0)	0x0
NORINTSTS0	0xEB00_0030	ROC/ RW1C	Normal Interrupt Status Register (Channel 0)	0x0
ERRINTSTS0	0xEB00_0032	ROC/ RW1C	Error Interrupt Status Register (Channel 0)	0x0
NORINTSTSEN0	0xEB00_0034	R/W	Normal Interrupt Status Enable Register (Channel 0)	0x0
ERRINTSTSEN0	0xEB00_0036	R/W	Error Interrupt Status Enable Register (Channel 0)	0x0
NORINTSIGEN0	0xEB00_0038	R/W	Normal Interrupt Signal Enable Register (Channel 0)	0x0
ERRINTSIGEN0	0xEB00_003A	R/W	Error Interrupt Signal Enable Register (Channel 0)	0x0
ACMD12ERRSTS0	0xEB00_003C	ROC	Auto CMD12 error status register (channel 0)	0x0
CAPAREG0	0xEB00_0040	HWInit	Capabilities Register (Channel 0)	0x05E80080
MAXCURR0	0xEB00_0048	HWInit	Maximum Current Capabilities Register	0x0

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Register	Address	R/W	Description	Reset Value
			(Channel 0)	
FEAER0	0xEB00_0050	W	Force Event Auto CMD12 Error Interrupt Register (Channel 0)	0x0000
FEERR0	0xEB00_0052	W	Force Event Error Interrupt Register Error Interrupt (Channel 0)	0x0000
ADMAERR0	0xEB00_0054	R/W	ADMA Error Status Register (Channel 0)	0x00
ADMASYSADDR0	0xEB00_0058	R/W	ADMA System Address Register (Channel 0)	0x00
CONTROL2_0	0xEB00_0080	R/W	Control register 2 (Channel 0)	0x0
CONTROL3_0	0xEB00_0084	R/W	FIFO Interrupt Control (Control Register 3) (Channel 0)	0x7F5F3F1F
CONTROL4_0	0xEB00_008C	R/W	Control register 4 (Channel 0)	0x0
HCVER0	0xEB00_00FE	HWInit	Host Controller Version Register (Channel 0)	0x2401
SDMASYSAD1	0xEB10_0000	R/W	SDMA System Address register (Channel 1)	0x0
BLKSIZE1	0xEB10_0004	R/W	Host DMA Buffer Boundary and Transfer Block Size Register (Channel 1)	0x0
BLKCNT1	0xEB10_0006	R/W	Blocks count for current transfer (channel 1)	0x0
ARGUMENT1	0xEB10_0008	R/W	Command Argument Register (Channel 1)	0x0
TRNMOD1	0xEB10_000C	R/W	Transfer Mode Setting Register (Channel 1)	0x0
CMDREG1	0xEB10_000E	R/W	Command Register (Channel 1)	0x0
RSPREG0_1	0xEB10_0010	ROC	Response Register 0 (Channel 1)	0x0
RSPREG1_1	0xEB10_0014	ROC	Response Register 1 (Channel 1)	0x0
RSPREG2_1	0xEB10_0018	ROC	Response Register 2 (Channel 1)	0x0
RSPREG3_1	0xEB10_001C	ROC	Response Register 3 (Channel 1)	0x0
BDATA1	0xEB10_0020	R/W	Buffer Data Register (Channel 1)	0x0
PRNSTS1	0xEB10_0024	R/ROC	Present State Register (Channel 1)	0x000A0000
HOSTCTL1	0xEB10_0028	R/W	Present State Register (Channel 1)	0x0
PWRCON1	0xEB10_0029	R/W	Present State Register (Channel 1)	0x0
BLKGAP1	0xEB10_002A	R/W	Block Gap Control Register (Channel 1)	0x0
WAKCON1	0xEB10_002B	R/W	Wakeup Control Register (Channel 1)	0x0
CLKCON1	0xEB10_002C	R/W	Command Register (Channel 1)	0x0
TIMEOUTCON1	0xEB10_002E	R/W	Timeout Control Register (Channel 1)	0x0
SWRST1	0xEB10_002F	R/W	Software Reset Register (Channel 1)	0x0
NORINTSTS1	0xEB10_0030	ROC/ RW1C	Normal Interrupt Status Register (Channel 1)	0x0
ERRINTSTS1	0xEB10_0032	ROC/ RW1C	Error Interrupt Status Register (Channel 1)	0x0
NORINTSTSEN1	0xEB10_0034	R/W	Normal Interrupt Status Enable Register (Channel 1)	0x0
ERRINTSTSEN1	0xEB10_0036	R/W	Error Interrupt Status Enable Register (Channel 1)	0x0

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Register	Address	R/W	Description	Reset Value
NORINTSIGEN1	0xEB10_0038	R/W	Normal Interrupt Signal Enable Register (Channel 1)	0x0
ERRINTSIGEN1	0xEB10_003A	R/W	Error Interrupt Signal Enable Register (Channel 1)	0x0
ACMD12ERRSTS1	0xEB10_003C	ROC	Auto CMD12 error status register (channel 1)	0x0
CAPAREG1	0xEB10_0040	HWInit	Capabilities Register (Channel 1)	0x05E80080
MAXCURR1	0xEB10_0048	HWInit	Maximum Current Capabilities Register (Channel 1)	0x0
FEAER1	0xEB10_0050	W	Force Event Auto CMD12 Error Interrupt Register (Channel 1)	0x0000
FEERR1	0xEB10_0052	W	Force Event Error Interrupt Register Error Interrupt (Channel 1)	0x0000
ADMAERR1	0xEB10_0054	R/W	ADMA Error Status Register (Channel 1)	0x00
ADMASYSADDR1	0xEB10_0058	R/W	ADMA System Address Register (Channel 1)	0x00
CONTROL2_1	0xEB10_0080	R/W	Control register 2 (Channel 1)	0x0
CONTROL3_1	0xEB10_0084	R/W	FIFO Interrupt Control (Control Register 3) (Channel 1)	0x7F5F3F1F
CONTROL4_1	0xEB10_008C	R/W	Control register 4 (Channel 1)	0x0
HCVER1	0xEB10_00FE	HWInit	Host Controller Version Register (Channel 1)	0x2401
SDMASYSAD2	0xEB20_0000	R/W	SDMA System Address register (Channel 2)	0x0
BLKSIZE2	0xEB20_0004	R/W	Host DMA Buffer Boundary and Transfer Block Size Register (Channel 2)	0x0
BLKCNT2	0xEB20_0006	R/W	Blocks count for current transfer (channel 2)	0x0
ARGUMENT2	0xEB20_0008	R/W	Command Argument Register (Channel 2)	0x0
TRNMOD2	0xEB20_000C	R/W	Transfer Mode Setting Register (Channel 2)	0x0
CMDREG2	0xEB20_000E	R/W	Command Register (Channel 2)	0x0
RSPREG0_2	0xEB20_0010	ROC	Response Register 0 (Channel 2)	0x0
RSPREG1_2	0xEB20_0014	ROC	Response Register 1 (Channel 2)	0x0
RSPREG2_2	0xEB20_0018	ROC	Response Register 2 (Channel 2)	0x0
RSPREG3_2	0xEB20_001C	ROC	Response Register 3 (Channel 2)	0x0
BDATA2	0xEB20_0020	R/W	Buffer Data Register (Channel 2)	0x0
PRNSTS2	0xEB20_0024	R/ROC	Present State Register (Channel 2)	0x000A0000
HOSTCTL2	0xEB20_0028	R/W	Present State Register (Channel 2)	0x0
PWRCON2	0xEB20_0029	R/W	Present State Register (Channel 2)	0x0
BLKGAP2	0xEB20_002A	R/W	Block Gap Control Register (Channel 2)	0x0
WAKCON2	0xEB20_002B	R/W	Wakeup Control Register (Channel 2)	0x0
CLKCON2	0xEB20_002C	R/W	Command Register (Channel 2)	0x0
TIMEOUTCON2	0xEB20_002E	R/W	Timeout Control Register (Channel 2)	0x0
SWRST2	0xEB20_002F	R/W	Software Reset Register (Channel 2)	0x0

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Register	Address	R/W	Description	Reset Value
NORINTSTS2	0xEB20_0030	ROC/ RW1C	Normal Interrupt Status Register (Channel 2)	0x0
ERRINTSTS2	0xEB20_0032	ROC/ RW1C	Error Interrupt Status Register (Channel 2)	0x0
NORINTSTSEN2	0xEB20_0034	R/W	Normal Interrupt Status Enable Register (Channel 2)	0x0
ERRINTSTSEN2	0xEB20_0036	R/W	Error Interrupt Status Enable Register (Channel 2)	0x0
NORINTSIGEN2	0xEB20_0038	R/W	Normal Interrupt Signal Enable Register (Channel 2)	0x0
ERRINTSIGEN2	0xEB20_003A	R/W	Error Interrupt Signal Enable Register (Channel 2)	0x0
ACMD12ERRSTS2	0xEB20_003C	ROC	Auto CMD12 error status register (channel 2)	0x0
CAPAREG2	0xEB20_0040	HWInit	Capabilities Register (Channel 2)	0x05E80080
MAXCURR2	0xEB20_0048	HWInit	Maximum Current Capabilities Register (Channel 2)	0x0
FEAER2	0xEB20_0050	W	Force Event Auto CMD12 Error Interrupt Register (Channel 2)	0x0000
FEERR2	0xEB20_0052	W	Force Event Error Interrupt Register Error Interrupt (Channel 2)	0x0000
ADMAERR2	0xEB20_0054	R/W	ADMA Error Status Register (Channel 2)	0x00
ADMASYSADDR2	0xEB20_0058	R/W	ADMA System Address Register (Channel 2)	0x00
CONTROL2_2	0xEB20_0080	R/W	Control register 2 (Channel 2)	0x0
CONTROL3_2	0xEB20_0084	R/W	FIFO Interrupt Control (Control Register 3) (Channel 2)	0x7F5F3F1F
CONTROL4_2	0xEB20_008C	R/W	Control register 4 (Channel 2)	0x0
HCVER2	0xEB20_00FE	HWInit	Host Controller Version Register (Channel 2)	0x2401
SDMASYSAD3	0xEB30_0000	R/W	SDMA System Address register (Channel 3)	0x0
BLKSIZE3	0xEB30_0004	R/W	Host DMA Buffer Boundary and Transfer Block Size Register (Channel 3)	0x0
BLKCNT3	0xEB30_0006	R/W	Blocks count for current transfer (channel 3)	0x0
ARGUMENT3	0xEB30_0008	R/W	Command Argument Register (Channel 3)	0x0
TRNMOD3	0xEB30_000C	R/W	Transfer Mode Setting Register (Channel 3)	0x0
CMDREG3	0xEB30_000E	R/W	Command Register (Channel 3)	0x0
RSPREG0_3	0xEB30_0010	ROC	Response Register 0 (Channel 3)	0x0
RSPREG1_3	0xEB30_0014	ROC	Response Register 1 (Channel 3)	0x0
RSPREG2_3	0xEB30_0018	ROC	Response Register 2 (Channel 3)	0x0
RSPREG3_3	0xEB30_001C	ROC	Response Register 3 (Channel 3)	0x0
BDATA3	0xEB30_0020	R/W	Buffer Data Register (Channel 3)	0x0
PRNSTS3	0xEB30_0024	R/ROC	Present State Register (Channel 3)	0x000A0000

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Register	Address	R/W	Description	Reset Value
HOSTCTL3	0xEB30_0028	R/W	Present State Register (Channel 3)	0x0
PWRCON3	0xEB30_0029	R/W	Present State Register (Channel 3)	0x0
BLKGAP3	0xEB30_002A	R/W	Block Gap Control Register (Channel 3)	0x0
WAKCON3	0xEB30_002B	R/W	Wakeup Control Register (Channel 3)	0x0
CLKCON3	0xEB30_002C	R/W	Command Register (Channel 3)	0x0
TIMEOUTCON3	0xEB30_002E	R/W	Timeout Control Register (Channel 3)	0x0
SWRST3	0xEB30_002F	R/W	Software Reset Register (Channel 3)	0x0
NORINTSTS3	0xEB30_0030	ROC/ RW1C	Normal Interrupt Status Register (Channel 3)	0x0
ERRINTSTS3	0xEB30_0032	ROC/ RW1C	Error Interrupt Status Register (Channel 3)	0x0
NORINTSTSEN3	0xEB30_0034	R/W	Normal Interrupt Status Enable Register (Channel 3)	0x0
ERRINTSTSEN3	0xEB30_0036	R/W	Error Interrupt Status Enable Register (Channel 3)	0x0
NORINTSIGEN3	0xEB30_0038	R/W	Normal Interrupt Signal Enable Register (Channel 3)	0x0
ERRINTSIGEN3	0xEB30_003A	R/W	Error Interrupt Signal Enable Register (Channel 3)	0x0
ACMD12ERRSTS3	0xEB30_003C	ROC	Auto CMD12 error status register (channel 3)	0x0
CAPAREG3	0xEB30_0040	HWInit	Capabilities Register (Channel 3)	0x05E80080
MAXCURR3	0xEB30_0048	HWInit	Maximum Current Capabilities Register (Channel 3)	0x0
FEAER3	0xEB30_0050	W	Force Event Auto CMD12 Error Interrupt Register (Channel 3)	0x0000
FEERR3	0xEB30_0052	W	Force Event Error Interrupt Register Error Interrupt (Channel 3)	0x0000
ADMAERR3	0xEB30_0054	R/W	ADMA Error Status Register (Channel 3)	0x00
ADMASYSADDR3	0xEB30_0058	R/W	ADMA System Address Register (Channel 3)	0x00
CONTROL2_3	0xEB30_0080	R/W	Control register 2 (Channel 3)	0x0
CONTROL3_3	0xEB30_0084	R/W	FIFO Interrupt Control (Control Register 3) (Channel 3)	0x7F5F3F1F
CONTROL4_3	0xEB30_008C	R/W	Control register 4 (Channel 3)	0x0
HCVER3	0xEB30_00FE	HWInit	Host Controller Version Register (Channel 3)	0x2401

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7.9.2 SDMA SYSTEM ADDRESS REGISTER

7.9.2.1 SDMA System Address Register

- SDMASYSAD0, R/W, Address = 0xEB00_0000
- SDMASYSAD1, R/W, Address = 0xEB10_0000
- SDMASYSAD2, R/W, Address = 0xEB20_0000
- SDMASYSAD3, R/W, Address = 0xEB30_0000

This register contains the physical system memory address used for DMA transfers.

SDMASYSAD	Bit	Description	Initial State
SDMASYSAD	[31:0]	SDMA System Address This register contains the system memory address for a DMA transfer. If the Host Controller stops a DMA transfer, this register points to the system address of the next contiguous data position. It is accessed if no transaction is in-progress (i.e., after a transaction has stopped). Read operations during transfers can return an invalid value. The Host Driver initializes this register before starting a DMA transaction. After DMA has stopped, the next system address of the next contiguous data position is read from this register. The DMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver set the next system address of the next data position to this register. If the most upper byte of this register (003h) is written, the Host Controller restarts the DMA transfer. If restarting DMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller starts at the next contiguous address stored here in the System Address register.	0x00

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7.9.3 BLOCK SIZE REGISTER

7.9.3.1 Host DMA Buffer Boundary and Transfer Block Size Register

- BLKSIZE0, R/W, Address = 0xEB00_0004
- BLKSIZE1, R/W, Address = 0xEB10_0004
- BLKSIZE2, R/W, Address = 0xEB20_0004
- BLKSIZE3, R/W, Address = 0xEB30_0004

This register is used to configure the number of bytes in a data block.

BLKSIZE	Bit	Description	Initial State
-	[15]	Reserved	0
BUF BOUND	[14:12]	Host DMA Buffer Boundary The large contiguous memory space may not be available in the virtual memory system. To perform long SDMA transfer, System Address register is updated at every system memory boundary during SDMA transfer. These bits specify the size of contiguous buffer in the system memory. The SDMA transfer waits at the every boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the SDMA System Address register. At the end of transfer, the Host Controller issue or not issue DMA Interrupt. In particular, DMA Interrupt is not issued after Transfer Complete Interrupt is issued. If this register is set to 0 (buffer size = 4K bytes), lower 12-bit of byte address points data in the contiguous buffer and the upper 20-bit points the location of the buffer in the system memory. The DMA transfer stops if the Host Controller detects carry out of the address from bit 11 to 12. These bits are supported if the SDMA Support in the Capabilities register is set to 1 and this function is active if DMA Enable in the Transfer Mode register is set to 1. 000b = 4K bytes (Detects A11 carry out) 001b = 8K bytes (Detects A12 carry out) 010b = 16K Bytes (Detects A13 carry out) 011b = 32K Bytes (Detects A14 carry out) 100b = 64K bytes (Detects A15 carry out) 101b = 128K Bytes (Detects A16 carry out) 110b = 256K Bytes (Detects A17 carry out) 111b = 512K Bytes (Detects A18 carry out)	0
BLKSIZE	[11:0]	Transfer Block Size This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. Values ranging from 1 up to maximum buffer size are set. In case of memory, it is set up to 512 bytes. It is accessed only if no transaction is in-progress (i.e., after a transaction has stopped). Read operations during transfers return an invalid value, and write operations are ignored. 0200h = 512 Bytes , 01FFh = 511 Bytes …… 0004h = 4 Bytes , 0003h = 3 Bytes 0002h = 2 Bytes , 0001h = 1 Byte 0000h = No data transfer	0

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7.9.4 BLOCK COUNT REGISTER

7.9.4.1 Blocks Count for Current Transfer

- BLKCNT0, R/W, Address = 0xEB00_0006
- BLKCNT1, R/W, Address = 0xEB10_0006
- BLKCNT2, R/W, Address = 0xEB20_0006
- BLKCNT3, R/W, Address = 0xEB30_0006

This register is used to configure the number of data blocks.

BLKCNT	Bit	Description	Initial State
BLKCNT	[15:0]	Blocks Count For Current Transfer This register is enabled if Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers. The Host Driver sets this register to a value between 1 and the maximum block count. The Host Controller decrements the block count after each block transfer and stops if the count reaches zero. Setting the block count to 0 results in no data blocks being transferred. This register must be accessed if no transaction is in-progress (i.e., after transactions are stopped). During data transfer, read operations on this register returns an invalid value and write operations are ignored. If saving transfer context as a result of a Suspend command, the number of blocks yet to be transferred is determined by reading this register. If restoring transfer context prior to issuing a Resume command, the Host Driver restores the previously saved block count. FFFFh = 65535 blocks … … 0002h = 2 blocks 0001h = 1 block 0000h = Stop Count	0

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7.9.5 ARGUMENT REGISTER

7.9.5.1 Command Argument Register

- ARGUMENT0, R/W, Address = 0xEB00_0008
- ARGUMENT1, R/W, Address = 0xEB10_0008
- ARGUMENT2, R/W, Address = 0xEB20_0008
- ARGUMENT3, R/W, Address = 0xEB30_0008

This register contains the SD Command Argument.

ARGUMENT	Bit	Description	Initial State
ARGUMENT	[31:0]	Command Argument The SD Command Argument is specified as bit [39:8] of Command-Format in the SD Memory Card Physical Layer Specification.	0

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7.9.6 TRANSFER MODE REGISTER

7.9.6.1 Transfer Mode Register Setting

- TRNMOD0, R/W, Address = 0xEB00_000C
- TRNMOD1, R/W, Address = 0xEB10_000C
- TRNMOD2, R/W, Address = 0xEB20_000C
- TRNMOD3, R/W, Address = 0xEB30_000C

This register is used to control the data transfer operations. The Host Driver sets this register before issuing a command which transfers data (Refer to Data Present Select in the Command register (9.7)), or before issuing a Resume command. The Host Driver saves the value of this register if data transfer is suspended (as a result of a Suspend command) and restore it before issuing a Resume command. To prevent data loss, the Host Controller implements write protection for this register during data transactions. Writes to this register is ignored if the Command Inhibit (DAT) in Present State register is 1.

TRNMOD	Bit	Description	Initial State
Reserved	[15:14]	Reserved	0
BOOTACK	[13]	Boot ACK Receive Enable when Boot mode	0
BOOTCMD	[12]	Boot Command mode Enable Note: In boot mode, Do Not Enable “Auto CMD12 Enable”	0
Reserved	[11:10]	Reserved	0
CCSCON	[9:8]	Command Completion Signal Control '00' = No CCS Operation (Normal operation and No CE-ATA mode) '01' = Read or Write data transfer CCS enable (Only CE-ATA mode) '10' = Without data transfer CCS enable (Only CE-ATA mode) '11' = Abort Completion Signal (ACS) generation (Only CE-ATA mode)	0
Reserved	[7:6]	Reserved	0
MUL1SIN0	[5]	Multi/ Single Block Select This bit enables multiple block DAT line data transfers. For any other commands, this bit is set to 0. If this bit is 0, it is not mandatory to set the Block Count register. (Refer to the Table below "Determination of Transfer Type") 1 = Multiple Block 0 = Single Block	0
RD1WT0	[4]	Data Transfer Direction Select This bit defines the direction of DAT line data transfers. The bit is set to 1 by the Host Driver to transfer data from the SD card to the SD Host Controller and it is set to 0 for all other commands. 1 = Read (Card to Host) 0 = Write (Host to Card)	0
Reserved	[3]	Reserved	0

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TRNMOD	Bit	Description	Initial State
ENACMD12	[2]	Auto CMD12 Enable Multiple block transfers for memory require CMD12 to stop the transaction. If this bit is set to 1 and last block transfer is complete, the Host Controller issues CMD12 automatically. The Host Driver does not set this bit to issue commands that do not require CMD12 to stop data transfer. 1 = Enable 0 = Disable	0
ENBLKCNT	[1]	Block Count Enable This bit is used to enable the Block Count register, which is only relevant for multiple block transfers. If this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. (Refer to the Table below "Determination of Transfer Type") 1 = Enable 0 = Disable	0
ENDMA	[0]	DMA Enable This bit enables DMA functionality. DMA is enabled if it is supported as indicated in the DMA Support in the Capabilities register. If DMA is not supported, this bit is meaningless and always read 0. If this bit is set to 1, a DMA operation begins if the Host Driver writes to the upper byte of Command register (00Fh). 1 = Enable 0 = Disable	0

Table below shows the summary of how register settings determine types of data transfer.

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Determination of Transfer Type

Multi/Single Block Select	Block Count Enable	Block Count	Function
0	Don't care	Don't care	Single Transfer
1	0	Don't care	Infinite Transfer
1	1	Not Zero	Multiple Transfer
1	1	Zero	Stop Multiple Transfer

NOTE: For CE-ATA access, (Auto) CMD12 must be issued after Command Completion Signal Disable.

Notification for Boot Mode Operation

NOTE:

1. In the boot mode, do not use “Auto Command 12 operation” and set "Response Type Select" field to 2'b00 (No Response).
2. This “Host Controller” do not support alternative boot operation using CMD0 with the argument of 0xFFFFFFFA
3. After boot code transfer is done, perform byte-write of address 0xD and set it to 0 so that CMD line goes back to HIGH (Make clear BOOTCMD, BOOTACK field). Then, wait for minimum of 56 SDCLK cycles as shown in the MMC 4.3 SPEC.
4. When BOOTACK is set, Host Controller needs to incur certain error interrupt if ACK pattern is not S-010-E. Currently, simply Data CRC Error occurs and thus, it is difficult to figure out ACK pattern is wrong.

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7.9.7 COMMAND REGISTER

7.9.7.1 Command Register

- CMDREG0, R/W, Address = 0xEB00_000E
- CMDREG1, R/W, Address = 0xEB10_000E
- CMDREG2, R/W, Address = 0xEB20_000E
- CMDREG3, R/W, Address = 0xEB30_000E

This register contains the SD Command Argument.

The Host Driver checks the Command Inhibit (DAT) bit and Command Inhibit (CMD) bit in the Present State register before writing to this register. Writing to the upper byte of this register triggers SD command generation. The Host Driver is responsible to write this register because the Host Controller does not protect the writing if Command Inhibit (CMD) is set.

CMDREG	Bit	Description	Initial State
Reserved	[15:14]	Reserved	
CMDIDX	[13:8]	Command Index These bits are set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the Command-Format in the SD Memory Card Physical Layer Specification and SDIO Card Specification.	
CMDTYP	[7:6]	Command Type There are three types of special commands: Suspend, Resume and Abort. These bits are set to 00b for all other commands. • Suspend Command If the Suspend command succeeds, the Host Controller assumes that the SD Bus has been released and it is possible to issue the next command, which uses the DAT line. The Host Controller de-asserts Read Wait for read transactions and stops checking busy for write transactions. The interrupt cycle starts, in 4-bit mode. If the Suspend command fails, the Host Controller maintains its current state, and the Host Driver restarts the transfer by setting Continue Request in the Block Gap Control register. • Resume Command The Host Driver re-starts the data transfer by restoring the registers in the range of 000-00Dh (Refer to Suspend and Resume mechanism). The Host Controller checks for busy before starting write transfers. • Abort Command If this command is set when executing a read transfer, the Host Controller stops reads to the buffer. If this command is set while executing a write transfer, the Host Controller stops driving the DAT line. After issuing the Abort command, the Host Driver must issue a software reset (Refer to Abort Transaction (5)). 11b = Abort CMD12, CMD52 for writing "I/O Abort" in CCCR 10b = Resume CMD52 for writing "Function Select" in CCCR 01b = Suspend CMD52 for writing "Bus Suspend" in CCCR	

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CMDREG	Bit	Description	Initial State
		00b = Normal Other commands	
DATAPRNT	[5]	Data Present Select This bit is set to 1 to indicate that data is present and transferred using the DAT line. It is set to 0 for the following: (1) Commands using only CMD line (ex. CMD52). (2) Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) (3) Resume command 1 = Data Present 0 = No Data Present	
ENCMDIDX	[4]	Command Index Check Enable If this bit is set to 1, the Host Controller checks the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. 1 = Enable 0 = Disable	
ENC MDCRC	[3]	Command CRC Check Enable If this bit is set to 1, the Host Controller checks the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The number of bits checked by the CRC field value changes according to the length of the response. 1 = Enable 0 = Disable	
Reserved	[2]	Reserved	
RSPTYP	[1:0]	Response Type Select 00 = No Response 01 = Response Length 136 10 = Response Length 48 11 = Response Length 48 check Busy after response	

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Relation between Parameters and the Name of Response Type

Response Type	Index Check Enable	CRC Check Enable	Name of Response Type
00	0	0	No Response
01	0	1	R2
10	0	0	R3, R4
10	1	1	R1, R6, R5
11	1	1	R1b, R5b

These bits determine Response types.

NOTE:

1. In the SDIO specification, response type notation of R5b is not defined. R5 includes R5b in the SDIO specification. But R5b is defined in this specification to specify the Host Controller checks busy after receiving response. For example, usually CMD52 is used as R5 but I/O abort command is used as R5b.
2. For CMD52 to read BS after writing "Bus Suspend," Command Type must be "Suspend" as well.

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7.10 RESPONSE REGISTER

This register is used to store responses from SD cards.

- Response Register 0 (Channel 0) (RSPREG0_0, ROC, Address = 0xEB00_0010)
- Response Register 1 (Channel 0) (RSPREG1_0, ROC, Address = 0xEB00_0014)
- Response Register 2 (Channel 0) (RSPREG2_0, ROC, Address = 0xEB00_0018)
- Response Register 3 (Channel 0) (RSPREG3_0, ROC, Address = 0xEB00_001C)

- Response Register 0 (Channel 1) (RSPREG0_1, ROC, Address = 0xEB10_0010)
- Response Register 1 (Channel 1) (RSPREG1_1, ROC, Address = 0xEB10_0014)
- Response Register 2 (Channel 1) (RSPREG2_1, ROC, Address = 0xEB10_0018)
- Response Register 3 (Channel 1) (RSPREG3_1, ROC, Address = 0xEB10_001C)

- Response Register 0 (Channel 2) (RSPREG0_2, ROC, Address = 0xEB20_0010)
- Response Register 1 (Channel 2) (RSPREG1_2, ROC, Address = 0xEB20_0014)
- Response Register 2 (Channel 2) (RSPREG2_2, ROC, Address = 0xEB20_0018)
- Response Register 3 (Channel 2) (RSPREG3_2, ROC, Address = 0xEB20_001C)

- Response Register 0 (Channel 3) (RSPREG0_3, ROC, Address = 0xEB30_0010)
- Response Register 1 (Channel 3) (RSPREG1_3, ROC, Address = 0xEB30_0014)
- Response Register 2 (Channel 3) (RSPREG2_3, ROC, Address = 0xEB30_0018)
- Response Register 3 (Channel 3) (RSPREG3_3, ROC, Address = 0xEB30_001C)

RSPREG	Bit	Description	Initial State
CMDRSP	[127:0]	Command Response The Table below describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register. 128-bit Response bit order : {RSPREG3, RSPREG2, RSPREG1, RSPREG0}	

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7.10.1 RESPONSE BIT DEFINITION FOR EACH RESPONSE TYPE

Kind of Response	Meaning of Response	Response Field	Response Register
R1, R1b (normal response)	Card Status	R [39:8]	REP [31:0]
R1b (Auto CMD12 response)	Card Status for Auto CMD12	R [39:8]	REP [127:96]
R2 (CID, CSD register)	CID or CSD reg. incl.	R [127:8]	REP [119:0]
R3 (OCR register)	OCR register for memory	R [39:8]	REP [31:0]
R4 (OCR register)	OCR register for I/O etc	R [39:8]	REP [31:0]
R5,R5b	SDIO response	R [39:8]	REP [31:0]
R6 (Published RCA response)	New published RCA[31:16] etc	R [39:8]	REP [31:0]

The Response Field indicates bit positions of "Responses" defined in the PHYSICAL LAYER SPECIFICATION Version 1.01. The Table (above) shows that most responses with a length of 48 (R[47:0]) have 32 bits of the response data (R[39:8]) stored in the Response register at REP[31:0]. Responses of type R1b (Auto CMD12 responses) have response data bits R[39:8] stored in the Response register at REP[127:96]. Responses with length 136 (R[135:0]) have 120 bits of the response data (R[127:8]) stored in the Response register at REP[119:0].

To be able to read the response status efficiently, the Host Controller only stores part of the response data in the Response register. This enables the Host Driver to efficiently read 32 bits of response data in one read cycle on a 32-bit bus system. Parts of the response, the Index field and the CRC, are checked by the Host Controller (as specified by the Command Index Check Enable and the Command CRC Check Enable bits in the Command register) and generate an error interrupt if an error is detected. The bit range for the CRC check depends on the response length. If the response length is 48, the Host Controller checks R[47:1], and if the response length is 136 the Host Controller checks R[119:1].

Since the Host Controller may have a multiple block data DAT line transfer executing concurrently with a CMD_wo_DAT command, the Host Controller stores the Auto CMD12 response in the upper bits (REP[127:96]) of the Response register. The CMD_wo_DAT response is stored in REP[31:0]. This allows the Host Controller to avoid overwriting the Auto CMD12 response with the CMD_wo_DAT and vice versa.

If the Host Controller modifies part of the Response register, as shown in the Table above, it shall preserve the unmodified bits.

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7.10.2 BUFFER DATA PORT REGISTER

7.10.2.1 Buffer Data Register

- BDATA0, R/W, Address = 0xEB00_0020
- BDATA1, R/W, Address = 0xEB10_0020
- BDATA2, R/W, Address = 0xEB20_0020
- BDATA3, R/W, Address = 0xEB30_0020

32-bit data port register to access internal buffer.

BDATA	Bit	Description	Initial State
BUFDAT	[31:0]	Buffer Data The Host Controller buffer is accessed through this 32-bit single port SRAM memory. Write and Read memories are separated.	Not fixed

NOTE: Detailed documents are to be copied from SD Host Standard Specification.

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7.10.3 PRESENT STATE REGISTER

7.10.3.1 Present State Register

- PRNSTS0, R/ROC, Address = 0xEB00_0024
- PRNSTS1, R/ROC, Address = 0xEB10_0024
- PRNSTS2, R/ROC, Address = 0xEB20_0024
- PRNSTS3, R/ROC, Address = 0xEB30_0024

This register contains the SD Command Argument.

PRNSTS	Bit	Description	Initial State
Reserved	[31:25]	Reserved	0
PRNTCMD	[24]	CMD Line Signal Level (RO) This status is used to check the CMD line level to recover from errors, and for debugging. Note: CMD port is mapped to SD0_CMD pin	0
PRNTDAT	[23:20]	DAT[3:0] Line Signal Level (RO) This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. D23 : DAT[3] D22 : DAT[2] D21 : DAT[1] D20 : DAT[0] Note: DAT port is mapped to SD0_DAT pin	Line State
Reserved	[19]	Reserved	1
PRNTCD	[18]	Card Detect Pin Level (RO) This bit reflects the inverse value of the SDCD# pin. Debouncing is not performed on this bit. This bit is valid if Card State Stable is set to 1, but it is not guaranteed because of propagation delay. Use of this bit is limited to testing since it must be debounced by software. 1 = Card present (SDCD#=0) 0 = No card present (SDCD#=1) Note: SDCD# port is mapped to SD0_nCD pin, SD2_nCD (Channel 2) port is fixed to LOW.	Line State
STBLCARD	[17]	Card State Stable (RO) This bit is used for testing. If this bit is 0, the Card Detect Pin Level is not stable. If this bit is set to 1, it means the Card Detect Pin Level is stable. No Card state is detected by this bit if set to 1 and Card Inserted is set to 0. The Software Reset For All in the Software Reset register does not affect this bit. 1 = No Card or Inserted 0 = Reset or Debouncing	1 (After Reset)
INSCARD	[16]	Card Inserted (RO) This bit indicates whether a card has been inserted. The Host Controller debounce this signal so that the Host Driver does not require to wait for it to stabilize. Changing from 0 to 1 generates a	0

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PRNSTS	Bit	Description	Initial State
		Card Insertion interrupt in the Normal Interrupt Status register and changing from 1 to 0 generates a Card Removal interrupt in the Normal Interrupt Status register. The Software Reset For All in the Software Reset register does not affect this bit. If a card is removed while its power is on and its clock is oscillating, the Host Controller clears SD Bus Power in the Power Control register and SD Clock Enable in the Clock Control register. If this bit is changed from 1 to 0, the Host Controller immediately stops driving CMD and DAT[3:0] (tri-state). In addition, the Host Driver must clear the Host Controller by the Software Reset For All in Software Reset register. The card detect is active regardless of the SD Bus Power. 1 = Card Inserted 0 = Reset or Debouncing or No Card	
Reserved	[15:12]	Reserved	
BUFRDRDY	[11]	Buffer Read Enable (ROC) This status is used for non-DMA read transfers. The Host Controller implements multiple buffers to transfer data efficiently. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs if all the block data is read from the buffer. A change of this bit from 0 to 1 occurs if block data is ready in the buffer and generates the Buffer Read Ready interrupt. 1 = Enables Read 0 = Disables Read	0
BUFWTRDY	[10]	Buffer Write Enable (ROC) This status is used for non-DMA write transfers. The Host Controller implements multiple buffers to transfer data efficiently. This read only flag indicates if space is available for write data. If this bit is 1, data is written to the buffer. A change of this bit from 1 to 0 occurs if all the block data is written to the buffer. A change of this bit from 0 to 1 occurs if top of block data is written to the buffer and generates the Buffer Write Ready interrupt. 1 = Write enable 0 = Write disable	0
RDTRANACT	[9]	Read Transfer Active (ROC) This status is used to detect completion of a read transfer. This bit is set to 1 for either of the following conditions: (1) After the end bit of the read command. (2) If writing a 1 to Continue Request in the Block Gap Control register to restart a read transfer. This bit is cleared to 0 for either of the following conditions: (1) If the last data block as specified by block length is transferred to the System. (2) If all valid data blocks have been transferred to the System and no current block transfers are being sent as a result of the Stop At Block Gap Request being set to 1. A Transfer Complete interrupt is generated if this bit changes to 0.	0

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PRNSTS	Bit	Description	Initial State
		1 = Transferring data 0 = No valid data	
WTTRANACT	[8]	Write Transfer Active (ROC) This status indicates that a write transfer is active. If this bit is 0, it means no valid write data exists in the Host Controller. This bit is set in either of the following cases: (1) After the end bit of the write command. (2) If 1 is written to Continue Request in the Block Gap Control register to restart a write transfer. This bit is cleared in either of the following cases: (1) After getting the CRC status of the last data block as specified by the transfer count (Single and Multiple) (2) After getting the CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, if this bit is changed to 0 a Block Gap Event interrupt is generated, as result of the Stop At Block Gap Request being set. This status is useful for the Host Driver to determine the right time to issue commands during write busy. 1 = Transferring data 0 = No valid data	0
Reserved	[7:3]	Reserved	0
DATLINEACT	[2]	DAT Line Active (ROC) This bit indicates whether one of the DAT line on SD Bus is in use. (a) In the case of read transactions This status indicates if a read transfer is In-progress on the SD Bus. Change in this value from 1 to 0 between data blocks generates a Block Gap Event interrupt in the Normal Interrupt Status register. This bit is set in either of the following cases: (1) After the end bit of the read command. (2) If 1 is written to Continue Request in the Block Gap Control register to restart a read transfer. This bit is cleared in either of the following cases: (1) If the end bit of the last data block is sent from the SD Bus to the Host Controller. (2) When beginning a wait read transfer at a stop at the block gap initiated by a Stop At Block Gap Request. The Host Controller waits at the next block gap by driving Read Wait at the start of the interrupt cycle. If the Read Wait signal is already driven (data buffer cannot receive data), the Host Controller waits for current block gap by continuing to drive the Read Wait signal. It is necessary to support Read Wait in order to use suspend/ resume function. (b) In the case of write transactions This status indicates that a write transfer is executing on the SD Bus. Change in this value from 1 to 0 generates a Transfer Complete interrupt in the Normal Interrupt Status register.	0

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PRNSTS	Bit	Description	Initial State
		This bit is set in either of the following cases: (1) After the end bit of the write command. (2) If 1 is written to Continue Request in the Block Gap Control register to continue a write transfer. This bit is cleared in either of the following cases: (1) If the SD card releases write busy of the last data block the Host Controller detects if output is not busy. If SD card does not drive busy signal for 8 SD Clocks, the Host Controller considers the card drive “Not Busy”. (2) If the SD card releases write busy prior to waiting for write transfer as a result of a Stop At Block Gap Request. 1 = DAT Line Active 0 = DAT Line Inactive	
CMDINHDAT	[1]	Command Inhibit (DAT) (ROC) (ROC) This status bit is generated if either the DAT Line Active or the Read Transfer Active is set to 1. If this bit is 0, it indicates the Host Controller can issue the next SD Command. Commands with busy signal belong to Command Inhibit (DAT) (ex. R1b, R5b type). Changing from 1 to 0 generates a Transfer Complete interrupt in the Normal Interrupt Status register. Note: The SD Host Driver saves registers in the range of 000-00Dh for a suspend transaction after this bit has changed from 1 to 0. 1 = Cannot issue command which uses the DAT line 0 = Issues command which uses the DAT line	0
CMDINHCMD	[0]	Command Inhibit (CMD) (ROC) If this bit is 0, it indicates the CMD line is not in use and the Host Controller issues a SD Command using the CMD line. This bit is set immediately after the Command register (00Fh) is written. This bit is cleared if the command response is received. Even if the Command Inhibit (DAT) is set to 1, Commands using only the CMD line is issued if this bit is 0. Changing from 1 to 0 generates a Command Complete interrupt in the Normal Interrupt Status register. If the Host Controller cannot issue the command because of a command conflict error (Refer to Command CRC Error) or because of Command Not Issued By Auto CMD12 Error, this bit remains 1 and the Command Complete is not set. Status issuing Auto CMD12 is not read from this bit. 1 = Cannot issue command 0 = Issues command using only CMD line	0

NOTE: Buffer Write Enable in Present register must not be asserted for DMA transfers since it generates Buffer Write Ready interrupt.

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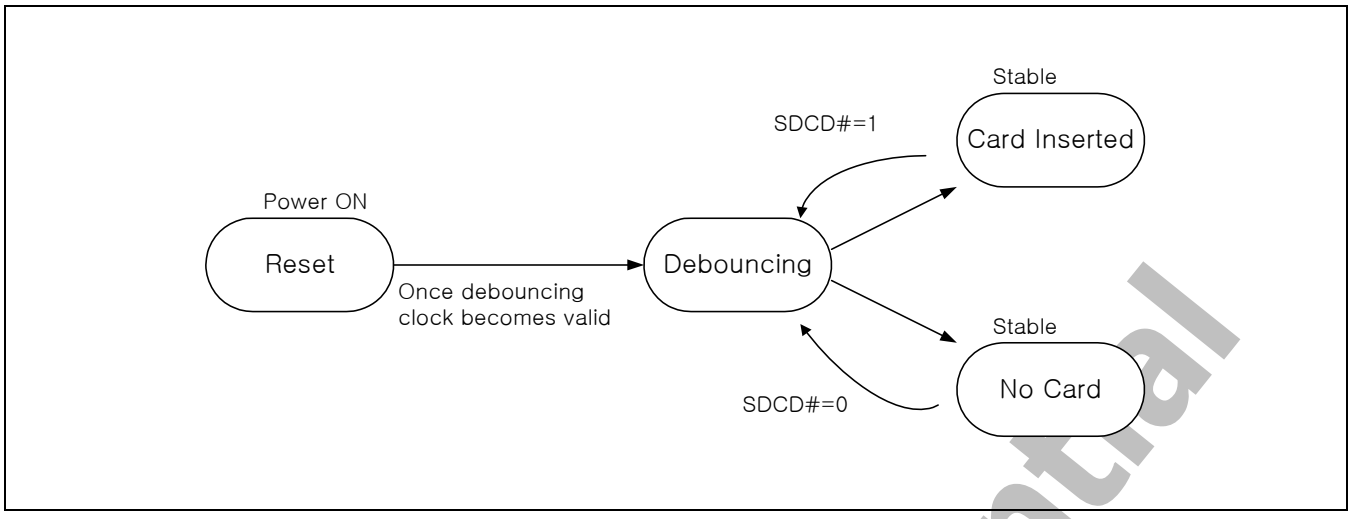

Figure 7-17 Card Detect State

The above *Figure 7-17* shows the state definitions of hardware that handles "Debouncing"

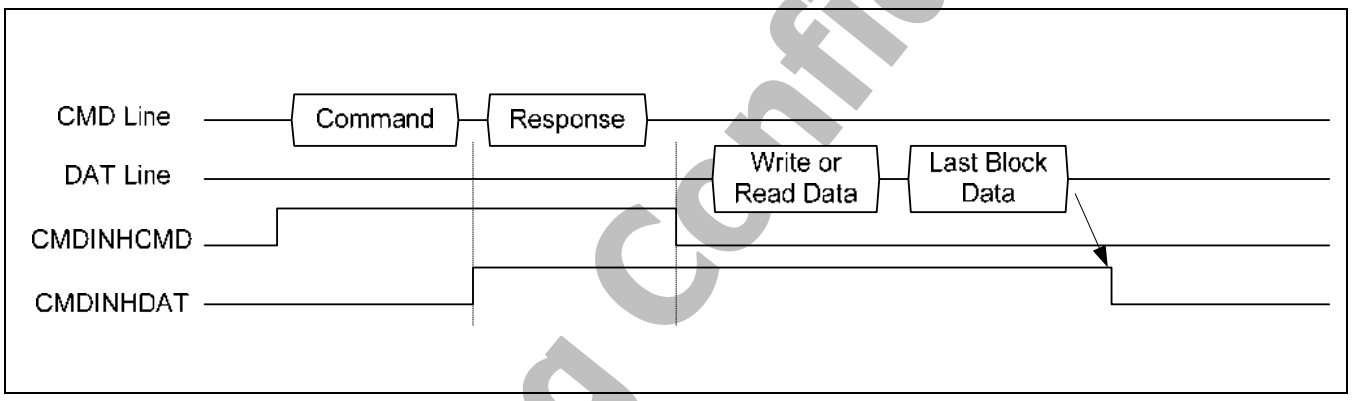

Figure 7-18 Timing of Command Inhibit (DAT) and Command Inhibit (CMD) with Data Transfer

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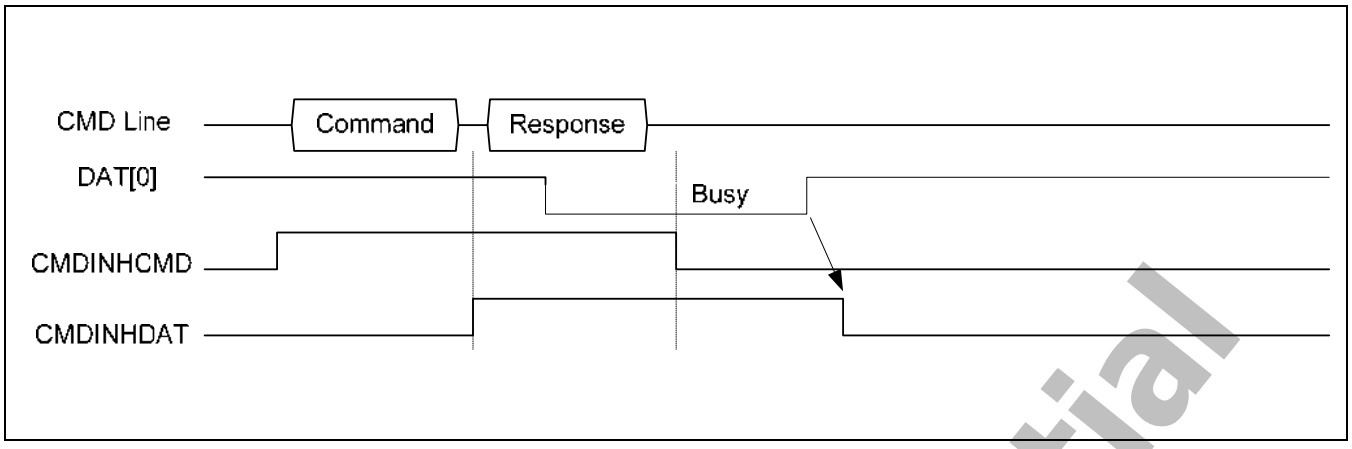

Figure 7-19 Timing of Command Inhibit (DAT) for the Case of Response with Busy

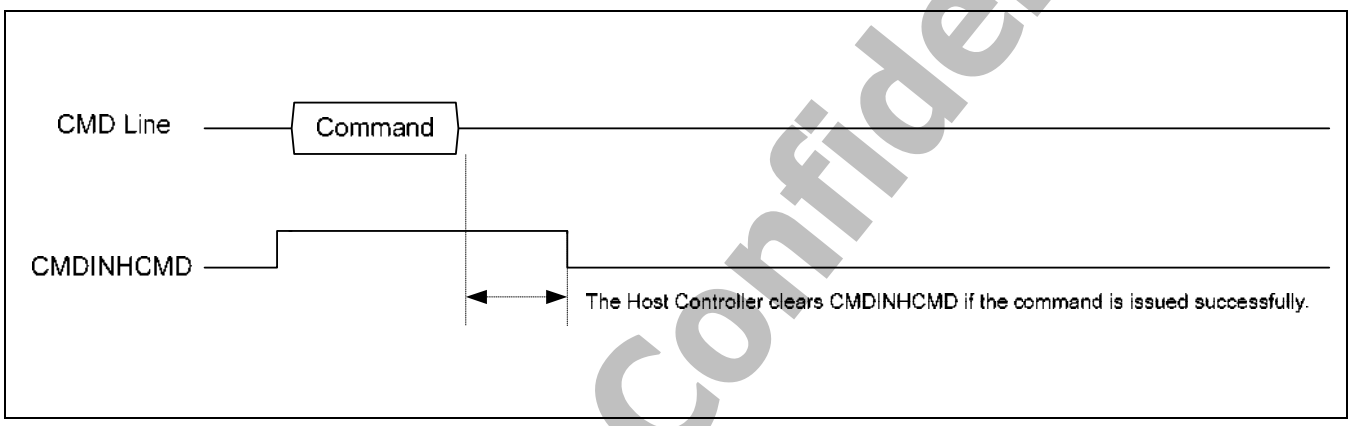

Figure 7-20 Timing of Command Inhibit (CMD) for the Case of No Response Command

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7.10.4 HOST CONTROL REGISTER

7.10.4.1 Present State Register

- HOSTCTL0, R/W, Address = 0xEB00_0028
- HOSTCTL1, R/W, Address = 0xEB10_0028
- HOSTCTL2, R/W, Address = 0xEB20_0028
- HOSTCTL3, R/W, Address = 0xEB30_0028

This register contains the SD Command Argument.

HOSTCTL	Bit	Description	Initial State
Reserved	[7]	Reserved This field should be fixed to LOW	0
Reserved	[6]	Reserved This field should be fixed to LOW	0
WIDE8	[5]	Extended Data Transfer Width (It is for MMC 8-bit card.) 1 = 8-bit operation 0 = Bit width is designated by the bit 1 (Data Transfer Width)	0
DMASEL	[4:3]	DMA Select One of supported DMA modes can be selected. The host driver checks support of DMA modes by referring the Capabilities register. Use of selected DMA is determined by DMA Enable of the Transfer Mode register. 00 = Selects SDMA 01 = Reserved 10 = Selects 32-bit Address ADMA2 11 = Selects 64-bit Address ADMA2 (Not supported)	0
OUTEDGEINV	[2]	Output Edge Inversion. If this bit is set to 0 (default), the Host Controller outputs CMD line and DAT lines at the falling edge of the SD Clock. If this bit is set to 1, the Host Controller outputs CMD line and DAT lines at the rising edge of the SD Clock 1 = Rising edge output 0 = Falling edge output	0
WIDE4	[1]	Data Transfer Width This bit selects the data width of the Host Controller. The Host Driver sets it to match the data width of the SD card. 1 = 4-bit mode 0 = 1-bit mode	0
Reserved	[0]	Reserved	0

NOTE: Card Detect Pin Level does not simply reflect SDCD# pin, but selects from SDCD, DAT[3], or CDTestlvl depending on CDSSigSel and SDCDSel values.

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7.10.5 POWER CONTROL REGISTER

This function is not implemented in this version.

7.10.5.1 Present State Register

- PWRCON0, R/W, Address = 0xEB00_0029
- PWRCON1, R/W, Address = 0xEB10_0029
- PWRCON2, R/W, Address = 0xEB20_0029
- PWRCON3, R/W, Address = 0xEB30_0029

This register contains the SD Command Argument.

PWRCON	Bit	Description	Initial State
Reserved	[7:4]	Reserved	
SELPWRLVL	[3:1]	SD Bus Voltage Select If these bits are set, the Host Driver selects the voltage level for the SD card. Before setting this register, the Host Driver checks the Voltage Support bits in the Capabilities register. If an unsupported voltage is selected, the Host System does not supply SD Bus voltage. 111b = 3.3V (Typ.) 110b = 3.0V (Typ.) 101b = 1.8V (Typ.) 100b – 000b = Reserved	0
PWRON	[0]	SD Bus Power Before setting this bit, the SD Host Driver sets SD Bus Voltage Select. If the Host Controller detects the No Card state, this bit is cleared. If this bit is cleared, the Host Controller immediately stops driving CMD and DAT[3:0] (tri-state) and drive SDCLK to low level. 1 = Power on 0 = Power off	0

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7.10.6 BLOCK GAP CONTROL REGISTER

7.10.6.1 Block Gap Control Register

- BLKGAP0, R/W, 0xEB00_002A
- BLKGAP1, R/W, 0xEB10_002A
- BLKGAP2, R/W, 0xEB20_002A
- BLKGAP3, R/W, 0xEB30_002A

This register contains the SD Command Argument.

BLKGAP	Bit	Description	Initial State
Reserved	[7:4]	Reserved	0
ENINTBGAP	[3]	Interrupt At Block Gap This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. If set to 1, it enables interrupt detection at the block gap for a multiple block transfer. If set to 0, it disables interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit must be set to 0. If the Host Driver detects an SD card insertion, it sets this bit according to the CCCR of the SDIO card. (RW) 1 = Enables 0 = Disables Note: it should be fixed to 0.	0
ENRWAIT	[2]	Read Wait Control The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using the DAT[2] line. Otherwise the Host Controller has to stop the SD Clock to hold read data, which restricts commands generation. If the Host Driver detects an SD card insertion, it sets this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit will never be set to 1 otherwise DAT line conflict might occur. If this bit is set to 0, Suspend/ Resume cannot be supported. (RW) 1 = Enables Read Wait Control 0 = Disables Read Wait Control	0
CONTREQ	[1]	Continue Request This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At Block Gap Request to 0 and set this bit 1 to restart the transfer. The Host Controller automatically clears this bit in either of the following cases: (1) If a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. (2) If a write transaction, the Write Transfer Active changes from 0 to 1 as the write transaction restarts. Therefore it is not necessary for Host Driver to set this bit to 0. If	0

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BLKGAP	Bit	Description	Initial State
		Stop At Block Gap Request is set to 1, any write to this bit is ignored. (RWAC) 1 = Restart 0 = Not affect	
STOPBGAP	[0]	Stop At Block Gap Request This bit is used to stop executing a transaction at the next block gap for both DMA and non-DMA transfers. Until the Transfer Complete is set to 1, indicating a transfer completion the Host Driver leaves this bit as 1. Clearing both the Stop At Block Gap Request and Continue Request does not restart the transaction. Read Wait stops the read transaction at the block gap. The Host Controller honours Stop At Block Gap Request for write transfers, but for read transfers it requires that the SD card support Read Wait. Therefore the Host Driver does not set this bit during read transfers unless the SD card supports Read Wait and has set Read Wait Control to 1. In the case of write transfers in which the Host Driver writes data to the Buffer Data Port register, the Host Driver sets this bit after all block data is written. If this bit is set to 1, the Host Driver does not write data to Buffer Data Port register. This bit affects Read Transfer Active, Write Transfer Active, DAT Line Active and Command Inhibit (DAT) in the Present State register. Regarding detailed control of bits D01 and D00. (RW) 1 = Stop 0 = Transfer	0

There are three cases to restart the transfer after stop at the block gap. Appropriate case depends on whether the Host Controller issues a Suspend command or the SD card accepts the Suspend command.

Cases are as follows:

1. If the Host Driver does not issue a Suspend command, the Continue Request restarts the transfer.
2. If the Host Driver issues a Suspend command and the SD card accepts it, a Resume command restarts the transfer.
3. If the Host Driver issues a Suspend command and the SD card does not accept it, the Continue Request restarts the transfer.

Any time Stop At Block Gap Request stops the data transfer, the Host Driver waits for Transfer Complete (in the Normal Interrupt Status register) before attempting to restart the transfer. If the data transfer by Continue Request is restarted, the Host Driver clears Stop At Block Gap Request before or simultaneously.

NOTE: After setting Stop At Block Gap Request field, it must not be cleared unless Block Gap Event or Transfer Complete interrupt occurs. Otherwise, the module hangs.

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7.10.7 WAKEUP CONTROL REGISTER

7.10.7.1 Wakeup Control Register

- WAKCON0, R/W, Address = 0xEB00_002B
- WAKCON1, R/W, Address = 0xEB10_002B
- WAKCON2, R/W, Address = 0xEB20_002B
- WAKCON3, R/W, Address = 0xEB30_002B

This register is mandatory for the Host Controller, but wakeup functionality depends on the Host Controller system hardware and software. The Host Driver sets SD Bus Power to 1 in the Power Control Register to maintains voltage on the SD Bus, if wakeup event via Card Interrupt is desired.

WAKCON	Bit	Description	Initial State
Reserved	[7:4]	Reserved	0
StaWakeup	[3]	Wakeup Event Status This status is set if the Card Inserted/ Removed or Card Interrupt Stop mode Wakeup Event Occurred. (ROC/RW1C) 1 = Wakeup Interrupt Occurred 0 = Wakeup Interrupt Not occurred or Cleared.	0
ENWKUPREM	[2]	Wakeup Event Enable On SD Card Removal This bit enables wakeup event via Card Removal assertion in the Normal Interrupt Status register. FN_WUS (Wake Up Support) in CIS does not affect this bit. (RW) 1 = Enables 0 = Disables	0
ENWKUPINS	[1]	Wakeup Event Enable On SD Card Insertion This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register. FN_WUS (Wake Up Support) in CIS does not affect this bit. (RW) 1 = Enables 0 = Disable	0
ENWKUPINT	[0]	Wakeup Event Enable On Card Interrupt This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register. This bit is set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1. (RW) 1 = Enables 0 = Disables	0

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7.10.8 CLOCK CONTROL REGISTER

7.10.8.1 Command Register

- CLKCON0, R/W, Address = 0xEB00_002C
- CLKCON1, R/W, Address = 0xEB10_002C
- CLKCON2, R/W, Address = 0xEB20_002C
- CLKCON3, R/W, Address = 0xEB30_002C

At the initialization of the Host Controller, the Host Driver sets the SDCLK Frequency Select according to the Capabilities register.

<table>
<tr><th>CLKCON</th><th>Bit</th><th>Description</th><th>Initial State</th></tr>
<tr><td>SELFREQ</td><td>[15:8]</td><td>SDCLK Frequency Select
This register is used to select the frequency of SDCLK pin. The frequency is not programmed directly; rather this register holds the divisor of the Base Clock Frequency For SD Clock in the Capabilities register. Only the following settings are allowed.
<table>
<tr><td>80h</td><td>base clock divided by 256</td></tr>
<tr><td>40h</td><td>base clock divided by 128</td></tr>
<tr><td>20h</td><td>base clock divided by 64</td></tr>
<tr><td>10h</td><td>base clock divided by 32</td></tr>
<tr><td>08h</td><td>base clock divided by 16</td></tr>
<tr><td>04h</td><td>base clock divided by 8</td></tr>
<tr><td>02h</td><td>base clock divided by 4</td></tr>
<tr><td>01h</td><td>base clock divided by 2</td></tr>
<tr><td>00h</td><td>base clock</td></tr>
</table>
Setting 00h specifies the highest frequency of the SD Clock. Setting multiple bits, the most significant bit is used as the divisor. But multiple bits must not be set. The two default divider values are calculated by the frequency that is defined by the Base Clock Frequency For SD Clock in the Capabilities register.
(1) 25MHz divider value,
(2) 400kHz divider value
According to the SD Physical Specification Version 1.01 and the SDIO Card Specification Version 1.0, maximum SD Clock frequency is 25MHz, and never exceeds this limit.
The frequency of SDCLK is set by the following formula:
Clock Frequency = (Base Clock)/ divisor
Therefore, select the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency. For example, if the Base Clock Frequency For SD Clock in the Capabilities register has the value 33MHz, and the target frequency is 25MHz, then selecting the divisor value of 01h yields 16.5MHz, which is the nearest frequency less than or equal to the target. Similarly, to approach a clock value of 400kHz, the divisor value of 40h yields the optimal clock value of</td><td>0</td></tr>
</table>

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CLKCON	Bit	Description	Initial State
		258kHz. (Base input clock should not exceed 102MHz.)	
Reserved	[7:4]	Reserved	
STBLEXTCLK	[3]	External Clock Stable This bit is set to 1 if SD Clock output is stable after writing to SD Clock Enable in this register to 1. The SD Host Driver waits to issue command to start until this bit is set to 1. (ROC) 1 = Ready 0 = Not Ready	0
ENSDCLK	[2]	SD Clock Enable The Host Controller stops SDCLK if this bit is written to 0. SDCLK Frequency Select changes if this bit is 0. Then, the Host Controller maintains the same clock frequency until SDCLK is stopped (Stop at SDCLK=0). If the Card Inserted in the Present State register is cleared, this clears the bit (RW). 1 = Enables 0 = Disables	0
STBLINTCLK	[1]	Internal Clock Stable This bit is set to 1 if SD Clock is stable after writing to Internal Clock Enable in this register to 1. The SD Host Driver waits to set SD Clock Enable until this bit is set to 1. Note: This is useful if PLL is used for a clock oscillator that requires setup time. (ROC) 1 = Ready 0 = Not Ready	0
ENINTCLK	[0]	Internal Clock Enable This bit is set to 0 if the Host Driver is not using the Host Controller or the Host Controller awaits a wakeup interrupt. The Host Controller must stop its internal clock to go at very low power state. Still, registers is able to be read and written. Clock starts to oscillate when this bit is set to 1. If clock oscillation is stable, the Host Controller can be set 'Internal Clock Stable (CLKCON)' when this bit as 1. This bit does not affect card detection. (RW) 1 = Oscillate 0 = Stop	

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7.10.9 TIMEOUT CONTROL REGISTER

7.10.9.1 Timeout Control Register

- TIMEOUTCON0, R/W, Address = 0xEB00_002E
- TIMEOUTCON1, R/W, Address = 0xEB10_002E
- TIMEOUTCON2, R/W, Address = 0xEB20_002E
- TIMEOUTCON3, R/W, Address = 0xEB30_002E

At the initialization of the Host Controller, the Host Driver sets the Data Timeout Counter Value according to the Capabilities register.

TIMEOUTCON	Bit	Description	Initial State
Reserved	[7:4]	Reserved	0
TIMEOUTCON	[3:0]	Data Timeout Counter Value This value determines the interval by which DAT line timeouts are detected. Refer to the Data Timeout Error in the Error Interrupt Status register for information on factors that dictate timeout generation. Timeout clock frequency is generated by dividing the base clock TMCLK value by this value. While setting this register, prevent inadvertent timeout events by clearing the Data Timeout Error Status Enable (in the Error Interrupt tatus Enable register) 1111b Reserved 1110b TMCLK x 2^27 1101b TMCLK x 2^26 …….. … 0001b TMCLK x 2^14 0000b TMCLK x 2^13	0

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7.10.10 SOFTWARE RESET REGISTER

7.10.10.1 Software Reset Register

- SWRST0, R/W, Address = 0xEB00_002F
- SWRST1, R/W, Address = 0xEB10_002F
- SWRST2, R/W, Address = 0xEB20_002F
- SWRST3, R/W, Address = 0xEB30_002F

A reset pulse is generated when writing 1 to each bit of this register. After completing the reset, the Host Controller clears each bit. Because it takes time to complete software reset, the SD Host Driver confirms that these bits are 0.

SWRST	Bit	Description	Initial State
Reserved	[7:3]	Reserved	0
RSTDAT	[2]	Software Reset For DAT Line Only part of data circuit is reset. DMA circuit is also reset. (RWAC) The following registers and bits are cleared by this bit: Buffer Data Port register Buffer is cleared and initialized. Present State register Buffer Read Enable Buffer Write Enable Read Transfer Active Write Transfer Active DAT Line Active Command Inhibit (DAT) Block Gap Control register Continue Request Stop At Block Gap Request Normal Interrupt Status register Buffer Read Ready Buffer Write Ready DMA Interrupt Block Gap Event Transfer Complete 1 = Reset 0 = Work	0
RSTCMD	[1]	Software Reset For CMD Line Only part of command circuit is reset. (RWAC). The following registers and bits are cleared by this bit: Present State register Command Inhibit (CMD) Normal Interrupt Status register Command Complete 1 = Reset 0 = Work	0
RSTALL	[0]	Software Reset For All This reset affects the entire Host Controller except for the card	0

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SWRST	Bit	Description	Initial State
		detection circuit. Register bits of type ROC, RW, RW1C, RWAC, HWInit are cleared to 0. During its initialization, the Host Driver sets this bit to 1 to reset the Host Controller. The Host Controller reset this bit to 0 if capabilities registers are valid and the Host Driver reads them. If this bit is set to 1, the SD card resets itself and must be reinitialized by the Host Driver. (RWAC) 1 = Reset 0 = Work	

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7.10.11 NORMAL INTERRUPT STATUS REGISTER

7.10.11.1 Normal Interrupt Status Register

- NORINTSTS0, ROC/RW1C, Address = 0xEB00_0030
- NORINTSTS1, ROC/RW1C, Address = 0xEB10_0030
- NORINTSTS2, ROC/RW1C, Address = 0xEB20_0030
- NORINTSTS3, ROC/RW1C, Address = 0xEB30_0030

The Normal Interrupt Status Enable affects reads of this register, but Normal Interrupt Signal Enable does not affect these reads. An interrupt is generated if the Normal Interrupt Signal Enable is enabled and at least one of the status bits is set to 1. For all bits except Card Interrupt and Error Interrupt, writing 1 to a bit clears it; writing 0 keeps the bit unchanged. More than one status is cleared with a single register write. The Card Interrupt is cleared if the card stops asserting the interrupt; that is, if the Card Driver services the interrupt condition.

NORINTSTS	Bit	Description	Initial State
STAERR	[15]	Error Interrupt If any of the bits in the Error Interrupt Status register are set, then this bit is set. Therefore the Host Driver checks this bit first to efficiently tests for an error. This bit is read only. (ROC) 0 = No Error 1 = Error	0
STAFIA3	[14]	FIFO SD Address Pointer Interrupt 3 Status (RW1C) 0 = Occurred 1 = Not Occurred If the FIFO Address of the SD clock side reaches the FIFO Interrupt Address register 3 values, this status bit is asserted.	0
STAFIA2	[13]	FIFO SD Address Pointer Interrupt 2 Status (RW1C) 0 = Occurred 1 = Not Occurred If the FIFO Address of the SD clock side reaches the FIFO Interrupt Address register 2 values, this status bit is asserted.	0
STAFIA1	[12]	FIFO SD Address Pointer Interrupt 1 Status (RW1C) 0 = Occurred 1 = Not Occurred If the FIFO Address of the SD clock side reaches the FIFO Interrupt Address register 1 value, this status bit is asserted.	0
STAFIA0	[11]	FIFO SD Address Pointer Interrupt 0 Status (RW1C) 0 = Occurred 1 = Not Occurred If the FIFO Address of the SD clock side reaches the FIFO Interrupt Address register 0 value, this status bit is asserted.	0
STARWAIT	[10]	Read Wait Interrupt Status (RW1C) 0 = Read Wait Interrupt Not Occurred 1 = Read Wait Interrupt Occurred Note: After checking response for the suspend command, release Read Wait interrupt status manually if BS = 0 (BS means 'Bus Status' field 'Bus Suspend' register in the SDIO card	0

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NORINTSTS	Bit	Description	Initial State
		specification) Note: Read Wait operation procedure is started after 4-SDCLK from the end of the block data read transfer.	
STACCS	[9]	CCS Interrupt Status (RW1C) Command Complete Signal Interrupt Status bit is for CE-ATA interface mode. 0 = CCS Interrupt Occurred 1 = CCS Interrupt Not Occurred	0
STACARDINT	[8]	Card Interrupt Writing this bit to 1 does not clear this bit. It is cleared by resetting the SD card interrupt factor. In 1-bit mode, the Host Controller detects the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, therefore there are some sample delays between the interrupt signal from the SD card and the interrupt to the Host System. It is necessary to define how to handle this delay. If this status is set and the Host Driver needs to start this interrupt service, Card Interrupt Signal Enable in the Normal Interrupt Signal Enable register must be set to 0 in order to clear the card interrupt status latched in the Host Controller and to stop driving the interrupt signal to the Host System. After completion of the card interrupt service (It must reset interrupt factors in the SD card and the interrupt signal may not be asserted), write 1 to clear this register field (RW1C) and set Card Interrupt Signal Enable to 1 to re-start sampling the interrupt signal. The Card Interrupt Status Enable must remain set to high. (RW1C) (2), (3) 1 = Generates Card Interrupt 0 = No Card Interrupt	0
STACARDREM	[7]	Card Removal This status is set if the Card Inserted in the Present State register changes from 1 to 0. If the Host Driver writes this bit to 1 to clear this status, the status of the Card Inserted in the Present State register must be confirmed. Because the card detect state may possibly be changed if the Host Driver clear this bit and interrupt event may not be generated. (RW1C) 1 = Card removed 0 = Card state stable or Debouncing	0
STACARDINS	[6]	Card Insertion This status is set if the Card Inserted in the Present State register changes from 0 to 1. If the Host Driver writes this bit to 1 to clear this status, the status of the Card Inserted in the Present State register must be confirmed. Because the card detect state may possibly be changed if the Host Driver clear this bit and interrupt event may not be generated. (RW1C) 1 = Card inserted 0 = Card state stable or Debouncing	0

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NORINTSTS	Bit	Description	Initial State
STABUFRDRDY	[5]	Buffer Read Ready This status is set if the Buffer Read Enable changes from 0 to 1. Refer to the Buffer Read Enable in the Present State register (9.10). (RW1C) 1 = Ready to read buffer 0 = Not ready to read buffer	0
STABUFWTRDY	[4]	Buffer Write Ready This status is set if the Buffer Write Enable changes from 0 to 1. Refer to the Buffer Write Enable in the Present State register (9.10). (RW1C) 1 = Ready to write buffer 0 = Not ready to write buffer	0
STADMAINT	[3]	DMA Interrupt This status is set if the Host Controller detects the Host SDMA Buffer boundary during transfer. Refer to the Host SDMA Buffer Boundary in the Block Size register (9.3). Other DMA interrupt factors may be added in the future. In case of ADMA, by setting interrupt field in the descriptor table, Host Controller generates this interrupt. If it is used for debugging. This interrupt is not generated after the Transfer Complete. (RW1C) 1 = Generates DMA Interrupt 0 = No DMA Interrupt	0
STABLKGAP	[2]	Block Gap Event If the Stop At Block Gap Request in the Block Gap Control register is set, this bit is set if both read/ write transaction is stopped at a block gap. If Stop At Block Gap Request is not set to 1, this bit is not set to 1. (RW1C) (1) In the case of a Read Transaction This bit is set at the falling edge of the DAT Line Active Status (When the transaction is stopped at SD Bus timing. The Read Wait must be supported in order to use this function). (2) Case of Write Transaction This bit is set at the falling edge of Write Transfer Active Status (After getting CRC status at SD Bus timing). 1 = Transaction stopped at block gap 0 = No Block Gap Event	0
STATRANCMPLT	[1]	Transfer Complete This bit is set if a read/ write transfer is complete. (1) In the case of a Read Transaction This bit is set at the falling edge of Read Transfer Active Status. There are two cases in which this interrupt is generated. The first is if a data transfer is complete as specified by data length (After the last data has been read to the Host System). The second if data has stopped at the block gap and complete the data transfer by setting the Stop At Block Gap Request in the Block Gap Control register (After valid data has been read to the Host	0

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<table>
<tr><th>NORINTSTS</th><th>Bit</th><th>Description</th><th>Initial State</th></tr>
<tr><td></td><td></td><td>System).
(2) In the case of a Write Transaction
This bit is set at the falling edge of the DAT Line Active Status. There are two cases in which this interrupt is generated. The first if the last data is written to the SD card as specified by data length and the busy signal released. The second if data transfers are stopped at the block gap by setting Stop At Block Gap Request in the Block Gap Control register and data transfers complete. (After valid data is written to the SD card and the busy signal released). (RW1C)
The table below shows that Transfer Complete has higher priority than Data Timeout Error. If both bits are set to 1, the data transfer is considered complete. Relation between Transfer Complete and Data
<table>
<tr><th>Transfer Complete</th><th>Data Timeout Error</th><th>Meaning of the status</th></tr>
<tr><td>0</td><td>0</td><td>Interrupted by another factor</td></tr>
<tr><td>0</td><td>1</td><td>Timeout occur during transfer</td></tr>
<tr><td>1</td><td>Don’t care</td><td>Data transfer complete</td></tr>
</table>
1 = Data Transfer Complete
0 = No Transfer Complete</td><td></td></tr>
<tr><td>STACMDCMPLT</td><td>[0]</td><td>Command Complete
This bit is set when receive the end bit of the command response. (Except Auto CMD12) Refer to Command Inhibit (CMD) in the Present State register.
The table below shows that Command Timeout Error has higher priority than Command Complete. If both bits are set to 1, it is considered that the response was not received correctly. (RW1C)
<table>
<tr><th>Command Complete</th><th>Command Timeout Error</th><th>Meaning of the Status</th></tr>
<tr><td>0</td><td>0</td><td>Interrupted by another factor</td></tr>
<tr><td>Don't care</td><td>1</td><td>Response not received within 64 SDCLK cycles.</td></tr>
<tr><td>1</td><td>0</td><td>Response received</td></tr>
</table>
1 = Command Complete
0 = No command complete</td><td>0</td></tr>
</table>

NOTE:

1. Host Driver checks if interrupt is actually cleared by polling or monitoring the INTREQ port. If HCLK is much faster than SDCLK, it takes long time to be cleared for the bits actually.
2. Card Interrupt status bit keeps previous value until next card interrupt period (level interrupt) and is cleared if write to 1 (RW1C).
3. SD/MMC Controller of the S5PV210 does not support "card interrupt at block gap" used if the multiple block 4-bit operation.

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7.10.12 ERROR INTERRUPT STATUS REGISTER

7.10.12.1 Error Interrupt Status Register

- ERRINTSTS0, ROC/RW1C, Address = 0xEB00_0032
- ERRINTSTS1, ROC/RW1C, Address = 0xEB10_0032
- ERRINTSTS2, ROC/RW1C, Address = 0xEB20_0032
- ERRINTSTS3, ROC/RW1C, Address = 0xEB30_0032

Signals defined in this register are enabled by the Error Interrupt Status Enable register, but not by the Error Interrupt Signal Enable register. Generates interrupt if the Error Interrupt Signal Enable is enabled and at least one of the statuses is set to 1. Writing to 1 clears the bit and writing to 0 keeps the bit unchanged. More than one status is cleared on one register write.

ERRINTSTS	Bit	Description	Initial State
Reserved	[15:11]	Reserved	0
STABOOTACKERR	[10]	Boot Ack Error This bit is set when the Host Controller detects Boot Ack receive error during Boot mode.	0
STAADMAERR	[9]	ADMA Error This bit is set if the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register, In addition, the Host Controller generates this Interrupt if it detects invalid descriptor data (Valid=0) at the ST_FDS state. ADMA Error State in the ADMA Error Status indicates that an error occurs in ST_FDS state. The Host Driver may find that Valid bit is not set at the error descriptor. 1 = Error 0 = No Error	0
STAACMDERR	[8]	Auto CMD12 Error Occurs if it detects that one of the bits in Auto CMD12 Error Status register has changed from 0 to 1. This bit is set to 1, if the errors in Auto CMD12 occur and if Auto CMD12 is not executed due to the previous command error. 1 = Error 0 = No Error	0
STACURERR	[7]	Current Limit Error Not implemented in this version. Always 0.	0
STADENDERR	[6]	Data End Bit Error Occurs if it detects 0 at the end bit position of read data which uses the DAT line or at the end bit position of the CRC Status. 1 = Error 0 = No Error	0
STADATCRCERR	[5]	Data CRC Error Occurs if it detects CRC error when transferring read data which uses the DAT line or if it detects the Write CRC status having a value of other than "010".	0

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ERRINTSTS	Bit	Description	Initial State
		1 = Error 0 = No Error	
STADATTOUTERR	[4]	Data Timeout Error Occurs if it detects one of following timeout conditions. (1) Busy timeout for R1b, R5b type (2) Busy timeout after Write CRC status (3) Write CRC Status timeout (4) Read Data timeout. 1 = Timeout 0 = No Error	0
STACMDIDXERR	[3]	Command Index Error Occurs if a Command Index error occurs in the command response. 1 = Error 0 = No Error	0
STACMDEBITERR	[2]	Command End Bit Error Occurs if it detects that the end bit of a command response is 0. 1 = End bit Error generated 0 = No Error	
STACMDCRCERR	[1]	Command CRC Error Command CRC Error is generated in two cases. (1) If a response is returned and the Command Timeout Error is set to 0 (indicating no timeout), this bit is set to 1 if it detects a CRC error in the command response. (2) The Host Controller detects a CMD line conflict by monitoring the CMD line if a command is issued. If the Host Controller drives the CMD line to 1 level, but detects 0 levels on the CMD line at the next SDCLK edge, then the Host Controller aborts the command (Stop driving CMD line) and set this bit to 1. The Command Timeout Error also set to 1 to distinguish CMD line conflict. 1 = Generates CRC Error 0 = No Error	0
STACMDTOUTERR	[0]	Command Timeout Error Occurs if no response is returned within 64 SDCLK cycles from the end bit of the command. If the Host Controller detects a CMD line conflict, in which case Command CRC Error also set as shown in Table below, this bit sets without waiting for 64 SDCLK cycles because the Host Controller aborts command. 1 = Timeout 0 = No Error	0

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The relation between Command CRC Error and Command Timeout Error is shown in Table below.

The Relation Between Command CRC Error and Command Timeout Error

Command CRC Error	Command Timeout Error	Kinds of Error
0	0	No Error
0	1	Response Timeout Error
1	0	Response CRC Error
1	1	CMD line conflict

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7.10.13 NORMAL INTERRUPT STATUS ENABLE REGISTER

7.10.13.1 Normal Interrupt Status Enable Register

- NORINTSTSEN0, R/W, Address = 0xEB00_0034
- NORINTSTSEN1, R/W, Address = 0xEB10_0034
- NORINTSTSEN2, R/W, Address = 0xEB20_0034
- NORINTSTSEN3, R/W, Address = 0xEB30_0034

Setting to 1 enables Interrupt Status.

NORINTSTSEN	Bit	Description	Initial State
-	[15]	Fixed to 0 The Host Driver controls error interrupts using the Error Interrupt Status Enable register. (R)	0
ENSTAFIA3	[14]	FIFO SD Address Pointer Interrupt 3 Status Enable 1 = Enabled 0 = Masked	0
ENSTAFIA2	[13]	FIFO SD Address Pointer Interrupt 2 Status Enable 1 = Enabled 0 = Masked	0
ENSTAFIA1	[12]	FIFO SD Address Pointer Interrupt 1 Status Enable 1 = Enabled 0 = Masked	0
ENSTAFIA0	[11]	FIFO SD Address Pointer Interrupt 0 Status Enable 1 = Enabled 0 = Masked	0
ENSTARWAIT	[10]	Read Wait interrupt status enable 1 = Enabled 0 = Masked	0
ENSTACCS	[9]	CCS Interrupt Status Enable 1 = Enabled 0 = Masked	0
ENSTACARDINT	[8]	Card Interrupt Status Enable If this bit is set to 0, the Host Controller clears interrupt request to the System. The Card Interrupt detection is stopped if this bit is cleared and restarted if this bit is set to 1. The Host Driver must clear the Card Interrupt Status Enable before servicing the Card Interrupt and must set this bit again after all interrupt requests from the card are cleared to prevent inadvertent interrupts. 1 = Enabled 0 = Masked	0
ENSTACARDREM	[7]	Card Removal Status Enable 1 = Enabled 0 = Masked	0

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NORINTSTSEN	Bit	Description	Initial State
ENSTACARDNS	[6]	Card Insertion Status Enable 1 = Enabled 0 = Masked	0
ENSTABUFRDRDY	[5]	Buffer Read Ready Status Enable 1 = Enabled 0 = Masked	0
ENSTABUFWTRDY	[4]	Buffer Write Ready Status Enable 1 = Enabled 0 = Masked	0
ENSTADMA	[3]	DMA Interrupt Status Enable 1 = Enabled 0 = Masked	0
ENSTABLKGAP	[2]	Block Gap Event Status Enable 1 = Enabled 0 = Masked	0
ENSTASTANSCMPLT	[1]	Transfer Complete Status Enable 1 = Enabled 0 = Masked	0
ENSTACMDCMPLT	[0]	Command Complete Status Enable 1 = Enabled 0 = Masked	0

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7.10.14 ERROR INTERRUPT STATUS ENABLE REGISTER

7.10.14.1 Error Interrupt Status Enable Register

- ERRINTSTSEN0, R/W, 0xEB00_0036
- ERRINTSTSEN1, R/W, 0xEB10_0036
- ERRINTSTSEN2, R/W, 0xEB20_0036
- ERRINTSTSEN3, R/W, 0xEB30_0036

Setting to 1 enables Error Interrupt Status.

ERRINTSTSEN	Bit	Description	Initial State
Reserved	[15:11]	Reserved	0
ENSTABOOTACKERR	[10]	Boot Ack Error Status Enable 1 = Enabled, 0 = Masked	0
ENSTAADMAERR	[9]	ADMA Error Status Enable 1 = Enabled, 0 = Masked	0
ENSTAACMDERR	[8]	Auto CMD12 Error Status Enable 1 = Enabled, 0 = Masked	0
ENSTACURERR	[7]	Current Limit Error Status Enable This function is not implemented in this version. 1 = Enabled 0 = Masked	0
ENSTADENDERR	[6]	Data End Bit Error Status Enable 1 = Enabled 0 = Masked	0
ENSTADATCRCERR	[5]	Data CRC Error Status Enable 1 = Enabled 0 = Masked	0
ENSTADATTOUTERR	[4]	Data Timeout Error Status Enable 1 = Enabled 0 = Masked	0
ENSTACMDIDXERR	[3]	Command Index Error Status Enable 1 = Enabled 0 = Masked	0
ENSTACMDEBITERR	[2]	Command End Bit Error Status Enable 1 = Enabled 0 = Masked	0
ENSTACMDCRCERR	[1]	Command CRC Error Status Enable 1 = Enabled 0 = Masked	0
ENSTACMDTOUTERR	[0]	Command Timeout Error Status Enable 1 = Enabled 0 = Masked	0

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7.10.15 NORMAL INTERRUPT SIGNAL ENABLE REGISTER

7.10.15.1 Normal Interrupt Signal Enable Register

- NORINTSIGEN0, R/W, Address = 0xEB00_0038
- NORINTSIGEN1, R/W, Address = 0xEB10_0038
- NORINTSIGEN2, R/W, Address = 0xEB20_0038
- NORINTSIGEN3, R/W, Address = 0xEB30_0038

This register is used to select which interrupt status is indicated to the Host System as the interrupt. These status bits share the same1 bit interrupt line. To enable interrupt generate set any of this bit to 1.

NORINTSIGEN	Bit	Description	Initial State
	[15]	Fixed to 0 The Host Driver controls error interrupts using the Error Interrupt Signal Enable register.	0
ENSIGFIA3	[14]	FIFO SD Address Pointer Interrupt 3 Signal Enable 1 = Enabled 0 = Masked	0
ENSIGFIA2	[13]	FIFO SD Address Pointer Interrupt 2 Signal Enable 1 = Enabled 0 = Masked	0
ENSIGFIA1	[12]	FIFO SD Address Pointer Interrupt 1 Signal Enable 1 = Enabled 0 = Masked	0
ENSIGFIA0	[11]	FIFO SD Address Pointer Interrupt 0 Signal Enable 1 = Enabled 0 = Masked	0
ENSIGRWAIT	[10]	Read Wait Interrupt Signal Enable 1 = Enabled 0 = Masked	0
ENSIGCCS	[9]	CCS Interrupt Signal Enable Command Complete Signal Interrupt Status bit is for CE-ATA interface mode. 1 = Enabled 0 = Masked	0
ENSIGCARDINT	[8]	Card Interrupt Signal Enable 1 = Enabled 0 = Masked	0
ENSIGCARDREM	[7]	Card Removal Signal Enable 1 = Enabled 0 = Masked	0
ENSIGCARDNS	[6]	Card Insertion Signal Enable 1 = Enabled 0 = Masked	0
ENSIGBUFRDRDY	[5]	Buffer Read Ready Signal Enable	0

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NORINTSIGEN	Bit	Description	Initial State
		1 = Enabled 0 = Masked	
ENSIGBUFWTRDY	[4]	Buffer Write Ready Signal Enable 1 = Enabled 0 = Masked	0
ENSIGDMA	[3]	DMA Interrupt Signal Enable 1 = Enabled 0 = Masked	0
ENSIGBLKGAP	[2]	Block Gap Event Signal Enable 1 = Enabled 0 = Masked	0
ENSIGSTANSCMPLT	[1]	Transfer Complete Signal Enable 1 = Enabled 0 = Masked	0
ENSIGCMDCMPLT	[0]	Command Complete Signal Enable 1 = Enabled 0 = Masked	0

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7.10.16 ERROR INTERRUPT SIGNAL ENABLE REGISTER

7.10.16.1 Error Interrupt Signal Enable Register

- ERRINTSIGEN0, R/W, Address = 0xEB00_003A
- ERRINTSIGEN1, R/W, Address = 0xEB10_003A
- ERRINTSIGEN2, R/W, Address = 0xEB20_003A
- ERRINTSIGEN3, R/W, Address = 0xEB30_003A

This register is used to select which interrupt status is notified to the Host System as the interrupt. These status bits share the same 1 bit interrupt line. To enable interrupt generate set any of this bit to 1.

ERRINTSIGEN	Bit	Description	Initial State
Reserved	[15:11]	Reserved	0
ENSIGBOOTACKERR	[10]	Boot Ack Error Signal Enable 1 = Enabled 0 = Masked	0
ENSIGADMAERR	[9]	ADMA Error Signal Enable 1 = Enabled 0 = Masked	0
ENSIGACMDERR	[8]	Auto CMD12 Error Signal Enable 1 = Enabled 0 = Masked	0
ENSIGCURERR	[7]	Current Limit Error Signal Enable This function is not implemented in this version. 1 = Enabled 0 = Masked	0
ENSIGDENDERR	[6]	Data End Bit Error Signal Enable 1 = Enabled 0 = Masked	0
ENSIGDATCRCERR	[5]	Data CRC Error Signal Enable 1 = Enabled 0 = Masked	0
ENSIGDATTOUTERR	[4]	Data Timeout Error Signal Enable 1 = Enabled 0 = Masked	0
ENSIGCMDIDXERR	[3]	Command Index Error Signal Enable 1 = Enabled 0 = Masked	0
ENSIGCMDEBITERR	[2]	Command End Bit Error Signal Enable 1 = Enabled 0 = Masked	0
ENSIGCMDCRCERR	[1]	Command CRC Error Signal Enable 1 = Enabled 0 = Masked	0
ENSIGCMDTOUTERR	[0]	Command Timeout Error Signal Enable	0

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ERRINTSIGEN	Bit	Description	Initial State
		1 = Enabled 0 = Masked	

NOTE: Detailed documents must be copied from SD Host Standard Specification.

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7.10.17 AUTOCMD12 ERROR STATUS REGISTER

7.10.17.1 Auto CMD12 Error Status Register

- ACMD12ERRSTS0, ROC, Address = 0xEB00_003C
- ACMD12ERRSTS1, ROC, Address = 0xEB10_003C
- ACMD12ERRSTS2, ROC, Address = 0xEB20_003C
- ACMD12ERRSTS3, ROC, Address = 0xEB30_003C

If Auto CMD12 Error Status is set, the Host Driver checks this register to identify what kind of error Auto CMD12 indicated. This register is valid if the Auto CMD12 Error is set.

ACMD12ERRSTS	Bit	Description	Initial State
Reserved	[15:8]	Reserved	0
STANCMDAER	[7]	Command Not Issued By Auto CMD12 Error If the bit is set to 1, it means CMD_wo_DAT is not executed due to an Auto CMD12 Error (D04-D01) in this register. 1 = Not Issued 0 = No error	0
Reserved	[6:5]	Reserved	0
STACMDIDXERR	[4]	Auto CMD12 Index Error Occurs if the Command Index error occurs in response to a command. 1 = Error 0 = No Error	0
STACMDEBITAER	[3]	Auto CMD12 End Bit Error Occurs it detects that the end bit of command response is 0. 1 = End Bit Error Generated 0 = No Error	0
STACMDCRCAER	[2]	Auto CMD12 CRC Error Occurs if it detects a CRC error in the command response. 1 = CRC Error Generated 0 = No Error	0
STACMDTOUTAER	[1]	Auto CMD12 Timeout Error Occurs if no response is returned within 64 SDCLK cycles from the end bit of command. If this bit is set to1, the other error status bits (D04-D02) are meaningless. 1 = Time out 0 = No Error	0
STANACMDAER	[0]	Auto CMD12 Not Executed If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. If this bit is set to 1, it means the Host Controller cannot issue Auto CMD12 to stop memory multiple block data transfer due to some error. If this bit is set to 1, other error status bits (D04-D01) are meaningless. 1 = Not executed 0 = Executed	0

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The relation between Auto CMD12 CRC Error and Auto CMD12 Timeout Error is shown below.

The relation between Command CRC Error and Command Timeout Error

Auto CMD12 CRC Error	Auto CMD12 Timeout Error	Kinds of Error
0	0	No Error
0	1	Response Timeout Error
1	0	Response CRC Error
1	1	CMD line conflict

The timing of changing Auto CMD12 Error Status is classified in three scenarios:

1. If the Host Controller is going to issue Auto CMD12
   - Set D00 to 1 if Auto CMD12 cannot be issued due to an error in the previous command.
   - Set D00 to 0 if Auto CMD12 is issued.
2. At the end bit of an Auto CMD12 response
   - Check received responses by checking the error bits D01, D02, D03 and D04.
   - Set to 1 if error is detected.
   - Set to 0 if error is not detected.
3. Before reading the Auto CMD12 Error Status bit D07
   - Set D07 to 1 if there is a command cannot be issued
   - Set D07 to 0 if there is no command to issue

Timing to generate the Auto CMD12 Error and writing to the Command register are asynchronous. Then D07 are sampled if driver never writes to the Command register. Therefore before reading the Auto CMD12 Error Status register, set the D07 status bit. Generates Auto CMD12 Error Interrupt if one of the error bits D00 to D04 is set to 1. The Command Not Issued by Auto CMD12 Error does not generate an interrupt.

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7.10.18 CAPABILITIES REGISTER

7.10.18.1 Capabilities Register

- CAPAREG0, HWInit, Address = 0xEB00_0040
- CAPAREG1, HWInit, Address = 0xEB10_0040
- CAPAREG2, HWInit, Address = 0xEB20_0040
- CAPAREG3, HWInit, Address = 0xEB30_0040

When HWINITFIN bit (CONTROL2 register) as 0, This register can be updated.

This register provides the Host Driver with information specific to the Host Controller implementation. The Host Controller implements these values as fixed or loaded from flash memory during power on initialization. Refer to Software Reset for the Software Reset register for loading from flash memory and completion timing control.

CAPAREG	Bit	Description	Initial State
Reserved	[31:27]	Reserved	
CAPAV18	[26]	Voltage Support 1.8V (HWInit) 1 = 1.8V Supported 0 = 1.8V Not Supported	1
CAPAV30	[25]	Voltage Support 3.0V (HWInit) 1 = 3.0V Supported 0 = 3.0V Not Supported	0
CAPAV33	[24]	Voltage Support 3.3V (HWInit) 1 = 3.3V Supported 0 = 3.3V Not Supported	1
CAPASUSRES	[23]	Suspend/Resume Support (HWInit) This bit indicates whether the Host Controller supports Suspend / Resume functionality. If this bit is 0, the Suspend and Resume mechanism are not supported and the Host Driver does not issue either Suspend or Resume commands. 1 = Supported 0 = Not Supported	1
CAPADMA	[22]	DMA Support (HWInit) This bit indicates whether the Host Controller is capable of using DMA to transfer data between system memory and the Host Controller directly. 1 = DMA Supported 0 = DMA Not Supported	1
CAPAHSPD	[21]	High Speed Support (HWInit) This bit indicates whether the Host Controller and the Host System support High Speed mode and they can supply SD Clock frequency from 25MHz to 50MHz. 1 = High Speed Supported 0 = High Speed Not Supported	1
Reserved	[20]	Reserved	0
CAPAADMA2	[19]	ADMA2 Support	1

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CAPAREG	Bit	Description	Initial State
		This bit indicates whether the Host Controller is capable of using ADMA2. 1 = ADMA2 Support 0 = ADMA2 not Support	
Reserved	[28]	Reserved	0
CAPAMAXBLKLEN	[17:16]	Max Block Length (HWInit) This value indicates the maximum block size that the Host Driver can read and write to the buffer in the Host Controller. The buffer transfers this block size without wait cycles. Three sizes are defined as indicated below. 00 = 512-byte 01 = 1024-byte 10 = 2048-byte 11 = Reserved	0
Reserved	[15:14]	Reserved	0
CAPABASECLK	[13:8]	Base Clock Frequency For SD Clock (HWInit) This value indicates the base (maximum) clock frequency for the SD Clock. Unit values are 1MHz. If the real frequency is 16.5MHz, the lager value is set to 01 0001b (17MHz) because the Host Driver use this value to calculate the clock divider value (Refer to the SDCLK Frequency Select in the Clock Control register.) and it does not exceed upper limit of the SD Clock frequency. The supported clock range is 10MHz to 63MHz. If these bits are all 0, the Host System has to get information via another method. Not 0 = 1MHz to 63MHz 000000b = Get information via another method	0
CAPATOUTUNIT	[7]	Timeout Clock Unit (HWInit) This bit shows the unit of base clock frequency used to detect Data Timeout Error. 0 = kHz 1 = MHz	1
Reserved	[6]	Reserved	0
CAPATOUTCLK	[5:0]	Timeout Clock Frequency (HWInit) This bit shows the base clock frequency used to detect Data Timeout Error. The Timeout Clock Unit defines the unit of this field value. Timeout Clock Unit =0 [kHz] unit: 1kHz to 63kHz Timeout Clock Unit =1 [MHz] unit: 1MHz to 63MHz Not 0 = 1kHz to 63kHz or 1MHz to 63MHz 00 0000b = Get information via another method	0

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7.10.19 MAXIMUM CURRENT CAPABILITIES REGISTER

7.10.19.1 Maximum Current Capabilities Register

- MAXCURR0, HWInit, Address = 0xEB00_0048
- MAXCURR1, HWInit, Address = 0xEB10_0048
- MAXCURR2, HWInit, Address = 0xEB20_0048
- MAXCURR3, HWInit, Address = 0xEB30_0048

When HWINITFIN bit (CONTROL2 register) as 0, This register can be updated.

These registers indicate maximum current capability for each voltage. The value is meaningful if Voltage Support is set in the Capabilities register. If this information is supplied by the Host System via another method, all Maximum Current Capabilities register will be 0.

MAXCURR	Bit	Description	Initial State
Reserved	[31:24]	Reserved	
MAXCURR18	[23:16]	Maximum Current for 1.8V (HWInit)	0
MAXCURR30	[15:8]	Maximum Current for 3.0V (HWInit)	0
MAXCURR33	[7:0]	Maximum Current for 3.3V (HWInit)	0

This register measures current in 4mA steps. Each voltage level's current support is described using the Table below.

Maximum Current Value Definition

Register Value	Current Value
0	Get information via another method
1	4mA
2	8mA
3	12mA
…	…
255	1020mA

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7.10.20 FORCE EVENT REGISTER FOR AUTO CMD12 ERROR STATUS

7.10.20.1 Force Event Auto CMD12 Error Interrupt Register

- FEAER0, W, Address = 0xEB00_0050
- FEAER1, W, Address = 0xEB10_0050
- FEAER2, W, Address = 0xEB20_0050
- FEAER3, W, Address = 0xEB30_0050

The Force Event Register is not a physically implemented register. Rather, it is an address at which the Auto CMD12 Error Status Register can be written.

Warning: 1: set each bit of the Auto CMD12 Error Status Register
0: no effect

- D15 D12

FEAER	Bit	Description	Initial State
Reserved	[15:8]	Reserved	0x0
FENCMDAER	[7]	Force Event for Command Not Issued By Auto CMD12 Error 1 = Generates Interrupt 0 = No Interrupt	0
Reserved	[6:5]	Reserved	0
FECMDIDXERR	[4]	Force Event for Auto CMD12 Index Error 1 = Interrupt 0 = No Interrupt	0
FECMDEBITAER	[3]	Force Event for Auto CMD12 End Bit Error 1 = Generates Interrupt 0 = No Interrupt	0
FECMDCRCAER	[2]	Force Event for Auto CMD12 CRC Error 1 = Generates Interrupt 0 = No Interrupt	0
FECMDTOUTAER	[1]	Force Event for Auto CMD12 Timeout Error 1 = Generates Interrupt 0 = No Interrupt	0
FENACMDAER	[0]	Force Event for Auto CMD12 Not Executed 1 = Generates Interrupt 0 = No Interrupt	0

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7.10.21 FORCE EVENT REGISTER FOR ERROR INTERRUPT STATUS

7.10.21.1 Force Event Error Interrupt Register Error Interrupt

- FEERR0, W, Address = 0xEB00_0052
- FEERR1, W, Address = 0xEB10_0052
- FEERR2, W, Address = 0xEB20_0052
- FEERR3, W, Address = 0xEB30_0052

The Force Event Register is not a physically implemented register. Rather, it is an address at which the Error Interrupt Status register is written. The effect of a write to this address is reflected in the Error Interrupt Status Register if the corresponding bit of the Error Interrupt Status Enable Register is set.

Warning: 1: set each bit of the Error Interrupt Status Register
0: no effect

NOTE: By setting this register, the Error Interrupt can be set in the Error Interrupt Status register. In order to generate interrupt signal, both the Error Interrupt Status Enable and Error Interrupt Signal Enable must be set.

FEERR	Bit	Description	Initial State
Reserved	[15:11]	Reserved	0x0
FEBOOTACKERR	[10]	Force Event for Boot Ack Error 1 = Interrupt is generated 0 = No Interrupt	0
FEADMAERR	[9]	Force Event for ADMA Error 1 = Generates Interrupt 0 = No Interrupt	0
FEACMDERR	[8]	Force Event for Auto CMD12 Error 1 = Generates Interrupt 0 = No Interrupt	0
Reserved	[7]	Reserved	0
FEDENDERR	[6]	Reserved	0
FEDATCRCERR	[5]	Force Event for Data CRC Error 1 = Generates Interrupt 0 = No Interrupt	0
FEDATTOUTERR	[4]	Force Event for Data Timeout Error 1 = Generates Interrupt 0 = No Interrupt	0
FECMDIDXERR	[3]	Force Event for Command Index Error 1 = Generates Interrupt 0 = No Interrupt	0
FECMDEBITERR	[2]	Force Event for Command End Bit Error 1 = Generates Interrupt 0 = No Interrupt	0

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FEERR	Bit	Description	Initial State
FECMDCRCERR	[1]	Force Event for Command CRC Error 1 = Generates Interrupt 0 = No Interrupt	0
FECMDTOUTERR	[0]	Force Event for Command Timeout Error 1 = Generates Interrupt 0 = No Interrupt	0

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7.10.22 ADMA ERROR STATUS REGISTER

7.10.22.1 ADMA Error Status Register

- ADMAERR0, R/W, Address = 0xEB00_0054
- ADMAERR1, R/W, Address = 0xEB10_0054
- ADMAERR2, R/W, Address = 0xEB20_0054
- ADMAERR3, R/W, Address = 0xEB30_0054

If ADMA Error Interrupt occurs, the ADMA Error States field in this register holds the ADMA state and the ADMA System Address Register holds the address around the error descriptor. For recovering the error, the Host Driver requires the ADMA state to identify the error descriptor address as follows:

- ST_STOP: Previous location set in the ADMA System Address register is the error descriptor address
- ST_FDS: Current location set in the ADMA System Address register is the error descriptor address
- ST_CADR: This sate is never set because do not generate ADMA error in this state.
- ST_TFR: Previous location set in the ADMA System Address register is the error descriptor address

In case of write operation, the Host Driver should use ACMD22 to get the number of written block rather than using this information, since unwritten data may exist in the Host Controller.

The Host Controller generates the ADMA Error Interrupt if it detects invalid descriptor data (Valid = 0) at the ST_FDS state. In this case, ADMA Error State indicates that an error occurs at ST_FDS state. The Host Driver finds that the Valid bit is not set in the error descriptor.

ADMAERR	Bit	Description	Initial State
Reserved	[31:11]	Reserved	0x00
STAADMAFINBLK	[10]	ADMA Final Block Transferred (ROC) In ADMA operation mode, this field is set to High if the Transfer Complete condition and the block are final (no block transfer remains). If this bit is Low when the Transfer Complete condition and Transfer Complete is done due to the Stop at Block Gap, so data to be transferred still remains.	0
ADMACONTREQ	[9]	ADMA Continue Request (WO) If the stop state by ADMA Interrupt, ADMA operation set this bit to HIGHT to continue.	0
ADMASTAINT	[8]	ADMA Interrupt Status (RW1C) This bit is set to HIGH if INT attribute in the ADMA Descriptor Table is asserted. This bit is not affected by ADMA error interrupt.	0
	[7:3]	Reserved	0
ADMALENMISERR	[2]	ADMA Length Mismatch Error This error occurs in the following 2 cases. (1) While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length.	00

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ADMAERR	Bit	Description	Initial State
		(2) Total data length can not be divided by the block length. 0 = No Error 1 = Error	
ADMAERRST	[1:0]	ADMA Error State This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. D01 - D00 ADMA Error State when error is occurred Contents of SYS_SDR register 00 = ST_STOP (Stop DMA) Points next of the error descriptor 01 = ST_FDS (Fetch Descriptor) Points the error descriptor 10 = Never set this state (Not used) 11 = ST_TFR (Transfer Data) Points the next of the error descriptor	0

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7.10.23 ADMA SYSTEM ADDRESS REGISTER

7.10.23.1 ADMA System Address Register

- ADMASYSADDR0, R/W, Address = 0xEB00_0058
- ADMASYSADDR1, R/W, Address = 0xEB10_0058
- ADMASYSADDR2, R/W, Address = 0xEB20_0058
- ADMASYSADDR3, R/W, Address = 0xEB30_0058

This register contains the physical Descriptor address used for ADMA data transfer.

ADMASYSADDR	Bit	Description	Initial State
ADMASYSAD	[31:0]	ADMA System Address This register holds byte address of executing command of the Descriptor table. 32-bit Address Descriptor uses lower 32-bit of this register. At the start of ADMA, the Host Driver sets start address of the Descriptor table. The ADMA increments this register address, which points to next line, if having fetched a Descriptor line. If the ADMA Error Interrupt is generated, this register holds valid Descriptor address depending on the ADMA state. The Host Driver programs Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. ADMA2 ignores lower 2-bit of this register and assumes it to be 00b. 32-bit Address ADMA Register Value 32-bit System Address xxxxxxxx 00000000h 00000000h xxxxxxxx 00000004h 00000004h xxxxxxxx 00000008h 00000008h xxxxxxxx 0000000Ch 0000000Ch …… …… xxxxxxxx FFFFFFFCh FFFFFFFCh Note: The data length of the ADMA Descriptor Table should be the word unit (multiple of the 4-byte).	00

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7.10.24 CONTROL REGISTER 2

7.10.24.1 Control Register 2

- CONTROL2_0, R/W, Address = 0xEB00_0080
- CONTROL2_1, R/W, Address = 0xEB10_0080
- CONTROL2_2, R/W, Address = 0xEB20_0080
- CONTROL2_3, R/W, Address = 0xEB30_0080

This register contains the SD Command Argument.

CONTROL2	Bit	Description	Initial State
ENSTAASYNCCLR	[31]	Write Status Clear Async Mode Enable This bit makes async-clear enable about Normal and Error interrupt status bit. During the initialization procedure command operation, this bit should be enabled. 0 = Disable 1 = Enable	0
ENCMDCNFMSK	[30]	Command Conflict Mask Enable This bit can mask enable the Command Conflict Status (bit [1:0] of the "ERROR INTERRUPT STATUS REGISTER") 0 = Mask Disable 1 = Mask Enable Note: If the OUTEDGEINV field in the Host Control Register is set (High Speed data transfer), this field should be enabled to prevent from command conflict status alarm.	0
Reserved	[29]	Reserved (must be 1'b0)	0
SELCARDOUT	[28]	Card Removed Condition Selection 0 = Card Removed condition is "Not Card Insert" State (When the transition from "Card Inserted" state to "Debouncing" state in *Figure 7-17*) 1 = Card Removed state is "Card Out" State (If the transition from "Debouncing" state to "No Card" state in *Figure 7-17*)	0
FLTCLKSEL	[27:24]	Filter Clock (iFLTCLK) Selection Filter Clock period = 2^(FltClkSel + 5) x iSDCLK period 0000 = 25 x iSDCLK 0001 = 26 x iSDCLK … 1111 = 220 x iSDCLK	0
LVLDAT	[23:16]	DAT line level Bit[23]=DAT[7], BIT[22]=DAT[6], BIT[21]=DAT[5], BIT[20]=DAT[4], Bit[19]=DAT[3], BIT[18]=DAT[2], BIT[17]=DAT[1], BIT[16]=DAT[0] (Read Only)	Line state
ENFBCLKTX	[15]	Feedback Clock Enable for Tx Data/Command Clock 0 = Disable 1 = Enable	0

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CONTROL2	Bit	Description	Initial State
ENFBCLKRX	[14]	Feedback Clock Enable for Rx Data/Command Clock 0 = Disable 1 = Enable	0
Reserved	[13]	Reserved (must be 1'b0)	0
SDOPSIGPC	[12]	SD Output Signal Power Control Support If set this field is enables output CMD and DAT referencing SD Bus Power bit in the "PWRCON register". 0 = CMD and DAT outputs are not controlled by SD Bus Power bit 1 = CMD and DAT outputs are controlled(masked) by SD Bus Power bit Note: This function is not implemented in this version.	0
ENBUSYCHKTXSTART	[11]	CE-ATA I/F mode Busy state check before Tx Data start state 0 = Disable 1 = Enable	0
DFCNT	[10:9]	Debounce Filter Count Debounce Filter Count setting register for Card Detect signal input (SDCD#) 00 = No use debounce filter 01 = 4 x iFLTCLK 10 = 16 x iFLTCLK 11 = 64 x iFLTCLK	0
ENCLKOUTHOLD	[8]	SDCLK Hold Enable Enter and exit of the SDCLK Hold state is done by Host Controller. 0 = Disable 1 = Enable Note: This field should be 1.	0
RWAITMODE	[7]	Read Wait Release Control 0 = Read Wait state is released by the Host Controller (Auto) 1 = Read Wait state is released by the Host Driver (Manual)	0
DISBUFRD	[6]	Buffer Read Disable 0 = Normal mode, user can read buffer(FIFO) data using 0x20 register 1 = User cannot read buffer(FIFO) data using 0x20 register. In this case, the buffer memory is read through memory area (Debug purpose).	0
SELBASECLK	[5:4]	Base Clock Source Select 00 or 01 = HCLK 10 = SCLK_MMC0~3 (from SYSCON), 11 = Reserved	00

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CONTROL2	Bit	Description	Initial State
SDINPSIGPC	[3]	SD Input Signal Power Control Support If set this field enables input CMD and DAT referencing SD Bus Power bit in the "PWRCON register". 0 = No Sync, no switch input enable signal (Command, Data) 1 = Sync, control input enable signal (Command, Data) Note: This function is not implemented in this version.	0
Reserved	[2]	Reserved	0
ENCLKOUTMSKCON	[1]	SDCLK output clock masking when Card Insert cleared If this field is High, it is used not to stop SDCLK if No Card state. 0 = Disable 1 = Enable	0
HWINITFIN	[0]	SD Host Controller Hardware Initialization Finish 0 = Not Finish 1 = Finish	0

NOTE:

1. Ensure to set SDCLK Hold Enable (EnSCHold) if the card does not support Read Wait to guarantee for Receive data not overwritten to the internal FIFO memory.
2. CMD_wo_DAT issue is prohibited during READ transfer if SDCLK Hold Enable is set.

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7.10.25 CONTROL REGISTERS 3 REGISTER

7.10.25.1 FIFO Interrupt Control (Control Register 3)

- CONTROL3_0, R/W, Address = 0xEB00_0084
- CONTROL3_1, R/W, Address = 0xEB10_0084
- CONTROL3_2, R/W, Address = 0xEB20_0084
- CONTROL3_3, R/W, Address = 0xEB30_0084

CONTROL3	Bit	Description	Initial State
FCSEL3	[31]	Feedback Clock Select [3] Reference (1)	0x0
FIA3	[30:24]	FIFO Interrupt Address register 3 FIFO (512Byte Buffer memory, word address unit) Initial value (0x7F) generates at 512-byte(128-word) position.	0x7F
FCSEL2	[23]	Feedback Clock Select [2] Reference (1)	0x0
FIA2	[22:16]	FIFO Interrupt Address register 2 FIFO (512Byte Buffer memory, word address unit) Initial value (0x5F) generates at 384-byte(96-word) position.	0x5F
FCSEL1	[15]	Feedback Clock Select [1] Reference (2)	0x0
FIA1	[14:8]	FIFO Interrupt Address register 1 FIFO (512Byte Buffer memory, word address unit) Initial value (0x3F) generates at 256-byte(64-word) position.	0x3F
FCSEL0	[7]	Feedback Clock Select [0] Reference (2)	0x0
FIA0	[6:0]	FIFO Interrupt Address register 0 FIFO (512Byte Buffer memory, word address unit) Initial value (0x1F) generates at 128-byte(32-word) position.	0x1F

NOTE:

1. FCSel[3:2] : Tx Feedback Clock Delay Control : Inverter delay means 10ns delay if SDCLK 50MHz setting '00', '01' = Inverter delay, '10', '11' = basic delay(aroujnd 2ns)
2. FCSel[1:0] : Rx Feedback Clock Delay Control : Inverter delay means10ns delay if SDCLK 50MHz setting '00', '01' = Inverter delay, '10', '11' = basic delay(aroujnd 2ns)
3. Tx Feedback inversion setting (FCSel[3:2] = '00' or '01'), Tx Feedback clock enable (ENFBCLKTX = 0) and Normal Speed mode (OUTEDGEINV = 0) setting make Tx data transfer mismatch (Do not set).

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7.10.26 CONTROL REGISTER 4

7.10.26.1 Control Register 4

- CONTROL4_0, R/W, Address = 0xEB00_008C
- CONTROL4_1, R/W, Address = 0xEB10_008C
- CONTROL4_2, R/W, Address = 0xEB20_008C
- CONTROL4_3, R/W, Address = 0xEB30_008C

CONTROL4	Bit	Description	Initial State
Reserved	[31:18]	Reserved	0
SELCLKPADDS	[17:16]	SD Clock Output PAD Drive Strength Select 00 = 2mA 01 = 4mA 10 = 7mA 11 = 9mA Note: This function is not implemented in this version.	0x3
Reserved	[15:2]	Reserved	-
STABLKGAPBUSY	[1]	Status Block Gap Access Busy This bit is "High" when the clock domain crossing (HCLK to SDCLK) operation is processing when the write operation to the BLKGAP register. This bit is status bit and Read Only (RO)	0
STABUSY	[0]	Status Busy This bit is "High" if the clock domain crossing (HCLK to SDCLK) operation is under process. This bit is status bit and Read Only (RO)	0

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7.10.27 HOST CONTROLLER VERSION REGISTER

7.10.27.1 Host Controller Version Register

- HCVER0, HWInit, Address = 0xEB00_00FE
- HCVER1, HWInit, Address = 0xEB10_00FE
- HCVER2, HWInit, Address = 0xEB20_00FE
- HCVER3, HWInit, Address = 0xEB30_00FE

This register contains the SD Command Argument.

HCVER	Bit	Description	Initial State
VENVER	[15:8]	Vendor Version Number This status is reserved for the vendor version number. The Host Driver should not use this status. 0x24: SDMMC4.2 Host Controller	0x24
SPECVER	[7:0]	Specification Version Number This status indicates the Host Controller Specification. Version. The upper and lower 4-bits indicate the version 00 = SD Host Specification Version 1.0 01 = SD Host Specification Version 2.0 Including the feature of the ADMA and Test Register Others = Reserved	0x01

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8 TRANSPORT STREAM INTERFACE

8.1 OVERVIEW OF TRANSPORT STREAM INTERFACE

The Transport Stream Interface (TSI) in S5PV210 receives transport stream data from channel chip, which it writes to a specific address of the output buffer (SDRAM). Depending on the bus bandwidth, TSI has 32 words FIFO.

Using word-aligned address, the TSI sends data streams to the output buffer (SDRAM). One packet size is equal to 47 words. The output buffer size should be equal to a multiple of 47 words (one packet size).

If the data is written in the output buffer, the SDRAM full interrupt occurs.

8.1.1 KEY FEATURES OF TRANSPORT STREAM INTERFACE

- Writes transport stream received from channel chip to output buffer (supports 1-/ 4-/ 8-beat burst, word-aligned)
- Supports TS interface in DVB-H/ DVB-T/ ISDB-T/ T-DMB/ DAB mode
- Supports TS_CLK falling/ rising edge data fetch mode
- Supports active high or active low mode for TS signals (TS_VALID, TS_SYNC, and TS_ERROR)
- Supports MSB to LSB or LSB to MSB data byte order
- Specifies the maximum size of output buffer for store transport stream as 256KBytes
- Supports two sync detecting modes:
  - TS_SYNC signal
  - Sync byte
- Supports PID filter mode with 32 PID filters
- Supports six error cases with SKIP/ STOP mode
- Supports TS_CLK filter.
  - TS_CLK maximum frequency
    - with TS_CLK filter: ~ 1/2 HCLK
    - without TS_CLK filter: ~ 1/4 HCLK

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8.1.2 BROADCAST MODE

TSI supports DVB-H, DVB-T, ISDB-T, T-DMA, and DAB modes. *Figure 8-1* shows an example of the broadcasting support scheme.

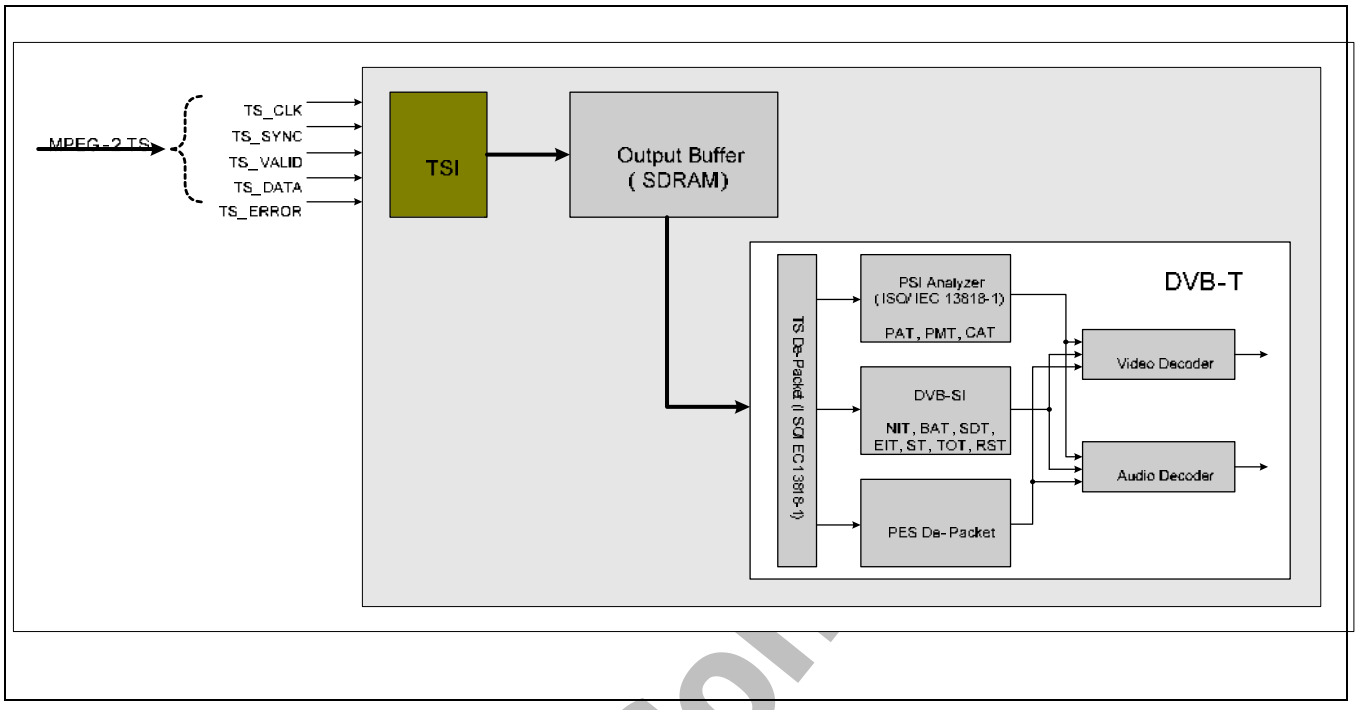

Figure 8-1 Support TSI in the Broadcasting Mode

The MPEG-2 transport stream contains a set of service information for program specific information (PSI). The transport stream is injected from an external channel chip and TSI stores it into output buffer. Then, TS De-Packet, PSI Analyzer, DVB-SI, and PED De-Packet blocks de-multiplex individual PSI from the transport stream and transfer it to audio and video decoders.

PSI comprises of Program Association Table (PAT), Program Map Table (PMT), and Conditional Access Table (CAT), defined in MPEG-2.

- PAT: Transmits the PID information of PMT and NID, and information about various service offering in transmitter.
- PMT: Transmit the PID information of transmit port packet and PCR information transferred with various services.
- CAT: Transmits information for charging broadcasting system used in transmitter.

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Table 8-1 shows the characteristics of several mobile-TV standard modes.

Table 8-1 Characteristics of Several Mobile-TV Standard Modes

Mobile TV Standard	Video Codec	Characteristics
DVB-T	MPEG-2	MP@ML 10Mbps, 720*480 @30fps
DVB-H	H.264	Up to Baseline 352*288 @15fps @384kbps
	WMV9	Up to SP @ML 356*288 @15fps @384kbps
T-DMB	H.264	Up to Baseline Profile 352*288 @30fps @768kbps
ISDB-T	H.264	Up to Baseline Profile 320*240 @15fps @384kbps

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8.1.3 BLOCK DIAGRAM OF TS INTERFACE

Figure 8-2 shows the overall functional block diagram of TS Interface.

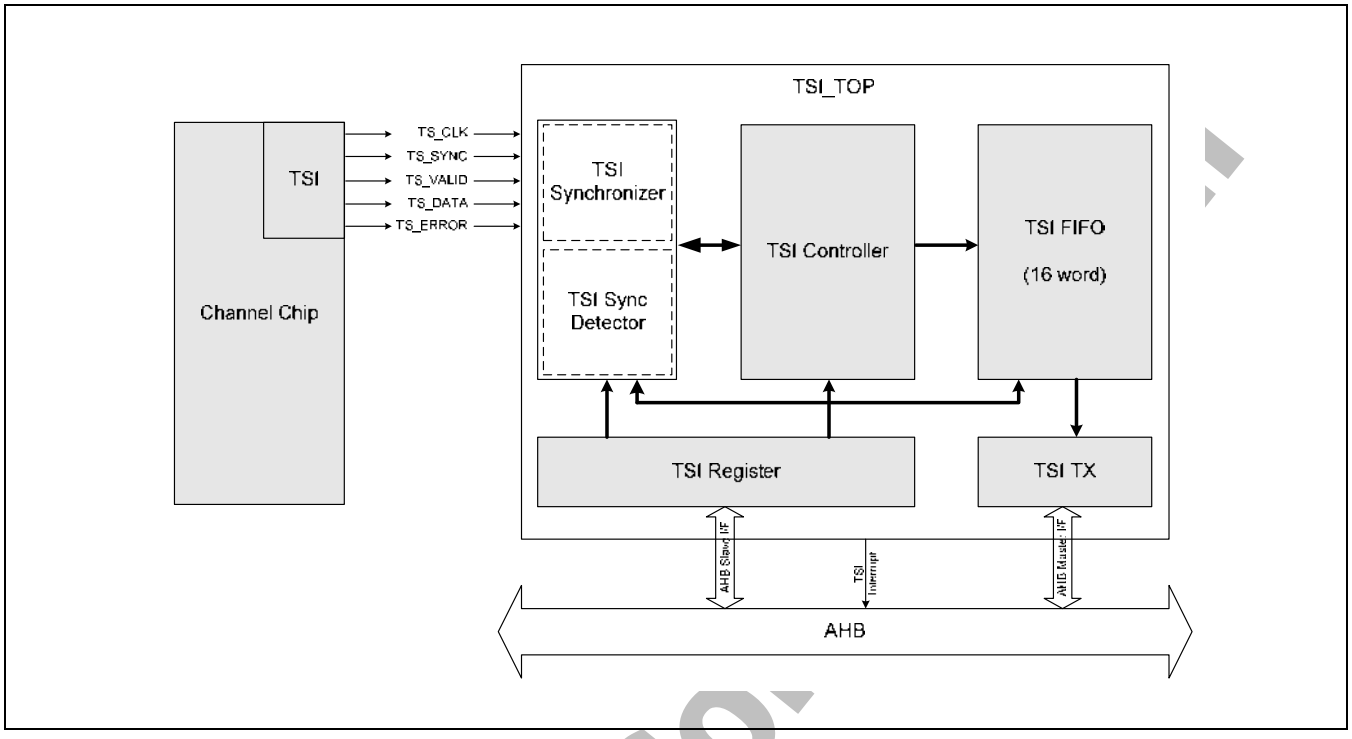

Figure 8-2 TSI Block Diagram

The transport stream data is transferred from an external channel chip via five signals such as TS_CLK, TS_SYNC, TS_VALID, TS_DATA, and TS_ERROR. TSI controller receives transport stream data by capturing the five signals with TSI synchronizer and TSI sync detector. The received transport stream data is stored on TSI FIFO, and TSI TX module transfers the transport stream data into output buffer using AHB master interface. User can control operations of TSI by setting TSI registers via AHB slave interface.

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8.1.4 I/O DESCRIPTION OF TSI

Table 8-2 describes the I/O ports of TSI.

Table 8-2 TSI I/O Description

Port Name	I/O	Description (Primary Function)	Source/ Destination
ts_clk	DI	Specifies the TSI system clock (66MHz).	Channel chip/ Buffer
ts_sync	DI	Specifies the TSI synchronization control signal.	Channel chip/ Buffer
ts_val	DI	Specifies the TSI valid signal.	Channel chip/ Buffer
ts_data	DI	Specifies the TSI input data.	Channel chip/ Buffer
ts_error	DI	Specifies the TSI error indicate signal.	Channel chip/ Buffer

, where

- DI - Digital Input Signal

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8.1.5 FUNCTIONAL DESCRIPTION

8.1.5.1 TSI Operation

The TS packet has a total of 188 bytes and it consists of the header, adaptation field, and payload. The TS header includes a packet identifier (PID), sync byte, and several control signals (such as transport scrambling, adaptation field, and continuity control). *Figure 8-3* shows the transport stream packet data format.

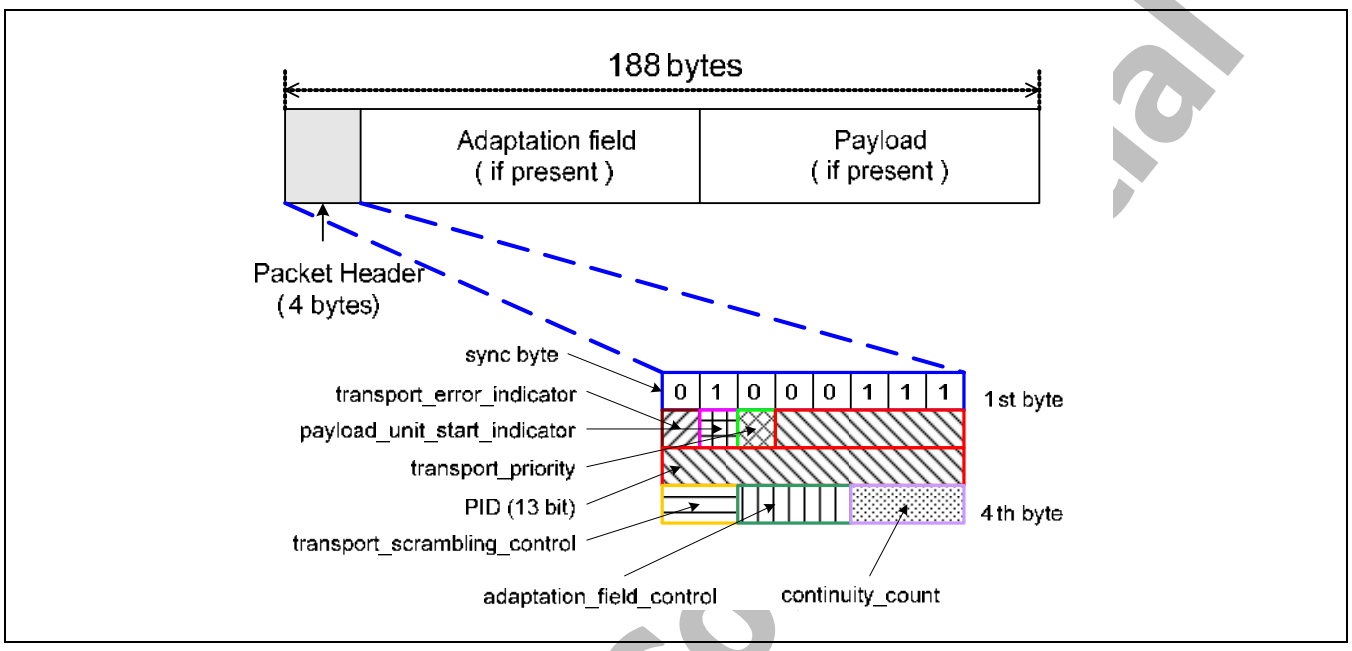

Figure 8-3 Transport Stream Packet Data Format

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8.1.5.2 Transport Stream Signals

You can set the transport stream signals (TS_CLK, TS_SYNC, TS_VALID, TS_ERROR, and TS_DATA) as active-high or active-low. The active mode of each signal can be set independently. *Figure 8-4* shows the timing diagram of transport stream signals and describes the timing operation of each signal.

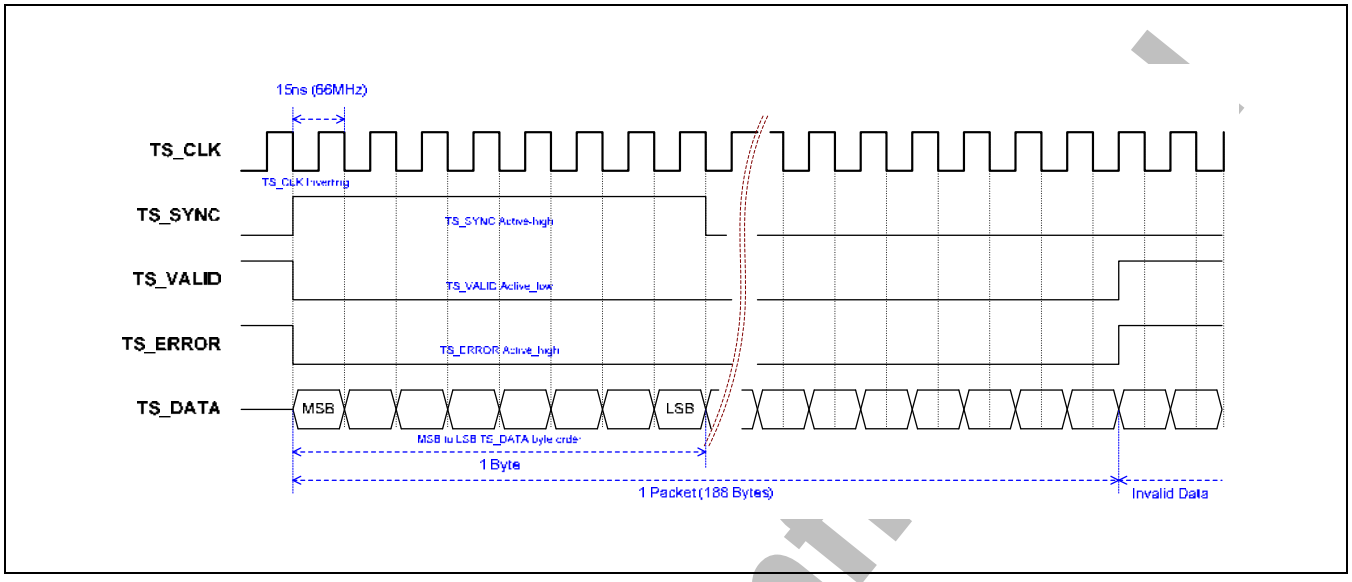

Figure 8-4 Transport Stream Signals

8.1.5.3 Sync Detection

The sync detection of transport stream is done using TS_SYNC signal and sync byte.

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8.1.5.3.1 Using TS_SYNC Signal

The sync detection of transport stream using TS_SYNC signal is done by:

- Considering the consecutive 8-bits TS_SYNC signal
- Observing only 1-bit TS_SYNC signal

Figure 8-5 shows the sync detection using TS_SYNC signal.

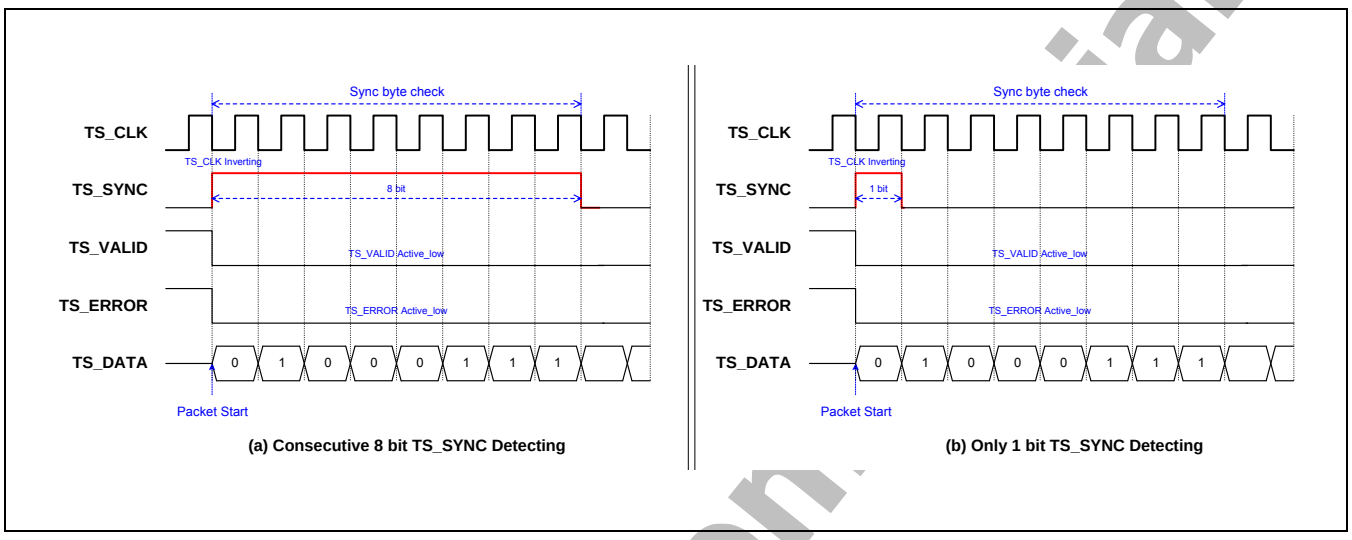

Figure 8-5 Sync Detection using TS_SYNC Signal

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8.1.5.3.2 Using Sync Byte

When sync detection using sync byte (0x47) is done, the 0x47 value is transferred in the middle of transport stream. This value can be wrongly recognized as the starting point of the packet. To prevent this situation, when the sync byte is set at TSI sync control register (sync_det_cnt (0~15)), TSI recognizes it as the starting point of the packet.

Three data counters and three current sync detecting counters are used in the TSI module. The current sync detecting counter displays the sync byte that is inputted up to that time. The data detecting counter displays the size of the transferring transport stream after the sync byte is inputted.

Consider that data counter is equal to 187 bytes. If the sync byte is inputted, it initializes the data counter by zero and increases the sync detecting counter by one. On the other hand, if the inputted data is not the sync byte, it disables the data counter and initializes the sync detecting counter by zero.

Consider the enabled total data counter to be less than 187. If the sync byte is inputted, it enables the data counter and increases the related sync detecting counter by one.

If the register value of one among the three sync detecting counters is the same as the value of TSI sync control register (sync_det_cnt), the sync detecting operation is completed.

Figure 8-6 shows the example of the sync detecting operation.

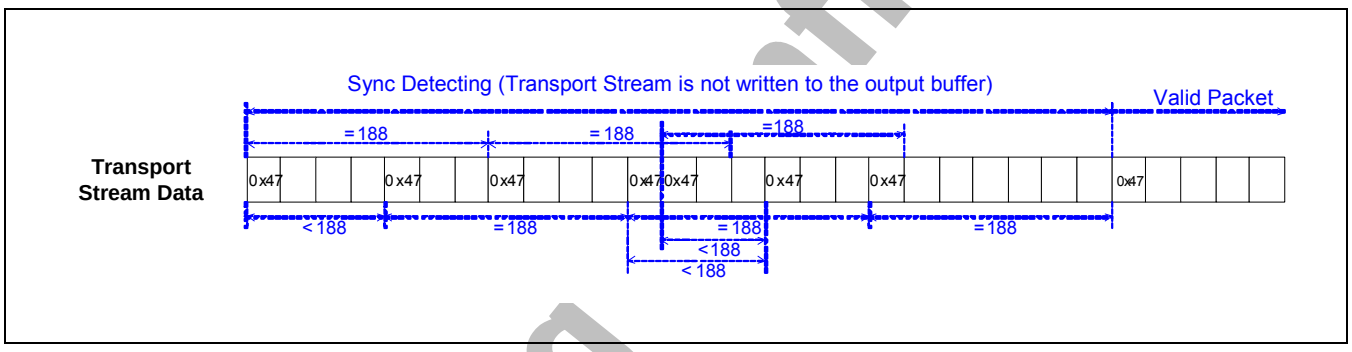

Figure 8-6 Sync Detection using Sync Byte (sync_det_cnt = 3)

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Table 8-3 shows the process of the sync detecting operation.

Table 8-3 Sync Detection Process using Sync Byte (sync_det_cnt = 3)

	Condition	Data Count	Sync Detecting Count
-	Sync detecting idle	All data count disabled	All sync detecting count set to 0
1	Sync byte input	Data count1 enabled	csdc1 = 1
2	Sync byte input, data count1 < 187	Data count2 enabled	csdc2 = 1
3	Sync byte input, data count1 == 187	Data count1 set to 0	csdc1 = 2
4	Sync byte input, data count2 == 187	Data count2 set to 0	csdc2 = 2
5	Sync byte input, data count1 < 187, data count2 < 187	Data count3 enabled	csdc3 = 1
6	Sync byte not input, data count1 == 187	Data count1 disabled	csdc1 = 0
7	Sync byte input, data count2 < 187, data count3 < 187	Data count1 enabled	csdc1 = 1
8	Sync byte input, data count2 == 187	Data count2 set to 0	csdc2 = 3
9	Sync byte not input, data count3 == 187	Data count3 disabled	csdc3 = 0
10	Sync byte input, data count2 == 187	Data count2 set to 0	csdc2 == 4. sync detecting complete

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8.1.5.4 Error Detection

TSI can generate six errors, as shown in *Table 8-4*. Each error occurs at the SKIP or STOP mode.

Whenever an error occurs at the SKIP mode, TSI generates an interrupt. Only after fixing the error (Padding or Skip) at the packet where the error occurred, TSI will continue to send data streams to the output buffer.

Whenever an error occurs at the STOP mode, TSI generates an interrupt and stops sending data streams to the output buffer.

In case the error is caused by SKIP or STOP mode in the TSI control register, the interrupt flag in TSI interrupt register is set to 1.

If the TSI mask register is enabled and if an error occurs, the error interrupt signal is sent to the MCU.

Table 8-4 Sync Detection Process using Sync Byte (sync_det_cnt = 3)

#	Error case		Description
1	Sync mismatch (only in TS_SYNC mode)		Sync byte is not received at the start of packet
2	Packet size underflow (only in TS_SYNC mode)		TS_SYNC signal is activated when the packet reception does not end
3	Packet size overflow	TS_SYNC mode	TS_SYNC signal is deactivated at the start of packet
		Sync byte mode	Sync byte is not received at the start of packet
4	TS_ERROR	Bit detecting	TS_ERROR signal is activated when the packet reception is operating.
		Packet detecting	TS_ERROR signal is activated for receiving one packet (Packet data is written to the OUTPUT buffer. Only error flag is generated).
5	TS_CLK timeout (only STOP mode)		TS_CLK is not toggled for n-cycles of HCLK (n is determined by 'TSI CLOCK COUNT register')
6	Internal FIFO full (only STOP mode)		Internal FIFO is filled with received data

Figure 8-7 shows the timing diagram of several TSI error cases. *Figure 8-7* -(a) describes the sync mismatch case. Figure 8-7 -(b) describes the packet size underflow case. Figure 8-7 -(c) and Figure 8-7 -(d) describe the packet size overflow case. Figure 8-7 -(e), Figure 8-7 -(f), and Figure 8-7 -(g) describe the ts_error case.

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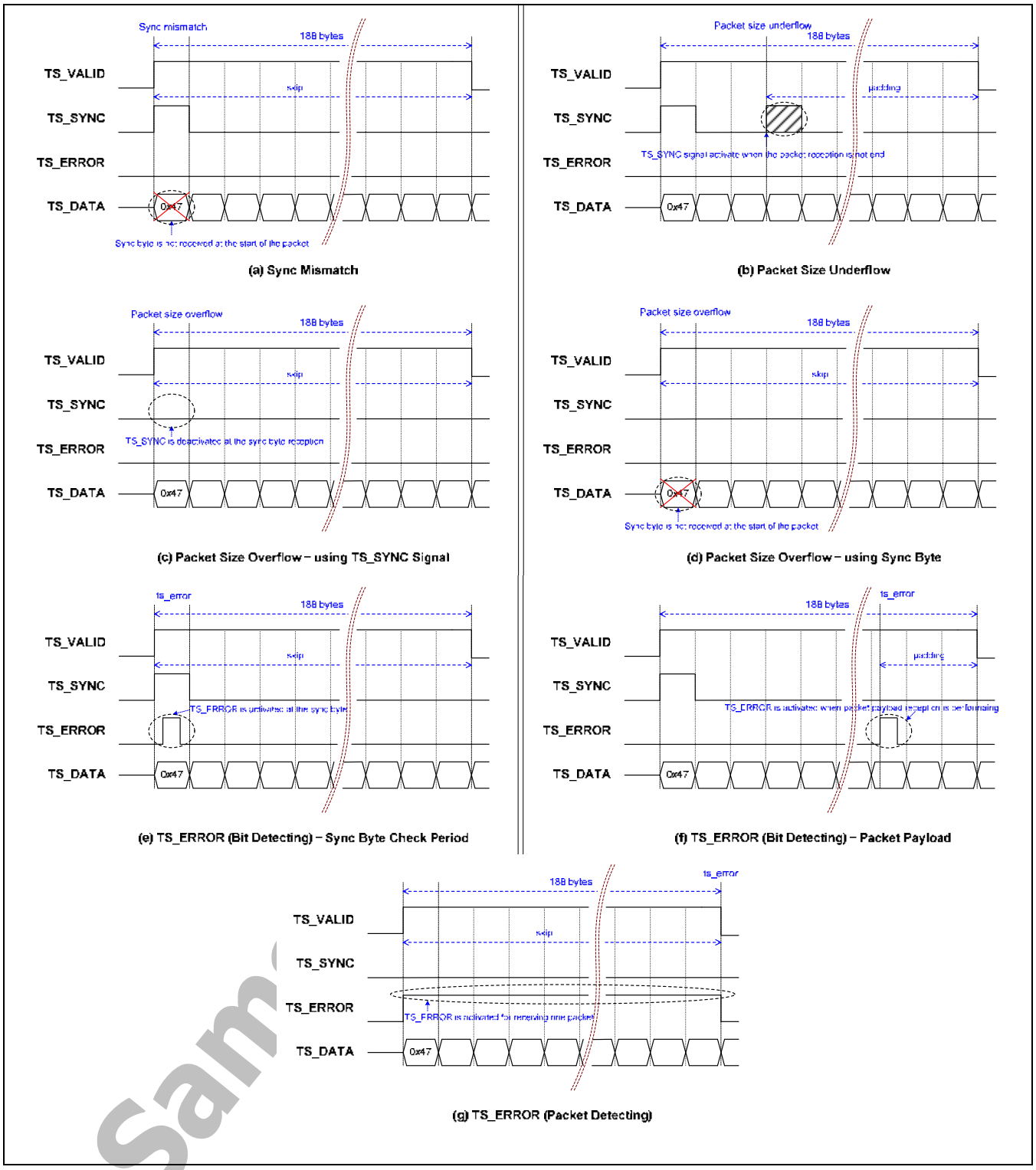

Figure 8-7 TSI Error Cases (with SKIP mode, TS_VALID / TS_SYNC / TS_ERROR is active high)

8.1.5.5 TS_CLK Filter

When HCLK maintains the same level as TS_CLK at the rising edge during two consecutive clock cycles, TS_CLK filter considers TS_CLK as valid.

In case TS_CLK filter is used, a half-period of the TS_CLK should have two or more periods of HCLK. The maximum frequency of TS_CLK will change depending on whether TS_CLK passes two-stage flip-flops (noise filter is disabled) or TS_CLK passes three-stage flip-flops (noise filter is enabled).

If HCLK with an operating frequency of 132MHz is used, the maximum frequency of TS_CLK is limited by 66MHz (without TS_CLK filter) and 33MHz (with TS_CLK filter). *Figure 8-8* shows the block diagram of TS_CLK filter.

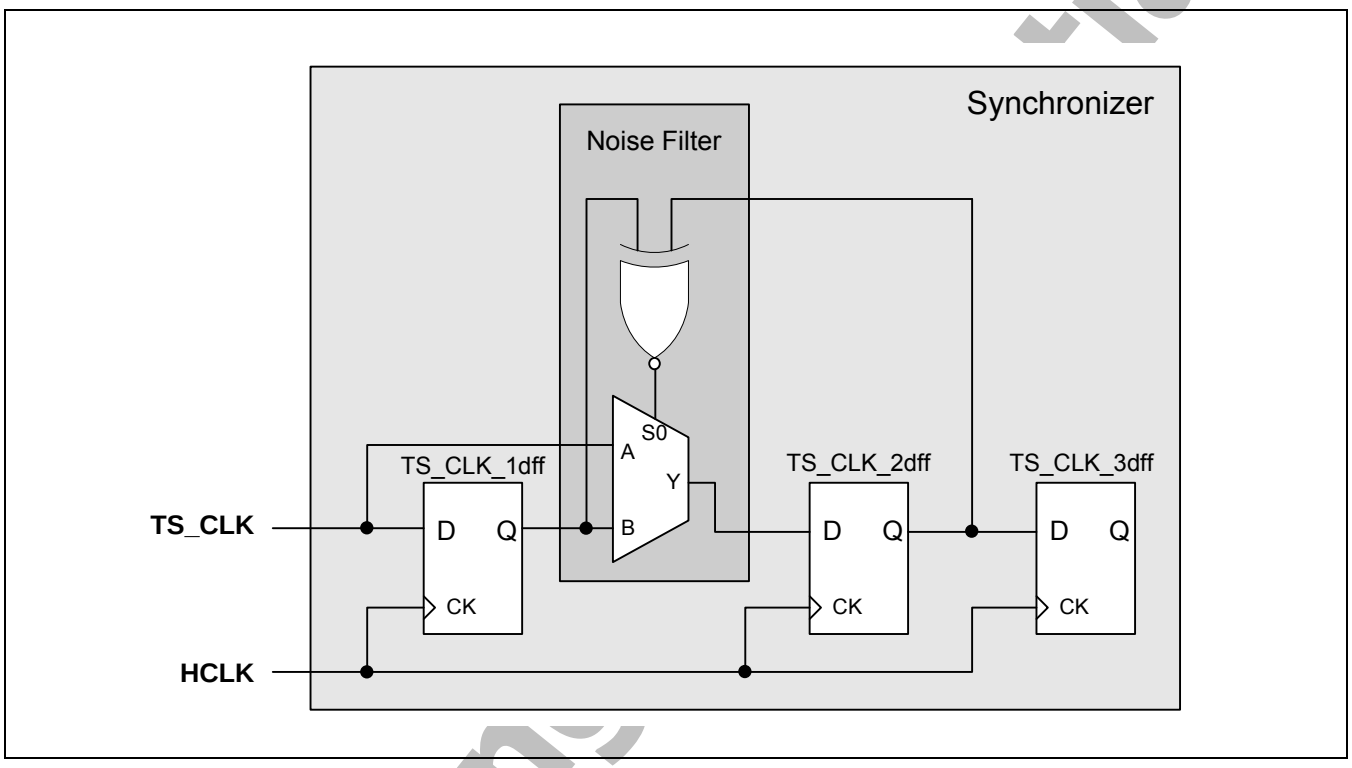

Figure 8-8 Block Diagram of TS_CLK Filter

8.1.5.6 Transport Stream Write

After the transport stream is received from the channel chip, it is stored in internal FIFO (32-word). The TSI sends the transport stream to the output buffer (DRAM) depending on the selected burst length (1-/ 4-/ 8-beat). Using word-aligned address, the TSI sends data streams to the output buffer (SDRAM). One packet size is equal to 47 words. The output buffer size should be equal to a multiple of 47 words (one packet size). If the data is written in the output buffer, the SDRAM full interrupt is generated and the destination address is reloaded in the base address.

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8.1.5.7 Program ID filter

TSI supports a Program ID (PID) filter mode that uses 32 PID filters. PID filter can switch on/off independently. Consider the PID filter mode as enabled. In case the PID of transmitted packet header is one of the 32 filters, the transport stream is treated as normal and stored to output buffer. However, if the PID filter mode is disabled, the PID filter value is not checked and all transport streams are recognized as normal.

8.1.5.8 TSI Control FSM

TSI has several operating modes. As shown in *Figure 8-9*, the TSI can switch from one mode to another according to the condition (state) of control signals.

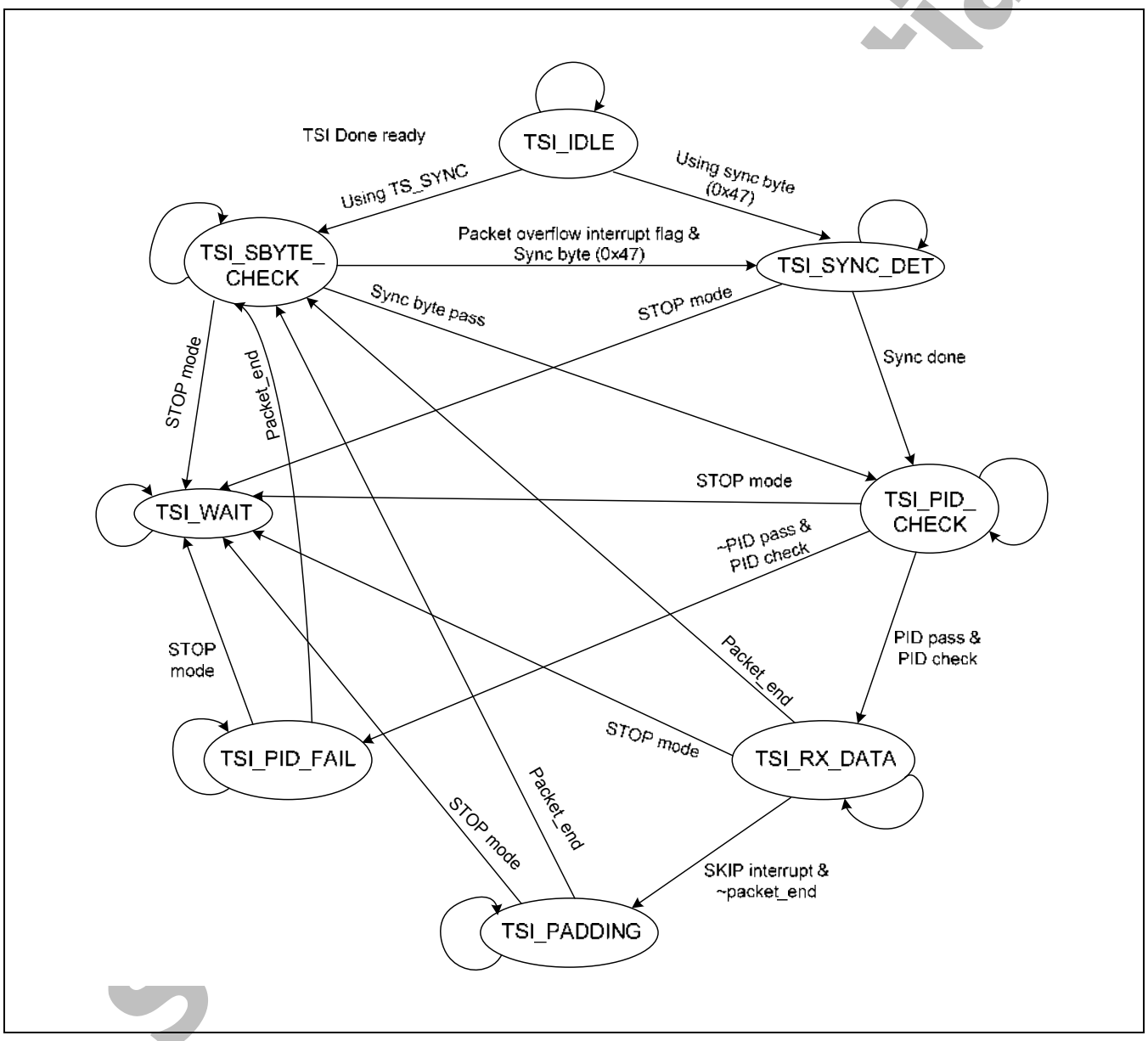

Figure 8-9 TSI Control Finite State Machine (FSM)

8.1.5.9 Shadow Base Address

TSI automatically changes the destination address of output buffer (SDRAM) with base address. When TSI is started (tsi_on = 1) or output buffer full interrupt is generated, address value of TS_BASE register is set as new destination address to store received packet data.

Example of Shadow Base Address usage:

1. Set the first address in TS_BASE register.
2. Start TSI (the first address is set as destination address).
3. Set the second address in TS_BASE register right after TSI starts. Output buffer becomes full (the second address is set as new destination address).
4. Set the third address in TS_BASE register when output buffer full interrupt is generated. Output buffer becomes full (the third address is set as new destination address).

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8.2 REGISTER DESCRIPTION

8.2.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
TS_CLKCON	0xEB40_0000	R/W	Specifies the TSI clock control register.	32'h0000_0002
TS_CON	0xEB40_0004	R/W	Specifies the TSI control register.	32'h1000_0000
TS_SYNC	0xEB40_0008	R/W	Specifies the TSI Sync control register.	32'h0000_00F0
TS_CNT	0xEB40_000C	R/W	Specifies the TSI clock count register.	32'h00FF_FFFF
TS_BASE	0xEB40_0010	R/W	Specifies the TS buffer base address.	32'h0000_0000
TS_SIZE	0xEB40_0014	R/W	Specifies the TS buffer size address.	32'h0000_0000
TS_CADDR	0xEB40_0018	R	Specifies the TS buffer current write address.	32'h0000_0000
TS_INT_MASK	0xEB40_001C	R/W	Specifies the TSI interrupt mask register.	32'h0000_0000
TS_INT	0xEB40_0020	R/W	Specifies the TSI interrupt flag register.	32'h0000_0000
TS_PID0	0xEB40_0024	R/W	Specifies the TSI PID filter0.	32'h0000_0000
TS_PID1	0xEB40_0028	R/W	Specifies the TSI PID filter1.	32'h0000_0000
TS_PID2	0xEB40_002C	R/W	Specifies the TSI PID filter2.	32'h0000_0000
TS_PID3	0xEB40_0030	R/W	Specifies the TSI PID filter3.	32'h0000_0000
TS_PID4	0xEB40_0034	R/W	Specifies the TSI PID filter4.	32'h0000_0000
TS_PID5	0xEB40_0038	R/W	Specifies the TSI PID filter5.	32'h0000_0000
TS_PID6	0xEB40_003C	R/W	Specifies the TSI PID filter6.	32'h0000_0000
TS_PID7	0xEB40_0040	R/W	Specifies the TSI PID filter7.	32'h0000_0000
TS_PID8	0xEB40_0044	R/W	Specifies the TSI PID filter8.	32'h0000_0000
TS_PID9	0xEB40_0048	R/W	Specifies the TSI PID filter9.	32'h0000_0000
TS_PID10	0xEB40_004C	R/W	Specifies the TSI PID filter10.	32'h0000_0000
TS_PID11	0xEB40_0050	R/W	Specifies the TSI PID filter11.	32'h0000_0000
TS_PID12	0xEB40_0054	R/W	Specifies the TSI PID filter12.	32'h0000_0000
TS_PID13	0xEB40_0058	R/W	Specifies the TSI PID filter13.	32'h0000_0000
TS_PID14	0xEB40_005C	R/W	Specifies the TSI PID filter14.	32'h0000_0000
TS_PID15	0xEB40_0060	R/W	Specifies the TSI PID filter15.	32'h0000_0000
TS_PID16	0xEB40_0064	R/W	Specifies the TSI PID filter16.	32'h0000_0000
TS_PID17	0xEB40_0068	R/W	Specifies the TSI PID filter17.	32'h0000_0000
TS_PID18	0xEB40_006C	R/W	Specifies the TSI PID filter18.	32'h0000_0000
TS_PID19	0xEB40_0070	R/W	Specifies the TSI PID filter19.	32'h0000_0000
TS_PID20	0xEB40_0074	R/W	Specifies the TSI PID filter20.	32'h0000_0000
TS_PID21	0xEB40_0078	R/W	Specifies the TSI PID filter21.	32'h0000_0000
TS_PID22	0xEB40_007C	R/W	Specifies the TSI PID filter22.	32'h0000_0000
TS_PID23	0xEB40_0080	R/W	Specifies the TSI PID filter23.	32'h0000_0000
TS_PID24	0xEB40_0084	R/W	Specifies the TSI PID filter24.	32'h0000_0000

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Register	Address	R/W	Description	Reset Value
TS_PID25	0xEB40_0088	R/W	Specifies the TSI PID filter25.	32'h0000_0000
TS_PID26	0xEB40_008C	R/W	Specifies the TSI PID filter26.	32'h0000_0000
TS_PID27	0xEB40_0090	R/W	Specifies the TSI PID filter27.	32'h0000_0000
TS_PID28	0xEB40_0094	R/W	Specifies the TSI PID filter28.	32'h0000_0000
TS_PID29	0xEB40_0098	R/W	Specifies the TSI PID filter29.	32'h0000_0000
TS_PID30	0xEB40_009C	R/W	Specifies the TSI PID filter30.	32'h0000_0000
TS_PID31	0xEB40_00A0	R/W	Specifies the TSI PID filter31.	32'h0000_0000
BYTE_SWAP	0xEB40_00BC	R/W	Specifies the TSI tx byte swap enable register for little endian.	32'h0000_0001

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8.2.2 TSI REGISTER DESCRIPTION

8.2.2.1 TSI Clock Control Register (TS_CLKCON, R/W, Address = 0xEB40_0000)

TS_CLKCON	Bit	Description	R/W	Initial State
Reserved	[31:2]	-	-	-
TSI clock down ready	[1]	If this field is set to 1, TSI block is ready to be down. 0 = Not ready 1 = Ready	R	1'b1
TSI on	[0]	TSI on/off. 0 = TSI off 1 = TSI on	R/W	1'b0

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8.2.2.2 TSI Control Register (TS_CON, R/W, Address = 0xEB40_0004)

TS_CON	Bit	Description	R/W	Initial State
TSI SWRESET	[31]	Initializes all registers and states of TSI block. 0 = No effect 1 = Reset (equals to H/W reset)	W	-
TS_CLK filter mode	[30]	Specifies the filter mode. 0 = Off 1 = On (use ts_clk filter. max. ts_clk frequency is 1/4 HCLK)	R/W	1'b0
TSI burst length	[29:28]	Sets the TSI burst length. 00 = 1-beat burst 01 = 4-beat burst 10 = 8-beat burst 11 = reserved.	R/W	2'b01
output_buffer_ full_int_mode	[27]	Sets the output buffer full interrupt mode. 0 = Disable 1 = Enable	R/W	1'b0
int_fifo_full_ int_mode	[26]	Sets the internal FIFO full interrupt mode. 0 = Disable 1 = Enable	R/W	1'b0
sync_mismatch_i nt_mode	[25:24]	Sets the sync mismatch interrupt mode. 0x = Disable 10 = Enable with skip mode 11 = Enable with stop mode	R/W	2'b00
psuf_int_mode	[23:22]	Sets the packet size underflow interrupt mode. 0x = Disable 10 = Enable with skip mode 11 = Enable with stop mode	R/W	2'b00
psof_int_mode	[21:20]	Sets the packet size overflow interrupt mode. 0x = Disable 10 = Enable with skip mode 11= Enable with stop mode	R/W	2'b00
ts_clk_timeout_ int_mode	[19]	Sets the TS_CLK timeout interrupt mode. 0 = Disable 1 = Enable	R/W	2'b00
ts_error_int_ mode	[18:16]	Sets the TS_ERROR interrupt mode. 0xx = Disable 100 = Enable with skip mode (detecting size: bit) 101 = Enable with stop mode (detecting size: bit) 110 = Enable with skip mode (detecting size: packet) 111 = Enable with stop mode (detecting size: packet)	R/W	3'b000
padding_pattern	[15:8]	Specifies the Padding pattern.	R/W	8'h00
pid_filter_mode	[7]	Specifies the PID filtering mode. 0 = Bypass mode 1 = Filtering mode	R/W	1'b0

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TS_CON	Bit	Description	R/W	Initial State
ts_error_active	[6]	Specifies the TS_ERROR active mode. 0 = Active high 1 = Active low	R/W	1'b0
data_byte_order	[5]	Specifies the TS_DATA byte ordering. 0 = MSB to LSB 1 = LSB to MSB	R/W	1'b0
ts_valid_active	[4]	Specifies the TS_VALID active mode. 0 = Active high 1 = Active low	R/W	1'b0
ts_sync_active	[3]	Specifies the TS_SYNC active mode. 0 = Active high 1 = Active low	R/W	1'b0
ts_clk_invert	[2]	Specifies the TS_CLK inverting mode. 0 = Non-inverting (falling-edge data fetch) 1 = Inverting (ringing-edge data fetch)	R/W	1'b0
Reserved	[1:0]	-	-	-

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8.2.2.3 TSI SYNC Control Register (TS_SYNC, R/W, Address = 0xEB40_0008)

TS_SYNC	Bit	Description	R/W	Initial State
Reserved	[31:20]	-	R	-
sync_csdc3	[19:16]	Specifies the Current sync detecting count3.	R	4'h0
sync_csdc2	[15:12]	Specifies the Current sync detecting count2.	R	4'h0
sync_csdc1	[11:8]	Specifies the Current sync detecting count1.	R/W	4'h0
sync_det_cnt	[7:4]	Specifies the Sync detecting count. If the sync detecting mode uses sync byte, this field indicates the initial detecting count.	-	4'hF
Reserved	[3:2]	-	R/W	-
sync_det_mode	[1:0]	Specifies the Sync detecting mode. 00 = Using TS_SYNC (detecting consecutive 8-bit) 01 = Using TS_SYNC (detecting only 1-bit) 1x = Using sync byte (0x47)		2'b00

8.2.2.4 TSI Clock Count Register (TS_CNT, R/W, Address = 0xEB40_000C)

TS_CNT	Bit	Description	R/W	Initial State
ts_clk_error_cnt	[31:0]	Specifies the TS_CLK timeout period. If the ts_clk does not toggle for n-times of hclk, ts_clk_timeout interrupt is generated. TS_CLK timeout period: HCLK(7.5ns) * n	R/W	32'h00FF_FFFF

8.2.2.5 TS Buffer Base Address Register (TS_BASE, R/W, Address = 0xEB40_0010)

TS_BASE	Bit	Description	R/W	Initial State
ts_base_addr	[31:2]	Specifies the TS buffer base address (word aligned).	R/W	30'h0
-	[1:0]	-	-	-

8.2.2.6 TS Buffer Size Address Register (TS_SIZE, R/W, Address = 0xEB40_0014)

TS_SIZE	Bit	Description	R/W	Initial State
Reserved	[31:16]	-	-	-
ts_buffer_size	[15:0]	This field should be 47-word (188-byte) * n , where n specifies the stream packet word count (0~348 word). If the buffer is full, the buffer write address is cleared to the buffer base address.	R/W	16'h0

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8.2.2.7 TS Buffer Current Address Register (TS_CADDR, R, Address = 0xEB40_0018)

TS_CADDR	Bit	Description	R/W	Initial State
ts_caddr	[31:2]	Specifies the TS buffer current write address.	R	30'h0
-	[1:0]	-	-	-

8.2.2.8 TSI Interrupt Mask Register (TS_INT_MASK, R/W, Address = 0xEB40_001C)

TS_INT_MASK	Bit	Description	R/W	Initial State
Reserved	[31:8]	-	-	-
dma_complete_mask	[7]	Specifies the DMA complete interrupt mask. 0 = Masking 1 = Not masking	R/W	1'b0
output_buffer_full_mask	[6]	Specifies the TSI interrupt mask: output buffer full. 0 = Masking 1 = Not masking	R/W	1'b0
int_fifo_full_mask	[5]	Specifies the TSI interrupt mask: internal FIFO full. 0 = Masking 1 = Not masking	R/W	1'b0
sync_mismatch_mask	[4]	Specifies the TSI interrupt mask: sync mismatch. 0 = Masking 1 = Not masking	R/W	1'b0
packet_size_underflow_mask	[3]	Specifies the TSI interrupt mask: packet size underflow. 0 = Masking 1 = Not masking	R/W	1'b0
packet_size_overflow_mask	[2]	Specifies the TSI interrupt mask: packet size overflow 0 = Masking 1 = Not masking	R/W	1'b0
TS_CLK_mask	[1]	Specifies the TSI interrupt mask: TS_CLK 0 = Masking 1= Not masking	R/W	1'b0
TS_ERROR_mask	[0]	Specifies the TSI interrupt mask: TS_ERROR 0 = Masking 1 = Not masking	R/W	1'b0

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8.2.2.9 TSI Interrupt Flag Register (TS_INT, R/W, Address = 0xEB40_0020)

TS_INT	Bit	Description	R/W	Initial State
Reserved	[31:8]	-	-	-
dma_complete_ flag	[7]	Specifies the Dma transfer complete flag. 0 = Interrupt is not generated 1 = Interrupt is generated (Writing '1' clears this field and writing '0' has no effect.)	R/W	1'b0
output_buffer_ful l_ flag	[6]	Specifies the Output buffer full interrupt flag. 0 = Interrupt is not generated 1 = Interrupt is generated (Writing '1' clears this field and writing '0' has no effect.)	R/W	1'b0
int_fifo_full_flag	[5]	Specifies the Internal FIFO full interrupt flag. 0 = Interrupt is not generated 1 = Interrupt is generated (Writing '1' clears this field and writing '0' has no effect.)	R/W	1'b0
sync_mismatch_ flag	[4]	Specifies the Sync mismatch interrupt flag. 0 = Interrupt is not generated 1 = Interrupt is generated (Writing '1' clears this field and writing '0' has no effect.)	R/W	1'b0
psuf_flag	[3]	Specifies the Packet underflow interrupt flag. 0 = Interrupt is not generated 1 = Interrupt is generated (Writing '1' clears this field and writing '0' has no effect.)	R/W	1'b0
psof_flag	[2]	Specifies the Packet overflow interrupt flag. 0 = Interrupt is not generated 1 = Interrupt is generated (Writing '1' clears this field and writing '0' has no effect.)	R/W	1'b0
ts_clk_timeout_ flag	[1]	Specifies the TS_CLK timeout interrupt flag. 0 = Interrupt is not generated 1 = Interrupt is generated (Writing '1' clears this field and writing '0' has no effect.)	R/W	1'b0
ts_error_flag	[0]	Specifies the TS_ERROR interrupt flag. 0 = Interrupt is not generated 1 = Interrupt is generated (Writing '1' clears this field and writing '0' has no effect.)	R/W	1'b0

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8.2.2.10 TSI PID Filter0 Address Register (TS_PID0, R/W, Address = 0xEB40_0024)

TS_PID0	Bit	Description	R/W	Initial State
Reserved	[31:14]	-	-	-
pid0_en	[13]	Specifies the PID filter0. 0 = Disable 1 = Enable	R/W	1'b0
pid0_value	[12:0]	Specifies the PID0 value. If an input stream's PID is different from this value, then the stream is ignored.	R/W	13'h0

8.2.2.11 TSI PID Filter1 Address Register (TS_PID1, R/W, Address = 0xEB40_0028)

8.2.2.12 TSI PID Filter2 Address Register (TS_PID2, R/W, Address = 0xEB40_002C)

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8.2.2.19 TSI PID Filter9 Address Register (TS_PID9, R/W, Address = 0xEB40_0048)

8.2.2.20 TSI PID Filter10 Address Register (TS_PID10, R/W, Address = 0xEB40_004C)

8.2.2.21 TSI PID Filter11 Address Register (TS_PID11, R/W, Address = 0xEB40_0050)

8.2.2.22 TSI PID Filter12 Address Register (TS_PID12, R/W, Address = 0xEB40_0054)

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8.2.2.23 TSI PID Filter13 Address Register (TS_PID13, R/W, Address = 0xEB40_0058)

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8.2.2.30 TSI PID Filter20 Address Register (TS_PID20, R/W, Address = 0xEB40_0074)

8.2.2.31 TSI PID Filter21 Address Register (TS_PID21, R/W, Address = 0xEB40_0078)

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8.2.2.40 TSI PID Filter30 Address Register (TS_PID30, R/W, Address = 0xEB40_009C)

8.2.2.41 TSI PID Filter31 Address Register (TS_PID31, R/W, Address = 0xEB40_00A0)

8.2.2.42 TSI TX Byte SWAP Register (BYTE_SWAP, R/W, Address = 0xEB40_00BC)

BYTE_SWAP	Bit	Description	R/W	Initial State
Reserved	[31:0]	-	R/W	-
byte_swap	[0]	Specifies the TSI tx byte swap enable register for little endian. 0 = Disable - big endian 1 = Enable - little endian		1'b1

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Section 9

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1 DISPLAY CONTROLLER

1.1 OVERVIEW OF DISPLAY CONTROLLER

The Display controller consists of logic for transferring image data from a local bus of the camera interface controller or a video buffer located in system memory to an external LCD driver interface. The LCD driver interface supports three kinds of interface, namely, RGB-interface, indirect-i80 interface, and YUV interface for writeback. The display controller uses up to five overlay image windows that support various color formats, 256 level alpha blending, color key, x-y position control, soft scrolling, and variable window size, among others.

The display controller supports various color formats such as RGB (1 bpp to 24 bpp) and YCbCr 4:4:4 (only local bus). It is programmed to support the different requirements on screen related to the number of horizontal and vertical pixels, data line width for the data interface, interface timing, and refresh rate.

The display controller transfers the video data and generates the necessary control signals, such as, RGB_VSYNC, RGB_HSYNC, RGB_VCLK, RGB_VDEN and SYS_CS0, SYS_CS1, SYS_WE. In addition to generating control signals, the display controller contains data ports for video data (RGB_VD[23:0], and SYS_VD), as shown in *Figure 1-1*.

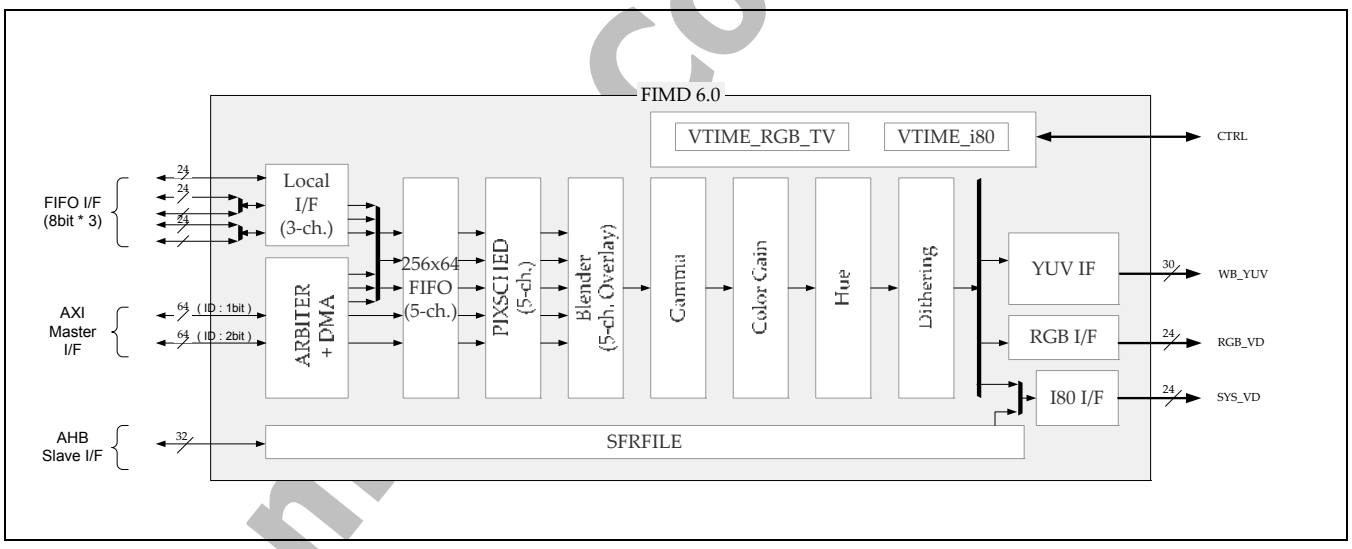

Figure 1-1 Block Diagram of Display Controller

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1.2 KEY FEATURES OF THE DISPLAY CONTROLLER

The key features of the display controller include:

Bus Interface	AMBA AXI 64-bit Master/ AHB 32-bit Slave Local Video Bus (YCbCr/ RGB)
Video Output Interface	RGB Interface (24-bit Parallel/ 8-bit Serial) (dummy insertion, color sub-sampling (RGB skip) mode) (general, delta structure) Indirect i80 interface WriteBack interface (YUV444 30-bit)
Dual Output Mode	Supports i80 and WriteBack Supports RGB and WriteBack
PIP (OSD) function	Supports 8-bpp (bit per pixel) palletized color Supports 16-bpp non-palletized color Supports unpacked 18-bpp non-palletized color Supports unpacked 24-bpp non-palletized color
	Supports X,Y indexed position
	Supports 8-bit Alpha blending (Plane/ Pixel)
Source format	**Window 0** Supports 1, 2, 4, or 8-bpp (bit per pixel) palletized color Supports 16, 18, or 24-bpp non-palletized color Supports RGB (8:8:8) local input from Local Bus (FIMC0) **Window 1** Supports 1, 2, 4, or 8-bpp (bit per pixel) palletized color Supports 16, 18, or 24-bpp non-palletized color Supports RGB (8:8:8) local input from Local Bus (FIMC1) **Window 2** Supports 1, 2, 4, or 8-bpp (bit per pixel) palletized color Supports 16, 18, or 24-bpp non-palletized color Supports RGB (8:8:8) local input from Local Bus (FIMC2) **Window 3/ 4** Supports 1, 2, 4, or 8-bpp (bit per pixel) palletized color Supports 16, 18, or 24-bpp non-palletized color
Configurable Burst Length	Programmable 4/ 8/ 16 Burst DMA
Palette	**Window 0/ 1/ 2/ 3/ 4** Supports 256 x 32 bits palette memory (5ea: One palette memory for each window)
Soft Scrolling	Horizontal = 1 Byte resolution Vertical = 1 pixel resolution
Virtual Screen	Virtual image can have up to 16MB image size. Each window can have its own virtual area.
Transparent Overlay	Supports Transparent Overlay

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Color Key (Chroma Key)	Supports color key function Supports simultaneously color key and blending function
Partial Display	Supports LCD partial display function through i80 interface
Image Enhancement	Supports Gamma control
	Supports Hue control
	Supports color gain control
	Supports pixel compensation (only for delta structure)

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1.3 FUNCTIONAL DESCRIPTION OF DISPLAY CONTROLLER

1.3.1 BRIEF DESCRIPTION OF THE SUB-BLOCK

The display controller consists of a VSFR, VDMA, VPRCS, VTIME, and video clock generator.

To configure the display controller, the VSFR has 121 programmable register sets, one gamma LUT register set (64 registers), one i80 command register set (12 registers), and five 256x32 palette memories.

VDMA is a dedicated display DMA that transfers video data in frame memory to VPRCS. By using this special DMA, you can display video data on screen without CPU intervention.

VPRCS receives video data from VDMA and sends it to display device (LCD) through data ports (RGB_VD, or SYS_VD), after changing the video data into a suitable data format. For example, 8-bit per pixel mode (8 bpp mode) or 16-bit per pixel mode (16 bpp mode).

VTIME consists of programmable logic to support the variable requirement of interface timing and rates commonly found in different LCD drivers. The VTIME block generates RGB_VSYNC, RGB_HSYNC, RGB_VCLK, RGB_VDEN, VEN_VSYNC, VEN_HSYNC, VEN_FIELD, VEN_HREF and SYS_CS0, SYS_CS1, SYS_WE, and so on.

Using the display controller data, you can select one of the above data paths by setting DISPLAY_PATH_SEL[1:0] (0xE010_7008). For more information, refer to Chapter, "Section 02.03. Clock controller".

1.3.2 DATA FLOW

FIFO is in the VDMA. If FIFO is empty or partially empty, the VDMA requests data fetching from frame memory based on burst memory transfer mode. The data transfer rate determines the size of FIFO.

The display controller contains five FIFOs (three local FIFOs and two DMA FIFOs), since it needs to support the overlay window display mode. Use one FIFO for one screen display mode.

VPRCS fetches data from FIFO. It contains the following functions for final image data: blending, image enhancing, and scheduling. It also supports the overlay function. This can overlay any image up to five window images, whose smaller or same size can be blended with the main window image having programmable alpha blending or color (chroma) key function.

Figure 1-2 shows the data flow from system bus to output buffer.

VDMA has five DMA channels (Ch0 ~ Ch4)and three local input interfaces (CAMIF0, CAMIF1, and CAMIF2). The Color Space Conversion (CSC) block changes Hue (YCbCr, local input only) data to RGB data for blending operation. Also, the alpha values written in SFR determine the level of blending. Data from output buffer appears in the Video Data Port.

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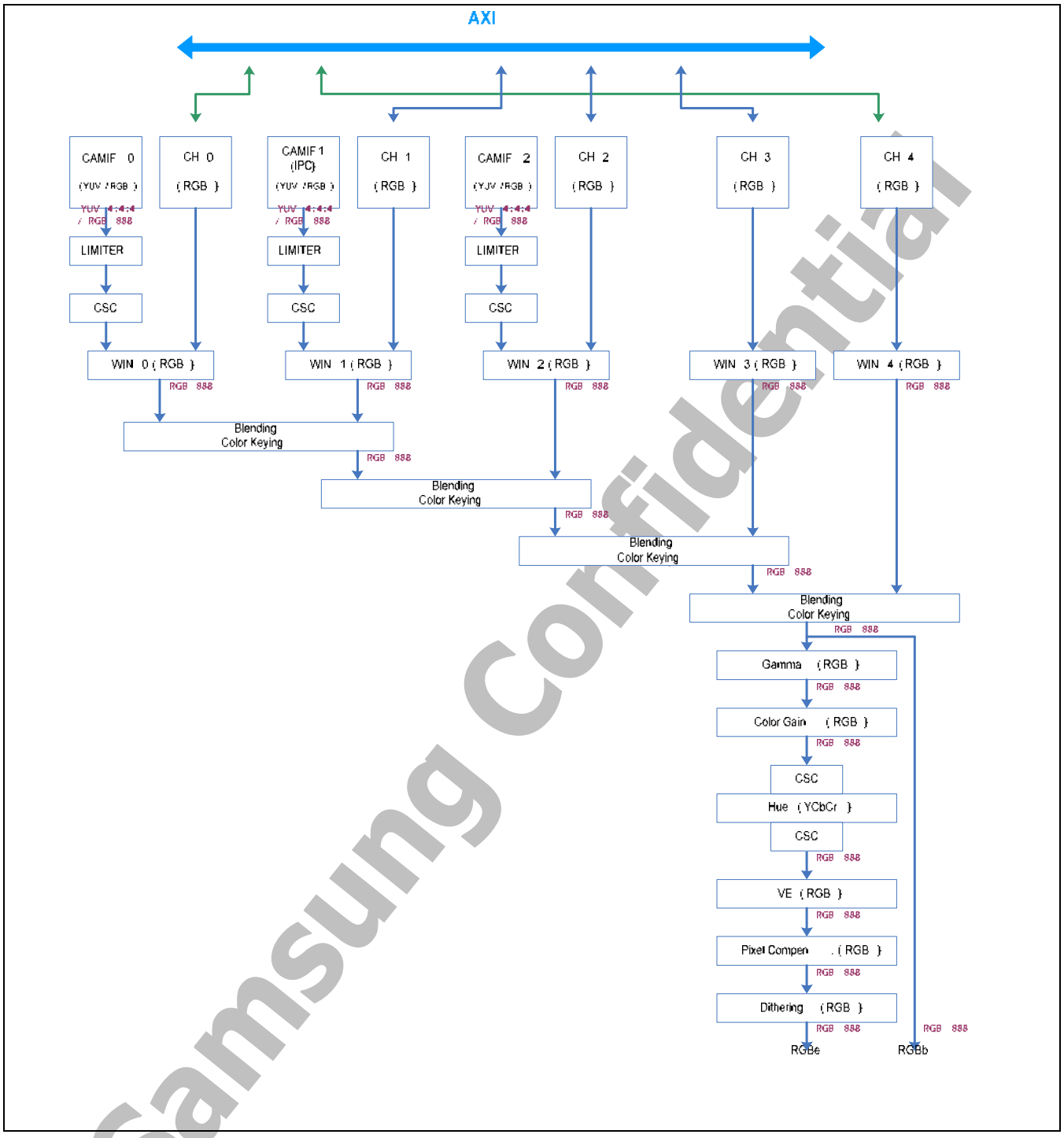

Figure 1-2 Block Diagram of the Data Flow

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1.3.2.1 Interface

The display controller supports three types of interfaces:

- The first type is the conventional RGB interface, which uses RGB data, vertical/ horizontal sync, data valid signal, and data sync clock.
- The second type is the indirect i80 Interface, which uses address, data, chip select, read/ write control, and register/ status indicating signal. The LCD driver using i80 Interface contains a frame buffer and can self-refresh, so the display controller updates one still image by writing only one time to the LCD.
- The third type is FIFO interface with CAMIF2 for writeback.

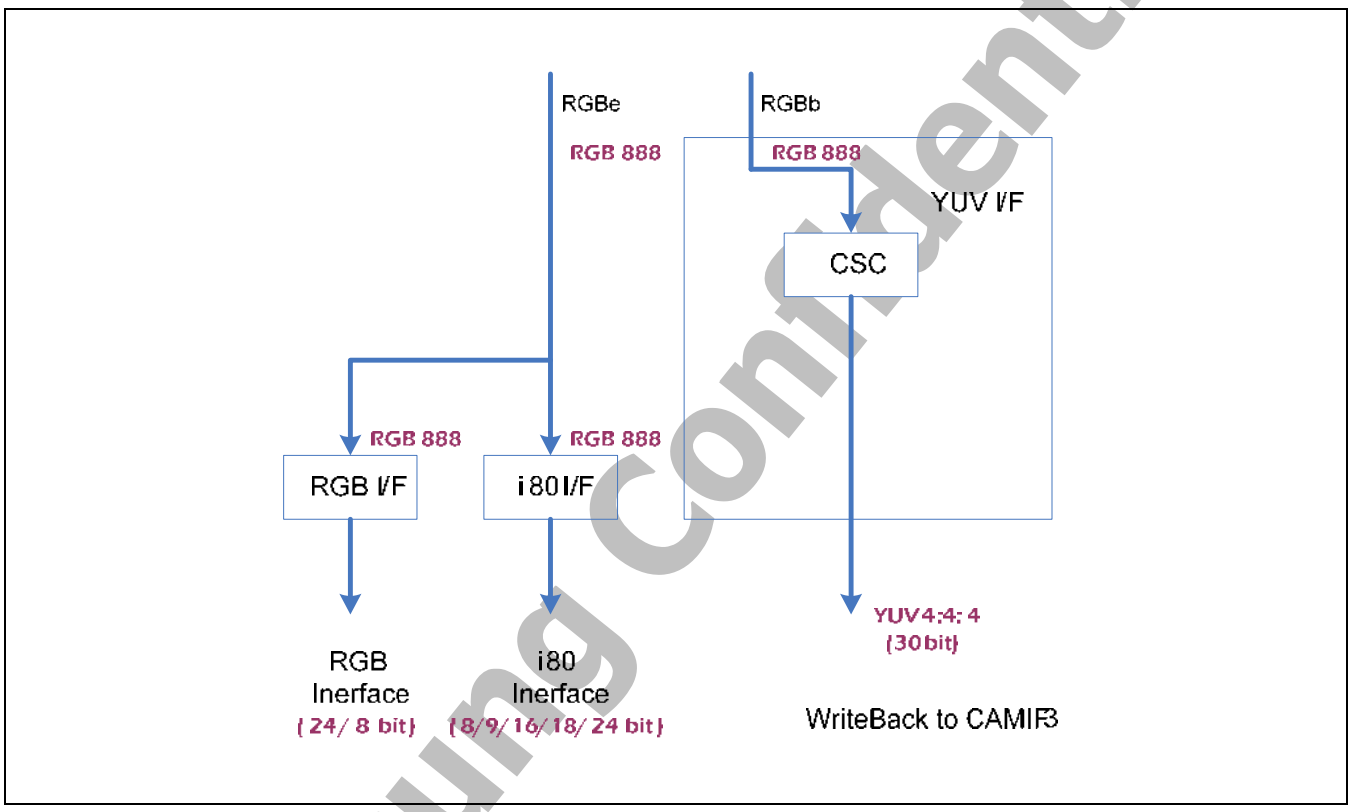

Figure 1-3 Block Diagram of the Interface

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1.3.3 OVERVIEW OF THE COLOR DATA

1.3.3.1 RGB Data Format

The display controller requests the specified memory format of frame buffer. The table below shows some examples of each display mode.

1.3.3.2 25BPP Display (A888)

(BSWP=0, HWSWP=0, WSWP=0)

	D[63:57]	D[56]	D[55:32]	D[31:25]	D[24]	D[23:0]
000H	Dummy Bit	AEN	P1	Dummy Bit	AEN	P2
008H	Dummy Bit	AEN	P3	Dummy Bit	AEN	P4
010H	Dummy Bit	AEN	P5	Dummy Bit	AEN	P6
…						

NOTE:

1. AEN: Specifies the transparency value selection bit.
   AEN = 0: Selects ALPHA0.
   AEN = 1: Selects ALPHA1.
   If per-pixel blending is set, then this pixel blends with alpha value selected by AEN.
   Alpha value is selected by SFR as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, and ALPHA1_B.
   For more information, refer to the section on “SFR”.
2. D [23:16] = Red data, D [15:8] = Green data, and D [7:0] = Blue data.

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1.3.3.2.1 32BPP (8888) Mode

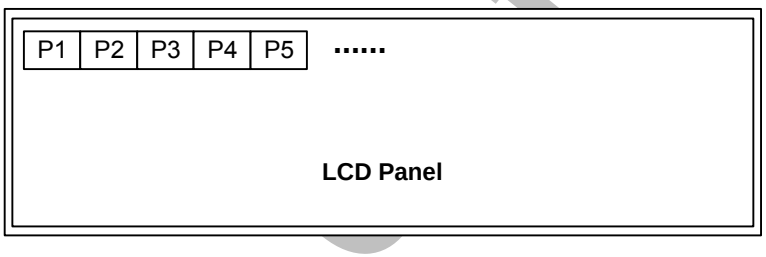
Pixel data contains Alpha value.

(BYSWP=0, HWSWP=0, WSWP=0)

	D[63:56]	D[55:32]	D[31:24]	D[23:0]
000H	ALPHA value	P1	ALPHA value	P2
008H	ALPHA value	P3	ALPHA value	P4
010H	ALPHA value	P5	ALPHA value	P6
…				

(BYSWP=0, HWSWP=0, WSWP=1)

	D[63:56]	D[55:32]	D[31:24]	D[23:0]
000H	ALPHA value	P2	ALPHA value	P1
008H	ALPHA value	P4	ALPHA value	P3
010H	ALPHA value	P6	ALPHA value	P5
…				



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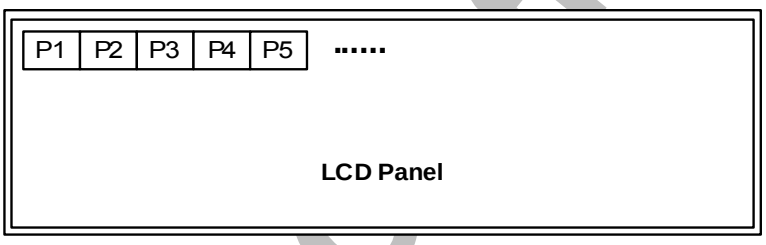
1.3.3.2.2 24BPP Display (A887)

(BSWP=0, HWSWP=0, WSWP=0)

	D[63:56]	D[55]	D[54:32]	D[31:24]	D[23]	D[22:0]
000H	Dummy Bit	AEN	P1	Dummy Bit	AEN	P2
008H	Dummy Bit	AEN	P3	Dummy Bit	AEN	P4
010H	Dummy Bit	AEN	P5	Dummy Bit	AEN	P6
…						

(BSWP=0, HWSWP=0, WSWP=1)

	D[63:56]	D[55]	D[54:32]	D[31:24]	D[23]	D[22:0]
000H	Dummy Bit	AEN	P2	Dummy Bit	AEN	P1
008H	Dummy Bit	AEN	P4	Dummy Bit	AEN	P3
010H	Dummy Bit	AEN	P6	Dummy Bit	AEN	P5
…						



NOTE:

1. AEN: Specifies the transparency value selection bit.
   AEN = 0: Selects ALPHA0.
   AEN = 1: Selects ALPHA1.
   If per-pixel blending is set, then this pixel blends with alpha value selected by AEN.
   Alpha value is selected by SFR as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, and ALPHA1_B.
   For more information, refer to the section on “SFR”.
2. D [22:15] = Red data, D [14:7] = Green data, and D [6:0] = Blue data.

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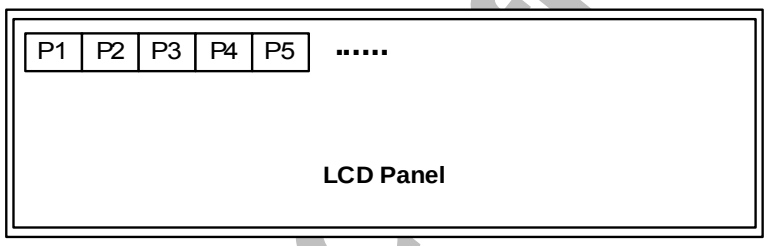
1.3.3.2.3 24BPP Display (888)

(BSWP =0, HWSWP=0, WSWP=0)

	D[63:56]	D[55:32]	D[31:24]	D[23:0]
000H	Dummy Bit	P1	Dummy Bit	P2
008H	Dummy Bit	P3	Dummy Bit	P4
010H	Dummy Bit	P5	Dummy Bit	P6
…				

(BSWP =0, HWSWP=0, WSWP=1)

	D[63:56]	D[55:32]	D[31:24]	D[23:0]
000H	Dummy Bit	P2	Dummy Bit	P1
008H	Dummy Bit	P4	Dummy Bit	P3
010H	Dummy Bit	P6	Dummy Bit	P5
…				



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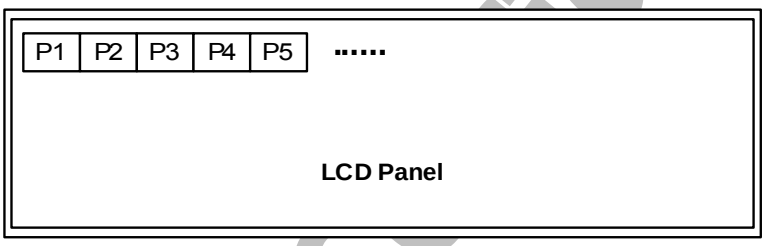
1.3.3.2.4 19BPP Display (A666)

(BSWP=0, HWSWP=0, WSWP=0)

	D[63:51]	D[50]	D[49:32]	D[31:19]	D[18]	D[17:0]
000H	Dummy Bit	AEN	P1	Dummy Bit	AEN	P2
008H	Dummy Bit	AEN	P3	Dummy Bit	AEN	P4
010H	Dummy Bit	AEN	P5	Dummy Bit	AEN	P6
…						

(BSWP=0, HWSWP=0, WSWP=1)

	D[63:51]	D[50]	D[49:32]	D[31:19]	D[18]	D[17:0]
000H	Dummy Bit	AEN	P2	Dummy Bit	AEN	P1
008H	Dummy Bit	AEN	P4	Dummy Bit	AEN	P3
010H	Dummy Bit	AEN	P6	Dummy Bit	AEN	P5
…						



NOTE:

1. AEN: Specifies the transparency value selection bit.
   AEN = 0: Selects ALPHA0.
   AEN = 1: Selects ALPHA1.
   If per-pixel blending is set, then this pixel blends with alpha value selected by AEN.
   Alpha value is selected by SFR as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, and ALPHA1_B.
   For more information, refer to the section on “SFR”.
2. D [17:12] = Red data, D [11:6] = Green data, and D [5:0] = Blue data.

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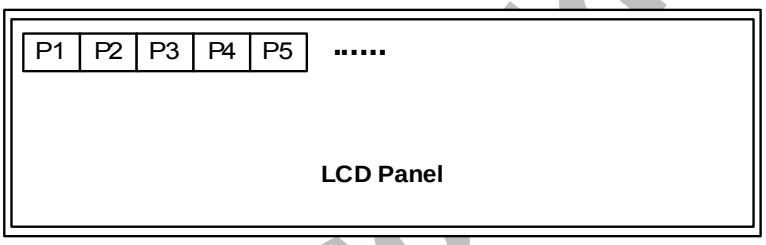
1.3.3.2.5 18BPP Display (666)

(BSWP =0, HWSWP=0, WSWP=0)

	D[63:50]	D[49:32]	D[31:18]	D[17:0]
000H	Dummy Bit	P1	Dummy Bit	P2
008H	Dummy Bit	P3	Dummy Bit	P4
010H	Dummy Bit	P5	Dummy Bit	P6
…				

(BSWP =0, HWSWP=0, WSWP=1)

	D[63:50]	D[49:32]	D[31:18]	D[17:0]
000H	Dummy Bit	P2	Dummy Bit	P1
008H	Dummy Bit	P4	Dummy Bit	P3
010H	Dummy Bit	P6	Dummy Bit	P5
…				



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1.3.3.2.6 16BPP Display (A555)

(BSWP=0, HWSWP=0, WSWP=0)

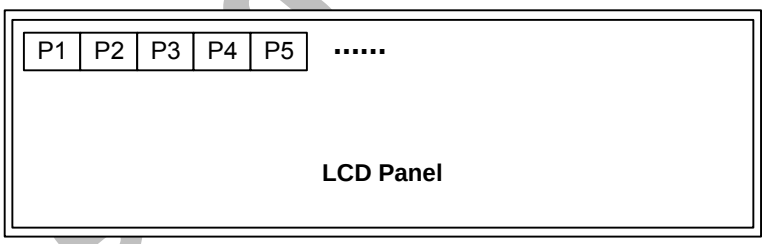
	D[63]	D[62:48]	D[47]	D[46:32]	D[31]	D[30:16]	D[15]	D[14:0]
000H	AEN1	P1	AEN2	P2	AEN3	P3	AEN4	P4
004H	AEN5	P5	AEN6	P6	AEN7	P7	AEN8	P8
008H	AEN9	P9	AEN10	P10	AEN11	P11	AEN12	P12
…								

(BSWP=0, HWSWP=0, WSWP=1)

	D[63]	D[62:48]	D[47]	D[46:32]	D[31]	D[30:16]	D[15]	D[14:0]
000H	AEN3	P3	AEN4	P4	AEN1	P1	AEN2	P2
004H	AEN7	P7	AEN8	P8	AEN5	P5	AEN6	P6
008H	AEN11	P11	AEN12	P12	AEN9	P9	AEN10	P10
…								

(BSWP=0, HWSWP=1, WSWP=0)

	D[63]	D[62:48]	D[47]	D[46:32]	D[31]	D[30:16]	D[15]	D[14:0]
000H	AEN4	P4	AEN3	P3	AEN2	P2	AEN1	P1
004H	AEN8	P8	AEN7	P7	AEN6	P6	AEN5	P5
008H	AEN12	P12	AEN11	P11	AEN10	P10	AEN9	P9
…								



NOTE:

1. AEN: Specifies the transparency value selection bit.
   AEN = 0: Selects ALPHA0.
   AEN = 1: Selects ALPHA1.
   If per-pixel blending is set, then this pixel blends with alpha value selected by AEN.
   Alpha value is selected by SFR as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, and ALPHA1_B.
   For more information, refer to the section on “SFR”.
2. D [14:10] = Red data, D [9:5] = Green data, and D [4:0] = Blue data.

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1.3.3.2.7 16BPP Display (1555)

(BSWP=0, HWSWP=0, WSWP=0)

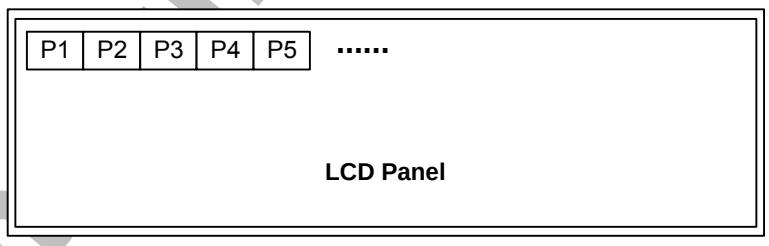
	D[63:48]	D[47:32]	D[31:16]	D[15:0]
000H	P1	P2	P3	P4
008H	P5	P6	P7	P8
010H	P9	P10	P11	P12
…				

(BSWP=0, HWSWP=0, WSWP=1)

	D[63:48]	D[47:32]	D[31:16]	D[15:0]
000H	P3	P4	P1	P2
008H	P7	P8	P5	P6
010H	P11	P12	P9	P10
…				

(BSWP=0, HWSWP=1, WSWP=0)

	D[63:48]	D[47:32]	D[31:16]	D[15:0]
000H	P4	P3	P2	P1
008H	P8	P7	P6	P5
010H	P12	P11	P10	P9
…				



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1.3.3.2.8 6BPP Display (565)

(BSWP=0, HWSWP=0, WSWP=0)

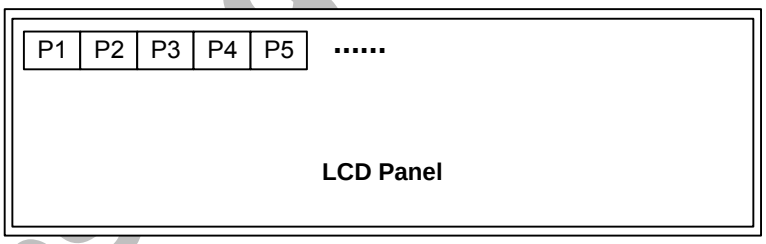
	D[63:48]	D[47:32]	D[31:16]	D[15:0]
000H	P1	P2	P3	P4
008H	P5	P6	P7	P8
010H	P9	P10	P11	P12
…				

(BSWP=0, HWSWP=0, WSWP=1)

	D[63:48]	D[47:32]	D[31:16]	D[15:0]
000H	P3	P4	P1	P2
008H	P7	P8	P5	P6
010H	P11	P12	P9	P10
…				

(BSWP=0, HWSWP=1, WSWP=0)

	D[63:48]	D[47:32]	D[31:16]	D[15:0]
000H	P4	P3	P2	P1
008H	P8	P7	P6	P5
010H	P12	P11	P10	P9
…				



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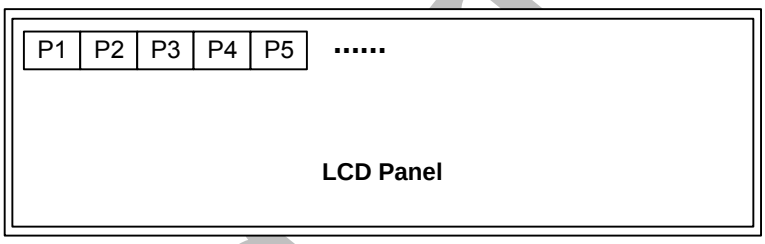
1.3.3.2.9 13BPP Display (A444)

(BYSWP=0, HWSWP=0, WSWP=0)

	D[63:61]	D[60]	D[59:48]	D[47:45]	D[44]	D[43:32]	D[31:29]	D[28]	D[27:16]	D[15:13]	D[12]	D[11:0]
000H	Dummy	AEN1	P1	Dummy	AEN2	P2	Dummy	AEN3	P3	Dummy	AEN4	P4
004H	Dummy	AEN5	P5	Dummy	AEN6	P6	Dummy	AEN7	P7	Dummy	AEN8	P8
008H	Dummy	AEN9	P9	Dummy	AEN10	P10	Dummy	AEN11	P11	Dummy	AEN12	P12
…												

(BYSWP=0, HWSWP=1, WSWP=0)

	D[63:61]	D[60]	D[59:48]	D[47:45]	D[44]	D[43:32]	D[31:29]	D[28]	D[27:16]	D[15:13]	D[12]	D[11:0]
000H	Dummy	AEN4	P4	Dummy	AEN3	P3	Dummy	AEN2	P2	Dummy	AEN1	P1
004H	Dummy	AEN8	P8	Dummy	AEN7	P7	Dummy	AEN6	P6	Dummy	AEN5	P5
008H	Dummy	AEN12	P12	Dummy	AEN11	P11	Dummy	AEN10	P10	Dummy	AEN9	P9
…												



NOTE:

1. AEN: Specifies the transparency value selection bit.
   AEN = 0: Selects ALPHA0.
   AEN = 1: Selects ALPHA1.
   If per-pixel blending is set, then this pixel blends with alpha value selected by AEN.
2. D[11:8] = Red data, D[7:4] = Green data, and D[3:0] = Blue data.
3. 16BPP (4444) mode. (For more information, refer to the section on “SFR”) Data has Alpha value.

(BYSWP=0, HWSWP=0, WSWP=0)

	D[63:60]	D[59:48]	D[47:44]	D[43:32]	D[31:28]	D[27:16]	D[15:12]	D[11:0]
000H	ALPHA1	P1	ALPHA2	P2	ALPHA3	P3	ALPHA4	P4
004H	ALPHA5	P5	ALPHA6	P6	ALPHA7	P7	ALPHA8	P8
008H	ALPHA9	P9	ALPHA10	P10	ALPHA11	P11	ALPHA12	P12
…								

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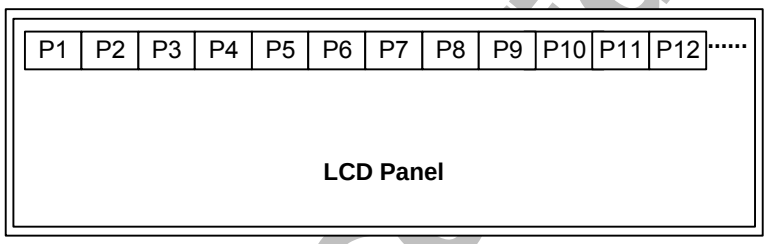
1.3.3.2.10 8BPP Display (A232)

(BYSWP=0, HWSWP=0, WSWP=0)

	D[63]	D[62:56]	D[55]	D[54:48]	D[47]	D[46:40]	D[39]	D[38:32]	D[31]	D[30:24]	D[23]	D[22:16]	D[15]	D[14:8]	D[7]	D[6:0]
000H	AEN	P1	AEN	P2	AEN	P3	AEN	P4	AEN	P5	AEN	P6	AEN	P7	AEN	P8
008H	AEN	P9	AEN	P10	AEN	P11	AEN	P12	AEN	P13	AEN	P14	AEN	P15	AEN	P16
010H	AEN	P17	AEN	P18	AEN	P19	AEN	P20	AEN	P21	AEN	P22	AEN	P23	AEN	P24
...																

(BYSWP=**1**, HWSWP=0, WSWP=0)

	D[63]	D[62:56]	D[55]	D[54:48]	D[47]	D[46:40]	D[39]	D[38:32]	D[31]	D[30:24]	D[23]	D[22:16]	D[15]	D[14:8]	D[7]	D[6:0]
000H	AEN	P8	AEN	P7	AEN	P6	AEN	P5	AEN	P4	AEN	P3	AEN	P2	AEN	P1
008H	AEN	P16	AEN	P15	AEN	P14	AEN	P13	AEN	P12	AEN	P11	AEN	P10	AEN	P9
010H	AEN	P24	AEN	P23	AEN	P22	AEN	P21	AEN	P20	AEN	P19	AEN	P18	AEN	P17
...																



NOTE:

1. AEN: Specifies the transparency value selection bit.
   AEN = 0: Selects ALPHA0.
   AEN = 1: Selects ALPHA1.
   If per-pixel blending is set, then this pixel blends alpha value selected by AEN.
   Alpha value is selected by SFR as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, and ALPHA1_B.
   For more information, refer to the section on “SFR”.
2. D [6:5] = Red data, D [4:2] = Green data, and D [1:0] = Blue data.

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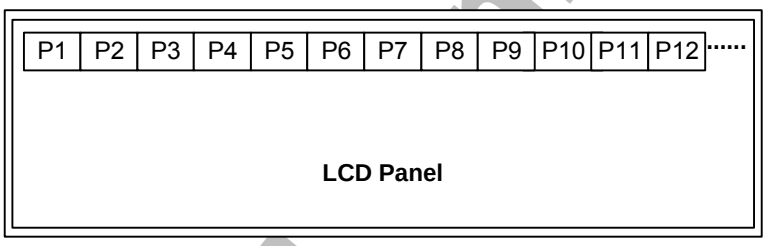
1.3.3.2.11 8BPP Display (Palette)

(BYSWP=0, HWSWP=0, WSWP=0)

	D[63:56]	D[55:48]	D[47:40]	D[39:32]	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P1	P2	P3	P4	P5	P6	P7	P8
008H	P9	P10	P11	P12	P13	P14	P15	P16
010H	P17	P18	P19	P20	P21	P22	P23	P24
…								

(BYSWP=1, HWSWP=0, WSWP=0)

	D[63:56]	D[55:48]	D[47:40]	D[39:32]	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P8	P7	P6	P5	P4	P3	P2	P1
008H	P16	P15	P14	P13	P12	P11	P10	P9
010H	P24	P23	P22	P21	P20	P19	P18	P17
…								



NOTE: AEN: Specifies the transparency value selection bit (with WPALCON: Palette output format).
AEN = 0: Selects ALPHA0.
AEN = 1: Selects ALPHA1.
If per-pixel blending is set, then this pixel blends with alpha value selected by AEN.
Alpha value is selected by SFR as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, and ALPHA1_B.
For more information, refer to the section on “SFR”.

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1.3.3.2.12 4BPP Display (Palette)

(BYSWP=0, HWSWP=0, WSWP=0)

	D[63:60]	D[59:56]	D[55:52]	D[51:48]	D[47:44]	D[43:40]	D[39:36]	D[35:32]
000H	P1	P2	P3	P4	P5	P6	P7	P8
008H	P17	P18	P19	P20	P21	P22	P23	P24
…								

	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
000H	P9	P10	P11	P12	P13	P14	P15	P16
008H	P25	P26	P27	P28	P29	P30	P31	P32
…								

(BYSWP=1, HWSWP=0, WSWP=0)

	D[63:60]	D[59:56]	D[55:52]	D[51:48]	D[47:44]	D[43:40]	D[39:36]	D[35:32]
000H	P15	P16	P13	P14	P11	P12	P9	P10
008H	P31	P32	P29	P30	P27	P28	P25	P26
…								

	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
000H	P7	P8	P5	P6	P3	P4	P1	P2
008H	P23	P24	P21	P22	P19	P20	P17	P18
…								

NOTE: AEN: Specifies the transparency value selection bit (with WPALCON: Palette output format)
AEN = 0: Selects ALPHA0.
AEN = 1: Selects ALPHA1.
If per-pixel blending is set, then this pixel blends with alpha value selected by AEN.
Alpha value is selected by SFR as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, and ALPHA1_B.
For more information, refer to the section on “SFR”.

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1.3.3.2.13 2BPP Display (Palette)

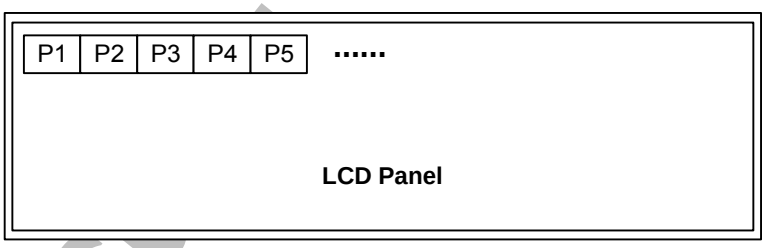
(BYSWP=0, HWSWP=0, WSWP=0)

	D[63:62]	D[61:60]	D[59:58]	D[57:56]	D[55:54]	D[53:52]	D[51:50]	D[49:48]
000H	P1	P2	P3	P4	P5	P6	P7	P8
008H	P33	P34	P35	P36	P37	P38	P39	P40
…								

	D[47:46]	D[45:44]	D[43:42]	D[41:40]	D[39:38]	D[37:36]	D[35:34]	D[33:32]
000H	P9	P10	P11	P12	P13	P14	P15	P16
008H	P41	P42	P43	P44	P45	P46	P47	P48
…								

	D[31:30]	D[29:28]	D[27:26]	D[25:24]	D[23:22]	D[21:20]	D[19:18]	D[17:16]
000H	P17	P18	P19	P20	P21	P22	P23	P24
008H	P49	P50	P51	P52	P53	P54	P55	P56
…								

	D[15:14]	D[13:12]	D[11:10]	D[9:8]	D[7:6]	D[5:4]	D[3:2]	D[1:0]
000H	P25	P26	P27	P28	P29	P30	P31	P32
008H	P57	P58	P59	P60	P61	P62	P63	P64
…								



NOTE: AEN: Specifies the transparency value selection bit (with WPALCON: Palette output format).
AEN = 0: Selects ALPHA0.
AEN = 1: Selects ALPHA1.
If per-pixel blending is set, then this pixel blends with alpha value selected by AEN.
Alpha value is selected by SFR as ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, and ALPHA1_B.
For more information, refer to the section on “SFR”.

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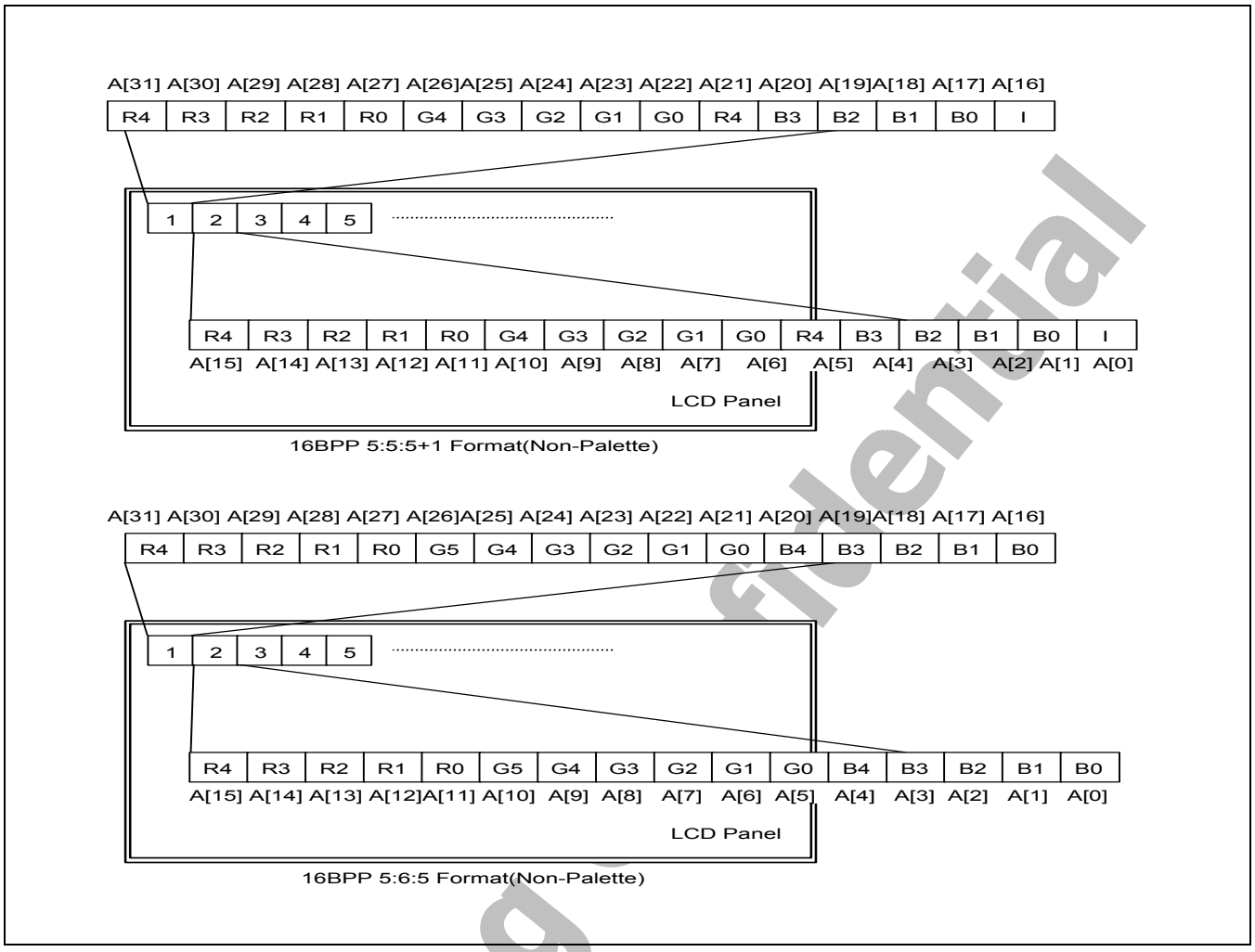

Figure 1-4 16BPP (5:6:5) Display Types

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1.3.4 COLOR SPACE CONVERSION (CSC)

1.3.4.1 Color Space Conversion YCbCr to RGB (CSCY2R)

CSCY2R (Color Space Conversion Y to R)

		601	709
Wide	R =	Y + 1.371(Cr - 128)	Y + 1.540(Cr - 128)
	G =	Y – 0.698(Cr – 128) – 0.336(Cb – 128)	Y – 0.459(Cr – 128) – 0.183(Cb – 128)
	B =	Y + 1.732(Cb – 128)	Y + 1.816(Cb – 128)
Narrow	R =	1.164(Y – 16) + 1.596(Cr - 128)	1.164(Y – 16) + 1.793(Cr - 128)
	G =	1.164(Y – 16) – 0.813(Cr – 128) – 0.391(Cb – 128)	1.164(Y – 16) – 0.534(Cr – 128) – 0.213(Cb – 128)
	B =	1.164(Y – 16) + 2.018(Cb – 128)	1.164(Y – 16) + 2.115(Cb – 128)

NOTE: "Wide" means RGB data has a nominal range from 16 to 235. On the other hand, "Narrow" means RGB data has a nominal range from 0 to 255.

Coefficient approximation.

- 1.164 = (2^7 + 2^4 + 2^2 + 2^0) >> 7
- 1.596 = (2^7 + 2^6 + 2^3 + 2^2) >> 7
- 0.813 = (2^6 + 2^5 + 2^3) >>7
- 0.391 = (2^5 + 2^4 + 2^1) >> 7
- 2.018 = (2^8 + 2^1) >> 7

1,793 = (2^7 + 2^6 + 2^5 + 2^2 + 2^1) >> 7

0.534 = (2^6 + 2^2) >> 7

0.213 = (2^4 + 2^3 + 2^1 + 2^0) >> 7

2.115 = (2^8 + 2^3 + 2^2 + 2^1 + 2^0) >> 7

- 1.371 = (2^8 + 2^6 + 2^4 + 2^3 + 2^2 + 2^1 + 2^0) >> 8
- 0.698 = (2^7 + 2^5 + 2^4 + 2^1 + 2^0) >> 8
- 0.336 = (2^6 + 2^4 + 2^2 + 2^1) >> 8
- 1.732 = (2^8 + 2^7 + 2^5 + 2^4 + 2^3 + 2^1 + 2^0) >> 8

1.540 = (2^8 + 2^7 + 2^3 + 2^1) >> 8

0.459 = (2^6 + 2^5 + 2^4 + 2^2 + 2^1) >> 8

0.183 = (2^5 + 2^3 + 2^2 + 2^1 + 2^0) >> 8

1.816 = (2^8 + 2^7 + 2^6 + 2^4 + 2^0) >> 8

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1.3.4.2 Color Space Conversion RGB to YCbCr (CSCR2Y)

CSCR2Y (Color Space Conversion R to Y)

		601	709
Wide	Y =	0.299R + 0.587G + 0.114B	0.213R + 0.715G + 0.072B
	Cb =	- 0.172R - 0.339G + 0.511B + 128	- 0.117R - 0.394G + 0.511B + 128
	Cr =	0.511R – 0.428G – 0.083B + 128	0.511R – 0.464G – 0.047B + 128
Narrow	Y =	0.257R + 0.504G + 0.098B + 16	0.183R + 0.614G + 0.062B + 16
	Cb =	- 0.148R - 0.291G + 0.439B + 128	- 0.101R - 0.338G + 0.439B + 128
	Cr =	0.439R – 0.368G – 0.071B + 128	0.439R – 0.399G – 0.040B + 128

NOTE: "Wide" means RGB data has a nominal range from 16 to 235. On the other hand, "Narrow" means RGB data has a nominal range from 0 to 255.

Coefficient approximation.

- 0.257 = (2^6 + 2^1) >> 8
- 0.504 = (2^7 + 2^0) >> 8
- 0.098 = (2^4 + 2^3 + 2^0) >> 8
- 0.148 = (2^5 + 2^2 + 2^1) >> 8
- 0.291 = (2^6 + 2^3 + 2^1) >> 8
- 0.439 = (2^6 + 2^5 + 2^4) >> 8
- 0.368 = (2^7 – 2^5 – 2^1) >> 8
- 0.071 = (2^4 + 2^1) >> 8

0.183 = (2^5 + 2^3 + 2^2 + 2^1 + 2^0) >> 8

0.614 = (2^7 + 2^4 + 2^3 + 2^2 + 2^0) >> 8

0.062 = (2^4) >> 8

0.101 = (2^4 + 2^3 + 2^1) >> 8

0.338 = (2^6 + 2^4 + 2^2 + 2^1 + 2^0) >> 8

0.399 = (2^6 + 2^5 + 2^2 + 2^1) >> 8

0.040 = (2^3 + 2^1) >> 8

- 0.299 = (2^6 + 2^3 + 2^2 + 2^0) >> 8
- 0.587 = (2^7 + 2^4 + 2^2 + 2^1) >> 8
- 0.114 = (2^4 + 2^3 + 2^2 + 2^0) >> 8
- 0.172 = (2^5 + 2^3 + 2^2) >> 8
- 0.339 = (2^6 + 2^4 + 2^3 – 2^0) >> 8
- 0.511 = (2^7 + 2^1 + 2^0) >> 8
- 0.428 = (2^7 – 2^4 – 2^1) >> 8
- 0.083 = (2^4 + 2^2 + 2^0) >> 8

0.213 = (2^5 + 2^4 + 2^2 + 2^1 + 2^0) >> 8

0.715 = (2^7 + 2^5 + 2^4 + 2^2 + 2^1 + 2^0) >> 8

0.072 = (2^4 + 2^1) >> 8

0.117 = (2^4 + 2^3 + 2^2 + 2^1) >> 8

0.394 = (2^6 + 2^5 + 2^2 + 2^0) >> 8

0.464 = (2^6 + 2^5 + 2^4 + 2^2 + 2^1 + 2^0) >> 8

0.047 = (2^3 + 2^2) >> 8

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1.3.5 PALETTE USAGE

1.3.5.1 Palette Configuration and Format Control

The display controller supports 256-color palette to select color mapping. You can select up to 256 colors from 32-bit colors using these formats.

256 color palette consists of 256 (depth) × 32-bit SPSRAM. Palette supports 8:8:8, 6:6:6, 5:5:5 (R: G: B), and other formats.

For Example:

See A:5:5:5 format, write palette, as shown in *Table 1-2*.

Connect VD pin to TFT LCD panel (R(5)=VD[23:19], G(5)=VD[15:11], and B(5)=VD[7:3]). AEN bit controls the blending function, enable or disable. Finally, set WPALCON (W1PAL, case window0) register to 0'b101. The 32-bit (8:8:8:8) format has an alpha value directly, without using alpha value register (ALPHA_0/1).

Table 1-1 32BPP (8:8:8:8) Palette Data Format

INDEX / Bit Pos.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	ALPHA								R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
01h	ALPHA								R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
.....	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
FFh	ALPHA								R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Number of VD	-	-	-	-	-	-	-	-	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 1-2 25BPP (A: 8:8:8) Palette Data Format

INDEX / Bit Pos.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	-	-	-	-	-	-	-	AEN	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
01h	-	-	-	-	-	-	-	AEN	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
.....	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
FFh	-	-	-	-	-	-	-	AEN	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Number of VD	-	-	-	-	-	-	-	-	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Table 1-3 19BPP (A: 6:6:6) Palette Data Format

INDEX / Bit Pos.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	-	-	-	-	-	-	-	-	-	-	-	-	-	AEN	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
01h	-	-	-	-	-	-	-	-	-	-	-	-	-	AEN	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
.....	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
FFh	-	-	-	-	-	-	-	-	-	-	-	-	-	AEN	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Number of VD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	23	22	21	20	19	18	15	14	13	12	11	10	7	6	5	4	3	2

Table 1-4 16BPP (A: 5:5:5) Palette Data Format

INDEX / Bit Pos.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AEN	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
01h	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AEN	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
.....	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
FFh	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AEN	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
Number of VD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	23	22	21	20	19	15	14	13	12	11	7	6	5	4	3

1.3.5.2 Palette Read/ Write

You should not access palette memory when the Vertical Status (VSTATUS) register has an ACTIVE status. VSTATUS must be checked to do Read/ Write operation on the palette.

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1.3.6 WINDOW BLENDING

1.3.6.1 Overview of Window Blending

The main function of the VPRCS module is window blending. Display controller comprises five window layers (win0 ~ win4).

Example of Application:

The system uses

win0 as OS window, full TV screen window, and so on.

win1 as small (next channel) TV screen with win2 as menu.

win3 as caption.

win 4 as channel information.

win3 and win4 have color limitation while using color index with Color LUT. This feature enhances the system performance by reducing the data rate of total system.

Example of Total Five Windows:

win 0 (base): Local/ (YCbCr, RGB without palette)

win 1 (Overlay1): RGB with palette

win 2 (Overlay2): RGB with palette

win 3 (Caption): RGB (1/2/4) with 16-level Color LUT

win 4 (Cursor): RGB (1/2) with 4-level Color LUT

Overlay Priority

Win 4 > Win 3 > Win 2 > Win 1 > Win 0

Color Key

The register value to ColorKey register must be set by 24-bit RGB format.

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Blending Equation

<Data blending>

Win01(R,G,B) = Win0(R,G,B) x b1 + Win1(R,G,B) x a1
Win012(R/G/B) = Win01(R/G/B) x b2 + Win2(R/G/B) x a2
Win0123(R/G/B) = Win012(R/G/B) x b3 + Win3(R/G/B) x a3
WinOut(R/G/B) = Win0123(R/G/B) x b4 + Win4(R/G/B) x a4

, where,

Win0(R) = Window 0's Red data,
Win0(G) = Window 0's Green data,
Win0(B) = Window 0's Blue data,
Win1(R) = Window 1's Red data,
...
b1 = Background's Data blending equation1 factor,
a1 = Foreground's Data blending equation1 factor,
b2 = Background's Data blending equation2 factor,
a2 = Foreground's Data blending equation2 factor,

<Alpha value blending>

AR(G,B)01 = AR(G,B)0 x q1 + AR(G,B)1 x p1
AR(G,B)012 = AR(G,B)01 x q2 + AR(G,B)2 x p2
AR(G,B)0123 = AR(G,B)012 x q3 + AR(G,B)3 x p3

, where,

AR0 = Window 0's Red blending factor,
AG0 = Window 0's Green blending factor,
AB0 = Window 0's Blue blending factor,
AR1 = Window 1's Red blending factor,...
AR01 = Window01's Red blending factor (alpha value blending between AR0 and AR1),
AG01 = Window01's Green blending factor (alpha value blending between AG0 and AG1),
AB01 = Window01's Blue blending factor (alpha value blending between AB0 and AB1),
AR012 = Window012's Red blending factor (alpha value blending between AR01 and AR2),
...
q1 = Background's Alpha value blending equation1 factor,
p1 = Foreground's Alpha value blending equation1 factor,
q2 = Background's Alpha value blending equation2 factor,
p2 = Foreground's Alpha value blending equation2 factor,…

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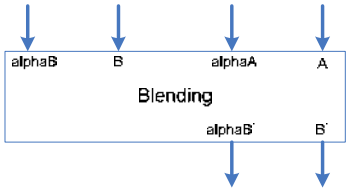

B' = a x A + b x B

alphaB' = p x alphaA + q x alphaB

a/b/p/q = 0	'a' is controlled by 'A_FUNC' @ BLENDEQ register	
or 1	'b'	" by 'B_FUNC' @ BLENDEQ register
or alphaA	'p'	" by 'P_FUNC' @ BLENDEQ register
or 1 - alphaA	'q'	" by 'Q_FUNC' @ BLENDEQ register
or alphaB		
or 1 - alphaB		
or A		
or 1 - A		
or B		
or 1 - B		
or ALPHA0		

Figure 1-5 Blending Equation

< Default blending equation >

Data blending>
B' = B x (1-alphaA) + A x alphaA

Alpha value blending>
alphaB' = 0 (= alphaB x 0 + alphaA x 0)

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1.3.6.2 Blending Diagram

The display controller can blend five layers for one pixel at the same time. ALPHA0_R, ALPHA0_G, ALPHA0_B, ALPHA1_R, ALPHA1_G, and ALPHA1_B registers control the alpha value (blending factor), which are implemented for each window layer and color (R,G,B).

The example below shows the R (Red) output using ALPHA_R value of each window.

All windows have two kinds of alpha blending value:

- Alpha value for transparency enable (AEN value ==1)
- Alpha value for transparency disable (AEN value == 0).

If WINEN_F and BLD_PIX are enabled and ALPHA_SEL is disabled, then AR is chosen using the following equation:

- AR = (Pixel(R)'s AEN value == 1'b1) ? Reg(ALPHA1_R) : Reg(ALPHA0_R);
- AG = (Pixel(G)'s AEN value == 1'b1) ? Reg(ALPHA1_G) : Reg(ALPHA0_G);
- AB = (Pixel(B)'s AEN value == 1'b1) ? Reg(ALPHA1_B) : Reg(ALPHA0_B);
  (where, BLD_ PIX == 1, ALPHA_SEL == 0)

If WINEN_F is enabled and BLD_PIX is disabled, then AR is controlled by ALPHA_SEL ALPHA0. AEN bit information is not used anymore.

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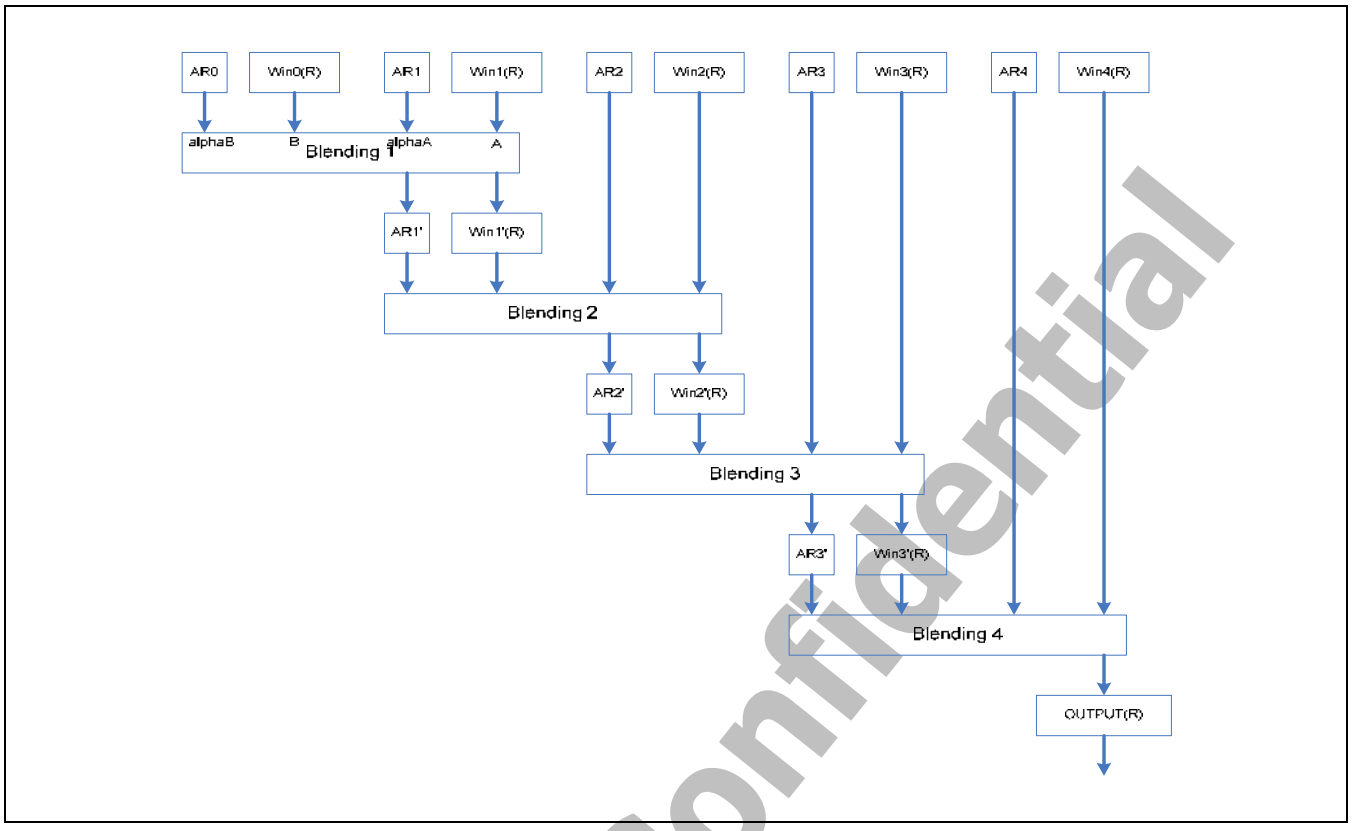

Figure 1-6 Blending Diagram

Example:

Window n's blending factor decision (n=0, 1, 2, 3, 4). For more information, refer to the section on "SFR".

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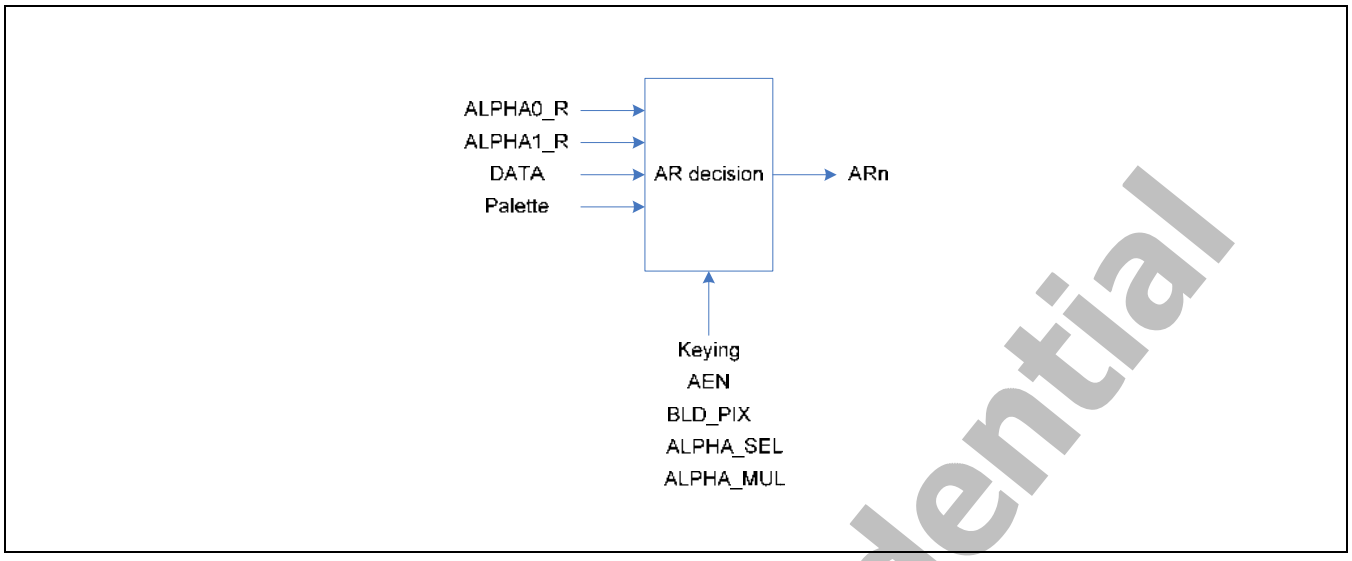

Figure 1-7 Blending Factor Decision

NOTE: If DATA [15:12] (BPPMODE_F = b'1110, ARGB4444 format) is used to blend, alpha value is {DATA [15:12], DATA [15:12]} (4-bit -> 8-bit expanding).

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1.3.6.3 Color-Key Function

The Color-Key function in display controller supports various effects for image mapping. For special functionality, the Color-Key register that specifies the color image of OSD layer is substituted by the background image--either as cursor image or preview image of the camera.

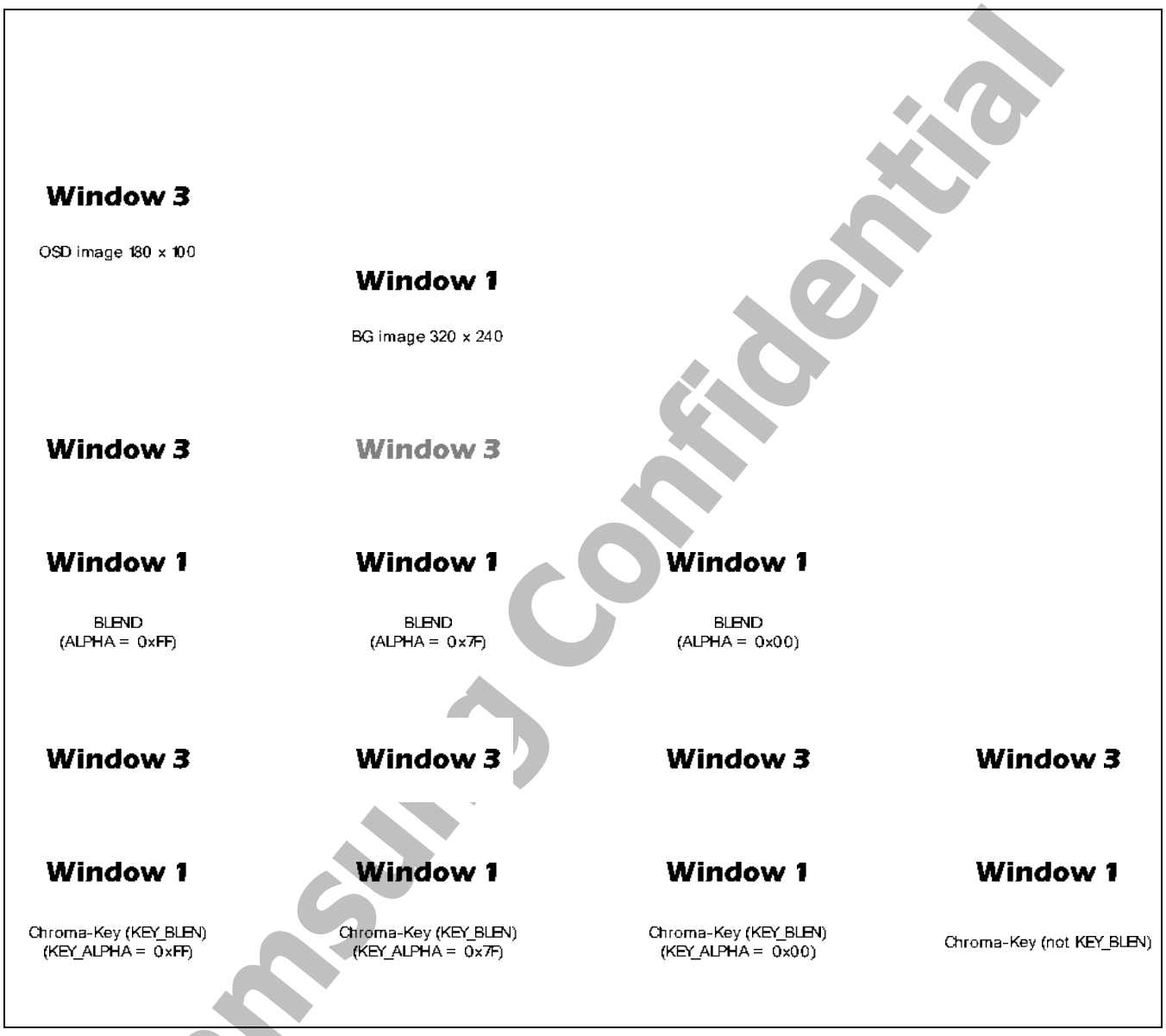

Figure 1-8 Color-Key Function Configurations

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1.3.6.4 Blending and COLOR-KEY Function

The display controller supports simultaneous blending function--with two transparency factors and Color-Key function in the same window.

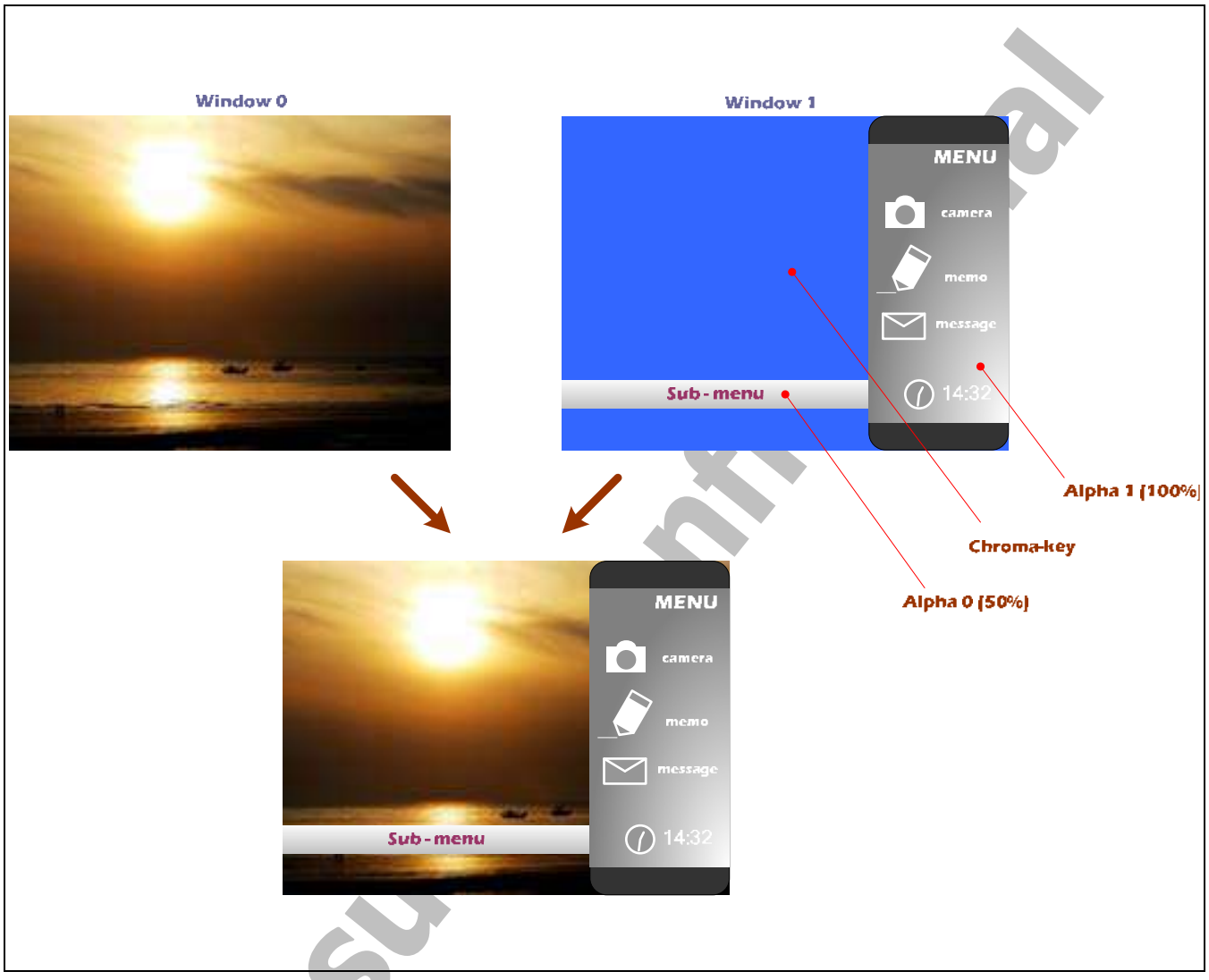

Figure 1-9 Blending and Color-Key Function

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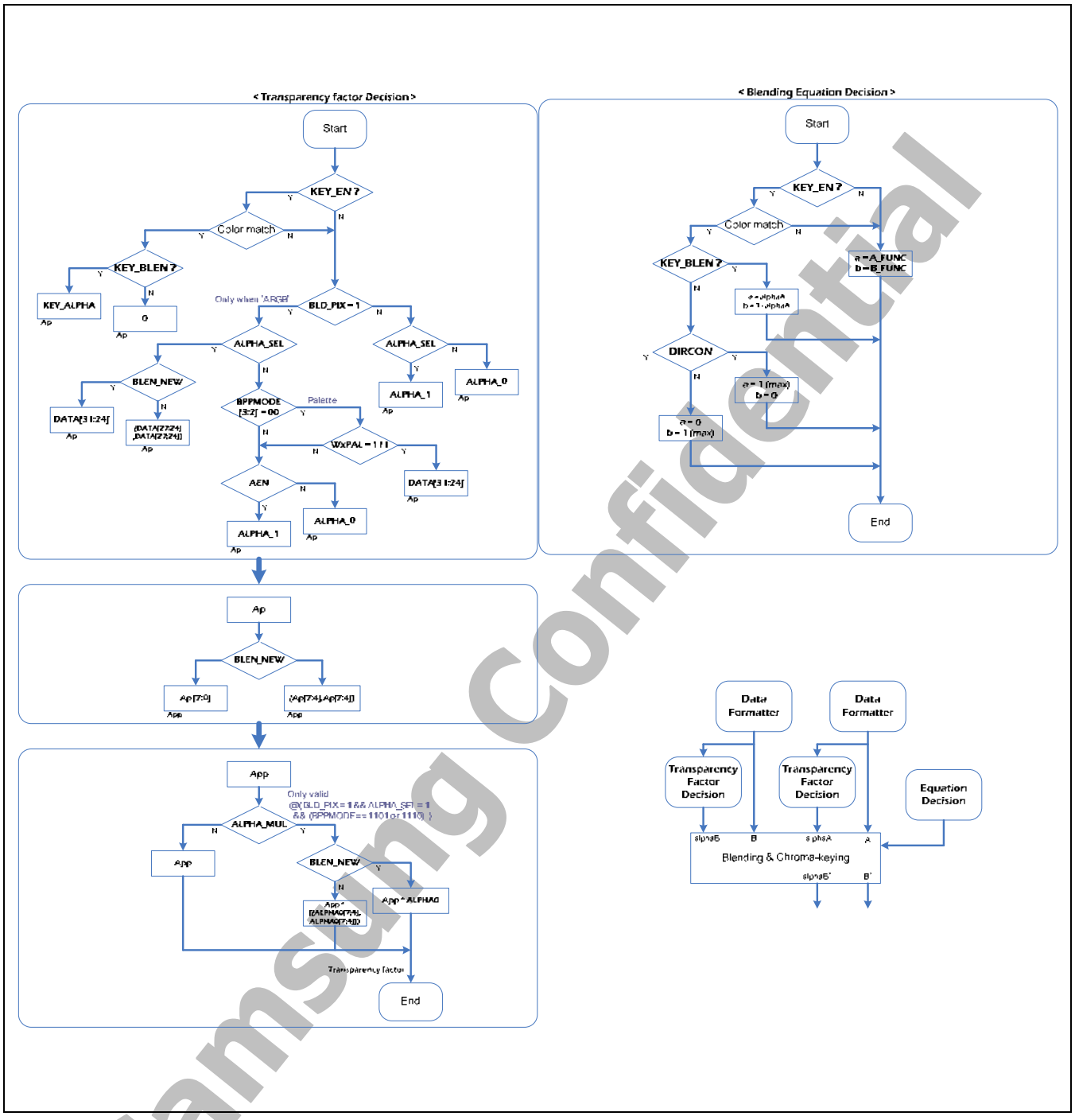

Figure 1-10 Blending Decision Diagram

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1.3.7 IMAGE ENHANCEMENT

1.3.7.1 Overview of Image Enhancement

One of the main functions of the VPRCS module is Image Enhancement. The display controller supports Gamma, Hue, Color Gain, and Pixel Compensation Control functions.

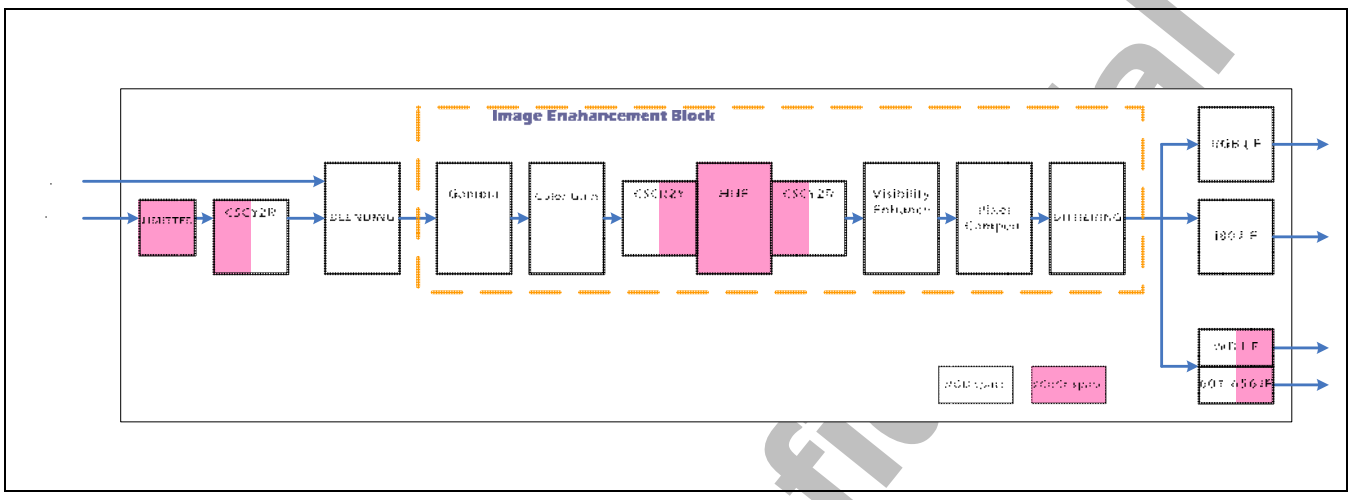

Figure 1-11 Image Enhancement Flow

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1.3.7.2 Gamma Control

Gamma control comprises of 65 LUT registers. The output value is determined by piecewise-linear operation between two LUT registers. The output value saturates at 255.

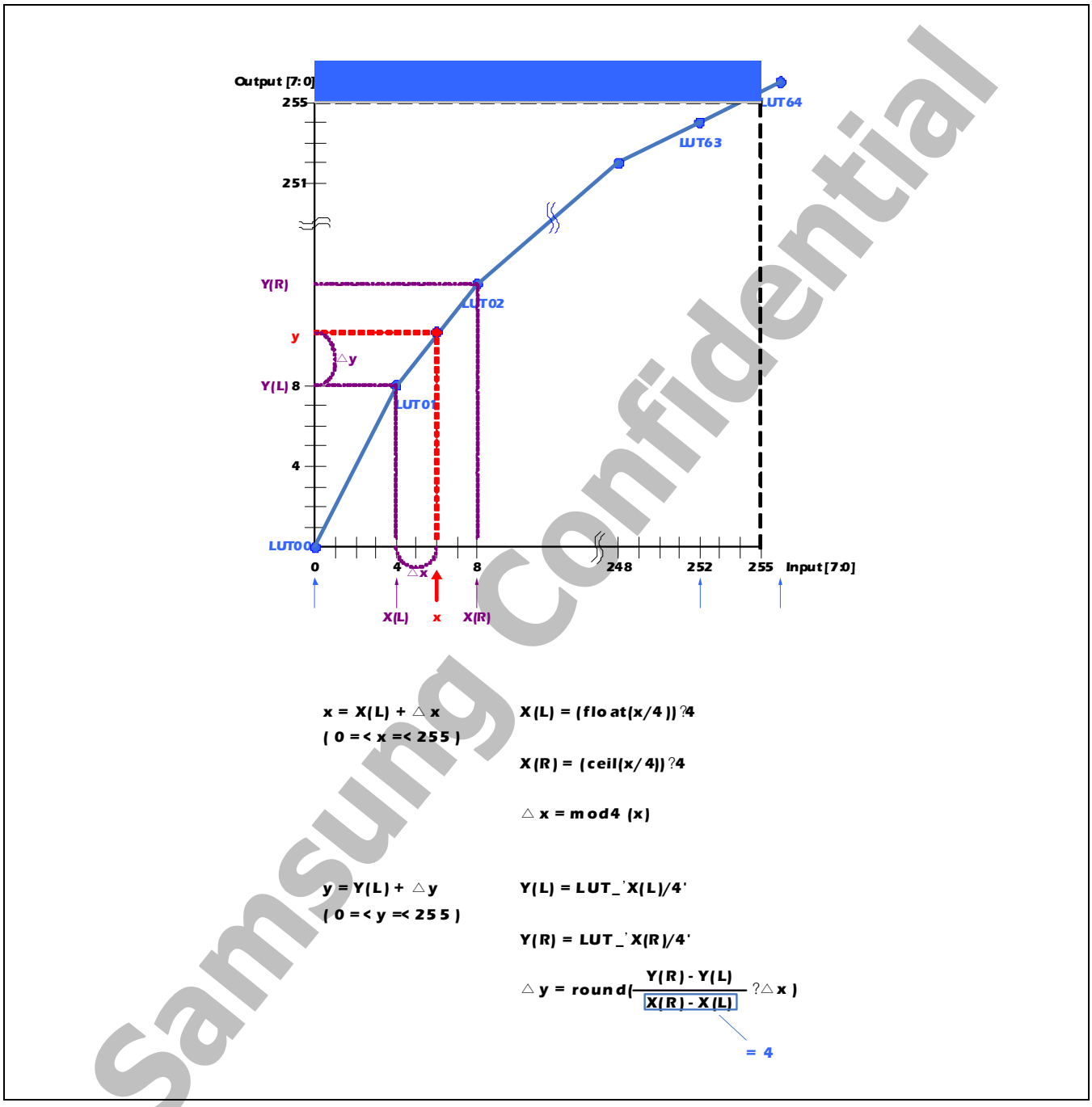

Figure 1-12 Image Enhancement Flow

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1.3.7.3 Color Gain Control

The Color Gain Control comprises of three registers for each color: Red, Green, and Blue. The maximum value of Color Gain is 3.99609375 (approximately 4) and it has an 8-bit resolution.

- R (color gain) = R • CG_RGAIN
- G (color gain) = G • CG_GGAIN
- B (color gain) = B • CG_BGAIN

CG_R(G,B)GAIN comprises of 2-bit integer and 8-bit fraction.

(Maximum value is approximately 4 with 8-bit resolution.) The output value saturates at 255.

1.3.7.4 Hue Control

Hue Control comprises of eight registers for coefficients of Hue matrix.

- Cb<hue> = CBG0•(Cb + OFFSET_IN) + CBG1•(Cr + OFFSET_IN) + OFFSET_OUT
- Cr<hue> = CRG0•(Cb + OFFSET_IN) + CRG1•(Cr + OFFSET_IN) + OFFSET_OUT
  (In general, OFFSET_IN is '-128' and OFFSET_OUT is '+128'.)
- CBG0 = (Cb + OFFSET_IN)>=0 ? CBG0_P : CBG0_N
- CBG1 = (Cr + OFFSET_IN)>=0 ? CBG1_P : CBG1_N
- CRG0 = (Cb + OFFSET_IN)>=0 ? CRG0_P : CRG0_N
- CRG0 = (Cr + OFFSET_IN)>=0 ? CRG1_P : CRG1_N

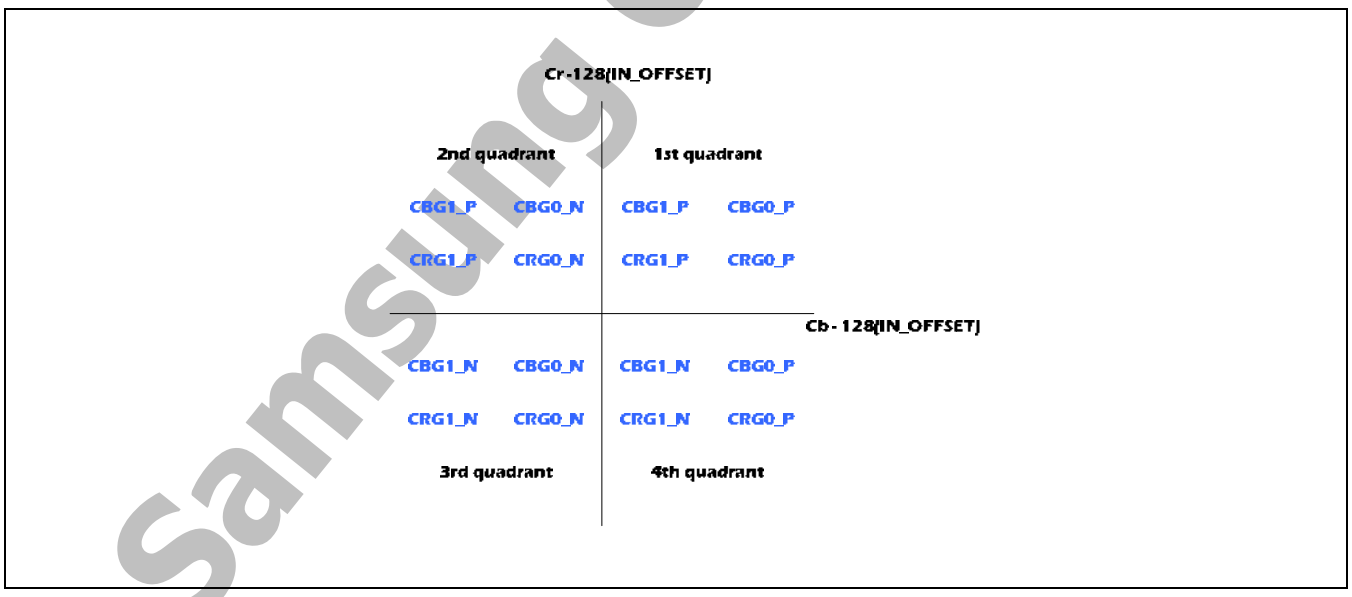

Figure 1-13 Hue Coefficient Decision

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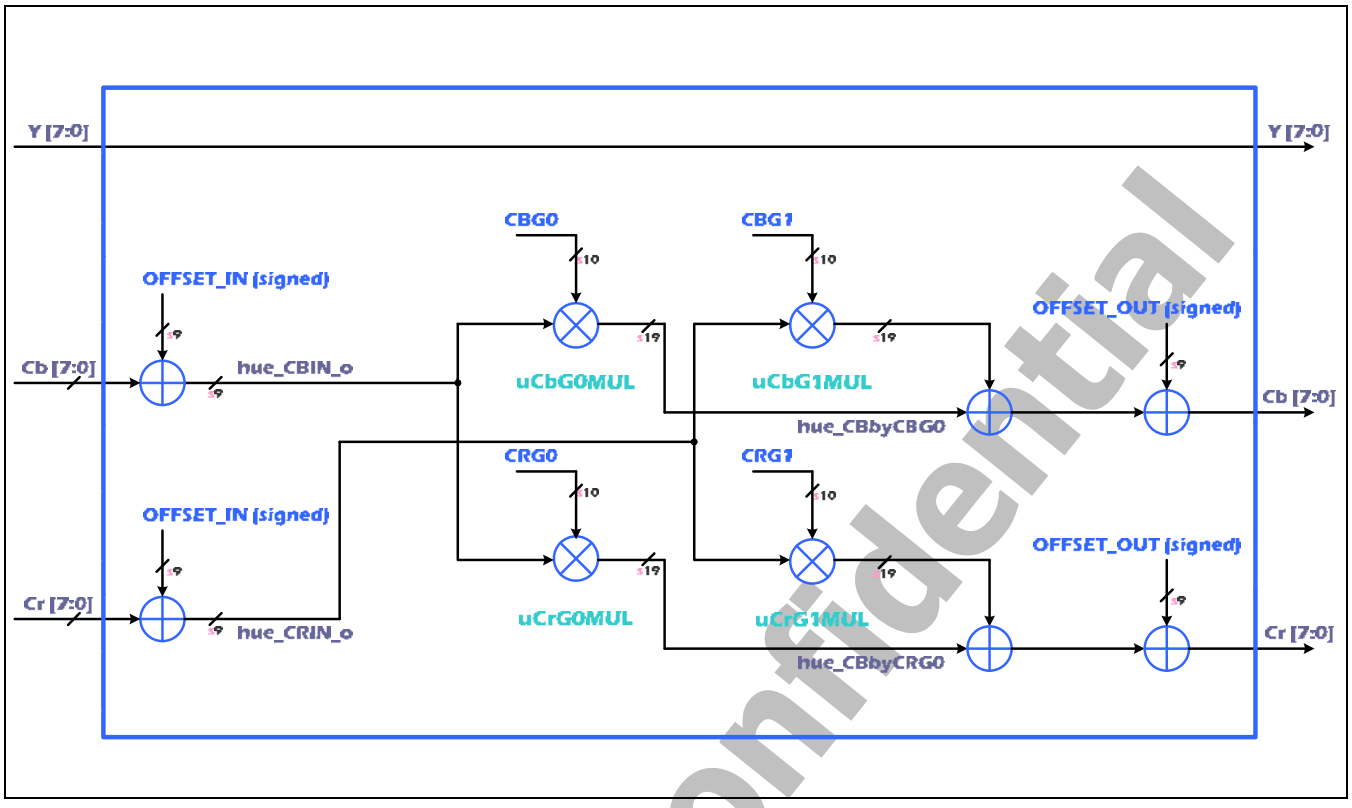

Figure 1-14 Hue Control Block Diagram

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1.3.7.5 Pixel Compensation Control

The purpose of Pixel Compensation Control is to compensate data for delta-structure.

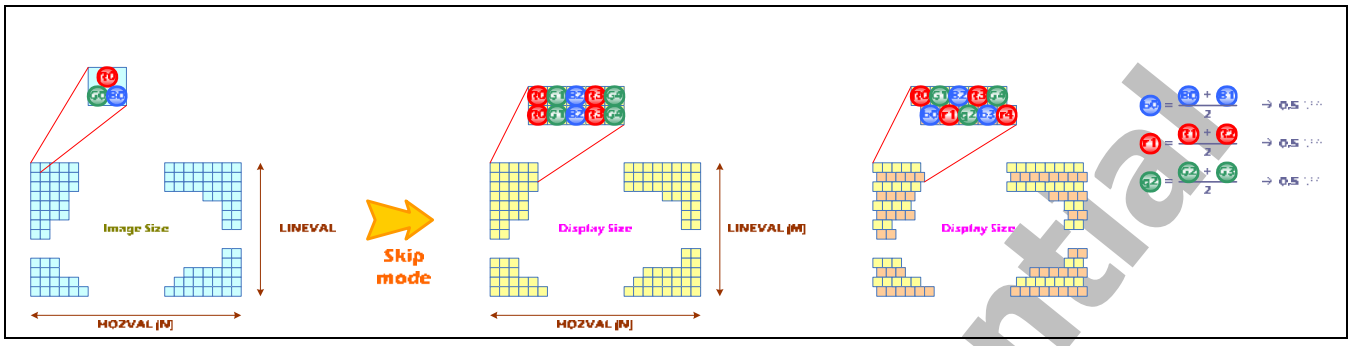

Figure 1-15 Example1. RGBSPSEL==1'b0, RGB_SKIP==1'b1, PIXCOMPEN_DIR==1'b0

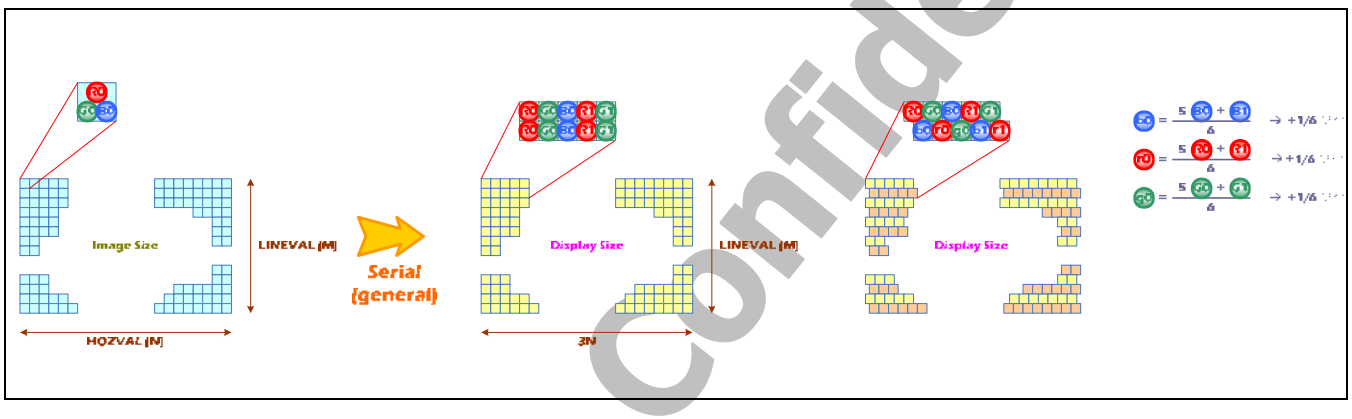

Figure 1-16 Example2. RGBSPSEL==1'b1, PIXCOMPEN_DIR==1'b0

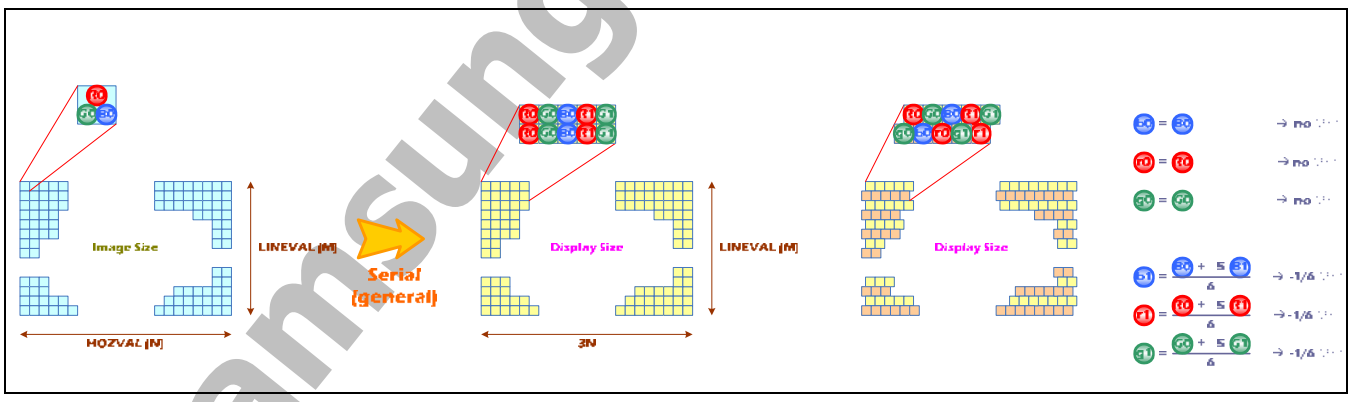

Figure 1-17 Example3. RGBSPSEL==1'b1, PIXCOMPEN_DIR==1'b1

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1.3.8 VTIME CONTROLLER OPERATION

VTIME comprises of two blocks, namely:

- VTIME_RGB_TV for RGB timing control
- VTIME_I80 for indirect i80 interface timing control

1.3.8.1 RGB Interface Controller

VTIME generates control signals such as RGB_VSYNC, RGB_HSYNC, RGB_VDEN, and RGB_VCLK signal for the RGB interface. These control signals are used while configuring the VIDTCON0/ 1/ 2 registers in the VSFR register.

Based on the programmable configurations of display control registers in the VSFR, the VTIME module generates programmable control signals that support different types of display devices.

The RGB_VSYNC signal causes the LCD line pointer to begin at the top of display. The configuration of both HOZVAL field and LINEVAL registers control pulse generation of RGB_VSYNC and RGB_HSYNC. Based on the following equations, the size of the LCD panel determines HOZVAL and LINEVAL:

- HOZVAL = (Horizontal display size) -1
- LINEVAL = (Vertical display size) -1

The CLKVAL field in VIDCON0 register controls the rate of RGB_VCLK signal. *Table 1-5* defines the relationship of RGB_VCLK and CLKVAL. The minimum value of CLKVAL is 1.

- RGB_VCLK (Hz) =HCLK/ (CLKVAL+1), where CLKVAL >= 1

Table 1-5 Relation 16BPP Between VCLK and CLKVAL (TFT, Frequency of Video Clock Source=60MHz)

CLKVAL	60MHz/X	VCLK
2	60 MHz/3	20.0 MHz
3	60 MHz/4	15.0 MHz
:	:	:
63	60 MHz/64	937.5 kHz

VSYNC, VBPD, VFPD, HSYNC, HBPD, HFPD, HOZVAL, and LINEVAL configure RGB_HSYNC and RGB_VSYNC signal. For more information, refer to Figure 9.1-20.

The frame rate is RGB_VSYNC signal frequency. The frame rate is related to the field of VSYNC, VBPD, VFPD, LINEVAL, HSYNC, HBPD, HFPD, HOZVAL, and CLKVAL registers. Most LCD drivers need their own adequate frame rate.

To calculate frame rate, use the following equation:

- Frame Rate = 1/ [{ (VSPW+1) + (VBPD+1) + (LIINEVAL + 1) + (VFPD+1) } x {(HSPW+1) + (HBPD +1) + (HFPD+1) + (HOZVAL + 1) } x { (CLKVAL+1) / (Frequency of Clock source) }]

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1.3.8.2 I80 Interface Controller

VTIME_I80 controls display controller for CPU style LDI. It has the following functions:

- Generates I80 Interface Control Signals
- CPU style LDI Command Control
- Timing Control for VDMA and VDPRCS

1.3.8.3 Output Control Signal Generation

VTIME_I80 generates SYS_CS0, SYS_CS1, SYS_WE, and SYS_RS control signals (For Timing Diagram, refer to Figure 9.1-27). Their timing parameters, LCD_CS_SETUP, LCD_WR_SETUP, LCD_WR_ACT, and LCD_WR_HOLD are set through I80IFCONA0 and I80IFCONA1 SFRs.

1.3.8.4 Partial Display Control

Although partial display is the main feature of CPU style LDI, VTIME_I80 does not support this function in hardware logic.

This function is implemented by SFR setting (LINEVAL, HOZVAL, OSD_LeftTopX_F, OSD_LeftTopY_F, OSD_RightBotX_F, OSD_RightBotY_F, PAGEWIDTH, and OFFSIZE).

1.3.8.5 LDI Command Control

LDI receives both command and data. Command specifies an index for selecting the SFR in LDI. In control signal for command and data, only SYS_RS signal has a special function. Usually, SYS_RS has a polarity of '1' for issuing command and vice versa.

Display controller has two kinds of command control:

- Auto command
- Normal command

Auto command is issued automatically, that is, without software control and at a pre-defined rate (rate = 2, 4, 6, ...30). If the rate is equal to 4, it implies that auto commands are send to LDI at the end of every 4 image frames. The software control issues Normal command.

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1.3.9 SETTING OF COMMANDS

1.3.9.1 Auto Command

If 0x1 (index), 0x32, 0x2 (index), 0x8f, 0x4 (index), or 0x99 are required to be sent to LDI at every 10 frames, the following steps are recommended:

- LDI_CMD0 ← 0x1, LDI_CMD1 ← 0x32, LDI_CMD2 ← 0x2,
- LDI_CMD3 ← 0x8f, LDI_CMD4 ← 0x4, LDI_CMD5 ← 0x99
- CMD0_EN ← 0x2, CMD1_EN ← 0x2, CMD2_EN ← 0x2,
- CMD3_EN ← 0x2, CMD4_EN ← 0x2, CMD5_EN ← 0x2
- CMD0_RS ← 0x1, CMD1_RS ← 0x0, CMD2_RS ← 0x1,
- CMD3_RS ← 0x0, CMD4_RS ← 0x1, CMD5_RS ← 0x0
- AUTO_CMD_RATE ← 0x5

NOTE:

1. For checking RS polarity, refer to your LDI specification.
2. It is not required to pack LDI_CMD from LDI_CMD0 to LDI_CMD11 contiguously. For example, it is only possible to use LDI_CMD0, LDI_CMD3, and LDI_CMD11.
3. Maximum 12 auto commands are available.

1.3.9.2 Normal Command

To execute Normal command, follow these steps:

Put commands into LDI_CMD0 ~ 11 (maximum 12 commands).

Set CMDx_EN in LDI_CMDCON0 to enable normal command x (For example, if you want to enable command 4, you have to set CMD4_EN to 0x01).

Set NORMAL_CMD_ST in I80IFCONB0/1.

The display controller has the following characteristics for command operations:

- Auto/ Normal/ Auto and Normal command mode is possible for each of the 12 commands.
- Sends 12 maximum commands between frames in its normal operation (Normal operation means ENVID=1 and video data is displayed in LCD panel).
- Issues commands in the order of CMD0 → CMD1 → CMD2 → CMD3 → … → CMD10 → CMD11.
- Skips disabled commands (CMDx_EN = 0x0).
  - Sends over 12 commands (Possible in Normal command and system initialization).
  - Set 12 LDI_CMDx, CMDx_EN, and CMDx_RS.
  - Set NORMAL_CMD_ST.
  - Read NORMAL_CMD_ST with polling. If 0, go to NORMAL_CMD_ST setting.

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1.2.7.2.1 Command Setting Example

** CMD0_EN = 2'b10, CMD1_EN = 2'b11, CMD2_EN = 2'b01, CMD3_EN = 2'b11, and CMD4_EN = 2'b01 (Auto Command: CMD0, CMD1, CMD3, Normal Command: CMD1, CMD2, CMD3, and CMD4)

** AUTO_COMMAND_RATE = 4'b0010 (per 4 frames)

** CMD0_RS = 1, CMD1_RS = 1, CMD2_RS = 0, CMD3_RS = 1, and CMD4_RS = 0.

** RSPOL = 0

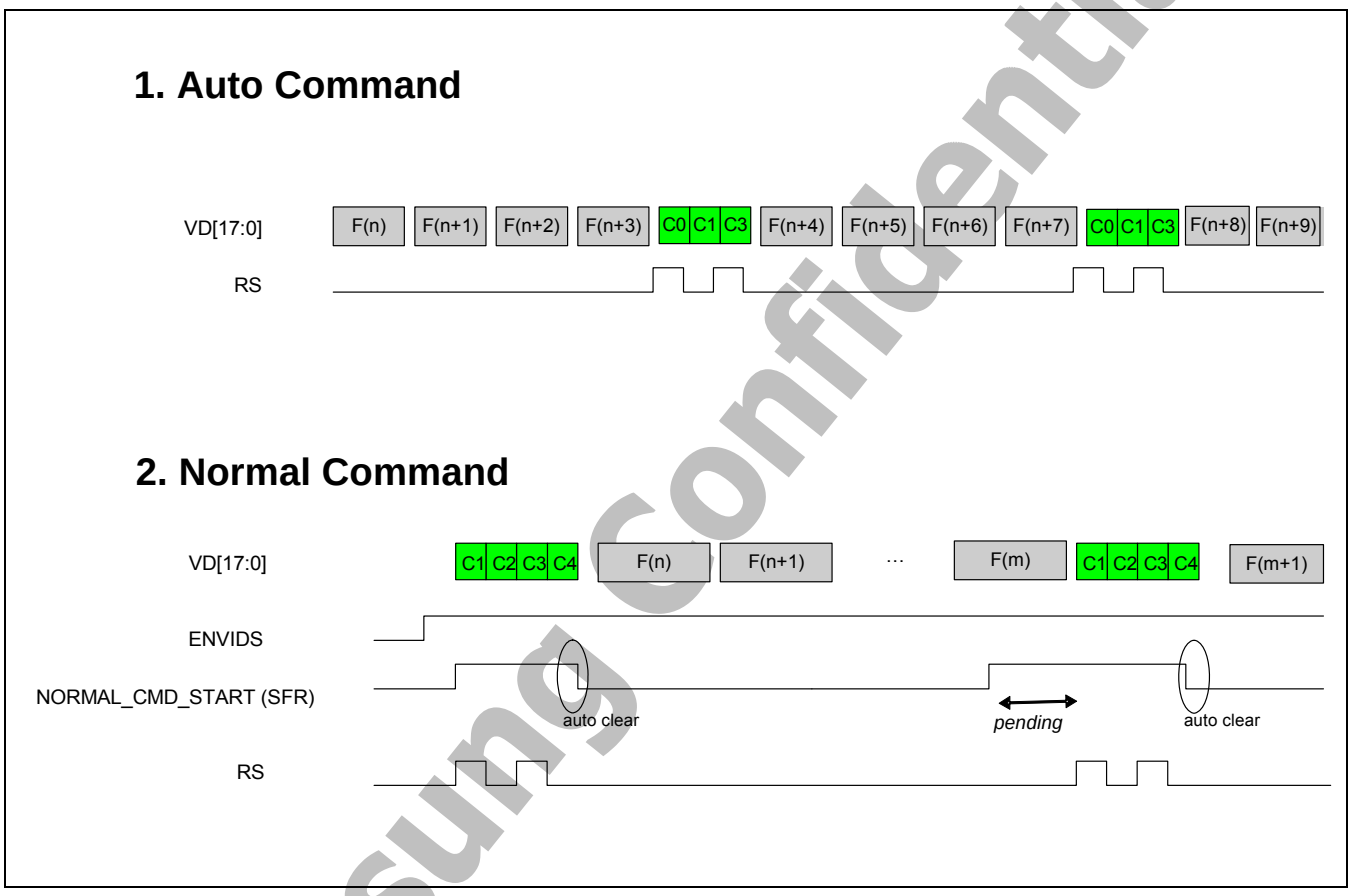

Figure 1-18 Sending Command

1.2.7.2.2 Indirect I80 Interface Trigger

VTIME_I80 starts its operation when a software trigger occurs. There are two kinds of triggers. However, software trigger is generated by setting TRGCON SFR.

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1.3.9.3 Interrupt

Completion of one frame generates Frame Done Interrupt.

1.3.9.3.1 Indirect I80 Interface Output Mode

The following table shows the output mode of Indirect i80 interface based on mode@VIDCON0.

Table 1-6 i80 Output Mode

VIDCON0 Register	Value	BPP	Bus Width	Split	DATA	Command
DSI_EN	1	24	24	X	{ R[7:0],G[7:0],B[7:0] }	CMD [23:0]
L0/1_DATA	000	16	16	X	{ R[7:3],G[7:2],B[7:3] }	CMD [15:0]
	001	18	16	O (1st) (2nd)	{ R[7:2],G[7:2],B[7:4] } { 14'b0,B[3:2] }	CMD [15:0] -
	010	18	9	O (1st) (2nd)	{ R[7:2],G[7:5] } { G[4:2],B[7:2] }	CMD [17:9] CMD [8:0]
	011	24	16	O (1st) (2nd)	{ R[7:0],G[7:0] } { B[7:0], 8'b0 }	- -
	100	18	18	X	{ R[7:2],G[7:2],B[7:2] }	CMD [17:0]
	101	16	8	O (1st) (2nd)	{ R[7:3],G[7:5] } { G[4:2],B[7:3] }	CMD [15:8] CMD [7:0]

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1.3.10 VIRTUAL DISPLAY

The display controller supports hardware horizontal or vertical scrolling. If the screen scrolls, change the fields of LCDBASEU and LCDBASEL (refer to *Figure 1-19*), but not the values of PAGEWIDTH and OFFSIZE. The size of video buffer in which the image is stored should be larger than the LCD panel screen size.

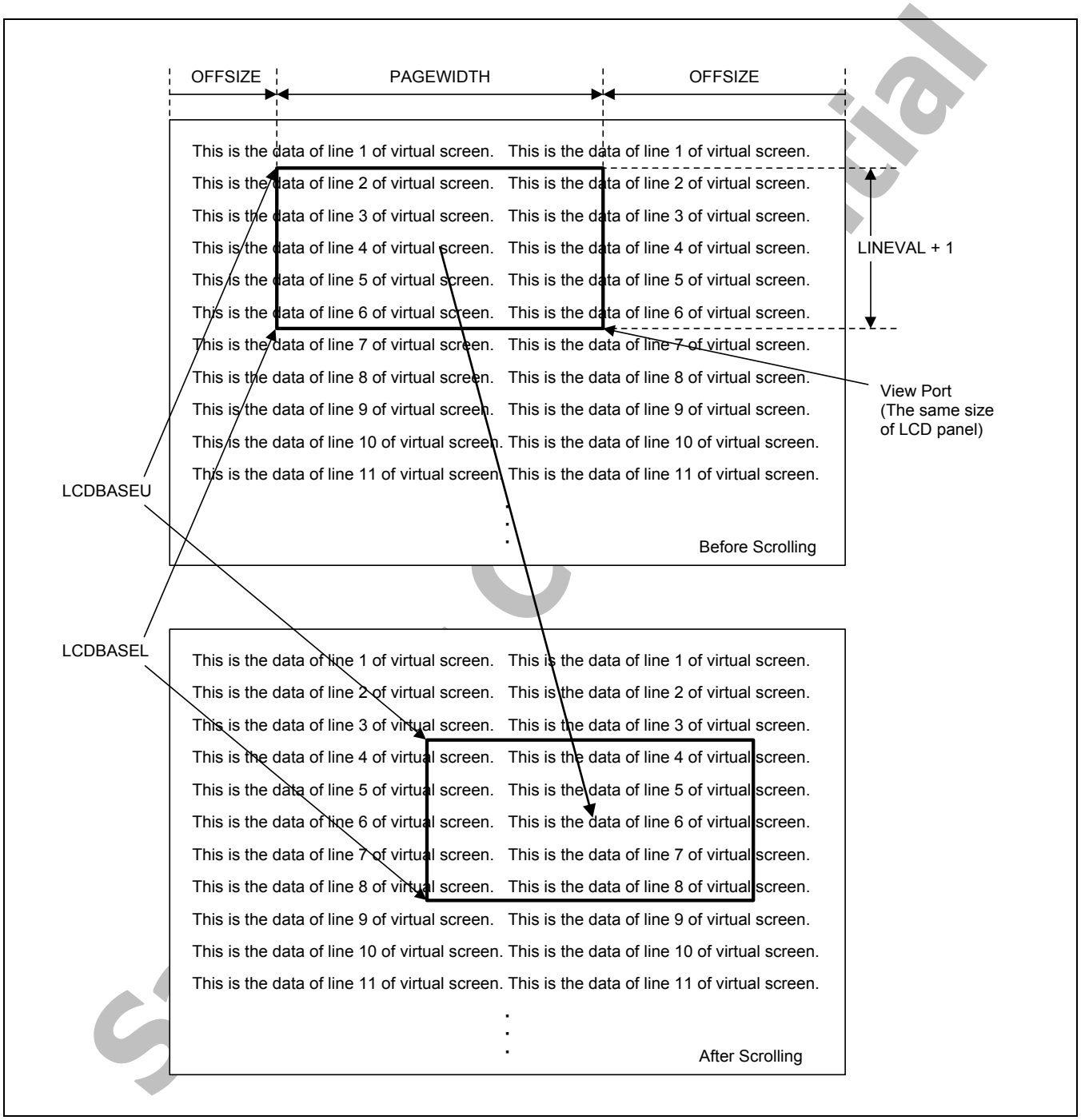

Figure 1-19 Example of Scrolling in Virtual Display

1.3.11 RGB INTERFACE SPEC

1.3.11.1 Signals

Signal	Input/Output	Description	PAD	Type
LCD_HSYNC	Output	Horizontal Sync. Signal	XvHSYNC	Muxed
LCD_VSYNC	Output	Vertical Sync. Signal	XvVSYNC	Muxed
LCD_VCLK	Output	LCD Video Clock	XvVCLK	Muxed
LCD_VDEN	Output	Data Enable	XvVDEN	Muxed
LCD_VD[23:0]	Output	YCbCr data output	XvVD[23:0]	Muxed

NOTE: Type field indicates whether pads are dedicated to signal or pads are connected to multiplexed signals.

1.3.11.2 LCD RGB Interface Timing

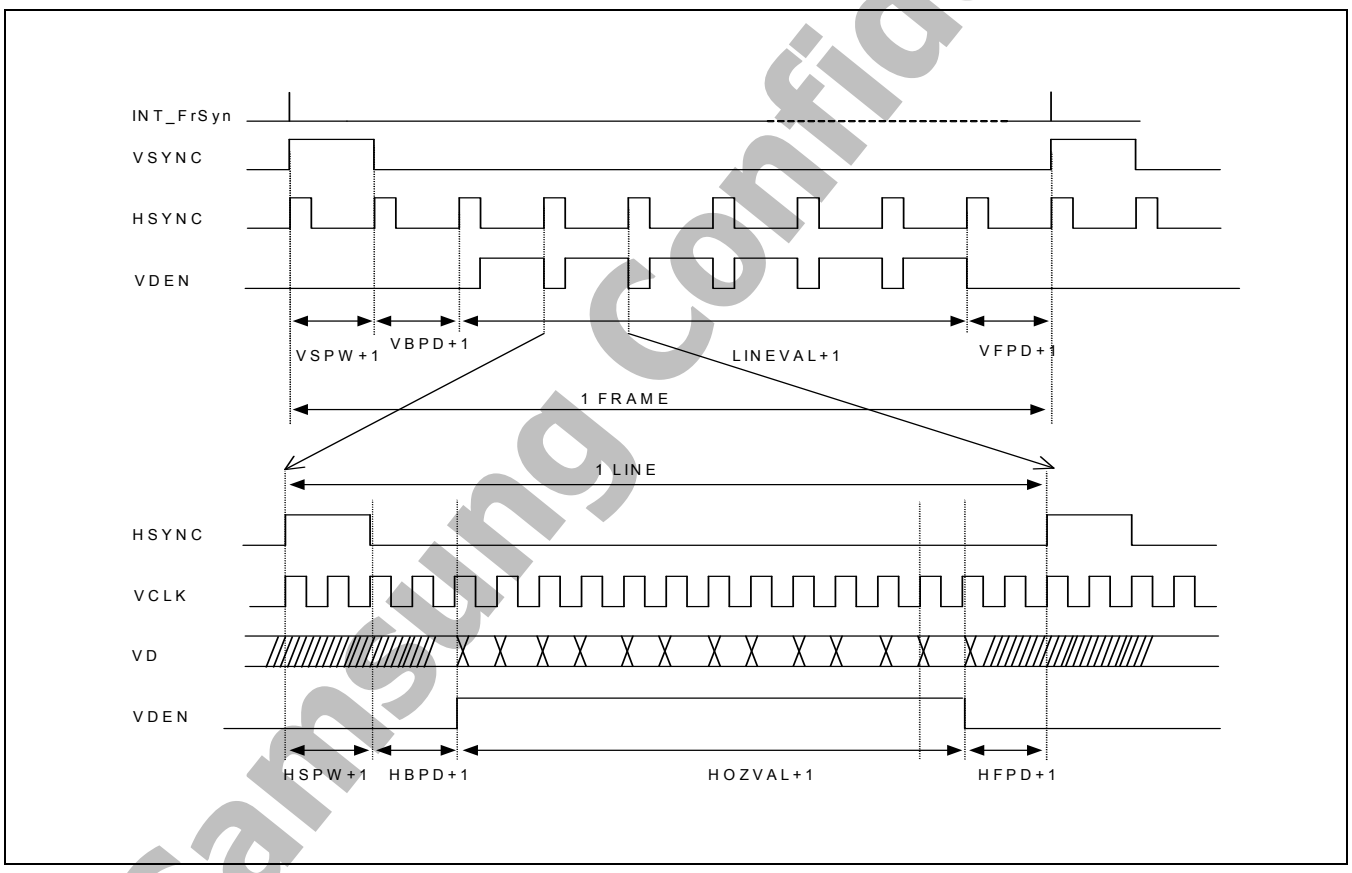

Figure 1-20 LCD RGB Interface Timing

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1.3.11.3 Parallel Output

1.3.11.3.1 General 24-bit Output (RGBSPSEL = 0, RGB_SKIP_EN = 0)

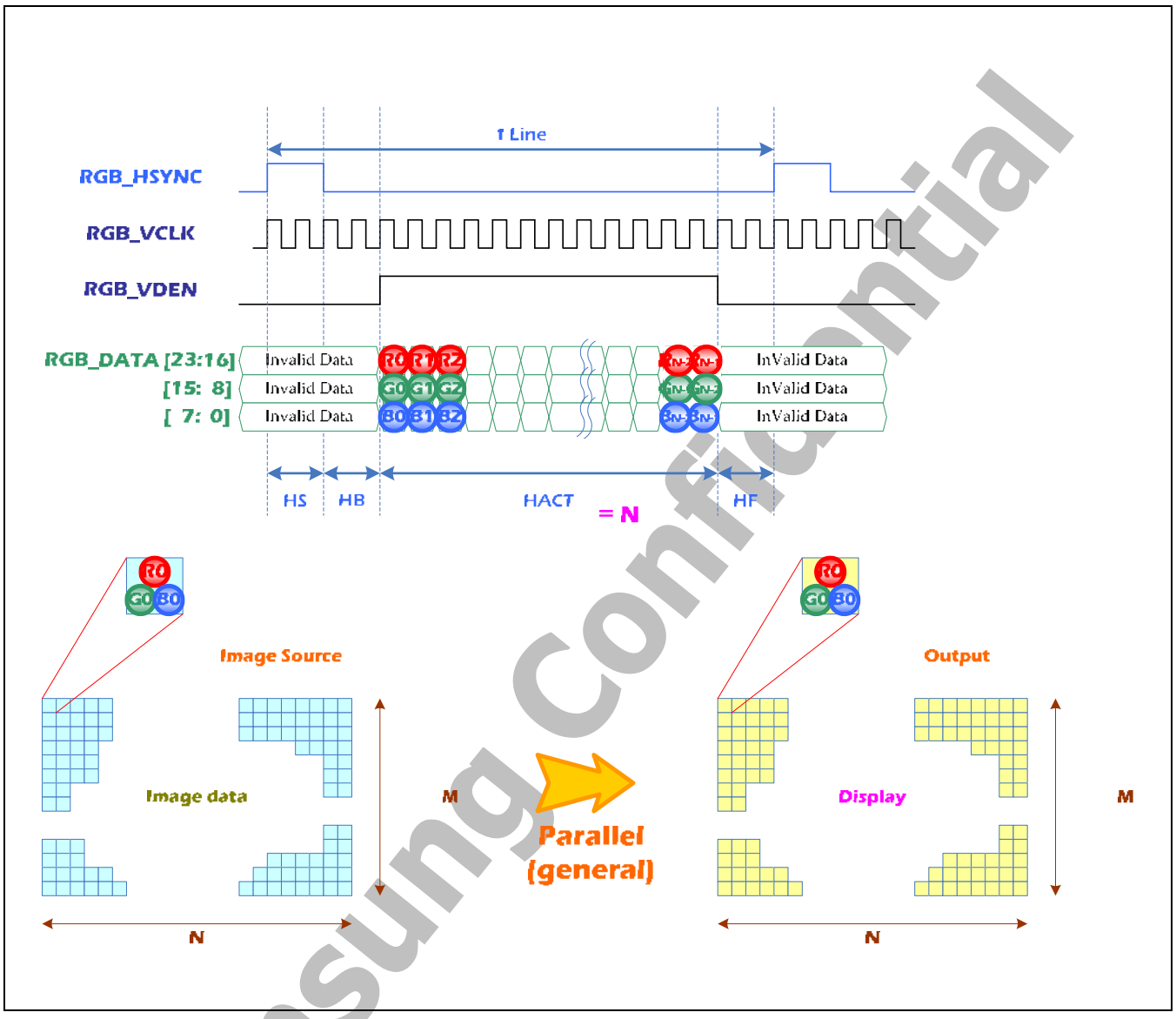

Figure 1-21 LCD RGB Interface Timing (RGB parallel)

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1.3.11.3.2 RGB SKIP 8-bit output (Color sub sampling) (RGBSPSEL = 0, RGB_SKIP_EN = 1)

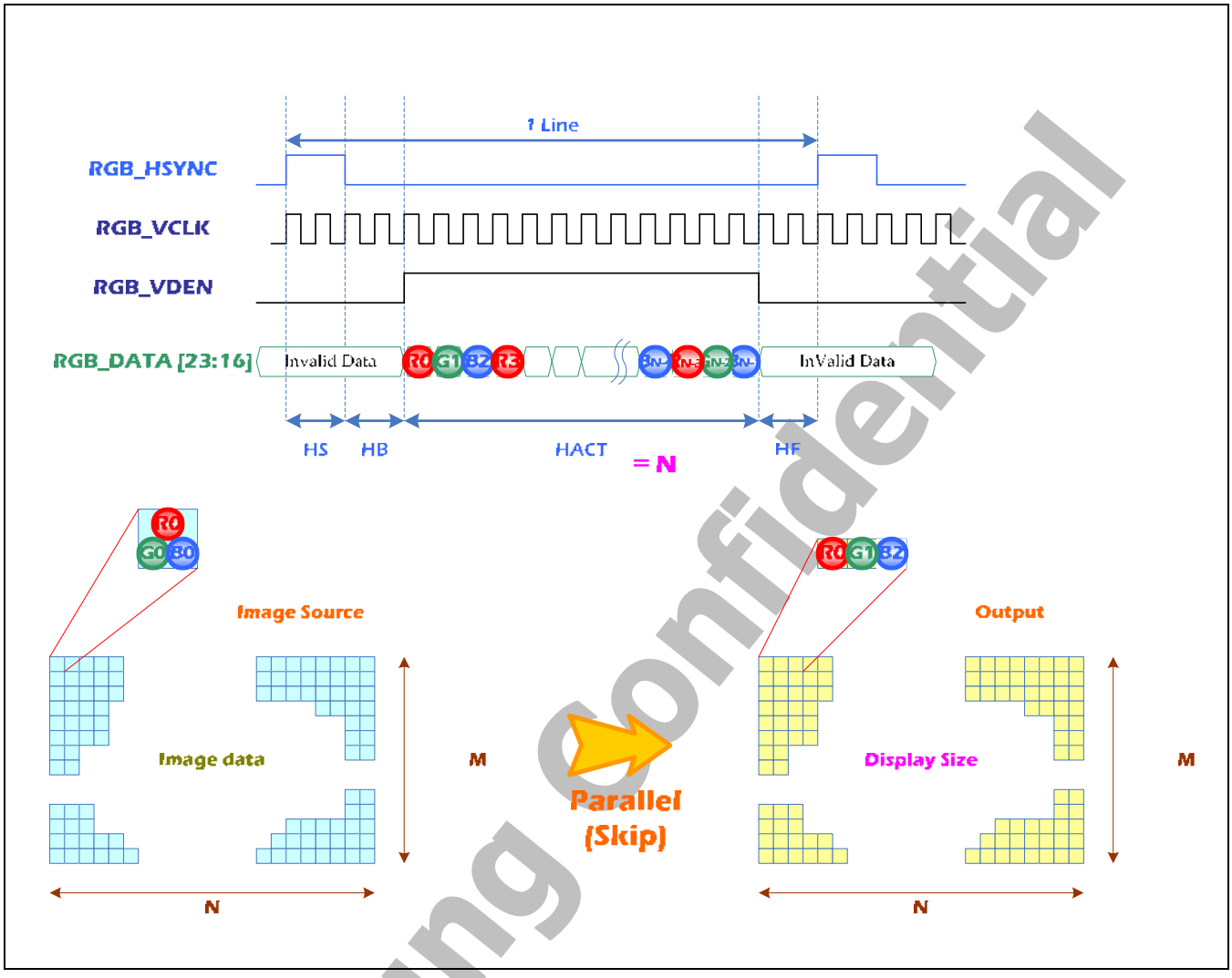

Figure 1-22 LCD RGB Interface Timing (RGB skip)

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1.3.11.4 Serial 8-bit Output

1.3.11.4.1 General 8-bit output (RGBSPSEL = 1, RGB_DUMMY_EN = 0)

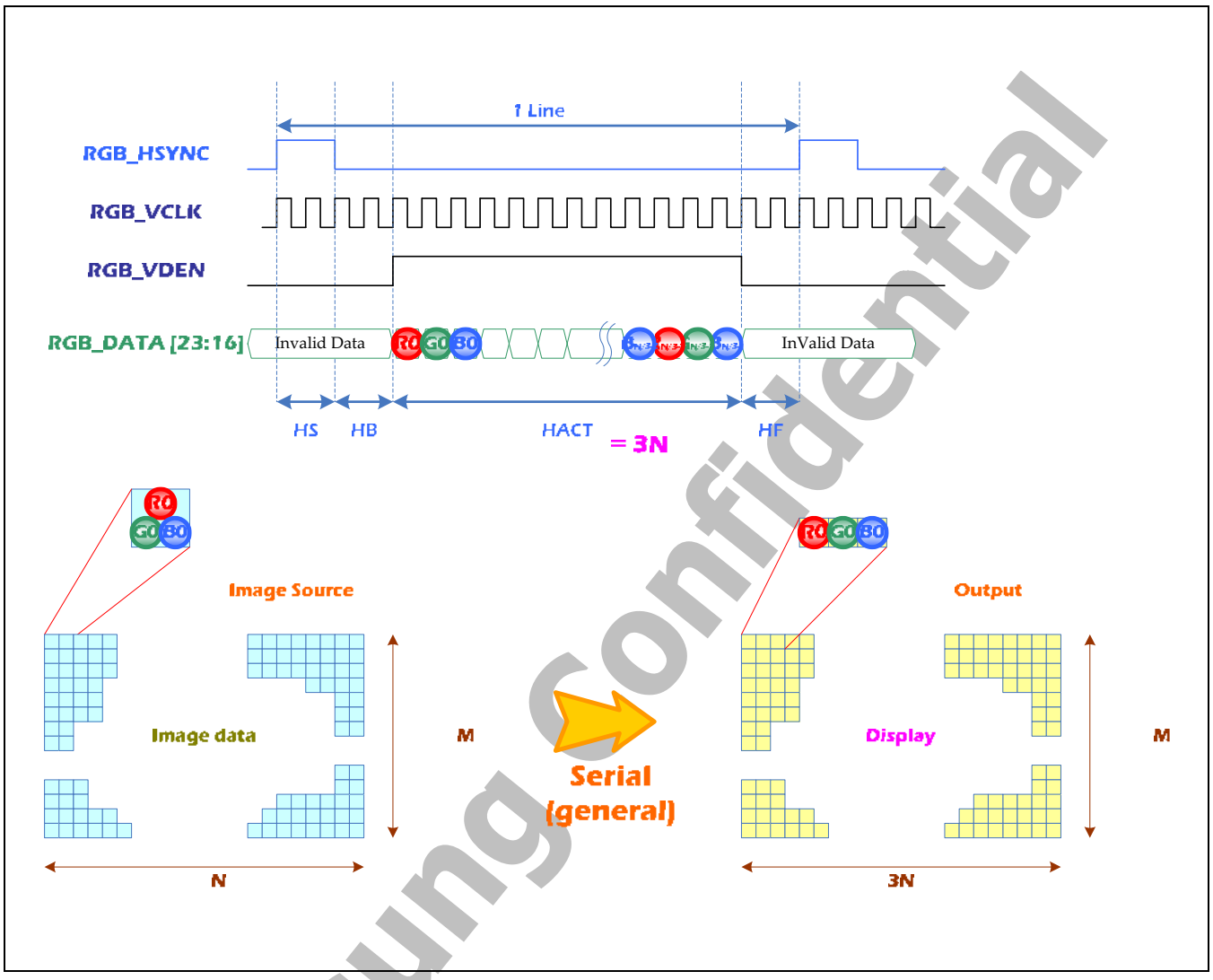

Figure 1-23 LCD RGB Interface Timing (RGB serial, Dummy disable)

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1.3.11.4.2 Dummy Insertion Output (RGBSPSEL = 1, RGB_DUMMY_EN = 1)

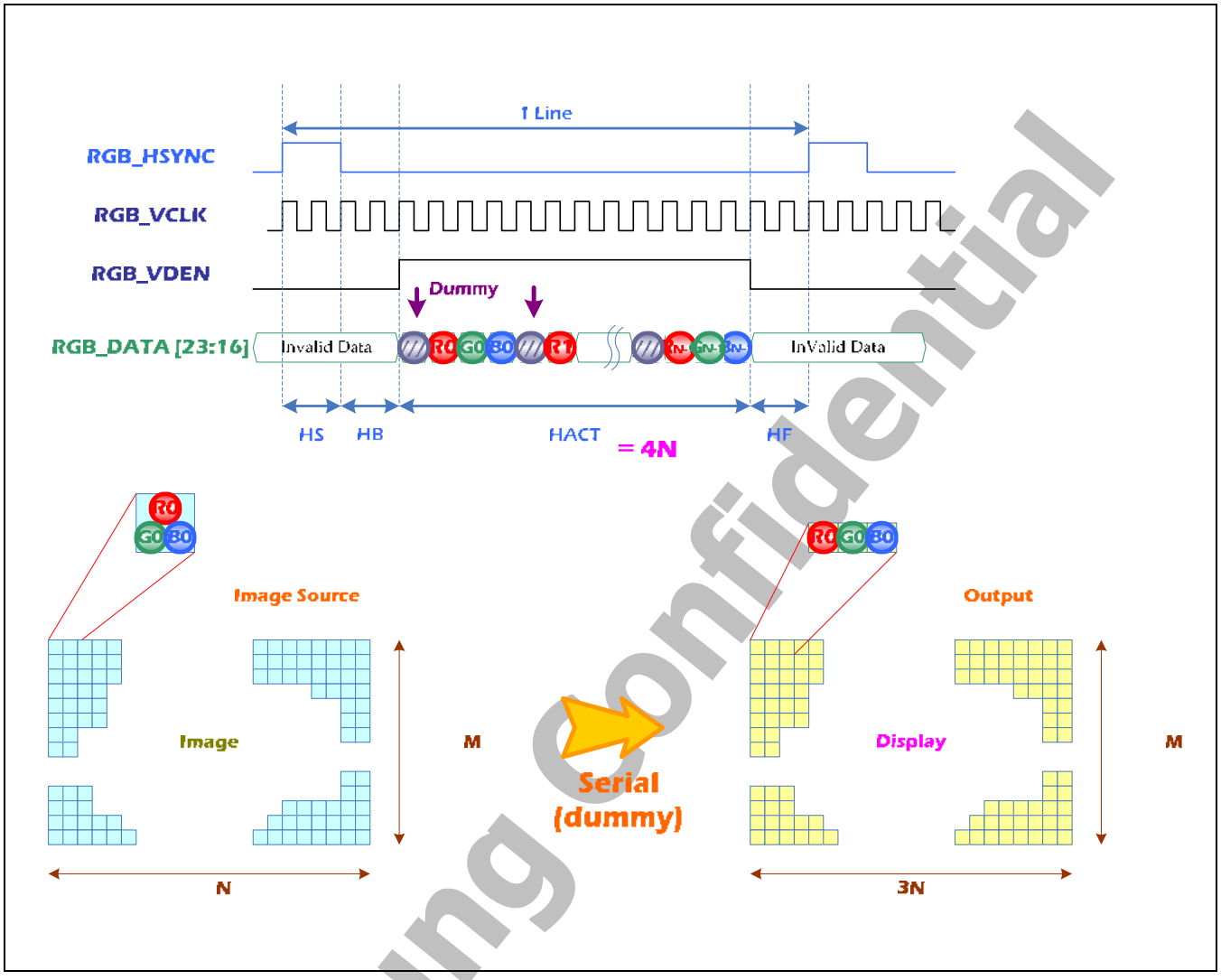

Figure 1-24 LCD RGB Interface Timing (RGB serial, Dummy insertion)

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1.3.11.5 Output Configuration Structure

1.3.11.5.1 Color Order Control

'RGB_ORDER_O' controls odd line color structure. On the other hand, 'RGB_ORDER_E' @VIDCON2 controls even line color structure.

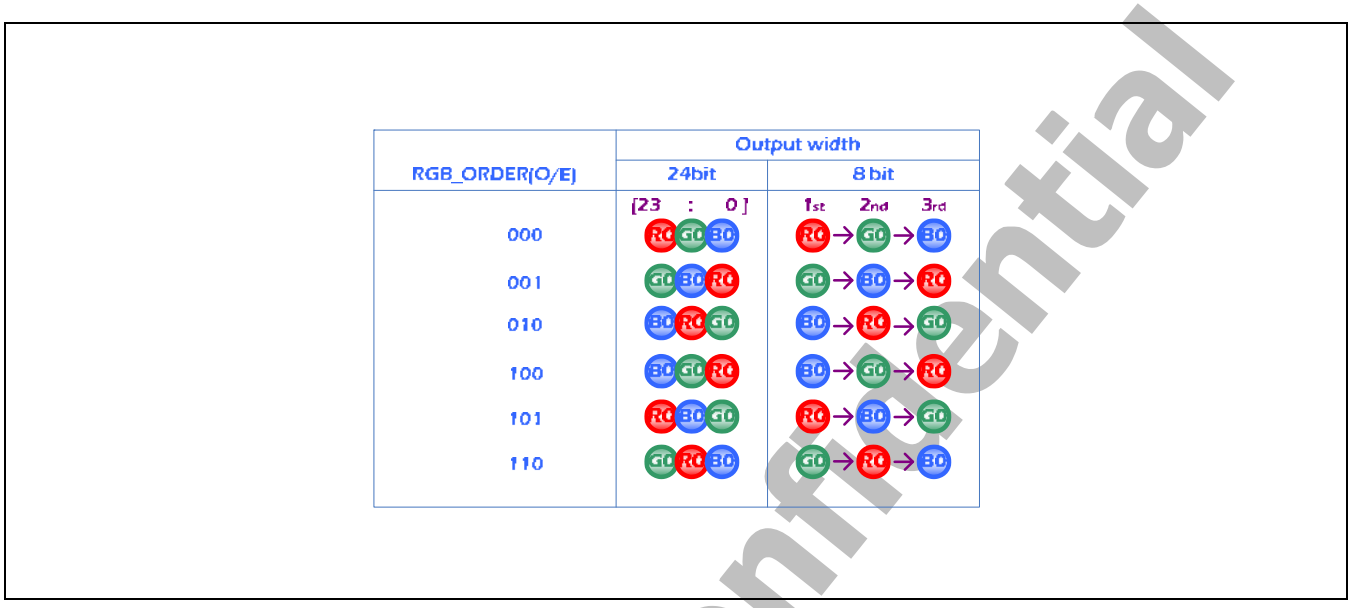

Figure 1-25 LCD RGB Output Order

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1.3.11.5.2 Example of Delta Structure

For more information, refer to register 'RGB_ORDER_O,E'.

Example:

RGB_ORDER_O = 000, RGB_ORDER_E = 001

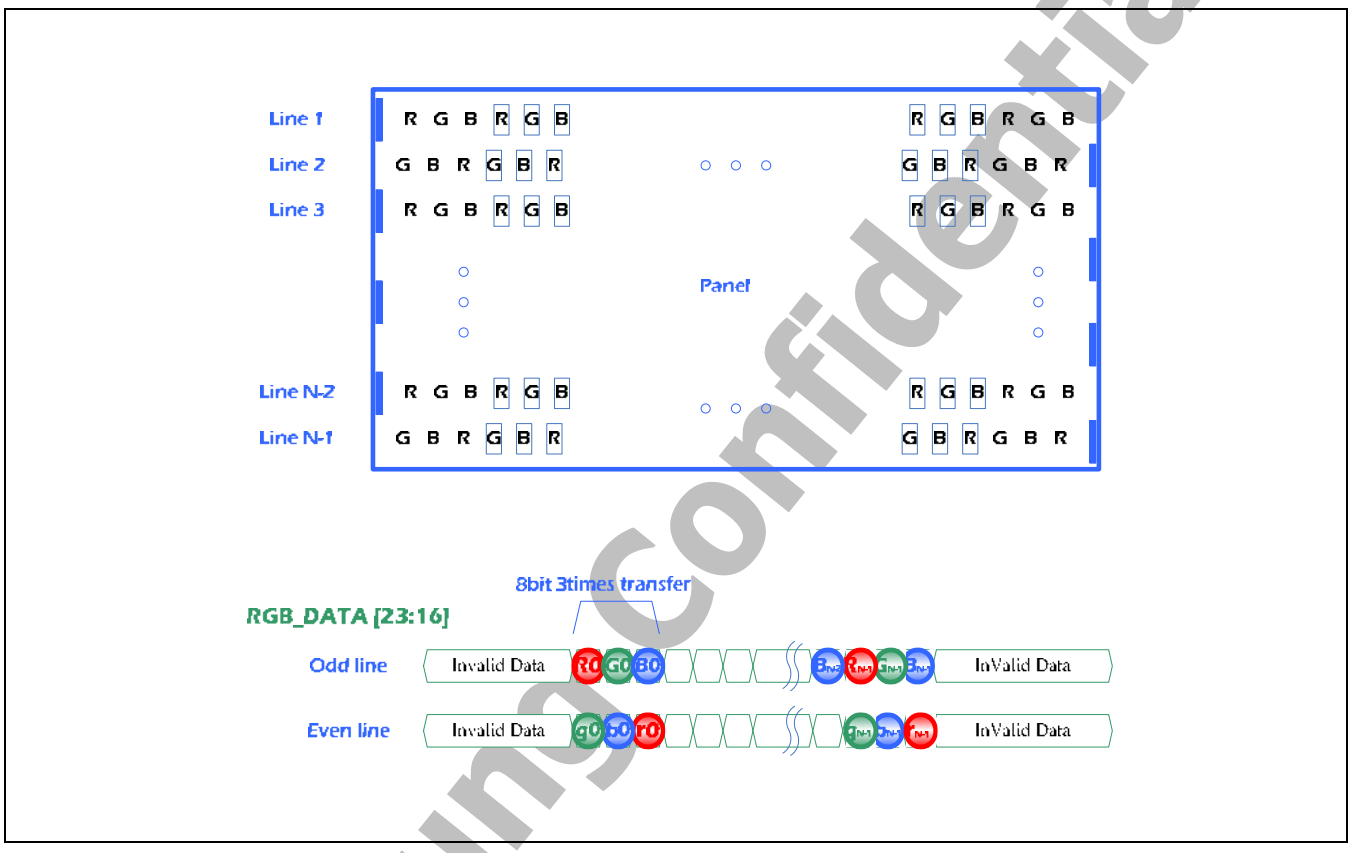

Figure 1-26 Delta Structure and LCD RGB Interface Timing

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1.3.12 LCD INDIRECT I80 SYSTEM INTERFACE

1.3.12.1 Signals

Signal	Input/Output	Description	PAD	Type
SYS_VD[17:0]	Input/Output	Video Data	XvVD[17:0]	Muxed
SYS_CS0	Output	Chip select for LCD0	XvHSYNC	Muxed
SYS_CS1	Output	Chip select for LCD1	XvVSYNC	Muxed
SYS_WE	Output	Write enable	XvVCLK	Muxed
SYS_OE	Output	Output enable	XvVD[23]	Muxed
SYS_RS/SYS_ADD[0]	Output	Address Output SYS_ADD[0] is Register/ State select	XvVDEN	Muxed

NOTE: Type field indicates whether pads are dedicated to the signal, or pads are connected to the multiplexed signals.

* MIPI DSI mode (when VIDCON0 [30] =1)
SYS_ADD [1] = SYS_ST: 0 when VDOUT is from Frame
SYS_ADD [1] = SYS_ST: 1 when VDOUT is from Command

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1.3.12.2 Indirect i80 System Interface WRITE Cycle Timing

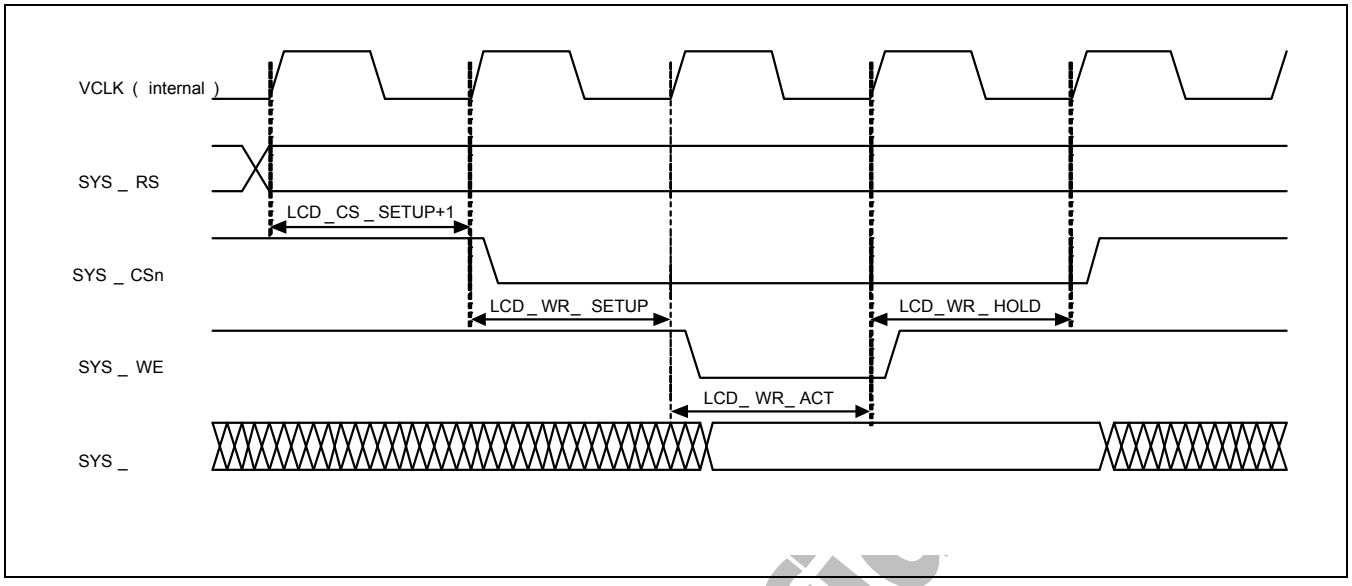

Figure 1-27 Indirect i80 System Interface WRITE Cycle Timing

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Table 1-7 RGB data pin map for RGB I/F

	Parallel RGB			Serial RGB	
	24BPP (888)	18BPP (666)	16BPP (565)	24BPP (888)	18BPP (666)
VD[23]	R[7]	R[5]	R[4]	D[7]	D[5]
VD[22]	R[6]	R[4]	R[3]	D[6]	D[4]
VD[21]	R[5]	R[3]	R[2]	D[5]	D[3]
VD[20]	R[4]	R[2]	R[1]	D[4]	D[2]
VD[19]	R[3]	R[1]	R[0]	D[3]	D[1]
VD[18]	R[2]	R[0]	-	D[2]	D[0]
VD[17]	R[1]	-	-	D[1]	-
VD[16]	R[0]	-	-	D[0]	-
VD[15]	G[7]	G[5]	G[5]	-	-
VD[14]	G[6]	G[4]	G[4]	-	-
VD[13]	G[5]	G[3]	G[3]	-	-
VD[12]	G[4]	G[2]	G[2]	-	-
VD[11]	G[3]	G[1]	G[1]	-	-
VD[10]	G[2]	G[0]	G[0]	-	-
VD[9]	G[1]	-	-	-	-
VD[8]	G[0]	-	-	-	-
VD[7]	B[7]	B[5]	B[4]	-	-
VD[6]	B[6]	B[4]	B[3]	-	-
VD[5]	B[5]	B[3]	B[2]	-	-
VD[4]	B[4]	B[2]	B[1]	-	-
VD[3]	B[3]	B[1]	B[0]	-	-
VD[2]	B[2]	B[0]	-	-	-
VD[1]	B[1]	-	-	-	
VD[0]	B[0]	-	-	-	-

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Table 1-8 RGB data pin map for I80 I/F

	I80 CPU Interface (Parallel)									
	16BPP(565)	**18BPP(666)**		**18BPP(666)**		**24BPP (888)**		**18BPP(666)**	**16BPP(565)**	
Lx_DATA16	000	001		010		011		100	101	
		1st	2nd	1st	2nd	1st	2nd		1st	2nd
VD[23]	-	-	-	-	-	-	-	-	-	-
VD[22]	-	-	-	-	-	-	-	-	-	-
VD[21]	-	-	-	-	-	-	-	-	-	-
VD[20]	-	-	-	-	-	-	-	-	-	-
VD[19]	-	-	-	-	-	-	-	-	-	-
VD[18]	-	-	-	-	-	-	-	-	-	-
VD[17]	-	-	-	-	-	-	-	R[5]	-	-
VD[16]	-	-	-	-	-	-	-	R[4]	-	-
VD[15]	R[4]	R[5]	-	-	-	R[7]	B[7]	R[3]	-	-
VD[14]	R[3]	R[4]	-	-	-	R[6]	B[6]	R[2]	-	-
VD[13]	R[2]	R[3]	-	-	-	R[5]	B[5]	R[1]	-	-
VD[12]	R[1]	R[2]	-	-	-	R[4]	B[4]	R[0]	-	-
VD[11]	R[0]	R[1]	-	-	-	R[3]	B[3]	G[5]	-	-
VD[10]	G[5]	R[0]	-	-	-	R[2]	B[2]	G[4]	-	-
VD[9]	G[4]	G[5]	-	-	-	R[1]	B[1]	G[3]	-	-
VD[8]	G[3]	G[4]	-	R[5]	G[2]	R[0]	B[0]	G[2]	-	-
VD[7]	G[2]	G[3]	-	R[4]	G[1]	G[7]	-	G[1]	R[4]	G[2]
VD[6]	G[1]	G[2]	-	R[3]	G[0]	G[6]	-	G[0]	R[3]	G[1]
VD[5]	G[0]	G[1]	-	R[2]	B[5]	G[5]	-	B[5]	R[2]	G[0]
VD[4]	B[4]	G[0]	-	R[1]	B[4]	G[4]	-	B[4]	R[1]	B[4]
VD[3]	B[3]	B[5]	-	R[0]	B[3]	G[3]	-	B[3]	R[0]	B[3]
VD[2]	B[2]	B[4]	-	G[5]	B[2]	G[2]	-	B[2]	G[5]	B[2]
VD[1]	B[1]	B[3]	B[1]	G[4]	B[1]	G[1]	-	B[1]	G[4]	B[1]
VD[0]	B[0]	B[2]	B[0]	G[3]	B[0]	G[0]	-	B[0]	G[3]	B[0]

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1.4 PROGRAMMER'S MODEL

1.4.1 OVERVIEW OF PROGRAMMER'S MODEL

Use the following registers to configure display controller:

1. VIDCON0: Configures video output format and displays enable/disable.
2. VIDCON1: Specifies RGB I/F control signal.
3. VIDCON2: Specifies output data format control.
4. VIDCON3: Specifies image enhancement control.
5. I80IFCONx: Specifies CPU interface control signal.
6. VIDTCONx: Configures video output timing and determines the size of display.
7. WINCONx: Specifies each window feature setting.
8. VIDOSDxA, VIDOSDxB: Specifies window position setting.
9. VIDOSDxC,D: Specifies OSD size setting.
10. VIDWxALPHA0/1: Specifies alpha value setting.
11. BLENDEQx: Specifies blending equation setting.
12. VIDWxxADDx: Specifies source image address setting.
13. WxKEYCONx: Specifies color key setting register.
14. WxKEYALPHA: Specifies color key alpha value setting.
15. WINxMAP: Specifies window color control.
16. GAMMALUT_xx: Specifies gamma value setting.
17. COLORGAINCON: Specifies color gain value setting.
18. HUExxx: Specifies Hue coefficient and offset value setting.
19. WPALCON: Specifies palette control register.
20. WxRTQOSCON: Specifies RTQoS control register.
21. WxPDATAxx: Specifies Window Palette Data of each Index.
22. SHDOWCON: Specifies Shadow control register.
23. WxRTQOSCON: Specifies QoS control register.

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1.5 REGISTER DESCRIPTION

1.5.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
VIDCON0	0xF800_0000	R/W	Specifies video control 0 register.	0x0000_0000
VIDCON1	0xF800_0004	R/W	Specifies video control 1 register.	0x0000_0000
VIDCON2	0xF800_0008	R/W	Specifies video control 2 register.	0x0000_0000
VIDCON3	0xF800_000C	R/W	Specifies video control 3 register.	0x0000_0000
VIDTCON0	0xF800_0010	R/W	Specifies video time control 0 register.	0x0000_0000
VIDTCON1	0xF800_0014	R/W	Specifies video time control 1 register.	0x0000_0000
VIDTCON2	0xF800_0018	R/W	Specifies video time control 2 register.	0x0000_0000
VIDTCON3	0xF800_001C	R/W	Specifies video time control 3 register.	0x0000_0000
WINCON0	0xF800_0020	R/W	Specifies window control 0 register.	0x0000_0000
WINCON1	0xF800_0024	R/W	Specifies window control 1 register.	0x0000_0000
WINCON2	0xF800_0028	R/W	Specifies window control 2 register.	0x0000_0000
WINCON3	0xF800_002C	R/W	Specifies window control 3 register.	0x0000_0000
WINCON4	0xF800_0030	R/W	Specifies window control 4 register.	0x0000_0000
SHADOWCON	0xF800_0034	R/W	Specifies window shadow control register.	0x0000_0000
VIDOSD0A	0xF800_0040	R/W	Specifies video window 0's position control register.	0x0000_0000
VIDOSD0B	0xF800_0044	R/W	Specifies video window 0's position control register.	0x0000_0000
VIDOSD0C	0xF800_0048	R/W	Specifies video window 0's size control register.	0x0000_0000
VIDOSD1A	0xF800_0050	R/W	Specifies video window 1's position control register.	0x0000_0000
VIDOSD1B	0xF800_0054	R/W	Specifies video window 1's position control register	0x0000_0000
VIDOSD1C	0xF800_0058	R/W	Specifies video window 1's alpha control register.	0x0000_0000
VIDOSD1D	0xF800_005C	R/W	Specifies video window 1's size control register.	0x0000_0000
VIDOSD2A	0xF800_0060	R/W	Specifies video window 2's position control register.	0x0000_0000
VIDOSD2B	0xF800_0064	R/W	Specifies video window 2's position control register.	0x0000_0000
VIDOSD2C	0xF800_0068	R/W	Specifies video window 2's alpha control register.	0x0000_0000
VIDOSD2D	0xF800_006C	R/W	Specifies video window 2's size control register.	0x0000_0000
VIDOSD3A	0xF800_0070	R/W	Specifies video window 3's position control register.	0x0000_0000

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Register	Address	R/W	Description	Reset Value
VIDOSD3B	0xF800_0074	R/W	Specifies video window 3's position control register.	0x0000_0000
VIDOSD3C	0xF800_0078	R/W	Specifies video window 3's alpha control register.	0x0000_0000
VIDOSD4A	0xF800_0080	R/W	Specifies video window 4's position control register.	0x0000_0000
VIDOSD4B	0xF800_0084	R/W	Specifies video window 4's position control register.	0x0000_0000
VIDOSD4C	0xF800_0088	R/W	Specifies video window 4's alpha control register.	0x0000_0000
VIDW00ADD0B0	0xF800_00A0	R/W	Specifies window 0's buffer start address register, buffer 0.	0x0000_0000
VIDW00ADD0B1	0xF800_00A4	R/W	Specifies window 0's buffer start address register, buffer 1.	0x0000_0000
VIDW00ADD0B2	0xF800_20A0	R/W	Specifies window 0's buffer start address register, buffer 2.	0x0000_0000
VIDW01ADD0B0	0xF800_00A8	R/W	Specifies window 1's buffer start address register, buffer 0.	0x0000_0000
VIDW01ADD0B1	0xF800_00AC	R/W	Specifies Window 1's buffer start address register, buffer 1.	0x0000_0000
VIDW01ADD0B2	0xF800_20A8	R/W	Specifies Window 1's buffer start address register, buffer 2.	0x0000_0000
VIDW02ADD0B0	0xF800_00B0	R/W	Specifies Window 2's buffer start address register, buffer 0.	0x0000_0000
VIDW02ADD0B1	0xF800_00B4	R/W	Specifies Window 2's buffer start address register, buffer 1.	0x0000_0000
VIDW02ADD0B2	0xF800_20B0	R/W	Specifies window 2's buffer start address register, buffer 2.	0x0000_0000
VIDW03ADD0B0	0xF800_00B8	R/W	Specifies window 3's buffer start address register, buffer 0.	0x0000_0000
VIDW03ADD0B1	0xF800_00BC	R/W	Specifies window 3's buffer start address register, buffer 1.	0x0000_0000
VIDW03ADD0B2	0xF800_20B8	R/W	Specifies window 3's buffer start address register, buffer 2.	0x0000_0000
VIDW04ADD0B0	0xF800_00C0	R/W	Specifies window 4's buffer start address register, buffer 0.	0x0000_0000
VIDW04ADD0B1	0xF800_00C4	R/W	Specifies window 4's buffer start address register, buffer 1.	0x0000_0000
VIDW04ADD0B2	0xF800_20C0	R/W	Specifies window 4's buffer start address register, buffer 2.	0x0000_0000
VIDW00ADD1B0	0xF800_00D0	R/W	Specifies window 0's buffer end address register, buffer 0.	0x0000_0000

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Register	Address	R/W	Description	Reset Value
VIDW00ADD1B1	0xF800_00D4	R/W	Specifies window 0's buffer end address register, buffer 1.	0x0000_0000
VIDW00ADD1B2	0xF800_20D0	R/W	Specifies window 0's buffer end address register, buffer 2.	0x0000_0000
VIDW01ADD1B0	0xF800_00D8	R/W	Specifies window 1's buffer end address register, buffer 0.	0x0000_0000
VIDW01ADD1B1	0xF800_00DC	R/W	Specifies window 1's buffer end address register, buffer 1.	0x0000_0000
VIDW01ADD1B2	0xF800_20D8	R/W	Specifies window 1's buffer end address register, buffer 2.	0x0000_0000
VIDW02ADD1B0	0xF800_00E0	R/W	Specifies window 2's buffer end address register, buffer 0.	0x0000_0000
VIDW02ADD1B1	0xF800_00E4	R/W	Specifies window 2's buffer end address register, buffer 1.	0x0000_0000
VIDW02ADD1B2	0xF800_20E0	R/W	Specifies window 2's buffer end address register, buffer 2.	0x0000_0000
VIDW03ADD1B0	0xF800_00E8	R/W	Specifies window 3's buffer end address register, buffer 0.	0x0000_0000
VIDW03ADD1B1	0xF800_00EC	R/W	Specifies window 3's buffer end address register, buffer 1.	0x0000_0000
VIDW03ADD1B2	0xF800_20E8	R/W	Specifies window 3's buffer end address register, buffer 2.	0x0000_0000
VIDW04ADD1B0	0xF800_00F0	R/W	Specifies window 4's buffer end address register, buffer 0.	0x0000_0000
VIDW04ADD1B1	0xF800_00F4	R/W	Specifies window 4's buffer end address register, buffer 1.	0x0000_0000
VIDW04ADD1B2	0xF800_20F0	R/W	Specifies window 4's buffer end address register, buffer 2.	0x0000_0000
VIDW00ADD2	0xF800_0100	R/W	Specifies window 0's buffer size register.	0x0000_0000
VIDW01ADD2	0xF800_0104	R/W	Specifies window 1's buffer size register.	0x0000_0000
VIDW02ADD2	0xF800_0108	R/W	Specifies window 2's buffer size register.	0x0000_0000
VIDW03ADD2	0xF800_010C	R/W	Specifies window 3's buffer size register.	0x0000_0000
VIDW04ADD2	0xF800_0110	R/W	Specifies window 4's buffer size register.	0x0000_0000
VIDINTCON0	0xF800_0130	R/W	Specifies video interrupt control register.	0x0000_0000
VIDINTCON1	0xF800_0134	R/W	Specifies video interrupt pending register.	0x0000_0000
W1KEYCON0	0xF800_0140	R/W	Specifies color key control register.	0x0000_0000
W1KEYCON1	0xF800_0144	R/W	Specifies color key value (transparent value) register.	0x0000_0000
W2KEYCON0	0xF800_0148	R/W	Specifies color key control register.	0x0000_0000
W2KEYCON1	0xF800_014C	R/W	Specifies color key value (transparent value) register.	0x0000_0000

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Register	Address	R/W	Description	Reset Value
W3KEYCON0	0xF800_0150	R/W	Specifies color key control register.	0x0000_0000
W3KEYCON1	0xF800_0154	R/W	Specifies color key value (transparent value) register.	0x0000_0000
W4KEYCON0	0xF800_0158	R/W	Specifies color key control register.	0x0000_0000
W4KEYCON1	0xF800_015C	R/W	Specifies color key value (transparent value) register.	0x0000_0000
W1KEYALPHA	0xF800_0160	R/W	Specifies color key alpha value register.	0x0000_0000
W2KEYALPHA	0xF800_0164	R/W	Specifies color key alpha value register.	0x0000_0000
W3KEYALPHA	0xF800_0168	R/W	Specifies color key alpha value register.	0x0000_0000
W4KEYALPHA	0xF800_016C	R/W	Specifies color key alpha value register.	0x0000_0000
DITHMODE	0xF800_0170	R/W	Specifies dithering mode register.	0x0000_0000
WIN0MAP	0xF800_0180	R/W	Specifies window 0's color control.	0x0000_0000
WIN1MAP	0xF800_0184	R/W	Specifies window 1's color control.	0x0000_0000
WIN2MAP	0xF800_0188	R/W	Specifies window 2's color control.	0x0000_0000
WIN3MAP	0xF800_018C	R/W	Specifies window 3's color control.	0x0000_0000
WIN4MAP	0xF800_0190	R/W	Specifies window 4's color control.	0x0000_0000
WPALCON_H	0xF800_019c	R/W	Specifies window palette control register.	0x0000_0000
WPALCON_L	0xF800_01A0	R/W	Specifies window palette control register.	0x0000_0000
TRIGCON	0xF800_01A4	R/W	Specifies i80/ RGB trigger control register.	0x0000_0000
I80IFCONA0	0xF800_01B0	R/W	Specifies i80 interface control 0 for main LDI.	0x0000_0000
I80IFCONA1	0xF800_01B4	R/W	Specifies i80 interface control 0 for sub LDI.	0x0000_0000
I80IFCONB0	0xF800_01B8	R/W	Specifies i80 interface control 1 for main LDI.	0x0000_0000
I80IFCONB1	0xF800_01BC	R/W	Specifies i80 interface control 1 for sub LDI.	0x0000_0000
COLORGAINCON	0xF800_01C0	R/W	Specifies color gain control register.	0x1004_0100
LDI_CMDCON0	0xF800_01D0	R/W	Specifies i80 interface LDI command control 0.	0x0000_0000
LDI_CMDCON1	0xF800_01D4	R/W	Specifies i80 interface LDI command control 1.	0x0000_0000
SIFCCON0	0xF800_01E0	R/W	Specifies LCD i80 system interface command control 0.	0x0000_0000
SIFCCON1	0xF800_01E4	R/W	Specifies LCD i80 system interface command control 1.	0x0000_0000
SIFCCON2	0xF800_01E8	R	Specifies LCD i80 system interface command control 2.	0x????_????
HUECOEF00	0xF800_01EC	R/W	Specifies Hue coefficient control register.	0x0100_0100
HUECOEF01	0xF800_01F0	R/W	Specifies Hue coefficient control register.	0x0000_0000

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Register	Address	R/W	Description	Reset Value
HUECOEF10	0xF800_01F4	R/W	Specifies Hue coefficient control register.	0x0000_0000
HUECOEF11	0xF800_01F8	R/W	Specifies Hue coefficient control register.	0x0100_0100
HUEOFFSET	0xF800_01FC	R/W	Specifies Hue offset control register.	0x0180_0080
VIDW0ALPHA0	0xF800_0200	R/W	Specifies window 0's alpha value 0 register.	0x0000_0000
VIDW0ALPHA1	0xF800_0204	R/W	Specifies window 0's alpha value 1 register.	0x0000_0000
VIDW1ALPHA0	0xF800_0208	R/W	Specifies window 1's alpha value 0 register.	0x0000_0000
VIDW1ALPHA1	0xF800_020c	R/W	Specifies window 1's alpha value 1 register.	0x0000_0000
VIDW2ALPHA0	0xF800_0210	R/W	Specifies window 2's alpha value 0 register.	0x0000_0000
VIDW2ALPHA1	0xF800_0214	R/W	Specifies window 2's alpha value 1 register.	0x0000_0000
VIDW3ALPHA0	0xF800_0218	R/W	Specifies window 3's alpha value 0 register.	0x0000_0000
VIDW3ALPHA1	0xF800_021c	R/W	Specifies window 3's alpha value 1 register.	0x0000_0000
VIDW4ALPHA0	0xF800_0220	R/W	Specifies window 4's alpha value 0 register.	0x0000_0000
VIDW4ALPHA1	0xF800_0224	R/W	Specifies window 4's alpha value 1 register.	0x0000_0000
BLENDEQ1	0xF800_0244	R/W	Specifies window 1's blending equation control register.	0x0000_00c2
BLENDEQ2	0xF800_0248	R/W	Specifies window 2's blending equation control register.	0x0000_00c2
BLENDEQ3	0xF800_024c	R/W	Specifies window 3's blending equation control register.	0x0000_00c2
BLENDEQ4	0xF800_0250	R/W	Specifies window 4's blending equation control register.	0x0000_00c2
BLENDCON	0xF800_0260	R/W	Specifies blending control register.	0x0000_0000
W0RTQOSCON	0xF800_0264	R/W	Specifies window 0's RTQOS control register.	0x0000_0000
W1RTQOSCON	0xF800_0268	R/W	Specifies window 1's RTQOS control register.	0x0000_0000
W2RTQOSCON	0xF800_026C	R/W	Specifies window 2's RTQOS control register.	0x0000_0000
W3RTQOSCON	0xF800_0270	R/W	Specifies window 3's RTQOS control register.	0x0000_0000
W4RTQOSCON	0xF800_0274	R/W	Specifies window 4's RTQOS control register.	0x0000_0000
LDI_CMD0	0xF800_0280	R/W	Specifies i80 interface LDI command 0.	0x0000_0000
LDI_CMD1	0xF800_0284	R/W	Specifies i80 interface LDI command 1.	0x0000_0000
LDI_CMD2	0xF800_0288	R/W	Specifies i80 interface LDI command 2.	0x0000_0000
LDI_CMD3	0xF800_028C	R/W	Specifies i80 interface LDI command 3.	0x0000_0000
LDI_CMD4	0xF800_0290	R/W	Specifies i80 interface LDI command 4.	0x0000_0000
LDI_CMD5	0xF800_0294	R/W	Specifies i80 interface LDI command 5.	0x0000_0000

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Register	Address	R/W	Description	Reset Value
LDI_CMD6	0xF800_0298	R/W	Specifies i80 interface LDI command 6.	0x0000_0000
LDI_CMD7	0xF800_029C	R/W	Specifies i80 interface LDI command 7.	0x0000_0000
LDI_CMD8	0xF800_02A0	R/W	Specifies i80 interface LDI command 8.	0x0000_0000
LDI_CMD9	0xF800_02A4	R/W	Specifies i80 interface LDI command 9.	0x0000_0000
LDI_CMD10	0xF800_02A8	R/W	Specifies i80 interface LDI command 10.	0x0000_0000
LDI_CMD11	0xF800_02AC	R/W	Specifies i80 interface LDI command 11.	0x0000_0000
GAMMALUT_01_00	0xF800_037C	R/W	Specifies Gamma LUT data of the index 0, 1.	0x0010_0000
GAMMALUT_03_02	0xF800_0380	R/W	Specifies Gamma LUT data of the index 2, 3.	0x0030_0020
GAMMALUT_05_04	0xF800_0384	R/W	Specifies Gamma LUT data of the index 4, 5.	0x0050_0040
GAMMALUT_07_06	0xF800_0388	R/W	Specifies Gamma LUT data of the index 6, 7.	0x0070_0060
GAMMALUT_09_08	0xF800_038c	R/W	Specifies Gamma LUT data of the index 8, 9.	0x0090_0080
GAMMALUT_11_10	0xF800_0390	R/W	Specifies Gamma LUT data of the index 10, 11.	0x00b0_00a0
GAMMALUT_13_12	0xF800_0394	R/W	Specifies Gamma LUT data of the index 12, 13.	0x00d0_00c0
GAMMALUT_15_14	0xF800_0398	R/W	Specifies Gamma LUT data of the index 14, 15.	0x00f0_00e0
GAMMALUT_17_16	0xF800_039C	R/W	Specifies Gamma LUT data of the index 16, 17.	0x0110_0100
GAMMALUT_19_18	0xF800_03a0	R/W	Specifies Gamma LUT data of the index 18, 19.	0x0130_0120
GAMMALUT_21_20	0xF800_03a4	R/W	Specifies Gamma LUT data of the index 20, 21.	0x0150_0140
GAMMALUT_23_22	0xF800_03a8	R/W	Specifies Gamma LUT data of the index 22, 23.	0x0170_0160
GAMMALUT_25_24	0xF800_03ac	R/W	Specifies Gamma LUT data of the index 24, 25.	0x0190_0180
GAMMALUT_27_26	0xF800_03b0	R/W	Specifies Gamma LUT data of the index 26, 27.	0x01b0_01a0
GAMMALUT_29_28	0xF800_03b4	R/W	Specifies Gamma LUT data of the index 28, 29.	0x01d0_01c0
GAMMALUT_31_30	0xF800_03b8	R/W	Specifies Gamma LUT data of the index 30, 31.	0x01f0_01e0
GAMMALUT_33_32	0xF800_03bc	R/W	Specifies Gamma LUT data of the index 32, 33.	0x0210_0200

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Register	Address	R/W	Description	Reset Value
GAMMALUT_35_34	0xF800_03c0	R/W	Specifies Gamma LUT data of the index 34, 35.	0x0230_0220
GAMMALUT_37_36	0xF800_03c4	R/W	Specifies Gamma LUT data of the index 36, 37.	0x0250_0240
GAMMALUT_39_38	0xF800_03c8	R/W	Specifies Gamma LUT data of the index 38, 39.	0x0270_0260
GAMMALUT_41_40	0xF800_03cc	R/W	Specifies Gamma LUT data of the index 40, 41.	0x0290_0280
GAMMALUT_43_42	0xF800_03d0	R/W	Specifies Gamma LUT data of the index 42, 43.	0x02b0_02a0
GAMMALUT_45_44	0xF800_03d4	R/W	Specifies Gamma LUT data of the index 44, 45.	0x02d0_02c0
GAMMALUT_47_46	0xF800_03d8	R/W	Specifies Gamma LUT data of the index 46, 47.	0x02f0_02e0
GAMMALUT_49_48	0xF800_03dc	R/W	Specifies Gamma LUT data of the index 48, 49.	0x0310_0300
GAMMALUT_51_50	0xF800_03e0	R/W	Specifies Gamma LUT data of the index 50, 51.	0x0330_0320
GAMMALUT_53_52	0xF800_03e4	R/W	Specifies Gamma LUT data of the index 52, 53.	0x0350_0340
GAMMALUT_55_54	0xF800_03e8	R/W	Specifies Gamma LUT data of the index 54, 55.	0x0370_0360
GAMMALUT_57_56	0xF800_03ec	R/W	Specifies Gamma LUT data of the index 56, 57.	0x0390_0380
GAMMALUT_59_58	0xF800_03f0	R/W	Specifies Gamma LUT data of the index 58, 59.	0x03b0_03a0
GAMMALUT_61_60	0xF800_03f4	R/W	Specifies Gamma LUT data of the index 60, 61.	0x03d0_03c0
GAMMALUT_63_62	0xF800_03f8	R/W	Specifies Gamma LUT data of the index 62, 63.	0x03f0_03e0
GAMMALUT_xx_64	0xF800_03fc	R/W	Specifies Gamma LUT data of the index 64.	0x0000_0400
SHD_VIDW00ADD0	0xF800_40A0	R	Specifies window 0's buffer start address register (shadow).	0x0000_0000
SHD_VIDW01ADD0	0xF800_40A8	R	Specifies window 1's buffer start address register (shadow).	0x0000_0000
SHD_VIDW02ADD0	0xF800_40B0	R	Specifies window 2's buffer start address register (shadow).	0x0000_0000
SHD_VIDW03ADD0	0xF800_40B8	R	Specifies window 3's buffer start address register (shadow).	0x0000_0000
SHD_VIDW04ADD0	0xF800_40C0	R	Specifies window 4's buffer start address register (shadow).	0x0000_0000

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Register	Address	R/W	Description	Reset Value
SHD_VIDW00ADD1	0xF800_40D0	R	Specifies window 0's buffer end address register (shadow)	0x0000_0000
SHD_VIDW01ADD1	0xF800_40D8	R	Specifies window 1's buffer end address register (shadow)	0x0000_0000
SHD_VIDW02ADD1	0xF800_40E0	R	Specifies window 2's buffer end address register (shadow).	0x0000_0000
SHD_VIDW03ADD1	0xF800_40E8	R	Specifies window 3's buffer end address register (shadow).	0x0000_0000
SHD_VIDW04ADD1	0xF800_40F0	R	Specifies window 4's buffer end address register (shadow).	0x0000_0000
SHD_VIDW00ADD2	0xF800_4100	R	Specifies window 0's buffer size register (shadow).	0x0000_0000
SHD_VIDW01ADD2	0xF800_4104	R	Specifies window 1's buffer size register (shadow).	0x0000_0000
SHD_VIDW02ADD2	0xF800_4108	R	Specifies window 2's buffer size register (shadow).	0x0000_0000
SHD_VIDW03ADD2	0xF800_410C	R	Specifies window 3's buffer size register (shadow).	0x0000_0000
SHD_VIDW04ADD2	0xF800_4110	R	Specifies window 4's buffer size register (shadow).	0x0000_0000

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1.5.2 PALETTE MEMORY (PALRAM)

	Start Address	End Address	R/W	Description	Reset Value
Win0 PalRam	0xF800_2400 (0xF800_0400)	0xF800_27FC (0xF800_07FC)	R/W	Specifies 0~255 entry palette data.	Undefined
Win1 PalRam	0xF800_2800 (0xF800_0800)	0xF800_2BFC (0xF800_0BFC)	R/W	Specifies 0~255 entry palette data.	Undefined
Win2 PalRam	0xF800_2C00	0xF800_2FFC	R/W	Specifies 0~255 entry palette data.	Undefined
Win3 PalRam	0xF800_3000	0xF800_33FC	R/W	Specifies 0~255 entry palette data.	Undefined
Win4 PalRam	0xF800_3400	0xF800_37FC	R/W	Specifies 0~255 entry palette data.	Undefined

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1.5.2.1 Video Main Control 0 Register (VIDCON0, R/W, Address = 0xF800_0000)

VIDCON0	Bit	Description	Initial State
Reserved	[31]	Reserved (should be 0).	0
DSI_EN	[30]	Enables MIPI DSI. 0 = Disables 1 = Enables (i80 24bit data interface, SYS_ADD[1])	0
Reserved	[29]	Reserved (should be 0)	0
VIDOUT	[28:26]	Determines the output format of Video Controller. 000 = RGB interface 001 = Reserved 010 = Indirect I80 interface for LDI0 011 = Indirect I80 interface for LDI1 100 = WB interface and RGB interface 101 = Reserved 110 = WB Interface and i80 interface for LDI0 111 = WB Interface and i80 interface for LDI1	000
L1_DATA16	[25:23]	Selects output data format mode of indirect i80 interface (LDI1). (VIDOUT[1:0] == 2'b11) 000 = 16-bit mode (16 bpp) 001 = 16 + 2-bit mode (18 bpp) 010 = 9 + 9-bit mode (18 bpp) 011 = 16 + 8-bit mode (24 bpp) 100 = 18-bit mode (18bpp) 101 = 8 + 8-bit mode (16bpp)	000
L0_DATA16	[22:20]	Selects output data format mode of indirect i80 interface (LDI0). (VIDOUT[1:0] == 2'b10) 000 = 16-bit mode (16 bpp) 001 = 16 + 2-bit mode (18 bpp) 010 = 9 + 9-bit mode (18 bpp) 011 = 16 + 8-bit mode (24 bpp) 100 = 18-bit mode (18bpp) 101 = 8 + 8-bit mode (16bpp)	000
Reserved	[19]	Reserved (should be 0).	0
RGSPSEL	[18]	Selects display mode (VIDOUT[1:0] == 2'b00). 0 = RGB parallel format 1 = RGB serial format Selects the display mode (VIDOUT[1:0] != 2'b00). 0 = RGB parallel format	0
PNRMODE	[17]	Controls inverting RGB_ORDER (@VIDCON3). 0 = Normal: RGBORDER[2] @VIDCON3 1 = Invert: ~RGBORDER[2] @VIDCON3 Note: This bit is used for the previous version of FIMD. You do not have to use this bit if you use RGB_ORDER@VIDCON3 register.	00
CLKVALUP	[16]	Selects CLKVAL_F update timing control. 0 = Always 1 = Start of a frame (only once per frame)	0

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VIDCON0	Bit	Description	Initial State
Reserved	[15:14]	Reserved.	0
CLKVAL_F	[13:6]	Determines the rates of VCLK and CLKVAL[7:0]. VCLK = HCLK / (CLKVAL+1), where CLKVAL >= 1 Notes. 1. The maximum frequency of VCLK is 100Mhz(pad:50pf). 2. CLKSEL_F register selects Video Clock Source.	0
VCLKFREE	[5]	Controls VCLK Free Run (Only valid at RGB IF mode). 0 = Normal mode (controls using ENVID) 1 = Free-run mode	0
CLKDIR	[4]	Selects the clock source as direct or divide using CLKVAL_F register. 0 = Direct clock (frequency of VCLK = frequency of Clock source) 1 = Divided by CLKVAL_F	0x00
Reserved	[3]	Should be 0.	0x0
CLKSEL_F	[2]	Selects the video clock source. 0 = HCLK 1 = SCLK_FIMD HCLK is the bus clock, whereas SCLK_FIMD is the special clock for display controller. For more information, refer to Chapter, “02.03 CLOCK CONTROLLER”.	0
ENVID	[1]	Enables/ disables video output and logic immediately. 0 = Disables the video output and display control signal. 1 = Enables the video output and display control signal.	0
ENVID_F	[0]	Enables/ disables video output and logic at current frame end. 0 = Disables the video output and display control signal. 1 = Enables the video output and display control signal. * If this bit is set to “on” and “off”, then “H” is read and video controller is enabled until the end of current frame.	0

NOTE: Display On: ENVID and ENVID_F are set to “1”.
Direct Off: ENVID and ENVID_F are set to “0” simultaneously.
Per Frame Off: ENVID_F is set to “0” and ENVID is set to “1”.

Caution: 1: If VIDCON0 is set for Per Frame Off in interlace mode, the value of INTERLACE_F should be set to “0” in the same time.
2: If display controller is off using direct off, it is impossible to turn on the display controller without reset.

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1.5.2.2 Video Main Control 1 Register (VIDCON1, R/W, Address = 0xF800_0004)

VIDCON1	Bit	Description	Initial State
LINECNT (read only)	[26:16]	Provides the status of the line counter (read only). Up count from 0 to LINEVAL.	0
FSTATUS	[15]	Specifies the Field Status (read only). 0 = ODD Field 1 = EVEN Field	0
VSTATUS	[14:13]	Specifies the Vertical Status (read only). 00 = VSYNC 01 = BACK Porch 10 = ACTIVE 11 = FRONT Porch	0
Reserved	[12:11]	Reserved	0
FIXVCLK	[10:9]	Specifies the VCLK hold scheme at data under-flow. 00 = VCLK hold 01 = VCLK running 11 = VCLK running and VDEN disable	0
Reserved	[8]	Reserved	0
IVCLK	[7]	Controls the polarity of the VCLK active edge. 0 = Video data is fetched at VCLK falling edge 1 = Video data is fetched at VCLK rising edge	0
IHSYNC	[6]	Specifies the HSYNC pulse polarity. 0 = Normal 1 = Inverted	0
IVSYNC	[5]	Specifies the VSYNC pulse polarity. 0 = Normal 1 = Inverted	0
IVDEN	[4]	Specifies the VDEN signal polarity. 0 = Normal 1 = Inverted	0
Reserved	[3:0]	Reserved	0x0

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1.5.2.3 Video Main Control 2 Register (VIDCON2, R/W, Address = 0xF800_0008)

VIDCON2	Bit	Description	Initial State
Reserved	[31:28]	Reserved	0
RGB_SKIP_EN	[27]	Enables the RGB skip mode (only where RGBSPSEL == 1'b0). 0 = Disables 1 = Enables	0
Reserved	[26]	Reserved	0
RGB_DUMMY_LOC	[25]	Controls RGB dummy insertion location (only where RGBSPSEL == 1'b1 and RGB_DUMMY_EN == 1'b1) 0 = Last (4th) position 1 = 1st position	0
RGB_DUMMY_EN	[24]	Enables RGB dummy insertion mode (only where RGBSPSEL == 1'b1) 0 = Disables 1 = Enables	0
Reserved	[23:22]	Reserved (should be 0)	0
RGB_ORDER_E	[21:19]	Controls RGB interface output order (Even line, line # 2, 4, 6, 8.) , where, RGBSPSEL== 1'b0 000 = RGB 001 = GBR 010 = BRG 100 = BGR 101 = RBG 110 = GRB , where, (RGBSPSEL == 1'b1) or (RGBSPSEL == 1'b0 and RGB_SKIP_EN = 1'b1) 000 = R→G→B 001 = G→B→R 010 = B→R→G 100 = B→G→R 101 = R→B→G 110 = G→R→B Note: PNR0[0] @VIDCON0 should be 0, when you use RGB_ORDER_O[2:0] @VIDCON3 register.	0
RGB_ORDER_O	[18:16]	Controls RGB interface output order (Odd Line, line #1, 3, 5, 7.) , where, RGBSPSEL== 1'b0 000 = RGB 001 = GBR 010 = BRG 100 = BGR 101 = RBG 110 = GRB , where, (RGBSPSEL == 1'b1) or (RGBSPSEL == 1'b0 and RGB_SKIP_EN = 1'b1) 000 = R→G→B 001 = G→B→R	0

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VIDCON2	Bit	Description	Initial State
		010 = B→R→G 100 = B→G→R 101 = R→B→G 110 = G→R→B Note: PNR0[0] @VIDCON0 should be 0, when you use RGB_ORDER_E[2:0]@VIDCON3 register.	
Reserved	[15:14]	Reserved. Note: This bit should be 1.	0
TVFORMATSEL	[13:12]	Specifies the output format of YUV data. 00 = Reserved 01 = YUV422 1x = YUV444	0
Reserved	[11:9]	Reserved	0
OrgYCbCr	[8]	Specifies the order of YUV data. 0 = Y - CbCr 1 = CbCr - Y	0
YUVOrd	[7]	Specifies the order of Chroma data. 0 = Cb - Cr 1 = Cr - Cb	0
Reserved	[6:5]	Reserved	0
WB_FRAME_SKIP	[4:0]	Controls the WB frame skip rate. The maximum rate is up to 1:30 [only where (VIDOUT[2:0] == 3'b001 or 3'b100 TV encoder interface), (INTERLACE_F==1'b0) and (TV422 or TVRGB output)]. 00000 = no skip (1 : 1) 00001 = skip rate = 1 : 2 00010 = skip rate = 1 : 3 … 11101 = skip rate = 1 : 30 1111x = reserved	0

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1.5.2.4 Video Main Control 3 Register (vidcon3, R/W, ADDRESS = 0xF800_000C)

VIDCON3	Bit	Description	Initial State
Reserved	[31:21]	Reserved (should be 0)	0
Reserved	[20:19]	Reserved	0
CG_ON	[18]	Enables Control Color Gain. 0 = Disables (bypass) 1 = Enables	0
Reserved	[17]	Reserved	0
GM_ON	[16]	Enables Control Gamma. 0 = Disables (bypass) 1 = Enables	0
Reserved	[15]	Reserved	0
HUE_CSC_F_Narrow	[14]	Controls HUE CSC_F Narrow/ Wide. 0 = Wide 1 = Narrow	0
HUE_CSC_F_EQ709	[13]	Controls HUE_CSC_F parameter. 0 = Eq. 601 1 = Eq.709	0
HUE_CSC_F_ON	[12]	Enables HUE_CSC_F. 0 = Disables 1 = Enables (when HUE_ON == 1'b1)	0
Reserved	[11]	Reserved	0
HUE_CSC_B_Narrow	[10]	Controls HUE CSC_B Narrow/ Wide. 0 = Wide 1 = Narrow	0
HUE_CSC_B_EQ709	[9]	Controls HUE_CSC_B parameter. 0 = Eq. 601 1 = Eq.709	0
HUE_CSC_B_ON	[8]	Enables HUE_CSC_B. 0 = Disables 1 = Enables (when HUE_ON == 1'b1)	0
HUE_ON	[7]	Enables Control Hue. 0 = Disables (bypass) 1 = Enables	0
Resrved	[6:2]	Reserved (should be 0)	0
PC_DIR	[1]	Controls Pixel Compensation direction. 0 = + 0.5(pos.) 1 = - 0.5(neg.)	0
PC_ON	[3:0]	Enables Pixel Compensation. 0 = Disable 1 = Enable Note: TV output data is compensated by PC_ON == 1'b1.	0x0

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1.5.2.5 Video Time Control 0 Register (VIDTCON0, R/W, Address = 0xF800_0010)

VIDTCON0	Bit	Description	Initial State
VBPDE	[31:24]	Vertical back porch specifies the number of inactive lines at the start of a frame after vertical synchronization period. (Only for even field of YVU interface)	0x00
VBPD	[23:16]	Vertical back porch specifies the number of inactive lines at the start of a frame after vertical synchronization period.	0x00
VFPD	[15:8]	Vertical front porch specifies the number of inactive lines at the end of a frame before vertical synchronization period.	0x00
VSPW	[7:0]	Vertical sync pulse width determines the high-level width of VSYNC pulse by counting the number of inactive lines.	0x00

1.5.2.6 Video Time Control 1 Register (VIDTCON1, R/W, Address = 0xF800_0014)

VIDTCON1	Bit	Description	Initial State
VFPDE	[31:24]	Vertical front porch specifies the number of inactive lines at the end of a frame before vertical synchronization period. (Only for the even field of YVU interface).	0
HBPD	[23:16]	Horizontal back porch specifies the number of VCLK periods between the falling edge of HSYNC and start of active data.	0x00
HFPD	[15:8]	Horizontal front porch specifies the number of VCLK periods between the end of active data and rising edge of HSYNC.	0x00
HSPW	[7:0]	Horizontal sync pulse width determines the high-level width of HSYNC pulse by counting the number of VCLK.	0x00

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1.5.2.7 Video Time Control 2 Register (VIDTCON2, R/W, Address = 0xF800_0018)

VIDTCON2	Bit	Description	Initial State
LINEVAL	[21:11]	Determines the vertical size of display. In the Interlace mode, (LINEVAL + 1) should be even.	0
HOZVAL	[10:0]	Determines the horizontal size of display.	0

NOTE: HOZVAL = (Horizontal display size) -1 and LINEVAL = (Vertical display size) –1.

1.5.2.8 Video Time Control3 Register (VIDTCON3, R/W, Address = 0xF800_001C)

VIDTCON3	Bit	Description	Initial State
VSYNCEN	[31]	Enables VSYNC Signal Output. 0 = Disables 1 = Enables VBPD(VFPD, VSPW) + 1 < LINEVAL (when VSYNCEN =1)	0
Reserved	[30]	Reserved (should be 0).	0
FRMEN	[29]	Enables the FRM signal output. 0 = Disables 1 = Enables	0
INVFRM	[28]	Controls the polarity of FRM pulse. 0 = Active HIGH 1 = Active LOW	0
FRMVRATE	[27:24]	Controls the FRM issue rate (Maximum rate up to 1:16)	0x00
Reserved	[23:16]	Reserved	0x00
FRMVFPD	[15:8]	Specifies the number of line between data active and FRM signal.	0x00
FRMVSPW	[7:0]	Specifies the number of line of FRM signal width. (FRMVFPD + 1) + (FRMVSPW + 1) < LINEVAL + 1 (in RGB)	0x00

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1.5.2.9 Window 0 Control Register (WINCON0, R/W, Address = 0xF800_0020)

WINCON0	Bit	Description	Initial State
BUFSTATUS_H	[31]	Specifies the Buffer Status (read only). Note: BUFSTATUS = {BUFSTATUS_H, BUFSTATUS_L} 00 = Buffer set 0 01 = Buffer set 1 10 = Buffer set 2	0
BUFSEL_H	[30]	Selects the Buffer set. Note: BUFSEL = {BUFSEL_H, BUFSEL_L} 00 = Buffer set 0 01 = Buffer set 1 10 = Buffer set 2 (only available where BUF_MODE == 1'b1)	0
LIMIT_ON	[29]	Enables CSC source limiter (for clamping xvYCC source). 0 = Disables 1 = Enables (when local SRC data has xvYCC color space, InRGB=1)	0
EQ709	[28]	Controls CSC parameter. 0 = Eq. 601 1 = Eq. 709 (when local SRC data has HD (709) color gamut)	0
nWide/Narrow	[27:26]	Chooses the color space conversion equation from YCbCr to RGB according to input value range (2'00 for YCbCr Wide range and 2'11 for YCbCr Narrow range) - Wide Range: Y/ Cb/ Cr: 255-0 - Narrow Range: Y: 235-16, Cb/ Cr: 240-16	00
TRGSTATUS	[25]	Specifies the Trigger Status (read only). 0 = No trigger is issued 1 = Trigger is issued	0
Reserved	[24:23]	Reserved	00
ENLOCAL_F	[22]	Selects the Data access method. 0 = Dedicated DMA 1 = Local Path	0
BUFSTATUS_L	[21]	Specifies the Buffer Status (read only). Note: BUFSTATUS = {BUFSTATUS_H, BUFSTATUS_L}	0
BUFSEL_L	[20]	Selects the Buffer set. Note: BUFSEL = {BUFSEL_H, BUFSEL_L}	0
BUFAUTOEN	[19]	Specifies the Double Buffer Auto control bit. 0 = Fixed by BUFSEL 1 = Auto Changed by Trigger Input	0
BITSWP_F	[18]	Specifies the Bit swap control bit. 0 = Swap Disable 1 = Swap Enable Note: It should be 0 when ENLOCAL is 1.	0
BYTSWP_F	[17]	Specifies the Byte swaps control bit. 0 = Swap Disable	0

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WINCON0	Bit	Description	Initial State
		1 = Swap Enable Note: It should be 0 when ENLOCAL is 1.	
HAWSWP_F	[16]	Specifies the Half-Word swap control bit. 0 = Swap Disable 1 = Swap Enable Note: It should be 0 when ENLOCAL is 1.	0
WSWP_F	[15]	Specifies the Word swap control bit. 0 = Swap Disable 1 = Swap Enable Note: It should be 0 when ENLOCAL is 1.	0
BUF_MODE	[14]	Selects the auto-buffering mode. 0 = Double 1 = Triple	0
InRGB	[13]	Specifies the input color space of source image (only for 'ENLOCAL' enable). 0 = RGB 1 = YCbCr	0
-	[12:11]	Reserved (Should be 0)	0
BURSTLEN	[10:9]	Selects the DMA Burst Maximum Length. 00 = 16 word–burst 01 = 8 word–burst 10 = 4 word–burst	0
Reserved	[8:7]	-	0
BLD_PIX_F	[6]	Selects the blending category (In case of window0, this is only required for deciding window 0's blending factor.) 0 = Per plane blending 1 = Per pixel blending	0
BPPMODE_F	[5:2]	Selects the Bits Per Pixel (BPP) mode for Window image. 0000 = 1 bpp 0001 = 2 bpp 0010 = 4 bpp 0011 = 8 bpp (palletized) 0100 = 8 bpp (non-palletized, A: 1-R:2-G:3-B:2) 0101 = 16 bpp (non-palletized, R:5-G:6-B:5) 0110 = 16 bpp (non-palletized, A:1-R:5-G:5-B:5) 0111 = 16 bpp (non-palletized, I :1-R:5-G:5-B:5) 1000 = Unpacked 18 bpp (non-palletized, R:6-G:6-B:6) 1001 = Unpacked 18 bpp (non-palletized, A:1-R:6-G:6-B:5) 1010 = Unpacked 19 bpp (non-palletized, A:1-R:6-G:6-B:6) 1011 = Unpacked 24 bpp (non-palletized R:8-G:8-B:8) 1100 = Unpacked 24 bpp (non-palletized A:1-R:8-G:8-B:7) *1101 = Unpacked 25 bpp (non-palletized A:1-R:8-G:8-B:8) *1110 = Unpacked 13 bpp (non-palletized A:1-R:4-G:4-B:4) 1111 = Unpacked 15 bpp (non-palletized R:5-G:5-B:5)	0

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WINCON0	Bit	Description	Initial State
		Note: *1101 = Supports unpacked 32 bpp (non-palletized A:8-R:8-G:8-B:8) for per pixel blending. *1110 = Supports 16 bpp (non-palletized A:4-R:4-G:4-B:4) for per pixel blending. (16 level blending)	
ALPHA_SEL_F	[1]	Selects the Alpha value. When per plane blending case (BLD_PIX ==0): 0 = Using ALPHA0_R/G/B values 1 = Using ALPHA1_R/G/B values When per pixel blending (BLD_PIX ==1) 0 = Selected by AEN (A value) 1 = Using DATA[31:24] data in word boundary (only when BPPMODE_F = 4'b1101) DATA[31:28], [15:12] data in word boundary (only when BPPMODE_F = 4'b1110)	0
ENWIN_F	[0]	Enables/ disables video output and logic immediately. 0 = Disables the video output and video control signal. 1 = Enables the video output and video control signal.	0

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1.5.2.10 Window 1 Control Register (WINCON1, R/W, Address = 0xF800_0024)

WINCON1	Bit	Description	Initial State
BUFSTATUS_H	[31]	Specifies the Buffer Status (read only). Note: BUFSTATUS = {BUFSTATUS_H, BUFSTATUS_L} 00 = Buffer set 0 01 = Buffer set 1 10 = Buffer set 2	0
BUFSEL_H	[30]	Select the Buffer set. Note: BUFSEL = {BUFSEL_H, BUFSEL_L} 00 = Buffer set 0 01 = Buffer set 1 10 = Buffer set 2 (only available when BUF_MODE == 1'b1)	0
LIMIT_ON	[29]	Enables Control CSC source limiter (for clamping xvYCC source). 0 = Disables 1 = Enables (when local SRC data has xvYCC color space, InRGB=1)	0
EQ709	[28]	Controls the CSC parameter. 0 = Eq.601 1 = Eq.709 (when local SRC data has HD(709) color gamut)	0
nWide/Narrow	[27:26]	Chooses the color space conversion equation from YCbCr to RGB based on input value range (2'00 for YCbCr Wide range and 2'11 for YCbCr Narrow range). - Wide Range: Y/ Cb/ Cr: 255-0 - Narrow Range: Y: 235-16, Cb/ Cr: 240-16	00
TRGSTATUS	[25]	Specifies Window 0 Software Trigger Update Status (read only). 0 = Update 1 = Not Update If the Software Trigger in window 1 occurs, this bit is automatically set to '1'. This value is cleared only after updating the shadow register sets.	0
Reserved	[24:23]	Reserved. (should be 0)	0
ENLOCAL_F	[22]	Selects the Data access method. 0 = Dedicated DMA 1 = Local Path	0
BUFSTATUS_L	[21]	Specifies the Buffer Status (read only). Note: BUFSTATUS = {BUFSTATUS_H, BUFSTATUS_L}	0
BUFSEL_L	[20]	Selects the Buffer set. Note: BUFSEL = {BUFSEL_H, BUFSEL_L}	0
BUFAUTOEN	[19]	Specifies the Double Buffer Auto control bit. 0 = Fixed by BUFSEL 1 = Auto changed by Trigger Input	0
BITSWP_F	[18]	Specifies the Bit swap control bit. 0 = Swap Disable 1 = Swap Enable Note: It should be 0 when ENLOCAL is 1.	0

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WINCON1	Bit	Description	Initial State
BYTSWP_F	[17]	Specifies the Byte swaps control bit. 0 = Swap Disable 1 = Swap Enable Note: It should be 0 when ENLOCAL is 1.	0
HAWSWP_F	[16]	Specifies the Half-Word swap control bit. 0 = Swap Disable 1 = Swap Enable Note: It should be 0 when ENLOCAL is 1.	0
WSWP_F	[15]	Specifies the Word swap control bit. 0 = Swap Disable 1 = Swap Enable Note: It should be 0 when ENLOCAL is 1.	0
BUF_MODE	[14]	Selects the auto-buffering mode. 0 = Double 1 = Triple	0
InRGB	[13]	Indicates the input color space of source image (only for 'EnLcal' enable). 0 = RGB 1 = YCbCr	0
-	[12:11]	Reserved (should be 0)	0
BURSTLEN	[10:9]	Specifies the DMA's Burst Maximum Length selection. 00 = 16 word- burst 01 = 8 word- burst 10 = 4 word- burst	0
-	[8]	Reserved (should be 0)	0
ALPHA_MUL_F	[7]	Specifies the Multiplied Alpha value mode. 0 = Disables 1 = Enables multiplied mode When ALPHA_MUL is 1, set BLD_PIX =1, ALPHA_SEL=1, and BPPMODE_F[5:2] = 4'b1101 or 4'b1110. Note: Alpha value = alpha_pixel (from data) * ALPHA0_R/G/B	0
BLD_PIX_F	[6]	Selects the blending category. 0 = Per plane blending 1 = Per pixel blending	0
BPPMODE_F	[5:2]	Selects the Bits Per Pixel (BPP) mode in Window image. 0000 = 1 bpp 0001 = 2 bpp 0010 = 4 bpp 0011 = 8 bpp (palletized) 0100 = 8 bpp (non-palletized, A: 1-R:2-G:3-B:2) 0101 = 16 bpp (non-palletized, R:5-G:6-B:5) 0110 = 16 bpp (non-palletized, A:1-R:5-G:5-B:5) 0111 = 16 bpp (non-palletized, I :1-R:5-G:5-B:5) 1000 = Unpacked 18 bpp (non-palletized, R:6-G:6-B:6) 1001 = Unpacked 18 bpp (non-palletized, A:1-R:6-G:6-B:5)	0

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WINCON1	Bit	Description	Initial State
		1010 = Unpacked 19 bpp (non-palletized, A:1-R:6-G:6-B:6) 1011 = Unpacked 24 bpp (non-palletized R:8-G:8-B:8) 1100 = Unpacked 24 bpp (non-palletized A:1-R:8-G:8-B:7) *1101 = Unpacked 25 bpp (non-palletized A:1-R:8-G:8-B:8) *1110 = Unpacked 13 bpp (non-palletized A:1-R:4-G:4-B:4) 1111 = Unpacked 15 bpp (non-palletized R:5-G:5-B:5) Note: *1101 = supports unpacked 32 bpp (non-palletized A:8-R:8-G:8-B:8) for per pixel blending. *1110 = supports 16 bpp (non-palletized A:4-R:4-G:4-B:4) for per pixel blending. (16 level blending)	
ALPHA_SEL_F	[1]	Selects the Alpha value. When Per plane blending case (BLD_PIX ==0) 0 = Using ALPHA0_R/G/B values 1 = Using ALPHA1_R/G/B values When Per pixel blending (BLD_PIX ==1) 0 = Selected by AEN (A value) 1 = Using DATA[31:24] data in word boundary (only when BPPMODE_F = 4'b1101) DATA[31:28], [15:12] data in word boundary (only when BPPMODE_F = 4'b1110)	0
ENWIN_F	[0]	Enables/ disables video output and logic immediately. 0 = Disables the video output and video control signal. 1 = Enables the video output and video control signal.	0

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1.5.2.11 Window 2 Control Register (WINCON2, R/W, Address = 0xF800_0028)

WINCON2	Bit	Description	Initial State
BUFSTATUS_H	[31]	Specifies the Buffer Status (read only). Note. BUFSTATUS = {BUFSTATUS_H, BUFSTATUS_L} 00 = Buffer set 0 01 = Buffer set 1 10 = Buffer set 2	0
BUFSEL_H	[30]	Selects the Buffer set. Note. BUFSEL = {BUFSEL_H, BUFSEL_L} 00 = Buffer set 0 01 = Buffer set 1 10 = Buffer set 2 (only available when BUF_MODE == 1'b1)	0
LIMIT_ON	[29]	Enables CSC source limiter (for clamping xvYCC source). 0 = Disables 1 = Enables (when local SRC data has xvYCC color space, InRGB=1)	0
EQ709	[28]	Controls CSC parameter. 0 = Eq.601 1 = Eq.709 (when local SRC data has HD (709) color gamut)	0
nWide/Narrow	[27:26]	Chooses color space conversion equation from YCbCr to RGB based on the input value range (2'00 for YCbCr Wide range and 2'11 for YCbCr Narrow range). - Wide Range: Y/ Cb/ Cr: 255-0 - Narrow Range: Y: 235-16, Cb/ Cr: 240-16	00
Reserved	[25:24]	Reserved	00
Reserved	[23]	Should be '0'.	0
ENLOCAL_F	[22]	Selects the Data access method. 0 = Dedicated DMA 1 = Local Path	0
BUFSTATUS_L	[21]	Specifies the Buffer Status (read only). Note: BUFSTATUS = {BUFSTATUS_H, BUFSTATUS_L}	
BUFSEL_L	[20]	Selects the Buffer set. Note: BUFSEL = {BUFSEL_H, BUFSEL_L}	0
BUFAUTOEN	[19]	Specifies the Double Buffer Auto control bit. 0 = Fixed by BUFSEL 1 = Auto changed by Trigger Input	0
BITSWP_F	[18]	Specifies the Bit swap control bit. 0 = Swap Disable 1 = Swap Enable Note: It should be 0 when ENLOCAL is 1.	0
BYTSWP_F	[17]	Specifies the Byte swaps control bit. 0 = Swap Disable 1 = Swap Enable Note: It should be 0 when ENLOCAL is 1.	0

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WINCON2	Bit	Description	Initial State
HAWSWP_F	[16]	Specifies the Half-Word swap control bit. 0 = Swap Disable 1 = Swap Enable Note: It should be 0 when ENLOCAL is 1.	0
WSWP_F	[15]	Specifies the Word swap control bit. 0 = Swap Disable 1 = Swap Enable Note: It should be 0 when ENLOCAL is 1.	0
BUF_MODE	[14]	Selects the auto-buffering mode. 0 = Double 1 = Triple	0
InRGB	[13]	Specifies the input color space of source image (only for 'EnLcal' enable). 0 = RGB 1 = YCbCr	0
-	[12:11]	Reserved (should be 0).	0
BURSTLEN	[10:9]	Selects the DMA's Burst Maximum Length. 00 = 16 word- burst 01 = 8 word- burst 10 = 4 word- burst	0
-	[8]	Reserved (should be 0).	0
ALPHA_MUL_F	[7]	Specifies the Multiplied Alpha value mode. 0 = Disables 1 = Enables multiplied mode When ALPHA_MUL is 1, set BLD_PIX =1, ALPHA_SEL=1, and BPPMODE_F[5:2] = 4'b1101 or 4'b1110. Note: Alpha value = alpha_pixel (from data) * ALPHA0_R/G/B	0
BLD_PIX_F	[6]	Selects the blending category. 0 = Per plane blending 1 = Per pixel blending	0
BPPMODE_F	[5:2]	Selects the Bits Per Pixel (BPP) mode in Window image. 0000 = 1 bpp 0001 = 2 bpp 0010 = 4 bpp 0011 = 8 bpp (palletized) 0100 = 8 bpp (non-palletized, A: 1-R:2-G:3-B:2) 0101 = 16 bpp (non-palletized, R:5-G:6-B:5) 0110 = 16 bpp (non-palletized, A:1-R:5-G:5-B:5) 0111 = 16 bpp (non-palletized, I :1-R:5-G:5-B:5) 1000 = Unpacked 18 bpp (non-palletized, R:6-G:6-B:6) 1001 = Unpacked 18 bpp (non-palletized, A:1-R:6-G:6-B:5) 1010 = Unpacked 19 bpp (non-palletized, A:1-R:6-G:6-B:6) 1011 = Unpacked 24 bpp (non-palletized R:8-G:8-B:8) 1100 = Unpacked 24 bpp (non-palletized A:1-R:8-G:8-B:7) *1101 = Unpacked 25 bpp (non-palletized A:1-R:8-G:8-B:8) *1110 = Unpacked 13 bpp (non-palletized A:1-R:4-G:4-B:4)	0

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WINCON2	Bit	Description	Initial State
		1111 = Unpacked 15 bpp (non-palletized R:5-G:5-B:5) Note: *1101 = Supports unpacked 32 bpp (non-palletized A:8-R:8-G:8-B:8) for per pixel blending. *1110 = Supports 16 bpp (non-palletized A:4-R:4-G:4-B:4) for per pixel blending. (16 level blending)	
ALPHA_SEL_F	[1]	Selects the Alpha value. When Per plane blending case BLD_PIX ==0: 0 = Using ALPHA0_R/G/B values 1 = Using ALPHA1_R/G/B values When Per pixel blending BLD_PIX ==1: 0 = Selected by AEN (A value) 1 = Using DATA[31:24] data in word boundary (only when BPPMODE_F = 4'b1101) DATA[31:28], [15:12] data in word boundary (only when BPPMODE_F = 4'b1110)	0
ENWIN_F	[0]	Enables/ disables the video output and logic immediately. 0 = Disables the video output and video control signal. 1 = Enables the video output and video control signal.	0

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1.5.2.12 Window 3 Control Register (WINCON3, R/W, Address = 0xF800_002C)

WINCON3	Bit	Description	Initial State
BUFSTATUS_H	[31]	Specifies the Buffer Status (read only). Note: BUFSTATUS = {BUFSTATUS_H, BUFSTATUS_L} 00 = Buffer set 0 01 = Buffer set 1 10 = Buffer set 2	
BUFSEL_H	[30]	Selects the Buffer set Note: BUFSEL = {BUFSEL_H, BUFSEL_L} 00 = Buffer set 0 01 = Buffer set 1 10 = Buffer set 2 (only available where BUF_MODE == 1'b1)	
-	[29:26]	Reserved (should be 0).	
TRIGSTATUS	[25]	Specifies the Trigger Status (read only) 0 = No trigger is issued 1 = Trigger is issued	
-	[24:22]	Reserved (should be 0).	
BUFSTATUS_L	[21]	Specifies the Buffer Status (read only). Note: BUFSTATUS = {BUFSTATUS_H, BUFSTATUS_L}	
BUFSEL_L	[20]	Selects the Buffer set. Note: BUFSEL = {BUFSEL_H, BUFSEL_L}	
BUFAUTOEN	[19]	Specifies the Double Buffer Auto control bit. 0 = Fixed by BUFSEL 1 = Auto changed by Trigger Input	
BITSWP_F	[18]	Specifies the Bit swap control bit. 0 = Swap Disable 1 = Swap Enable	0
BYTSWP_F	[17]	Specifies the Byte swaps control bit. 0 = Swap Disable 1 = Swap Enable	0
HAWSWP_F	[16]	Specifies the Half-Word swap control bit. 0 = Swap Disable 1 = Swap Enable	0
WSWP_F	[15]	Specifies the Word swap control bit. 0 = Swap Disable 1 = Swap Enable	
BUF_MODE	[14]	Selects the auto-buffering mode. 0 = Double 1 = Triple	0
-	[13:11]	Reserved (should be 0).	0
BURSTLEN	[10:9]	Selects the DMA Burst Maximum Length. 00 = 16 word- burst 01 = 8 word- burst 10 = 4 word- burst	0

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WINCON3	Bit	Description	Initial State
-	[8]	Reserved (should be 0).	0
ALPHA_MUL_F	[7]	Specifies the Multiplied Alpha value mode. 0 = Disables 1 = Enables multiplied mode When ALPHA_MUL is 1, set BLD_PIX =1, ALPHA_SEL=1, and BPPMODE_F[5:2] = 4'b1101 or 4'b1110. Note. Alpha value = alpha_pixel (from data) * ALPHA0_R/G/B	0
BLD_PIX_F	[6]	Selects the blending category. 0 = Per plane blending 1 = Per pixel blending	
BPPMODE_F	[5:2]	Selects the Bits Per Pixel (BPP) mode in Window image. 0000 = 1 bpp 0001 = 2 bpp 0010 = 4 bpp 0011 = 8 bpp (palletized) 0100 = 8 bpp (non-palletized, A: 1-R:2-G:3-B:2) 0101 = 16 bpp (non-palletized, R:5-G:6-B:5) 0110 = 16 bpp (non-palletized, A:1-R:5-G:5-B:5) 0111 = 16 bpp (non-palletized, I :1-R:5-G:5-B:5) 1000 = Unpacked 18 bpp (non-palletized, R:6-G:6-B:6) 1001 = Unpacked 18 bpp (non-palletized, A:1-R:6-G:6-B:5) 1010 = Unpacked 19 bpp (non-palletized, A:1-R:6-G:6-B:6) 1011 = Unpacked 24 bpp (non-palletized R:8-G:8-B:8) 1100 = Unpacked 24 bpp (non-palletized A:1-R:8-G:8-B:7) *1101 = Unpacked 25 bpp (non-palletized A:1-R:8-G:8-B:8) *1110 = Unpacked 13 bpp (non-palletized A:1-R:4-G:4-B:4) 1111 = Unpacked 15 bpp (non-palletized R:5-G:5-B:5) Note: *1101 = Supports unpacked 32 bpp (non-palletized A:8-R:8-G:8-B:8) for per pixel blending. *1110 = Supports 16 bpp (non-palletized A:4-R:4-G:4-B:4) for per pixel blending. (16 level blending)	0
ALPHA_SEL_F	[1]	Selects the Alpha value. When Per plane blending case BLD_PIX ==0: 0 = Using ALPHA0_R/G/B values 1 = Using ALPHA1_R/G/B values When Per pixel blending BLD_PIX ==1: 0 = Selected by AEN (A value) 1 = Using DATA[31:24] data in word boundary (only when BPPMODE_F = 4'b1101) DATA[31:28], [15:12] data in word boundary (only when BPPMODE_F = 4'b1110)	0
ENWIN_F	[0]	Enables/ disables video output and logic immediately. 0 = Disables the video output and video control signal. 1 = Enables the video output and video control signal.	0

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1.5.2.13 Window 4 Control Register (WINCON4, R/W, Address = 0xF800_0030)

WINCON4	Bit	Description	Initial State
BUFSTATUS_H	[31]	Specifies the Buffer Status (read only). Note: BUFSTATUS = {BUFSTATUS_H, BUFSTATUS_L} 00 = Buffer set 0 01 = Buffer set 1 10 = Buffer set 2	0
BUFSEL_H	[30]	Selects the Buffer set. Note: BUFSEL = {BUFSEL_H, BUFSEL_L} 00 = Buffer set 0 01 = Buffer set 1 10 = Buffer set 2 (only available where BUF_MODE == 1'b1)	0
-	[29:26]	Reserved (should be 0).	0
TRIGSTATUS	[25]	Specifies the Trigger Status (read only). 0 = No trigger is issued 1 = Trigger is issued	0
-	[24:22]	Reserved (should be 00).	0
BUFSTATUS_L	[21]	Specifies the Buffer Status (read only). Note: BUFSTATUS = {BUFSTATUS_H, BUFSTATUS_L}	0
BUFSEL_L	[20]	Selects the Buffer set. Note: BUFSEL = {BUFSEL_H, BUFSEL_L}	0
BUFAUTOEN	[19]	Specifies the Double Buffer Auto control bit. 0 = Fixed by BUFSEL 1 = Auto changed by Trigger Input	0
BITSWP_F	[18]	Specifies the Bit swap control bit. 0 = Swap Disable 1 = Swap Enable	0
BYTSWP_F	[17]	Specifies the Byte swap control bit. 0 = Swap Disable 1 = Swap Enable	0
HAWSWP_F	[16]	Specifies the Half-Word swap control bit. 0 = Swap Disable 1 = Swap Enable	0
WSWP_F	[15]	Specifies the Word swap control bit. 0 = Swap Disable 1 = Swap Enable	0
BUF_MODE	[14]	Selects the auto-buffering mode. 0 = Double 1 = Triple	0
-	[13:11]	Reserved (should be 0).	0
BURSTLEN	[10:9]	Selects the DMA Burst Maximum Length. 00 = 16 word- burst 01 = 8 word- burst 10 = 4 word- burst	0

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WINCON4	Bit	Description	Initial State
-	[8]	Reserved (should be 0)	0
ALPHA_MUL_F	[7]	Specifies the Multiplied Alpha value mode. 0 = Disables 1 = Enables multiplied mode When ALPHA_MUL is 1, set BLD_PIX =1, ALPHA_SEL=1, and BPPMODE_F[5:2] = 4'b1101 or 4'b1110. Note: Alpha value = alpha_pixel (from data) * ALPHA0_R/G/B	0
BLD_PIX_F	[6]	Selects the blending category. 0 = Per plane blending 1 = Per pixel blending	0
BPPMODE_F	[5:2]	Selects the Bits Per Pixel (BPP) mode in Window image. 0000 = 1 bpp 0001 = 2 bpp 0010 = 4 bpp 0011 = 8 bpp (palletized) 0100 = 8 bpp (non-palletized, A: 1-R:2-G:3-B:2) 0101 = 16 bpp (non-palletized, R:5-G:6-B:5) 0110 = 16 bpp (non-palletized, A:1-R:5-G:5-B:5) 0111 = 16 bpp (non-palletized, I :1-R:5-G:5-B:5) 1000 = Unpacked 18 bpp (non-palletized, R:6-G:6-B:6) 1001 = Unpacked 18 bpp (non-palletized, A:1-R:6-G:6-B:5) 1010 = Unpacked 19 bpp (non-palletized, A:1-R:6-G:6-B:6) 1011 = Unpacked 24 bpp (non-palletized, R:8-G:8-B:8) 1100 = Unpacked 24 bpp (non-palletized, A:1-R:8-G:8-B:7) *1101 = Unpacked 25 bpp (non-palletized, A:1-R:8-G:8-B:8) *1110 = Unpacked 13 bpp (non-palletized, A:1-R:4-G:4-B:4) 1111 = Unpacked 15 bpp (non-palletized, R:5-G:5-B:5) Note: *1101 = Support unpacked 32 bpp (non-palletized, A:8-R:8-G:8-B:8) for per pixel blending. *1110 = Support 16 bpp (non-palletized A:4-R:4-G:4-B:4) for per pixel blending. (16 level blending)	0
ALPHA_SEL_F	[1]	Selects the Alpha value. When Per plane blending case BLD_PIX ==0: 0 = Using ALPHA0_R/G/B values 1 = Using ALPHA1_R/G/B values When Per pixel blending BLD_PIX ==1: 0 = Selected by AEN (A value) 1 = Using DATA[31:24] data in word boundary (only when BPPMODE_F = 4'b1101) DATA[31:28], [15:12] data in word boundary (only when BPPMODE_F = 4'b1110)	0
ENWIN_F	[0]	Enables/ disables video output and logic immediately. 0 = Disables the video output and video control signal. 1 = Enables the video output and video control signal.	0

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1.5.2.14 Window Shadow Control Register (VIDOSD0C, R/W, Address = 0xF800_0034)

SHODOWCON	Bit	Description	Initial State
-	[31:15]	Reserved (should be 0).	0
W4_SHADOW _PROTECT	[14]	Protects to update window 4's shadow register (xxx_F). 0 = Updates shadow register per fram0 1 = Protects to update (updates shadow register at next frame after 'SHADOW_PROTECT' turns to be 1'b0)	0
W3_SHADOW _PROTECT	[13]	Protects to update window 3's shadow register (xxx_F) 0 = Updates shadow register per frame 1 = Protects to update (updates shadow register at next frame after 'SHADOW_PROTECT' turns to be 1'b0)	0
W2_SHADOW _PROTECT	[12]	Protects to update window 2's shadow register (xxx_F) 0 = Updates shadow register per frame 1 = Protects to update (updates shadow register at next frame after 'SHADOW_PROTECT' turns to be 1'b0)	0
W1_SHADOW _PROTECT	[11]	Protects to update window 1's shadow register (xxx_F) 0 = Updates shadow register per frame 1 = Protects to update (update shadow register at next frame after 'SHADOW_PROTECT' turns to be 1'b0)	0
W0_SHADOW _PROTECT	[10]	Protects to update window 0's shadow register (xxx_F) 0 = Updates shadow register per frame 1 = Protects to update (update shadow register at next frame after 'SHADOW_PROTECT' turns to be 1'b0)	0
-	[9:8]	Reserved	0
C2_ENLOCAL_F	7	Enables Channel 2 Local Path. 0 = Disables 1 = Enables	0
C1_ENLOCAL_F	6	Enables Channel 1 Local Path. 0 = Disables 1 = Enables	0
C0_ENLOCAL_F	5	Enables Channel 0 Local Path. 0 = Disables 1 = Enables	0
C4_EN_F	4	Enables Channel 4. 0 = Disables 1 = Enables	0
C3_EN_F	3	Enables Channel 3. 0 = Disables 1 = Enables	0
C2_EN_F	2	Enables Channel 2. 0 = Disables 1 = Enables	0
C1_EN_F	1	Enables Channel 1. 0 = Disables 1 = Enables	0
C0_EN_F	0	Enables Channel 0. 0 = Disables 1 = Enables	0

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1.5.2.15 Channel Mapping Control Register2 (WINCHMAP2, R/W, Address = 0xEE00_ 003C)

WINCHMAP2	Bit	Description	Initial State
CH4FISEL	[30:28]	Selects Channel 4's channel. 001 = Window 0 010 = Window 1 101 = Window 2 110 = Window 3 111 = Window 4	111
CH3FISEL	[27:25]	Selects Channel 3's channel. 001 = Window 0 010 = Window 1 101 = Window 2 110 = Window 3 111 = Window 4	110
CH2FISEL	[24:22]	Selects Channel 2's channel. 001 = Window 0 010 = Window 1 101 = Window 2 110 = Window 3 111 = Window 4	101
CH1FISEL	[21:19]	Selects Channel 1's channel. 001 = Window 0 010 = Window 1 101 = Window 2 110 = Window 3 111 = Window 4	010
CH0FISEL	[18:16]	Selects Channel 0's channel. 001 = Window 0 010 = Window 1 101 = Window 2 110 = Window 3 111 = Window 4	001
W4FISEL	[14:12]	Selects Window 4's channel. 001 = Channel 0 010 = Channel 1 101 = Channel 2 110 = Channel 3 111 = Channel 4	111
W3FISEL	[11:9]	Selects Window 3's channel. 001 = Channel 0 010 = Channel 1 101 = Channel 2 110 = Channel 3 111 = Channel 4	110
W2FISEL	[8:6]	Selects Window 2's channel. 001 = Channel 0 010 = Channel 1 101 = Channel 2	101

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WINCHMAP2	Bit	Description	Initial State
		110 = Channel 3 111 = Channel 4	
W1FISEL	[5:3]	Selects Window 1's channel. 001 = Channel 0 010 = Channel 1 101 = Channel 2 110 = Channel 3 111 = Channel 4	010
W0FISEL	[2:0]	Selects Window 0's channel. 001 = Channel 0 010 = Channel 1 101 = Channel 2 110 = Channel 3 111 = Channel 4	001

1.5.2.16 Window 0 Position Control A Register (VIDOSD0A, R/W, Address = 0xF800_0040)

VIDOSD0A	Bit	Description	Initial State
OSD_LeftTopX_F	[21:11]	Specifies the horizontal screen coordinate for left top pixel of OSD image.	0
OSD_LeftTopY_F	[10:0]	Specifies the vertical screen coordinate for left top pixel of OSD image (For interlace TV output, this value must be set to half of the original screen y coordinate. The original screen y coordinate must be even.)	0

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1.5.2.17 Window 0 Position Control B Register (VIDOSD0B, R/W, Address = 0xF800_0044)

VIDOSD0B	Bit	Description	Initial State
OSD_RightBotX_F	[21:11]	Specifies the horizontal screen coordinate for right bottom pixel of OSD image.	0
OSD_RightBotY_F	[10:0]	Specifies the vertical screen coordinate for right bottom pixel of OSD image. (For interlace TV output, this value must be set to half of the original screen y coordinate. The original screen y coordinate must be odd value.)	0

NOTE: Registers must have word boundary X position. Therefore, 24 BPP mode must have X position by 1 pixel. (For example, X = 0, 1, 2, 3….)
16 BPP mode must have X position by 2 pixel. (For example, X = 0, 2, 4, 6….)
8 BPP mode must have X position by 4 pixel. (For example, X = 0, 4, 8, 12….)

1.5.2.18 Window 0 Position Control C Register (VIDOSD0C, R/W, Address = 0xF800_0048)

VIDOSD0C	Bit	Description	Initial State
Reserved	[25:24]	Reserved (should be 0)	0
OSDSIZE	[23:0]	Specifies the Window Size For example, Height * Width (Number of Word)	0

1.5.2.19 Window 1 Position Control A Register (VIDOSD0C, R/W, Address = 0xF800_0050)

VIDOSD1A	Bit	Description	Initial State
OSD_LeftTopX_F	[21:11]	Specifies the Horizontal screen coordinate for left top pixel of OSD image.	0
OSD_LeftTopY_F	[10:0]	Specifies the Vertical screen coordinate for left top pixel of OSD image. (For interlace TV output, this value must be set to half of the original screen y coordinate. The original screen y coordinate must be even.)	0

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1.5.2.20 Window 1 Position Control B Register (VIDOSD1B, R/W, Address = 0xF800_0054)

VIDOSD1B	Bit	Description	Initial State
OSD_RightBotX_F	[21:11]	Specifies the horizontal screen coordinate for right bottom pixel of OSD image.	0
OSD_RightBotY_F	[10:0]	Specifies the vertical screen coordinate for right bottom pixel of OSD image. (For interlace TV output, this value must be set to half of the original screen y coordinate. The original screen y coordinate must be odd value.)	0

NOTE: Registers must have word boundary X position.
Therefore, 24 BPP mode must have X position by 1 pixel. (For example, X = 0, 1, 2, 3….)
16 BPP mode must have X position by 2 pixel. (For example, X = 0, 2, 4, 6….)
8 BPP mode must have X position by 4 pixel. (For example, X = 0, 4, 8, 12….)

1.5.2.21 Window 1 Position Control C Register (VIDOSD1C, R/W, Address = 0xF800_0058)

VIDOSD1C	Bit	Description	Initial State
Reserved	[24]	Reserved	0
ALPHA0_R_H_F	[23:20]	Specifies Red Alpha upper value (case AEN == 0)	0
ALPHA0_G_H_F	[19:16]	Specifies Green Alpha upper value (case AEN == 0)	0
ALPHA0_B_H_F	[15:12]	Specifies Blue Alpha upper value (case AEN == 0)	0
ALPHA1_R_H_F	[11:8]	Specifies Red Alpha upper value (case AEN == 1)	0
ALPHA1_G_H_F	[7:4]	Specifies Green Alpha upper value (case AEN == 1)	0
ALPHA1_B_H_F	[3:0]	Specifies Blue Alpha upper value (case AEN == 1)	0

NOTE: Refer to VIDW1ALPHA0,1 register

1.5.2.22 Window 1 Position Control D Register (VIDOSD1D, R/W, Address = 0xF800_005C)

VIDOSD1D	Bit	Description	Initial State
Reserved	[25:24]	Reserved (should be 0)	0
OSDSIZE	[23:0]	Specifies Window Size. For example, Height * Width(Number of Word)	0

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1.5.2.23 Window 2 Position Control A Register (VIDOSD2A, R/W, Address = 0xF800_0060)

VIDOSD2A	Bit	Description	Initial State
OSD_LeftTopX_F	[21:11]	Specifies the horizontal screen coordinate for left top pixel of OSD image.	0
OSD_LeftTopY_F	[10:0]	Specifies the vertical screen coordinate for left top pixel of OSD image. (For interlace TV output, this value must be set to half of the original screen y coordinate. The original screen y coordinate must be even value.)	0

1.5.2.24 Window 2 Position Control B Register (VIDOSD2B, R/W, Address = 0xF800_0064)

VIDOSD2B	Bit	Description	Initial State
OSD_RightBotX_F	[21:11]	Specifies the horizontal screen coordinate for right bottom pixel of OSD image.	0
OSD_RightBotY_F	[10:0]	Specifies the vertical screen coordinate for right bottom pixel of OSD image. (For interlace TV output, this value must be set to half of the original screen y coordinate. The original screen y coordinate must be odd value.)	0

NOTE: Registers must have word boundary X position.
Therefore, 24 BPP mode must have X position by 1 pixel. (For example, X = 0, 1, 2, 3….)
16 BPP mode must have X position by 2 pixel. (For example, X = 0, 2, 4, 6….)
8 BPP mode must have X position by 4 pixel. (For example, X = 0, 4, 8, 12….)

1.5.2.25 Window 2 Position Control C Register (VIDOSD2C, R/W, Address = 0xF800_0068)

VIDOSD2C	Bit	Description	Initial State
Reserved	[24]	Reserved	0
ALPHA0_R_H_F	[23:20]	Specifies the Red Alpha upper value (case AEN == 0).	0
ALPHA0_G_H_F	[19:16]	Specifies the Green Alpha upper value (case AEN == 0).	0
ALPHA0_B_H_F	[15:12]	Specifies the Blue Alpha upper value (case AEN == 0).	0
ALPHA1_R_H_F	[11:8]	Specifies the Red Alpha upper value (case AEN == 1).	0
ALPHA1_G_H_F	[7:4]	Specifies the Green Alpha upper value (case AEN == 1).	0
ALPHA1_B_H_F	[3:0]	Specifies the Blue Alpha upper value (case AEN == 1).	0

NOTE: For more information, refer to VIDW2ALPHA0,1 register.

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1.5.2.26 Window 2 Position Control D Register (VIDOSD2D, R/W, Address = 0xF800_006C)

VIDOSD2D	Bit	Description	Initial State
Reserved	[25:24]	Reserved (should be 0)	0
OSDSIZE	[23:0]	Specifies the Window Size For example, Height * Width(Number of Word)	0

1.5.2.27 Window 3 Position Control A Register (VIDOSD3A, R/W, Address = 0xF800_0070)

VIDOSD3A	Bit	Description	Initial State
OSD_LeftTopX_F	[21:11]	Specifies the Horizontal screen coordinate for left top pixel of OSD image	0
OSD_LeftTopY_F	[10:0]	Specifies the Vertical screen coordinate for left top pixel of OSD image. (For interlace TV output, this value must be set to half of the original screen y coordinate. The original screen y coordinate must be even value.)	0

1.5.2.28 Window 3 Position Control B Register (VIDOSD3B, R/W, Address = 0xF800_0074)

VIDOSD3B	Bit	Description	Initial State
OSD_RightBotX_F	[21:11]	Specifies the Horizontal screen coordinate for right bottom pixel of OSD image.	0
OSD_RightBotY_F	[10:0]	Specifies the Vertical screen coordinate for right bottom pixel of OSD image. (For interlace TV output, this value must be set to half of the original screen y coordinate. The original screen y coordinate must be odd value.)	0

NOTE: Registers must have word boundary X position.
Therefore, 24 BPP mode must have X position by 1 pixel. (For example, X = 0, 1, 2, 3….)
16 BPP mode must have X position by 2 pixel. (For example, X = 0, 2, 4, 6….)
8 BPP mode must have X position by 4 pixel. (For example, X = 0, 4, 8, 12….)

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1.5.2.29 Window 3 Position Control C Register (VIDOSD3C, R/W, Address = 0xF800_0078)

VIDOSD3C	Bit	Description	Initial State
Reserved	[24]	Reserved	0
ALPHA0_R_H_F	[23:20]	Specifies the Red Alpha upper value (case AEN == 0).	0
ALPHA0_G_H_F	[19:16]	Specifies the Green Alpha upper value (case AEN == 0).	0
ALPHA0_B_H_F	[15:12]	Specifies the Blue Alpha upper value (case AEN == 0).	0
ALPHA1_R_H_F	[11:8]	Specifies the Red Alpha upper value (case AEN == 1).	0
ALPHA1_G_H_F	[7:4]	Specifies the Green Alpha upper value (case AEN == 1).	0
ALPHA1_B_H_F	[3:0]	Specifies the Blue Alpha upper value (case AEN == 1).	0

NOTE: For more information, refer to VIDW3ALPHA0, 1 register.

1.5.2.30 Window 4 Position Control A Register (VIDOSD4A, R/W, Address = 0xF800_0080)

VIDOSD4A	Bit	Description	Initial State
OSD_LeftTopX_F	[21:11]	Specifies the Horizontal screen coordinate for left top pixel of OSD image.	0
OSD_LeftTopY_F	[10:0]	Specifies the Vertical screen coordinate for left top pixel of OSD image. (For interlace TV output, this value must be set to half of the original screen y coordinate. The original screen y coordinate MUST be even value.)	0

1.5.2.31 Window 4 Position Control B Register (VIDOSD4B, R/W, Address = 0xF800_0084)

VIDOSD4B	Bit	Description	Initial State
OSD_RightBotX_F	[21:11]	Specifies the Horizontal screen coordinate for right bottom pixel of OSD image.	0
OSD_RightBotY_F	[10:0]	Specifies the Vertical screen coordinate for right bottom pixel of OSD image. (For interlace TV output, this value must be set to half of the original screen y coordinate. The original screen y coordinate MUST be odd value.)	0

NOTE: Registers must have word boundary X position.
Therefore, 24 BPP mode must have X position by 1 pixel. (For example, X = 0, 1, 2, 3….)
16 BPP mode must have X position by 2 pixel. (For example, X = 0, 2, 4, 6….)
8 BPP mode must have X position by 4 pixel. (For example, X = 0, 4, 8, 12….)

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1.5.2.32 Window 4 Position Control C Register (VIDOSD4C, R/W, Address = 0xF800_0088)

VIDOSD4C	Bit	Description	Initial State
Reserved	[24]	Reserved	0
ALPHA0_R_H_F	[23:20]	Specifies the Red Alpha upper value (case AEN == 0).	0
ALPHA0_G_H_F	[19:16]	Specifies the Green Alpha upper value (case AEN == 0).	0
ALPHA0_B_H_F	[15:12]	Specifies the Blue Alpha upper value (case AEN == 0).	0
ALPHA1_R_H_F	[11:8]	Specifies the Red Alpha upper value (case AEN == 1).	0
ALPHA1_G_H_F	[7:4]	Specifies the Green Alpha upper value (case AEN == 1).	0
ALPHA1_B_H_F	[3:0]	Specifies the Blue Alpha upper value (case AEN == 1).	0

NOTE: For more information, refer to VIDW4ALPHA0,1 register.

1.5.2.33 Frame Buffer Address 0 Register (VIDW)

- VIDW00ADD0B0, R/W, Address = 0xF800_00A0
- VIDW00ADD0B1, R/W, Address = 0xF800_00A4
- VIDW00ADD0B2, R/W, Address = 0xF800_20A0
- VIDW01ADD0B0, R/W, Address = 0xF800_00A8
- VIDW01ADD0B1, R/W, Address = 0xF800_00AC
- VIDW01ADD0B2, R/W, Address = 0xF800_20A8
- VIDW02ADD0B0, R/W, Address = 0xF800_00B0
- VIDW02ADD0B1, R/W, Address = 0xF800_00B4
- VIDW02ADD0B2, R/W, Address = 0xF800_20B0
- VIDW03ADD0B0, R/W, Address = 0xF800_00B8
- VIDW03ADD0B1, R/W, Address = 0xF800_00BC
- VIDW03ADD0B2, R/W, Address = 0xF800_20B8
- VIDW04ADD0B0, R/W, Address = 0xF800_00C0
- VIDW04ADD0B1, R/W, Address = 0xF800_00C4
- VIDW04ADD0B2, R/W, Address = 0xF800_20C0

VIDWxxADD0	Bit	Description	Initial State
VBASEU_F	[31:0]	Specifies A [31:0] of the start address for Video frame buffer.	0

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1.5.2.34 Frame Buffer Address 1 Register (VIDW)

- VIDW00ADD1B0, R/W, Address = 0xF800_00D0
- VIDW00ADD1B1, R/W, Address = 0xF800_00D4
- VIDW00ADD1B2, R/W, Address = 0xF800_20D0
- VIDW01ADD1B0, R/W, Address = 0xF800_0D8
- VIDW01ADD1B1, R/W, Address = 0xF800_00DC
- VIDW01ADD1B2, R/W, Address = 0xF800_20D8
- VIDW02ADD1B0, R/W, Address = 0xF800_00E0
- VIDW02ADD1B1, R/W, Address = 0xF800_00E4
- VIDW02ADD1B2, R/W, Address = 0xF800_20E0
- VIDW03ADD1B0, R/W, Address = 0xF800_00E8
- VIDW03ADD1B1, R/W, Address = 0xF800_00EC
- VIDW03ADD1B2, R/W, Address = 0xF800_20E8
- VIDW04ADD1B0, R/W, Address = 0xF800_00F0
- VIDW04ADD1B1, R/W, Address = 0xF800_00F4
- VIDW04ADD1B2, R/W, Address = 0xF800_20F0

VIDWxxADD1	Bit	Description	Initial State
VBASEL_F	[31:0]	Specifies A[31:0] of the end address for Video frame buffer. VBASEL = VBASEU + (PAGEWIDTH+OFFSIZE) x (LINEVAL+1)	0x0

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1.5.2.35 Rame Buffer Address 2 Register (VIDW)

- VIDW00ADD2, R/W, Address = 0xF800_0100
- VIDW01ADD2, R/W, Address = 0xF800_0104
- VIDW02ADD2, R/W, Address = 0xF800_0108
- VIDW03ADD2, R/W, Address = 0xF800_010C
- VIDW04ADD2, R/W, Address = 0xF800_0110

VIDWxxADD2	Bit	Description	Initial State
OFFSIZE_F	[25:13]	Specifies the Virtual screen offset size (number of byte). This value defines the difference between address of last byte displayed on the previous Video line and address of first byte to be displayed in the new Video line. OFFSIZE_F must have value that is multiple of 4-byte size or 0.	0
PAGEWIDTH_F	[12:0]	Specifies the Virtual screen page width (number of byte). This value defines the width of view port in the frame. PAGEWIDTH must have bigger value than the burst size and the size must be aligned word boundary.	0

NOTE: 'PAGEWIDTH + OFFSET' should be aligned double-word aligned (8-byte).

1.5.2.36 Video Interrupt Control 0 Register (VIDINTCON0, R/W, Address = 0xF800_0130)

VIDINTCON0	Bit	Description	Initial State
Reserved	[31:26]	Reserved	0
FIFOINTERVAL	[25:20]	Controls the interval of the FIFO interrupt.	0
SYSMAINCON	[19]	Sends complete interrupt enable bit to Main LCD 0 = Disables Interrupt 1 = Enables Interrupt Note: This bit is meaningful if both INTEN and I80IFDONE are high.	0
SYSSUBCON	[18]	Sends complete interrupt enable bit to Sub LCD 0 = Disables Interrupt. 1 = Enables Interrupt. Note: This bit is meaningful if both INTEN and I80IFDONE are high.	0
I80IFDONE	[17]	Enables the I80 Interface Interrupt (only for I80 Interface mode). 0 = Disables Interrupt. 1 = Enables Interrupt. Note: This bit is meaningful if INTEN is high.	0
FRAMESEL0	[16:15]	Specifies the Video Frame Interrupt 0 at start of: 00 = BACK Porch 01 = VSYNC 10 = ACTIVE	0

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VIDINTCON0	Bit	Description	Initial State
		11 = FRONT Porch	
FRAMESEL1	[14:13]	Specifies the Video Frame Interrupt 1 at start of: 00 = None 01 = BACK Porch 10 = VSYNC 11 = FRONT Porch	0
INTFRMEN	[12]	Specifies the Video Frame Interrupt Enable Control Bit. 0 = Disables Video Frame Interrupt 1 = Enables Video Frame Interrupt Note: This bit is meaningful when INTEN is high.	0
FIFOSEL	[11:5]	Specifies the FIFO Interrupt control bit. Each bit has a special significance: [11] Window 4 control (0 = disables, 1 = enables) [10] Window 3 control (0 = disables, 1 = enables) [9] Window 2 control (0 = disables, 1 = enables) [8] Reserved [7] Reserved [6] Window 1 control (0 = disables, 1 = enables) [5] Window 0 control (0 = disables, 1 = enables) Note: This bit is meaningful if both INTEN and INTFIFOEN are high	0
FIFOLEVEL	[4:2]	Selects the Video FIFO Interrupt Level. 000 = 0 ~ 25% 001 = 0 ~ 50% 010 = 0 ~ 75% 011 = 0% (empty) 100 = 100% (full)	0
INTFIFOEN	[1]	Specifies the Video FIFO Interrupt Enable Control Bit. 0 = Disables Video FIFO Level Interrupt 1 = Enables Video FIFO Level Interrupt Note: This bit is meaningful if INTEN is high.	0
INTEN	[0]	Specifies the Video Interrupt Enable Control Bit. 0 = Disables Video Interrupt 1 = Enables Video Interrupt	0

NOTE:

1. If video frame interrupt occurs, you can select maximum two points by setting FRAMESEL0 and FRAMESEL1. For example, in case of FRAMESEL0=00 and FRAMESEL1=11, video frame interrupt is triggered both at the start of back porch and front porch.
2. S5PV210 interrupt controller has three interrupt sources related to display controller, namely, LCD[0], LCD[1] and LCD[2]. (For more information, refer to Chapter 4.1, “Vectored Interrupt Controller”). LCD[0] specifies FIFO Level interrupt, LCD[1] specifies video frame sync interrupt and LCD[2] specifies i80 done interface interrupt.

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1.5.2.37 Video Interrupt Control 1 Register (VIDINTCON1, R/W, Address = 0xF800_0134)

VIDINTCON1	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
Reserved	[4:3]	Reserved (should be 0).	0
INTI80PEND	[2]	Specifies the i80 Done interrupt. Writes “1” to clear this bit. 0 = Interrupt has not been requested 1 = I80 Done status has asserted the interrupt request	0
INTFRMPEND	[1]	Specifies the Frame sync interrupt. Writes “1” to clear this bit. 0 = Interrupt has not been requested 1 = Frame sync status has asserted the interrupt request	0
INTFIFOPEND	[0]	Specifies the FIFO Level interrupt. Writes “1” to clear this bit. 0 = Interrupt has not been requested 1 = FIFO empty status has asserted the interrupt request	0

1.5.2.38 Win1 Color Key 0 Register (W1KEYCON0, R/W, Address = 0xF800_0140)

W1KEYCON0	Bit	Description	Initial State
KEYBLEN_F	[26]	Enables blending. 0 = Disables blending 1 = Enables blending using original Alpha for non-key area and KEY_ALPHA for key area	0
KEYEN_F	[25]	Enables/Disables Color Key (Chroma key). 0 = Disables color key 1 = Enables color key	0
DIRCON_F	[24]	Controls color key (Chroma key) direction. 0 = If the pixel value matches foreground image with COLVAL, the pixel from background image is displayed (only in OSD area) 1 = If the pixel value matches background image with COLVAL, the pixel from foreground image is displayed (only in OSD area)	0
COMPKEY_F	[23:0]	Each bit corresponds to COLVAL [23:0]. If some position bit is set, then it disables the position bit of COLVAL.	0

NOTE: Set BLD_PIX = 1, ALPHA_SEL =0, A_FUNC = 0x2, and B_FUNC = 0x3 to enable alpha blending using color key.

1.5.2.39 Win 1 Color key 1 Register (W1KEYCON1, R/W, Address = 0xF800_0144)

W1KEYCON1	Bit	Description	Initial State
COLVAL_F	[23:0]	Specifies the color key value for transparent pixel effect.	0

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1.5.2.40 Win2 Color Key 0 Register (W2KEYCON0, R/W, Address = 0xF800_0148)

W2KEYCON0	Bit	Description	Initial State
KEYBLEN_F	[26]	Enables blending. 0 = Disables blending 1 = Enables blending using original Alpha for non-key area and KEY_ALPHA for key area	0
KEYEN_F	[25]	Enables color key (Chroma key). 0 = Disables color key 1 = Enables color key	0
DIRCON_F	[24]	Controls color key (Chroma key) direction. 0 = If the pixel value matches foreground image with COLVAL, the pixel from background image is displayed (only in OSD area) 1 = If the pixel value matches background image with COLVAL, the pixel from foreground image is displayed (only in OSD area)	0
COMPKEY_F	[23:0]	Each bit corresponds to COLVAL [23:0]. If some position bit is set, then it disables the position bit of COLVAL.	0

NOTE: Set BLD_PIX = 1, ALPHA_SEL =0, A_FUNC = 0x2, and B_FUNC = 0x3 to enable alpha blending using color key.

1.5.2.41 Win2 Color key 1 Register (W2KEYCON1, R/W, Address = 0xF800_014C)

W2KEYCON1	Bit	Description	Initial State
COLVAL_F	[23:0]	Specifies the color key value for transparent pixel effect.	0

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1.5.2.42 Win3 Color Key 0 Register (W3KEYCON0, R/W, Address = 0xF800_0150)

W3KEYCON0	Bit	Description	Initial State
KEYBLEN_F	[26]	Enables blending. 0 = Disables blending 1 = Enables blending using original Alpha for non-key area and KEY_ALPHA for key area	0
KEYEN_F	[25]	Enables Color Key (Chroma key). 0 = Disables color key 1 = Enables color key	0
DIRCON_F	[24]	Controls Color key (Chroma key) direction. 0 = If the pixel value matches foreground image with COLVAL, the pixel from background image is displayed (only in OSD area) 1 = If the pixel value matches background image with COLVAL, the pixel from foreground image is displayed (only in OSD area)	0
COMPKEY_F	[23:0]	Each bit corresponds to COLVAL [23:0]. If some position bit is set, then it disables the position bit of COLVAL.	0

NOTE: Set BLD_PIX = 1, ALPHA_SEL =0, A_FUNC = 0x2, and B_FUNC = 0x3 to enable alpha blending using color key.

1.5.2.43 Win3 Color key 1 Register (W3KEYCON1, R/W, Address = 0xF800_0154)

W3KEYCON1	Bit	Description	Initial State
COLVAL_F	[23:0]	Specifies the color key value for transparent pixel effect.	0

1.5.2.44 Win4 Color Key 0 Register (W4KEYCON0, R/W, Address = 0xF800_0158)

W4KEYCON0	Bit	Description	Initial State
KEYBLEN_F	[26]	Enables blending. 0 = Disables blending 1 = Enables blending using original Alpha for non-key area and KEY_ALPHA for key area	0
KEYEN_F	[25]	Enables color Key (Chroma key). 0 = Disables color key 1 = Enables color key	0
DIRCON_F	[24]	Controls color key (Chroma key) direction. 0 = If the pixel value matches foreground image with COLVAL, the pixel from background image is displayed (only in OSD area) 1 = If the pixel value matches background image with COLVAL, the pixel from foreground image is displayed (only in OSD area)	0
COMPKEY_F	[23:0]	Each bit corresponds to COLVAL [23:0]. If some position bit is set, then it disables the COLVAL position bit.	0

NOTE: Set BLD_PIX = 1, ALPHA_SEL =0, A_FUNC = 0x2, and B_FUNC = 0x3 to enable alpha blending using color key.

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1.5.2.45 Win4 Color key 1 Register (W4KEYCON1, R/W, Address = (W4KEYCON1, R/W, Address = 0xF800_015C)

W4KEYCON1	Bit	Description	Initial State
COLVAL_F	[23:0]	Specifies the color key value for transparent pixel effect.	0

NOTE: Both COLVAL and COMPKEY use 24-bit color data in all BPP modes.

@ BPP24 mode: 24-bit color value is valid.

- A. COLVAL
  - Red: COLVAL [23:17]
  - Green: COLVAL [15: 8]
  - Blue: COLVAL [7:0]

- B. COMPKEY
  - Red: COMPKEY [23:17]
  - Green: COMPKEY [15: 8]
  - Blue: COMPKEY [7:0]

@ BPP16 (5:6:5) mode: 16-bit color value is valid.

- A. COLVAL
  - Red: COLVAL [23:19]
  - Green: COLVAL [15: 10]
  - Blue: COLVAL [7:3]

- B. COMPKEY
  - Red: COMPKEY [23:19]
  - Green: COMPKEY [15: 10]
  - Blue: COMPKEY [7:3]
  - COMPKEY [18:16] must be 0x7.
  - COMPKEY [9: 8] must be 0x3.
  - COMPKEY [2:0] must be 0x7.

NOTE: COMPKEY register must be set properly for each BPP mode.

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1.5.2.46 Win1 Color Key ALPHA Control Register (W1KEYALPHA, R/W, Address = 0xF800_0160)

W1KEYALPHA	Bit	Description	Initial State
-	[31:14]	Reserved.	0
KEYALPHA_R_F	[23:0]	Specifies the Key alpha R value.	0
KEYALPHA_G_F	[15:8]	Specifies the Key alpha G value.	0
KEYALPHA_B_F	[7:0]	Specifies the Key alpha B value.	0

1.5.2.47 Win2 Color Key ALPHA Control Register (W2KEYALPHA, R/W, Address = 0xF800_0164)

W2KEYALPHA	Bit	Description	Initial State
-	[31:14]	Reserved.	0
KEYALPHA_R_F	[23:0]	Specifies the Key alpha R value.	0
KEYALPHA_G_F	[15:8]	Specifies the Key alpha G value.	0
KEYALPHA_B_F	[7:0]	Specifies the Key alpha B value.	0

1.5.2.48 Win3 Color Key ALPHA Control Register (W3KEYALPHA, R/W, Address = 0xF800_0168)

W3KEYALPHA	Bit	Description	Initial State
-	[31:14]	Reserved.	0
KEYALPHA_R_F	[23:0]	Specifies the Key alpha R value.	0
KEYALPHA_G_F	[15:8]	Specifies the Key alpha G value.	0
KEYALPHA_B_F	[7:0]	Specifies the Key alpha B value.	0

1.5.2.49 Win4 Color Key ALPHA Control Register (W4KEYALPHA, R/W, Address = 0xF800_016C)

W4KEYALPHA	Bit	Description	Initial State
-	[31:14]	Reserved.	0
KEYALPHA_R_F	[23:0]	Specifies the Key alpha R value.	0
KEYALPHA_G_F	[15:8]	Specifies the Key alpha G value.	0
KEYALPHA_B_F	[7:0]	Specifies the Key alpha B value.	0

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1.5.2.50 Dithering Control 1 Register (DITHMODE, R/W, Address = 0xF800_0170)

DITHMODE	Bit	Description	Initial State
	[7]	Not used for normal access (Writing not-zero values to these registers results in abnormal behavior.)	0
RDithPos	[6:5]	Controls Red Dither bit. 00 = 8-bit 01 = 6-bit 10 = 5-bit	0
GDithPos	[4:3]	Controls Green Dither bit. 00 = 8-bit 01 = 6-bit 10 = 5-bit	0
BDithPos	[2:1]	Controls Blue Dither bit. 00 = 8-bit 01 = 6-bit 10 = 5-bit	0
DITHEN_F	[0]	Enables Dithering bit. 0 = Disables dithering 1 = Enables dithering	0

1.5.2.51 Win0 Color MAP (WIN0MAP, R/W, Address = 0xF800_0180)

WIN0MAP	Bit	Description	Initial State
MAPCOLEN_F	[24]	Specifies window's color mapping control bit. If this bit is enabled, then Video DMA stops and MAPCOLOR appears on background image instead of original image. 0 = Disables 1 = Enables	0
MAPCOLOR	[23:0]	Specifies the color value.	0

1.5.2.52 Win1 Color MAP (WIN1MAP, R/W, Address = 0xF800_0184)

WIN1MAP	Bit	Description	Initial State
MAPCOLEN_F	[24]	Specifies the window's color mapping control bit. If this bit is enabled, then Video DMA stops and MAPCOLOR appears on background image instead of original image. 0 = Disables 1 = Enables	0
MAPCOLOR	[23:0]	Specifies the color value.	0

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1.5.2.53 Win2 Color MAP (WIN2MAP, R/W, Address = 0xF800_0188)

WIN2MAP	Bit	Description	Initial State
MAPCOLEN_F	[24]	Specifies the window's color mapping control bit. If this bit is enabled, then Video DMA stops and MAPCOLOR appears on background image instead of original image. 0 = Disables 1 = Enables	0
MAPCOLOR	[23:0]	Specifies the color value.	0

1.5.2.54 Win3 Color MAP (WIN3MAP, R/W, Address = 0xF800_018C)

WIN3MAP	Bit	Description	Initial State
MAPCOLEN_F	[24]	Specifies the window's color mapping control bit. If this bit is enabled, then Video DMA stops and MAPCOLOR appears on background image instead of original image. 0 = Disables 1 = Enables	0
MAPCOLOR	[23:0]	Specifies the color value.	0

1.5.2.55 Win4 Color MAP (WIN4MAP, R/W, Address = 0xF800_0190)

WIN4MAP	Bit	Description	Initial State
MAPCOLEN_F	[24]	Specifies the window's color mapping control bit. If this bit is enabled, then Video DMA stops and MAPCOLOR appears on background image instead of original image. 0 = Disables 1 = Enables	0
MAPCOLOR	[23:0]	Specifies the color value.	0

1.5.2.56 Window Palette control Register (WPALCON_H, R/W, Address = 0xF800_019C)

WPALCON_H	Bit	Description	Initial State
Reserved	[31:19]	Reserved	0
W4PAL_H	[18:17]	W4PAL[2:1]	0
Reserved	[16:15]	Reserved	0
W3PAL_H	[14:13]	W3PAL[2:1]	0
Reserved	[12:11]	Reserved	0
W2PAL_H	[10: 9]	W2PAL[2:1]	0
Reserved	[8: 0]	Reserved	0

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1.5.2.57 Window Palette control Register (WPALCON_L, R/W, Address = 0xF800_01A0)

WPALCON_L	Bit	Description	Initial State
Reserved	[31:23]	Reserved	0
PALUPDATEEN	[9]	0 = Normal Mode 1 = Enable (Palette Update)	0
W4PAL_L	[8]	W4PAL[0]	0
W3PAL_L	[7]	W3PAL[0]	0
W2PAL_L	[6]	W2PAL[0]	0
W1PAL_L	[5: 3]	W1PAL[2:0]	0
W0PAL_L	[2: 0]	W0PAL[2:0]	0

NOTE: WPALCON = {WPALCON_H,WPALCON_L}

WPALCON	Description	Initial State
PALUPDATEEN	0 = Normal Mode 1 = Enable (Palette Update)	0
W4PAL[3:0]	Specifies the size of palette data format of Window 4. 000 = 16-bit (5:6:5) 001 = 16-bit (A:5:5:5) 010 = 18-bit (6:6:6) 011 = 18-bit (A:6:6:5) 100 = 19-bit (A:6:6:6) 101 = 24-bit (8:8:8) 110 = 25-bit (A:8:8:8) 111 = 32-bit (8:8:8:8) (A: 8-bit)	0
W3PAL[2:0]	Specifies the size of palette data format of Window 3. 000 = 16-bit (5:6:5) 001 = 16-bit (A:5:5:5) 010 = 18-bit (6:6:6) 011 = 18-bit (A:6:6:5) 100 = 19-bit (A:6:6:6) 101 = 24-bit (8:8:8) 110 = 25-bit (A:8:8:8) 111 = 32-bit (8:8:8:8) (A: 8-bit)	0
W2PAL[2:0]	Specifies the size of palette data format of Window 2. 000 = 16-bit (5:6:5) 001 = 16-bit (A:5:5:5) 010 = 18-bit (6:6:6) 011 = 18-bit (A:6:6:5) 100 = 19-bit (A:6:6:6) 101 = 24-bit (8:8:8) 110 = 25-bit (A:8:8:8) 111 = 32-bit (8:8:8:8) (A: 8-bit)	0

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WPALCON	Description	Initial State
W1PAL[2:0]	Specifies the size of palette data format of Window 1. 000 = 25-bit (A:8:8:8) 001 = 24-bit (8:8:8) 010 = 19-bit (A:6:6:6) 011 = 18-bit (A:6:6:5) 100 = 18-bit (6:6:6) 101 = 16-bit (A:5:5:5) 110 = 16-bit (5:6:5) 111 = 32-bit (8:8:8:8) (A: 8-bit)	0
W0PAL[2:0]	Specifies the size of palette data format of Window 0. 000 = 25-bit (A:8:8:8) 001 = 24-bit (8:8:8) 010 = 19-bit (A:6:6:6) 011 = 18-bit (A:6:6:5) 100 = 18-bit (6:6:6) 101 = 16-bit (A:5:5:5) 110 = 16-bit (5:6:5) 111 = 32-bit (8:8:8:8) (A: 8-bit)	0

NOTE: The bit map for W0/ W1 is different from W2/ W3/ W4.

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1.5.2.58 I80 / RGB Trigger Control Register (TRIGCON, R/W, Address = 0xF800_01A4)

TRIGCON	Bit	Description	Initial State
-	[31:27]	Reserved	0
SWTRGCMD_W4BUF	[26]	Specifies Window 4 double buffer trigger. 1 = Enables Software Trigger Command (write only) * Only when TRGMODE_W4BUF is '1'	0
TRGMODE_W4BUF	[25]	Specifies Window 4 double buffer trigger. 0 = Disables Trigger 1 = Enables Trigger	0
Reserved	[24:22]	Reserved	0
SWTRGCMD_W3BUF	[21]	Specifies Window 3 double buffer trigger. 1 = Enables Software Trigger Command (write only) * Only when TRGMODE_W3BUF is '1'	0
TRGMODE_W3BUF	[20]	Specifies Window 3 double buffer trigger. 0 = Disables Trigger 1 = Enables Trigger	0
Reserved	[19:17]	Reserved	0
SWTRGCMD_W2BUF	[16]	Specifies Window 2 double buffer trigger. 1 = Enables Software Trigger Command (write only) * Only when TRGMODE_W2BUF is '1'	0
TRGMODE_W2BUF	[15]	Specifies Window 2 double buffer trigger. 0 = Disables Trigger 1 = Enables Trigger	0
Reserved	[14:12]	Reserved	0
SWTRGCMD_W1BUF	[11]	Specifies Window 1 double buffer trigger. 1 = Enables Software Trigger Command (write only) * Only when TRGMODE_W1BUF is '1'	0
TRGMODE_W1BUF	[10]	Specifies Window 1 double buffer trigger. 0 = Disables Trigger 1 = Enables Trigger	0
Reserved	[9:7]	Reserved	0
SWTRGCMD_W0BUF	[6]	Specifies Window 0 double buffer trigger. 1 = Enables Software Trigger Command (write only) * Only when TRGMODE_W0BUF is '1'	0
TRGMODE_W0BUF	[5]	Specifies Window 0 double buffer trigger. 0 = Disables Trigger 1 = Enables Trigger	0
Reserved	[4:3]	Reserved	0

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TRIGCON	Bit	Description	Initial State
SWFRSTATUS_I80	[2]	Specifies Frame Done Status (read only; I80 start trigger) 0 = Not Requested 1 = Requested * Clear Condition: Read or New Frame Start * Only when TRGMODE is '1'	0
SWTRGCMD_I80	[1]	Enables I80 start trigger. 1 = Software Triggering Command (write only) * Only when TRGMODE is '1'	0
TRGMODE_I80	[0]	Enables I80 start trigger. 0 = Disables i80 Software Trigger 1 = Enables i80 Software Trigger	0

NOTE: Two continuous software trigger inputs generated in some video clocks (VCLK) are recognized as one.

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1.5.2.59 LCD I80 Interface Control 0 (I80IFCONAx)

- I80IFCONA0, R/W, Address = 0xF800_01B0
- I80IFCONA1, R/W, Address = 0xF800_01B4

I80IFCONAx	Bit	Description	Initial State
Reserved	[22:20]	Reserved	0
LCD_CS_SETUP	[19:16]	Specifies the numbers of clock cycles for the active period of address signal enable to chip select enable.	0
LCD_WR _SETUP	[15:12]	Specifies the numbers of clock cycles for the active period of CS signal enable to write signal enable.	0
LCD_WR_ACT	[11:8]	Specifies the numbers of clock cycles for the active period of chip select enable.	0
LCD_WR _HOLD	[7:4]	Specifies the numbers of clock cycles for the active period of chip select disable to write signal disable.	0
Reserved	[3]	Reserved	
RSPOL	[2]	Specifies the polarity of RS Signal 0 = Low 1 = High	0
Reserved	[1]	Reserved	0
I80IFEN	[0]	Controls the LCD I80 interface. 0 = Disables 1 = Enables	0

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1.5.2.60 LCD I80 Interface Control 1 (I80IFCONBx)

- I80IFCONB0, R/W, Address = 0xF800_01B8
- I80IFCONB1, R/W, Address = 0xF800_01BC

I80IFCONBx	Bit	Description	Initial State
Reserved	[11:10]	Reserved	0
NORMAL_CMD_ST	[9]	1 = Normal Command Start * Auto clears after sending out one set of commands	0
Reserved	[8:7]	Reserved	
FRAME_SKIP	[6:5]	Specifies the I80 Interface Output Frame Decimation Factor. 00 = 1 (No Skip) 01 = 2 10 = 3	00
Reserved	[4]	Reserved	0
AUTO_CMD_RATE	[3:0]	0000 = Disables auto command (If you don't use any auto-command, then you should set AUTO_CMD_RATE as "0000".) 0001 = per 2 Frames 0010 = per 4 Frames 0011 = per 6 Frames … 1111 = per 30 Frames	0000

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1.5.2.61 Color GAIN Control Register (COLORGAINCON, R/W, Address = 0xF800_01C0)

COLORGAINCON	Bit	Description	Initial State
Reserved	[31:30]	Reserved	0
CG_RGAIN	[29:20]	Specifies the color gain value of R data (maximum 4, 8-bit resolution). 0h000 = 0 0h001 = 0.00390625 (1/256) 0h002 = 0.0078125 (2/256) … 0h0FF = 0.99609375 (255/256) 0h100 = 1.0 … 0x3FF = 3.99609375 (max)	0x100
CG_GGAIN	[19:10]	Specifies the color gain value of G data (maximum 4, 8-bit resolution). 0h000 = 0 0h001 = 0.00390625 (1/256) 0h002 = 0.0078125 (2/256) … 0h0FF = 0.99609375 (255/256) 0h100 = 1.0 … 0x3FF = 3.99609375 (max)	0x100
CG_BGAIN	[9:0]	Specifies the color gain value of B data (maximum 4, 8-bit resolution). 0h000 = 0 0h001 = 0.00390625 (1/256) 0h002 = 0.0078125 (2/256) … 0h0FF = 0.99609375 (255/256) 0h100 = 1.0 … 0x3FF = 3.99609375 (max)	0x100

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1.5.2.62 LCD i80 Interface Command Control 0 (LDI_CMDCON0, R/W, Address = 0xF800_01D0)

LDI_CMDCON0	Bit	Description	Initial State
Reserved	[31:24]	Reserved	
CMD11_EN	[23:22]	00 = Disables 01 = Enables Normal Command 10 = Enables Auto Command 11 = Enables Normal and Auto Command	00
CMD10_EN	[21:20]	00 = Disables 01 = Enables Normal Command 10 = Enables Auto Command 11 = Enables Normal and Auto Command	00
CMD9_EN	[19:18]	00 = Disables 01 = Enables Normal Command 10 = Enables Auto Command 11 = Enables Normal and Auto Command	00
CMD8_EN	[17:16]	00 = Disables 01 = Enables Normal Command 10 = Enables Auto Command 11 = Enables Normal and Auto Command	00
CMD7_EN	[15:14]	00 = Disables 01 = Enables Normal Command 10 = Enables Auto Command 11 = Enables Normal and Auto Command	00
CMD6_EN	[13:12]	00 = Disables 01 = Enables Normal Command 10 = Enables Auto Command 11 = Enables Normal and Auto Command	00
CMD5_EN	[11:10]	00 = Disables 01 = Enables Normal Command 10 = Enables Auto Command 11 = Enables Normal and Auto Command	00
CMD4_EN	[9:8]	00 = Disables 01 = Enables Normal Command 10 = Enables Auto Command 11 = Enables Normal and Auto Command	00
CMD3_EN	[7:6]	00 = Disables 01 = Enables Normal Command 10 = Enables Auto Command 11 = Enables Normal and Auto Command	00
CMD2_EN	[5:4]	00 = Disables 01 = Enables Normal Command 10 = Enables Auto Command 11 = Normal and Auto Command Enable	00
CMD1_EN	[3:2]	00 = Disables 01 = Enables Normal Command 10 = Enables Auto Command 11 = Enables Normal and Auto Command	00

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LDI_CMDCON0	Bit	Description	Initial State
CMD0_EN	[1:0]	00 = Disables 01 = Enables Normal Command 10 = Enables Auto Command 11 = Enables Normal and Auto Command	00

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1.5.2.63 LCD i80 Interface Command Control 1 (LDI_CMDCON1, R/W, Address = 0xF800_01D4)

LDI_CMDCON1	Bit	Description	Initial State
Reserved	[31:10]	Reserved	0
CMD11_RS	[11]	Controls Command 11 RS	0
CMD10_RS	[10]	Controls Command 10 RS	0
CMD9_RS	[9]	Controls Command 9 RS	0
CMD8_RS	[8]	Controls Command 8 RS	0
CMD7_RS	[7]	Controls Command 7 RS	0
CMD6_RS	[6]	Controls Command 6 RS	0
CMD5_RS	[5]	Controls Command 5 RS	0
CMD4_RS	[4]	Controls Command 4 RS	0
CMD3_RS	[3]	Controls Command 3 RS	0
CMD2_RS	[2]	Controls Command 2 RS	0
CMD1_RS	[1]	Controls Command 1 RS	0
CMD0_RS	[0]	Controls Command 0 RS	0

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1.5.2.64 I80 System Interface Manual Command Control 0 (SIFCCON0, R/W, Address = 0xF800_01E0)

SIFCCON0	Bit	Description	Initial State
Reserved	[7]	Reserved (should be 0)	0
SYS_ST_CON	[6]	Controls LCD i80 System Interface ST Signal. 0 = Low 1 = High	0
SYS_RS_CON	[5]	Controls LCD i80 System Interface RS Signal. 0 = Low 1 = High	0
SYS_nCS0_CON	[4]	Controls LCD i80 System Interface nCS0 (main) Signal. 0 = Disables (High) 1 = Enables (Low)	0
SYS_nCS1_CON	[3]	Controls LCD i80 System Interface nCS1 (sub) Signal. 0 = Disables (High) 1 = Enables (Low)	0
SYS_nOE_CON	[2]	Controls LCD i80 System Interface nOE Signal. 0 = Disables (High) 1 = Enables (Low)	0
SYS_nWE_CON	[1]	Controls LCD i80 System Interface nWE Signal. 0 = Disables (High) 1 = Enables (Low)	0
SCOMEN	[0]	Enables LCD i80 System Interface Command Mode. 0 = Disables (Normal Mode) 1= Enables (Manual Command Mode)	

1.5.2.65 I80 System Interface Manual Command Control 1 (SIFCCON1, R/W, Address = 0xF800_01E4)

SIFCCON1	Bit	Description	Initial State
SYS_WDATA	[23:0]	Controls the LCD i80 System Interface Write Data.	0

1.5.2.66 I80 System Interface Manual Command Control 2 (SIFCCON2, R/W, Address = 0xF800_01E8)

SIFCCON2	Bit	Description	Initial State
SYS_RDATA	[23:0]	Controls the LCD i80 System Interface Read Data.	0

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1.5.2.67 Hue Control Registers (HUECOEF00, R/W, Address = 0xF800_0200)

- HUECOEF00, R/W, Address = 0xF800_01EC
- HUECOEF01, R/W, Address = 0xF800_01F0
- HUECOEF02, R/W, Address = 0xF800_01F4
- HUECOEF03, R/W, Address = 0xF800_01F8

HUECOEF0x	Bit	Description	Initial State
-	[31:26]	Reserved	0
CBGx_P	[25:16]	Specifies the Hue matrix coefficient 00 (when 'cb + In_offset' is positive). (Signed) 0h000 = 0 0h001 = 0.00390625 (1/256) 0h002 = 0.0078125 (2/256) … 0h0FF = 0.99609375 (255/256) 0h100 = 1.0 (256/256) 0h300 = -1.0 (-256/256) 0h301 = - 0.99609375 (-255/256) … 0h3FF = -0.00390625 (-1/256) 0h101 ~ 2FF = Reserved (don't use)	0x100
-	[15:10]	Reserved	0
CBGx_N	[9:0]	Specifies the Hue matrix coefficient 00 (when 'cb + In_offset' is negative). (Signed) 0h000 = 0 0h001 = 0.00390625 (1/256) 0h002 = 0.0078125 (2/256) … 0h0FF = 0.99609375 (255/256) 0h100 = 1.0 (256/256) 0h300 = -1.0 (-256/256) 0h301 = - 0.99609375 (-255/256) … 0h3FF = -0.00390625 (-1/256) 0h101 ~ 2FF = Reserved (don't use)	0x100

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1.5.2.68 Hue Offset Control Register (HUEOFFSET, R/W, Address = 0xF800_01fC)

HUEOFFSET	Bit	Description	Initial State
-	[31:25]	Reserved	0
OFFSET_IN	[24:16]	Specifies the Hue matrix input offset (signed). 0h000 = + 0 0h001 = + 1 0h002 = + 2 … 0h0FF = + 255 0h100 = - 256 … 0x1FF = - 1	0x180 (-128)
-	[15:9]	Reserved	0
OFFSET_OUT	[8:0]	Specifies the Hue matrix output offset (signed). 0h000 = + 0 0h001 = + 1 0h002 = + 2 … 0h0FF = + 255 0h100 = - 256 … 0x1FF = - 1	0x080 (+128)

NOTE: Generally, HUE_OFFSET_IN = -128 and HUE_OFFSET_OUT = +128

Hue Equation:

Cb<hue> = CBG0•(Cb + OFFSET_IN) + CBG1•(Cr + OFFSET_IN) + OFFSET_OUT
Cr<hue> = CRG0•(Cb + OFFSET_IN) + CRG1•(Cr + OFFSET_IN) + OFFSET_OUT

Coefficient Decision:

CBG0 = (Cb - 128)>=0 ? CBG0_P: CBG0_N
CBG1 = (Cr - 128)>=0 ? CBG1_P: CBG1_N
CRG0 = (Cb - 128)>=0 ? CRG0_P: CRG0_N
CRG0 = (Cr- 1 28)>=0 ? CRG1_P: CRG1_N

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1.5.2.69 Window 0 Alpha0 Control Register (VIDW0ALPHA0, R/W, Address = 0xF800_0200)

VIDW0ALPHA0	Bit	Description	Initial State
Reserved	[24]	Reserved	0
ALPHA0_R_F	[23:16]	Specifies the Red Alpha value (case AEN == 0).	0
ALPHA0_G_F	[15:8]	Specifies the Green Alpha value (case AEN == 0).	0
ALPHA0_B_F	[7:0]	Specifies the Blue Alpha value (case AEN == 0).	0

1.5.2.70 Window 0 Alpha1 control Register (VIDW0 ALPHA1, R/W, Address = 0xF800_0204)

VIDW0ALPHA1	Bit	Description	Initial State
Reserved	[24]	Reserved	0
ALPHA1_R_F	[23:16]	Specifies the Red Alpha value (case AEN == 1).	0
ALPHA1_G_F	[15:8]	Specifies the Green Alpha value (case AEN == 1).	0
ALPHA1_B_F	[7:0]	Specifies the Blue Alpha value (case AEN == 1).	0

1.5.2.71 Window 1 Alpha0 control Register (VIDW1ALPHA0, R/W, Address = 0xF800_0208)

VIDW1ALPHA0	Bit	Description	Initial State
Reserved	[24]	Reserved	0
Reserved	[23:20]	Reserved	0
ALPHA0_R_L_F	[19:16]	Specifies the Red Alpha lower value (case AEN == 0).	0
-	[15:12]	Reserved	0
ALPHA0_G_L_F	[11: 8]	Specifies the Green Alpha lower value (case AEN == 0).	0
-	[7: 4]	Reserved	0
ALPHA0_B_L_F	[3: 0]	Specifies the Blue Alpha lower value (case AEN == 0).	0

NOTE: ALPHA0_R (G, B) [7:4] = ALPHA0_R(G,B)_H[3:0]@VIDOSD1C
ALPHA0_R(G,B) [3:0] = ALPHA0_R(G,B)_L[3:0]@VIDW1ALPHA0

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1.5.2.72 Window 1 Alpha1 Control Register (VIDW0ALPHA1, R/W, Address = 0xF800_020C)

VIDW0ALPHA1	Bit	Description	Initial State
Reserved	[24]	Reserved	0
Reserved	[23:20]	Reserved	0
ALPHA1_R_L_F	[19:16]	Specifies the Red Alpha lower value (case AEN == 1).	0
-	[15:12]	Reserved	0
ALPHA1_G_L_F	[11: 8]	Specifies the Green Alpha lower value (case AEN == 1).	0
-	[7: 4]	Reserved	0
ALPHA1_B_L_F	[3: 0]	Specifies the Blue Alpha lower value (case AEN == 1).	0

NOTE: ALPHA1_R(G,B) [7:4] = ALPHA1_R(G,B)_H[3:0]@VIDOSD1C
ALPHA1_R(G,B) [3:0] = ALPHA1_R(G,B)_L[3:0]@VIDW1ALPHA1

1.5.2.73 Window 2 Alpha0 Control Register (VIDW0ALPHA0, R/W, Address = 0xF800_0210)

VIDW0ALPHA0	Bit	Description	Initial State
Reserved	[24]	Reserved	0
Reserved	[23:20]	Reserved	0
ALPHA0_R_L_F	[19:16]	Specifies the Red Alpha lower value (case AEN == 0).	0
-	[15:12]	Reserved	0
ALPHA0_G_L_F	[11: 8]	Specifies the Green Alpha lower value (case AEN == 0).	0
-	[7: 4]	Reserved	0
ALPHA0_B_L_F	[3: 0]	Specifies the Blue Alpha lower value (case AEN == 0).	0

NOTE: ALPHA0_R (G, B) [7:4] = ALPHA0_R (G, B)_H[3:0]@VIDOSD2C
ALPHA0_R (G, B) [3:0] = ALPHA0_R (G, B)_L[3:0]@VIDW2ALPHA0

1.5.2.74 Window 2 Alpha1 control Register (VIDW2ALPHA1, R/W, Address = 0xF800_0214)

VIDW2ALPHA1	Bit	Description	Initial State
Reserved	[24]	Reserved	0
Reserved	[23:20]	Reserved	0
ALPHA1_R_L_F	[19:16]	Specifies the Red Alpha lower value (case AEN == 1).	0
-	[15:12]	Reserved	0
ALPHA1_G_L_F	[11: 8]	Specifies the Green Alpha lower value (case AEN == 1).	0
-	[7: 4]	Reserved	0
ALPHA1_B_L_F	[3: 0]	Specifies the Blue Alpha lower value (case AEN == 1).	0

NOTE: ALPHA1_R (G, B) [7:4] = ALPHA1_R (G, B)_H[3:0]@VIDOSD2C
ALPHA1_R (G, B) [3:0] = ALPHA1_R (G, B)_L[3:0]@VIDW2ALPHA1

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1.5.2.75 Window 3 Alpha0 Control Register (VIDW0ALPHA0, R/W, Address = 0xF800_0218)

VIDW0ALPHA0	Bit	Description	Initial State
Reserved	[24]	Reserved	0
Reserved	[23:20]	Reserved	0
ALPHA0_R_L_F	[19:16]	Specifies the Red Alpha lower value (case AEN == 0).	0
-	[15:12]	Reserved	0
ALPHA0_G_L_F	[11: 8]	Specifies the Green Alpha lower value (case AEN == 0).	0
-	[7: 4]	Reserved	0
ALPHA0_B_L_F	[3: 0]	Specifies the Blue Alpha lower value (case AEN == 0).	0

NOTE: ALPHA0_R(G,B) [7:4] = ALPHA0_R(G,B)_H[3:0]@VIDOSD3C
ALPHA0_R(G,B) [3:0] = ALPHA0_R(G,B)_L[3:0]@VIDW3ALPHA0

1.5.2.76 Window 3 Alpha1 Control Register (VIDW3ALPHA1, R/W, Address = 0xF800_021C)

VIDW3ALPHA1	Bit	Description	Initial State
Reserved	[24]	Reserved	0
Reserved	[23:16]	Reserved	0
ALPHA1_R_L_F	[19:16]	Specifies the Red Alpha lower value (case AEN == 1).	0
-	[15:12]	Reserved	0
ALPHA1_G_L_F	[11: 8]	Specifies the Green Alpha lower value (case AEN == 1).	0
-	[7: 4]	Reserved	0
ALPHA1_B_L_F	[3: 0]	Specifies the Blue Alpha lower value (case AEN == 1).	0

NOTE: ALPHA1_R(G,B) [7:4] = ALPHA1_R(G,B)_H[3:0]@VIDOSD3C
ALPHA1_R(G,B) [3:0] = ALPHA1_R(G,B)_L[3:0]@VIDW3ALPHA1

1.5.2.77 Window 4 Alpha0 Control Register (VIDW4 ALPHA0, R/W, Address = 0xF800_0220)

VIDW4ALPHA0	Bit	Description	Initial State
Reserved	[24]	Reserved	0
Reserved	[23:20]	Reserved	0
ALPHA0_R_L_F	[19:16]	Specifies the Red Alpha lower value (case AEN == 0).	0
-	[15:12]	Reserved	0
ALPHA0_G_L_F	[11: 8]	Specifies the Green Alpha lower value (case AEN == 0).	0
-	[7: 4]	Reserved	0
ALPHA0_B_L_F	[3: 0]	Specifies the Blue Alpha lower value (case AEN == 0).	0

NOTE: ALPHA0_R(G,B) [7:4] = ALPHA0_R(G,B)_H[3:0]@VIDOSD4C
ALPHA0_R(G,B) [3:0] = ALPHA0_R(G,B)_L[3:0]@VIDW4ALPHA0

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1.5.2.78 Window 4 Alpha1 Control Register (VIDW0ALPHA1, R/W, Address = 0xF800_0224)

VIDW0ALPHA1	Bit	Description	Initial State
Reserved	[24]	Reserved	0
Reserved	[23:20]	Reserved	0
ALPHA1_R_L_F	[19:16]	Specifies the Red Alpha lower value (case AEN == 1).	0
-	[15:12]	Reserved	0
ALPHA1_G_L_F	[11: 8]	Specifies the Green Alpha lower value (case AEN == 1).	0
-	[7: 4]	Reserved	0
ALPHA1_B_L_F	[3: 0]	Specifies the Blue Alpha lower value (case AEN == 1).	0

NOTE: ALPHA1_R(G,B) [7:4] = ALPHA1_R(G,B)_H[3:0]@VIDOSD4C
ALPHA1_R(G,B) [3:0] = ALPHA1_R(G,B)_L[3:0]@VIDW4ALPHA1

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1.5.2.79 Window 1 Blending Equation Control Register (BLENDEQ1, R/W, Address = 0xF800_0244)

BLENDEQ1	Bit	Description	Initial State
Reserved	[31:22]	Reserved	0x000
Q_FUNC_F	[21:18]	Specifies the constant used in alphaB (alpha value of *background) 0000 = 0 (zero) 0001 = 1 (maximum) 0010 = **alphaA (alpha value of *foreground) 0011 = 1 - alphaA 0100 = alphaB 0101 = 1 - alphaB 0110 = ALPHA0 0111 = Reserved 100x = Reserved 1010 = A (foreground color data) 1011 = 1 - A 1100 = B (background color data) 1101 = 1 - B 111x = Reserved	0x0
-	[17:16]	Reserved	00
P_FUNC_F	[15:12]	Specifies the constant used in alpha. Same as above (see COEF_Q).	0x0
-	[11:10]	Reserved	00
B_FUNC_F	[9:6]	Specifies the constant used in B. Same as above (see COEF_Q).	0x3
-	[5:4]	Reserved	00
A_FUNC_F	[3:0]	Specifies the constant used in A. Same as above (see COEF_Q).	0x2

NOTE: For more information, refer to Figure 1-5, “Blending equation”.
background = Window 0, foreground = Window 1 (in Blend Equation 1)
alphaA and alphaB are decided by BPPMODE_F, BLD_PIX, ALPHA_SEL @WINCONx, and WxPAL @WPALCON.

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1.5.2.80 Window 2 Blending Equation Control Register (BLENDEQ2, R/W, Address = 0xF800_0248)

BLENDEQ2	Bit	Description	Initial State
Reserved	[31:22]	Reserved	0x000
Q_FUNC_F	[21:18]	Specifies the constant used in alphaB (alpha value of *background). 0000 = 0 (zero) 0001 = 1 (maximum) 0010 = **alphaA (alpha value of *foreground) 0011 = 1 – alphaA 0100 = alphaB 0101 = 1 – alphaB 0110 = ALPHA0 0111 = Reserved 100x = Reserved 1010 = A (foreground color data) 1011 = 1 – A 1100 = B (background color data) 1101 = 1 – B 111x = Reserved	0x0
-	[17:16]	Reserved	00
P_FUNC_F	[15:12]	Specifies the constant used in alpha. Same as above (see COEF_Q)	0x0
-	[11:10]	Reserved	00
B_FUNC_F	[9:6]	Specifies the constant used in B. Same as above (see COEF_Q)	0x3
-	[5:4]	Reserved	00
A_FUNC_F	[3:0]	Specifies the constant used in A. Same as above (see COEF_Q)	0x2

NOTE: For more information, refer to Figure 1-5, “Blending equation”.
background = Window 01, foreground = Window 2 (in Blend Equation 2)
alphaA and alphaB are decided by BPPMODE_F, BLD_PIX, ALPHA_SEL @WINCONx, and WxPAL @WPALCON.

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1.5.2.81 Window 3 Blending Equation Control Register (BLENDEQ3, R/W, Address = 0xF800_024C)

BLENDEQ3	Bit	Description	Initial State
Reserved	[31:22]	Reserved	0x000
Q_FUNC_F	[21:18]	Specifies the constant used in alphaB (alpha value of *background) 0000 = 0 (zero) 0001 = 1 (maximum) 0010 = **alphaA (alpha value of *foreground) 0011 = 1 – alphaA 0100 = alphaB 0101 = 1 – alphaB 0110 = ALPHA0 0111 = Reserved 100x = Reserved 1010 = A (foreground color data) 1011 = 1 – A 1100 = B (background color data) 1101 = 1 – B 111x = Reserved	0x0
-	[17:16]	Reserved	00
P_FUNC_F	[15:12]	Specifies the constant used in alpha. Same as above (see COEF_Q).	0x0
-	[11:10]	Reserved	00
B_FUNC_F	[9:6]	Specifies the constant used in B. Same as above (see COEF_Q).	0x3
-	[5:4]	Reserved	00
A_FUNC_F	[3:0]	Specifies the constant used in A. Same as above (see COEF_Q).	0x2

NOTE: For more information, refer to Figure 1-5, “Blending equation”.
background = Window 012, foreground = Window 3 (in Blend Equation 3)
alphaA and alphaB are decided by BPPMODE_F, BLD_PIX, ALPHA_SEL @WINCONx, and WxPAL @WPALCON.

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1.5.2.82 Window 4 Blending Equation Control Register (BLENDEQ4, R/W, Address = 0xF800_0250)

BLENDEQ4	Bit	Description	Initial State
Reserved	[31:22]	Reserved	0x000
Q_FUNC_F	[21:18]	Specifies the constant used in alphaB (alpha value of *background) 0000 = 0 (zero) 0001 = 1 (maximum) 0010 = **alphaA (alpha value of *foreground) 0011 = 1 – alphaA 0100 = alphaB 0101 = 1 – alphaB 0110 = ALPHA0 0111 = Reserved 100x = Reserved 1010 = A (foreground color data) 1011 = 1 – A 1100 = B (background color data) 1101 = 1 – B 111x = Reserved	0x0
-	[17:16]	Reserved	00
P_FUNC_F	[15:12]	Specifies the constant used in alpha. Same as above (see COEF_Q).	0x0
-	[11:10]	Reserved	00
B_FUNC_F	[9:6]	Specifies the constant used in B. Same as above (see COEF_Q).	0x3
-	[5:4]	Reserved	00
A_FUNC_F	[3:0]	Specifies the constant used in A. Same as above (see COEF_Q).	0x2

NOTE: For more information, refer to Figure 1-5, “Blending equation”.
background = Window 0123, foreground = Window 4 (in Blend Equation 4)
alphaA and alphaB are decided by BPPMODE_F, BLD_PIX, ALPHA_SEL @WINCONx, and WxPAL @WPALCON.

1.5.2.83 Blending Equation Control Register (BLENDCON, R/W, Address = 0xF800_0260)

BLENDCON	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0x000
BLEND_NEW	[0]	Specifies the Alpha value width. 0 = 4-bit alpha value 1 = 8-bit alpha value	0x0

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1.5.2.84 Window RTQOS Control Registers

- W0RTQOSCON, R/W, Address = 0xF800_0264
- W1RTQOSCON, R/W, Address = 0xF800_0268
- W2RTQOSCON, R/W, Address = 0xF800_026C
- W3RTQOSCON, R/W, Address = 0xF800_0270
- W4RTQOSCON, R/W, Address = 0xF800_0274

HUECOEF0x	Bit	Description	Initial State
-	[31:12]	Reserved (should be 0)	0
FIFOLEVEL	[11:4]	Specifies the real-time QoS FIFO level. If FIFO depth is less than FIFOLEVEL[7:0], then RTQoS output is 1.	0
-	[3:2]	Reserved (should be 0)	0
QOS_GATE_DIS	[1]	Disables the RTQoS output signal gate. 0 = Gated 1 = Not gated	0
-	[0]	Reserved (should be 0).	0

1.5.2.85 Write-Back Control Registers

WRITEBACK	Bit	Description	Initial State
WRITEBACK_EN	[31]	Write-Back enable. 0 : disable 1 : enable	0

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1.5.2.86 LCD I80 Interface Command (I80IFCONx)

- LDI_CMD0, R/W, Address = 0xF800_0280
- LDI_CMD1, R/W, Address = 0xF800_0284
- LDI_CMD2, R/W, Address = 0xF800_0288
- LDI_CMD3, R/W, Address = 0xF800_028C
- LDI_CMD4, R/W, Address = 0xF800_0290
- LDI_CMD5, R/W, Address = 0xF800_0294
- LDI_CMD6, R/W, Address = 0xF800_0298
- LDI_CMD7, R/W, Address = 0xF800_029C
- LDI_CMD8, R/W, Address = 0xF800_02A0
- LDI_CMD9, R/W, Address = 0xF800_02A4
- LDI_CMD10, R/W, Address = 0xF800_02A8
- LDI_CMD11, R/W, Address = 0xF800_02AC

I80IFCONx	Bit	Description	Initial State
LDI_CMD	[23:0]	Specifies the LDI command.	0

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1.5.2.87 Win0 Palette Ram Access Address (not SFR)

Register	Address	R/W	Description	Initial State
00	0xF800_2400 (0xF800_0400)	R/W	Specifies the Window 0 Palette entry 0 address.	undefined
01	0xF800_2404 (0xF800_0404)	R/W	Specifies the Window 0 Palette entry 1 address.	undefined
-	-	-	-	-
FF	0xF800_27FC (0xF800_07FC)	R/W	Specifies the Window 0 Palette entry 255 address.	undefined

1.5.2.88 Win1 Palette Ram Access Address (not SFR)

Register	Address	R/W	Description	Initial State
00	0xF800_2800 (0xF800_0800)	R/W	Specifies the Window 1 Palette entry 0 address.	undefined
01	0xF800_2804 (0xF800_0804)	R/W	Specifies the Window 1 Palette entry 1 address.	undefined
-	-	-	-	-
FF	0xF800_2BFC (0xF800_0BFC)	R/W	Specifies the Window 1 Palette entry 255 address.	undefined

1.5.2.89 Win2 Palette Ram Access Address (not SFR)

Register	Address	R/W	Description	Initial State
00	0xF800_2C00	R/W	Specifies the Window 2 Palette entry 0 address.	undefined
01	0xF800_2C04	R/W	Specifies the Window 2 Palette entry 1 address.	undefined
-	-	-	-	-
FF	0xF800_2FFC	R/W	Specifies the Window 2 Palette entry 255 address.	undefined

1.5.2.90 Win3 Palette Ram Access Address (not SFR)

Register	Address	R/W	Description	Initial State
00	0xF800_3000	R/W	Specifies the Window 3 Palette entry 0 address.	undefined
01	0xF800_3004	R/W	Specifies the Window 3 Palette entry 1 address.	undefined
-	-	-	-	-
FF	0xF800_33FC	R/W	Specifies the Window 3 Palette entry 255 address.	undefined

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1.5.2.91 Win4 Palette Ram Access Address (not SFR)

Register	Address	R/W	Description	Reset Value
00	0xF800_3400	R/W	Specifies the Window 4 Palette entry 0 address.	undefined
01	0xF800_3404	R/W	Specifies the Window 4 Palette entry 1 address.	undefined
-	-	-	-	-
FF	0xF800_37FC	R/W	Specifies the Window 4 Palette entry 255 address.	undefined

1.5.2.92 Window RTQOS Control Registers

- W0RTQOSCON, R/W, Address = 0xF800_0264
- W1RTQOSCON, R/W, Address = 0xF800_0268
- W2RTQOSCON, R/W, Address = 0xF800_026C
- W3RTQOSCON, R/W, Address = 0xF800_0270
- W4RTQOSCON, R/W, Address = 0xF800_0274

HUECOEF0x	Bit	Description	Initial State
-	[31:12]	Reserved (should be 0).	0
FIFOLEVEL	[11:4]	Specifies the real-time QoS FIFO level. If FIFO depth is less than FIFOLEVEL[7:0], the RTQoS output is 1.	0
-	[3:2]	Reserved (should be 0).	0
QOS_GATE_DIS	[1]	Disables the RTQoS output signal gate. 0 = Gated 1 = Not gated	0
-	[0]	Reserved (should be 0).	0

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1.5.3 GAMMA LUT DATA

Register	Address	R/W	Description	Reset Value
GAMMALUT_1_0	0X0037C	R/W	Specifies the Gamma LUT data of the index 0, 1.	0X0010_0000
GAMMALUT_3_2	0X00380	R/W	Specifies the Gamma LUT data of the index 2, 3.	0X0030_0020
GAMMALUT_5_4	0X00384	R/W	Specifies the Gamma LUT data of the index 4, 5.	0X0050_0040
GAMMALUT_7_6	0X00388	R/W	Specifies the Gamma LUT data of the index 6, 7.	0X0070_0060
GAMMALUT_9_8	0X0038C	R/W	Specifies the Gamma LUT data of the index 8, 9.	0X0090_0080
GAMMALUT_11_10	0X00390	R/W	Specifies the Gamma LUT data of the index 10, 11.	0X00B0_00A0
GAMMALUT_13_12	0X00394	R/W	Specifies the Gamma LUT data of the index 12, 13.	0X00D0_00C0
GAMMALUT_15_14	0X00398	R/W	Specifies the Gamma LUT data of the index 14, 15.	0X00F0_00E0
GAMMALUT_17_16	0X0039C	R/W	Specifies the Gamma LUT data of the index 16, 17.	0X0110_0100
GAMMALUT_19_18	0X003A0	R/W	Specifies the Gamma LUT data of the index 18, 19.	0X0130_0120
GAMMALUT_21_20	0X003A4	R/W	Specifies the Gamma LUT data of the index 20, 21.	0X0150_0140
GAMMALUT_23_22	0X003A8	R/W	Specifies the Gamma LUT data of the index 22, 23.	0X0170_0160
GAMMALUT_25_24	0X003AC	R/W	Specifies the Gamma LUT data of the index 24, 25.	0X0190_0180
GAMMALUT_27_26	0X003B0	R/W	Specifies the Gamma LUT data of the index 26, 27.	0X01B0_01A0
GAMMALUT_29_28	0X003B4	R/W	Specifies the Gamma LUT data of the index 28, 29.	0X01D0_01C0
GAMMALUT_31_30	0X003B8	R/W	Specifies the Gamma LUT data of the index 30, 31.	0X01F0_01E0
GAMMALUT_33_32	0X003BC	R/W	Specifies the Gamma LUT data of the index 32, 33.	0X0210_0200
GAMMALUT_35_34	0X003C0	R/W	Specifies the Gamma LUT data of the index 34, 35.	0X0230_0220
GAMMALUT_37_36	0X003C4	R/W	Specifies the Gamma LUT data of the index 36, 37.	0X0250_0240
GAMMALUT_39_38	0X003C8	R/W	Specifies the Gamma LUT data of the index 38, 39.	0X0270_0260
GAMMALUT_41_40	0X003CC	R/W	Specifies the Gamma LUT data of the index 40, 41.	0X0290_0280
GAMMALUT_43_42	0X003D0	R/W	Specifies the Gamma LUT data of the index 42, 43.	0X02B0_02A0
GAMMALUT_45_44	0X003D4	R/W	Specifies the Gamma LUT data of the index 44, 45.	0X02D0_02C0
GAMMALUT_47_46	0X003D8	R/W	Specifies the Gamma LUT data of the index 46, 47.	0X02F0_02E0
GAMMALUT_49_48	0X003DC	R/W	Specifies the Gamma LUT data of the index 48, 49.	0X0310_0300
GAMMALUT_51_50	0X003E0	R/W	Specifies the Gamma LUT data of the index 50, 51.	0X0330_0320
GAMMALUT_53_52	0X003E4	R/W	Specifies the Gamma LUT data of the index 52, 53.	0X0350_0340
GAMMALUT_55_54	0X003E8	R/W	Specifies the Gamma LUT data of the index 54, 55.	0X0370_0360
GAMMALUT_57_56	0X003EC	R/W	Specifies the Gamma LUT data of the index 56, 57.	0X0390_0380
GAMMALUT_59_58	0X003F0	R/W	Specifies the Gamma LUT data of the index 58, 59.	0X03B0_03A0
GAMMALUT_61_60	0X003F4	R/W	Specifies the Gamma LUT data of the index 60, 61.	0X03D0_03C0
GAMMALUT_63_62	0X003F8	R/W	Specifies the Gamma LUT data of the index 62, 63.	0X03F0_03E0
GAMMALUT_xx_64	0X003FC	R/W	Specifies the Gamma LUT data of the index 64.	0X0000_0400

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GAMMALUT_x_y	Bit	Description	Initial State
GM_LUT_x	[26:18]	Specifies the Gamma LUT value register of index x.	
GM_LUT_y	[10: 2]	Specifies the Gamma LUT value register of index y.	

1.5.3.1 Frame Buffer Address 0 Shadow Registers

- SHD_VIDW00ADD0, R/W, Address = 0xF800_40A0
- SHD_VIDW01ADD0, R/W, Address = 0xF800_40A8
- SHD_VIDW02ADD0, R/W, Address = 0xF800_40B0
- SHD_VIDW03ADD0, R/W, Address = 0xF800_40B8
- SHD_VIDW04ADD0, R/W, Address = 0xF800_40C0

SHD_VIDWxxADD0	Bit	Description	Initial State
VBANK_F	[31:24]	Specifies A[31:24] of the bank location for video buffer in the system memory (Shadow).	0
VBASEU_F	[23:0]	Specifies A[23:0] of the start address for video frame buffer (Shadow).	0

1.5.3.2 Frame Buffer Address 1 Shadow Registers

- SHD_VIDW00ADD1, R/W, Address = 0xF800_40D0
- SHD_VIDW01ADD1, R/W, Address = 0xF800_40D8
- SHD_VIDW02ADD1, R/W, Address = 0xF800_40D0
- SHD_VIDW03ADD1, R/W, Address = 0xF800_40D8
- SHD_VIDW04ADD1, R/W, Address = 0xF800_40D0

SHD_VIDWxxADD1	Bit	Description	Initial State
VBASEL_F	[23:0]	Specifies A[23:0] of the end address for video buffer (Shadow).	0x0

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1.5.3.3 Frame Buffer Address 2 Shadow Registers

- SHD_VIDW00ADD2, R/W, Address = 0xF800_40A0
- SHD_VIDW01ADD2, R/W, Address = 0xF800_40A8
- SHD_VIDW02ADD2, R/W, Address = 0xF800_40B0
- SHD_VIDW03ADD2, R/W, Address = 0xF800_40B8
- SHD_VIDW04ADD2, R/W, Address = 0xF800_40C0

SHD_VIDWxxADD2	Bit	Description	Initial State
OFFSIZE_F	[25:13]	Specifies the Virtual screen offset size that is the number of byte (Shadow).	0
PAGEWIDTH_F	[12:0]	Specifies the Virtual screen page width (number of byte). This value defines the width of view port in the frame (Shadow).	0

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2 CAMERA INTERFACE

2.1 OVERVIEW OF CAMERA INTERFACE

The camera interface (CAMIF) in S5PV210 is a fully interactive mobile camera interface. CAMIF supports ITU R BT-601/656 standard, AXI interface and MIPI (CSI). The maximum input image size of CAMIF is 8192 x 8192 pixels.

S5PV210 has three CAMIF units, namely, CAMIF0, CAMIF1 and CAMIF2, as shown in *Figure 2-1*.

Each of these units is designed to perform different functions, as shown in *Figure 2-2.*

- T_PatternMux generates test pattern to calibrate input sync signals as HREF and VSYNC.
- Capture specifies the capturing signal and window cut. Use the register settings to invert video sync signals and pixel clock polarity in CAMIF.
- Scaler generates various sizes for an image.
- Input DMA (read only) reads from the memory image data.
- Output DMA (write only) writes image data to memory.
- CAMIF supports image rotation (90 degrees clockwise) and image effect functions.

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The key application of these features is in a folder-type cellular phone.

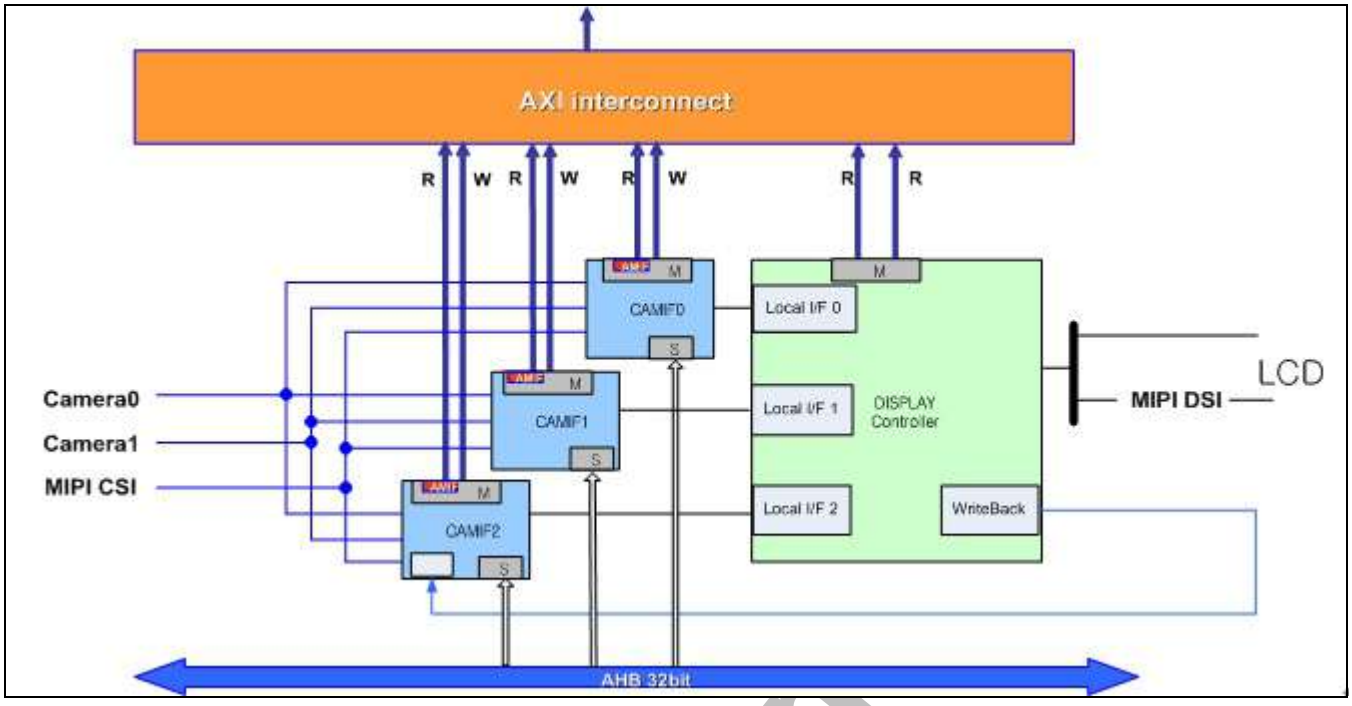

Figure 2-1 Subset of Visual System in S5PV210

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2.2 KEY FEATURES OF CAMIF

The key features of CAMIF include:

- Multiple input support
  - ITU-R BT 601/ 656/ 709 mode
  - DMA (AXI 64-bit interface) mode
  - MIPI (CSI) mode
  - Direct FIFO (PlayBack) mode
- Multiple output support
  - DMA (AXI 64-bit interface) mode
  - Direct FIFO mode
- Digital Zoom In (DZI) capability
- Multiple camera input
- Programmable polarity of video sync signals
- Supports maximum 8192 x 8192 pixels input (Refer to *Table 2-1*)
- Image mirror and rotation (X-axis mirror, Y-axis mirror, 90°, 180°, and 270° rotation)
- Generates various image formats
- Supports capture frame control
- Supports image effect

Table 2-1 Maximum Size

	Item	Maximum Size		
		CAMIF0	CAMIF1	CAMIF2
Scaler	Scaler input Hsize (=PreDstWidth)	4224 pixels	4224 pixels	1920 pixels
	Scaler bypass mode	8192 pixels	8192 pixels	8192 pixels
Output Rotator	TargetHsize (without output rotation)	4224 pixels	4224 pixels	1920 pixels
	TargetHsize (with output rotation)	1920 pixels	1920 pixels	1280 pixels
Input Rotator	REAL_WIDTH (without input rotation)	8192 pixels	8192 pixels	8192 pixels
	REAL_HEIGHT (with input rotation)	1920 pixels	1920 pixels	1280 pixels

NOTE: The maximum size of Scaler and Rotator depends on the line buffer size.
The maximum size of the Output Rotator and Input Rotator is less than the maximum size of Scaler.

Note: Minimum input size : 32 x 32

Note: Minimum output size : 32 x 32 (normal) , 128 x 128 (output rotation and interlace out are enable)

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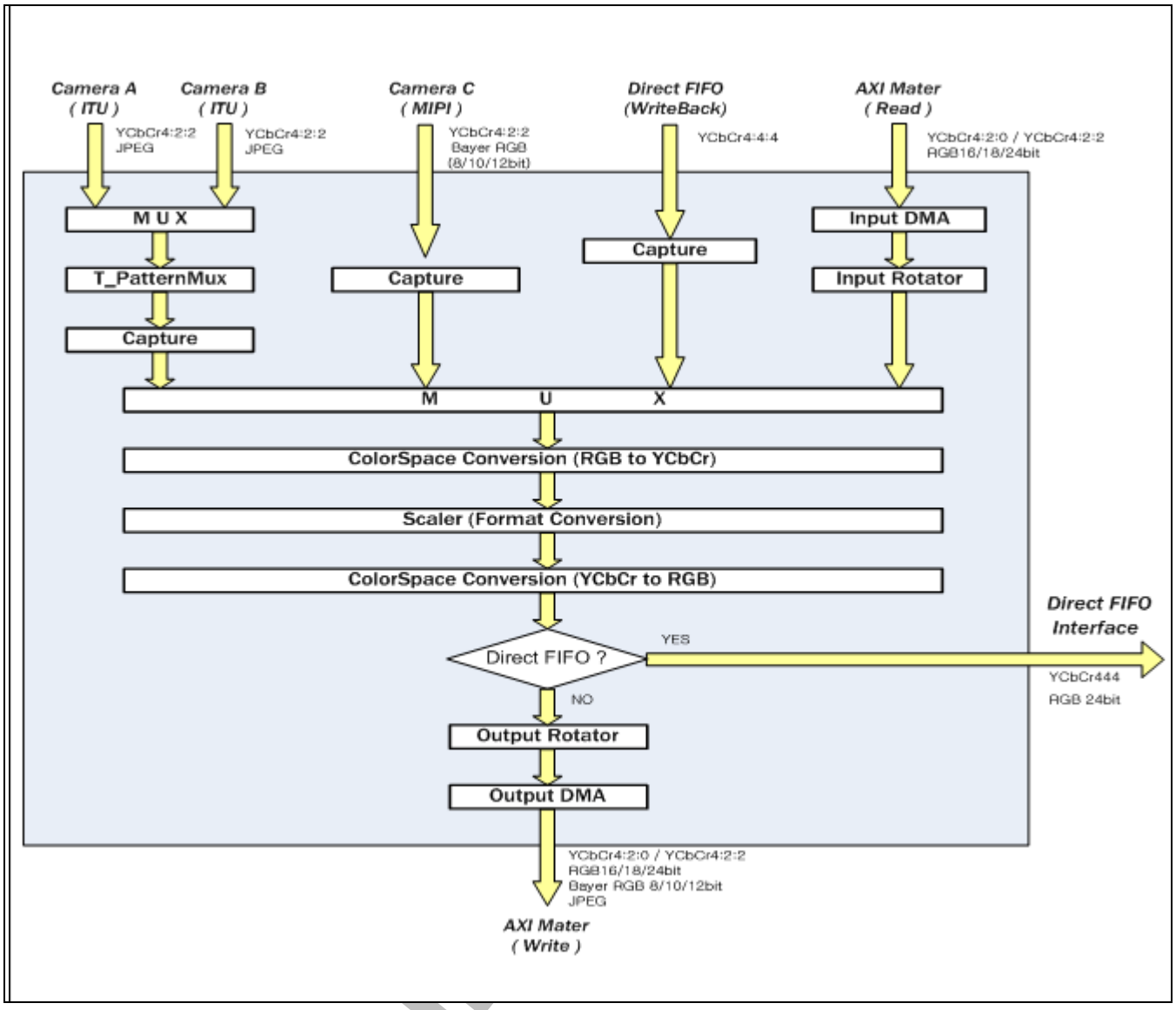

Figure 2-2 Camera Interface Overview

NOTE: In case of Direct FIFO (WriteBack) input mode, CAMIF does not support cropping, capture frame control, test pattern, and scaler bypass function.

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2.3 EXTERNAL INTERFACE

CAMIF supports three video standards, namely:

- ITU-R BT 601 YCbCr 8-bit mode
- ITU-R BT 656 YCbCr 8-bit mode
- MIPI mode

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2.4 INPUT/ OUTPUT DESCRIPTION

Table 2-2 ITU Camera Interface Signal Description

Signal	I/O	Description	PAD	Type
External ITU Camera Processor A Interface Signal				
PCLK_A	I	Specifies the Pixel Clock driven by external Camera processor A.	XciPCLK	Muxed
VSYNC_A	I	Specifies the Frame Sync driven by external Camera processor A.	XciVSYNC	Muxed
HREF_A	I	Specifies the Horizontal Sync driven by external Camera processor A.	XciHREF	Muxed
DATA _A[7:0]	I	Specifies the Pixel Data driven by external Camera processor A.	XciDATA [7:0]	Muxed
FIELD_A	I	Specifies the Field signal driven by external Camera processor A.	XciFIELD	Muxed
CAM_MCLK_A	O	Specifies the Clock for external Camera processor A.	XciCLKenb	Muxed
External ITU Camera Processor B Interface Signal				
PCLK_B	I	Specifies the Pixel Clock driven by external Camera processor B.	XmsmADDR[8]	Muxed
VSYNC_B	I	Specifies the Frame Sync driven by external Camera processor B.	XmsmADDR[9]	Muxed
HREF_B	I	Specifies the Horizontal Sync driven by external Camera processor B.	XmsmADDR[10]	Muxed
DATA_B[7:0]	I	Specifies the Pixel Data driven by external Camera processor B.	XmsmADDR[7:0]	Muxed
FIELD_B	I	Specifies the Field signal driven by external Camera processor B.	XmsmADDR[11]	Muxed
CAM_MCLK_B	O	Specifies the Clock for external Camera processor B.	XmsmADDR[12]	Muxed

NOTE: I/O direction. I: input, O: output, and B: bi-direction.
Type field indicates whether pads are dedicated to the signal or pads are connected to the multiplexed signals.

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2.5 TIMING DIAGRAM AND DATA ALIGNMENT OF CAMERA

2.5.1 TIMING DIAGRAM OF ITU CAMERA

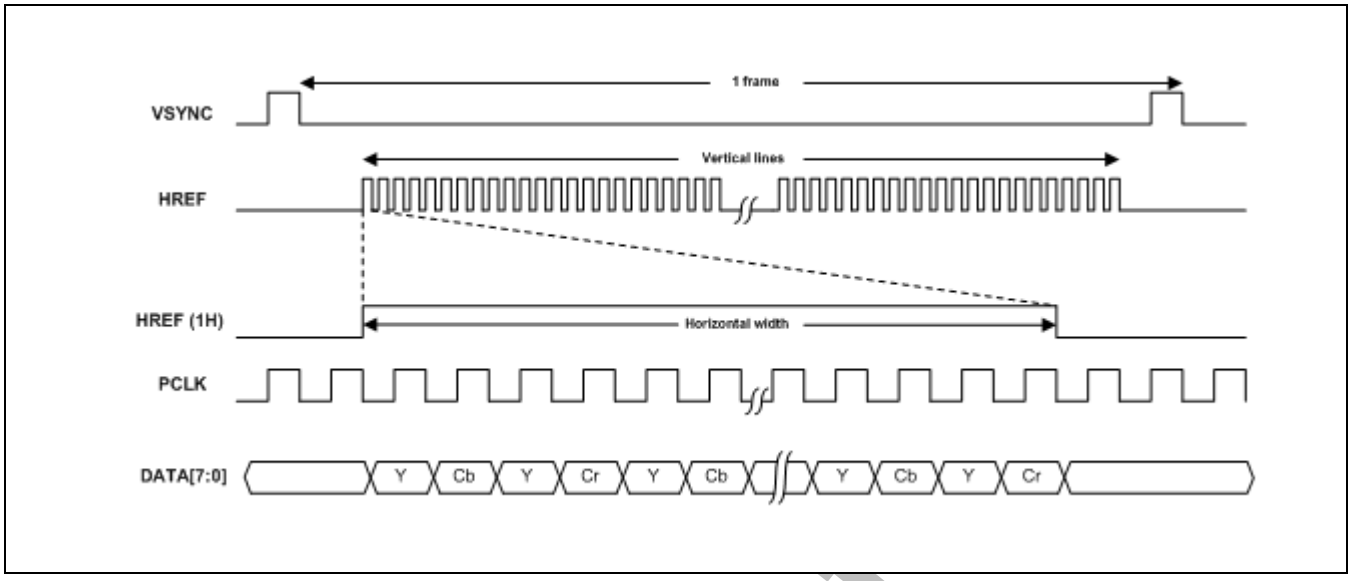

Figure 2-3 ITU-R BT 601 Input Timing Diagram

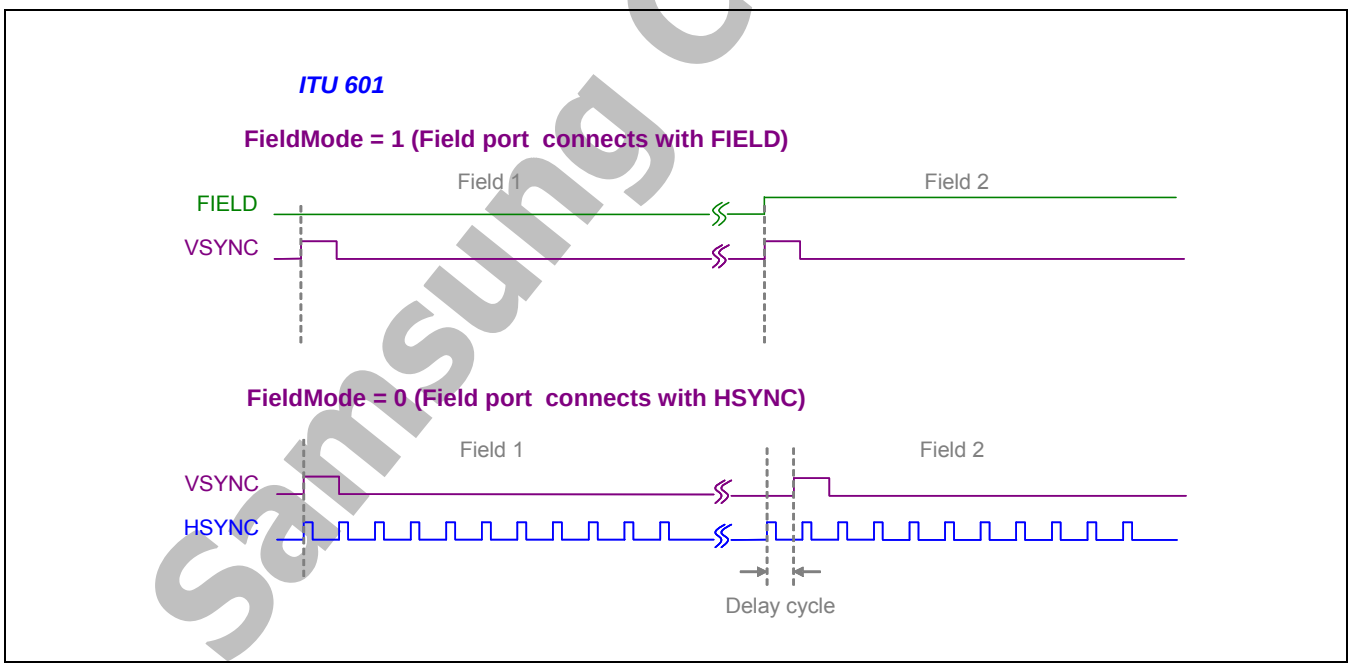

Figure 2-4 ITU-R BT 601 Interlace Handling Diagram

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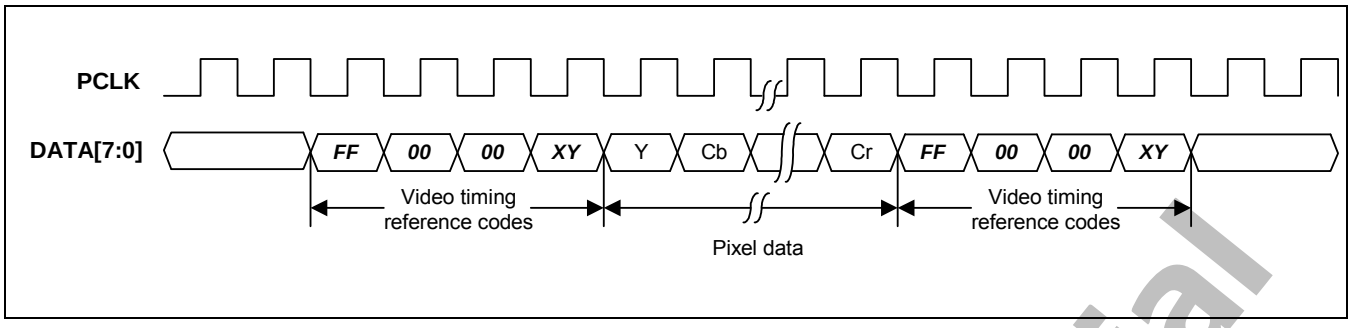

Figure 2-5 ITU-R BT 656 Input Timing Diagram

There are two timing reference signals in ITU-R BT 656 format: one at the beginning of each video data block (start of active video, SAV) and other at the end of each video data block (end of active video, EAV), as shown in *Figure 2-5* and *Table 2-3*.

Table 2-3 Video Timing Reference Codes of ITU-656 8-Bit Format

Data Bit Number	First Word	Second Word	Third Word	Fourth Word
7 (MSB)	1	0	0	1
6	1	0	0	F
5	1	0	0	V
4	1	0	0	H
3	1	0	0	P3
2	1	0	0	P2
1	1	0	0	P1
0	1	0	0	P0

NOTE: F = 0 (during field 1), 1 (during field 2)
V = 0 (elsewhere), 1 (during field blanking)
H = 0 (in SAV: Start of Active Video), 1 (in EAV: End of Active Video)
P0, P1, P2, P3 = Protection Bit
The camera interface logic catches video sync bits like H (SAV, EAV) and V (Frame Sync) after reserving data as "FF-00-00".

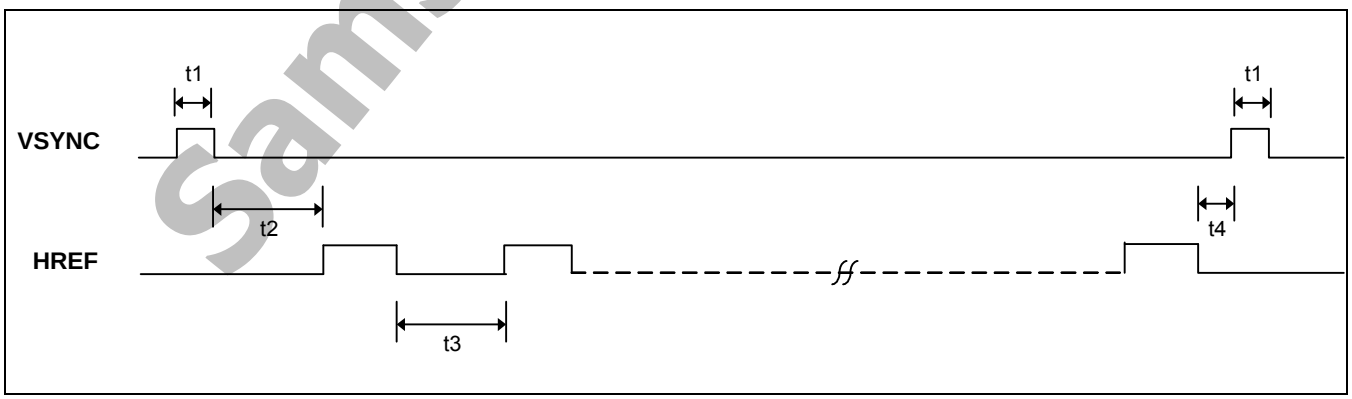

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Figure 2-6 Sync Signal Timing Diagram

Table 2-4 Sync Signal Timing Requirements

	Minimum	Maximum
t1	2 Horizontal Line	-
t2	2 Cycles of Pixel Clock + 5 Cycles of System Bus Clock	-
t3	2 Cycles of Pixel Clock	-
t4	12 Cycles of Pixel Clock	-

NOTE: If rotator is enabled, then (t4 + t1) should be sufficient to finish DMA transactions, since DMA transactions for rotator line buffer are delayed by 4 or 8 horizontal lines.

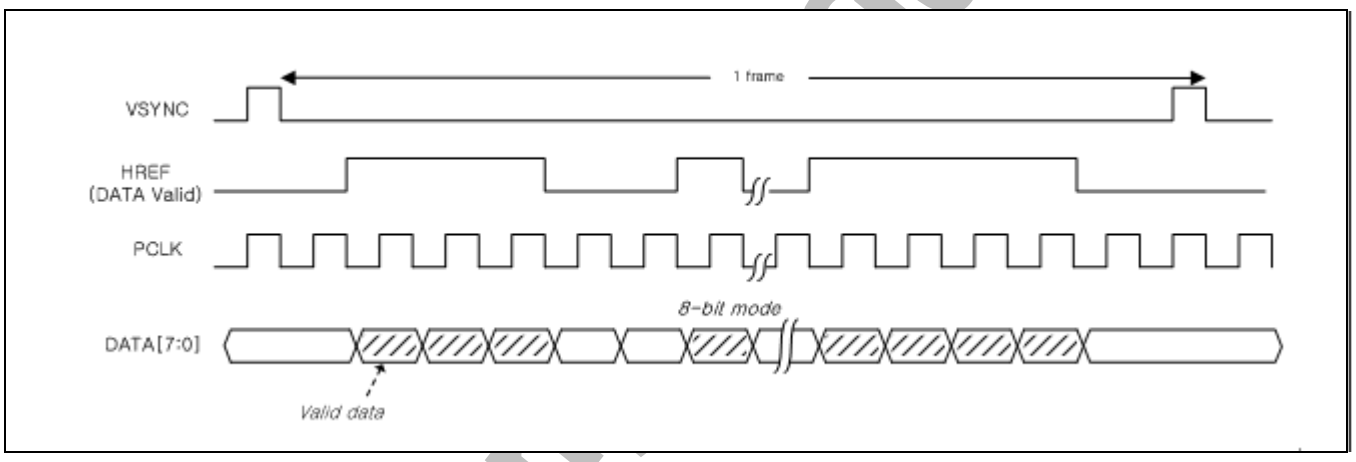

Figure 2-7 JPEG Input Timing Diagram (ITU 601 and Freerun Clock Mode)

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2.5.2 MIPI CSI DATA ALIGNMENT FROM MIPI CAMERA

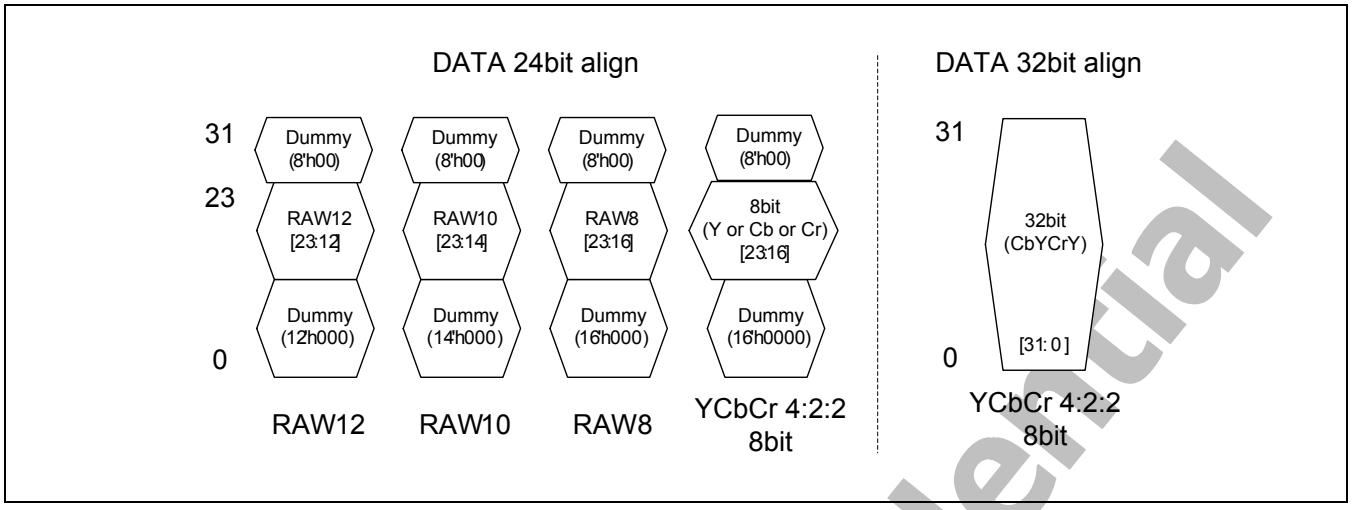

Figure 2-8 MIPI CSI DATA Alignment

Table 2-5 DATA Order of YCbCr422 Align

Format	Stream Order of Content	DATA – 24-bit Align	DATA – 32-bit Align
YCbCr422	Cb1→Y1→Cr1→Y2→ ...	DATA1[23:16] = Cb1 DATA2[23:16] = Y1 DATA3[23:16] = Cr1 DATA4[23:16] = Y2	DATA1[31:24] = Cb1 DATA1[23:16] = Y1 DATA1[15:8] = Cr1 DATA1[7:0] = Y2

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2.6 EXTERNAL CONNECTION GUIDE

The CAMIF input signals must not result in inter-skewing of the pixel clock line. Therefore, it is recommended to use next pin location and routing.

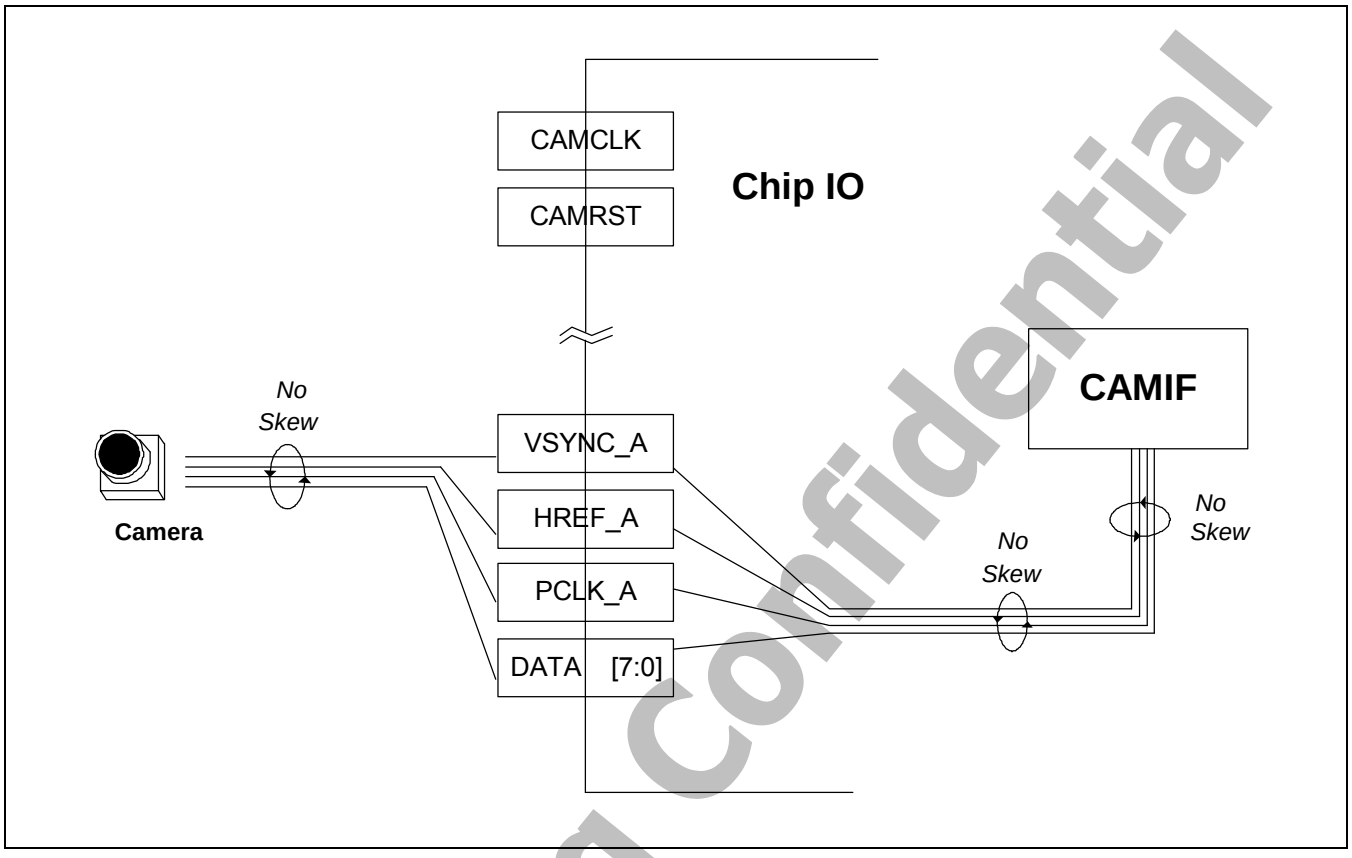

Figure 2-9 IO Connection Guide

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2.7 CAMERA INTERFACE OPERATION

2.7.1 INPUT/ OUTPUT DMA PORTS

Each CAMIF consists of two DMA ports, namely, Input DMA Port and Output DMA Port. From the view of system bus, both the ports are independent. The Input DMA port reads the image data from memory. On the other hand, the Output DMA port stores the image data into memory. These two master ports support various digital applications such as Digital Still Camera (DSC), MPEG-4 video conference, video recording, and so on.

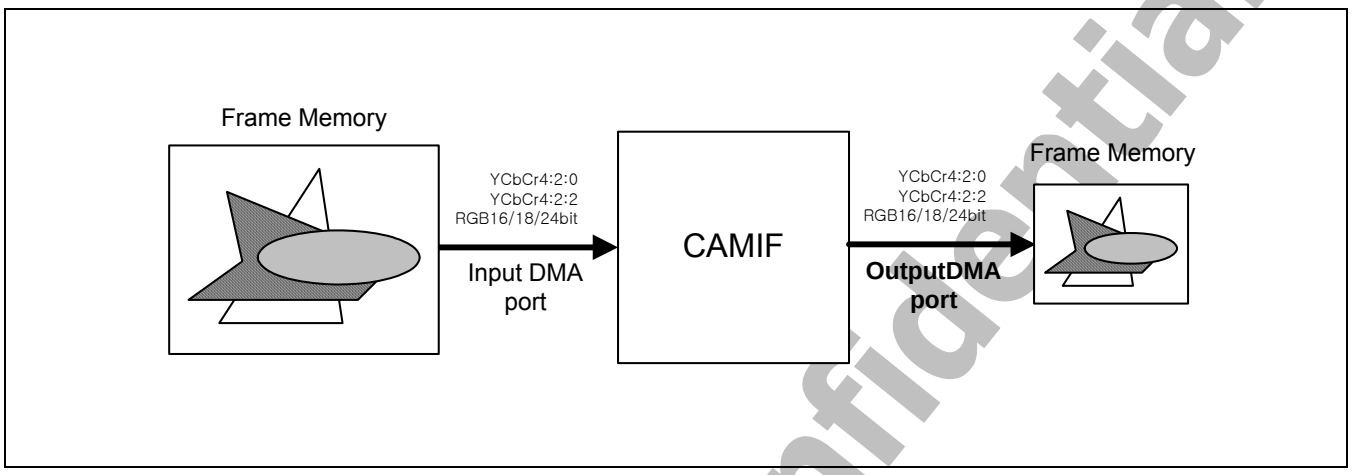

Figure 2-10 Input / Output DMA Ports

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2.7.2 CLOCK DOMAIN

Each CAMIF consists of three clock domains. The first clock domain is the system bus clock. The second clock domain is the camera pixel clock, PCLK. The third clock domain is the internal core clock. The system bus clock must be faster than the camera pixel clock.

As shown in *Figure 2-11*, CAM_MCLK must be separated from the fixed frequency like PLL clock. If external clock oscillator is used, CAM_MCLK should be floated. It is not necessary for the three clock domains to synchronize. Other signals like PCLK should similarly be connected to Schmitt-triggered level shifter.

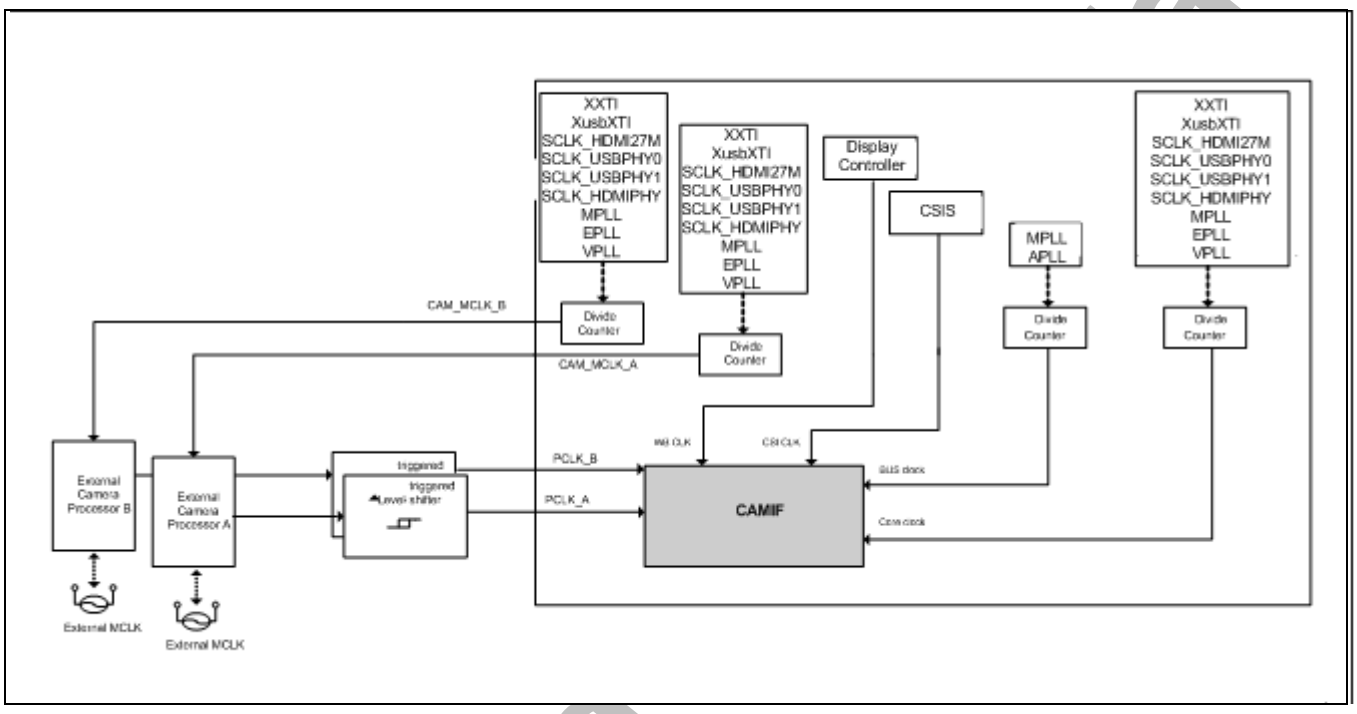

Figure 2-11 CAMIF Clock Generation

NOTE: The maximum frequency of core clock depends on whether user uses a local path between CAMIF and display controller or not. When it comes to the local path, the maximum frequency of core clock is 133MHz(It is recommended to use MPLL as the source of core clock). For other operation modes except for the local path, the maximum frequency of core clock is 166MHz(BUS clock should be used).
The maximum frequency of both CAM_MCLK_A and CAM_MCLK_B is 100MHz. And the maximum frequency of both PCLK_A and PCLK_B is 83MHz.

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2.7.3 FRAME MEMORY HIERARCHY

Frame memory consists of four ping-pong memories for output DMA ports. Also, the ping-pong memory consists of three element memories, namely, luminance Y, chrominance Cb, and chrominance Cr. It is recommended that the arbitration priority of CAMIF must be higher than any other masters (except for LCD controller). It is highly recommended to set the CAMIF priorities as fixed priorities, not rotation priorities.

In case of multi-AHB bus, the priority of system bus (including CAMIF) must be higher than others. If the bus traffic is so heavy that a DMA operation cannot complete for one horizontal period plus blank, it might result in mal-functioning. Therefore, the priority of CAMIF must be changed to other round robin or circular arbitration priorities. It is recommended that the bus including CAMIF should have a higher priority than any other buses in the memory matrix system. The CAMIF should not be the default master of AMBA system.

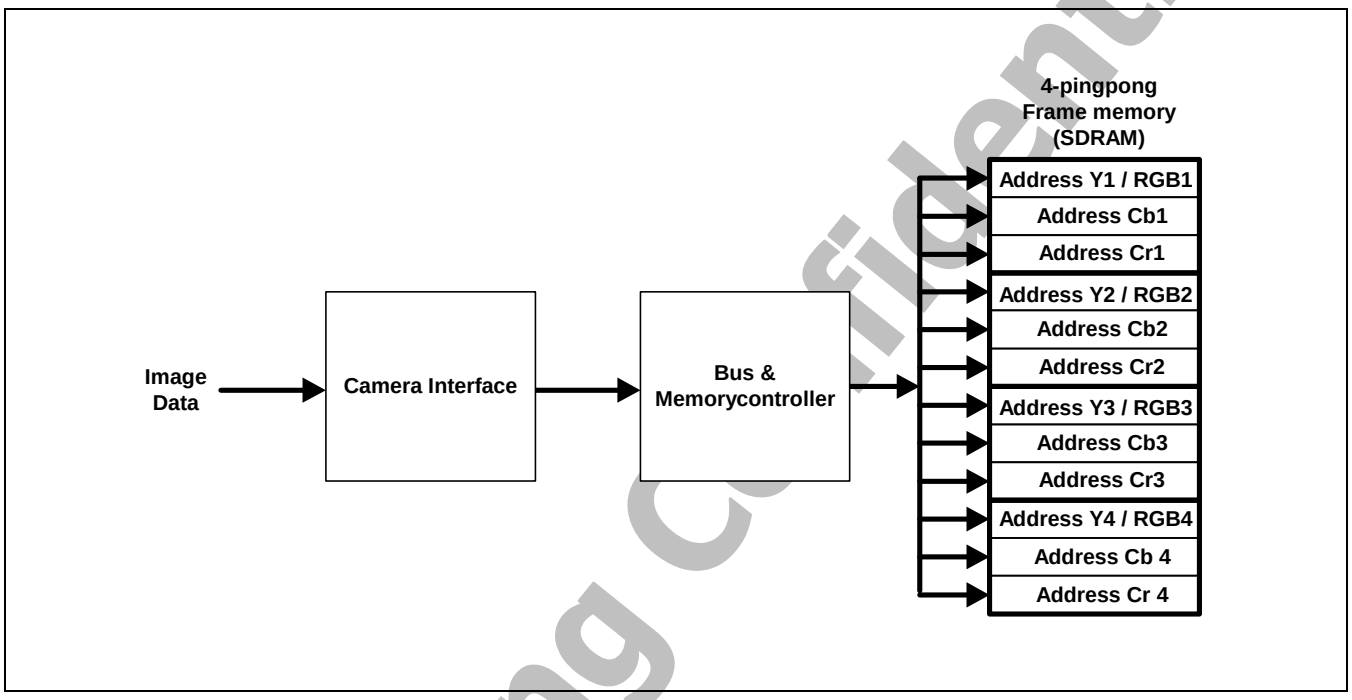

Figure 2-12 Ping-pong Memory Hierarchy

2.7.4 MEMORY STORING METHOD

The storing order of frame memory is little-endian. The first entering pixel is stored in the LSB sides, while the last entering pixel is stored in the MSB sides. The carried data by AXI bus is 64-bit. Therefore, CAMIF makes each Y-Cb-Cr words using little endian style. End-of-horizontal line not aligned with 64-bit is padded with zero for RAW8, RAW10 and RAW12 format, For more information, refer to *Figure 2-13*.

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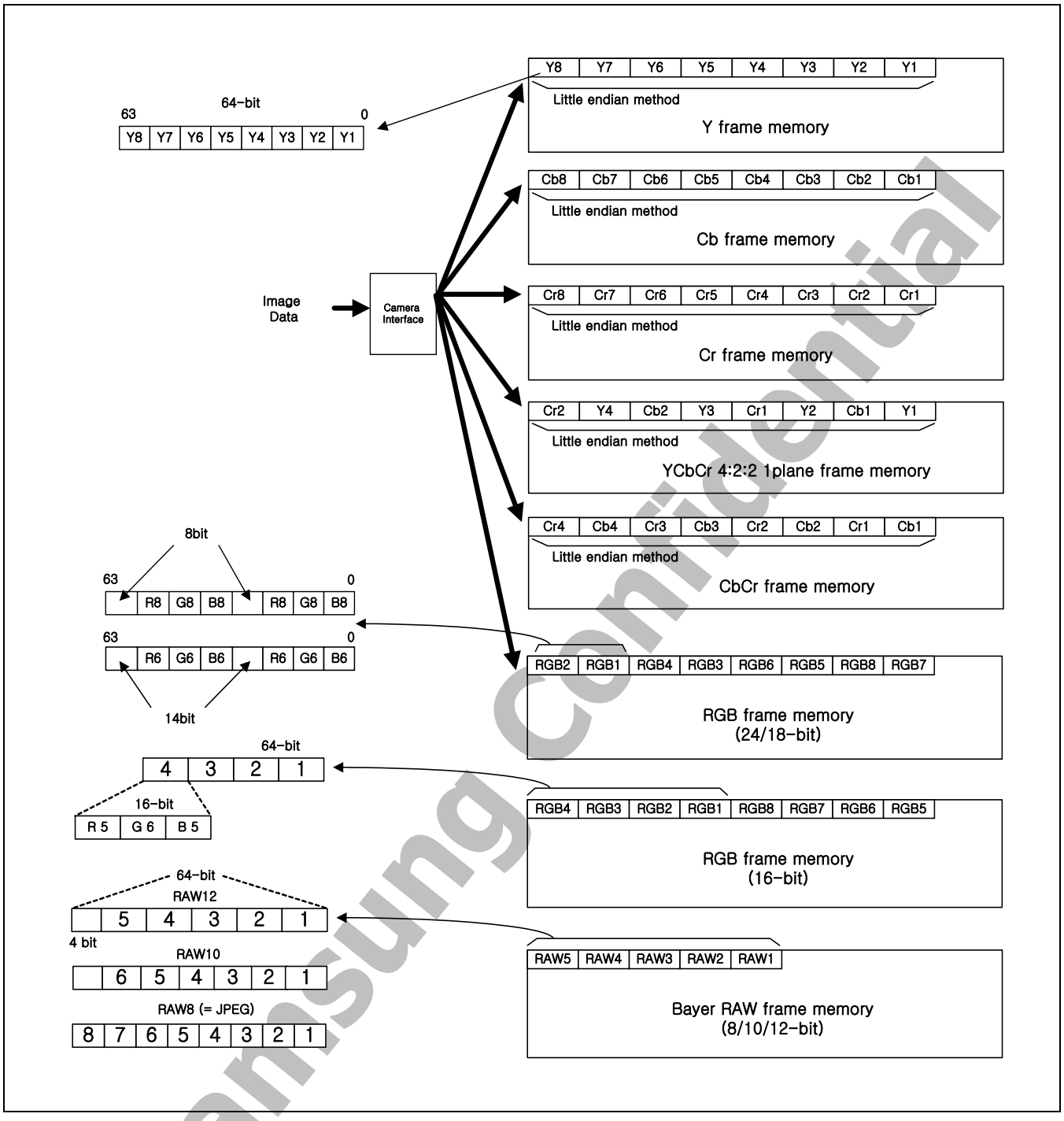

Figure 2-13 Memory Storing Style

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2.7.5 TIMING DIAGRAM FOR REGISTER SETTING

The first register setting for frame capture command can happen anytime in the frame period. It is recommended to first set the VSYNC “L” state, input DMA start “L” state, and then VVALID “H” state. VSYNC and VVALID

information can be read from status SFR. For more information, refer to *Figure 2-14*.

All commands (including ImgCptEn) are valid at VSYNC falling edge or VVALID rising edge. Except for the first SFR setting, all commands should be programmed in the Interrupt Service Routine (ISR). Size, image mirror or rotation, windowing, and zoom in settings are allowed to change during capturing. In case of DMA input mode, all commands should be programmed after the InputDMA and OutputDMA operation end, as shown in *Figure 2-15*.

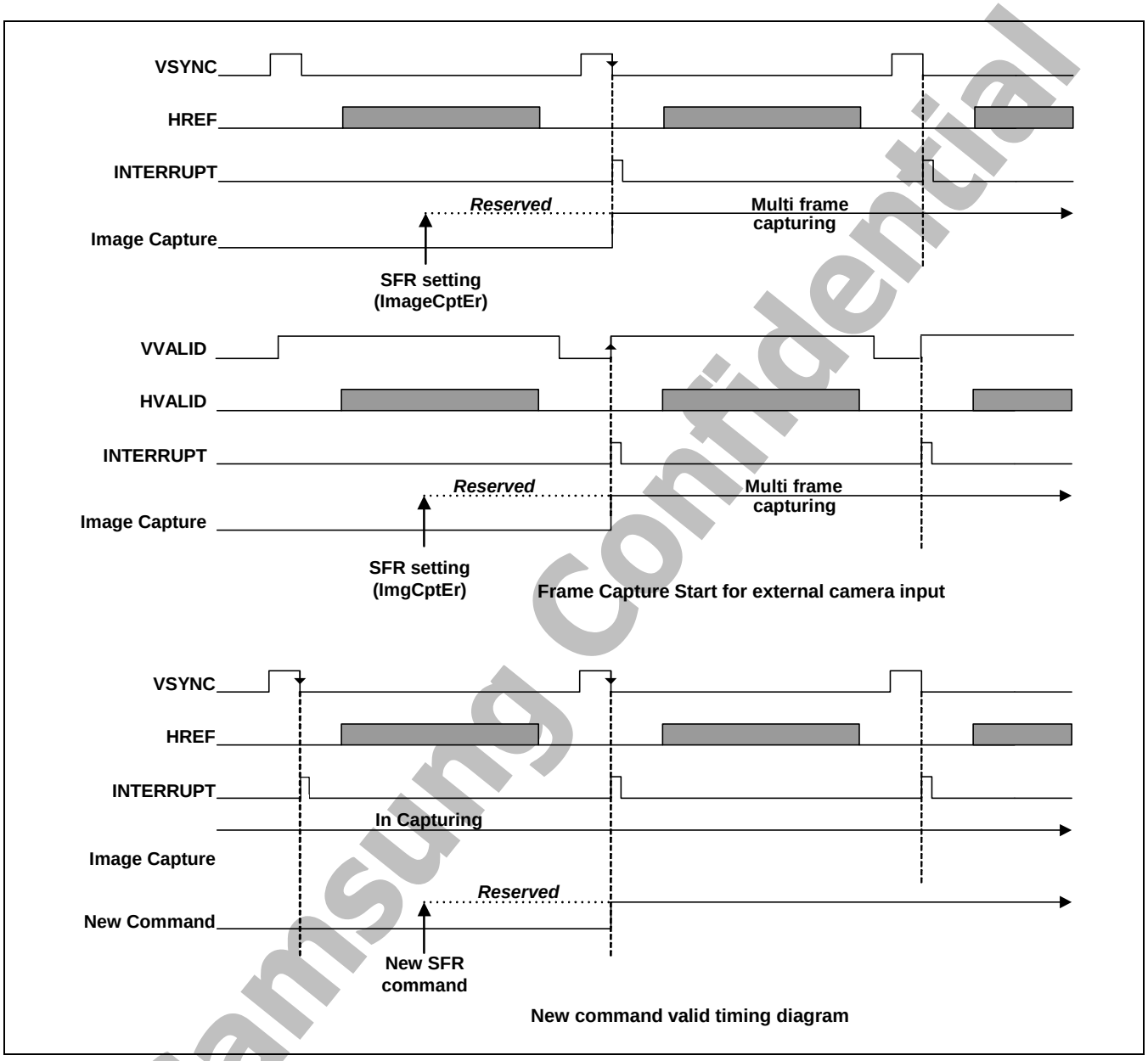

Figure 2-14 Timing Diagram for Camera Input Register setting

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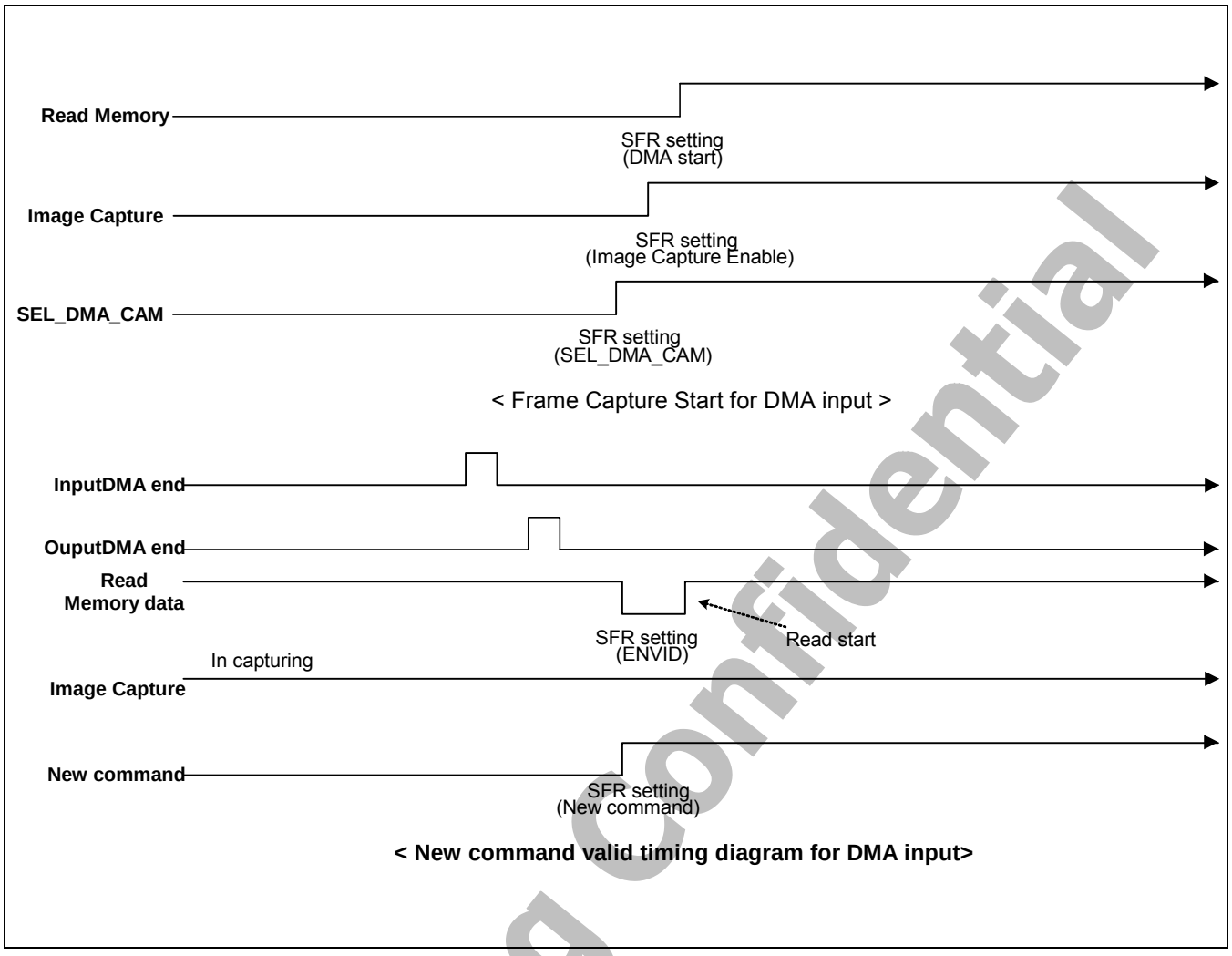

Figure 2-15 Timing Diagram for DMA input Register Setting

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2.7.6 TIMING DIAGRAM FOR LAST IRQ

The IRQ (except LastIRQ) is generated before image capture. Last IRQ specifies the end of camera signal capture. It can be set by the timing diagram shown in *Figure 2-16*. LastIRQEn specifies the ISR setting for next frame command. Therefore, for proper Last IRQ, you should follow the next sequence between LastIRQEn and ImgCptEn/ ImgCptEn_Sc.

It is recommended that ImgCptEn/ ImgCptEn_SC is set at the same time and at the end of SFR setting in ISR. FrameCnt specifies the next frame count. It is read in ISR.

As shown in *Figure 2-17*, the last captured frame count is "1", that is, Frame 1 specifies the last captured frame among frame 0~3. FrameCnt is increased by 1 at IRQ rising. The DMA input is selected by setting SFR. In this case, IRQ is generated after Output DMA operation is completed per frame. The SFR setting (ENVID_M '0' → '1') makes this mode aware of the starting point, and therefore, this mode does not require IRQ of starting point and LastIRQ. FrameCnt is increased by 1 at ENVID_M (InputDMA start) low to rising ('0' → '1') and ImgCptEn_SC '1'.

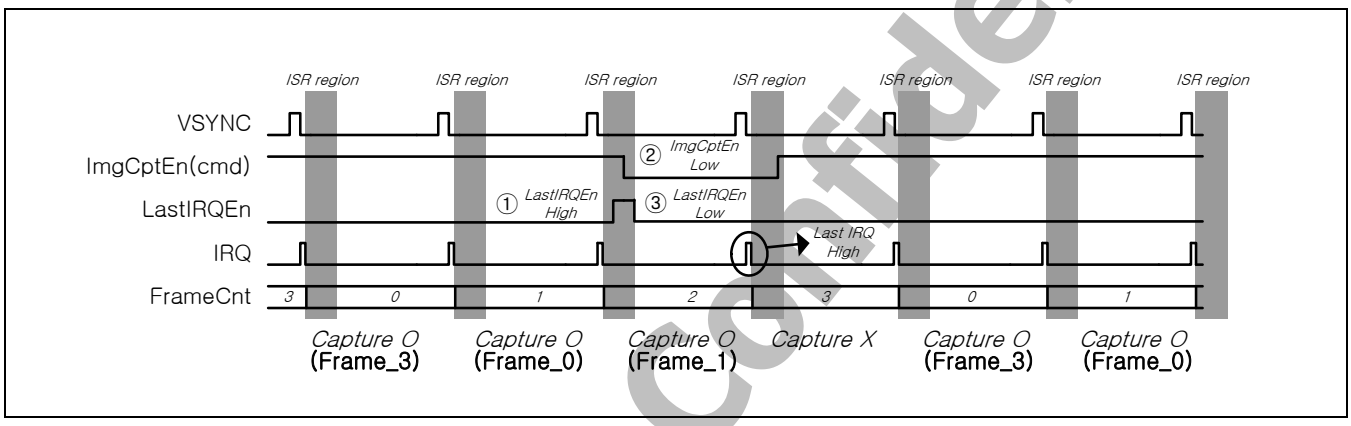

Figure 2-16 Timing Diagram for Last IRQ (LastIRQEn is Enabled)

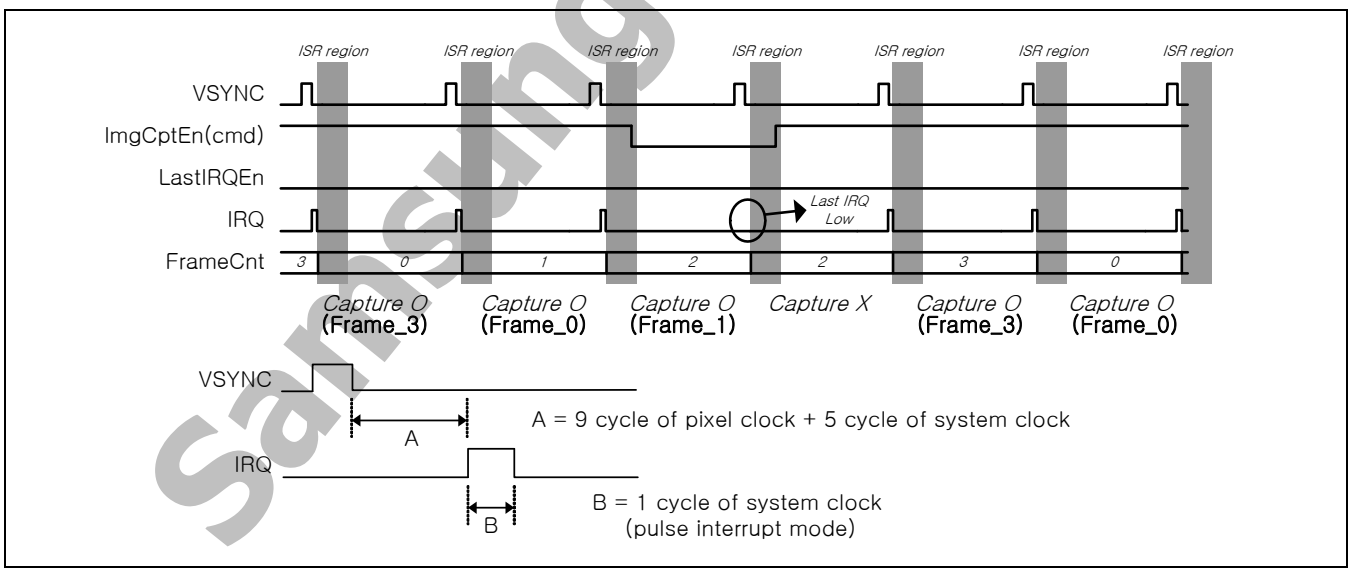

Figure 2-17 Diagram for Last IRQ (LastIRQEn is Disabled) and Timing Requirement

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2.7.7 TIMING DIAGRAM FOR IRQ (MEMORY DATA SCALING MODE)

You can select the Input DMA by setting SFR. After the DMA operation is completed for each frame, IRQ is generated. The SFR setting (ENVID_M '0' → '1') makes this mode aware of the starting point, and therefore, this mode does not require IRQ of starting point and LastIRQ. FrameCnt is increased by 1 at ENVID_M low to rising ('0' → '1') and ImgCptEn_SC '1'.

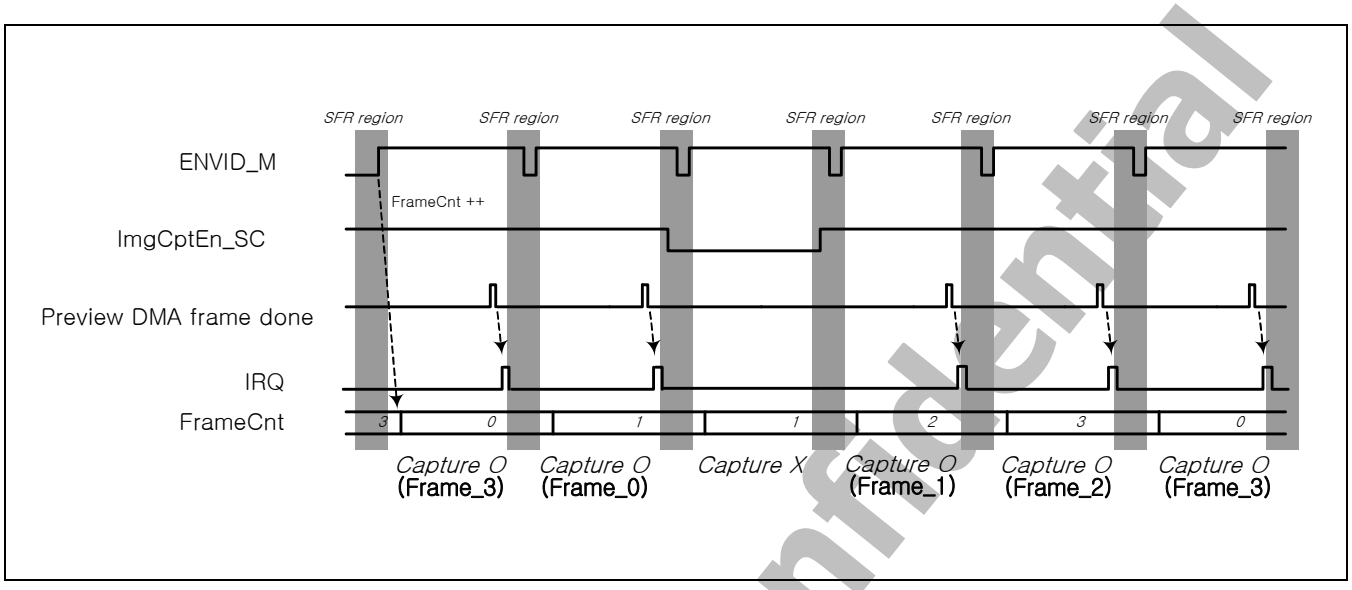

Figure 2-18 Timing Diagram for IRQ (Input DMA Path)

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2.7.8 INPUT DMA FEATURE

Input DMA supports memory data scaling.

Two different image data are required for Picture-in-Picture (PIP) operation. The first image is saved in memory by codecs like H.264, MPEG4, JPEG, and so on, while the second image is saved in memory via input DMA path.

The input DMA path comprises of YCbCr/RGB output format through scaler/ DMA path. The LCD controller displays and controls the two images.

If input DMA (reading the memory data) is used in the path, SEL_DMA_CAM (MSCTRL bit [3]) signal must be set to '1'. This input path is called Memory Scaling DMA path. The window zoom function is disabled in Memory Scaling DMA path.

NOTE: The memory image format for input DMA input includes:

- YCbCr 4:2:0 (non-interleave)
- YCbCr 4:2:2 (non-interleave)
- YCbCr 4:2:2 (Interleave)
- RGB

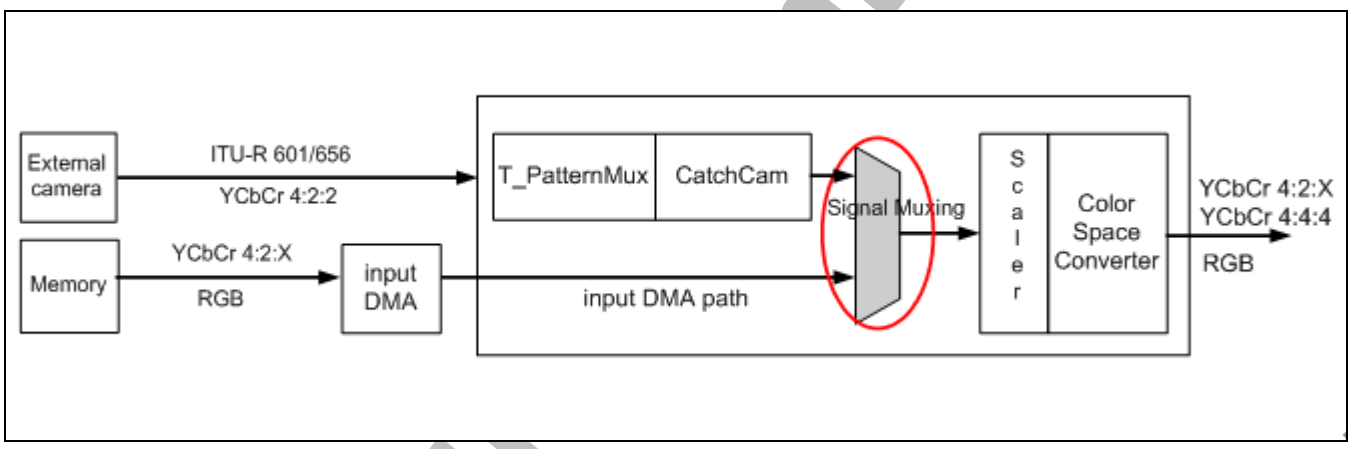

Figure 2-19 Input DMA or External Camera Interface

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2.7.9 CAMERA INTERLACE INPUT SUPPORT

To get data from the external camera, S5PV210 provides two modes, namely, ITU-R BT 601 YCbCr 8-bit mode and ITU-R BT 656 YCbCr 8-bit mode. It supports progressive input and interlaced input in both the modes.

2.7.9.1 Progressive Input

In progressive mode, all the input data is stored in four buffers (that is in ping-pong memory designated by SFR) sequentially by the unit of frame. For more information, refer to *Figure 2-20*.

2.7.9.2 Interlaced Input

In interlaced mode, all the input data is stored in four buffers (that is in ping-pong memory designated by SFR). However, in this mode, both field frame data and odd field frame data are stored successively. Therefore, even field frame data is stored in first and third ping-pong memories, while odd field frame data is stored second and fourth ping-pong memories. In case of image capture, start frame is always even field frame.

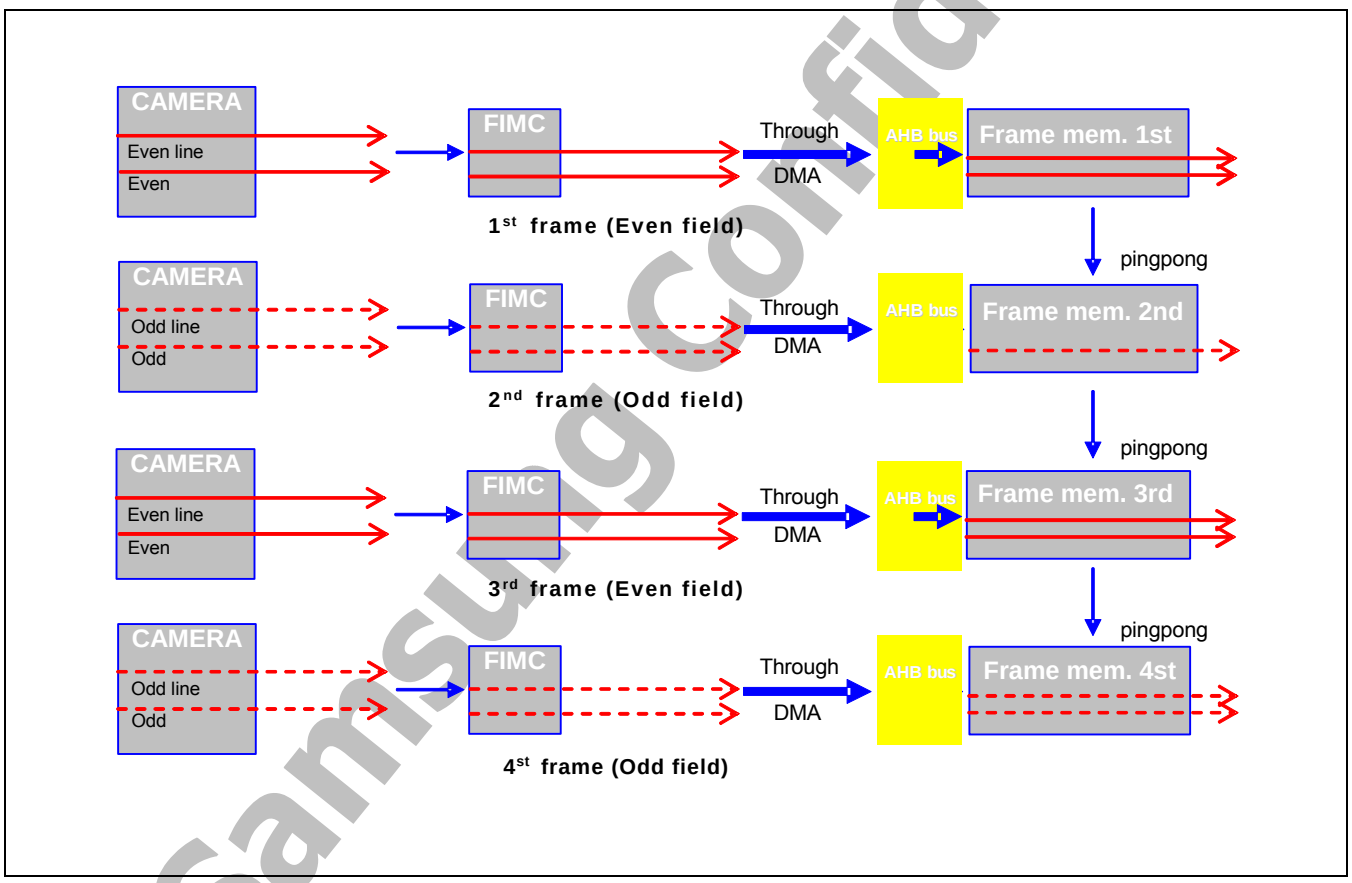

Figure 2-20 Frame Buffer Control

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2.8 REGISTER DESCRIPTION

2.8.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
CISRCFMT0	0xFB20_0000	R/W	Specifies input source format.	0x0000_0000
CIWDOFST0	0xFB20_0004	R/W	Specifies window offset register.	0x0000_0000
CIGCTRL0	0xFB20_0008	R/W	Specifies global control register.	0x2001_0080
CIWDOFST20	0xFB20_0014	R/W	Specifies window offset register 2.	0x0000_0000
CIOYSA10	0xFB20_0018	R/W	Specifies Y 1st frame start address for output DMA.	0x0000_0000
CIOYSA20	0xFB20_001C	R/W	Specifies Y 2nd frame start address for output DMA.	0x0000_0000
CIOYSA30	0xFB20_0020	R/W	Specifies Y 3rd frame start address for output DMA.	0x0000_0000
CIOYSA40	0xFB20_0024	R/W	Specifies Y 4th frame start address for output DMA.	0x0000_0000
CIOCBSA10	0xFB20_0028	R/W	Specifies Cb 1st frame start address for output DMA.	0x0000_0000
CIOCBSA20	0xFB20_002C	R/W	Specifies Cb 2nd frame start address for output DMA.	0x0000_0000
CIOCBSA30	0xFB20_0030	R/W	Specifies Cb 3rd frame start address for output DMA.	0x0000_0000
CIOCBSA40	0xFB20_0034	R/W	Specifies Cb 4th frame start address for output DMA.	0x0000_0000
CIOCRSA10	0xFB20_0038	R/W	Specifies Cr 1st frame start address for output DMA.	0x0000_0000
CIOCRSA20	0xFB20_003C	R/W	Specifies Cr 2nd frame start address for output DMA.	0x0000_0000
CIOCRSA30	0xFB20_0040	R/W	Specifies Cr 3rd frame start address for output DMA.	0x0000_0000
CIOCRSA40	0xFB20_0044	R/W	Specifies Cr 4th frame start address for output DMA.	0x0000_0000
CITRGFMT0	0xFB20_0048	R/W	Specifies target image format.	0x0000_0000
CIOCTRL0	0xFB20_004C	R/W	Specifies control-related Output DMA.	0x0000_0000
CISCPRERATIO0	0xFB20_0050	R/W	Specifies pre-scaler control 1.	0x0000_0000
CISCPREDST0	0xFB20_0054	R/W	Specifies pre-scaler control 2.	0x0000_0000
CISCCTRL0	0xFB20_0058	R/W	Specifies main-scaler control.	0x1800_0000
CITAREA0	0xFB20_005C	R/W	Specifies target area.	0x0000_0000
CIOLINESKIP0	0xFB20_0060	R/W	Specifies output DMA line skip.	0x0000_0000
CISTATUS0	0xFB20_0064	R/W	Specifies status register.	0x0000_0000
CIIMGCPT0	0xFB20_00C0	R/W	Specifies image capture enable command.	0x0000_0000

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Register	Address	R/W	Description	Reset Value
CICPTSEQ0	0xFB20_00C4	R/W	Specifies sequence-related capture.	0xFFFF_FFFF
CITHOLD0	0xFB20_00C8	R/W	Specifies QoS threshold.	0x0000_0000
CIIMGEFF0	0xFB20_00D0	R/W	Specifies related image effects.	0x0010_0080
CIIYSA00	0xFB20_00D4	R/W	Specifies Y frame start address for Input DMA.	0x0000_0000
CIICBSA00	0xFB20_00D8	R/W	Specifies Cb frame start address for Input DMA.	0x0000_0000
CIICRSA00	0xFB20_00DC	R/W	Specifies Cr frame start address for Input DMA.	0x0000_0000
CIILINESKIP_Y0	0xFB20_00EC	R/W	Specifies input DMA Y line skip.	0x0000_0000
CIILINESKIP_Cb0	0xFB20_00F0	R/W	Specifies input DMA Cb line skip.	0x0000_0000
CIILINESKIP_Cr0	0xFB20_00F4	R/W	Specifies input DMA Cr line skip.	0x0000_0000
CIREAL_ISIZE0	0xFB20_00F8	R/W	Specifies real input DMA image size.	0x0000_0000
MSCTRL0	0xFB20_00FC	R/W	Specifies input DMA control register.	0x0400_0000
CIIYSA10	0xFB20_0144	R/W	Specifies Y frame start address 1 for Input DMA.	0x0000_0000
CIICBSA10	0xFB20_0148	R/W	Specifies Cb frame start address 1 for Input DMA.	0x0000_0000
CIICRSA10	0xFB20_014C	R/W	Specifies Cr frame start address 1 for Input DMA.	0x0000_0000
CIOYOFF0	0xFB20_0168	R/W	Specifies output DMA Y offset.	0x0000_0000
CIOCBOFF0	0xFB20_016C	R/W	Specifies output DMA Cb offset.	0x0000_0000
CIOCROFF0	0xFB20_0170	R/W	Specifies output DMA Cr offset.	0x0000_0000
CIIYOFF0	0xFB20_0174	R/W	Specifies input DMA Y offset.	0x0000_0000
CIICBOFF0	0xFB20_0178	R/W	Specifies input DMA Cb offset.	0x0000_0000
CIICROFF0	0xFB20_017C	R/W	Specifies input DMA Cr offset.	0x0000_0000
ORGISIZE0	0xFB20_0180	R/W	Specifies input DMA original image size.	0x0000_0000
ORGOSIZE0	0xFB20_0184	R/W	Specifies output DMA original image size.	0x0000_0000
CIEXTEN0	0xFB20_0188	R/W	Specifies real output DMA image size.	0x0000_0000
CIDMAPARAM0	0xFB20_018C	R/W	Specifies DMA parameter register.	0x0000_0000
CSIIMGFMT0	0xFB20_0194	R/W	Specifies MIPI CSI image format register.	0x0000_001E
CMISC0	0xFB20_0198	R/W	Specifies miscellaneous control	0x0000_0000
CIKEY0	0xFB20_019C	R/W	Specifies key detect register.	0x0000_0000

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Register	Address	R/W	Description	Reset Value

Register	Address	R/W	Description	Reset Value
CISRCFMT1	0xFB30_0000	R/W	Specifies input source format.	0x0000_0000
CIWDOFST1	0xFB30_0004	R/W	Specifies window offset register.	0x0000_0000
CIGCTRL1	0xFB30_0008	R/W	Specifies global control register.	0x2001_0080
CIWDOFST21	0xFB30_0014	R/W	Specifies window offset register 2.	0x0000_0000
CIOYSA11	0xFB30_0018	R/W	Specifies Y 1st frame start address for output DMA.	0x0000_0000
CIOYSA21	0xFB30_001C	R/W	Specifies Y 2nd frame start address for output DMA.	0x0000_0000
CIOYSA31	0xFB30_0020	R/W	Specifies Y 3rd frame start address for output DMA.	0x0000_0000
CIOYSA41	0xFB30_0024	R/W	Specifies Y 4th frame start address for output DMA.	0x0000_0000
CIOCBSA11	0xFB30_0028	R/W	Specifies Cb 1st frame start address for output DMA.	0x0000_0000
CIOCBSA21	0xFB30_002C	R/W	Specifies Cb 2nd frame start address for output DMA.	0x0000_0000
CIOCBSA31	0xFB30_0030	R/W	Specifies Cb 3rd frame start address for output DMA.	0x0000_0000
CIOCBSA41	0xFB30_0034	R/W	Specifies Cb 4th frame start address for output DMA.	0x0000_0000
CIOCRSA11	0xFB30_0038	R/W	Specifies Cr 1st frame start address for output DMA.	0x0000_0000
CIOCRSA21	0xFB30_003C	R/W	Specifies Cr 2nd frame start address for output DMA.	0x0000_0000
CIOCRSA31	0xFB30_0040	R/W	Specifies Cr 3rd frame start address for output DMA.	0x0000_0000
CIOCRSA41	0xFB30_0044	R/W	Specifies Cr 4th frame start address for output DMA.	0x0000_0000
CITRGFMT1	0xFB30_0048	R/W	Specifies target image format.	0x0000_0000
CIOCTRL1	0xFB30_004C	R/W	Specifies control-related Output DMA.	0x0000_0000
CISCPRERATIO1	0xFB30_0050	R/W	Specifies pre-scaler control 1.	0x0000_0000
CISCPREDST1	0xFB30_0054	R/W	Specifies pre-scaler control 2.	0x0000_0000
CISCCTRL1	0xFB30_0058	R/W	Specifies main-scaler control.	0x1800_0000
CITAREA1	0xFB30_005C	R/W	Specifies target area.	0x0000_0000
CIOLINESKIP1	0xFB30_0060	R/W	Specifies output DMA line skip.	0x0000_0000
CISTATUS1	0xFB30_0064	R/W	Specifies status register.	0x0000_0000
CIIMGCPT1	0xFB30_00C0	R/W	Specifies image capture enable command.	0x0000_0000
CICPTSEQ1	0xFB30_00C4	R/W	Specifies sequence-related capture.	0xFFFF_FFFF
CITHOLD1	0xFB30_00C8	R/W	Specifies QoS threshold.	0x0000_0000
CIIMGEFF1	0xFB30_00D0	R/W	Specifies related image effects.	0x0010_0080
CIIYSA01	0xFB30_00D4	R/W	Specifies Y frame start address for Input	0x0000_0000

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Register	Address	R/W	Description	Reset Value
			DMA.	
CIICBSA01	0xFB30_00D8	R/W	Specifies Cb frame start address for Input DMA.	0x0000_0000
CIICRSA01	0xFB30_00DC	R/W	Specifies Cr frame start address for Input DMA.	0x0000_0000
CIILINESKIP_Y1	0xFB30_00EC	R/W	Specifies input DMA Y line skip.	0x0000_0000
CIILINESKIP_Cb1	0xFB30_00F0	R/W	Specifies input DMA Cb line skip.	0x0000_0000
CIILINESKIP_Cr1	0xFB30_00F4	R/W	Specifies input DMA Cr line skip.	0x0000_0000
CIREAL_ISIZE1	0xFB30_00F8	R/W	Specifies real input DMA image size.	0x0000_0000
MSCTRL1	0xFB30_00FC	R/W	Specifies input DMA control register.	0x0400_0000
CIIYSA11	0xFB30_0144	R/W	Specifies Y frame start address 1 for Input DMA.	0x0000_0000
CIICBSA11	0xFB30_0148	R/W	Specifies Cb frame start address 1 for Input DMA.	0x0000_0000
CIICRSA11	0xFB30_014C	R/W	Specifies Cr frame start address 1 for Input DMA.	0x0000_0000
CIOYOFF1	0xFB30_0168	R/W	Specifies output DMA Y offset.	0x0000_0000
CIOCBOFF1	0xFB30_016C	R/W	Specifies output DMA Cb offset.	0x0000_0000
CIOCROFF1	0xFB30_0170	R/W	Specifies output DMA Cr offset.	0x0000_0000
CIIYOFF1	0xFB30_0174	R/W	Specifies input DMA Y offset.	0x0000_0000
CIICBOFF1	0xFB30_0178	R/W	Specifies input DMA Cb offset.	0x0000_0000
CIICROFF1	0xFB30_017C	R/W	Specifies input DMA Cr offset.	0x0000_0000
ORGISIZE1	0xFB30_0180	R/W	Specifies input DMA original image size.	0x0000_0000
ORGOSIZE1	0xFB30_0184	R/W	Specifies output DMA original image size.	0x0000_0000
CIEXTEN1	0xFB30_0188	R/W	Specifies real output DMA image size.	0x0000_0000
CIDMAPARAM1	0xFB30_018C	R/W	Specifies DMA parameter register.	0x0000_0000
CSIIMGFMT1	0xFB30_0194	R/W	Specifies MIPI CSI image format register.	0x0000_001E
CMISC1	0xFB30_0198	R/W	Specifies miscellaneous control	0x0000_0000
CIKEY1	0xFB30_019C	R/W	Specifies key detect register.	0x0000_0000

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Register	Address	R/W	Description	Reset Value
CISRCFMT2	0xFB40_0000	R/W	Specifies input source format.	0x0000_0000
CIWDOFST2	0xFB40_0004	R/W	Specifies window offset register.	0x0000_0000
CIGCTRL2	0xFB40_0008	R/W	Specifies global control register.	0x2001_0080
CIWDOFST22	0xFB40_0014	R/W	Specifies window offset register 2.	0x0000_0000
CIOYSA12	0xFB40_0018	R/W	Specifies Y 1st frame start address for output DMA.	0x0000_0000
CIOYSA22	0xFB40_001C	R/W	Specifies Y 2nd frame start address for output DMA.	0x0000_0000
CIOYSA32	0xFB40_0020	R/W	Specifies Y 3rd frame start address for output DMA.	0x0000_0000
CIOYSA42	0xFB40_0024	R/W	Specifies Y 4th frame start address for output DMA.	0x0000_0000
CIOCBSA12	0xFB40_0028	R/W	Specifies Cb 1st frame start address for output DMA.	0x0000_0000
CIOCBSA22	0xFB40_002C	R/W	Specifies Cb 2nd frame start address for output DMA.	0x0000_0000
CIOCBSA32	0xFB40_0030	R/W	Specifies Cb 3rd frame start address for output DMA.	0x0000_0000
CIOCBSA42	0xFB40_0034	R/W	Specifies Cb 4th frame start address for output DMA.	0x0000_0000
CIOCRSA12	0xFB40_0038	R/W	Specifies Cr 1st frame start address for output DMA.	0x0000_0000
CIOCRSA22	0xFB40_003C	R/W	Specifies Cr 2nd frame start address for output DMA.	0x0000_0000
CIOCRSA32	0xFB40_0040	R/W	Specifies Cr 3rd frame start address for output DMA.	0x0000_0000
CIOCRSA42	0xFB40_0044	R/W	Specifies Cr 4th frame start address for output DMA.	0x0000_0000
CITRGFMT2	0xFB40_0048	R/W	Specifies target image format.	0x0000_0000
CIOCTRL2	0xFB40_004C	R/W	Specifies control-related Output DMA.	0x0000_0000
CISCPRERATIO2	0xFB40_0050	R/W	Specifies pre-scaler control 1.	0x0000_0000
CISCPREDST2	0xFB40_0054	R/W	Specifies pre-scaler control 2.	0x0000_0000
CISCCTRL2	0xFB40_0058	R/W	Specifies main-scaler control.	0x1800_0000
CITAREA2	0xFB40_005C	R/W	Specifies target area.	0x0000_0000
CIOLINESKIP2	0xFB40_0060	R/W	Specifies output DMA line skip.	0x0000_0000
CISTATUS2	0xFB40_0064	R/W	Specifies status register.	0x0000_0000
CIIMGCPT2	0xFB40_00C0	R/W	Specifies image capture enable command.	0x0000_0000
CICPTSEQ2	0xFB40_00C4	R/W	Specifies sequence-related capture.	0xFFFF_FFFF
CITHOLD2	0xFB40_00C8	R/W	Specifies QoS threshold.	0x0000_0000
CIIMGEFF2	0xFB40_00D0	R/W	Specifies related image effects.	0x0010_0080

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Register	Address	R/W	Description	Reset Value
CIIYSA02	0xFB40_00D4	R/W	Specifies Y frame start address for Input DMA.	0x0000_0000
CIICBSA02	0xFB40_00D8	R/W	Specifies Cb frame start address for Input DMA.	0x0000_0000
CIICRSA02	0xFB40_00DC	R/W	Specifies Cr frame start address for Input DMA.	0x0000_0000
CIILINESKIP_Y2	0xFB40_00EC	R/W	Specifies input DMA Y line skip.	0x0000_0000
CIILINESKIP_Cb2	0xFB40_00F0	R/W	Specifies input DMA Cb line skip.	0x0000_0000
CIILINESKIP_Cr2	0xFB40_00F4	R/W	Specifies input DMA Cr line skip.	0x0000_0000
CIREAL_ISIZE2	0xFB40_00F8	R/W	Specifies real input DMA image size.	0x0000_0000
MSCTRL2	0xFB40_00FC	R/W	Specifies input DMA control register.	0x0400_0000
CIIYSA12	0xFB40_0144	R/W	Specifies Y frame start address 1 for Input DMA.	0x0000_0000
CIICBSA12	0xFB40_0148	R/W	Specifies Cb frame start address 1 for Input DMA.	0x0000_0000
CIICRSA12	0xFB40_014C	R/W	Specifies Cr frame start address 1 for Input DMA.	0x0000_0000
CIOYOFF2	0xFB40_0168	R/W	Specifies output DMA Y offset.	0x0000_0000
CIOCBOFF2	0xFB40_016C	R/W	Specifies output DMA Cb offset.	0x0000_0000
CIOCROFF2	0xFB40_0170	R/W	Specifies output DMA Cr offset.	0x0000_0000
CIIYOFF2	0xFB40_0174	R/W	Specifies input DMA Y offset.	0x0000_0000
CIICBOFF2	0xFB40_0178	R/W	Specifies input DMA Cb offset.	0x0000_0000
CIICROFF2	0xFB40_017C	R/W	Specifies input DMA Cr offset.	0x0000_0000
ORGISIZE2	0xFB40_0180	R/W	Specifies input DMA original image size.	0x0000_0000
ORGOSIZE2	0xFB40_0184	R/W	Specifies output DMA original image size.	0x0000_0000
CIEXTEN2	0xFB40_0188	R/W	Specifies real output DMA image size.	0x0000_0000
CIDMAPARAM2	0xFB40_018C	R/W	Specifies DMA parameter register.	0x0000_0000
CSIIMGFMT2	0xFB40_0194	R/W	Specifies MIPI CSI image format register.	0x0000_001E
CMISC2	0xFB40_0198	R/W	Specifies miscellaneous control	0x0000_0000
CIKEY2	0xFB40_019C	R/W	Specifies key detect register.	0x0000_0000

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NOTE: 'L' means that SFR can change at vsync edge during camera capture. (O: possible change, X: impossible change). Also, 'M' means that SFRs have relationship capturing result while using input DMA path. (O: relationship, X: no relationship).

2.8.1.1 Camera Source Format Register (CISRCFMTn)

- CISRCFMT0, R/W, Address = 0xFB20_0000
- CISRCFMT1, R/W, Address = 0xFB30_0000
- CISRCFMT2, R/W, Address = 0xFB40_0000

CISRCFMTn	Bit	Description	Initial State
ITU601_656n	[31]	1 = ITU-R BT.601 YCbCr 8-bit mode enable 0 = ITU-R BT.656 YCbCr 8-bit mode enable (ML=XX)	0
UVOffset	[30]	Controls Cb,Cr value offset. 1 = Cb=Cb+128 , Cr=Cr+128 0 = +0 (normally used) (ML=XX)	0
Reserved	[29]	Should be '0'.	0
SrcHsize_CAM	[28:16]	Specifies the source horizontal pixel number (camera or FIFO input). For more information, refer to gathering extension register (SrcHsize_CAM_ext). Note) 16's multiple. Must be 4's multiple of PreHorRatio if WinOfsEn is 0 (ML=XO)	0
Order422_CAM	[15:14]	Specifies the camera input YCbCr order for 8-bit mode. 8-bit mode Data Flow ⟶ 00 = Y0Cb0Y1Cr0… 01 = Y0Cr0Y1Cb0… 10 = Cb0Y0Cr0Y1… 11 = Cr0Y0Cb0Y1… (ML=XX)	0
SrcVsize_CAM	[13:0]	Specifies the source vertical pixel number (Camera or FIFO input). Note) It must be a multiple of PreVerRatio if V scale down or WinOfsEn is 0. It should be 2's multiple in case YCbCr 422 input and cam interlace mode. (ML=XO)	0

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2.8.1.2 Camera Window Offset Register (CIWDOFSTn)

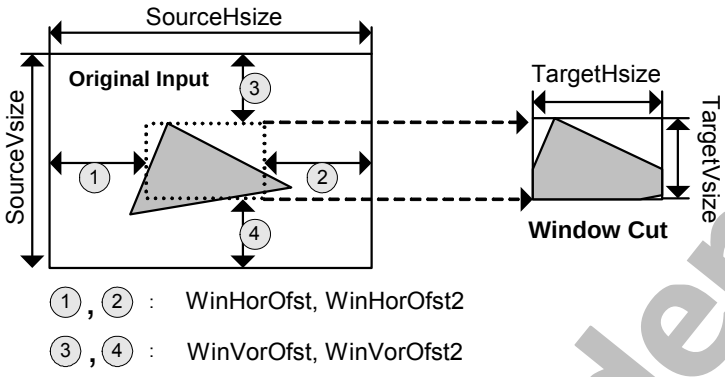

Figure 2-21 Camera Window Offset Scheme

WinHorOfst2 and WinVerOfst2 are assigned in the CIWDOFST2n registers.

- CIWDOFST0, R/W, Address = 0xFB20_0004
- CIWDOFST1, R/W, Address = 0xFB30_0004
- CIWDOFST2, R/W, Address = 0xFB40_0004

CIWDOFSTn	Bit	Description	Initial State
WinOfsEn	[31]	1 = Enables window offset 0 = No offset Note) If input format is either RAW or WB(Write Back), this function is not valid. (ML=XO)	0
ClrOvFiY	[30]	1 = Clears the overflow indication flag of input FIFO Y 0 = Normal (ML=XX)	0
ClrOvRLB	[29]	Clears the overflow indication flag of Line Buffer for Rotation. (ML=XX)	0
Reserved	[28:27]	Reserved	0

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WinHorOfst	[26:16]	Specifies window horizontal offset by pixel unit. It should be multiple of 2. Note) CAMIF0 & CAMIF2 : SourceHsize-WinHorOfst- WinHorOfst2 should be a multiple of 16. For more information, refer to gathering extension register (WinHorOfst_ext). (ML=XO)	0
ClrOvFiCb	[15]	1 = Clears the overflow indication flag of input FIFO Cb 0 = Normal (ML=XX)	0
ClrOvFiCr	[14]	1 = Clears the overflow indication flag of input FIFO Cr 0 = Normal (ML=XX)	0
Reserved	[13:12]	Reserved	0
WinVerOfst	[11:0]	Specifies window vertical offset by pixel unit. In case of interlaced input, this value should be 2's multiple. (ML=XO)	0

NOTE: Clear bits should be set to zero after clearing the flags.

Below constraints of Crop HSIZE and Crop Vsize are only for CAMIF0 & CAMIF1 & CAMIF2.

Crop Hsize (= SourceHsize - WinHorOfst - WinHorOfst2) must be 16's multiple. Also, It should be 4's multiple of PreHorRatio.

Crop Vsize (= SourceVsize - WinVerOfst - WinVerOfst2) must be multiple of PreVerRatio when V scale down. Must be an even number and minimum 8 if the output image format is YCbCr 4:2:0.

Example:

Crop Hsize	Permitted Prescale_ratio	PreDstWidth_xx
8n	2	4n
16n	2 or 4	4n
32n	2, 4 or 8	4n

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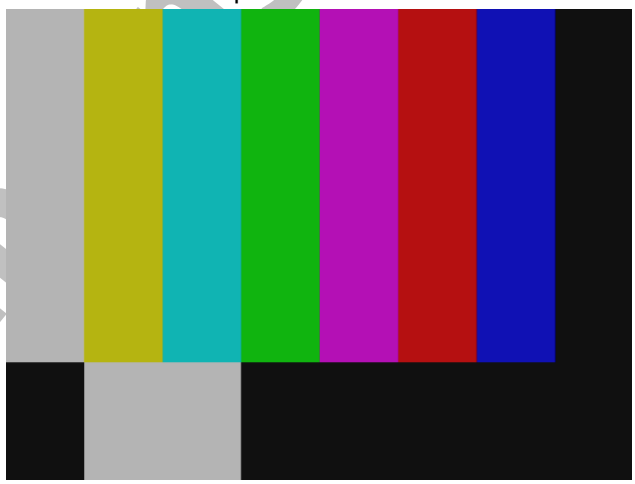
2.8.1.3 Global Control Register (CIGCTRLn)

- CIGCTRL0, R/W, Address = 0xFB20_0008
- CIGCTRL1, R/W, Address = 0xFB30_0008
- CIGCTRL2, R/W, Address = 0xFB40_0008

CIGCTRLn	Bit	Description	Initial State
SwRst	[31]	Specifies the camera interface software reset. Before you set this bit, set the ITU601_656n bit of CISRCFMT as “1” temporarily at first SFR setting. Next sequence is recommended. [ITU601 case: ITU601_656n “1” → SwRst “1” → SwRst “0” for first SFR setting], [ITU656 case: ITU601_656n “1” → SwRst “1” → SwRst “0” → ITU601_656n “0” for first SFR setting] Note) 1) User should not use SwRst function in the middle of transferring data out by DMA. 2) User should disable 'ImgCptEn' and ' IRQ_Enable' bit before using this function. (ML=XX)	0
Reserved	[30]	Should be ‘0’.	0
SelCam_ITU	[29]	Selects external multiple ITU camera. 1 = Selects ITU Camera A 0 = Selects ITU Camera B (ML=XX)	1
TestPattern	[28:27]	This register should be set at ITU-T 601 8-bit mode only, not at ITU-T 656 mode. Source CAM size should be 640 x 480 size and Order422_CAM register should be ‘00’. 00 = External camera processor input (normal) 01 = Color bar test pattern  10 = Reserved 11 = Reserved (ML=XX)	0

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CIGCTRLn	Bit	Description	Initial State
InvPolPCLK	[26]	1 = Inverse the polarity of PCLK 0 = Normal (ML=XX)	0
InvPolVSYNC	[25]	1 = Inverse the polarity of VSYNC 0 = Normal (ML=XX)	0
InvPolHREF	[24]	1 = Inverse the polarity of HREF 0 = Normal (ML=XX)	0
Reserved	[23]	Should be '0'.	0
IRQ_Ovfen	[22]	1 = Enables Overflow interrupt (Interrupt is generated during overflow occurrence) 0 = Disables Overflow interrupt (normal) (ML=XX)	0
Href_mask	[21]	1 = Mask out Href during Vsync blank 0 = No mask (ML=XX)	0
Reserved	[20]	Should be '1'.	0
IRQ_CLR	[19]	Writes IRQ_CLR to '1' to clear Interrupt. This bit Auto-clear. (ML=XX)	0
IRQ_EndDisable	[18]	This bit is related to Camera or Local FIFO(WB) input only. 1 = Interrupt enables at Frame end point 0 = Interrupt disables at Frame end point (default) (ML=XX)	0
IRQ_StartEnable	[17]	This bit is related to Camera or Local FIFO(WB) input only. 1 = Interrupt disables at Frame start point 0 = Interrupt enables at Frame start point (default) (ML=XX)	0
IRQ_Enable	[16]	1 = Enables Interrupt (default) 0 = Disables Interrupt Note: If the interrupt enables, then the bit[20]@CIGCTRLn should be set to '1'. (ML=XX)	1
Reserved	[15:14]	Reserved	0
SwUpdate	[13]	Updates shadow register by software setting (Both DMA input and Camera input are applied) 1 = Shadow register updates immediately (Autoclears 1 to 0) 0 = Shadow register updates at Hardware frame start pulse (ML=XX)	0
ShadowDisable	[12]	Shadow register cannot be updated by Hardware frame start (input path should be local path). At the start of first frame, it is necessary to set ShadowDisable as '0'. 1 = Disables (update is impossible)	0

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CIGCTRLn	Bit	Description	Initial State
		0 = Enables (update is possible) (ML=XX)	
Reserved	[11:9]	-	0
CAM_JPEG	[8]	Specifies the camera input in 8-bit JPEG format. If the image format is selected as JPEG format, the image format conversion is not possible. It should be set as scaler bypass mode and ITU601 8-bit mode. 1 = JPEG format 0 = Non-JPEG format (ML=XX)	0
Reserved	[7]	Should be '1'.	1
SelWB_CAMIF	[6]	Specifies the WriteBack input select signal. 1 = WriteBack input select (YCbCr4:4:4 only) 0 = Camera input select (ML=XX)	0
CSC_601_709	[5]	Selects ColorSpaceConversion equation. 1 = ITU709 equation select (HD size target method) 0 = ITU601 equation select (SD size target method) (ML=XO)	0
InvPolHSYNC	[4]	1 = Inverses the polarity of HSYNC (this bit is useful only when delay count interlace mode and FIELD port is connected to HSYNC) 0 = Normal (ML=XX)	0
SelCam_CAMIF	[3]	Selects the External camera. 1 = Selects MIPI Camera 0 = Selects ITU Camera (ML=XX)	0
FIELDMODE	[2]	Specifies the ITU601 interlace field mode (Do not care this bit in ITU656 mode). 1 = Uses the FIELD port mode (FIELD port = FIELD signal) 0 = Uses the Edge delay count mode (FIELD port = HSYNC signal) Note: Check the FIELD port connection. (ML=XX)	0
InvPolFIELD	[1]	1 = Inverses the polarity of FIELD 0 = Normal (ML=XX)	0
Cam_Interlace	[0]	Specifies the External Camera scan method. 1 = Interlace 0 = Progressive If this mode is enable, control signals cannot change under operation except ImgCptEn,ImgCptEnSC and ScalerStart (ML=XX)	0

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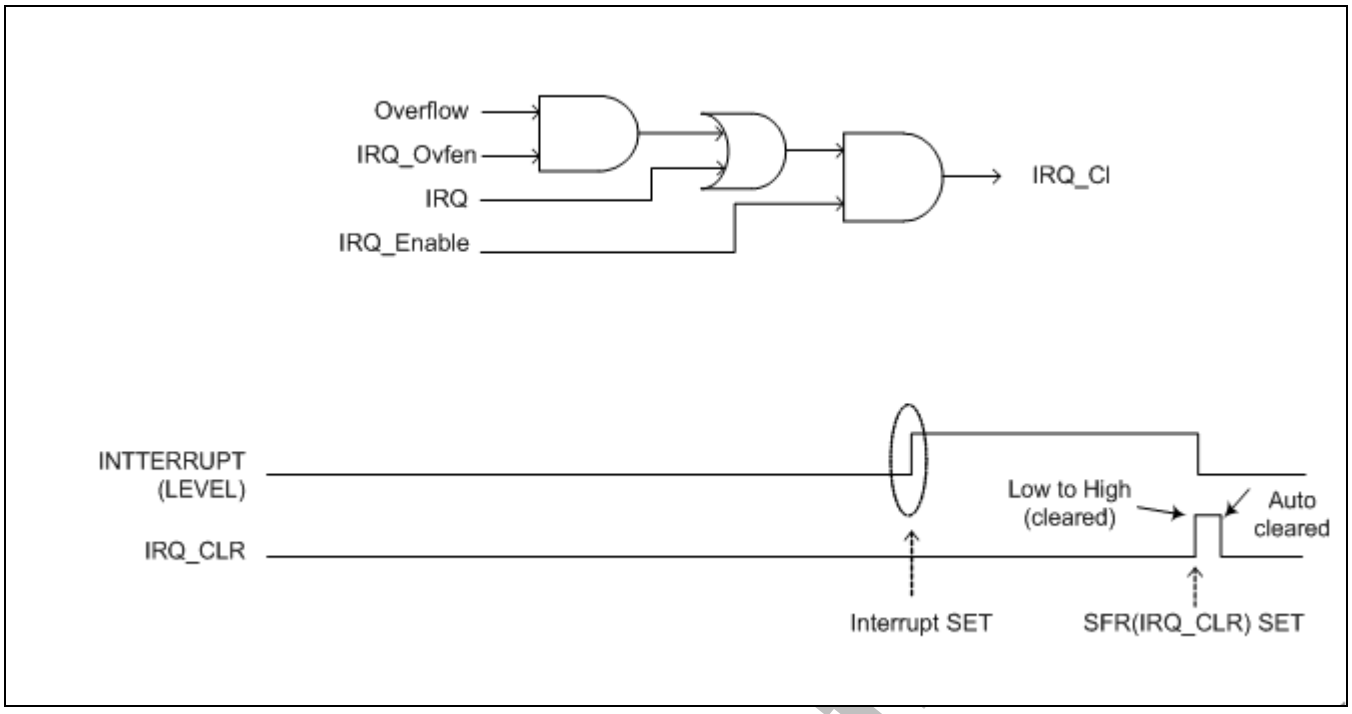

Figure 2-22 Interrupt Generation Scheme

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2.8.1.4 Window Offset Register 2 (CIWDOFST2n)

- CIWDOFST20, R/W, Address = 0xFB20_0014
- CIWDOFST21, R/W, Address = 0xFB30_0014
- CIWDOFST22, R/W, Address = 0xFB40_0014

CIWDOFST2n	Bit	Description	Initial State
Reserved	[31:28]	Reserved	0
WinHorOfst2	[27:16]	Specifies the window horizontal offset2 by pixel unit. It should be multiple of 2. Note) CAMIF0 & CAMIF2 : SourceHsize-WinHorOfst- WinHorOfst2 should be multiple of 16. (ML=XO)	0
Reserved	[15:12]	Reserved	0

WinVerOfst2	[11:0]	Specifies the window vertical offset2 by pixel unit. In case of interlaced input, this value should be 2's multiple. (ML=XO)	0

2.8.1.5 Output DMA Y1 Start Address Register (ClOYSA1n)

- ClOYSA10, R/W, Address = 0xFB20_0018
- ClOYSA11, R/W, Address = 0xFB30_0018
- ClOYSA12, R/W, Address = 0xFB40_0018

ClOYSA1n	Bit	Description	Initial State
ClOYSA1	[31:0]	Output format: YCbCr 2/3 plane → Y 1st frame start address Output format: YCbCr 1 plane → YCbCr 1st frame start address Output format: RGB → RGB 1st frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, ClOYSA1[11:0] should be 0x000. (ML=OX)	0

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2.8.1.6 Output DMA Y2 Start Address Register (CIOYSA2n)

- CIOYSA20, R/W, Address = 0xFB20_001C
- CIOYSA21, R/W, Address = 0xFB30_001C
- CIOYSA22, R/W, Address = 0xFB40_001C

CIOYSA2n	Bit	Description	Initial State
CIOYSA2	[31:0]	Output format: YCbCr 2/3 plane → Y 2nd frame start address Output format: YCbCr 1 plane → YCbCr 2nd frame start address Output format: RGB → RGB 2nd frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

2.8.1.7 Output DMA Y3 Start Address Register (CIOYSA3n)

- CIOYSA30, R/W, Address = 0xFB20_0020
- CIOYSA31, R/W, Address = 0xFB30_0020
- CIOYSA32, R/W, Address = 0xFB40_0020

CIOYSA3n	Bit	Description	Initial State
CIOYSA3	[31:0]	Output format: YCbCr 2/3 plane → Y 3rd frame start address Output format: YCbCr 1 plane → YCbCr 3rd frame start address Output format: RGB → RGB 3rd frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

2.8.1.8 Output DMA Y4 Start Address Register (CIOYSA4n)

- CIOYSA40, R/W, Address = 0xFB20_0024
- CIOYSA41, R/W, Address = 0xFB30_0024
- CIOYSA42, R/W, Address = 0xFB40_0024

CIOYSA4n	Bit	Description	Initial State
CIOYSA4	[31:0]	Output format: YCbCr 2/3 plane → Y 4th frame start address Output format: YCbCr 1 plane → YCbCr 4th frame start address Output format: RGB → RGB 4th frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

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2.8.1.9 Output DMA Cb1 Start Address Register (CIOCBSA1n)

- CIOCBSA10, R/W, Address = 0xFB20_0028
- CIOCBSA11, R/W, Address = 0xFB30_0028
- CIOCBSA12, R/W, Address = 0xFB40_0028

CIOCBSA1n	Bit	Description	Initial State
CIOCBSA1	[31:0]	Output format: YCbCr 3 plane → Cb 1st frame start address Output format: YCbCr 2 plane → CbCr 1st frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

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2.8.1.10 Output DMA Cb2 Start Address Register (CIOCBSA2n)

- CIOCBSA20, R/W, Address = 0xFB20_002C
- CIOCBSA21, R/W, Address = 0xFB30_002C
- CIOCBSA22, R/W, Address = 0xFB40_002C

CIOCBSA2n	Bit	Description	Initial State
CIOCBSA2	[31:0]	Output format: YCbCr 3 plane → Cb 2nd frame start address Output format: YCbCr 2 plane → CbCr 2nd frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

2.8.1.11 Output DMA Cb3 Start Address Register (CIOCBSA3n)

- CIOCBSA30, R/W, Address = 0xFB20_0030
- CIOCBSA31, R/W, Address = 0xFB30_0030
- CIOCBSA32, R/W, Address = 0xFB40_0030

CIOCBSA3n	Bit	Description	Initial State
CIOCBSA3	[31:0]	Output format: YCbCr 3 plane → Cb 3rd frame start address Output format: YCbCr 2 plane → CbCr 3rd frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

2.8.1.12 Output DMA Cb4 Start Address Register (CIOCBSA4n)

- CIOCBSA40, R/W, Address = 0xFB20_0034
- CIOCBSA41, R/W, Address = 0xFB30_0034
- CIOCBSA42, R/W, Address = 0xFB40_0034

CIOCBSA4n	Bit	Description	Initial State
CIOCBSA4	[31:0]	Output format: YCbCr 3 plane → Cb 4th frame start address Output format: YCbCr 2 plane → CbCr 4th frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

2.8.1.13 Output DMA Cr1 Start Address Register (CIOCRSA1n)

- CIOCRSA10, R/W, Address = 0xFB20_0038

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- CIOCRSA11, R/W, Address = 0xFB30_0038
- CIOCRSA12, R/W, Address = 0xFB40_0038

CIOCRSA1n	Bit	Description	Initial State
CIOCRSA1	[31:0]	Output format: YCbCr 3 plane → Cr 1st frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

2.8.1.14 Output DMA Cr2 Start Address Register (CIOCRSA2n)

- CIOCRSA20, R/W, Address = 0xFB20_003C
- CIOCRSA21, R/W, Address = 0xFB30_003C
- CIOCRSA22, R/W, Address = 0xFB40_003C

CIOCRSA2n	Bit	Description	Initial State
CIOCRSA2	[31:0]	Output format: YCbCr 3 plane → Cr 2nd frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

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2.8.1.15 Output DMA Cr3 Start Address Register (CIOCRSA3n)

- CIOCRSA30, R/W, Address = 0xFB20_0040
- CIOCRSA31, R/W, Address = 0xFB30_0040
- CIOCRSA32, R/W, Address = 0xFB40_0040

CIOCRSA3n	Bit	Description	Initial State
CIOCRSA3	[31:0]	Output format: YCbCr 3 plane → Cr 3rd frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

2.8.1.16 Output DMA Cr4 Start Address Register (CIOCRSA4n)

- CIOCRSA40, R/W, Address = 0xFB20_0044
- CIOCRSA41, R/W, Address = 0xFB30_0044
- CIOCRSA42, R/W, Address = 0xFB40_0044

CIOCRSA4n	Bit	Description	Initial State
CIOCRSA4	[31:0]	Output format: YCbCr 3 plane → Cr 4th frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

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2.8.1.17 Target Format Register (CITRGFMTn)

- CITRGFMT0, R/W, Address = 0xFB20_0048
- CITRGFMT1, R/W, Address = 0xFB30_0048
- CITRGFMT2, R/W, Address = 0xFB40_0048

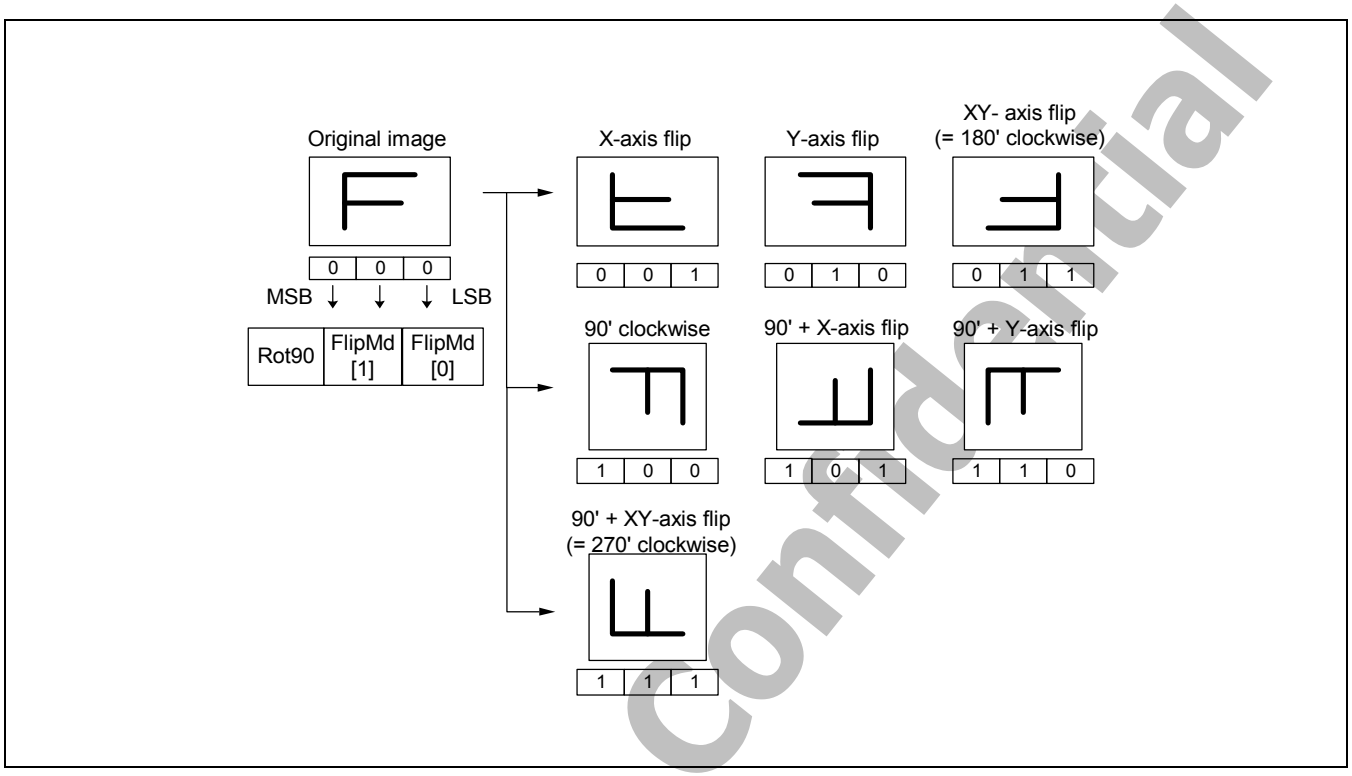

Figure 2-23 Image Mirror and Rotation

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CITRGFMTn	Bit	Description	Initial State
InRot90	[31]	1 = Rotate clockwise 90° (Using the Input Rotator only). Input Rotator and Output Rotator do not work at the same time. If InRot90 mode is enabled, then output data path should be LCD FIFO path.) 0 = Input Rotator bypass (ML=OO)	0
OutFormat	[30:29]	00 = YCbCr 4:2:0 output image format (2 or 3 plane) 01 = YCbCr 4:2:2 output image format (2 or 3 plane) (ref. 2 or 3 plane format register → C_INT_OUT) 10 = YCbCr 4:2:2 output image format (1 plane) 11 = RGB output image format (Ref. RGB format register → OutRGB_FMT). Note: Refer to gathering extension register for format YCbCr444. (ML=OO)	0
TargetHsize	[28:16]	Specifies the horizontal pixel number of target image. Refer to gathering extension register (TargetHsize_ext). Note.) CAMIF0 and CAMIF2 : In case of output DMA, TargetHsize should be multiple of 16. CAMIF1 : In case of interlaced output DMA and 90-degree-rotation, TargetVsize should be more than 16 (ML=OO)	0
OutFlipMd	[15:14]	Specifies image mirror and rotation for output DMA. 00 = Normal 01 = X-axis mirror 10 = Y-axis mirror 11 = 180° rotation Note) User cannot use this function, If input format is among CAM_JPEG or MIPI RAW or MIPI User-defined format. (ML=OO)	0
OutRot90	[13]	1 = Rotate clockwise 90° (Using the Output Rotator) 0 = Output Rotator bypass Note) User cannot use this function, If input format is among CAM_JPEG or MIPI RAW or MIPI User-defined format. (ML=OO)	0

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CITRGFMTn	Bit	Description	Initial State
TargetVsize	[12:0]	Specifies vertical pixel number of target image. The minimum number is 4. Refer to gathering extension register (TargetVsize_ext). CAMIF0 and CAMIF2 : In case of output DMA and 90-degree-rotation, TargetVsize should be multiple of 16. In case of interlaced output DMA and 90-degree-rotation, TargetVsize should be multiple of 32. CAMIF1 In case of interlaced output DMA and 90-degree-rotation, TargetVsize should be more than 32. (ML=OO)	0

TargetHsize and TargetVsize should not be larger than Camera SourceHsize and Camera SourceVsize. InputDMA source size does not care.

Caution: Only input rotator supports InputDMA image data. The output rotator supports Camera or InputDMA image data. Input and output rotators should not work at the same time because input and output rotator memories are shared for saving the memory size.

NOTE: If the TargetVsize value is set to an odd number (N) when output format is YCbCr 4:2:0, the odd numbers (N) of Y lines and (N-1)/2 of Cb, Cr lines are generated. Also, X-flip or XY-flip is not allowed. Thus, YCbCr 4:2:0 output format should use an even TargetVsize number.

NOTE: If TargetVsize value cannot be divided by 4 (4n+1,4n+2,4n+3) when output format is YCbCr 4:2:0 and Interlaced out, The odd number(N) of Y lines and the (N-1)/2 of Cb, Cr lines are generated. Also, X-flip or XY-flip are not allowed. Thus YCbCr 4:2:0 ouput format and Interlaced out should use 4's multiple TargetVsize number.

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2.8.1.18 Output DMA Control Register (CIOCTRLn)

- CIOCTRL0, R/W, Address = 0xFB20_004C
- CIOCTRL1, R/W, Address = 0xFB30_004C
- CIOCTRL2, R/W, Address = 0xFB40_004C

<table>
<tr><th>CIOCTRLn</th><th>Bit</th><th>Description</th><th>Initial State</th></tr>
<tr><td>Weave_out</td><td>[31]</td><td>Even and Odd fields can be weaved together and combined to form a complete progressive frame by hardware. This field is useful for interlace DMA output mode (Interlace_out or CAM_INTERLACE). Even field address (1st frame start address) is used weave address. Odd fields address (2nd frame start address) is ignored.
1 = Weave
2 = Normal
(ML=0X)</td><td>0</td></tr>
<tr><td>Reserved</td><td>[30:26]</td><td>Reserved</td><td>0</td></tr>
<tr><td>Order2p_out</td><td>[25:24]</td><td>Specifies YCbCr 4:2:0 or 4:2:2 2plane output Chroma memory storing style order (should be C_INT_OUT = 1).
<table>
<tr><td>bit</td><td>MSB LSB</td></tr>
<tr><td>00</td><td>Cr3Cb3Cr2Cb2Cr1Cb1Cr0Cb0</td></tr>
<tr><td>01</td><td>Cb3Cr3Cb2Cr2Cb1Cr1Cb0Cr0</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table>
(ML=OO)</td><td>0</td></tr>
<tr><td>Reserved</td><td>[23:4]</td><td>Reserved</td><td>0</td></tr>
<tr><td>C_INT_OUT</td><td>[3]</td><td>1 = YCbCr 4:2:0 or 4:2:2 2plane output format
0 = YCbCr 4:2:0 or 4:2:2 3plane output format
(ML=OO)</td><td>0</td></tr>
<tr><td>LastIRQEn</td><td>[2]</td><td>1 = enables last IRQ at the end of frame capture (It is recommended to check the done signal of capturing image for JPEG)
0 = normal
(ML=XX)</td><td>0</td></tr>
<tr><td>Order422_out</td><td>[1:0]</td><td>Specifies YCbCr 4:2:2 1plane output memory storing style order.
<table>
<tr><td>bit</td><td>MSB LSB</td></tr>
<tr><td>00</td><td>Cr1Y3Cb1Y2Cr0Y1Cb0Y0</td></tr>
<tr><td>01</td><td>Cb1Y3Cr1Y2Cb0Y1Cr0Y0</td></tr>
<tr><td>10</td><td>Y3Cr1Y2Cb1Y1Cr0Y0Cb0</td></tr>
<tr><td>11</td><td>Y3Cb1Y2Cr1Y1Cb0Y0Cr0</td></tr>
</table>
(ML=OO)</td><td>0</td></tr>
</table>

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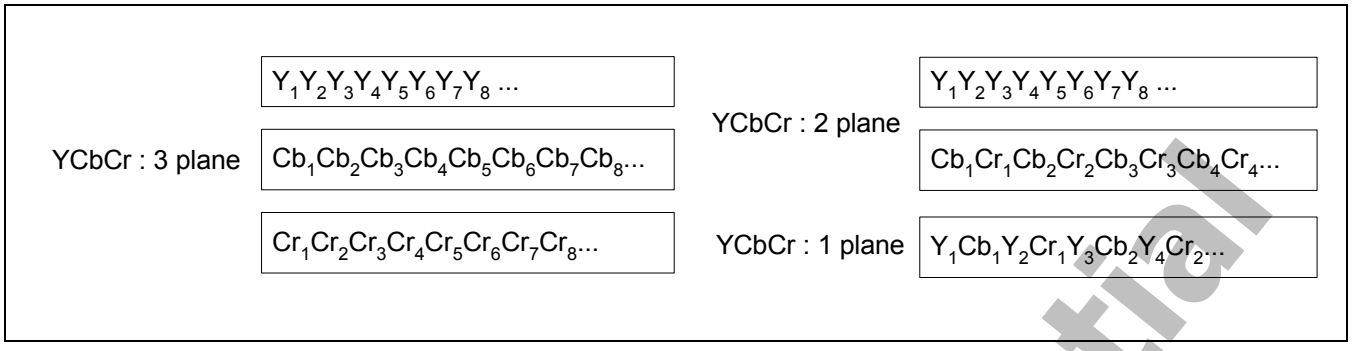

Figure 2-24 YCbCr Plane Memory Storing Style

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2.8.2 REGISTER SETTING GUIDE FOR SCALER

SRC_Width and DST_Width satisfy the double word (8-bytes) boundary constraints such that the number of horizontal pixel represents kn, where n = 1, 2, 3 … and k = 1/ 2/ 8 for 24bpp RGB/ 16bpp RGB/ YCbCr420 image.

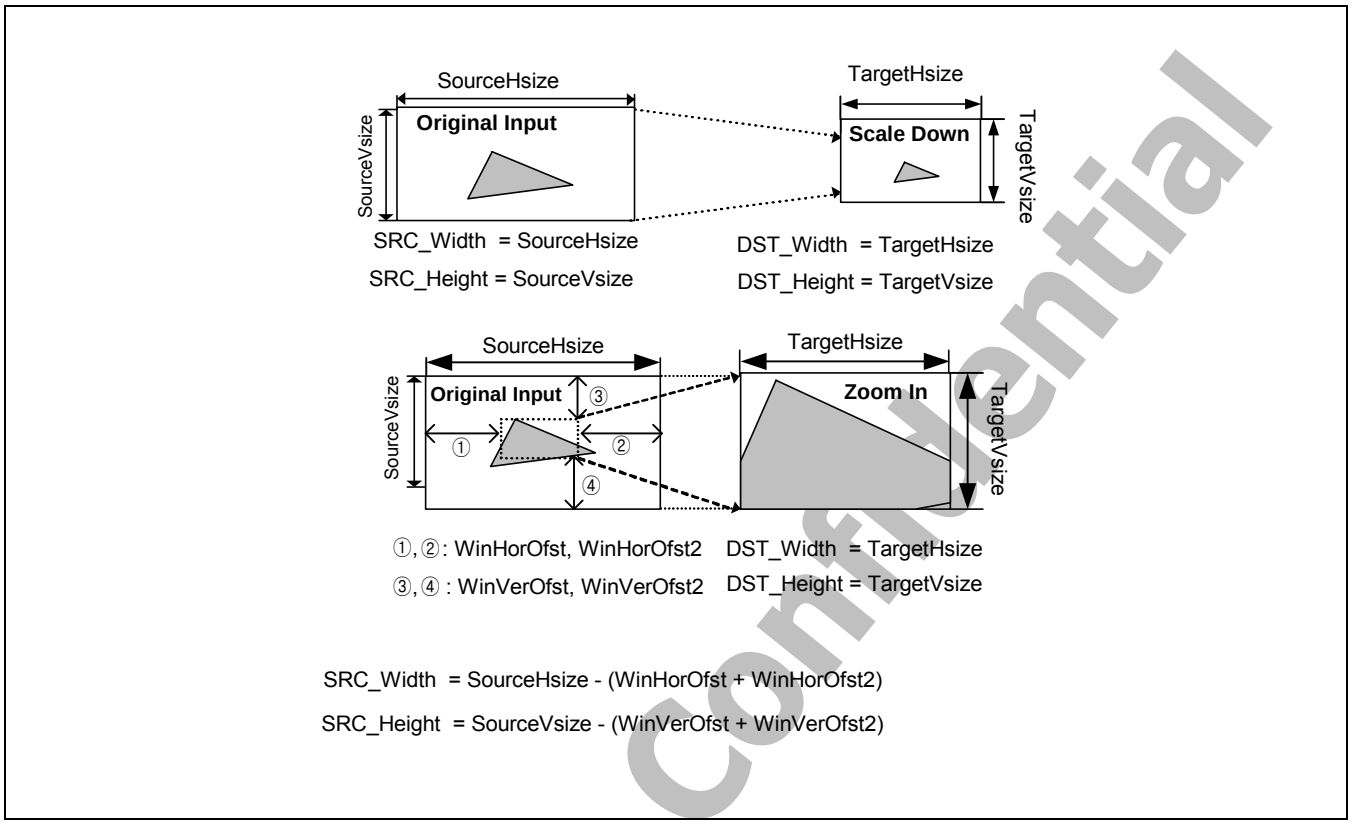

Figure 2-25 Scaling Scheme

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The other control registers of pre-scaled image size, pre-scale ratio, pre-scale shift ratio, and main scale ratio are defined according to the following equations:

- If (SRC_Width >= 64 × DST_Width) { Exit(-1); /* Out Of Horizontal Scale Range */ }
  else if (SRC_Width >= 32 × DST_Width) { PreHorRatio = 32; H_Shift = 5 }
  else if (SRC_Width >= 16 × DST_Width) { PreHorRatio = 16; H_Shift = 4 }
  else if (SRC_Width >= 8 × DST_Width) { PreHorRatio = 8; H_Shift = 3 }
  else if (SRC_Width >= 4 × DST_Width) { PreHorRatio = 4; H_Shift = 2 }
  else if (SRC_Width >= 2 × DST_Width) { PreHorRatio = 2; H_Shift = 1 }
  else { PreHorRatio = 1; H_Shift = 0 }

  PreDstWidth = SRC_Width / PreHorRatio

CAMIF0 & CAMIF2	MainHorRatio = (SRC_Width << 8) / (DST_Width << H_Shift)
CAMIF1	MainHorRatio = (SRC_Width << 14) / (DST_Width << H_Shift)

- If (SRC_Height >= 64 × DST_Height) { Exit(-1); /* Out Of Vertical Scale Range */ }
  else if (SRC_Height >= 32 × DST_Height) { PreVerRatio = 32; V_Shift = 5 }
  else if (SRC_Height >= 16 × DST_Height) { PreVerRatio = 16; V_Shift = 4 }
  else if (SRC_Height >= 8 × DST_Height) { PreVerRatio = 8; V_Shift = 3 }
  else if (SRC_Height >= 4 × DST_Height) { PreVerRatio = 4; V_Shift = 2 }
  else if (SRC_Height >= 2 × DST_Height) { PreVerRatio = 2; V_Shift = 1 }
  else { PreVerRatio = 1; V_Shift = 0 }

  PreDstHeight = SRC_Height / PreVerRatio

CAMIF0 & CAMIF2	MainVerRatio = (SRC_Height << 8) / (DST_Height << V_Shift)
CAMIF1	MainVerRatio = (SRC_Height <<14) / (DST_Height << V_Shift)

SHfactor = 10 – (H_Shift + V_Shift)

Caution: In case of Zoom-in, you should check the next equation (CAM-In case).
((SourceHsize - (WinHorOfst + WinHorOfst2)) / PreHorRatio) ≤ Max. scaler line buffer size width

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2.8.2.1 Pre-Scaler Control Register 1 (CISCPRERATIOn)

- CISCPRERATIO0, R/W, Address = 0xFB20_0050
- CISCPRERATIO1, R/W, Address = 0xFB30_0050
- CISCPRERATIO2, R/W, Address = 0xFB40_0050

CISCPRERATIOn	Bit	Description	Initial State
SHfactor	[31:28]	Specifies the shift factor for pre-scaler. (ML=OO)	0
Reserved	[27:23]	Reserved	0
PreHorRatio	[22:16]	Specifies the horizontal ratio of pre-scaler. (ML=OO)	0
Reserved	[15:7]	Reserved	0
PreVerRatio	[6:0]	Specifies the vertical ratio of pre-scaler. (ML=OO)	0

2.8.2.2 Pre-Scaler Control Register 2 (CISCPREDSTn)

- CISCPREDST0, R/W, Address = 0xFB20_0054
- CISCPREDST1, R/W, Address = 0xFB30_0054
- CISCPREDST2, R/W, Address = 0xFB40_0054

CISCPREDSTn	Bit	Description	Initial State
Reserved	[31:30]	Reserved	0
PreDstWidth	[29:16]	Specifies the destination width for pre-scaler. (ML=OO)	0
Reserved	[15:14]	Reserved	0
PreDstHeight	[13:0]	Specifies the destination height for pre-scaler. (ML=OO)	0

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2.8.2.3 Main-Scaler Control Register (CISCCTRLn)

- CISCCTRL0, R/W, Address = 0xFB20_0058
- CISCCTRL1, R/W, Address = 0xFB30_0058
- CISCCTRL2, R/W, Address = 0xFB40_0058

CISCCTRLn	Bit	Description	Initial State
ScalerBypass	[31]	Specifies scaler bypass. In this case, ImgCptEn_SC should be 0, but ImgCptEn should be 1. Generally, this mode is used to handle a large image whose size is greater than the maximum size of scaler. (This mode is intended to capture the JPEG input image for DSC application). In this case, the input pixel buffering depends on only the input FIFOs; therefore, the system bus should not be busy in this mode. ScalerBypass has certain restrictions. For instance, size scaling, color space conversion, input DMA mode, Write Back mode and RGB format are not allowed. If input format is YCbCr4:2:2, the output format should also be YCbCr4:2:2 or YCbCr4:2:0. (ML=XX)	0
ScaleUp_H	[30]	Specifies horizontal scale up/ down flag for scaler (In 1:1 scale ratio, this bit should be “1”.) 1 = Up 0 = Down (ML=OO)	0
ScaleUp_V	[29]	Specifies vertical scale up/down flag for scaler (In 1:1 scale ratio, this bit should be “1”.) 1 = Up 0 = Down (ML=OO)	0
CSCR2Y	[28]	Selects YCbCr data dynamic range for color space conversion from RGB to YCbCr. 1 = Wide => Y/Cb/Cr (0 ~ 255): Wide default 0 = Narrow => Y (16 ~ 235), Cb/Cr (16 ~ 240) ※ Recommended CSC range setting CSCR2Y= CSCY2R (Wide=Wide or Narrow=Narrow) (ML=OO)	1
CSCY2R	[27]	Specifies YCbCr data dynamic range selection for the color space conversion from YCbCr to RGB. 1 = Wide => Y/Cb/Cr (0 ~ 255): Wide default 0 = Narrow => Y (16 ~ 235), Cb/Cr (16 ~ 240) (ML=OO)	1
LCDPathEn	[26]	Enables FIFO mode. 1 = Enables for FIFO output 0 = Enables for DMA output.	0

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CISCCTRLn	Bit	Description	Initial State
		If FIFO mode is enabled, then the input mode should be DMA input and WSWP bit at WINCON0(0xF800_0020) in LCD controller should be '0'. The FIFO mode output format is YCbCr4;4:4 3 Plane or RGB 24-bit. Its selection depends on OutFormat register. OutFormat = RGB → RGB24bit. Other setting means YCbCr4:4:4. If interlace out end DMA input want to set together, Output mode should be FIFO output (ML=OO)	
Interlace	[25]	Output scan method selection register. (RAW and JPEG input formats are not available) 1 : Interlace scan out (Input data should be progressive mode) 0 : progressive scan out Note) If this bit is configured by 0 for interlacced input, the output is also interlaced format not converted into progressive one. (ML=OX)	0
MainHorRatio	[24:16]	Specifies horizontal scale ratio for main-scaler. Note) CAMIF1 : Refer to the gathering extension register(MainHorRatio_ext). (ML=OO)	0
ScalerStart	[15]	Specifies the Scaler start. 1 = Scaler start 0 = Scaler stop or scaler bypass (ML=OO)	0
InRGB_FMT	[14:13]	Specifies input DMA RGB format. 00 = RGB565, 01 = RGB666 10 = RGB888, 11 = Reserved (ML=OX)	0
OutRGB_FMT	[12:11]	Specifies output DMA RGB format. 00 = RGB565 01 = RGB666 10 = RGB888 11 = Reserved (ML=OO)	0
Ext_RGB	[10]	Specifies input RGB data extension enable bit for conversion of RGB565/666 mode to RGB888 mode. 1 = Extension 0 = normal i) Input R = 5-bit in RGB565 mode 10100 -> 10100101 (Extension): [7]=[2], [6]=[1], [5]=[0] 10100 -> 10100000 (Normal) ii) Input R = 6-bit in RGB666 mode	0

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CISCCTRLn	Bit	Description	Initial State
		101100 -> 10110010 (Extension): [7]=[1], [6]=[0] 101100 -> 10110000 (Normal) (ML=OO)	
One2One	[9]	Scaler does not run interpolation, but runs repetition for upsampling. Sometimes other IP needs this method if input format are YCbCr4:2:0 and YCbCr4:2:2. Scalerbypass should be set to '0' and don't care plane. Caution!: One2One should be used if input/ output format and size are same. One2One function has size constraints, as described in Table 9.2-1. For example: input YCbCr4:2:0 2plane -> output YCbCr4:2:0 3plane (O.K) (ML=OO)	0
MainVerRatio	[8:0]	Specifies vertical scale ratio for main-scaler. Note) CAMIF1 : Refer to the gathering extension register(MainVerRatio_ext) (ML=OO)	0

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Table 2-6 Color Space Conversion Equations

	Wide	Narrow
CSCY2R (601)	R = Y + 1.371(Cr-128) G = Y – 0.698(Cr-128) – 0.336(Cb-128) B = Y + 1.732(Cb-128)	R = 1.164(Y-16) + 1.596(Cr-128) G = 1.164(Y-16) – 0.813(Cr-128) – 0.391(Cb-128) B = 1.164(Y-16) + 2.018(Cb-128)
CSCY2R (709)	R = Y + 1.540(Cr-128) G = Y – 0.459(Cr-128) – 0.183(Cb-128) B = Y + 1.816(Cb-128)	R = 1.164(Y-16) + 1.793(Cr-128) G = 1.164(Y-16) – 0.534(Cr-128) – 0.213(Cb-128) B = 1.164(Y-16) + 2.115(Cb-128)
CSCR2Y (601)	Y = 0.299R + 0.587G + 0.114B Cb = – 0.172R – 0.339G + 0.511B +128 Cr = 0.511R – 0.428G – 0.083B + 128	Y = 0.257R + 0.504G + 0.098B + 16 Cb = – 0.148R – 0.291G + 0.439B + 128 Cr = 0.439R – 0.368G – 0.071B +128
CSCR2Y (709)	Y = 0.213R + 0.715G + 0.072B Cb = – 0.117R – 0.394G + 0.511B +128 Cr = 0.511R – 0.464G – 0.047B + 128	Y = 0.183R + 0.614G + 0.062B + 16 Cb = – 0.101R – 0.338G + 0.439B + 128 Cr = 0.439R – 0.399G – 0.040B +128

DMA Mode Operation (Normal mode): DMA Input → DMA Output

The source image format is in one of the following formats: YCbCr420, YCbCr422, YCbCr444 and RGB16-/ 18-/ 24-bit. On the other hand, the destination image format is in one of the following ones: YCbCr420, YCbCr422, YCbCr444 and RGB 16-/18-/24-bit. (Input and output format are possible for both Progressive and Interlace format).

All source and destination image data need to be stored in memory system aligned with double word boundary and should support DMA operation. Therefore, the width of source and destination image should satisfy the double word boundary condition.

FIFO Mode Operation: DMA Input → FIFO Output

In FIFO Mode, (LCDPathEn =1), two types of color space conversion are available such as RGB2YCbCr and YCbCr2RGB. This is similar to DMA mode operation. The destination image is transferred to FIFO in display controller (or some other IP with FIFO interface) without additional memory bandwidth such as CAMIF-to-Memory and Memory-to-Display Controller. Output data format is determined only by Output format register: OutFormat = RGB format (24-bit RGB) or OutFormat=YCbCr format(YCbCr444). The source image format and destination image format restrictions are described in the table below.

Table 2-7 FIFO Mode Image Format

<table>
<tr><th colspan="2">DMA input (Progressive / Interlace)</th><th>FIFO output (Progressive / Interlace)</th></tr>
<tr><td rowspan="3">YCbCr</td><td>YCbCr420: 3/2 plane</td><td rowspan="4">YCbCr 444 3 plane
or
RGB 24-bit</td></tr>
<tr><td>YCbCr422: 3/2/1 plane</td></tr>
<tr><td>YCbCr444: 3/2 plane</td></tr>
<tr><td>RGB</td><td>RGB 16-/ 18-/ 24-bit</td></tr>
</table>

In FIFO mode (LCDPathEnable =1), you can either select progressive or interlace scan mode based on the

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“interlace” control register, Register Files Lists.

The “interlace” control bit is available if LCDPathEn=1, otherwise its value is unaffected by DMA mode operation, which supports only progressive scan mode. Even if an interlaced scan mode is enabled (LCDPathEn = 1 and Interlace = 1), per frame management, which consists of even field and odd filed, is automatic. This means that user interruption is unnecessary to interfield switching in the same frame. Therefore, the frame management scheme is identical for both progressive and interlaced scan modes. Interlace is not supported if camera processor selects the input data

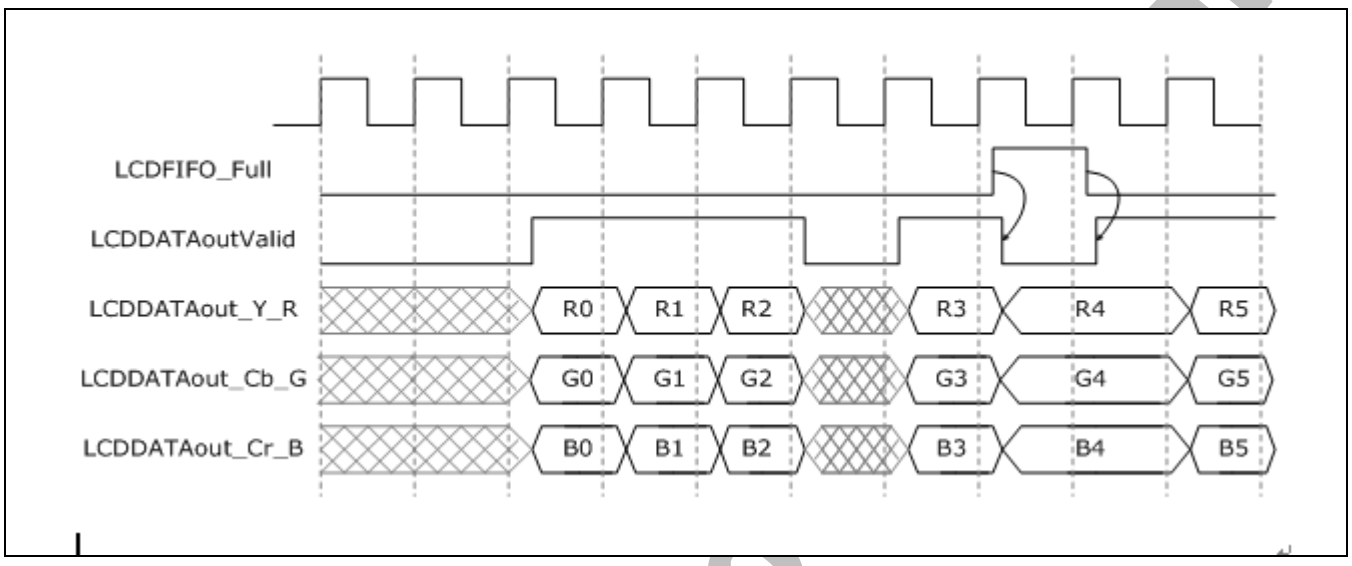

Figure 2-26 I/O Timing Diagram for Direct Path

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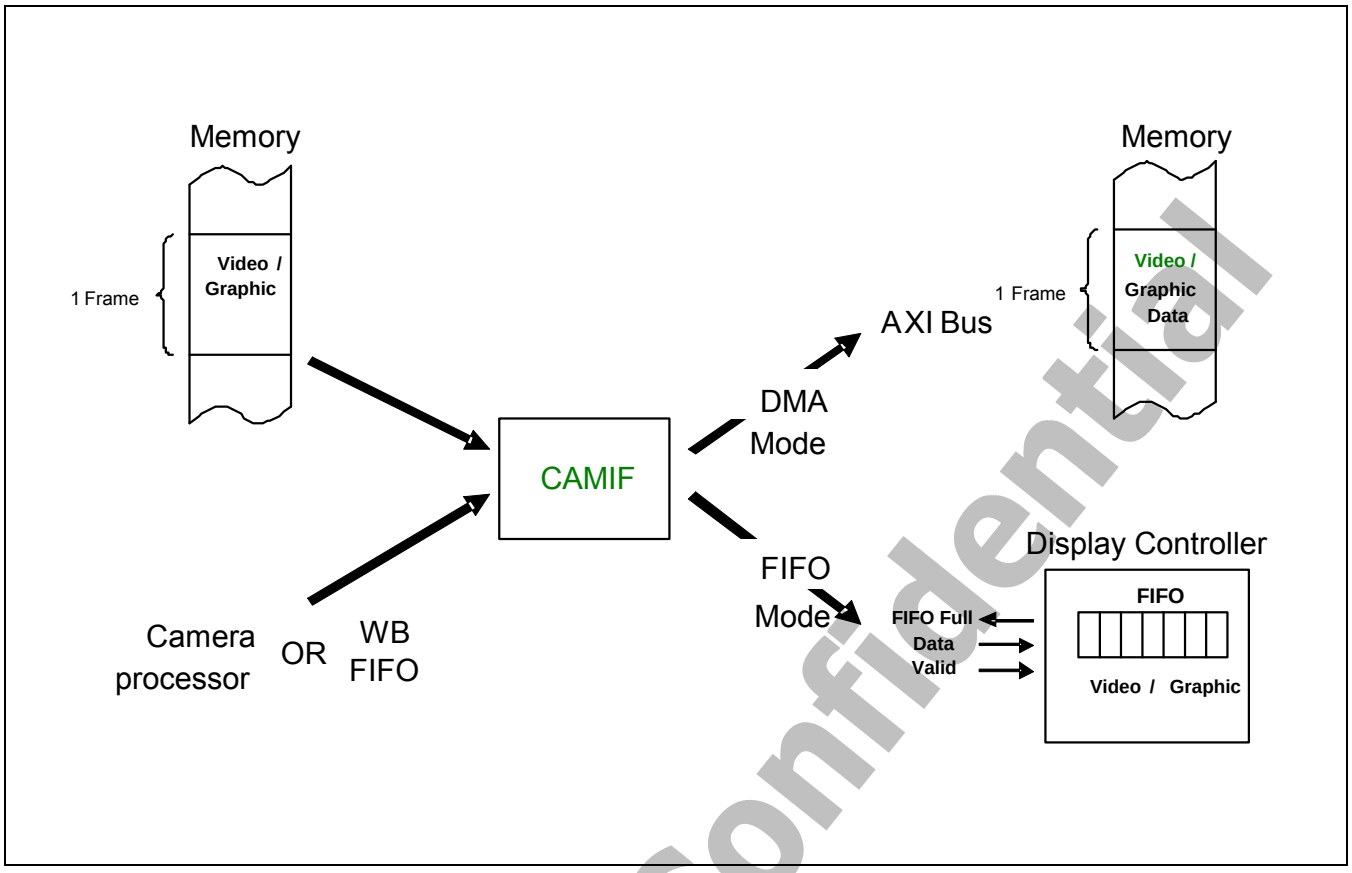

Figure 2-27 Input & Output Modes in CAMIF

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2.8.2.4 Output DMA Target Area Register (CITAREAn)

- CITAREA0, R/W, Address = 0xFB20_005C
- CITAREA1, R/W, Address = 0xFB30_005C
- CITAREA2, R/W, Address = 0xFB40_005C

CITAREAn	Bit	Description	Initial State
Reserved	[31:28]	Reserved	0
CITAREA	[27:0]	Specifies target area for output DMA = Target H size x Target V size. (ML=OO)	0

2.8.2.5 Output DMA Line Skip Register (CIOLINESKIPn)

- CIOLINESKIP0, R/W, Address = 0xFB20_0060
- CIOLINESKIP1, R/W, Address = 0xFB30_0060
- CIOLINESKIP2, R/W, Address = 0xFB40_0060

CIOLINESKIPn	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
OLINESKIP_Cr	[23:20]	Specifies Cr Line skip for output DMA. If OLINESKIP_Cr is k, Cr Line is stored in every k+1 line. Note) Maximum value can be 8 (ML=OO)	0
Reserved	[19:14]	Reserved	0
OLINESKIP_Cb	[13:10]	Specifies Cb Line skip for output DMA. If OLINESKIP_Cb is k, Cb Line is stored in every k+1 line. Note) Maximum value can be 8 (ML=OO)	0
Reserved	[9:4]	Reserved	0
OLINESKIP_Y	[3:0]	Specifies Y Line skip for output DMA. If OLINESKIP_Y is k, Y Line is stored in every k+1 line. Note) Maximum value can be 8 (ML=OO)	0

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2.8.2.6 Status Register (CISTATUSn)

- CISTATUS0, Address = 0xFB20_0064
- CISTATUS1, Address = 0xFB30_0064
- CISTATUS2, Address = 0xFB40_0064

CISTATUSn	Bit	Description	RW	Initial State
OvFiY	[31]	Specifies overflow state of FIFO Y. (ML=XX)	R	0
OvFiCb	[30]	Specifies overflow state of FIFO Cb. (ML=XX)	R	0
OvFiCr	[29]	Specifies overflow state of FIFO Cr. (ML=XX)	R	0
VSYNC	[28]	Specifies camera VSYNC (CPU refers this bit for first SFR setting after external camera muxing. It is seen in the ITU-R BT 656 mode). (ML=XX)	R	0
FrameCnt	[27:26]	Specifies frame count of output DMA. This counter value specifies the next frame number. (ML=XX)	R	0
WinOfstEn	[25]	Specifies window offset enable status. (ML=XX)	R	0
FlipMd	[24:23]	Specifies flip mode of output DMA. (ML=XX)	R	0
ImgCptEn	[22]	Specifies image capture enable of global camera interface. (ML=XX)	R	0
ImgCptEn_SC	[21]	Specifies image capture enable of scaler path. (ML=XX)	R	0
VSYNC_A	[20]	Specifies external camera A VSYNC. Polarity inversion is not adopted. (ML=XX)	R	X
VSYNC_B	[19]	Specifies external camera B VSYNC. Polarity inversion is not adopted. (ML=XX)	R	X
OvRLB	[18]	Specifies overflow status of line buffer for rotation. (ML=XX)	R	0
FrameEnd	[17]	If the frame operation finishes, then FrameEnd is generated and FrameEnd is cleared by setting ‘0’. (ML=XX)	R/W	0
LastCaptureEnd	[16]	Specifies last frame capture status. LastCaptureEnd is cleared by setting ‘0’. This signal is applied only by camera input mode. (ML=XX)	R/W	0

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CISTATUSn	Bit	Description	RW	Initial State
VVALID_A	[15]	Specifies external camera A VVALID. (ML=XX)	R	X
VVALID_B	[14]	Specifies external camera B VVALID. (ML=XX)	R	X
IRQ_CAM	[13]	Specifies interrupt status for camera input mode. (ML=XX)	R	0
IRQ_DMAend	[12]	Specifies interrupt status for DMA frame end in DMA input mode. (ML=XX)	R	0
FrameCptStatus	[11]	Specifies capture frame control status. 1 = Enables present capture 0 = Disables present capture (ML=XX)	R	0
FrameFieldStatus	[10]	Specifies ITU camera field status and internal value after inverse polarity. 1 = Present frame Field1 0 = Present frame Field0 (ML=XX)	R	0
LCD_ENSTATUS	[9]	Specifies LCD controller enable status. 1 = Enables 0 = Disables (ML=XX)	R	0
ENVID_STATUS	[8]	Specifies Input DMA enable internal status. Sometimes this status is used to check whether the software completely clears ENVID bit or not. 1 = Enables Input DMA operation remain 0 = Disables Input DMA operation	R	
Reserved	[7:0]	Reserved	-	0

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2.8.2.7 Image Capture Enable Register (CIIMGCPTn)

- CIIMGCPT0, R/W, Address = 0xFB20_00C0
- CIIMGCPT1, R/W, Address = 0xFB30_00C0
- CIIMGCPT2, R/W, Address = 0xFB40_00C0

CIIMGCPTn	Bit	Description	Initial State
ImgCptEn	[31]	Enables camera interface global capture. (ML=XO)	0
ImgCptEn_Sc	[30]	Enables capture for scaler. This bit must be zero in scaler-bypass mode. (ML=OO)	0
Reserved	[29:26]	Reserved	0
Cpt_FrEn	[25]	Controls capture frame (only camera progressive input is applied). 1 = Enables (Step-by-Step frame one shot mode) 0 = Disables (FreeRun mode) Note) User should configure 0 for user-defined packet or CAM_JPEG mode. User should not change this bit under capture enable status. (ML=XO)	0
Reserved	[24]	Reserved	0
Cpt_FrPtr	[23:19]	Captures sequence turnaround pointer. (ML=XX)	0
Cpt_ FrMod	[18]	Captures frame control mode. 1 = Applies Cpt_FrCnt mode (Captures Cpt_FrCnt frames along Cpt_FrSeq, after enabling capture DMA frame control. If Cpt_FrCnt = 0, then capture ends.) 0 = Apply Cpt_FrEn mode (Captures frames along Cpt_FrSeq when Cpt_FrEn is high. This sequence repeats until capture frame control is disabled.) (ML=XX)	0
Cpt_ FrCnt	[17:10]	Specifies number of frames to be captured. If register reads, then you can see the value of a shadow register, which is downcounted if a frame is captured. In other words, Cpt_FrCnt has an initially loaded value after a frame is captured. Note) User have to disable and enable Cpt_FrEn register before starting CAMIF to use this (capture frame count) funciton (ML=XX)	0
Reserved	[9:0]	Reserved	0

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2.8.2.8 Capture Sequence Register (CICPTSEQn)

- CICPTSEQ0, R/W, Address = 0xFB20_00C4
- CICPTSEQ1, R/W, Address = 0xFB30_00C4
- CICPTSEQ2, R/W, Address = 0xFB40_00C4

CICPTSEQn	Bit	Description	Initial State
Cpt_FrSeq	[31:0]	Specifies capture sequence pattern. This register is valid if Cpt_FrEn has a high value. (ML=XX)	FFFF_FFFF

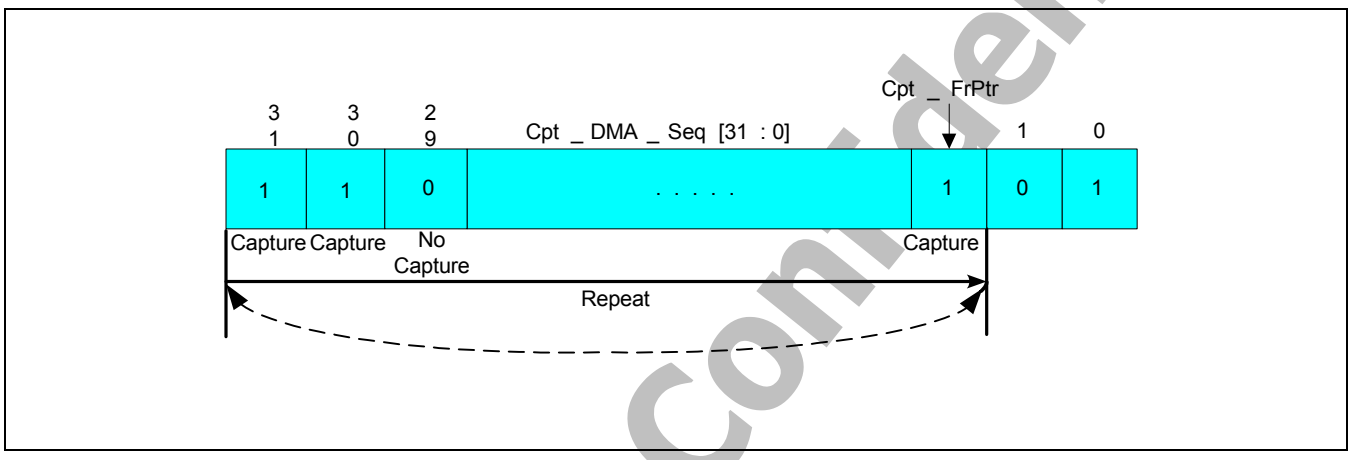

Figure 2-28 Capture Frame Control

※ For skipped frames, IRQ is not generated and FrameCnt is not increased.

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2.8.2.9 QoS Threshold Register (CITHOLDn)

- CITHOLD0, R/W, Address = 0xFB20_00C8
- CITHOLD1, R/W, Address = 0xFB30_00C8
- CITHOLD2, R/W, Address = 0xFB40_00C8

CITHOLDn	Bit	Description	Initial State
R_QoS_EN	[31]	1 : QoS Enable for Read DMA channel buffer 0 : QoS Disable for Read DMA channel buffer Read DMA QoS Enable and Write DMA QoS Enable cannot set simultaneously. Only one QoS Enable is possible. (ML=XO)	0
W_QoS_EN	[30]	1 : QoS Enable for Write DMA channel buffer 0 : QoS Disable for Write DMA channel buffer Read DMA QoS Enable and Write DMA QoS Enable cannot set simultaneously. Only one QoS Enable is possible. (ML=XO)	0
Reserved	[29:23]		0
RTh_QoS	[22:16]	Read buffer threshold register.(related Input DMA) If RTh_QoS >= Buffer write count, Read channel is generated no margin signal for bus high performance (ML=XO)	0
Reserved	[15:7]		0
WTh_QoS	[6:0]	Write buffer threshold register.(related Output DMA) If WTh_QoS < Buffer write count, Write channel is generated no margin signal for bus high performance (ML=XO)	0

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2.8.2.10 Image Effects Register (CIIMGEFFn)

- CIIMGEFF0, R/W, Address = 0xFB20_00D0
- CIIMGEFF1, R/W, Address = 0xFB30_00D0
- CIIMGEFF2, R/W, Address = 0xFB40_00D0

CIIMGEFFn	Bit	Description	Initial State
Reserved	[31]	Reserved	0
IE_ON	[30]	0 = Disables image effect function 1 = Enables image effect function (ML=OO)	0
IE_AFTER_SC	[29]	Specifies image effect location 1 = After scaling (camera, write back mode and input DMA image are applied except scaler bypass mode) 0 = Before scaling (only ITU camera image are applied) It applies image effect, even though it is in scaler bypass mode. (ML=OO)	0
FIN	[28:26]	Specifies image effect selection. 3'd0 = Bypass 3'd1 = Arbitrary Cb/Cr 3'd2 = Negative 3'd3 = Art Freeze 3'd4 = Embossing 3'd5 = Silhouette (ML=OO)	0
Reserved	[25:21]	Reserved	0
PAT_Cb	[20:13]	Used only for FIN is Arbitrary Cb/Cr (PAT_Cb/Cr == 8'd128 for Grayscale) Wide CSC Range: 0 < PAT_Cb < 255 Narrow CSC Range: 16 ≤ PAT_Cb ≤ 240 (ML=OO)	8'd128
Reserved	[12:8]	Reserved	0
PAT_Cr	[7:0]	Used only for FIN is Arbitrary Cb/Cr (PAT_Cb/Cr == 8'd128 for Grayscale) Wide CSC Range: 0 < PAT_Cr < 255 Narrow CSC Range: 16 ≤ PAT_Cr ≤ 240 (ML=OO)	8'd128

Cf) sepia: PAT_Cb = 8'd115, PAT_Cr = 8'd145

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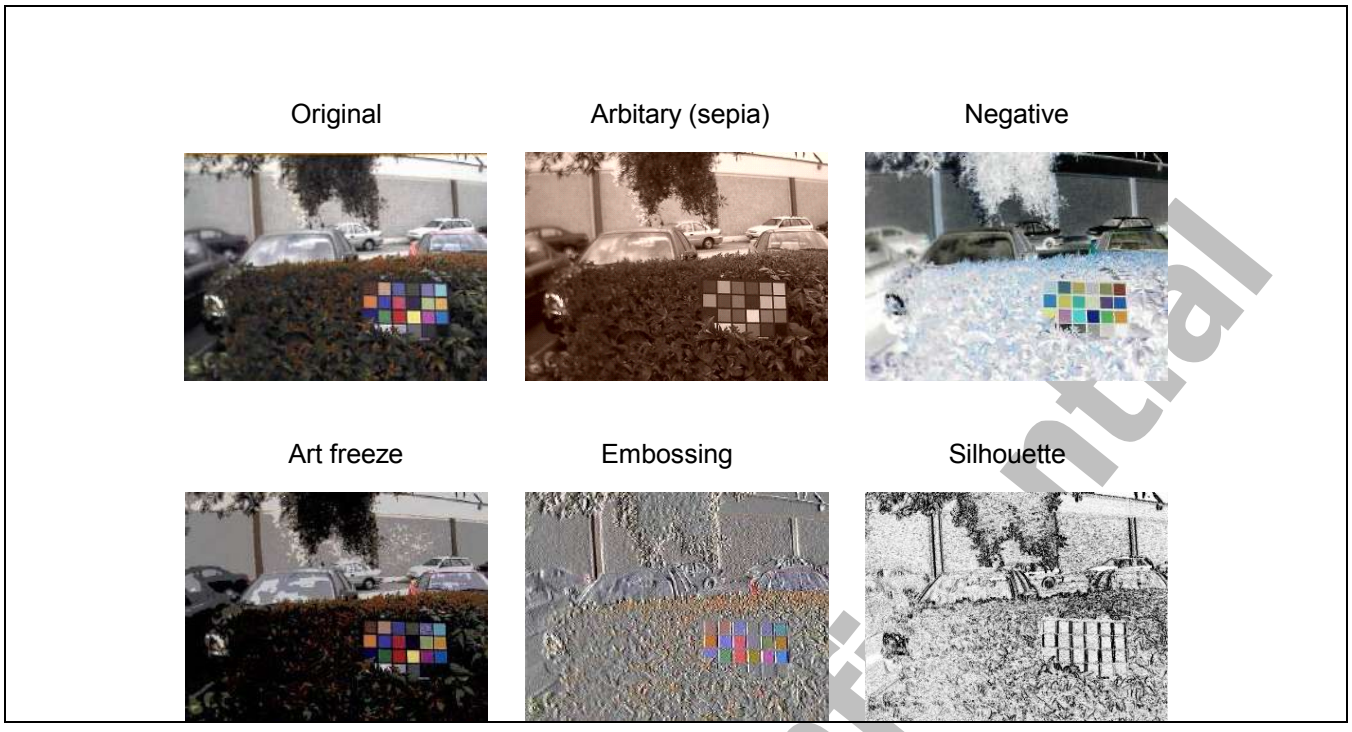

Figure 2-29 Image Effect

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2.8.2.11 Input DMA Y0 Start Register (CIIYSA0n)

- CIIYSA0, R/W, Address = 0xFB20_00D4
- CIIYSA1, R/W, Address = 0xFB30_00D4
- CIIYSA2, R/W, Address = 0xFB40_00D4

CIIYSA0n	Bit	Description	Initial State
CIIYSA0	[31:0]	Input format: YCbCr 2/3 plane → Y frame start address Input format: YCbCr 1 plane → YCbCr frame start address Input format: RGB → RGB frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

2.8.2.12 Input DMA Cb0 Start Register (CIICBSA0n)

- CIICBSA00, R/W, Address = 0xFB20_00D8
- CIICBSA01, R/W, Address = 0xFB30_00D8
- CIICBSA02, R/W, Address = 0xFB40_00D8

CIICBSA0n	Bit	Description	Initial State
CIICBSA0	[31:0]	Input format: YCbCr 3 plane → Cb frame start address Input format: YCbCr 2 plane → CbCr frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

2.8.2.13 Input DMA Cr0 Start Register (CIICRSA0n)

- CIICRSA00, R/W, Address = 0xFB20_00DC
- CIICRSA01, R/W, Address = 0xFB30_00DC
- CIICRSA02, R/W, Address = 0xFB40_00DC

CIICRSA0n	Bit	Description	Initial State
CIICRSA0	[31:0]	Input format: YCbCr 3 plane → Cr frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

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2.8.2.14 Input DMA Y Line Skip Register (CIILINESKIP_Yn)

- CIILINESKIP_Y0, R/W, Address = 0xFB20_00EC
- CIILINESKIP_Y1, R/W, Address = 0xFB30_00EC
- CIILINESKIP_Y2, R/W, Address = 0xFB40_00EC

CIILINESKIP_Yn	Bit	Description	Initial State
Reserved	[31:28]	Reserved	0
ILINESKIP_Y	[27:24]	Specifies Y Line Skip for Input DMA Note) Maximum value can be 8 (ML=OX)	0
Reserved	[23:0]	Reserved	0

2.8.2.15 Input DMA Cb Line Skip Register (CIILINESKIP_CBn)

- CIILINESKIP_CB0, R/W, Address = 0xFB20_00F0
- CIILINESKIP_CB1, R/W, Address = 0xFB30_00F0
- CIILINESKIP_CB2, R/W, Address = 0xFB40_00F0

CIILINESKIP_CBn	Bit	Description	Initial State
Reserved	[31:28]	Reserved	0
ILINESKIP_Cb	[27:24]	Specifies Cb Line Skip for Input DMA Note) Maximum value can be 8 (ML=OX)	0
Reserved	[23:0]	Reserved	0

2.8.2.16 Input DMA Cr Line Skip Register (CIILINESKIP_CRn)

- CIILINESKIP_CR0, R/W, Address = 0xFB20_00F4
- CIILINESKIP_CR1, R/W, Address = 0xFB30_00F4
- CIILINESKIP_CR2, R/W, Address = 0xFB40_00F4

CIILINESKIP_CRn	Bit	Description	Initial State
Reserved	[31:28]	Reserved	0
ILINESKIP_Cr	[27:24]	Specifies Cr Line Skip for Input DMA Note) Maximum value can be 8 (ML=OX)	0
Reserved	[23:0]	Reserved	0

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2.8.2.17 Real Input DMA Size Register (CIREAL_ISIZEn)

- CIREAL_ISIZE0, R/W, Address = 0xFB20_00F8
- CIREAL_ISIZE1, R/W, Address = 0xFB30_00F8
- CIREAL_ISIZE2, R/W, Address = 0xFB40_00F8

CIREAL_ISIZEn	Bit	Description	Initial State
AutoLoadEnable	[31]	Restarts input DMA automatically (only software trigger mode). At the start of first frame, it is required to set ENVID_M start. After the first frame, the next frame does not need ENVID_M setting. If autoload function is running, size and format value should be fixed. 0 = Disables AutoLoad 1 = Enables AutoLoad (ML=OX)	0
ADDR_CH_DIS	[30]	Disables input DMA address change (only software trigger mode) At the start of first frame, ADDR_CH_DIS should be equal to '0'. 0 = Enables address change 1 = Disables address change (ML=OX)	0
REAL_HEIGHT	[29:16]	Specifies input DMA real image vertical pixel size (Minimum 8). Note) 1) 2's multiple : YCbCr 420 2) 4's multiple : Weave-in mode and YCbCr 420 input 3) 2's multiple : Weave-in mode except YCbCr 420 input 4) 2's multiple : Input rotator ON except RGB, YCbCr 444 input Note) Must be multiple of PreVerRatio. If InRot90 = 1, then it must be 16's multiple. Must be 4's multiple of PreHorRatio. Minimum 16. (ML=OX)	0
Reserved	[15:14]	Reserved	0
REAL_WIDTH	[13:0]	Specifies input DMA real image horizontal pixel size. Note) Must be 16's multiple. Must be 4's multiple of PreHorRatio. Minimum 16. If InRot90 = 1, then it must be minimum 8. Must be multiple of PreVerRatio. (ML=OX)	0

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2.8.2.18 Input DMA Control Register (MSCTRLn)

- MSCTRL0, Address = 0xFB20_00FC
- MSCTRL1, Address = 0xFB30_00FC
- MSCTRL2, Address = 0xFB40_00FC

<table>
<tr><th>MSCTRLn</th><th>Bit</th><th>Description</th><th>R/W</th><th>Initial State</th></tr>
<tr><td>Weave_in</td><td>[31]</td><td>Even and Odd fields can be read separately from a complete progressive frame. The 1st frame reads even field data and the 2nd frame reads odd field data. When 1st and 2nd frame operation finish, InputDMA is disabled. Both Weave_in and Interlace_out should be set in simultaneous frames. Also, it is recommended that pingpong address should not be changed at Interlace even/ odd field (BC_SEL field should 0) .
0 = Weave
1 = Normal

Note)
When using input rotator in Weave_in mode, output horizontal size should be even value. Because vertical data will be converted into horizontal one after rotating.
(ML=XX)</td><td>R/W</td><td>0</td></tr>
<tr><td>Reserved</td><td>[30:28]</td><td>Reserved</td><td>R/W</td><td>0</td></tr>
<tr><td>Successive_cnt</td><td>[27:24]</td><td>Specifies input DMA burst successive count (Default is 4 but 3, 2, or 1 are also possible). This value should not be ‘0’.
(ML=OX)</td><td>R/W</td><td>4’d4</td></tr>
<tr><td>Reserved</td><td>[23:20]</td><td>Reserved</td><td>R/W</td><td>0</td></tr>
<tr><td>InBuf_Mode</td><td>[19]</td><td>Specifies input DMA buffer address mode.
1 = Ping-Pong buffer mode (Address 0 and 1 are valid)
0 = Single buffer mode (Only address 0 is valid)
(ML=OX)</td><td>R/W</td><td>0</td></tr>
<tr><td>Reserved</td><td>[18]</td><td>Reserved</td><td>R/W</td><td>0</td></tr>
<tr><td>Order2p_in</td><td>[17:16]</td><td>Specifies YCbCr 4:2:0 or 4:2:2 2plane memory reading style order in source input DMA image.
<table>
<tr><th>Bit</th><th>MSB LSB</th></tr>
<tr><td>00</td><td>Cr3Cb3Cr2Cb2Cr1Cb1Cr0Cb0</td></tr>
<tr><td>01</td><td>Cb3Cr3Cb2Cr2Cb1Cr1Cb0Cr0</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table>
(ML=OX)</td><td>R/W</td><td>0</td></tr>
<tr><td>C_INT_IN</td><td>[15]</td><td>1 = YCbCr 4:2:0 or 4:2:2 2plane input format
0 = YCbCr 4:2:0 or 4:2:2 3plane input format
(ML=OX)</td><td>R/W</td><td>0</td></tr>
</table>

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<table>
<tr><th>MSCTRLn</th><th>Bit</th><th>Description</th><th>R/W</th><th>Initial State</th></tr>
<tr><td>InFlipMd</td><td>[14:13]</td><td>Specifies image mirror and rotation for input DMA.
00 = Normal
01 = X-axis mirror
10 = Y-axis mirror
11 = 180° rotation (XY-axis mirror)
Note) [Memory to memory path] If input/output image format are all YCbCr 3plane, 'InFlipMd' must be used instead of OutFlipMd.
(ML=OX)</td><td>R/W</td><td>0</td></tr>
<tr><td>FIFO_CTRL</td><td>[12]</td><td>Specifies a basis FIFO control of input DMA or Input Rotator.
0 = FIFO Full (Next burst transaction is possible except Full FIFO)
1 = FIFO Empty (Next burst transaction is possible when FIFO is empty)
(ML=XX)</td><td>R/W</td><td>0</td></tr>
<tr><td>Reserved</td><td>[11]</td><td>Reserved</td><td>R/W</td><td>0</td></tr>
<tr><td>BC_SEL</td><td>[10]</td><td>Selects the input DMA buffer change.
0 = Ping-Pong address is changed at interlace even/odd field end.
1 = Ping-Pong address is changed at the frame operation end.
(ML=OX)</td><td>R/W</td><td>0</td></tr>
<tr><td>Reserved</td><td>[9]</td><td>Reserved</td><td>RW</td><td>0</td></tr>
<tr><td>Buffer_Ptr</td><td>[8]</td><td>Specifies the input DMA buffer address selection pointer. This register initializes to set the first frame address before starting input DMA.
This register should not be written under frame operation.
0 = Buffer address 0
1 = Buffer address 1
(ML=OX)</td><td>RW</td><td>0</td></tr>
<tr><td>Reserved</td><td>[7]</td><td>Reserved</td><td>RW</td><td>0</td></tr>
<tr><td>EOF_M</td><td>[6]</td><td>If Input DMA operation is complete, it generates end of frame.
(ML=OX)</td><td>R</td><td>0</td></tr>
<tr><td>Order422_M</td><td>[5:4]</td><td>If source input DMA image is 1plane YCbCr 4:2:2, then 1plane YCbCr 4:2:2 inputs memory reading order style.
<table>
<tr><td>bit</td><td>MSB LSB</td></tr>
<tr><td>00</td><td>Y3Cb1Y2Cr1Y1Cb0Y0Cr0</td></tr>
<tr><td>01</td><td>Cb1Y3Cr1Y2Cb0Y1Cr0Y0</td></tr>
<tr><td>10</td><td>Y3Cr1Y2Cb1Y1Cr0Y0Cb0</td></tr>
<tr><td>11</td><td>Cr1Y3Cb1Y2Cr0Y1Cb0Y0</td></tr>
</table>
(ML=OX)</td><td>R/W</td><td>0</td></tr>
</table>

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MSCTRLn	Bit	Description	R/W	Initial State
SEL_DMA_ CAM	[3]	Selects input data selection. 0 = External camera input path 1 = Memory data input path (Input DMA) (ML=OX)	R/W	0
InFormat_M	[2:1]	Specifies the source image format for input DMA. 00 = YCbCr 4:2:0 input image format. (2 or 3 plane) 01 = YCbCr 4:2:2 input image format. (2 or 3 plane) (ref. 2 or 3 plane format register → C_INT_IN) 10 = YCbCr 4:2:2 input image format. (1 plane) 11 = RGB input image format. (ref. RGB format register → InRGB_FMT) Note) Refer to the gathering extension register. YCbCr444_IN (ML=OX)	R/W	0
ENVID_M	[0]	Starts input DMA operation (Software setting triggers low to high). The hardware clears automatically. If data flows from input DMA to local direct FIFO, the software can clear this bit when LCD_ENSTATUS is '0'. 1) SEL_DMA_CAM = '0', ENVID_M don't care (using external camera signal) 2) SEL_DMA_CAM = '1', ENVID_M is set (0→1), then Input DMA operation starts (ML=OX)	R/W	0

NOTE: ENVID_M SFR must be set at the end. Starting order for using DMA input path.
SEL_DMA_CAM (others SFR setting) → Image Capture Enable and Scaler start SFR setting → ENVID_M SFR setting.

- Cf.) Image Capture Enable SFR must be set at the end. Starting order for using Direct FIFO input path.
  SEL_DMA_CAM → SelWB_CAMIF (others SFR setting) → Image Capture Enable and Scaler start SFR setting
- Cf.) Image Capture Enable SFR be set at last. Starting order for using camera input path.
  SEL_DMA_CAM → SelWB_CAMIF → SelCam_CAMIF (others SFR setting) → Image Capture Enable and Scaler start SFR setting

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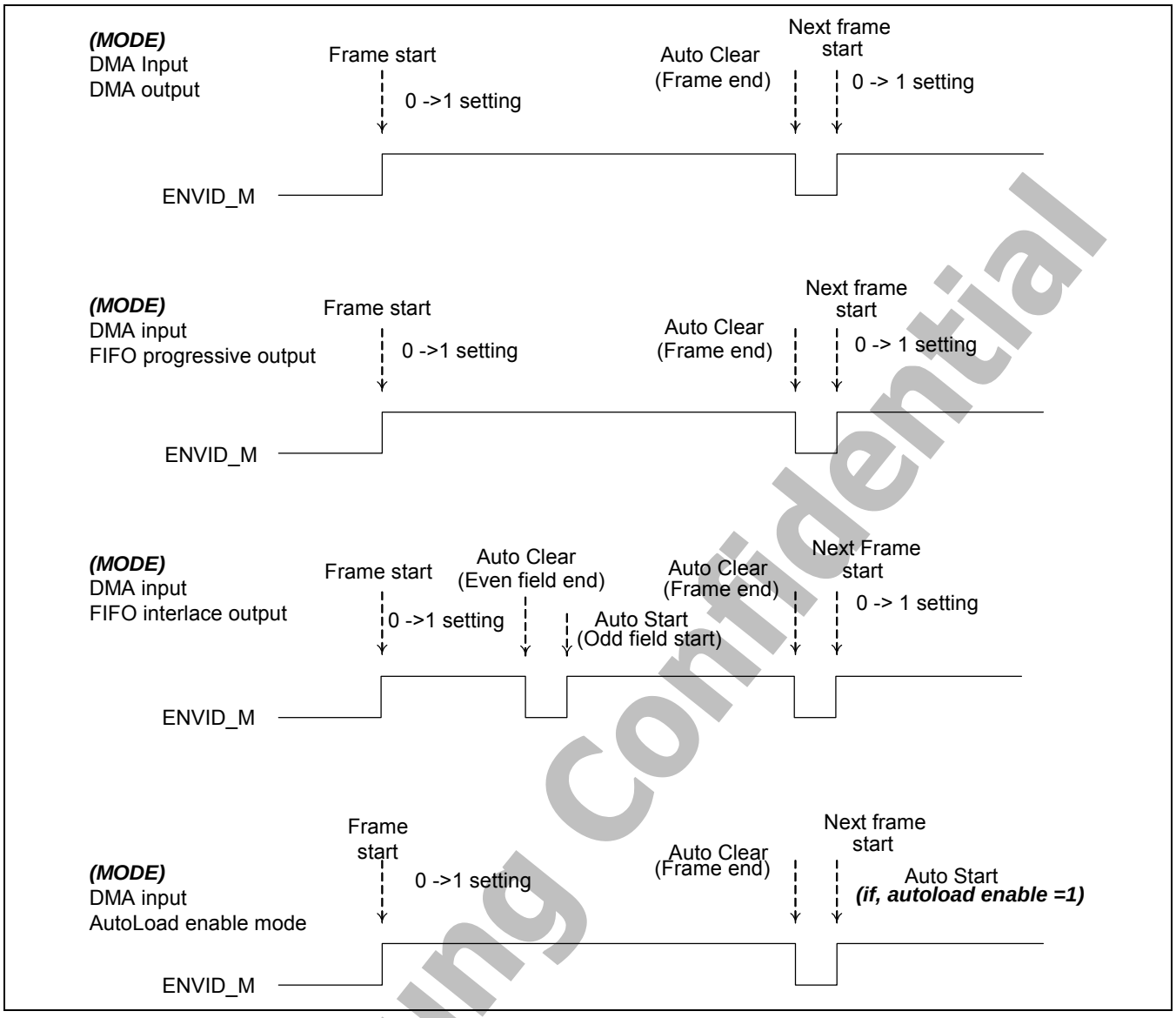

Figure 2-30 ENVID_M SFR Setting When Input DMA Start to Read Memory Data

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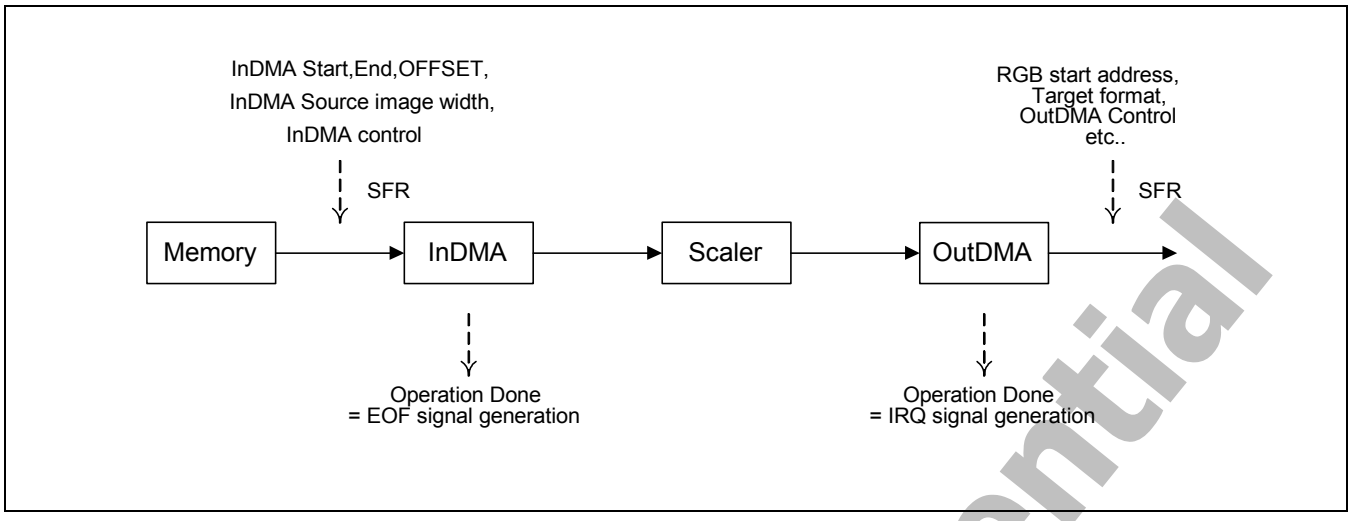

Figure 2-31 SFR and Operation (Related Each DMA When Selected Input DMA Path)

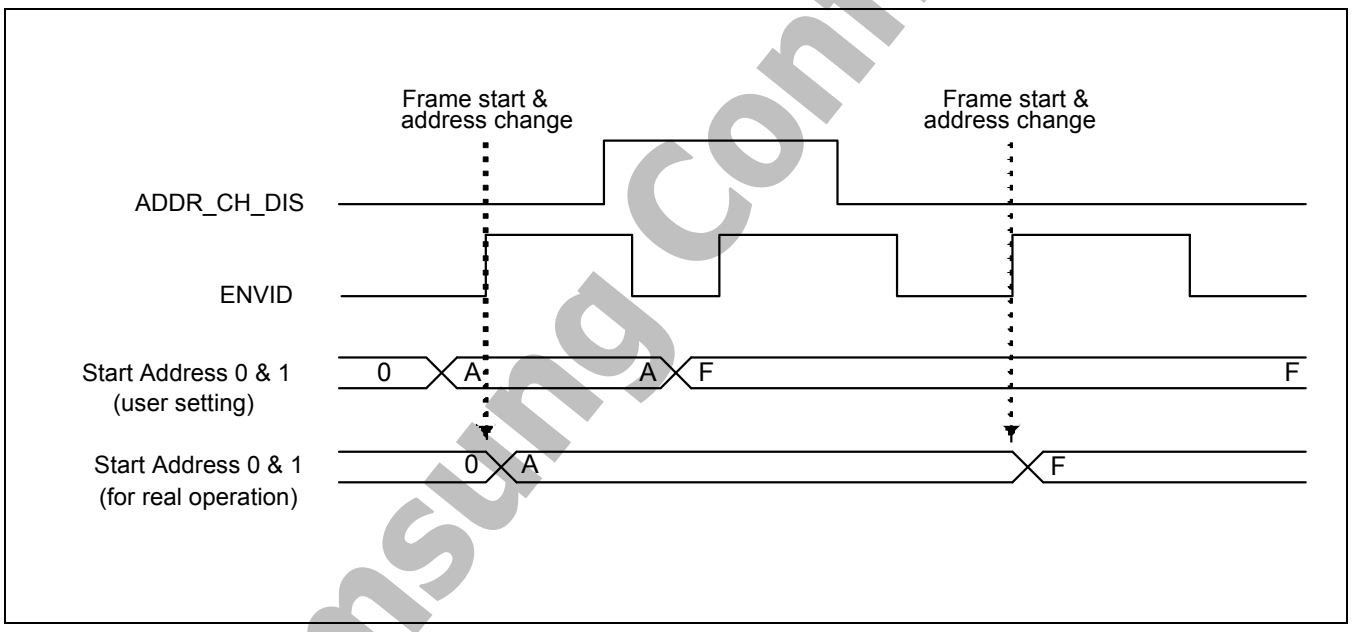

Figure 2-32 Input DMA Address Change Timing (progressive to progressive)

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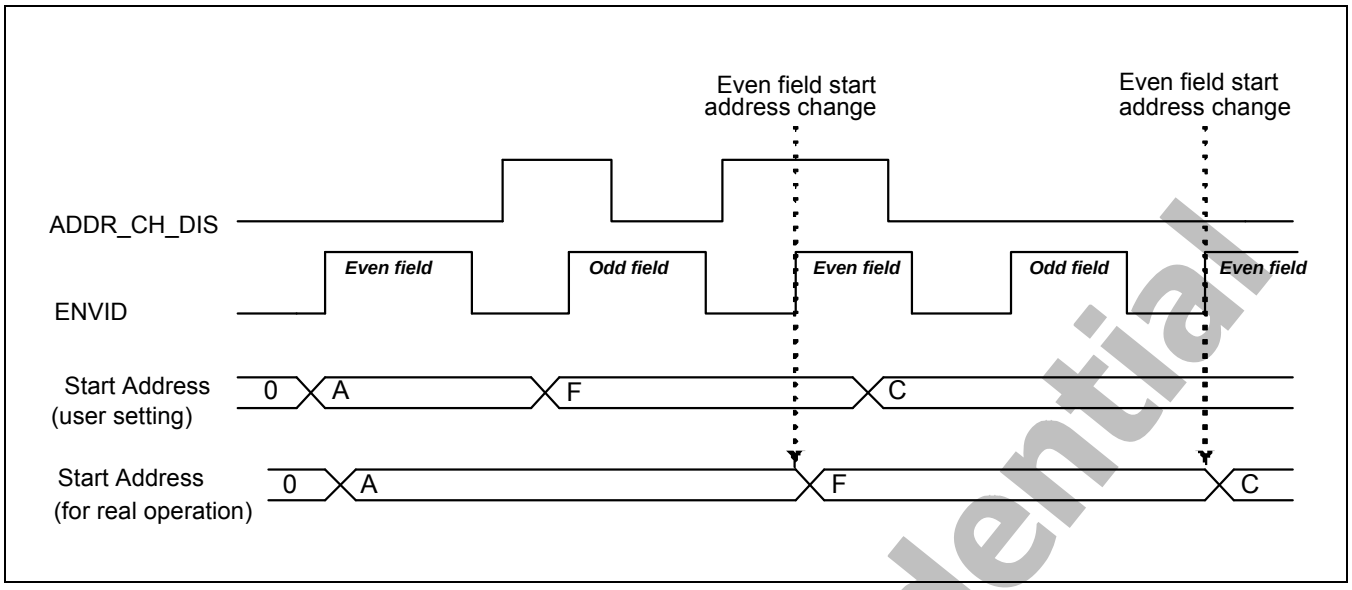

Figure 2-33 Input DMA Address Change Timing (progressive to interlace)

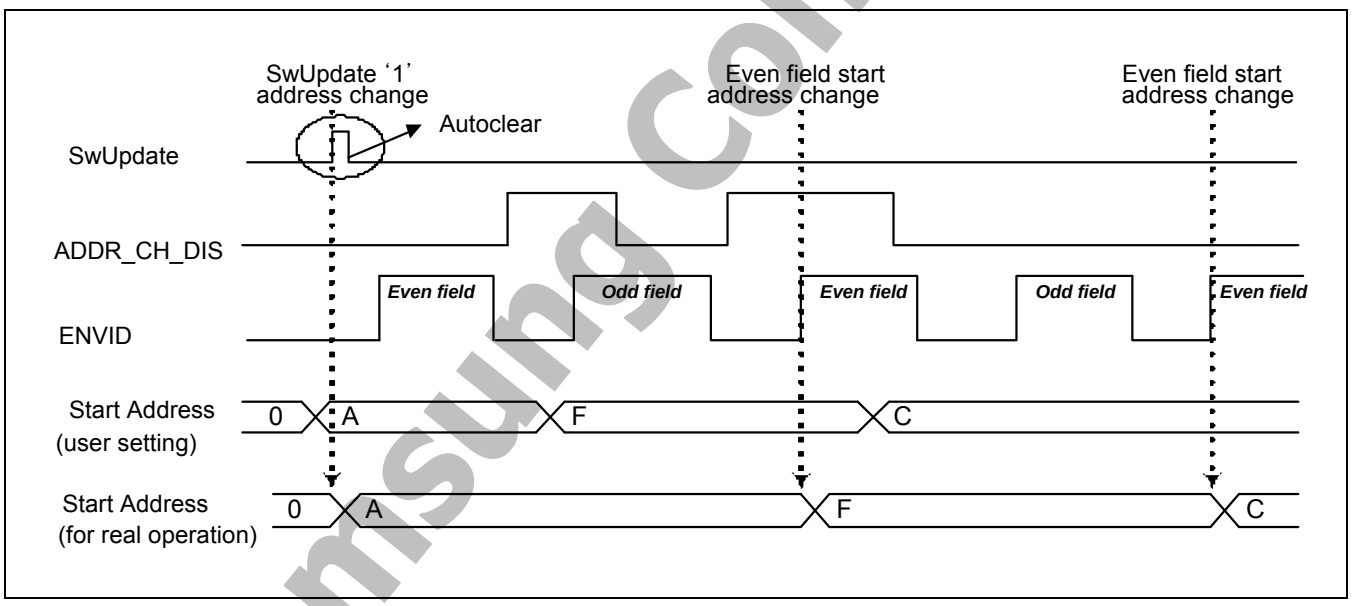

Figure 2-34 Input DMA Address Change Timing (Software Update)

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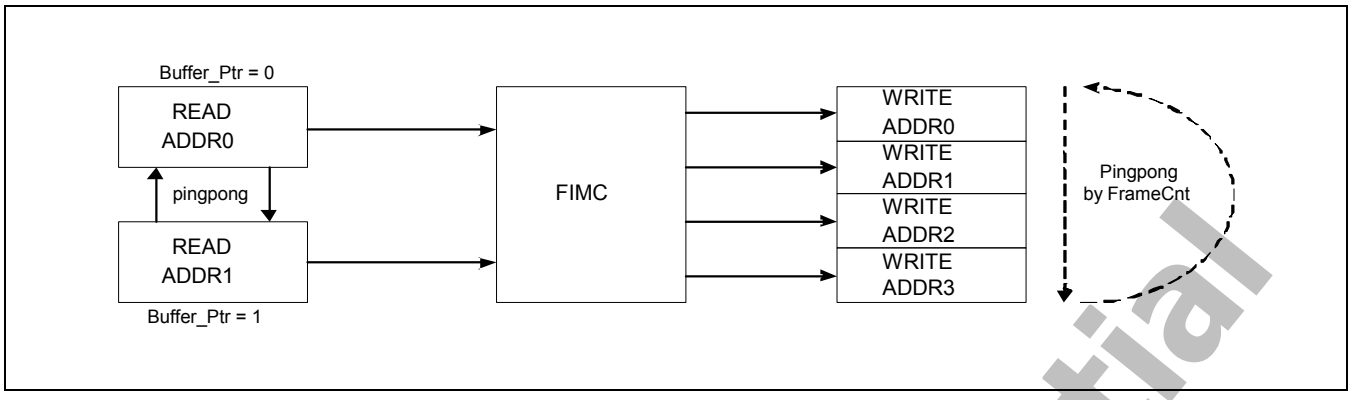

Figure 2-35 Input/Ouput DMA pingpong Address Change Scheme

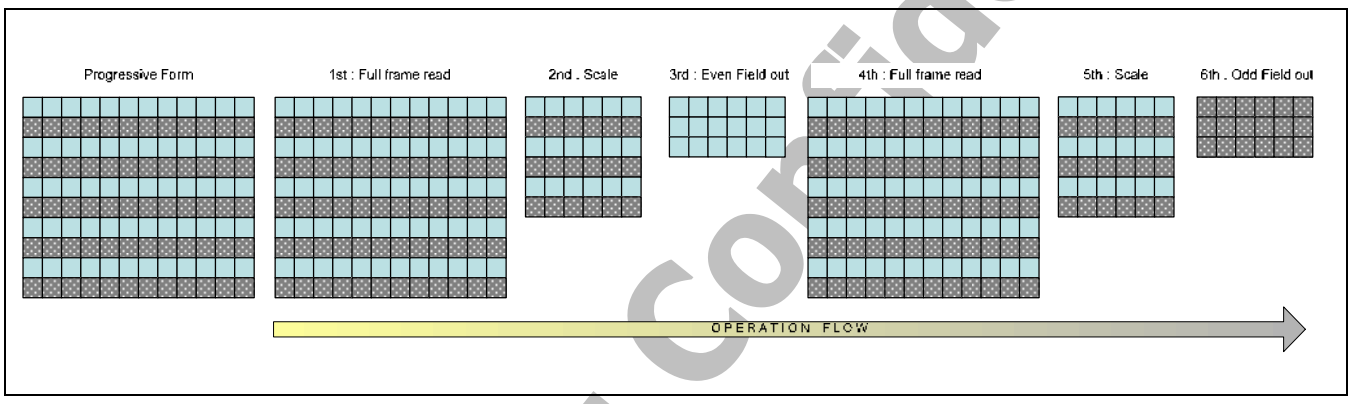

Figure 2-36 Input DMA Progressive-in to Interlace-out (only interlace_out setting)

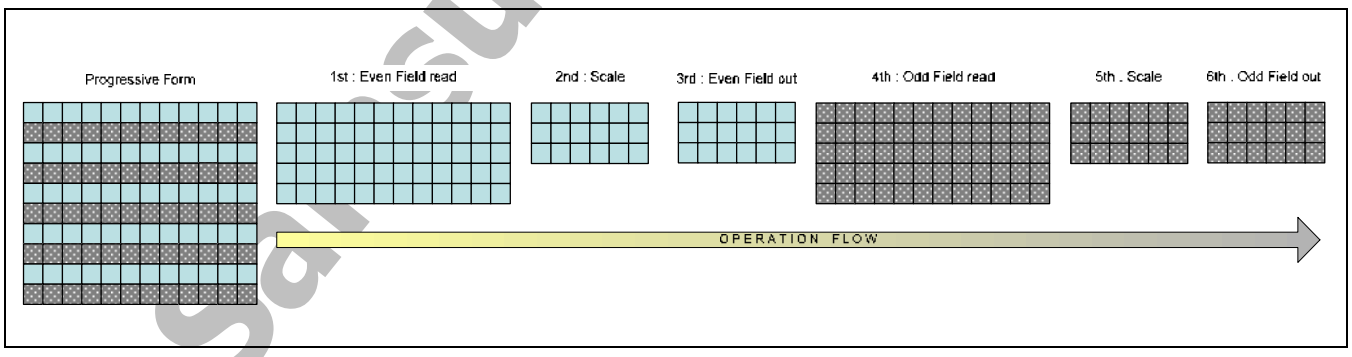

Figure 2-37 Input DMA Progressive-in to Interlace-out (Weave_in and Interlace_out setting)

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2.8.2.19 Input DMA Y1 Start Register (CIIYSA1n)

- CIIYSA10, R/W, Address = 0xFB20_0144
- CIIYSA11, R/W, Address = 0xFB30_0144
- CIIYSA12, R/W, Address = 0xFB40_0144

CIIYSA1n	Bit	Description	Initial State
CIIYSA1	[31:0]	Input format: YCbCr 2/3 plane → Y frame start address Input format: YCbCr 1 plane → YCbCr frame start address Input format: RGB → RGB frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

2.8.2.20 Input DMA CB1 Start Register (CIICBSA1n)

- CIICBSA10, R/W, Address = 0xFB20_0148
- CIICBSA11, R/W, Address = 0xFB30_0148
- CIICBSA12, R/W, Address = 0xFB40_0148

CIICBSA1n	Bit	Description	Initial State
CIICBSA1	[31:0]	Input format: YCbCr 3 plane → Cb frame start address Input format: YCbCr 2 plane → CbCr frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

2.8.2.21 Input DMA CR1 Start Register (CIICRSA1n)

- CIICRSA10, R/W, Address = 0xFB20_014C
- CIICRSA11, R/W, Address = 0xFB30_014C
- CIICRSA12, R/W, Address = 0xFB40_014C

CIICRSA1n	Bit	Description	Initial State
CIICRSA1	[31:0]	Input format: YCbCr 3 plane → Cr frame start address Note: In tile mode, this value should be aligned 4Kbytes. That is to say, CIOYSA1[11:0] should be 0x000. (ML=OX)	0

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2.8.2.22 Output DMA Y Offset Register (ClOYOFFn)

- ClOYOFF0, R/W, Address = 0xFB20_0168
- ClOYOFF1, R/W, Address = 0xFB30_0168
- ClOYOFF2, R/W, Address = 0xFB40_0168

ClOYOFFn	Bit	Description	Initial State
Reserved	[31:30]	Reserved	0
OYOFF_V	[29:16]	Output DMA vertical offset for Y component Output format: YCbCr 2/3 plane → Y height offset Output format: YCbCr 1 plane → YCbCr height offset Output format: RGB → RGB height offset Note) Offset value is based on line unit (ML=OO)	0
Reserved	[15:14]	Reserved	0
OYOFF_H	[13:0]	Output DMA horizontal offset for Y component Output format: YCbCr 2/3 plane → Y width offset Output format: YCbCr 1 plane → YCbCr width offset Output format: RGB → RGB width offset Note) Offset value is based on pixel unit (ML=OO)	0

2.8.2.23 Output DMA Cb Offset Register (ClOCBOFFn)

- ClOCBOFF0, R/W, Address = 0xFB20_016C
- ClOCBOFF1, R/W, Address = 0xFB30_016C
- ClOCBOFF2, R/W, Address = 0xFB40_016C

ClOCBOFFn	Bit	Description	Initial State
Reserved	[31:30]	Reserved	0
OCBOFF_V	[29:16]	Output DMA vertical offset for Cb component Output format: YCbCr 3 plane → Cb height offset Output format: YCbCr 2 plane → CbCr height offset Note) Offset value is based on line unit (ML=OO)	0
Reserved	[15:14]	Reserved	0

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OCBOFF_H	[13:0]	Output DMA horizontal offset for Cb component Output format: YCbCr 3 plane → Cb width offset Output format: YCbCr 2 plane → CbCr width offset Note) Offset value is based on pixel unit (ML=OO)	0

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2.8.2.24 Output DMA Cr Offset Register

- CIOCROFF0, R/W, Address = 0xFB20_0170
- CIOCROFF1, R/W, Address = 0xFB30_0170
- CIOCROFF2, R/W, Address = 0xFB40_0170

CIOCROFFn	Bit	Description	Initial State
Reserved	[31:30]	Reserved	0
OCROFF_V	[29:16]	Specifies the output DMA vertical offset for Cr component. Output format: YCbCr 3 plane → Cr height offset Note) Offset value is based on line unit (ML=OO)	0
Reserved	[15:14]	Reserved	0
OCROFF_H	[13:0]	Specifies the output DMA horizontal offset for Cr component. Output format: YCbCr 3 plane → Cr width offset Note) Offset value is based on pixel unit (ML=OO)	0

2.8.2.25 Input DMA Y Offset Register (CIIYOFFn)

- CIIYOFF0, R/W, Address = 0xFB20_0174
- CIIYOFF1, R/W, Address = 0xFB30_0174
- CIIYOFF2, R/W, Address = 0xFB40_0174

CIIYOFFn	Bit	Description	Initial State
Reserved	[31:30]	Reserved	0
IYOFF_V	[29:16]	Specifies the input DMA vertical offset for Y component. Input format: YCbCr 2/3 plane → Y height offset Input format: YCbCr 1 plane → YCbCr height offset Input format: RGB → RGB height offset Note) Offset value is based on line unit (ML=OX)	0
Reserved	[15:14]	Reserved	0
IYOFF_H	[13:0]	Specifies the input DMA horizontal offset for Y component. Input format: YCbCr 2/3 plane → Y width offset Input format: YCbCr 1 plane → YCbCr width offset Input format: RGB → RGB width offset Note) Offset value is based on pixel unit (ML=OX)	0

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2.8.2.26 Input DMA Cb Offset Register (CIICBOFFn)

- CIICBOFF0, R/W, Address = 0xFB20_0178
- CIICBOFF1, R/W, Address = 0xFB30_0178
- CIICBOFF2, R/W, Address = 0xFB40_0178

CIICBOFFn	Bit	Description	Initial State
Reserved	[31:30]	Reserved	0
ICBOFF_V	[29:16]	Specifies the input DMA vertical offset for Cb component. Input format: YCbCr 3 plane → Cb height offset Input format: YCbCr 2 plane → CbCr height offset Note) Offset value is based on line unit (ML=OX)	0
Reserved	[15:14]	Reserved	0
ICBOFF_H	[13:0]	Specifies the input DMA horizontal offset for Cb component. Input format: YCbCr 3 plane → Cb width offset Input format: YCbCr 2 plane → CbCr width offset Note) Offset value is based on pixel unit (ML=OX)	0

2.8.2.27 Input DMA Cr Offset Register (CIICROFFn)

- CIICRFF0, R/W, Address = 0xFB20_017C
- CIICRFF1, R/W, Address = 0xFB30_017C
- CIICRFF2, R/W, Address = 0xFB40_017C

CIICROFFn	Bit	Description	Initial State
Reserved	[31:30]	Reserved	0
ICROFF_V	[29:16]	Specifies the input DMA vertical offset for Cr component. Input format: YCbCr 3 plane → Cr height offset Note) Offset value is based on line unit (ML=OX)	0
Reserved	[15:14]	Reserved	0
ICROFF_H	[13:0]	Specifies the input DMA horizontal offset for Cr component. Input format: YCbCr 3 plane → Cr width offset Note) Offset value is based on pixel unit (ML=OX)	0

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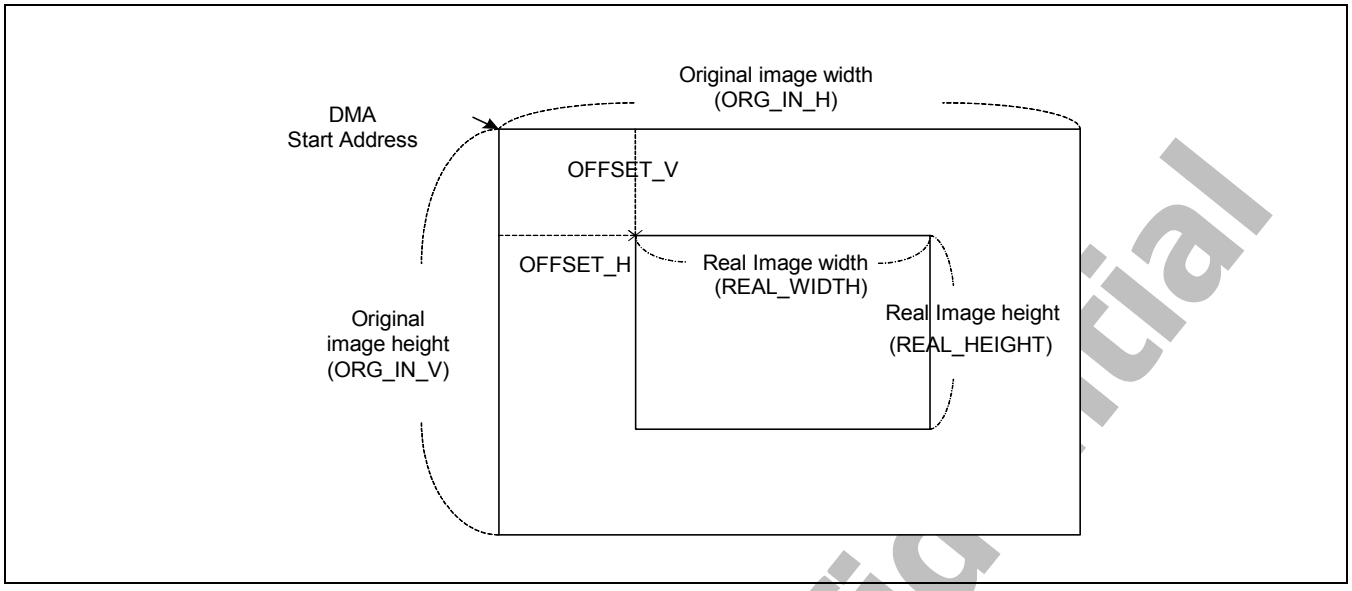

Figure 2-38 Input DMA Offset and Image Size

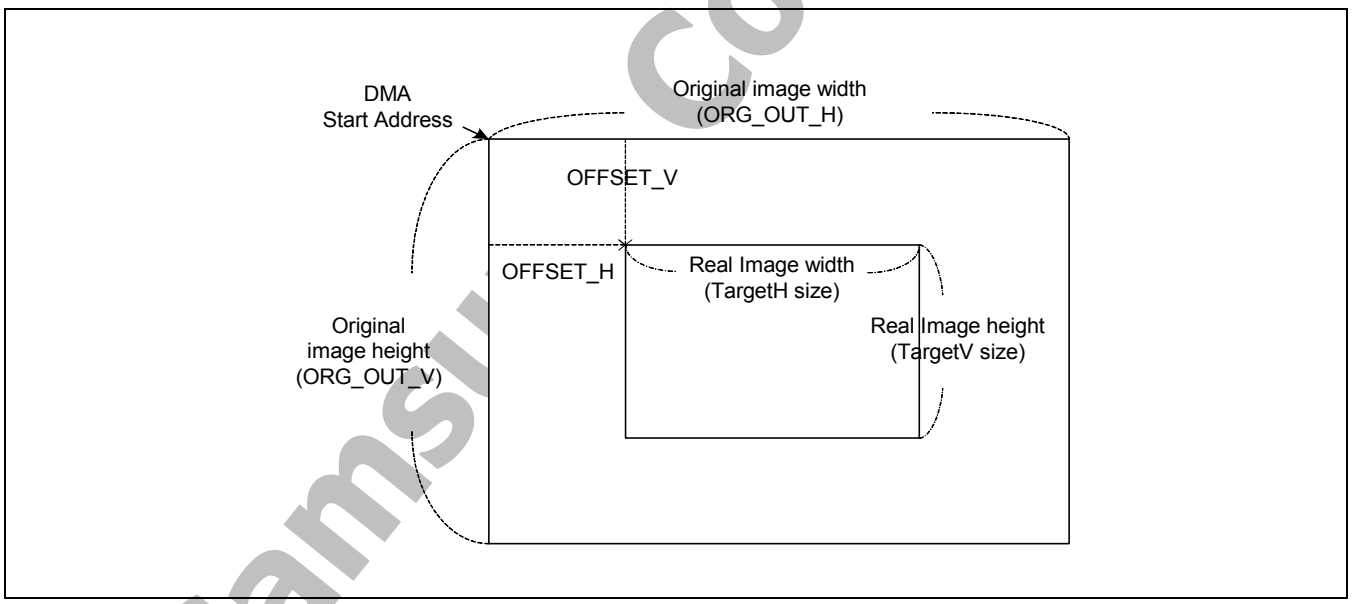

Figure 2-39 Output DMA Offset and Image Size

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- **DMA Start Address**
  Start address of ADDRStart_Y/Cb/Cr/RGB points to the first address, where the corresponding component of Y/Cb/Cr/RGB is read or written. ADDRStart_Cb is only valid for 2 or 3 planes YCbCr420, 422, 444 source image formats. ADDRStart_Cr is only valid for 3 planes YCbCr420, 422, 444 source image.

Only for CAMIF0 & CAMIF2 : Each of these should be aligned with double word boundary (that is ADDRStart_X[2:0] = 3'b000).

- **DMA OFFSET**
  - Offset_H_Y = Y offset per a horizontal line (8's multiple only for CAMIF0,2)
    = Number of pixel (or sample) in horizontal offset
  - Offset_H_Cb = Cb offset per a horizontal line (8's multiple only for CAMIF0,2)
    = Number of pixel (or sample) in horizontal offset
  - Offset_H_ Cr = Cr offset per a horizontal line (8's multiple only for CAMIF0,2)
    = Number of pixel (or sample) in horizontal offset
-
  - Offset_V_Y = Number of vertical Y offset
  -
  - Offset_V_Cb = Number of vertical Cb offset
  - Offset_V_Cr = Number of vertical Cr offset

2.8.2.28 Original Input DMA Image Size (ORGISIZEn)

- ORGISIZE0, R/W, Address = 0xFB20_0180
- ORGISIZE1, R/W, Address = 0xFB30_0180
- ORGISIZE2, R/W, Address = 0xFB40_0180

ORGISIZEn	Bit	Description	Initial State
Reserved	[31:30]	Reserved	0
ORG_IN_V	[29:16]	Specifies the input DMA original image vertical pixel size. (minimum is 8). This size should not be less than REAL_HEIGHT register. Note) When Input rotator is enabled : this value should be multiple of 8 (ML=OX)	0
Reserved	[15:14]	Reserved	0

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ORG_IN_H	[13:0]	Specifies the input DMA source image horizontal pixel size. Must be multiple of 16. This size should not be less than REAL_WIDTH register. (ML=OX)	0

Note : Memory region of input DMA should follow below equation for input rotator is enabled.

ORG_IN_V + [8-{(ORG_IN_V - OFFSET_V)%8}]

2.8.2.29 Original Output DMA Image Size (ORGOSIZEn)

- ORGOSIZE0, R/W, Address = 0xFB20_0184
- ORGOSIZE1, R/W, Address = 0xFB30_0184
- ORGOSIZE2, R/W, Address = 0xFB40_0184

ORGOSIZEn	Bit	Description	Initial State
Reserved	[31:30]	Reserved	0
ORG_OUT_V	[29:16]	Specifies the output DMA original image vertical pixel size (minimum is 8). This size should not be less than TargetVsize register. If output rotator is running, this size should not be less than TargetHsize register. Note) If output format is YCbCr 420, this value should be even number. (ML=OO)	0
Reserved	[15:14]	Reserved	0
ORG_OUT_H	[13:0]	Specifies the output DMA source image horizontal pixel size. Must be multiple of 16. This size should not be less than TargetHsize register. If output rotator is running, this size should not be less than TargetVsize register. (ML=OO)	0

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2.8.2.30 Gathering Extension Register (CIEXTENn)

- CIEXTEN0, R/W, Address = 0xFB20_0188
- CIEXTEN1, R/W, Address = 0xFB30_0188
- CIEXTEN2, R/W, Address = 0xFB40_0188

CIEXTENn	Bit	Description	Initial State
Reserved	[31]	Reserved	0
SrcHsize_CAM_ext	[30]	Specifies the bit value [13] of camera source horizontal pixel number register. {SrcHsize_CAM_ext,SrcHsize_CAM} = {[13], [12:0]}. Thus, total camera source horizontal size = [13:0] (ML=OO)	0
Reserved	[29]	Reserved	0
WinHorOfst_ext	[28]	Specifies the bit value [11] of window horizontal offset register. {WinHorOfst_ext,WinHorOfst} = {[11],[10:0]}. Thus, total window horizontal offset size = [11:0] (ML=OO)	0
Reserved	[27]	Reserved	
TargetHsize_ext	[26]	Specifies the bit value [13] of target image horizontal pixel number register. {TargetHsize_ext,TargetHsize} = {[13],[12:0]} Thus, total target image horizontal size = [13:0] (ML=OO)	0
Reserved	[25]	Reserved	0
TargetVsize_ext	[24]	Specifies the bit value [13] of target image vertical number register. {TargetVsize_ext,TargetVsize} = {[13],[12:0]} Thus, total target image vertical size = [13:0] (ML=OO)	0
Reserved	[23]	Reserved	0
YCbCr444_OUT	[22]	If this bit is 1, output format is YCbCr 444. This register priority is higher than OutFormat in CITRGFMTn (described in Chapter 8.17). (ML=OO)	0
Reserved	[21]	Reserved	0
YCbCr444_IN	[20]	Input DMA format YCbCr4:4:4 (this register priority is higher than InFormat_M register) (ML=OX)	0
Reserved	[19:16]	Reserved	0
MainHorRatio_ext	[15:10]	CAMIF1: Bit value [5:0] of the Mainscale horizontal ratio register. {MainHorRatio,MainHorRatio_ext} = {[14:6],[5:0]} Thus, total Mainscale horizontal ratio register range = [14:0] (ML=OO)	0
Reserved	[9:6]	Reserved	0

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MainVerRatio_ext	[5:0]	CAMIF1: Bit value [5:0] of the Mainscale vertical ratio register. {MainVerRatio,MainVerRatio_ext} = {[14:6],[5:0]} Thus, total Mainscale vertical ratio register range = [14:0] (ML=OO)	0

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2.8.2.31 DMA Parameter Register (CIDMAPARAMn)

- CIDMAPARAM0, R/W, Address = 0xFB20_018C
- CIDMAPARAM1, R/W, Address = 0xFB30_018C
- CIDAMPARAM2, R/W, Address = 0xFB40_018C

CIDMAPARAMn	Bit	Description	Initial State
Reserved	[31]	Reserved	0
MODE_R	[30:29]	Specifies the INPUT DMA address access style. 0 = Linear 1 = Reserved 2 = Reserved 3 = 64x32 tile (ML=OX)	0
Reserved	[28:15]	Reserved	0
MODE_W	[14:13]	Specifies the OUTPUT DMA address access style. 0 = Linear 1 = Reserved 2 = Reserved 3 = 64x32 tile Note) If input format is either CAM_JPEG or MIPI RAW, User can not use 64x32 tile mode. (ML=XX)	0
Reserved	[12:4]	Reserved	0
Reserved	[3:0]	Reserved	0

NOTE: Refer to Chapter 9.7, “MFC” for Tile Mode description.

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2.8.2.32 Mipi Input Format Register (CSIIMGFMTn)

- CSIIMGFMT0, R/W, Address = 0xFB20_0194
- CSIIMGFMT1, R/W, Address = 0xFB30_0194
- CSIIMGFMT2, R/W, Address = 0xFB40_0194

CSIIMGFMTn	Bit	Description	Initial State
Reserved	[31:10]	Reserved	0
DATAb_port	[9:8]	Specifies the MIPI CSIS data align. 0 = 24-bit align 1 = 32-bit align 2 = Reserved 3 = Reserved (ML=XX)	0
Reserved	[7:6]	Reserved	0
ImgFormOfCh0	[5:0]	Specifies the image format of MIPI Channel 0. If the RAW format is image format, image format conversion is not possible. Set scaler bypass mode. 0x1E = YUV422 8-bit 0x2A = RAW8 0x2B = RAW10 0x2C = RAW12 (ML=XX)	0x1E

NOTE: Frame End Address calculation method (useful only for TILE 64x32 access mode)

Note: When tile mode is enable, lower 13bits of Base_address[31:0] have Zero value. So, SFRs related to Base_adddress should be zero their lower 13bits

When condition is YCbCr4:2:0 3plane & In Rotator 90' & X,XY-flip & Horizontal size $\leq$ 32 & OFFSET_X_Cr $\neq$ 0, Minimum input size is 64x64.

Example: Image pixel size: 720p (1280 x 720), Format: YCbCr4:2:0 2plane (NV12)

```
* hor_img_size (width) = 1280byte, ver_img_size (height) = 720
if (hor_img_size % 16 == 0)     hor_img_offset = 0
else     hor_img_offset = 16 – (hor_img_size % 16)
if (ver_img_size % 16 == 0)     ver_img_offset = 0
elsever_img_offset = 16 – (ver_img_size % 16)
if (Luma) { // Y plane
pixel_x = hor_img_size+hor_img_offset = 1280
pixel_y = ver_img_size+ver_img_offset = 720
}
else if (Chroma) { // Cb/Cr plane
```

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pixel_x = hor_img_size+hor_img_offset = 1280
pixel_y = (ver_img_size+ver_img_offset) / 2 = 360
}

1) Luma case
pixel_x_minus = pixel_x - 1 = 1279
pixel_y_minus = pixel_y - 1 = 719 = 1011001111 (binary)
roundup_x = INT (INT ((pixel_x - 1)/16)/8) + 1 = 10
roundup_y = INT(INT((pixel_y - 1)/16)/4) + 1 = 12

if (pixel_y_minus[5] == 0) // pixel_y_minus[5:0]='b 001111 , pixel_y_minus[5]=0
pic_range = pixel_y_minus[14:6] * roundup_x + pixel_x_minus[14:8] + 1 = 11 * 10 + 4 + 1 = 115
else
pic_range = roundup_x * roundup_y

2) Chroma case
pixel_x_minus = pixel_x - 1 = 1279
pixel_y_minus = pixel_y - 1 = 359 = 101100111 (binary)
roundup_x = INT (INT ((pixel_x - 1)/16)/8) + 1 = 10
roundup_y = INT(INT((pixel_y - 1)/16)/4) + 1 = 6

if (pixel_y_minus[5] == 0) // pixel_y_minus[5:0]='b 100111 , pixel_y_minus[5]=1
pic_range = pixel_y_minus[14:6] * roundup_x + pixel_x_minus[14:8] + 1
else
pic_range = roundup_x * roundup_y = 10 * 6 = 60

Thus, each plane frame end address = Base_address[31:0] + {pic_range, 2'b0, 11'b0}

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2.8.2.33 Miscellaneous Register (CMISCn)

- CMISC0, R/W, Address = 0xFB20_0198
- CMISC1, R/W, Address = 0xFB30_0198
- CMISC2, R/W, Address = 0xFB40_0198

CMISCn	Bit	Description	Initial State
Reserved	[31:2]	-	0
SEL_CORE_CLOCK	[1]	Specifies Clock source selection for CAMIF core block. 0 : Bus clock 1 : Special clock for local path operation between CAMIF and Display Controller. (ML=OO)	0
Reserved	[0]	-	0

2.8.2.34 Key Detect Register (CIKEYn)

- CIKEY0, R/W, Address = 0xFB20_019C
- CIKEY1, R/W, Address = 0xFB30_019C
- CIKEY2, R/W, Address = 0xFB40_019C

CIKEYn	Bit	Description	Initial State
KEY_DETECT	[31]	Specifies KEY detect for graphic layer scaling. 1 = KEY detect ON 0 = OFF (Normal) (ML=OO)	0
Reserved	[30:28]	-	0
R_KEY	[27:20]	Specifies 'R' of the RGB region key value. (ML=OO)	0
Reserved	[19:18]	-	0
G_KEY	[17:10]	Specifies 'G' of the RGB region key value. (ML=OO)	0
Reserved	[9:8]	-	0
B_KEY	[7:0]	Specifies 'B' of the RGB region key value. (ML=OO)	0

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3 MIPI DSIM

3.1 ARCHITECTURE OF MIPI DSM

3.1.1 KEY FEATURES OF MIPI DSM

The key features of MIPI DSIM include:

- Complies to MIPI DSI Standard Specification V1.01r11
  - Maximum resolution ranges up to XGA (1028x768)
  - Supports 1, 2, 3, or 4 data lanes
  - Supports pixel format: 16bpp, 18bpp packed, 18bpp loosely packed (3 byte format), and 24bpp

- Interfaces
  - Complies with Protocol-to-PHY Interface (PPI) in MIPI D-PHY Specification V0.90
  - Supports RGB Interface for Video Image Input from display controller
  - Supports I80 Interface for Command Mode Image input from display controller
  - Supports PMS control interface for PLL to configure byte clock frequency
  - Supports Prescaler to generate escape clock from byte clock

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3.1.2 BLOCK DIAGRAM OF MIPI DSI SYSTEM

3.1.2.1 Total System Block Diagram

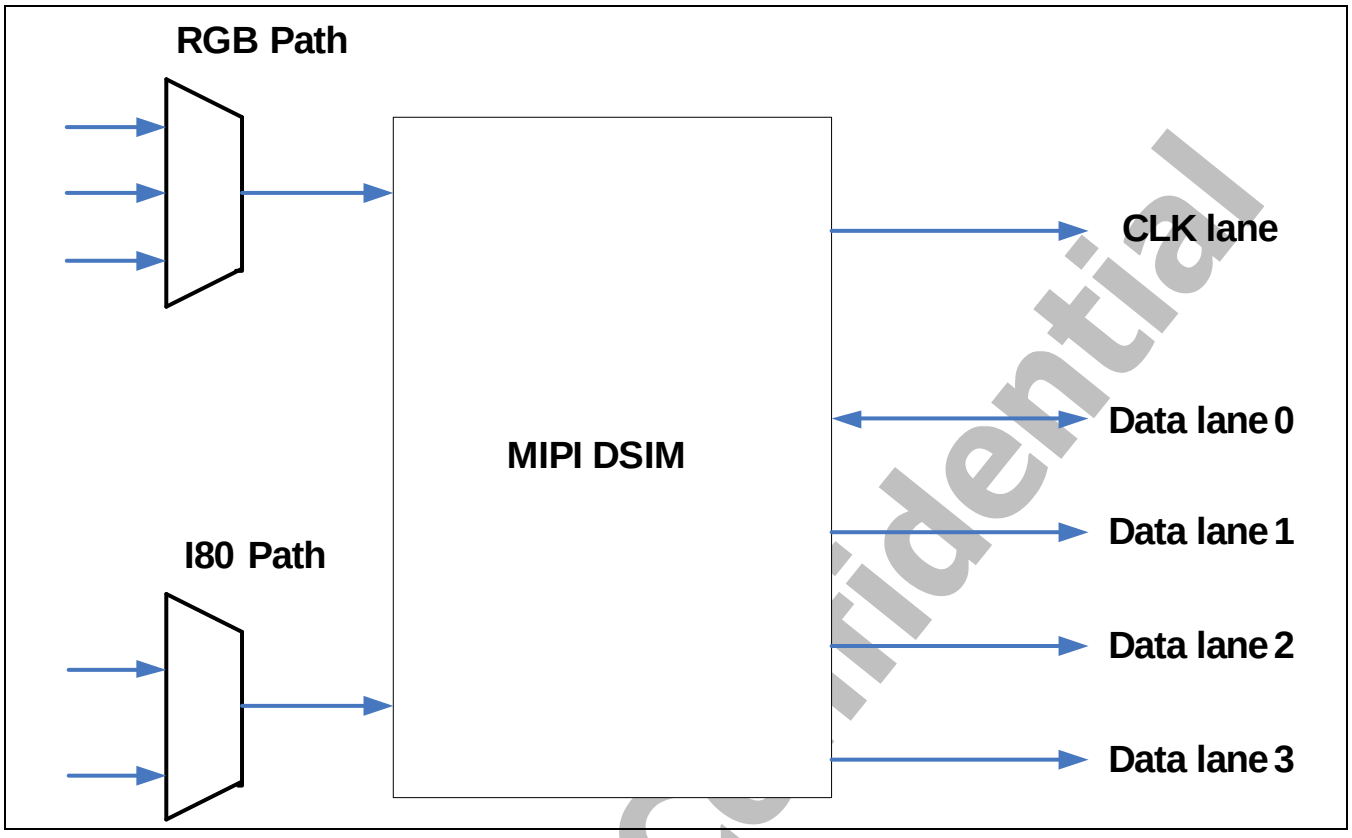

Figure 3-1 MIPI DSI System Block Diagram

NOTE:

1. DSIM gets data from the different IPs.
2. You can select one of above data paths by setting DISPLAY_PATH_SEL [1:0] (0xE010_7008).

For more information, refer to Section, "2-3 S5PV210_CMU".

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3.1.2.2 Internal Primary FIFOs

Table 3-1 describes configurable-sized primary FIFOs.

Table 3-1 Internal Primary FIFO List

Port	FIFO Type	Size	Description
Main display	Packet Header FIFO	3byte X 64 depth	Specifies the packet header FIFO for main display.
	Payload FIFO	4byte X 1024 depth	Specifies the payload FIFO for main display image.
Sub display for I80 INTERFACE image data	Packet Header FIFO	3byte X 4 depth	Specifies the packet header FIFO for I80 INTERFACE sub display.
	Payload FIFO	4byte X 512 depth	Specifies the payload FIFO for I80 INTERFACE sub display image.
Command for I80 INTERFACE command	Packet Header FIFO	3byte X 16 depth	Specifies the packet header FIFO for I80 INTERFACE command packet.
	Payload FIFO	4byte X 16 depth	Specifies the payload FIFO for I80 INTERFACE command long packet payload.
SFR for general packets	Packet Header FIFO	3byte X 16 depth	Specifies the packet header FIFO for general packet.
	Payload FIFO	4byte X 512 depth	Specifies the payload FIFO for general long packet.
RX FIFO	Packet header and Payload FIFO	4byte X 64 depth	Specifies Rx FIFO for LPDR. This FIFO is common for packet header and payload.

3.1.2.3 Packet Header Arbitration

There are four-packet headers FIFOs for Tx, namely, main display, sub display, I80 INTERFACE command, and SFR FIFO. The main and sub display FIFO packet headers contain the image data, while the I80 INTERFACE command FIFO packet header contains the command packets. On the other hand, the SFR FIFO packet header contains command packets, sub display image data (in Video mode), and so on.

The packet header arbiter has a “Fixed priority” algorithm. Priority order is fixed as main display, sub display, I80 INTERFACE command, and SFR FIFO packet header.

In the Video mode, sub display and I80 INTERFACE command FIFO are not used. The SFR FIFO packet header checks if the main display FIFO is empty (no request) in not-active image region and then sends its request.

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3.1.2.4 RxFIFO Structure

To read the packets received via low power data receiving mode, RxFIFO acts like an SFR. RxFIFO is an asynchronous FIFO with ByteClk and PCLK domains as input clock and output clock domains respectively. The Rx data is synchronized to RxClk. RXBUF has four Rx Byte buffers for aligning byte to word.

The packet headers of all the packets stored in RXFIFO are word-aligned, that is, the first byte of a packet is always stored in LSB. For example, if a long packet has 7-byte payload, the last byte is filled with dummy byte and the next packet is stored in the next word, as shown in *Figure 3-2*.

NOTE: CRC data is not stored in RXFIFO.

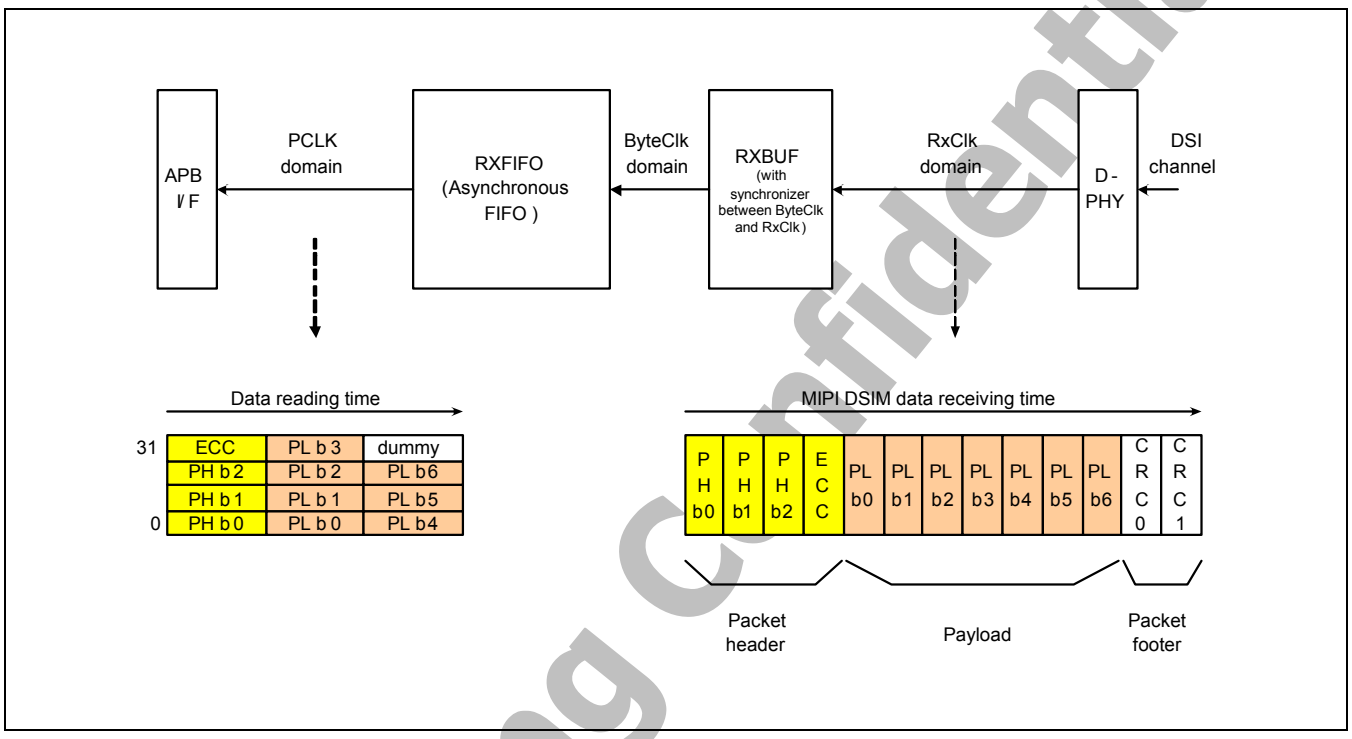

Figure 3-2 Rx Data Word Alignment

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3.1.3 INTERFACES AND PROTOCOL

Display Controller-to-DSI Conceptual Signal Converting Diagram in Video Mode

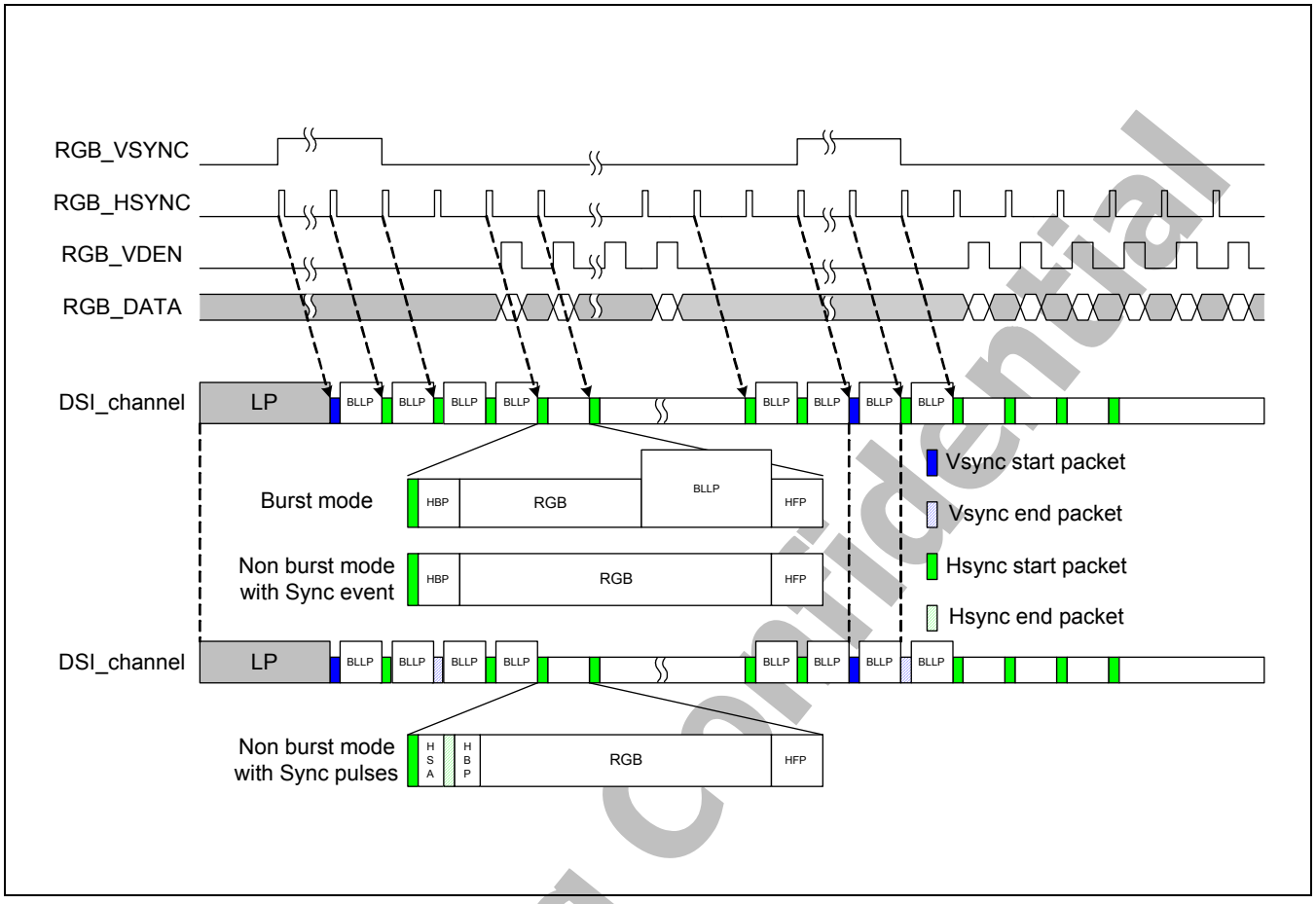

Figure 3-3 Signal Converting Diagram in Video Mode

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3.1.3.1 Interface Timing and Protocol

3.1.3.1.1 Display Controller Interface

MIPI DSI Master has two-display controller interfaces, namely, RGB INTERFACE for main display and CPU INTERFACE (I80 INTERFACE) for main/ sub display. The Video mode uses RGB INTERFACE while the Command mode uses CPU INTERFACE.

The RGB image data is loaded on the data bus of RGB INTERFACE and I80 INTERFACE with the same order: RGB_VD[23:0] or SYS_VDOUT[23:0] is {R[7:0],G[7:0],B[7:0]}. Each byte aligns to the most significant bit. For instance, in the 12-bit mode, only three 4-bit values are valid as R, G, and B each, that is, data[23:20], data[15:12], and data[7:4]. The DSIM ignores rest of the bits.

3.1.3.1.2 RGB Interface

Vsync, Hsync, and VDEN are active high signals. Among the three signals, Vsync and Hsync are pulse types that spend several video clocks. RGB_VD[23:0] is {R[7:0],G[7:0],B[7:0]}. All sync signals are synchronized to the rising edge of RGB_VCLK. The display controller sends minimum one horizontal line length of Vsync pulse, V back porch, and V front porch. Hsync pulse width should be longer than 1-byte clock cycle.

3.1.3.1.3 HSA Mode

HSA mode specifies the Horizontal Sync Pulse area disable mode.

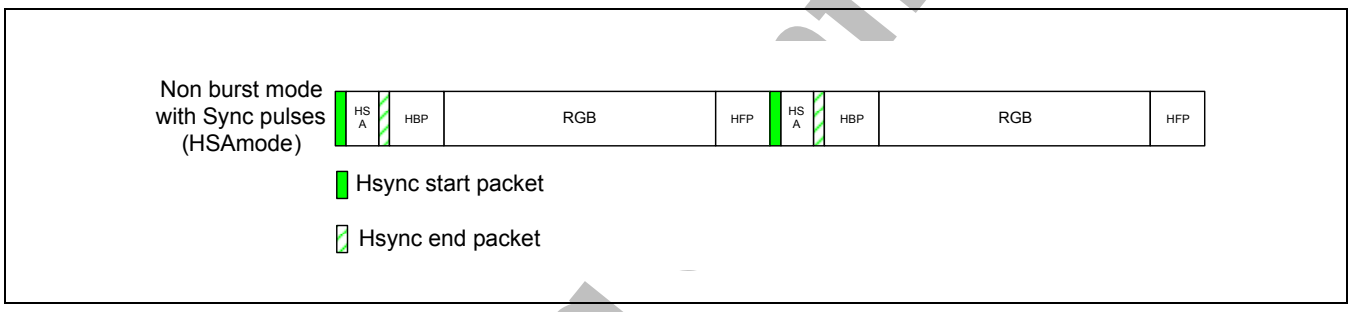

Figure 3-4 Block Timing Diagram of HSA Mode (HSA mode reset: DSIM_CONFIG[20] = 0)

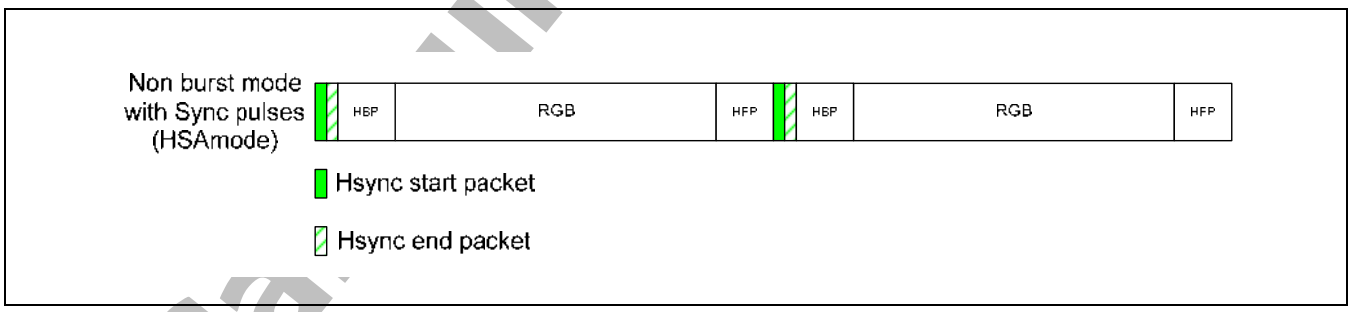

Figure 3-5 Block Timing Diagram of HSA Mode (HSA mode set: DSIM_CONFIG[20] = 1)

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HBP mode HBP mode specifies the Horizontal Back Porch disable mode.

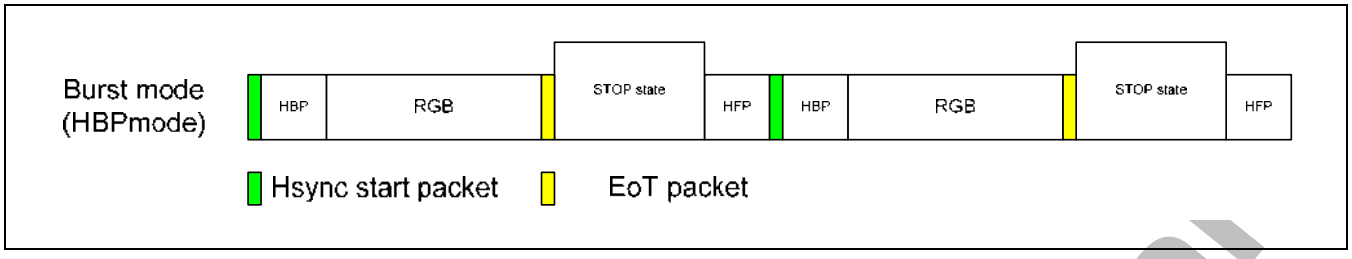

Figure 3-6 Block Timing Diagram of HBP Mode (HBP Mode Reset: DSIM_CONFIG[21] = 0)

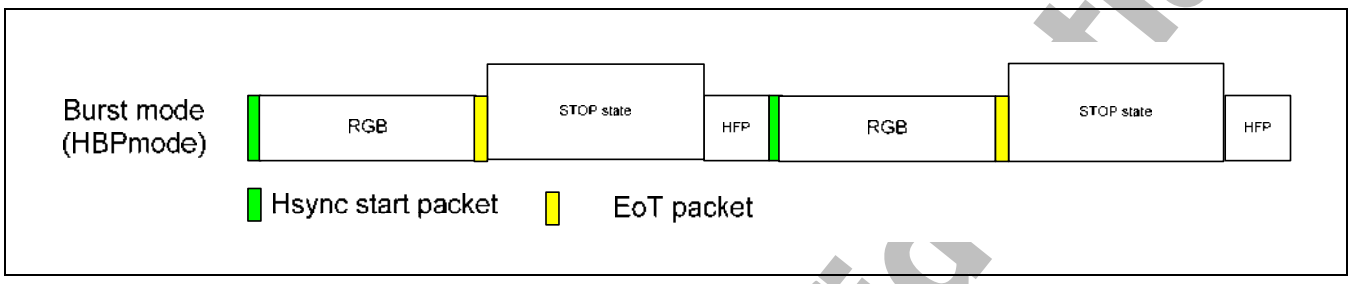

Figure 3-7 Block Timing Diagram of HBP Mode (HBP Mode Set: DSIM_CONFIG[21] = 1)

HFP mode HFP mode specifies the Horizontal Front Porch disable mode.

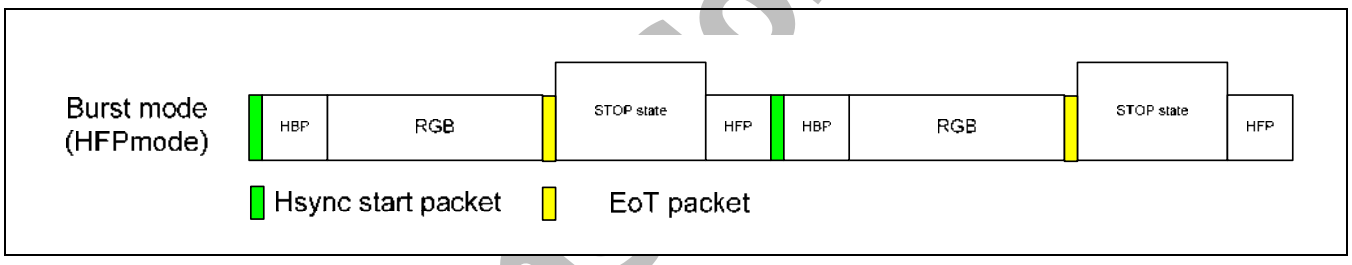

Figure 3-8 Block Timing Diagram of HFP Mode (HFP Mode Reset: DSIM_CONFIG[22] = 0)

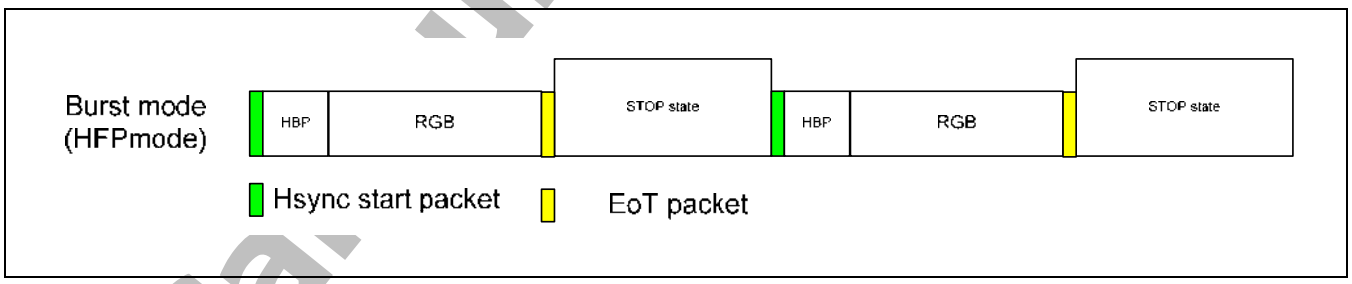

Figure 3-9 Block Timing Diagram of HFP Mode (HFP Mode Set: DSIM_CONFIG[22] = 1)

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3.1.3.1.4 HSE Mode

HSE mode specifies the Horizontal Sync End Packet Enable mode in Vsync pulse or Vporch area.

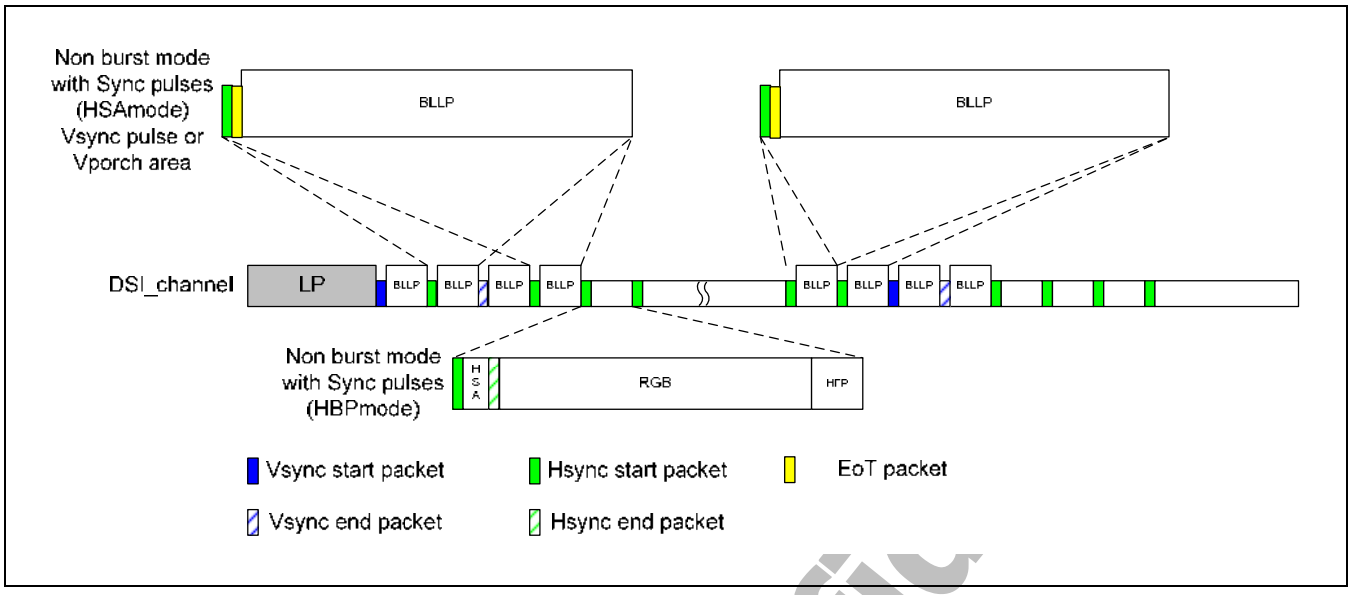

Figure 3-10 Block Timing Diagram of HSE Mode (HSE Mode Reset: DSIM_CONFIG[23] = 0)

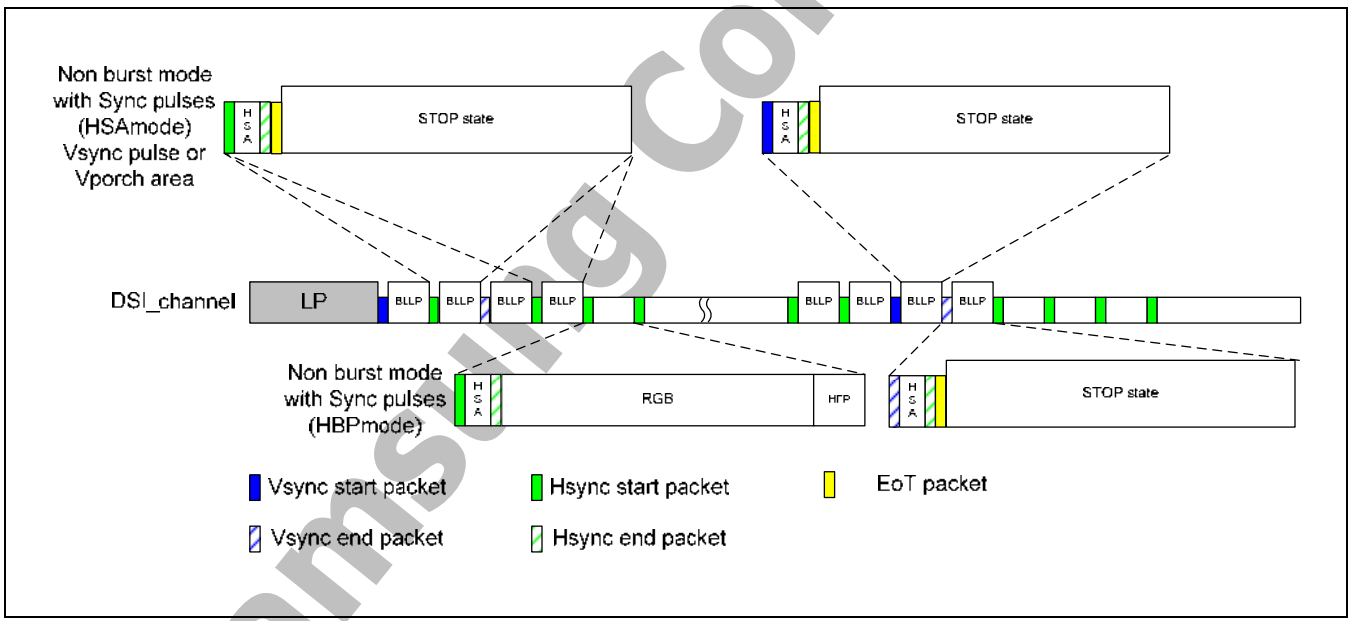

Figure 3-11 Block Timing Diagram of HSE Mode (HSE Mode Set: DSIM_CONFIG[23] = 1)

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3.1.3.1.5 Transfer General Data in Video Mode

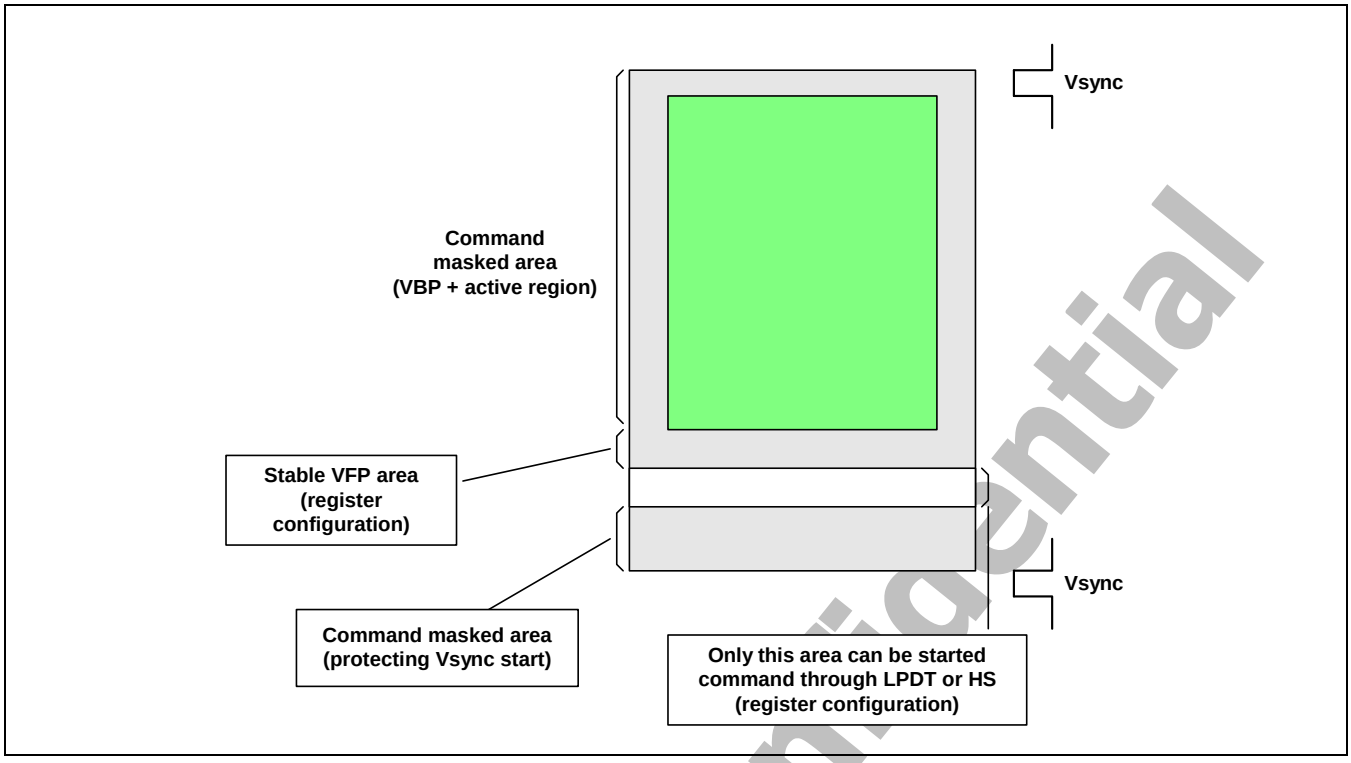

Figure 3-12 Stable VFP Area Before Command Transfer Allowing Area

3.1.3.1.6 MIPI DSIM Converts RGB Interface to Video Mode

Vsync and Hsync packets are extremely important to protect image in Video mode. MIPI DSIM allows several lines in VFP area to transfer general data transfer. As shown in *Figure 3-12*, the vertical front porch is divided into three areas, namely, stable VFP area, command allowed area, and command masked area.

The register configures stable VFP area. Configuration boundary is 11'h000 ~ 11'h7FFF in DSIM_MVPORCH.

The register also configures the command allowed area. Configuration boundary is 4'h0 ~ 4'hF in DSIM_MVPORCH. Only this area is allowed to start "command transfer" through HS mode or LPDT. In LPDT, data transferring takes a long time to complete (approximately hundreds of microseconds or more). In this time, Hsync packet does not arrive due to LPDT long packet. MIPI DSIM comprises of big size FIFO for lost Hsync packet. After LPDT, MIPI DSIM transfers these Hsync packets immediately through HS mode.

To protect Vsync, command masked area is masked area. This area is calculated using LPDT bandwidth. For example, if EscClk is 10MHz, the maximum long packet payload size is 1KB and LPDT, LPDT transferring time is 824us (packet size: 1030byte, LPDT maximum bandwidth: 10Mbps). If one line time is 20us, the line timing violation occurs in 42 lines. Therefore, command masked area is larger than 42 + α. This 'α' is transferring time of the violated Hsync packets.

Display controller should be configured in such a way that VFP lines are sum of stable vfp, command allowed area, and command masked area.

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3.1.3.1.7 I80 Interface

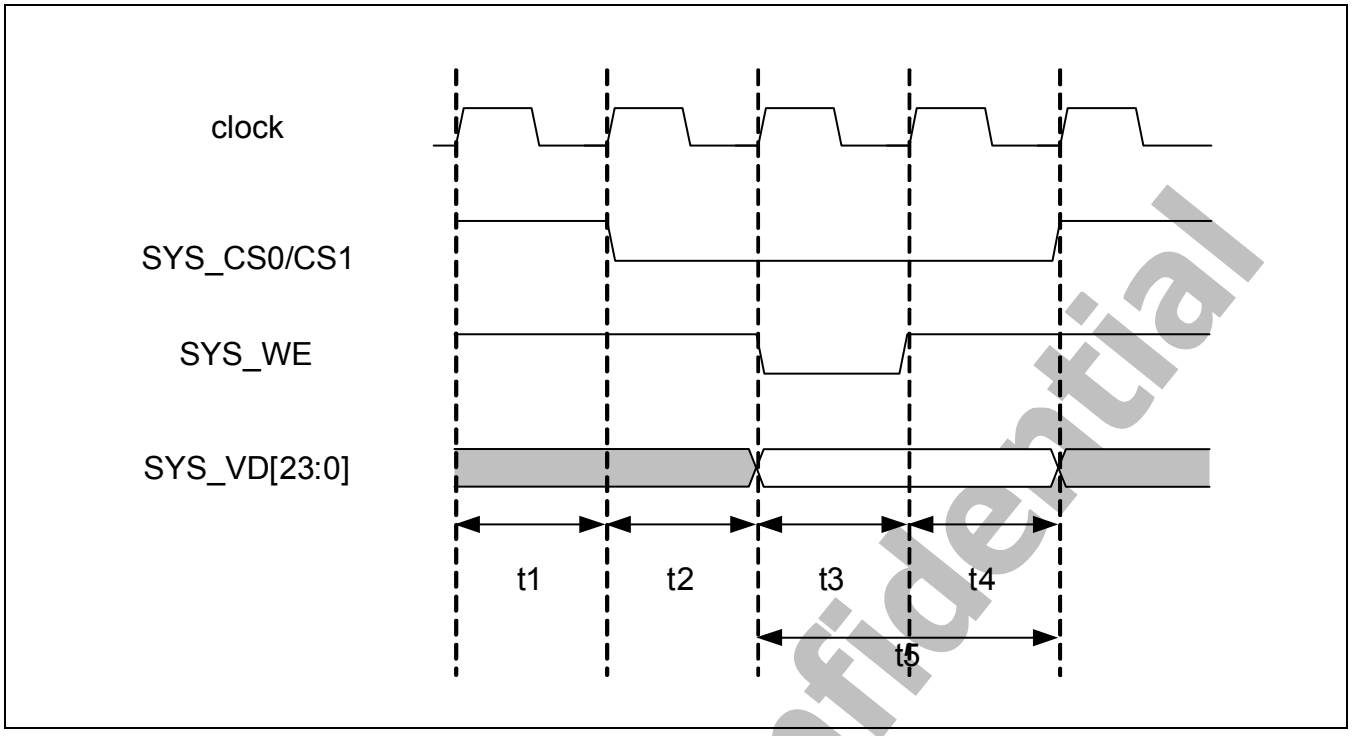

Figure 3-13 I80 Interface Timing Diagram

- T1 ≥ 1 clock cycle.
- T2 ≥ 0 clock cycle.
- T3 ≥ 1 clock cycle.
- T4 ≥ 0 clock cycle.
- T5 ≥ 1 clock cycle.
- T2+T3+T4 > 1 cycle of byte clock

A display controller generates these signals with its internal clock: SYS_CS0/CS1, SYS_WE, and SYS_VD. MIPI DSI master decodes the SYS_ADDR. *Table 3-2* describes the I80 INTERFACE address map.

Table 3-2 I80 Interface Address Map

SYS_ADDR[1:0]	Description
2'b00	Specifies the image data.
2'b01	Reserved
2'b10	Specifies the payload data.
2'b11	Specifies the packet header.

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Figure 3-14 shows how MIPI DSI Master makes packet from the image data stream via i80 INTERFACE in Command mode. MIPI DSI master makes packet from the first line with DCS command “write_memory_start” and the other lines with DCS command “write_memory_continue”.

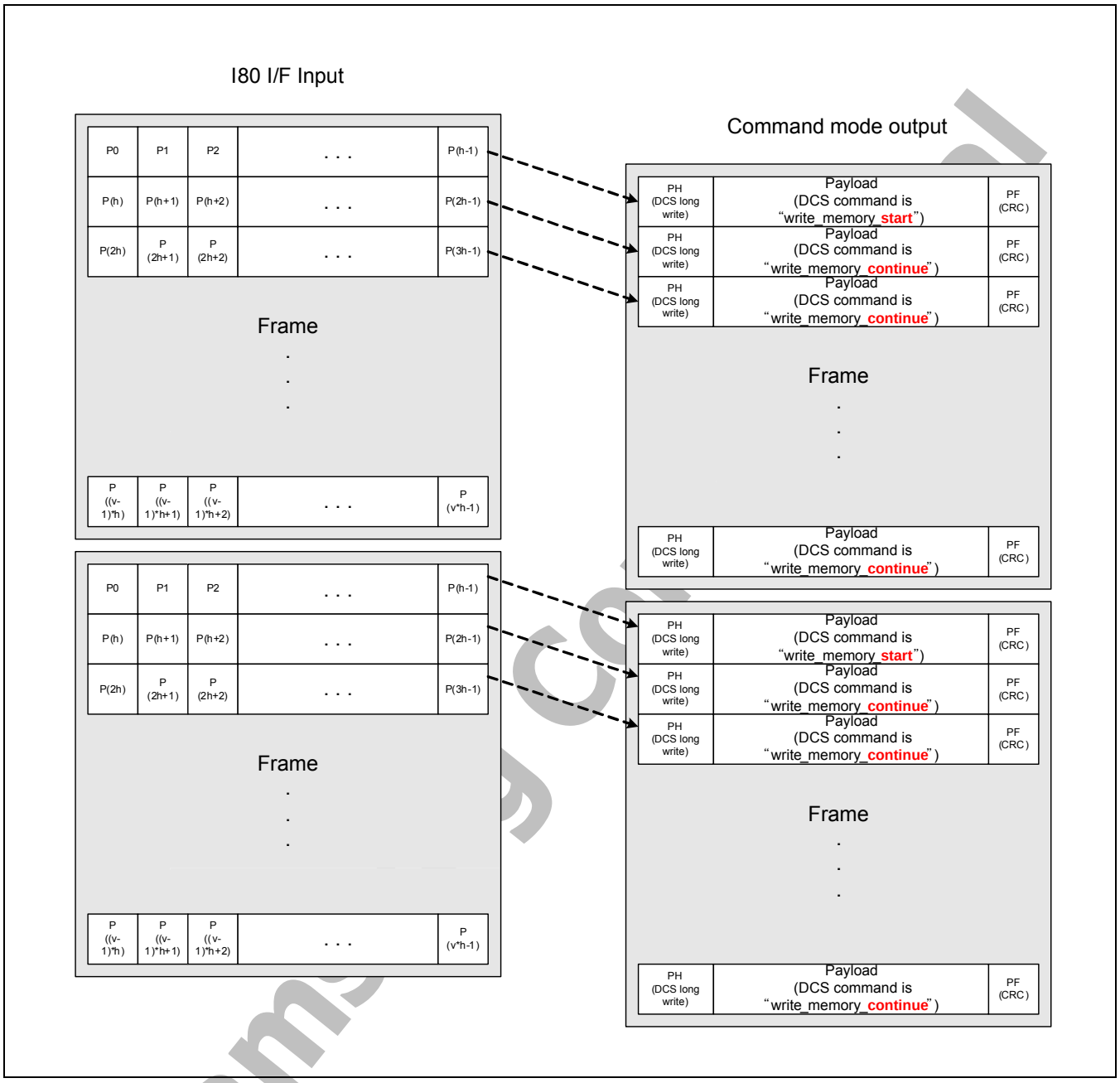

Figure 3-14 Packetizing for MIPI DSI Command Mode from I80 Interface

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3.1.3.1.8 Relation Between Input Transactions and DSI Transactions

Table 3-3 Relation Between Input Transactions and DSI Transactions

Input Interface	Input transaction	DSI Transaction
RGB	RGB transaction	Specifies the RGB Packet. 888, 666, 666 (loosely packed), and 565 should be specified via register configuration.
I80	I80 Image Transaction	Specifies the Data type, that is, “DCS Long Write packet”. (DCS command is “memory write start/continue”.)
I80	I80 Command Transaction	Specifies any DSI packet. Bytes in I80 transaction should be the same bytes in DSI packets.
SFR	Header and Payload FIFO access	Specifies any DSI Packets. Bytes in APB transaction should be the same bytes in DSI packets.

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3.1.4 CONFIGURATION

3.1.4.1 Video Mode Versus Command Mode

MIPI DSI Master Block supports two modes, namely, Video mode and Command mode.

3.1.5 DUAL DISPLAY VERSUS SINGLE DISPLAY

3.1.5.1 Dual Display

MIPI DSI Master supports dual display configuration in Command mode only, that is, both main and sub display image should be transmitted via i80 interface.

3.1.5.2 Single Display

For single display configuration, use video mode or command mode.

3.1.6 PLL

To transmit Image data, MIPI DSI Master Block needs high frequency clock (80MHz ~ 1GHz) generated by PLL.

To configure PLL, MIPI DSI Master comprises of SFRs and corresponding interface signals. PLL is embedded in PHY module. You should use other PLL in SoC if it meets the timing specification.

3.1.7 BUFFER

In MIPI DSI standard specification, DSI Master sends image stream in burst mode. The image stream transmits in high-speed and bit-clock frequency. This mode allows the device to stay in stop state longer to reduce power consumption. For this mode, MIPI DSI Master has a dual line buffer to store one complete line and send it faster at the next line time.

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3.2 I/O DESCRIPTION

Table 3-4 MIPI-DPHY Interface Slave Signal

Signal	I/O	Description	Pad	Type
MIPI_DP_0	B	Specifies the DP signal for MIPI-DPHY Master data-lane 0.	XmipiDP[0]	Dedicated
MIPI_DN_0	B	Specifies the DN signal for MIPI-DPHY Master data-lane 0.	XmipiDN[0]	Dedicated
MIPI_DP_1	O	Specifies the DP signal for MIPI-DPHY Master data-lane 1.	XmipiDP[1]	Dedicated
MIPI_DN_1	O	Specifies the DN signal for MIPI-DPHY Master data-lane 1.	XmipiDN[1]	Dedicated
MIPI_DP_2	O	Specifies the DP signal for MIPI-DPHY Master data-lane 2.	XmipiDP[2]	Dedicated
MIPI_DN_2	O	Specifies the DN signal for MIPI-DPHY Master data-lane 2.	XmipiDN[2]	Dedicated
MIPI_DP_3	O	Specifies the DP signal for MIPI-DPHY Master data-lane 3.	XmipiDP[3]	Dedicated
MIPI_DN_3	O	Specifies the DN signal for MIPI-DPHY Master data-lane 3.	XmipiDN[3]	Dedicated
MIPI_CLK_TX_P	O	Specifies the DP signal for MIPI-DPHY Master clock-lane.	XmipiCLK_TX_P	Dedicated
MIPI_CLK_TX_N	O	Specifies the DN signal for MIPI-DPHY Master clock-lane.	XmipiCLK_TX_N	Dedicated

NOTE:

1. I/O direction. I: input, O: output, and B: bi-direction.
2. Type field indicates whether pads are dedicated to the signal or pads are connected to the multiplexed signals.

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3.3 REGISTER DESCRIPTION

3.3.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
DSIM_STATUS	0xFA50_0000	R	Specifies the status register.	0x0010_010F
DSIM_SWRST	0xFA50_0004	R/W	Specifies the software reset register.	0x0000_0000
DSIM_CLKCTRL	0xFA50_0008	R/W	Specifies the clock control register.	0x0000_FFFF
DSIM_TIMEOUT	0xFA50_000C	R/W	Specifies the time out register.	0x00FF_FFFF
DSIM_CONFIG	0xFA50_0010	R/W	Specifies the configuration register.	0x0200_0000
DSIM_ESCMODE	0xFA50_0014	R/W	Specifies the escape mode register.	0x0000_0000
DSIM_MDRESOL	0xFA50_0018	R/W	Specifies the main display image resolution register.	0x0300_0400
DSIM_MVPORCH	0xFA50_001C	R/W	Specifies the main display Vporch register.	0xF000_0000
DSIM_MHPORCH	0xFA50_0020	R/W	Specifies the main display Hporch register.	0x0000_0000
DSIM_MSYNC	0xFA50_0024	R/W	Specifies the main display Sync Area register.	0x0000_0000
DSIM_SDRESOL	0xFA50_0028	R/W	Specifies the sub display image resolution register.	0x0300_0400
DSIM_INTSRC	0xFA50_002C	R/W	Specifies the interrupt source register.	0x0000_0000
DSIM_INTMSK	0xFA50_0030	R/W	Specifies the interrupt mask register.	0xB337_FFFF
DSIM_PKTHDR	0xFA50_0034	W	Specifies the packet header FIFO register.	0x0000_0000
DSIM_PAYLOAD	0xFA50_0038	W	Specifies the payload FIFO register.	0x0000_0000
DSIM_RXFIFO	0xFA50_003C	R	Specifies the read FIFO register.	0xXXXX_XXXX
DSIM_FIFOTHLD	0xFA50_0040	R/W	Specifies the FIFO threshold level register.	0x0000_01FF
DSIM_FIFOCTRL	0xFA50_0044	R	Specifies the FIFO status and control register.	0x0155_551F
DSIM_MEMACCHR	0xFA50_0048	R/W	Specifies the FIFO memory AC characteristic register.	0x0000_4040
DSIM_PLLCTRL	0xFA50_004C	R/W	Specifies the PLL control register.	0x0000_0000
DSIM_PLLTMR	0xFA50_0050	R/W	Specifies the PLL timer register.	0xFFFF_FFFF
DSIM_PHYACCHR	0xFA50_0054	R/W	Specifies the D-PHY AC characteristic register.	0x0000_0000
DSIM_PHYACCHR1	0xFA50_0058	R/W	Specifies the D-PHY AC characteristic register 1.	0x0000_0000

NOTE: M_RESETN at MIPI_PHY_CON0 (0xE010_7200) should be '1' before enabling DSIM.

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3.3.1.1 Status Register (DSIM_STATUS, R, Address = 0xFA50_0000)

This register reads and checks internal and interface status. It also checks FSM status, Line buffer status, current image line number, and so on.

DSIM_STATUS	Bit	Description	Initial State
PllStable	[31]	D-phy pll generates stable byteclk.	0
Reserved	[30:21]	Reserved	0
SwRstRls	[20]	Specifies the software reset status. 0 = Reset state 1 = Release state	0
Reserved	[19:17]	Reserved	0
Direction	[16]	Specifies the data direction indicator. 0 = Forward direction 1 = Backward direction	1
Reserved	[15:11]	Reserved	0
TxReadyHsClk	[10]	Specifies the HS clock ready at clock lane. 0 = Not ready for transmitting HS data at clock lane 1 = Ready for transmitting HS data at clock lane	0
UlpsClk	[9]	Specifies the ULPS indicator at clock lane. 0 = No ULPS in clock lane 1 = ULSP in clock lane	1
StopstateClk	[8]	Specifies the stop state indicator at clock lane. 0 = No stop state in clock lane 1 = Stop state in clock lane	0
UlpsDat[3:0]	[7:4]	Specifies the ULPS indicator at data lanes. UlpsDat[0]: Data lane 0 UlpsDat[1]: Data lane 1 UlpsDat[2]: Data lane 2 UlpsDat[3]: Data lane 3 0 = No ULPS in each data lane 1 = ULPS in each data lane	F
StopstateDat[3:0]	[3:0]	Specifies the stop state indicator at data lane. StopstateDat[0]: Data lane 0 StopstateDat[1]: Data lane 1 StopstateDat[2]: Data lane 2 StopstateDat[3]: Data lane 3 0 = No stop state in each data lane 1 = Stop state in each data lane	0

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3.3.1.2 Software Reset Register (DSIM_SWRST, R/W, Address = 0xFA50_0004)

DSIM_SWRST	Bit	Description	Initial State
Reserved	[31:17]	Reserved	-
FuncRst	[16]	Specifies the software reset (High active). "Software reset" resets all FF in MIPI DSIM (except SFRs: STATUS, SWRST, CLKCTRL,TIMEOUT,CONFIG, ESCMODE*, MDRESOL, MDVPORCH, MHPORCH, MSYNC, INTMSK, SDRESOL, FIFOTHLD, FIFOCTRL**, MEMACCHR, PLLCTRL, PLLTMR, PHYACCHR, and VERINFORM). 0 = Standby 1 = Reset *: ForceStopstate, CmdLpdt, TxLpdt, **: nInitRx, nInitSfr, nInitI80, nInitSub, nInitMD	0
Reserved	[15:1]	Reserved	-
SwRst	[0]	Specifies the software reset (High active). "Software reset" resets all FF in MIPI DSIM (except some SFRs: STATUS, SWRST, CLKCTRL, PLLCTRL, PLLTMR, and PHYTUNE). 0 = Standby 1 = Reset	0

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3.3.1.3 Clock Control Register (DSIM_CLKCTRL, R/W, Address = 0xFA50_0008)

DSIM_CLKCTRL	Bit	Description	Initial State
TxRequestHsClk	[31]	Specifies the HS clock request for HS transfer at clock lane (Turn on HS clock)	0
Reserved	[30:29]	Reserved	-
EscClkEn	[28]	Enables the escape clock generating prescaler. 0 = Disables 1 = Enables	0
PLLBypass	[27]	Sets the PLLBypass signal connected to D-PHY module input for selecting clock source bit. For more information, refer to MIPI D-PHY specification. 0 = PLL output 1 = External Serial clock	0
ByteClkSrc	[26:25]	Selects byte clock source. (It must be 00.) 00 = D-PHY PLL (default). PLL_out clock is used to generate ByteClk by dividing 8.	0
ByteClkEn	[24]	Enables byte clock. 1 = Disables 0 = Enables	0
LaneEscClkEn	[23:19]	Enables escape clock for D-phy lane. LaneEscClkEn[0] = Clock lane LaneEscClkEn[1] = Data lane 0 LaneEscClkEn[2] = Data lane 1 LaneEscClkEn[3] = Data lane 2 LaneEscClkEn[4] = Data lane 3 0 = Disables 1 = Enables	0
Reserved	[18:16]	Reserved	-
EscPrescaler	[15:0]	Specifies the escape clock prescaler value. The escape clock frequency range varies up to 20MHz. Note: The requirement for BTA is that the Host Escclk frequency should range between 66.7 ~ 150% of the peripheral escape clock frequency. EscClk = ByteClk / (EscPrescaler)	0xFFFF

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3.3.1.4 Time Out register (DSIM_TIMEOUT, R/W, Address = 0xFA50_000C)

DSIM_TIMEOUT	Bit	Description	Initial State
Reserved	[31:24]	Reserved	-
BtaTout	[23:16]	Specifies the timer for BTA. This register specifies time out from BTA request to change the direction with respect to Tx escape clock.	0xFF
LpdrTout	[15:0]	Specifies the timer for LP Rx mode timeout. This register specifies time out on how long RxValid deasserts, after RxLpdt asserts with respect to Tx escape clock. RxValid specifies Rx data valid indicator. RxLpdt specifies an indicator that D-phy is under RxLpdt mode. RxValid and RxLpdt specifies signal from D-phy.	0xFFFF

3.3.1.5 Configuration Register (DSIM_CONFIG, R/W, 0xFA50_0010)

This register configures MIPI DSI master such as data lane number, input interface, porch area, frame rate, BTA, LPDT, ULPS, and so on.

DSIM_CONFIG	Bit	Description	Initial State
Reserved	[31:30]	Reserved	-
Mflush_VS	[29]	Auto flush of MD FIFO using Vsync pulse. It needs that Main display FIFO should be flushed for deleting garbage data. 0 = Enable (defalut) 1 = Disable	1
EoT_r03	[28]	Disables EoT packet in HS mode. 0 = Enables EoT packet generation for V1.01r11 1 = Disables EoT packet generation for V1.01r03	0
SyncInform	[27]	Selects Sync Pulse or Event mode in Video mode. 0 = Event mode (non burst, burst) 1 = Pulse mode (non burst only) In command mode, this bit is ignored.	0
BurstMode	[26]	Selects Burst mode in Video mode In Non-burst mode, RGB data area is filled with RGB data and Null packets, according to input bandwidth of RGB interface. In Burst mode, RGB data area is filled with RGB data only. 0 = Non-burst mode 1 = Burst mode In command mode, this bit is ignored.	0
VideoMode	[25]	Specifies display configuration. 0 = Command mode 1 = Video mode	1

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DSIM_CONFIG	Bit	Description	Initial State
AutoMode	[24]	Specifies auto vertical count mode. In Video mode, the vertical line transition uses line counter configured by VSA, VBP, and Vertical resolution. If this bit is set to '1', the line counter does not use VSA and VBP registers. 0 = Configuration mode 1 = Auto mode In command mode, this bit is ignored.	0
HseMode	[23]	In Vsync pulse and Vporch area, MIPI DSI master transfers only Hsync start packet to MIPI DSI slave at MIPI DSI spec 1.1r02. This bit transfers Hsync end packet in Vsync pulse and Vporch area (optional). 0 = Disables transfer 1 = Enables transfer In command mode, this bit is ignored.	0
HfpMode	[22]	Specifies HFP disable mode. If this bit set, DSI master ignores HFP area in Video mode. 0 = Enables 1 = Disables In command mode, this bit is ignored.	0
HbpMode	[21]	Specifies HBP disable mode. If this bit set, DSI master ignores HBP area in Video mode. 0 = Enables 1 = Disables In command mode, this bit is ignored.	0
HsaMode	[20]	Specifies HSA disable mode. If this bit set, DSI master ignores HSA area in Video mode. 0 = Enables 1 = Disables In command mode, this bit is ignored.	0
MainVc	[19:18]	Specifies virtual channel number for main display.	0
SubVc	[17:16]	Specifies virtual channel number for sub display.	0
Reserved	[15]	Reserved	-
MainPixFormat	[14:12]	Specifies pixel stream format for main display. 000 = 3bpp (for Command mode only) 001 = 8bpp (for Command mode only) 010 = 12bpp (for Command mode only) 011 = 16bpp (for Command mode only) 100 = 16-bit RGB (565) (for Video mode only) 101 = 18-bit RGB (666: packed pixel stream) (for Video mode only) 110 = 18-bit RGB (666: loosely packed pixel stream) for Common 111 = 24-bit RGB (888) for common	0

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DSIM_CONFIG	Bit	Description	Initial State
Reserved	[11]	Reserved	-
SubPixFormat	[10:8]	Specifies pixel stream format for sub display. 000 = 3bpp (for Command mode only) 001 = 8bpp (for Command mode only) 010 = 12bpp (for Command mode only) 011 = 16bpp (for Command mode only) 100 = 16-bit RGB (565) (for Video mode only) 101 = 18-bit RGB (666: packed pixel stream) for Video mode only) 110 = 18-bit RGB (666: loosely packed pixel stream) for common) 111 = 24-bit RGB (888) (for Common)	0
Reserved	[7]	Reserved	-
NumOfDatLane	[6:5]	Sets the data lane number. 00 = Data lane 0 (1 data lane) 01 = Data lane 0 ~ 1 (2 data lanes) 10 = Data lane 0 ~ 2 (3 data lanes) 11 = Data lane 0 ~ 3 (4 data lanes)	0
LaneEn[4:0]	[4:0]	Enables the lane. If Lane_EN is disabled, the lane ignores input and drives initial value through output port. 0 = Lane is off. 1 = Lane is on. LaneEn[0] = Clock lane enabler LaneEn[1] = Data lane 0 enabler LaneEn[2] = Data lane 1 enabler LaneEn[3] = Data lane 2 enabler LaneEn[4] = Data lane 3 enabler	0

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3.3.1.6 Escape Mode Register (DSIM_ESCMODE, R/W, Address = 0xFA50_0014)

This register configures MIPI DSI master.

DSIM_ESCMODE	Bit	Description	Initial State
STOPstate_Cnt	[31:21]	After transmitting read packet or write “set_tear_on” command, BTA requests to D-phy automatically. This counter value specifies the interval value between transmitting read packet (or write “set_tear_on” command) and BTA request. 11'h000 = 2 EscClk 11'h001 = 2 EscClk + 1 EscClk ~ 11'h3FF = 2 EscClk + 1023 EscClk	0
ForceStopstate	[20]	Forces Stopstate for D-PHY.	0
Reserved	[19:17]	Reserved	-
ForceBta	[16]	Forces Bus Turn Around. 1 = Sends the protocol layer request to D-PHY. MIPI DSI peripheral becomes master after BTA sequence. This bit clears automatically after receiving BTA acknowledge from MIPI DSI peripheral.	0
Reserved	[15:8]	Reserved	-
CmdLpdt	[7]	Specifies LPDT transfers command in SFR FIFO. 0 = HS Mode 1 = LP Mode	0
TxLpdt	[6]	Specifies data transmission in LP mode (all data transfer in LPDT). 0 = HS Mode 1 = LP Mode	0
Reserved	[5]	Reserved	-
TxTriggerRst	[4]	Specifies remote reset trigger function. After trigger operation, these bits will be cleared automatically.	0
TxUlpsDat	[3]	Specifies ULPS request for data lane. Manually clears after ULPS exit.	0
TxUlpsExit	[2]	Specifies ULPS exit request for data lane. Manually clears after ULPS exit.	0
TxUlpsClk	[1]	Specifies ULPS request for clock lane. Manually clears after ULPS exit.	0
TxUlpsClkExit	[0]	Specifies ULPS exit request for clock lane. Manually clears after ULPS exit.	0

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3.3.1.7 Main Display Image Resolution Register (DSIM_MDRESOL, R/W, Address = 0xFA50_0018)

DSIM_MDRESOL	Bit	Description	Initial State
MainStandby	[31]	Specifies standby for receiving DISPCON output in Command mode after setting all configuration. 0 = Not ready 1 = Stand by Standby should be set after configuration (resolution, reqtype, pixelform, and so on) is set for command mode. In Video mode, if this bit value is 0, data is not transferred.	0
Reserved	[30:27]	Reserved	-
MainVResol[10:0]	[26:16]	Specifies Vertical resolution (1 ~ 768).	0x300
Reserved	[15:11]	Reserved	-
MainHResol[10:0]	[10:0]	Specifies Horizontal resolution (1 ~ 1024).	0x400

3.3.1.8 Main Display VPORCH Register (DSIM_MVPORCH, R/W, Address = 0xFA50_001C)

DSIM_MVPORCH	Bit	Description	Initial State
CmdAllow	[31:28]	Specifies the number of horizontal lines, where command packet transmission is allowed after Stable VFP period. For more information, see *Figure 3-12*	0xF
Reserved	[27]	Reserved	-
StableVfp[10:0]	[26:16]	Specifies the number of horizontal lines, where command packet transmission is not allowed after end of active region. For more information, see *Figure 3-12* *Note: In Command mode, these bits are ignored.	0
Reserved	[15:11]	Reserved	-
MainVbp[10:0]	[10:0]	Specifies vertical back porch width for Video mode (line count). In Command mode, these bits are ignored.	0

NOTE: * Transfers command packets after Stable VFP area. Display controller VFP lines should be set based on sum of these values: Stable VFP, command allowing area and command masked area. See the section for transferring general data in Video mode.

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3.3.1.9 Main Display HPORCH Register (DSIM_MHPORCH, R/W, Address = 0xFA50_0020)

DSIM_MHPORCH	Bit	Description	Initial State
MainHfp[15:0]	[31:16]	Specifies the horizontal front porch width for Video mode. HFP is specified using blank packet. These bits specify the word counts for blank packet in HFP. In Command mode, these bits are ignored.	0
MainHbp[15:0]	[15:0]	Specifies the horizontal back porch width for Video mode. HBP is specified using blank packet. These bits specify the word counts for blank packet in HBP. In Command mode, these bits are ignored.	0

3.3.1.10 Main Display Sync Area Register (DSIM_MSYNC, R/W, Address = 0xFA50_0024)

DSIM_MSYNC	Bit	Description	Initial State
MainVsa[9:0]	[31:22]	Specifies the vertical sync pulse width for Video mode (Line count). In command mode, these bits are ignored.	0
Reserved	[21:16]	Reserved	-
MianHsa[15:0]	[15:0]	Specifies the horizontal sync pulse width for Video mode. HSA is specified using blank packet. These bits specify word counts for blank packet in HSA. In command mode, these bits are ignored.	0

3.3.1.11 Sub Display Image Resolution Register (DSIM_SDRESOL, R/W, Address = 0xFA50_0028)

DSIM_SDRESOL	Bit	Description	Initial State
SubStandby	[31]	Specifies standby for receiving DISPCON output in Command mode after setting all configuration. 0 = Not ready 1 = Standby Standby should be set after configuration (resolution, reqtype, pixelform, and so on) is set for command mode. In Video mode, this bit is ignored.	0
Reserved	[30:27]	Reserved	-
SubVResol[10:0]	[26:16]	Specifies the Vertical resolution (1 ~ 768).	0x300
Reserved	[15:11]	Reserved	-
SubHResol[10:0]	[10:0]	Specifies the Horizontal resolution (1 ~ 1024).	0x400

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3.3.1.12 Interrupt Source Register (DSIM_INTSRC, R/W, Address = 0xFA50_002C)

This register identifies interrupt sources.
Internal block error, data transmit interrupt, inter-layer (D_PHY) error, etc.
The bits are set even if they are masked off by DSIM_INTMSK_REG.
Write '1' to clear the Interrupt.

DSIM_INTSRC	Bit	Description	Initial State
PllStable	[31]	Indicates that D-phy PLL is stable.	0
SwRstRelease	[30]	Releases the software reset.	0
SFRFifoEmpty	[29]	Specifies the SFR payload FIFO empty.	0
Reserved	[28:26]	Reserved	-
BusTurnOver	[25]	Indicates when bus grant turns over from DSI slave to DSI master.	0
FrameDone	[24]	Indicates when MIPI DSIM transfers the whole image frame. Note: If Hsync is not received during two line times, internal timer is timed out and this bit is flagged.	0
Reserved	[23:22]	Reserved	-
LpdrTout	[21]	Specifies the LP Rx timeout. See time out register (0x10).	0
TaTout	[20]	Turns around Acknowledge Timeout. See time out register (0x10).	0
Reserved	[19]	Reserved	-
RxDatDone	[18]	Completes receiving data.	0
RxTE	[17]	Receives TE Rx trigger.	0
RxAck	[16]	Receives ACK Rx trigger.	0
ErrRxECC	[15]	Specifies the ECC multi bit error in LPDR.	0
ErrRxCRC	[14]	Specifies the CRC error in LPDR.	0
ErrEsc3	[13]	Specifies the escape mode entry error lane 3. For more information, refer to standard D-PHY specification.	0
ErrEsc2	[12]	Specifies the escape mode entry error lane 2. For more information, refer to standard D-PHY specification.	0
ErrEsc1	[11]	Specifies the escape mode entry error lane 1. For more information, refer to standard D-PHY specification.	0
ErrEsc0	[10]	Specifies the escape mode entry error lane 0. For more information, refer to standard D-PHY specification.	0
ErrSync2	[9]	Specifies the LPDT sync error lane 3. For more information, refer to standard D-PHY specification.	0
ErrSync2	[8]	Specifies the LPDT Sync Error lane2. For more information, refer to standard D-PHY specification.	0
ErrSync1	[7]	Specifies the LPDT Sync Error lane1. For more information, refer to standard D-PHY specification.	0
ErrSync0	[6]	Specifies the LPDT Sync Error lane0. For more information, refer to standard D-PHY specification.	0

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DSIM_INTSRC	Bit	Description	Initial State
ErrControl2	[5]	Controls Error lane3. For more information, refer to standard D-PHY specification.	0
ErrControl2	[4]	Controls Error lane2. For more information, refer to standard D-PHY specification.	0
ErrControl1	[3]	Controls Error lane1. For more information, refer to standard D-PHY specification.	0
ErrControl0	[2]	Controls Error lane0. For more information, refer to standard D-PHY specification.	0
ErrContentLP0	[1]	Specifies the LP0 Contention Error (only lane0, because BTA occurs at lane0 only). For more information, refer to standard D-PHY specification.	0
ErrContentLP1	[0]	Specifies the LP1 Contention Error (only lane0, because BTA occurs at lane0 only). For more information, refer to standard D-PHY specification.	0

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3.3.1.13 Interrupt Mask Register (DSIM_INTMSK, R/W, Address = 0xFA50_0030)

This register masks interrupt sources.

DSIM_INTMSK	Bit	Description	Initial State
MskPllStable	[31]	Indicates that D-PHY PLL is stable.	-
MskSwRstRelease	[30]	Releases software reset.	0
MskSFRFifoEmpty	[29]	Empties SFR payload FIFO.	1
Reserved	[28:26]	Reserved	-
MskBusTurnOver	[25]	Indicates when bus grant turns over from DSI slave to DSI master.	1
MskFrameDone	[24]	Indicates when MIPI DSIM transfers whole image frame.	1
Reserved	[23:22]	Reserved	-
MskLpdrTout	[21]	Specifies LP Rx timeout. See time out register (0x10).	1
MskTaTout	[20]	Specifies turnaround acknowledge timeout. See time out register (0x10)	1
Reserved	[19]	Reserved	-
MskRxDatDone	[18]	Specifies completion of data receiving.	1
MskRxTE	[17]	Specifies receipt of TE Rx trigger.	1
MskRxAck	[16]	Specifies receipt of ACK Rx trigger.	1
MskRxECC	[15]	Specifies ECC multibit error in LPDR.	1
MskRxCRC	[14]	Specifies CRC error in LPDR.	1
MskEsc3	[13]	Specifies escape mode entry error in lane3. For more information, refer to standard D-PHY specification.	1
MskEsc2	[12]	Specifies escape mode entry error in lane2. For more information, refer to standard D-PHY specification.	1
MskEsc1	[11]	Specifies escape mode entry error in lane1. For more information, refer to standard D-PHY specification.	1
MskEsc0	[10]	Specifies escape mode entry error in lane0. For more information, refer to standard D-PHY specification.	1
MskSync3	[9]	Specifies LPDT sync error in lane3. For more information, refer to standard D-PHY specification.	1
MskSync2	[8]	Specifies LPDT sync error in lane2. For more information, refer to standard D-PHY specification.	1
MskSync1	[7]	Specifies LPDT sync error in lane1. For more information, refer to standard D-PHY specification.	1
MskSync0	[6]	Specifies LPDT sync error in lane0. For more information, refer to standard D-PHY specification.	1
MskControl3	[4]	Controls error in lane3. For more information, refer to standard D-PHY specification.	1
MskControl2	[4]	Controls error in lane2. For more information, refer to standard D-PHY specification.	1
MskControl1	[3]	Controls error in lane1. For more information, refer to	1

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DSIM_INTMSK	Bit	Description	Initial State
		standard D-PHY specification.	
MskControl0	[2]	Controls error in lane0. For more information, refer to standard D-PHY specification.	1
MskContentLP0	[1]	Specifies LP0 contention error. For more information, refer to standard D-PHY specification.	1
MskContentLP1	[0]	Specifies LP1 contention error. For more information, refer to standard D-PHY specification.	1

3.3.1.14 Packet Header FIFO Register (DSIM_PKTHDR, W, Address = 0xFA50_0034)

This register is the FIFO for packet header to send DSI packets.

DSIM_PKTHDR	Bit	Description	Initial State
Reserved	[31:24]	Reserved	-
PacketHeader	[23:0]	Writes the packet header of Tx packet. [7:0] = DI [15:8] = Dat0 (Word Count lower byte for long packet) [23:16] = Dat1 (Word Count upper byte for long packet)	0

3.3.1.15 Payload FIFO Register (DSIM_PAYLOAD, W, Address = 0xFA50_0038)

This register specifies the FIFO for payload to send DSI packets.

DSIM_PAYLOAD	Bit	Description	Initial State
Payload	[31:0]	Writes the Payload of Tx packet.	0

3.3.1.16 Read FIFO Register (DSIM_RXFIFO, R, Address = 0xFA50_003C)

This register is the gate of FIFO read

DSIM_RXFIFO	Bit	Description	Initial State
RxDat	[31:0]	In the Rx mode, you can read Rx data through this register. Note that the CRC in packet is not stored in RxFIFO.	Unknown

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3.3.1.17 PLL Control Register (DSIM_PLLCTRL, R/W, Address = 0xFA50_004C)

This register configures PLL control, D-PHY, clock range indication, and so on.

DSIM_PLLCTRL	Bit	Description	Initial State
Reserved	[31:28]	Should be 0.	-
FreqBand[3:0]	[27:24]	Indicates Bitclk frequency band for D-PHY global timing. For more information, refer to *Table 3-7*.	0
PllEn	[23]	Enables PLL.	0
Reserved	[22:20]	Should be 0.	-
PMS[19:1]	[19:1]	Specifies the PLL PMS value.	0
Reserved	[0]	Reserved	0

3.3.1.18 PLL Timer Register (DSIM_PLLTMR, R/W, Address = 0xFA50_0050)

DSIM_PLLTMR	Bit	Description	Initial State
PllTimer	[31:0]	Specifies the PLL Timer for stability of the generated clock (System clock cycle base). If the timer value goes to 0x00000000, the clock stable bit of status and interrupt register is set.	0xFFFFFFFF

3.3.1.19 DSIM D-PHY AC Characteristic Register (DSIM_PHYACCHR, R/W, Address = 0xFA50_0054)

DSIM_PHYACCHR	Bit	Description	Initial State
Reserved	[31:15]	Reserved. Should be 0.	0
AFC_EN	[14]	Enables AFC. 0 = Disables 1 = Enables	0
Reserved	[13:8]	Reserved. Should be 0.	0
AFC_CTL	[7:5]	Specifies the AFC control value for MIPI DPHY. This value is meaningful when AFC_EN is 1. Refer to Table 8.7-6 for more information.	0
Reserved	[4:0]	Reserved. Should be 0.	0

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3.3.1.20 DSIM D-PHY AC Characteristic Register 1 (DSIM_PHYACCCHR1, R/W, Address = 0xFA50_0058)

DSIM_PHYACCHR	Bit	Description	Initial State
Reserved	[31:7]	Reserved. Should be 0.	0
Reserved	[6:4]	Reserved	0
Reserved	[3:2]	Reserved	0
DpDnSwap_CLK	[1]	Swaps Dp/Dn channel of clock lane. If this bit is set, Dp and Dn channel swap each other.	0
DpDnSwap_DAT	[0]	Swaps Dp/Dn channel of Data lanes. If this bit is set, Dp and Dn channel swap each other.	0

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3.4 DPHY PLL CONTROL

3.4.1 PMS SETTING SAMPLE FOR MIPI PLL

3.4.1.1 PMS Setting

Writes a value to PMS field in DSIM_PLLCTRL (0xFA50_004C) to set PMS value for DPHY PLL. Each P, M, and S resides in PMS [18:13], PMS[12:4], and PMS[3:1] .

Before setting the PMS value, follow these instructions:

1. Do not set the P or M value as zero, since setting the P(00000) or M(0000000000) causes malfunction of the PLL.
2. The selected M value should be chosen within the range of 41~125 for PLL stability. The VCO output frequency range of MIPI_PLL varies from 500MHz to 1000MHz
3. Keep to range of Fin_pll varies from 6 MHz to 12 MHz, using P code setting.

Table 3-5 PMS and Frequency Constraint

	Function	Value	Description
Fin	Fin	6~200MHz	Specifies PLL input frequency.
Fin_pll	Fin/P	6 ~ 12 MHz	Specifies PFD input frequency.
VCO_out	(M*Fin)/P	500 ~ 1000 MHz	Specifies VCO output frequency.
Fout	(M*Fin)/(P*2^S)	15.625 ~ 1000 MHz	Specifies PLL output frequency.
P[5:0]	P	1 ~ 63	Specifies PMS[18:13].
M[8:0]	M	20 ~ 511	Specifies PMS[12:4].
S[2:0]	2^S	1, 2, 4, 8, 16, 32	Specifies PMS[3:1].

Table 3-6 AFC Code

Serial Clock	AFC_CTL[2:0]
6 ~ 6.99 MHz	001
7 ~ 7.99 MHz	000
8 ~ 8.99 MHz	011
9 ~ 9.99 MHz	010
10 ~ 10.99 MHz	101
11 ~ 12 MHz	100

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Table 3-7 Band Control Setting

Serial Clock (= ByteClk X 8)	FreqBand[3:0]
~ 99.99 MHz	0000
100 ~ 119.99 MHz	0001
120 ~ 159.99 MHz	0010
160 ~ 199.99 MHz	0011
200 ~ 239.99 MHz	0100
140 ~ 319.99 MHz	0101
320 ~ 389.99 MHz	0110
390 ~ 449.99 MHz	0111
450 ~ 509.99 MHz	1000
510 ~ 559.99 MHz	1001
560 ~ 639.99 MHz	1010
640 ~ 689.99 MHz	1011
690 ~ 769.99 MHz	1100
770 ~ 869.99 MHz	1101
870 ~ 949.99 MHz	1110
950 ~ 1000 MHz	1111

3.4.1.2 Sample for Fout 80 MHz

To set PMS value for Fout 80 MHz, refer to the following table.

	Case 1	Case 2
Fin	24MHz	30MHz
Fin_pll	8MHz	10MHz
P[5:0]	3	3
M[8:0]	80	64
S[2:0]	8	8
VCO_out	640MHz	640MHz
Fout	80MHz	80MHz

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3.4.1.3 Sample for Fout 1000 MHz

To set PMS value for Fout 1000 MHz, refer to the following table.

	Case 1	Case 2
Fin	24MHz	30MHz
Fin_pll	8MHz	10MHz
P[5:0]	3	3
M[9:0]	125	100
S[2:0]	1	1
VCO_out	1000MHz	1000MHz
Fout	1000MHz	1000MHz

3.4.1.4 Sample for Fout 999 MHz

To set PMS value for Fout 999 MHz, refer to the following table.

	Case 1	Case 2
Fin	27MHz	9MHz
Fin_pll	9MHz	9MHz
P[5:0]	3	1
M[9:0]	111	111
S[2:0]	1	1
VCO_out	999MHz	999MHz
Fout	999MHz	999MHz

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4 MIPI CSIS

4.1 OVERVIEW OF MIPI CSIS

The key features of MIPI CSIS include:

- Compliance to MIPI CSI2 Standard Specification Version 1.0
  - Supports 1, 2, 3, or 4 data lanes
  - Supports 1 channel
  - Supports RAW8, RAW10, RAW12, and YUV422 8-bit
  - All of User defined Byte-based Data packet

- Interfaces
  - Compatible with PPI (Protocol-to-PHY Interface) in MIPI D-PHY Specification Version 0.90

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4.2 BLOCK DIAGRAM

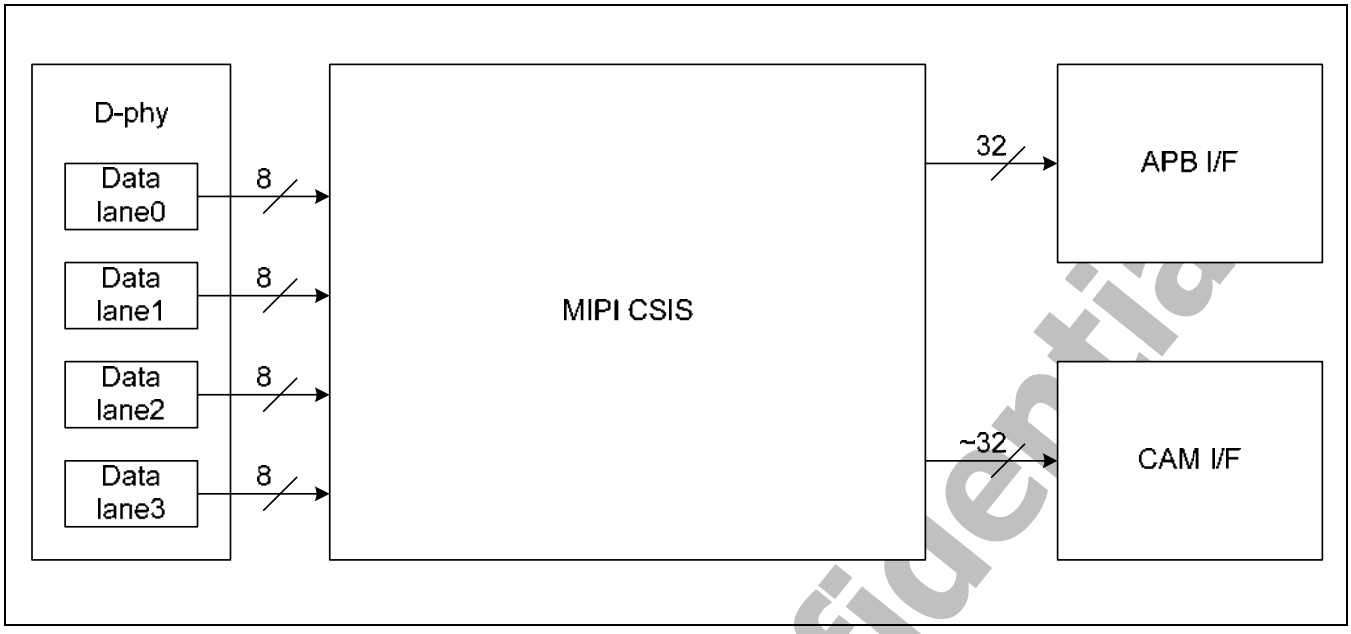

Figure 4-1 MIPI CSI System Block Diagram

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4.3 INTERFACE AND PROTOCOL

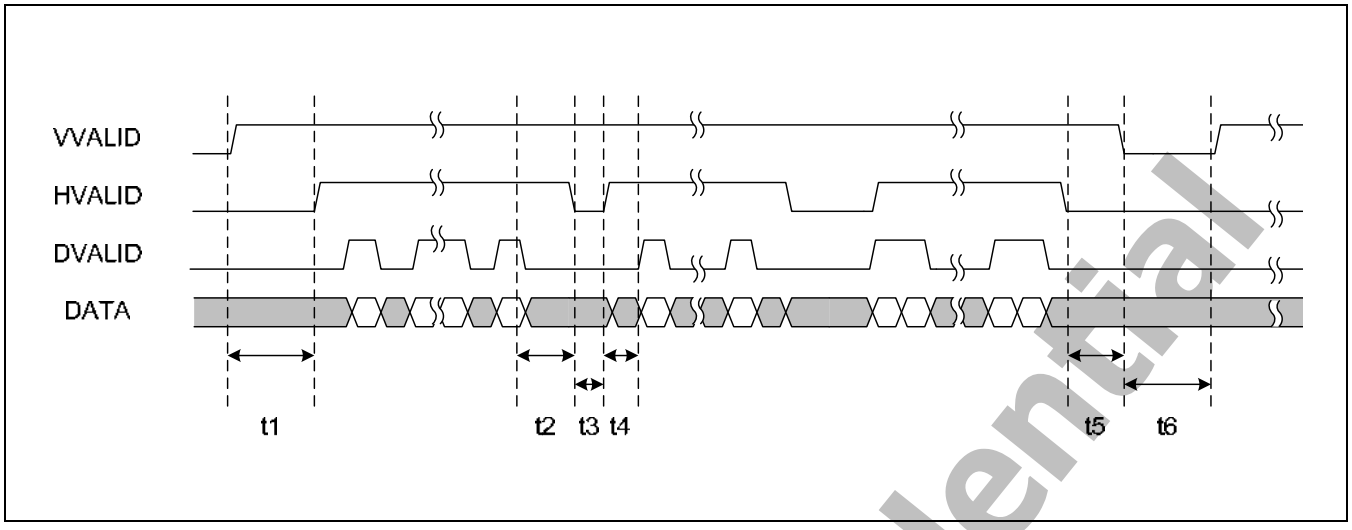

Figure 4-2 Waveform of Output Data

Table 4-1 Timing Diagram of Output Data

	Description	Minimum Cycle of Pixel Clock
t1	Specifies the interval between rising of VVALID and first rising of HVALID.	Vsync_SIntv + 1 (1 ~ 64)
t2	Specifies the interval between last falling of DVALID and falling of HVALID.	Hsync_LIntv + 2 (2 ~ 66)
t3	Specifies the interval between falling of HVALID and rising of next HVALID.	1
t4	Specifies the interval between rising of HVALID and first rising of DVALID.	0
t5	Specifies the interval between last falling of HVALID and falling of VVALID.	Vsync_EIntv (0 ~ 4095)
t6	Specifies the interval between falling of VVALID and rising of next VVALID.	1

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4.4 DATA FORMAT

4.4.1 DATA ALIGNMENT

CSIS supports two type of data alignment, as illustrated in *Figure 4-3*.

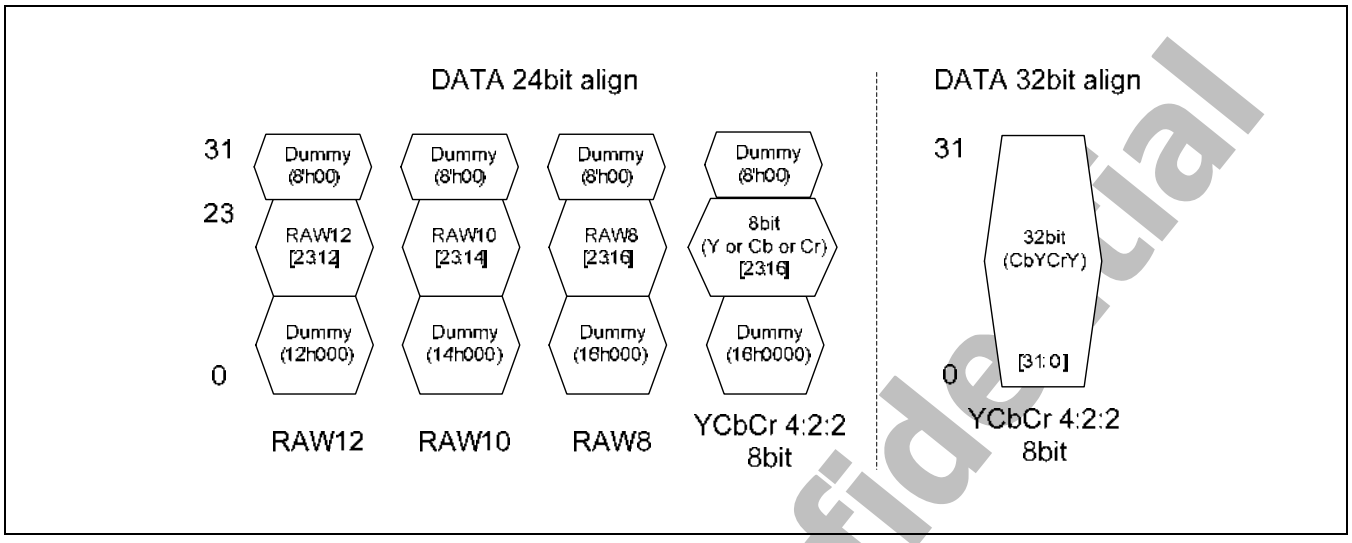

Figure 4-3 MIPI CSIS Data Alignment

4.4.2 YUV422 8-BIT ORDER

YUV422 8-bit format data is stored as a UYVY sequence, as specified in *Table 4-2*.

Table 4-2 Data Order of YUV422 Alignment

Format	Stream Order of content	24-bit Alignment	32-bit Alignment
YUV422 8-bit	U1→Y1→V1→Y2→ ...	DATA1[23:16] = U1	DATA1[31:24] = U1
		DATA2[23:16] = Y1	DATA1[23:16] = Y1
		DATA3[23:16] = V1	DATA1[15:8] = V1
		DATA4[23:16] = Y2	DATA1[7:0] = Y2

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4.5 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
DPDATA0	B	Specifies the DP signal for MIPI-DPHY slave data-lane 0.	XmipiSDP0	Dedicated
DNDATA0	B	Specifies the DN signal for MIPI-DPHY slave data-lane 0.	XmipiSDN0	Dedicated
DPDATA1	B	Specifies the DP signal for MIPI-DPHY slave data-lane 1.	XmipiSDP1	Dedicated
DNDATA1	B	Specifies the DN signal for MIPI-DPHY slave data-lane 1.	XmipiSDN1	Dedicated
DPDATA2	B	Specifies the DP signal for MIPI-DPHY slave data-lane 2.	XmipiSDP2	Dedicated
DNDATA2	B	Specifies the DN signal for MIPI-DPHY slave data-lane 2.	XmipiSDN2	Dedicated
DPDATA3	B	Specifies the DP signal for MIPI-DPHY slave data-lane 3.	XmipiSDP3	Dedicated
DNDATA3	B	Specifies the DN signal for MIPI-DPHY slave data-lane 3.	XmipiSDN3	Dedicated
DPCLK	B	Specifies the DP signal for MIPI-DPHY slave clock-lane.	XmipiSDPCLK	Dedicated
DNCLK	B	Specifies the DN signal for MIPI-DPHY slave clock-lane.	XmipiSDNCLK	Dedicated

NOTE:

1. I/O direction. I: input, O: output, and B: bi-direction.
2. Type field indicates whether pads are dedicated to signal or connected to the multiplexed signals.

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4.6 REGISTER DESCRIPTION

4.6.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
CSIS_CONTROL	0xFA60_0000	R/W	Specifies the control register.	0x0010_0000
CSIS_DPHYCTRL	0xFA60_0004	R/W	Specifies the D-PHY control register.	0x0000_0000
CSIS_CONFIG	0xFA60_0008	R/W	Specifies the configuration register.	0x0000_0000
CSIS_DPHYSTS	0xFA60_000C	R	Specifies the D-PHY stop state register.	0x0000_00F1
CSIS_INTMSK	0xFA60_0010	R/W	Specifies the interrupt mask register.	0x0000_0000
CSIS_INTSRC	0xFA60_0014	R/W	Specifies the interrupt status register.	0x0000_0000
CSIS_RESOL	0xFA60_002C	R/W	Specifies the image resolution register.	0x8000_8000
SDW_CONFIG	0xFA60_0038	R/W	Specifies the shadow register of configuration.	0x0000_0000
SDW_RESOL	0xFA60_003C	R	Specifies the shadow register of resolution.	0x8000_8000
CSIS_PKTDATA	0xFA60_2000 ~ 0xFA60_3FFC	R	Specifies the memory area for storing non-image data. Odd frame: 0x2000 ~ 0x2FFC Even frame: 0x3000 ~ 0x3FFC	0xXXXX_XXXX

NOTE: S_RESETN at MIPI_PHY_CON0 (0xE010_E814) should be '1' before enabling CSIS.

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4.6.1.1 Control Register (CSIS_CONTROL, R/W, Address = 0xFA60_0000)

CSIS_CONTROL	Bit	Description	Initial State
S_DpDn_Swap_Clk	[31]	Swaps Dp channel and Dn channel of clock lanes. 0 = Default 1 = Swaps	0
S_DpDn_Swap_Dat	[30]	Swaps Dp channel and Dn channel of data lanes. 0 = Default 1 = Swaps	0
Reserved	[29:21]	Should be 0.	0
Parallel	[20]	Specifies data alignment size. Refer to *4.4 "Data Format"*. 0 = 24-bit data alignment 1 = 32-bit data alignment	1
Reserved	[19:17]	Should be 0.	0
Update_Shadow	[16]	Updates the shadow registers. 0 = Default 1 = Updates the shadow registers After configuration, set this bit for updating shadow registers. This bit is cleared automatically after updating shadow registers.	0
Reserved	[15:9]	Should be 0.	0
WCLK_Src	[8]	Specifies wrapper clock source. 0 = PCLK 1 = EXTCLK This bit determines the source of pixel clock, which transfers image data to CAMIF.	0
Reserved	[7:5]	Should be 0.	0
SwRst	[4]	Specifies software reset. 0 = No reset 1 = Reset All writable registers in CSIS return to their reset value. After this bit is active for three cycles, this bit is de-asserted automatically. Note: Almost all MIPI CSIS blocks use “ByteClk” from D-PHY. “ByteClk” is not a continuous clock. You must assert software reset if the camera module is turned off.	0
Reserved	[3:1]	Reserved	0
Enable	[0]	Specifies the CSIS system on/ off. 0 = Off 1 = On If this bit is low even though the CSIS clock is alive, then any request from CSIS is not serviced and kept waiting. Once the main host disables CSIS, it should be reset by software or hardware before the main host enables CSIS again.	0

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4.6.1.2 D-PHY Control Register (CSIS_DPHYCTRL, R/W, Address = 0xFA60_0004)

This register controls D-PHY.

CSIS_DPHYCTRL	Bit	Description	Initial State
Reserved	[31:4]	Should not change the value.	0
DPHYOn	[4:0]	Enables D-PHY clock and data lane. [4]: Data lane 3 [3]: Data lane 2 [2]: Data lane 1 [1]: Data lane 0 [0]: Clock lane 0 = Disables 1 = Enables	0

4.6.1.3 Configuration Register (CSIS_CONFIG, R/W, Address = 0xFA60_0008)

CSIS_CONFIG	Bit	Description	Initial State
Hsync_LIntv	[31:26]	Specifies the interval between Hsync falling and Hsync rising (Line interval). As shown in *Figure 4-2*, t2 specifies this interval. 6'h00 ~ 6'h3F cycle of Pixel clock.	0
Vsync_SIntv	[25:20]	Specifies the interval between Vsync rising and first Hsync rising. As shown in *Figure 4-2*, t1 specifies this interval. 6'h00 ~ 6'h3F cycle of Pixel clock	0
Vsync_EIntv	[19:8]	Specifies the interval between last Hsync falling and Vsync falling. As shown in *Figure 4-2*, t5 specifies this interval. 12'h000 ~ 12'hFFF cycle of Pixel clock	0
DataFormat[5:0]	[7:2]	Specifies the image data format. 0x1E = YUV422 (8-bit) 0x2A = RAW8 0x2B = RAW10 0x2C = RAW12 0x30 = user defined 1 0x31 = user defined 2 0x32 = user defined 3 0x33 = user defined 4 Others = Reserved	0
NumOfDatLane	[1:0]	Specifies the number of data lanes. 00 = 1 Data Lane 01 = 2 Data Lane 10 = 3 Data Lane 11 = 4 Data Lane	0

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4.6.1.4 DPHY State Register (CSIS_DPHYSTS, R, Address = 0xFA60_000C)

CSIS_DPHYSTS	Bit	Description	Initial State
Reserved	[31:12]	Reserved	0
UlpsDat	[11:8]	Determines whether the data lane [3:0] is in ULPS. [7]: Data lane 3 [6]: Data lane 2 [5]: Data lane 1 [4]: Data lane 0 0 = Not ULPS 1 = ULPS	0
StopStateDat	[7:4]	Determines whether the data lane [3:0] is in Stop state. [7]: Data lane 3 [6]: Data lane 2 [5]: Data lane 1 [4]: Data lane 0 0 = Not Stop state 1 = Stop state	F
Reserved	[3:2]	Reserved	0
UlpsClk	[1]	Determines whether the clock lane is in ULPS. 0 = Not ULPS 1 = ULPS	0
StopStateClk	[0]	Determines whether the clock lane is in Stop state. 0 = Not Stop state 1 = Stop state	1

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4.6.1.5 Interrupt Mask Register (CSIS_INTMSK, R/W, Address = 0xFA60_0010)

This register masks the interrupt sources.

CSIS_INTMSK	Bit	Description	Initial State
MSK_EvenBefore	[31]	Receives non-image data at even frame and before image. 0 = Disables Interrupt 1 = Enables Interrupt	0
MSK_EvenAfter	[30]	Receives non-image data at even frame and after image. 0 = Disables Interrupt 1 = Enables Interrupt	0
MSK_OddBefore	[29]	Receives non-image data at odd frame and before image. 0 = Disables Interrupt 1 = Enables Interrupt	0
MSK_OddAfter	[28]	Receives non-image data at odd frame and after image. 0 = Disables Interrupt 1 = Enables Interrupt	0
Reserved	[27:13]	Reserved	0
MSK_ERR _SOT_HS	[12]	Specifies start of transmission error. 0 = Disables Interrupt 1 = Enables Interrupt	0
Reserved	[11:6]	Reserved	0
MSK_ERR_LOST_FS	[5]	Lost of Frame Start packet 0 = Disables Interrupt 1 = Enables Interrupt	0
MSK_ERR_LOST_FE	[4]	Lost of Frame End packet 0 = Disables Interrupt 1 = Enables Interrupt	0
MSK_ERR_OVER	[3]	Controls error. 0 = Disables Interrupt 1 = Enables Interrupt	0
MSK_ERR_ECC	[2]	Specifies ECC error. 0 = Disables Interrupt 1 = Enables Interrupt	0
MSK_ERR_CRC	[1]	Specifies CRC error. 0 = Disables Interrupt 1 = Enables Interrupt	0
MSK_ERR_ID	[0]	Specifies unknown ID error. 0 = Disables Interrupt 1 = Enables Interrupt	0

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4.6.1.6 Interrupt Source Register (CSIS_INTSRC, R/W, Address = 0xFA60_0014)

This register identifies interrupt sources.

CSIS_INTSRC	Bit	Description	Initial State
EvenBefore	[31]	Receives non-image data at even frame and before image. Write 1 = Clears the status bit Write 0 = No effect	0
EvenAfter	[30]	Receives non-image data at even frame and after image. Write 1 = Clears the status bit Write 0 = No effect	0
OddBefore	[29]	Receives non-image data at odd frame and before image. Write 1 = Clears the status bit Write 0 = No effect	0
OddAfter	[28]	Receives non-image data at odd frame and after image. Write 1 = Clears status bit Write 0 = No effect	0
Reserved	[27:16]	Reserved	0
ERR_SOT_HS	[15:12]	Specifies start of transmission error.	0
Reserved	[11:6]	Reserved	0
ERR_LOST_FS	[5]	Indicates the lost of Frame Start packet	0
ERR_LOST_FE	[4]	Indicates the lost of Frame End packet	0
ERR_OVER	[3]	Specifies overflow caused in image FIFO. The outer bandwidth has to be faster than the input bandwidth. However, image FIFO can overflow due to user fault. There are two ways to prevent overflow: Tune output pixel clock faster than current: WCLK_Src in CSIS_CTRL register should be set to 1. Then assign a faster clock. Tune input byte clock slower than current: Set register in camera module through I2C channel. When this interrupt is generated, Turn the camera off. Assert software reset. If you do not assert software reset, MIPI CSIS will not receive any data. Tune the clock frequency and re-configure all the related registers. MIPI CSIS module is now ready for operation. Write 1 = Clears the status bit. Write 0 = Has no effect.	0
ERR_ECC	[2]	Specifies ECC error. Write 1 = Clears status bit Write 0 = No effect	0
ERR_CRC	[1]	Specifies CRC error. Write 1 = Clears status bit Write 0 = No effect	0

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CSIS_INTSRC	Bit	Description	Initial State
ERR_ID	[0]	Specifies unknown ID error. Write 1 = Clears status bit Write 0 = No effect	0

4.6.1.7 Resolution Register (CSIS_RESOL, R/W, Address = 0xFA60_002C)

CSIS_RESOL	Bit	Description	Initial State
HResol	[31:16]	Specifies horizontal image resolution. Input boundary of each image format is as follows: YUV422 (8-bit): 0x0001 ~ 0xFFFF RAW8: 0x0001 ~ 0xFFFF RAW10: 4n (where n is 1, 2, 3, …) RAW12: 2n (where n is 1, 2, 3, …)	0x8080
VResol	[15:0]	Specifies vertical image resolution. Input boundary: 0x0001 ~ 0xFFFF	0x8080

4.6.1.8 Shadow Configuration Register (CSIS_sdw_config, R, Address = 0xFA60_0038)

CSIS_SDW_CONFIG	Bit	Description	Initial State
Hsync_LIntv	[31:26]	Specifies current interval between Hsync falling and Hsync rising (Line interval).	0
Vsync_SIntv	[25:20]	Specifies current interval between Vsync rising and first Hsync rising.	0
Vsync_EIntv	[19:8]	Specifies current interval between last Hsync falling and Vsync falling.	0
DataFormat[5:0]	[7:2]	Specifies current image data format.	0
NumOfDatLane[1:0]	[1:0]	Specifies current number of data lanes. These bits are always the same as the number of data lanes in CSIS_CONFIG register because these bits are static signals that do not change in operation.	0

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4.6.1.9 Shadow Resolution Register (CSIS_SDW_resol, R, Address = 0xFA60_003C)

CSIS_PKTDATA	Bit	Description	Initial State
HResol	[31:16]	Specifies current horizontal image resolution.	0
VResol	[15:0]	Specifies current vertical image resolution.	0

4.6.1.10 Packet Data Register (CSIS_PKTDATA, R, Address = 0xFA60_2000 ~ 0xFA60_3FFC)

CSIS_PKTDATA	Bit	Description	Initial State
PktData	[31:0]	Specifies packet data.	Unknown

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5 G3D

5.1 OVERVIEW OF G3D

The G3D block is based on the SGX540 core from Imagination Technologies. SGX represents a new generation of programmable PowerVR graphics IP cores. The PowerVR SGX architecture is scalable and can target all market segments--from mainstream mobile devices to high-end desktop graphics. The PowerVR SGX540 core is designed for feature phones, PDA, and handheld gaming applications.

PowerVR SGX processes a number of differing multimedia data types concurrently, such as:

- Pixel Data
- Vertex Data
- General Purpose Processing

5.1.1 KEY FEATURES OF G3D

The key features of G3D include:

- Supports 3D and vector graphics on common hardware
- Uses Tile-based architecture
- Incorporates Universal Scalable Shader engine, which is a multi-threaded engine with Pixel and Vertex Shader functionality
- Supports industry standard APIs such as OGL-ES 1.1 and 2.0, OpenVG 1.0
- Supports multiple operating systems such as Symbian, Linux, WinCE, and future versions of these systems
- Enables fine-grained task switching, load balancing, and power management
- Supports advanced geometry DMA driven operation for minimum CPU interaction
- Supports programmable high-quality image anti-aliasing
- Enables fully virtualized memory addressing for smooth functioning of operating system in a unified memory architecture
- Supports standard master and slave AXI bus interfaces

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5.1.2 3D FEATURES IN G3D

The 3D features in G3D include:

- Supports deferred pixel shading
- Uses on-chip tile floating point depth buffer
- Supports 8-bit stencil with on-chip tile stencil buffer
- Provides eight parallel depth/ stencil tests per clock
- Supports scissor test
- Supports textures such as:
  - Cube Map
  - Projected
  - Non-square
- Supports texture formats such as:
  - RGBA: 8888, 4444, 565, 1555, and 1565
  - Monochromatic: 8, 16, 16f, 32f, and 32int
  - Dual channel: 8:8, 16:16, and 16f:16f
  - Compressed textures: PVR-TC1, PVR-TC2, and ETC1
  - All YUV formats (programmable)
- Supports the same resolution for both frame buffer maximum size and texture maximum size
  - Frame buffer maximum size = 2048 x 2048
  - Texture maximum size = 2048 x 2048
- Controls texture filtering
  - Bilinear, Trilinear, and Anisotropic
  - Independent minimum and mag control
- Supports anti-aliasing
  - 4x Multisampling
  - Programmable sample positions
- Supports indexed primitive list
  - Bus mastered
- Provides programmable vertex DMA
- Supports “render to texture” including twiddled formats
  - Generates auto MipMap generation
- Multiple on-chip render targets (MRT) is dependent on the availability of on-chip memory used as intermediate data stores (not included in the SGX540 core)

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5.1.3 USSE FEATURES IN G3D

USSE represents the engine at centre of PowerVR SGX540 architecture. It supports a broad range of instructions. The key features of USSE in G3D include:

- Supports single programming model
  - Enables multi-threading with 16 simultaneous execution threads and up to 64 simultaneous data instances
  - Provides zero-cost swapping in and swapping out of threads
  - Supports cached program execution model with maximum program size of 4096 instructions
  - Contains dedicated pixel processing and vertex processing instructions
  - Supports 2048 32-bit registers
- Supports SIMD execution unit related operations in
  - 32-bit IEEE float
  - 2-way 16-bit fixed point
  - 4-way 8-bit integer
  - 32-bit bitwise (logical only)
- Controls static and dynamic flow in
  - Subroutine calls
  - Loops
  - Conditional branches
  - Zero-cost instruction predication
- Supports procedural geometry
  - Allows generation of primitives
  - Enables effective geometry compression
  - Supports high order surface
- Enables external data access
  - Reads from main memory via cache
  - Writes to main memory
  - Supports data fence facility
- Reads dependent texture

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5.1.4 2D FEATURES IN G3D

A dedicated processing pipeline processes 2D graphics within the SGX540 core. The OpenVG API uses these advanced techniques. This API is fully supported.

The 2D features in G3D include:

- Supports x2 clock frequency, that is, twice the frequency of the SGX540 core (optional)
- Supports ROP 2, 3, and 4 (including AA text)
- Supports source, pattern (brush), destination, and mask surface
- Enables alpha blending (per-pixel and global)
- Supports color key
- Supports these input formats: 1-, 2-, 4- and 8-bit palletized; and 4- and 8-bit alpha
- Supports these input and output formats: RGB(A) -- 3:3:2, 4:4:4:4, 5:5:5, 5:5:5:1, 5:6:5, 8:8:8:8, and 8:8:8:0
- Strides up to 2048 pixels
- Provides throughput (Note: All performance figures are affected by memory bandwidth. The basic assumption is that 2D pipeline operates at x2 SGX540 core frequency).
  - All ROPs (including color fill) – Two per clock
  - Source Copy – Two per clock
  - Alpha Blends – 2 per clock
  - Rotated Blits – 2 per clock
- Supports other 2D features such as:
  - Clipping, scissoring, and masking
  - Paint generation and image interpolation
  - Geometry generation
  - Translucency
  - Gradients
  - Complex pixel filters
  - Perspective texturing
  - Transformations
  - Strokes
  - Multi segment lines, wide lines, and multi segment wide lines
  - Mitred line intersections
  - Multi vertex polygons
  - Arbitrary polygon fills using gradients, blends, and translucency
  - Smooth arbitrary rotation

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5.1.5 BLOCK DIAGRAM OF SGX540

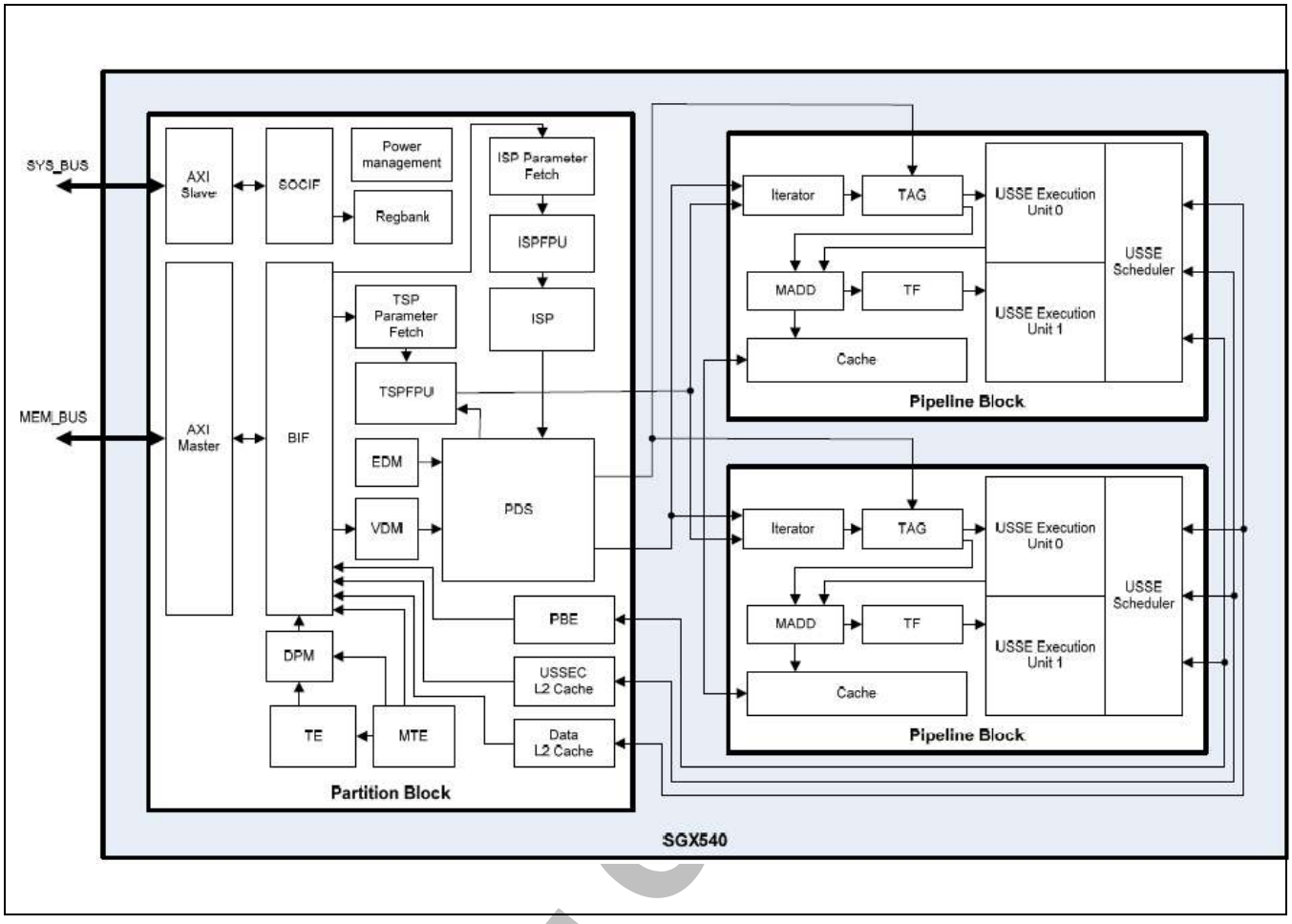

Figure 5-1 SGX540 Block Diagram

Figure 5-1 describes the terms used in the block diagram above.

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Table 5-1 Glossary of Terms

Term	Description	Term	Description
VS	Vertex Shader	USSE	Universal Scalable Shader Engine
PS	Pixel Shader	TF	Texture Filter
OGL	Open GL Application Programming Interface	MADD	Mux/ Arb/ Demux/ Decompress – Cache Management Module
DMS	Data Master Selector	MTE	Macro Tiling Engine
PP	Pixel Presenter	ROP	Collective Term For 2D Raster Operations
VDM	Vertex Data Master	MRT	Multiple Render Target
GPDM	General Purpose Data Master	TE	Tiling Engine
PDM	Pixel Data Master	DPM	Dynamic Parameter Management
ISP	Image Synthesis Processor – Hidden Surface Removal Engine	TSP FPU	Texturing and Shading Floating Point Setup Unit
PDS	Programmable Data Sequencer	TAG	Texture Address Generator

The SGX540 block is based on the PowerVR SGX core from Imagination Technologies.

5.1.5.1 Coarse Grain Scheduler

The Coarse Grain Scheduler (CGS) specifies the main system controller for the PowerVR SGX540 architecture. It consists of two stages, namely, the Data Master Selector (DMS) and the Programmable Data Sequencer (PDS). The DMS processes requests from data masters and determines which tasks will be executed based on the resource requirements. The PDS then controls the loading and processing of data on the USSE.

5.1.5.2 Data Master Selector

The DMS processes request from the data masters and selects a task to be executed by the USSE and PDS by tracking task resource requirements. The selected data master then has its resource allocated and source data from the individual data master, which is passed to the PDS sequencing engine.

There are three data masters in the SGX540 core, namely:

- Pixel Data Master (PDM)
- Vertex Data Master (VDM)
- General Purpose Data Master (GPDM)

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5.1.5.3 Pixel Data Master

The PDM initiates “rasterize processing” within the system. It consists of the ISP and Pixel Presenter (PP) modules. Each pixel pipeline processes pixels for a different half of a given tile, which allows for optimum efficiency within each pipe due to locality of data.

5.1.5.4 VDM Data Master

The VDM initiates “transform and lighting processing” within the system. The VDM module reads an input control stream, which contains triangle index data and state data. The state data indicates the PDS program, size of the vertices, and amount of USSE output buffer resource available to the VDM. The triangle data is parsed to determine unique indices that must be processed by the USSE. These are grouped together according to the configuration provided by the driver and presented to the DMS.

5.1.5.5 General Purpose Data Master

The GPDM responds to events within the system. Each event causes an interrupt to the host or synchronized execution of a program on the PDS. The program may or may not cause a subsequent task to be executed on the USSE.

5.1.5.6 PDS

The DMS and PDS controls whether vertices, pixels, or imaging data operations are processed by the USSE. It controls the order, location, and size of these operations. It also controls two operations: fetching essential data for the USSE and allocating resources.

5.1.5.7 USSE

USSE is a user programmable processing unit. Although general in nature, its instructions and features are optimized for three types of tasks, namely, processing vertices (vertex shading), processing pixels (pixel shading), and imaging processing.

5.1.5.8 Multi-Level Cache

The multi-level cache is a level cache consisting of two modules, namely, the Main Cache and the Mux, Arbiter, Demux, De-Compression Unit (MADD).

MADD is a wrapper around the main cache module that manages and formats requests to and from the cache. It also provides Level 0 caching for texture and USSE requests.

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5.1.5.9 Vertex Processing

There are three main processes within the PowerVR architecture that must be performed to generate 3D graphics.

- To create screen space representation, triangle information in the form of vertices must be transformed and be lit.
- To create display lists in memory, these transformed and lit vertices are passed through a tiling engine.
- To create the final image in the Pixel Processing pipeline, the display list in memory is rasterized on a tile-by-tile basis. The transform and light and tiling operation together can be regarded as the vertex-processing pipeline.

5.1.5.10 Transform and Lighting

A 3D object is expressed in terms of triangles, each of which is made up of three vertices with a minimum of X, Y, and Z coordinates. The basic steps to transform a typical 3D application are explained below, along with a brief description of lighting models. The transform and lighting (TNL) process within SGX540 is performed by data moving through VDM, PDS, and USSE respectively.

5.1.5.11 Macro Tiling Engine

The Macro Tiling Engine (MTE) takes in vertex and index data from the USSE and PDS, and generates a macro-tiled block of vertex index data. This data is written to memory after removing the redundant data. In addition to this, the MTE generates a set of primitive blocks for the tiling engine. A primitive block is a list of primitives, where each primitive consists of its indices and fixed point x,y of the vertices.

5.1.5.12 Tiling Engine

The Tiling Engine (TE) accepts blocks of primitive data from the MTE, and performs two incremental tiling algorithms, namely, the bounding box and perfect tiling algorithms. These algorithms produce a minimal list of tiles containing the primitives. Information about the primitives contained within the tiles is written as a control stream (display list) to memory, which is dynamically allocated by the Dynamic Parameter Management (DPM) block.

5.1.5.13 Dynamic Parameter Management

DPM ensures that SGX540 is able to render arbitrarily complex scenes. During tiling, the DPM allocates memory from a parameter memory pool, and after rasterization releases it. SGX540 breaks down the display list into groups of tiles (macro tiles), and each macro tile is rendered separately (“Partial Rendering”). As each macro tile is rendered, the results are merged with the render results from a previous macro tile to produce the correct final image.

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5.1.5.14 Pixel Processing

The Pixel Processing pipeline takes the result of vertex processing process from the memory and performs a number of processes to generate the final rasterized pixels. This can be divided into three main stages:

- Hidden Surface Removal (ISP)
- Texturing and Shading (TSP, Iterators, TAG, TF, and USSE)
- Pixel Formatting (Pixel Co-Processor)

5.1.5.15 Image Synthesis Processor

To determine the visible pixels for each triangle in a given tile before being textured and shaded, the Image Synthesis Processor (ISP) specifies the first stage of pixel-processing pipeline that performs hidden surface removal. This is a key feature of the PowerVR architecture that is referred to as deferred texturing and shading. It performs a pixel accurate occlusion detection operation ahead of the computationally intensive pixel shading operations.

5.1.5.16 TSP

The TSP parameter fetches requests, and parses position and TSP vertex data from internal 3D display list--for visible primitives produced by the hidden surface removal engine (ISP).

To set up triangle for the TSP, the TSP FPU uses vertex data sourced from the TSP parameter fetch. Multiple plane equations are produced that define how colors and texture coordinate sets are interpolated across primitives.

5.1.5.17 Texture Address Generator

The Texture Address Generator (TAG) receives a set of coordinates from iterators or the USSE, along with their corresponding state information. From this, it calculates a set of addresses to perform the required texture lookup. It also generates a set of coefficients to be used by the return Texture Filter (TF) module.

5.1.5.18 Texture Filter

The Texture Filter (TF) receives data from the cache, following requests submitted by the TAG module, and filters the resultant data as required. It computes bilinear, trilinear, and anisotropic filtering results. These results are then passed into the USSE for combining with the complex pixel shader calculated colors that are written to the Pixel Co-processor module.

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5.1.6 BLOCK DIAGRAM OF INTEGRATION INFORMATION

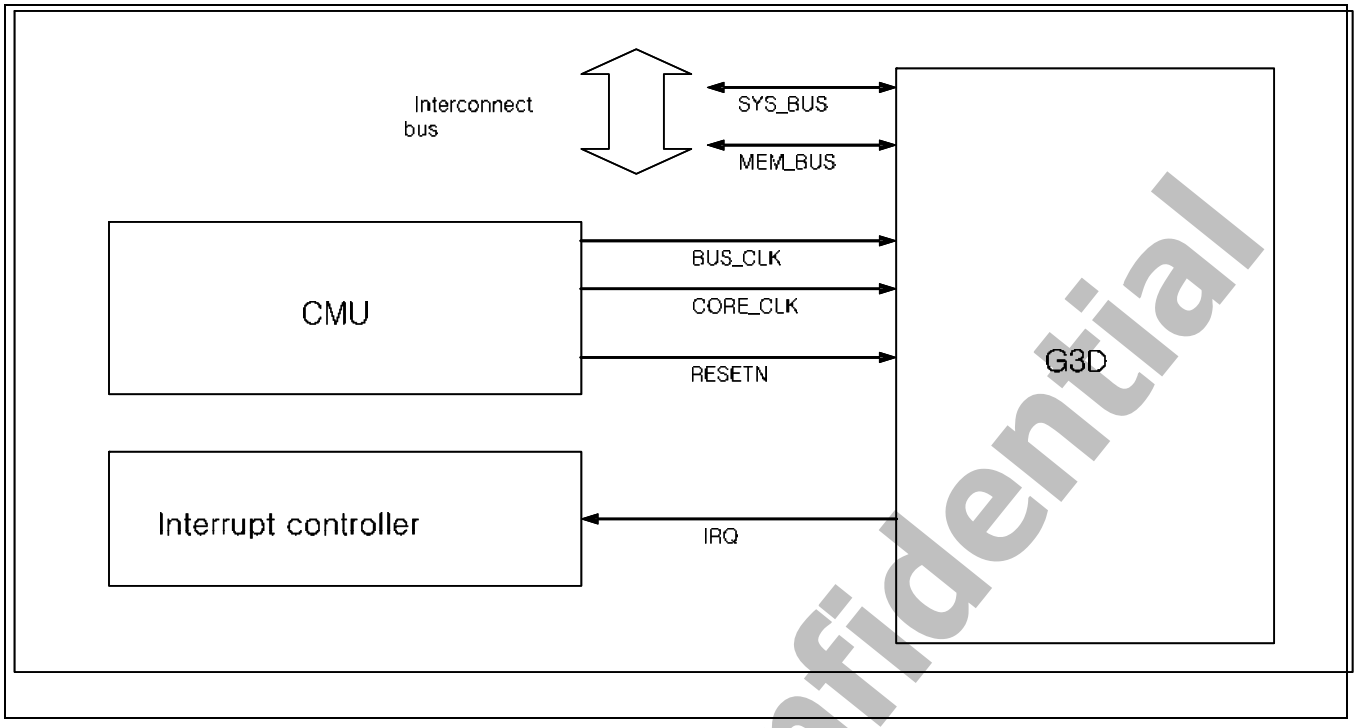

Figure 5-2 Block Diagram of Integration Information with Related Block

The Clock Management Unit (CMU) comprises of two blocks: BUS_CLK (for bus interface part) and CORE_CLK (for G3D internal function part). Both clocks are supported in 200Mhz clock domain, but you can set the two clocks with different clocks. BUS_CLK and CORE_CLK can be fully asynchronous.

G3D block has six controllable clock domains partitioned internally to functional areas of the design. It automatically controls clock gating if some blocks are not used at that time.

G3D block has its own power domain. If you do not use G3D block, then you can turn off the G3D block thoroughly by setting PMU. The detail power states are summarized in *Table 5-2*. You can see the detailed explanation of power mode in Chapter, “PMU”.

Table 5-2 Power Mode Summary About G3D

Power Mode	NORMAL	IDLE	DEEP-IDLE	STOP	DEEP-STOP	SLEEP
G3D	Power on/ Clock gating/ Power gating	KEEP power state in NORMAL mode(NOTE)	KEEP power state in NORMAL mode/ Power gating	Clock gating/ Power gating	Power gating	Power off

NOTE: KEEP power state in NORMAL mode means power-on G3D in NORMAL mode is still power-on, clock-gated G3D in NORMAL mode is still clock-gated, and power-gated G3D in NORMAL mode is still power-gated.

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5.1.7 REGISTER MAP

G3D contains the same control registers, as shown in *Table 5-3* Contact us for more information about registers, descriptions, operating systems support, and 3D libraries.

Refer to http://www.khronos.org about Open APIs like OGL-ES and OpenVG.

Table 5-3 G3D Register Summary

Module Name	Start Address	End Address	Size
G3D	0xF300_0000	0xF3FF_FFFF	16M bytes

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6 MULTI FORMAT CODEC

6.1 INTRODUCTION

The multi-format video codec is a synthesizable core which can perform encoding and decoding of multiple streams at 30fps up to 1080p resolution image (1920x1080).

The MFC can handle a real-time coding up to 16 multi-channels which supports H.264, MPEG4, MPEG2, VC-1 and H.263. Detailed features are described in later sections. Note that MFC can support up to 16 channels, but the actual number of channels is dependent on use cases and limited by many system specific factors, such as the system memory, the clock speed provided to MFC, and so on.

6.1.1 SUPPORTED STANDARDS

- ITU-T H.264, ISO/IEC 14496-10
  - Decoding : High Profile Level 4.0 1920x1080 @ 30fps 20Mbps
    - Baseline Profile Level 4.0
      - Except FMO (Flexible Macroblock Ordering), ASO (Arbitrary Slice Ordering) and RS (Redundant Slice)
    - Main Profile Level 4.0
    - High Profile Level 4.0
  - Encoding : High Profile Level 4.0 1920x1080 @ 30fps 20Mbps
    - Baseline / Main / High Profile
    - - Except FMO (Flexible Macroblock Ordering), ASO (Arbitrary Slice Ordering) and RS (Redundant Slice)
    - Support 8x8 transform in high profile
    - Support cyclic intra macroblock refresh
- ITU-T H.263 Profile 3
  - Decoding : Profile 3 Level 70 D1 @30fps 8Mbps
    - Profile 3, restricted up to SD resolution 30fps
    - Support H.263 Annexes
      - Annex I: Advanced Intra Coding
      - Annex J: De-blocking (in-loop) filter
      - Annex K: Slice Structured Mode without RS & ASO
      - Annex T: Modified Quantization
      - Annex D: Unrestricted Motion Vector Mode
      - Annex F: Advanced Prediction Mode except overlapped motion compensation for luminance
  - Encoding : Base Profile @ 30fps 8Mbps
    - Baseline Profile
    - Support custom size up to 1920x1088

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- ISO/IEC 14496-2 MPEG4
  - Decoding : Advanced Simple Profile Level 5 D1 @ 30fps 8Mbps
    - MPEG4 Simple Profile
    - MPEG4 Advanced Simple Profile Level 5
    - Xvid
    - De-blocking filter for post-processing
      - Error resilience tools: re-sync marker, data-partitioning with reversible VLC
    - Data-partitioning supports up to SD resolution
    - Support quarter pixel motion compensation
    - GMC (Global Motion Compensation) is restricted to 1 warp point
      - 2 and 3-warping point supported with quality degradation, i.e. continuing decoding with corrupted image
    - Support only one rectangular visual object
    - Only forward reversible VLC (RVLC) is supported
    - Support error resilience tool
    - Support post-processing by re-using H.263 in-loop filter.
  - Encoding : Advanced Simple Profile Level 5 D1 @ 30fps 8Mbps
    - Support MPEG4 Simple / Advanced Simple Profile
      - Except data partitioning, RVLC
    - Support only one rectangular visual object
    - Support only DC prediction
- ISO/IEC 13818-2 MPEG2
  - Decoding : Main Profile High Level 1920x1080 @ 30fps 40Mbps
    - Support Main Profile High Level
    - Support MPEG1 except D-picture
- SMPTE 421M VC-1
  - Decoding : Advanced Profile Level 3 1920x1080 @ 30fps 45Mbps
    - Support Simple Profile Medium Level
    - Support Main Profile High Level
    - Support Advanced Profile Level 3
    - Multi-resolution is not processed inside video decoder
    - Provide Range Mapping information for post-processing

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6.1.2 FEATURES

- Image features
  - Max size: 1920x1088 @ progressive mode
    1920x544 @ interlaced mode
  - Min size : 32x32 @ progressive mode
    32x16 @ interlaced mode
  - Input image size for encoding
    - Arbitrary input image size for encoding (no constraints such as multiple of 8 or 16)
  - Chrominance interleaved in external memory
  - 4:2:0 for encoding
  - 4:2:0 for decoding
  - Support monochrome for H.264 decoding
  - 8 bits per sample
  - Non paired field mode is not supported
- Slice
  - Minimum size: 16x16
- Picture coding structure at encoding
  - Progressive mode
  - Field mode (only H.264)
- Inter prediction at encoding
  - Number of reference frames : Max 2 (P frame: 1 or 2, B frame: 2)
  - Search range: Horizontal +/- 64, Vertical +/- 32
  - Motion estimation resolution: 1/4 pel for H264, 1/2 pel for MPEG4
  - Number of B frames: 1 or 2
  - Supported modes
    - H264: 16x16, 16x8, 8x16, 8x8, spatial direct mode
    - MPEG4: 4MV & UMV
- Intra macroblock for encoding
  - Support cyclic intra macroblock refresh
  - Intra prediction: Support 4x4 (9 modes), 16x16 (4 modes), 8x8 (9 modes) at H.264
- Rate control at encoding
  - CBR (Constant Bit-Rate) and VBR (Variable Bit-Rate)
  - Frame level (H.264/MPEG4/H.263) and macroblock level (H.264) rate control can be enabled or disabled selectively
- Stream
  - Time-multiplexed multi-stream encoding/decoding up to 16 channels
  - Start code must be included at every position of frame or slice in the stream at decoding

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6.1.3 TARGET PERFORMANCE AND FUNCTIONS

6.1.3.1 Video Decoding Capability

- Decoding up to 1080p@30fps at 200MHz core clock frequency and 200MHz bus clock frequency
- The maximum resolution can be limited by the video standards, even though MFC has a capability to handle up to 1080p.

6.1.3.2 Video Encoding Capability

- Encoding up to 1080p@30fps at 200MHz core clock frequency and 200MHz bus clock frequency
- The performance numbers are verified under the condition that the number of reference frames for a P frame is 1.
- The maximum resolution can be limited by the video standards, even though MFC has a capability to handle up to 1080p.

6.1.3.3 Error Detection

- H264
  - Header error detection
    - Checking if firmware parsing is out of range
  - H/W
    - VLD error detection: When there is no stream to decode before stream decoder is complete.
    - Macroblock error detection: When MB type is out of range (i.e., 0~25 @ I slice / 0~30 @ P slice / 0~48 @ B slice)
    - Sub MB type error detection: When sub_MB_type or intra prediction mode is out of range (i.e., Intra prediction mode 0~7, sub_mb_type 0~2 @ P slice / 0~11 @ B slice)
    - IDF error detection: When ref_idx value is greater than num_ref_idx_lx_active_minus1 (PPS)
    - Delta Q error detection: When mb_qp_delta is out of range (i.e., -26~25)
    - Timeout interrupt: When decoding time is greater than the firmware setting
- MPEG2/ MPEG4/ H.263/ VC-1
  - Header error detection: When the result of firmware parsing is out of range
  - H/W
    - VLD error: When VLD Result is out of table.
    - Coeff error: When AC/DC coefficient of 1 block is more than 64
    - Time out interrupt: When decoding time is greater than firmware setting

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6.2 HARDWARE OVERVIEW

6.2.1 BLOCK DIAGRAM

Top level of the MFC in *Figure 6-1* contains the hardware modules, including an OpenRISC with 8KB I-cache and 4KB D-cache. The optimum partition of the codec functions into software and hardware has ensured that the small sized hardware supports multiple standards. The hardware operates encoding and decoding at the slice level. On the other hand, the firmware on RISC performs other processing, such as slice header parsing and/or generation. Settings by the host processor can be changed at the frame boundary through the host interface.

Figure 6-1 presents a block diagram of MFC which is composed of RISC, MFC core, RG, bus interface, host interface, and stream interface. MFC core includes many codec accelerators. RG stands for register group which can be accessed by RISC and HOST. Host and RISC can communicate through registers in RG and risc2host interrupt generated by register in RG. If RISC gets some interrupt or information from HW, RISC set the registers to let host know the status of MFC. Host clears the interrupt signal by resetting the MFC_RISC_HOST_INT register.

There are two AXI master interfaces in which both Port_A and Port_B are used for full performance. As per the AXI standard, MFC masters take care of read/write hazard issues. Before read access of written data by MFC, internal masters in MFC always check the response of write access.

The search SRAM in the diagram contains reference image for motion estimation and motion compensation.

The shared SRAM is for sharing current image for encoding.

To reduce bandwidth for reference image loading, there is a pixel cache in the MFC core. The size is 2KB for luma and 1KB for chroma. In encoding case, only chroma reference will be loaded by pixel cache, because luma reference is already loaded in search SRAM for motion estimation. To use the pixel cache in decoding, reconstruction image have to be placed in Port_A memory area.

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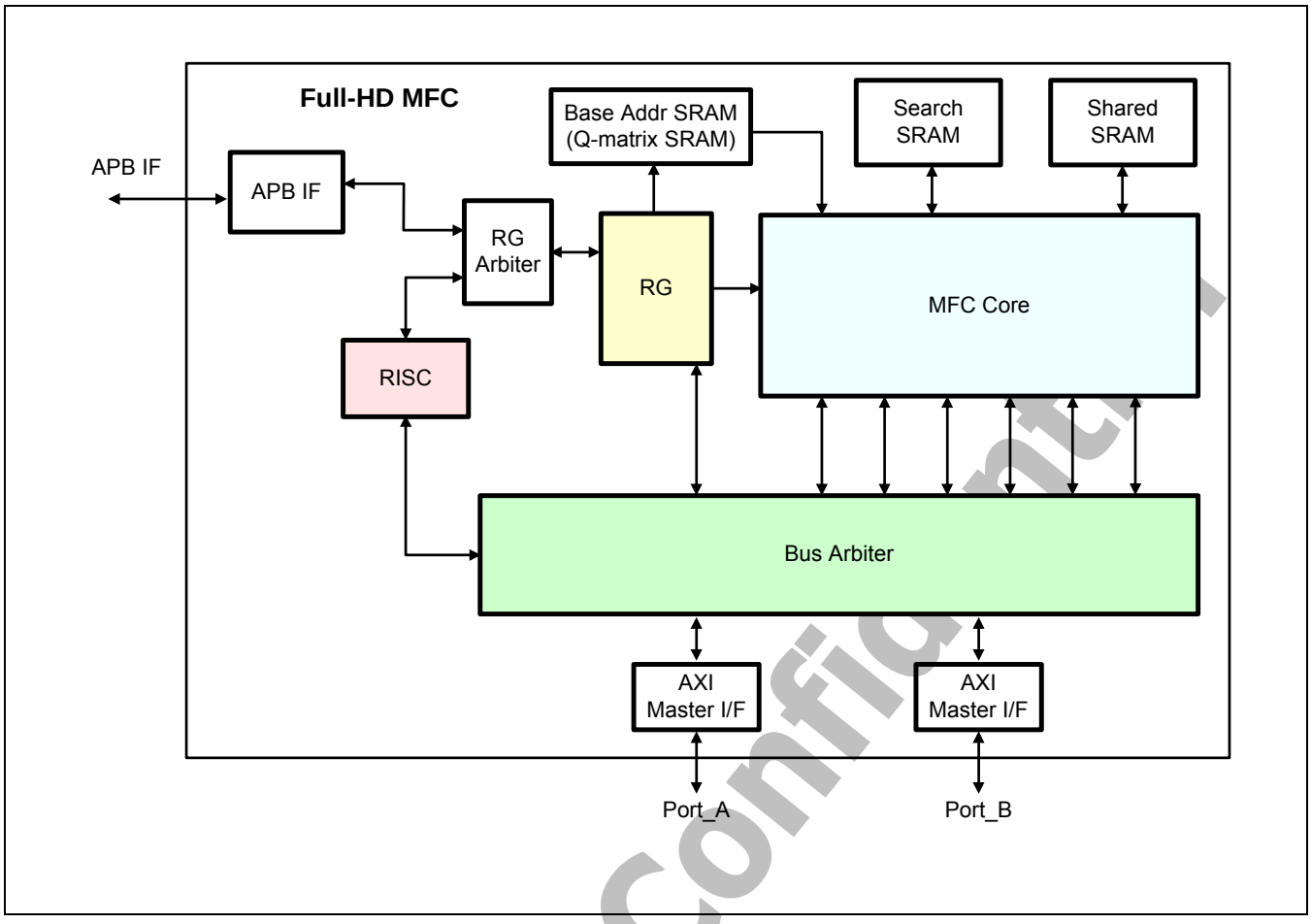

Figure 6-1 MFC Block Diagram

There are several internal masters in MFC core. Their interfaces are controlled by the bus arbiter. Internal masters have an index[6:0] register controlled by firmware. This register may be used to generate address, which will be an output of AXI interface.

After getting an index, the bus arbiter makes a decision which port to be used based on Index[6] (Index[6] = 0 for Port_A and 1 for Port_B). With Index[5:0], the bus arbiter get a base address from Q-matrix SRAM. The real address is calculated with the base address and DRAM_BASE_ADDR in AXI_MASTER. Therefore host must set a base address before starting codec.

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6.2.2 FRAME MEMORY

A frame memory area is specified by base address, horizontal and vertical image size. A complete image consists of Y, Cb and Cr components. The Cb and Cr pixels are stored in a byte interleaved way. Therefore, an image needs 2 frame buffers, one for Y and another for Cb and Cr components, as shown in *Figure 6-2*. The sum of image horizontal size and image horizontal offset should be multiple of 16: Horizontal offset makes the value of horizontal size to be multiple of 16. The vertical image size for Cb/Cr frame buffer should be half of the Y frame buffer.

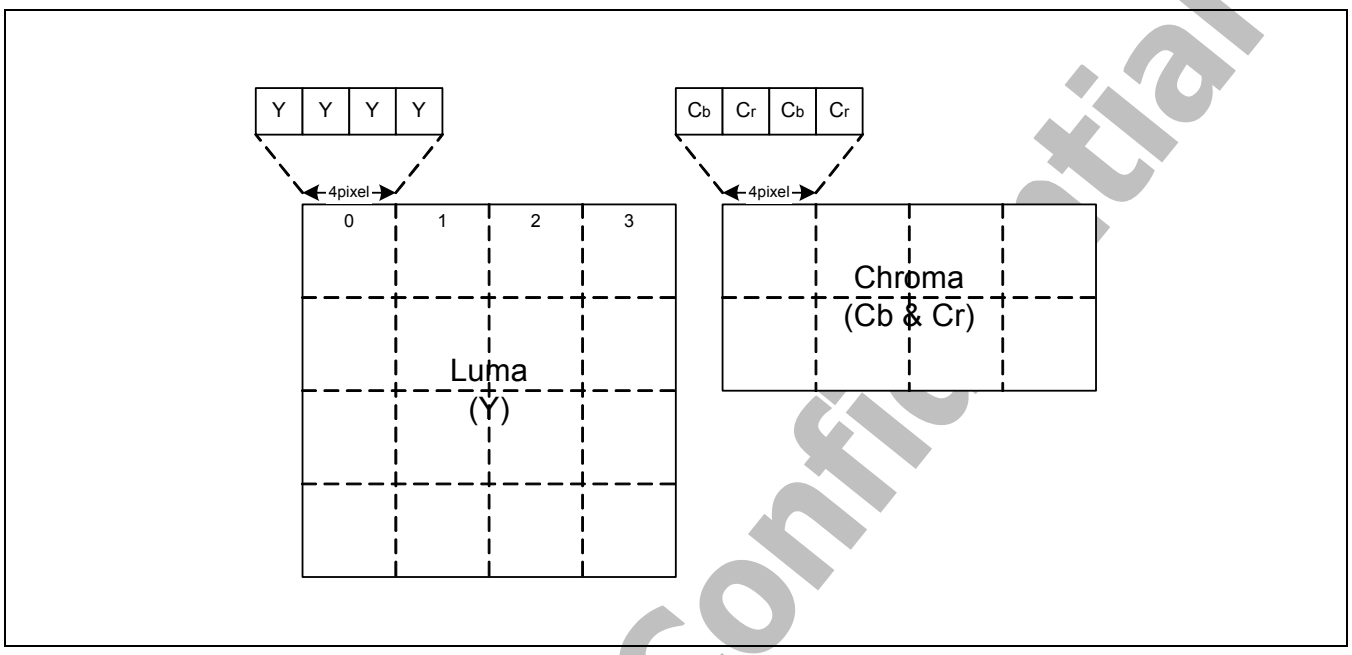

Figure 6-2 Luma and Chroma Pixel (8 bytes-aligned)

Reference picture is always made in the tile mode memory structure. Decoding reconstruction image is made in 64 pixels x 32 lines tiled mode. Encoding reconstruction image is made in 16 pixels x 16 lines tiled mode.

Current picture for encoding can be stored in two ways, linear memory structure or tile mode memory structure, depending on ENC_MAP_FOR_CUR register (0xF170_C51C). Host sets external memory parameters with the memory structure configuration. The physical memory address of each pixel data is determined by the memory structure, base address, and coordinates of pixel in the frame.

Figure 6-3 and *Figure 6-4* shows the tile mode memory structure of a QCIF image for 16x16 and 64x32 configuration.

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x_addr	0	4	8	12	16	20	24	28	32	36	40	44	48	52	56
y_addr	Logical mapping table (MB order)														
0	0	1	2	3	4	5	6	7	8	9	10				
16	11	12	13	14	15	16	17	18	19	20	21				
32	22	23	24	25	26	27	28	29	30	31	32				
48	33	34	35	36	37	38	39	40	41	42	43				
64	44	45	46	47	48	49	50	51	52	53	54				
80	55	56	57	58	59	60	61	62	63	64	65				
96	66	67	68	69	70	71	72	73	74	75	76				
112	77	78	79	80	81	82	83	84	85	86	87				
128	88	89	90	91	92	93	94	95	96	97	98				

Bank0	Bank1	Bank2	Bank3

```
** x_add:  word unit. Y_add: line unit

pixel_x = horizontal_image_size (ex: 1280)
pixel_y = vertical_image_size (ex: 720)
pixel_x_minus = pixel_x - 1;
pixel_y_minus = pixel_y - 1;
roundup_x = ((pixel_x - 1)/16)/8 + 1;
roundup_y = ((pixel_y - 1)/16)/4 + 1;

if (((pixel_y -32) <= y_addr) && (y_addr < pixel_y) &&
   (pixel_y_minus[5] == 0) && (y_addr[5] == 0)) {
 row_add = y_addr[13:6] * roundup_x + x_addr[20:6]
 bank_add = y_addr[4] ? {~x_addr[3], x_addr[2]} : {x_addr[3], x_addr[2]}
 col_add = {x_addr[5], x_addr[4:3], y_addr[3:0], x_addr[1:0]}
}
else {
 row_add = y_addr[13:6] * roundup_x + x_addr[20:5]
 bank_add = y_addr[4] ? {~x_addr[3], x_addr[2]} : {x_addr[3], x_addr[2]}
 col_add = {y_addr[5], x_addr[4:3], y_addr[3:0], x_addr[1:0]}
}

if (pixel_y_minus[5] == 0)
 pic_range = pixel_y_minus[14:6] * roundup_x + pixel_x_minus[14:8] + 1
else
 pic_range = roundup_x * roundup_y
```

Figure 6-3 QCIF Image in 16pixel x 16lines (1x1) Tiled Mode

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x_addr	0	4	8	12	16	20	24	28	32	36	40	44	48
y_addr	Logical mapping table (MB order)												
0	0	1	2	3	4	5	6	7	8	9	10		
16	11	12	13	14	15	16	17	18	19	20	21		
32	22	23	24	25	26	27	28	29	30	31	32		
48	33	34	35	36	37	38	39	40	41	42	43		
64	44	45	46	47	48	49	50	51	52	53	54		
80	55	56	57	58	59	60	61	62	63	64	65		
96	66	67	68	69	70	71	72	73	74	75	76		
112	77	78	79	80	81	82	83	84	85	86	87		
128	88	89	90	91	92	93	94	95	96	97	98		
144													

Bank0	Bank1	Bank2	Bank3

```
** x_add:  word unit. Y_add: line unit

pixel_x = horizontal_image_size (ex: 1280)
pixel_y = vertical_image_size (ex: 720)
pixel_x_minus = pixel_x - 1;
pixel_y_minus = pixel_y - 1;
roundup_x = ((pixel_x - 1)/16)/8 + 1;
roundup_y = ((pixel_y - 1)/16)/4 + 1;

if (((pixel_y -32) <= y_addr) && (y_addr < pixel_y) &&
   (pixel_y_minus[5] == 0) && (y_addr[5] == 0)) {
 row_add = y_addr[11:6] * roundup_x + x_addr[20:6]
 bank_add = {x_addr[5], x_addr[4]}
 col_add = {y_addr[4:0], x_addr[3:0]}
}
else {
 row_add = y_addr[13:6] * roundup_x + x_addr[20:5]
 bank_add = x_addr[5] ? {~y_addr[5], x_addr[4]} : {y_addr[5], x_addr[4]}
 col_add = {y_addr[4:0], x_addr[3:0]}
}

if (pixel_y_minus[5] == 0)
 pic_range = pixel_y_minus[14:6] * roundup_x + pixel_x_minus[14:8] + 1
else
 pic_range = roundup_x * roundup_y
```

Figure 6-4 QCIF Image in 64pixel x 32lines (4x2) Tiled Mode

6.3 REGISTER DESCRIPTION

6.3.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
Control Registers				
MFC_SW_RESET	0xF170_0000	R/W	Soft reset for each module in MFC. Each bit has following interpretation. 0 = Reset 1 = Release	0x000003fe
MFC_RISC_HOST_INT	0xF170_0008	R/W	MFC to host interrupt register. An interrupt is raised when MFC enables the INTERRUPT bit. Host CPU needs to check this register, properly process an ISR (Interrupt Service Routine), and clear the INTERRUPT bit.	0x00000000
MFC_HOST2RISC_ COMMAND	0xF170_0030	R/W	Host to MFC command register. Host can send command to MFC to open instance or close instance.	0x00000000
MFC_HOST2RISC_ARG1	0xF170_0034	R/W	The first argument of the host command	0x00000000
MFC_HOST2RISC_ARG2	0xF170_0038	R/W	The second argument of the host command	0x00000000
MFC_HOST2RISC_ARG3	0xF170_003C	R/W	Context memory address	0x00000000
MFC_HOST2RISC_ARG4	0xF170_0040	R/W	Context memory size	0x00000000
MFC_RISC2HOST_ COMMAND	0xF170_0044	R/W	MFC to host command register. MFC can respond to host using the MFC_RISC2HOST_COMMAND register	0x00000000
MFC_RISC2HOST_ARG1	0xF170_0048	R/W	MFC to host argument register. This register is used with the MFC_RISC2HOST_COMMAND register	0x00000000
MFC_RISC2HOST_ARG2	0xF170_004C	R/W	The second argument of the host command	0x00000000
MFC_RISC2HOST_ARG3	0xF170_0050	R/W	The Third argument of the host command	0x00000000
MFC_RISC2HOST_ARG4	0xF170_0054	R/W	The fourth argument of the host command	0x00000000
MFC_FIRMWARE_ VERSION	0xF170_0058	R	Firmware version information register	0x00000000
DBG_INFO_OUTPUT1	0xF170_0064	R	Debug information output register 1	0x00000000
DBG_INFO_OUTPUT1	0xF170_0068	R	Debug information output register 2	0x00000000
MFC_FIRMWARE_STAT US	0xF170_0080	R	Firmware status register	0x00000000
MFC_MC_DRAMBASE_ ADDR_A	0xF170_0508	R/W	DRAM base address which indicates the base address for the memory map of the port A	0xD3000000
MFC_MC_DRAMBASE_ ADDR_B	0xF170_050C	R/W	DRAM base address which indicates the base address for the memory map of the port B	0x23000000

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Register	Address	R/W	Description	Reset Value
MFC_MC_STATUS	0xF170_0510	R	Bus arbiter's status. This register can be used to check whether the bus is busy or not before resetting MFC.	0x0000000X
MFC_COMMON_BASE_ADDR_0~63 [16:0]	0xF170_0600~ 0xF170_06FC	R/W	Codec common memory region for start address.	X
MFC_COMMON_BASE_ADDR_64~127 [16:0]	0xF170_0700~ 0xF170_07FC	R/W	Codec common memory region for start address.	X
Codec Registers				
MFC_HSIZE_PX	0xF170_0818	R/W	Picture width at encoder	0x00000000
MFC_VSIZE_PX	0xF170_081C	R/W	Picture height at encoder In the interlaced-field coding mode, it specifies the coded height of a field. In the progressive or interlaced-frame coding mode, it is the coded height of a frame at encoder.	0x00000000
MFC_PROFILE	0xF170_0830	R/W	Profile and level control register at encoder	0x00000000
MFC_PICTURE_STRUCT	0xF170_083C	R/W	Field picture/frame picture flag register at encoder	0x00000000
MFC_LF_CONTROL	0xF170_0848	R/W	Loop filter control	0x00000000
MFC_LF_ALPHA_OFF	0xF170_084C	R/W	Loop filter alpha offset	0x00000000
MFC_LF_BETA_OFF	0xF170_0850	R/W	Loop filter beta offset	0x00000000
MFC_QP_OFFSET	0xF170_0C30	R/W	QP information offset from the DPB start address	0x00000000
MFC_QP_OUT_EN	0xF170_0C34	R/W	QP information enable at decoder	0x00000000
MFC_SI_RTN_CHID	0xF170_2000	R/W	Return channel instance ID register	0x00000000
MFC_COMMON_SI_RG_1 ~ 15	0xF170_2004~ 0xF170_203C	R/W	Return the status of MFC after processing	0x00000000
MFC_SI_CH0_INST_ID	0xF170_2040	R/W	CH0 instance ID and control register	0x00000000
MFC_SI_CH1_INST_ID	0xF170_2080	R/W	CH1 instance ID and control register	0x00000000
MFC_COMMON_CH0_RG_1 ~ 15	0xF170_2044~ 0xF170_207C	R/W	Host and MFC interface registers through CH0	0x00000000
MFC_COMMON_CH1_RG_1 ~ 15	0xF170_2084~ 0xF170_20BC	R/W	Host and MFC interface registers through CH1	0x00000000
MFC_COMMON_SI_RG_1	0xF170_2004	R	Vertical resolution register	0x00000000
MFC_COMMON_SI_RG_2	0xF170_2008	R	Horizontal resolution register	0x00000000
MFC_COMMON_SI_RG_3	0xF170_200C	R	Required buffer number register	0x00000000
MFC_COMMON_SI_RG_4	0xF170_2010	R	Luminance address register for display	0x00000000

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Register	Address	R/W	Description	Reset Value
MFC_COMMON_SI_RG_5	0xF170_2014	R	Chrominance address register for display	0x00000000
MFC_COMMON_SI_RG_6	0xF170_2018	R	Decoded frame size for a frame	0x00000000
MFC_COMMON_SI_RG_7	0xF170_201C	R	Display status register	0x00000000
MFC_COMMON_SI_RG_8	0xF170_2020	R	Frame type register	0x00000000
MFC_COMMON_SI_RG_9	0xF170_2024	R	Luminance address register in decoding order	0x00000000
MFC_COMMON_SI_RG_10	0xF170_2028	R	Chrominance address setting register in decoding order	0x00000000
MFC_COMMON_SI_RG_11	0xF170_202C	R	Decoding status register	0x00000000
MFC_COMMON_CHx_RG_1	0xF170_2044 or 0xF170_2084	R/W	Start address of the CPB (coded picture buffer) in the external stream buffer.	0x00000000
MFC_COMMON_CHx_RG_2	0xF170_2048 or 0xF170_2088	R/W	Decoding unit size register	0x00000000
MFC_COMMON_CHx_RG_3	0xF170_204C or 0xF170_208C	R/W	Channel descriptor buffer address	0x00000000
Reserved	0xF170_2050 or 0xF170_2090		Reserved	0x00000000
Reserved	0xF170_2054 or 0xF170_2094		Reserved	0x00000000
MFC_COMMON_CHx_RG_6	0xF170_2058 or 0xF170_ 2098	R/W	CPB size register	0x00000000
MFC_COMMON_CHx_RG_7	0xF170_205C or 0xF170_209C	R/W	Descriptor buffer size register	0x00000000
MFC_COMMON_CHx_RG_8	0xF170_2060 or 0xF170_20A0	R/W	Release buffer register to specify the individual DPB availability	0x00000000
MFC_COMMON_CHx_RG_9	0xF170_2064 or 0xF170_20A4	R/W	Shared memory address	0x00000000
MFC_COMMON_CHx_RG_10	0xF170_2068 or 0xF170_20A8	R/W	DPB configuration that host prepared for decoding	0x00000000

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Register	Address	R/W	Description	Reset Value
MFC_COMMON_CHx_RG_11	0xF170_206C or 0xF170_20AC	R/W	Command sequence number from the host	0x00000000
MFC_COMMON_SI_RG_1	0xF170_2004	R	Encoded stream size register	0x00000000
MFC_COMMON_SI_RG_2	0xF170_2008	R	Encoded picture count register	0x00000000
MFC_COMMON_SI_RG_3	0xF170_200C	R	Stream buffer write pointer	0x00000000
MFC_COMMON_SI_RG_4	0xF170_2010	R/W	Slice type of the current frame to be encoded	0x00000000
MFC_COMMON_SI_RG_5	0xF170_2014	R/W	Encoded luma address	0x00000000
MFC_COMMON_SI_RG_6	0xF170_2018	R/W	Encoded chroma address	0x00000000
MFC_COMMON_CHx_RG_1	0xF170_2044 or 0xF170_2084	R/W	Stream buffer start address at encoder.	0x00000000
MFC_COMMON_CHx_RG_3	0xF170_204C or 0xF170_208C	R/W	Stream buffer size register	0x00000000
MFC_COMMON_CHx_RG_4	0xF170_2050 or 0xF170_2090	R/W	Current luma address	0x00000000
MFC_COMMON_CHx_RG_5	0xF170_2054 or 0xF170_2094	R/W	Current chroma address	0x00000000
MFC_COMMON_CHx_RG_6	0xF170_2058 or 0xF170_2098	R/W	Frame insertion control register	0x00000000
MFC_COMMON_CHx_RG_9	0xF170_2064 or 0xF170_20A4	R/W	Shared memory address	0x00000000
MFC_COMMON_CHx_RG_10	0xF170_2068 or 0xF170_20A8	R/W	Flushing input buffer	0x00000000
MFC_COMMON_CHx_RG_11	0xF170_206C or 0xF170_20AC	R/W	Command sequence number from the host	0x00000000
Encoding Resters				
ENC_PIC_TYPE_CTRL	0xF170_C504	R/W	Picture type control register	0x00000000
ENC_B_RECON_WRITE_ON	0xF170_C508	R/W	B-frame reconstructed data write control register	0x00000000
ENC_MSLICE_CTRL	0xF170_C50C	R/W	Multi-slice control register	0x00000000

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Register	Address	R/W	Description	Reset Value
ENC_MSLICE_MB	0xF170_C510	R/W	Slice size register when multi slice is enabled. Fixed number of macroblocks is used to determine the size of one slice.	0x00000000
ENC_MSLICE_Bit	0xF170_C514	R/W	Slice size register when multi slice is enabled. Bit count is used to determine the size of one slice.	0x00000000
ENC_CIR_CTRL	0xF170_C518	R/W	Intra refresh macroblock setting register	0x00000000
ENC_MAP_FOR_CUR	0xF170_C51C	R/W	Memory structure setting register of the current frame.	0x00000000
ENC_PADDING_CTRL	0xF170_C520	R/W	Padding control register	0x00000000
ENC_COMMON_INTRA_BIAS	0xF170_C588	R/W	Intra mode bias register for the macroblock mode decision	0x00000000
ENC_COMMON_BI_DIRECT_BIAS	0xF170_C58C	R/W	Bi-directional mode bias register for the macroblock mode decision	0x00000000
RC_CONFIG	0xF170_C5A0	R/W	Configuration of the rate control	0x00000000
RC_FRAME_RATE	0xF170_D0D0	R/W	Frame rate for the frame level RC	0x00000000
RC_BIT_RATE	0xF170_C5A8	R/W	Target bit rate for the frame level RC	0x00000000
RC_QBOUND	0xF170_C5AC	R/W	Maximum and minimum value of the quantization parameter	0x00000000
RC_RPARA	0xF170_C5B0	R/W	Rate control reaction coefficient	0x00000000
RC_MB_CTRL	0xF170_C5B4	R/W	Control the macroblock adaptive scaling features	0x00000000
H264_ENC_ENTRP_MODE	0xF170_D004	R/W	Entropy coding mode.	0x00000000
H264_ENC_NUM_OF_REF	0xF170_D010	R/W	The maximum number of reference pictures.	0x00000000
H264_ENC_TRANS_8X8_FLAG	0xF170_D034	R/W	8x8 transform enable flag in PPS at high profile.	0x00000000
MPEG4_ENC_QUART_PXL	0xF170_E008	R/W	Quarter pel interpolation control register	0x00000000
Shared Memory Structure				
EXTENDED_DECODE_STATUS	0x0000	R	Extended decode status	Undef
SET_FRAME_TAG	0x0004	W	Setting frame tag of an output frame	Undef
GET_FRAME_TAG_TOP	0x0008	R	Getting the first frame tag of an output frame	Undef
GET_FRAME_TAG_BOTTOM	0x000C	R	Getting the second frame tag of an output frame	Undef
PIC_TIME_TOP	0x0010	R	Presentation time of an output frame or top field	Undef
PIC_TIME_BOTTOM	0x0014	R	Presentation time of the bottom field	Undef

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Register	Address	R/W	Description	Reset Value
START_BYTE_NUM	0x0018	R/W	An offset of the start position in the stream when the start position is not aligned	Undef
CROP_INFO1	0x0020	R	Frame cropping information. Valid for H.264 only.	Undef
CROP_INFO2	0x0024	R	Frame cropping information. Valid for H.264 only.	Undef
EXT_ENC_CONTROL	0x0028	W	Encoder control	Undef
ENC_PARAM_CHANGE	0x002C	W	Encoding parameter change that signals the change of bitrate, frame rate, or the GOP size	Undef
VOP_TIMING	0x0030	W	VOP timing	Undef
HEC_PERIOD	0x0034	W	The number of consecutive video packet between header extension codes	Undef
METADATA_ENABLE	0x0038	W	Enable storing the metadata information to the shared memory	Undef
METADATA_STATUS	0x003C	R	Getting the presence of the metadata	Undef
METADATA_DISPLAY_INDEX	0x0040	R	DPB number when concealed macroblock or QP is enabled	Undef
EXT_METADATA_START_ADDR	0x0044	W	The start address of the metadata memory	Undef
PUT_EXTRADATA	0x0048	W	Signaling the existence of extra metadata.	Undef
EXTRADATA_ADDR	0x004C	W	The address of extra metadata.	Undef
ALLOCATED_LUMA_DPB_SIZE	0x0064	W	Size of luma DPB that host allocated for decoding	Undef
ALLOCATED_CHROMA_DPB_SIZE	0x0068	W	Size of chroma DPB that host allocated for decoding	Undef
ALLOCATED_MV_SIZE	0x006C	W	Size of motion vector buffers that host allocated for decoding	Undef
P_B_FRAME_QP	0x0070	W	P frame QP and B frame QP	Undef
ASPECT_RATIO_IDC	0x0074	W	VUI aspect ratio IDC for H.264 encoding	Undef
EXTENDED_SAR	0x0078	W	Extended sample aspect ratio for H.264 VUI encoding	Undef
DISP_PIC_PROFILE	0x007C	R	Profile info for displayed picture	Undef
FLUSH_CMD_TYPE	0x0080	R	Type of a flushed command	Undef
FLUSH_CMD_INBUF1	0x0084	R	Input buffer pointer of a flushed command	Undef
FLUSH_CMD_INBUF2	0x0088	R	Input buffer pointer of a flushed command	Undef
FLUSH_CMD_OUTBUF	0x008C	R	Output buffer pointer of a flushed command	Undef
NEW_RC_BIT_RATE	0x0090	W	Updated target bit rate	Undef
NEW_RC_FRAME_RATE	0x0094	W	Updated target frame rate	Undef
NEW_I_PERIOD	0x0098	W	Updated intra period	Undef

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Register	Address	R/W	Description	Reset Value
H264_I_PERIOD	0x009C	W	Intra picture period to generate open GOP. Valid for H.264 encoder only	Undef
RC_CONTROL_CONFIG	0x00A0	W	Rate control configuration register for fixed target bit control	Undef
BATCH_INPUT_ ADDR	0x00A4	W	Start address of the input structure for batch encoding	Undef
BATCH_OUTPUT_ADDR	0x00A8	W	Start address of the output structure for batch encoding	Undef
BATCH_OUTPUT_ SIZE	0x00AC	W	Size of the output structure for batch encoding	Undef
MIN_LUMA_DPB_SIZE	0x00B0	R	Minimum size of luma DPB that host needs to allocate for decoding	Undef
H264_POC_TYPE	0x00B8	R	POC_TYPE of H.264 decoder.	Undef
MIN_CHROMA_DPB_SIZE	0x00BC	R	Minimum size of chroma DPB that host needs to allocate for decoding	Undef
DISP_PIC_FRAME_TYPE	0x00C0	R	Frame type of a displayed picture	Undef
FREE_LUMA_DPB	0x00C4	R	Available luma DPB address	Undef
ASPECT_RATIO_INFO	0x00C8	R	Aspect ratio information for MPEG4 decoding	Undef
EXTENDED_PAR	0x00CC	R	Extended pixel aspect ratio information for MPEG4 decoding	Undef
DBG_HISTORY_INPUT0	0x00D0	W	Debug history input register 0 for stage counter settings	Undef
DBG_HISTORY_INPUT1	0x00D4	W	Debug history input register 1 for stage counter settings	Undef
DBG_HISTORY_OUTPUT	0x00D8	R	Output size register for stage counter history	Undef
HIERARCHICAL_P_QP	0x00E0	W	QP for hierarchical P frames	Undef

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6.3.2 CONTROL REGISTERS

6.3.2.1 MFC Core Control Register

6.3.2.1.1 MFC Software Reset Register (MFC_SW_RESET, R/W, Address = 0xF170_0000)

MFC_SW_RESET	Bit	Description	Initial State
Reserved	[31:10]	Reserved	0
RSTN_RG_MPEG2	[9]	Soft reset for RG_MPEG2	1
RSTN_RG_MPEG4	[8]	Soft reset for RG_MPEG4	1
RSTN_RG_VC1	[7]	Soft reset for RG_VC1	1
RSTN_RG_H264	[6]	Soft reset for RG_H264	1
RSTN_RG_COMMON	[5]	Soft reset for RG_COMMON and RG_DECCOM	1
RSTN_DMX	[4]	Soft reset for DMX 0	1
RSTN_VI	[3]	Soft reset for VI	1
RSTN_MFCCORE	[2]	Soft reset for MFC core	1
RSTN_MC	[1]	Soft reset for MC	1
RSTN_RISC	[0]	Soft reset for RISC core	0

6.3.2.1.2 RISC to Host Interrupt Register (MFC_RISC_HOST_INT, R/W, Address = 0xF170_0008)

MFC_RISC_HOST_INT	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
INTERRUPT	[0]	0 = Interrupt clear 1 = Interrupt is raised by MFC	0

6.3.2.1.3 HOST2RISC Command Register (MFC_HOST2RISC_COMMAND, R/W, Address = 0xF170_0030)

MFC_HOST2RISC_COMMAND	Bit	Description	Initial State
HOST2RISC_COMMAND	[31:0]	0 = No operation 1 = OPEN_CH (open instance) 2 = CLOSE_CH (close instance) 3 = SYS_INIT (system initialization) 4 = FLUSH_COMMAND (flush commands in ch0, ch1) 5 = SLEEP 6 = WAKEUP 7 = CONTINUE_ENC (continue encoding) 8 = ABORT_ENC (abort encoding)	0

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6.3.2.1.4 HOST2RISC Argument Registers (MFC_HOST2RISC_ARG1, R/W, Address = 0xF170_0034)

MFC_HOST2RISC_ARG1	Bit	Description	Initial State
HOST2RISC_ARG1	[31:0]	As per HOST2RISC_COMMAND, HOST2RISC_ARG has different meanings as follows. <OPEN_CH> A codec type should be specified as follows. 0 = H.264 Decoding 1 = VC1 Advanced Profile Decoding 2 = MPEG4 / XVid Decoding 3 = MPEG1/MPEG2 Decoding 4 = H.263 Decoding 5 = VC1 Simple/Main Profile Decoding 6 = Reserved 7 = Reserved 8 = Reserved 9 = Reserved 16 = H.264 Encoding 17 = MPEG4 Encoding 18 = H.263 Encoding 19 = VC9 Decoding 20 = VC1 Decoding without start code <CLOSE_CH> An instance ID to close should be specified <SYS_INIT> Size of the memory for the firmware should be specified (currently 400KB)	0

6.3.2.1.5 HOST2RISC Argument Registers (MFC_HOST2RISC_ARG2, R/W, Address = 0xF170_0038)

MFC_HOST2RISC_ARG2	Bit	Description	Initial State
Reserved	[31]	Reserved	0
HOST2RISC_ARG2	[30:0]	When HOST2RISC_COMMAND is OPEN_CH, it enables/disables pixel cache <Encoder> 0 = Enable pixel cache 3 = Disable pixel cache <Decoder> 0 = Enable pixel cache for P picture only 1 = Enable pixel cache for B picture only 2 = Enable pixel cache for both P and B pictures 3 = Disable pixel cache	0

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6.3.2.1.6 HOST2RISC Argument Registers (MFC_HOST2RISC_ARG3, R/W, Address = 0xF170_003C)

MFC_HOST2RISC_ARG3	Bit	Description	Initial State
CONTEXT_ADDR	[31:0]	Context memory address for an instance	0

6.3.2.1.7 HOST2RISC Argument Registers (MFC_HOST2RISC_ARG4, R/W, Address = 0xF170_0040)

MFC_HOST2RISC_ARG4	Bit	Description	Initial State
CONTEXT_SIZE	[31:0]	Context memory size for an instance. H.264 decoder requires 600KB and others require 10KB.	0

6.3.2.1.8 RISC2HOST Command Register (MFC_RISC2HOST_COMMAND, R/W, Address = 0xF170_0044)

MFC_RISC2HOST_ COMMAND	Bit	Description	Initial State
RISC2HOST_COMMAND	[31:0]	0 = RISC2HOST_CMD_EMPTY 1 = RISC2HOST_CMD_OPEN_CH_RET 2 = RISC2HOST_CMD_CLOSE_CH_RET 3 = Reserved 4 = RISC2HOST_CMD_SEQ_DONE_RET 5 = RISC2HOST_CMD_FRAME_DONE_RET 6 = RISC2HOST_CMD_SLICE_DONE_RET 7 = RISC2HOST_CMD_ENC_COMPLETE_RET 8 = RISC2HOST_CMD_SYS_INIT_RET 9 = RISC2HOST_CMD_FIRMWARE_STATUS_RET 10 = RISC2HOST_CMD_SLEEP_RET 11 = RISC2HOST_CMD_WAKEUP_RET 12 = RISC2HOST_CMD_FLUSH_COMMAND_RET 13 = RISC2HOST_CMD_ABORT_RET 14 = RISC2HOST_CMD_BATCH_ENC_RET 15 = RISC2HOST_CMD_INIT_BUFFERS_RET 16 = RISC2HOST_CMD_EDFU_INT_RET 17~31 = Reserved 32 = RISC2HOST_CMD_ERROR_RET	0

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6.3.2.1.9 RISC2HOST Argument Registers (MFC_RISC2HOST_ARG1, R/W, Address = 0xF170_0048)

MFC_RISC2HOST_ARG1	Bit	Description	Initial State
MFC_RISC2HOST_ARG1	[31:0]	<OPEN> An instance ID will be returned <SYS_INIT> Firmware memory size will be returned(currently 400KB) <SEQ_START, FRAME_START, LAST_SEQ, INIT_BUFFERS, FRAME_START_REALLOC> A channel ID will be returned <FLUSH_COMMAND> [31:16]: Instance ID of CH1 [15:0]: Instance ID of CH0	0

NOTE: When host receives FLUSH_COMMAND_RET, it should check the shared memory at 0x80. 0x8C to figure out the input and output pointers in each command channel. If [31:16] is not 0xFFFF, a command in CH1 has been flushed. If [15:0] is not 0xFFFF, a command in CH0 has been flushed.

6.3.2.1.10 RISC2HOST Argument Registers (MFC_RISC2HOST_ARG2, R/W, Address = 0xF170_004C)

MFC_RISC2HOST_ARG2	Bit	Description	Initial State
DISP_ERROR_STATUS	[31:16]	Error status for the displayed frame. Error codes are defined in 1.3.2.2	0
DEC_ERROR_STATUS	[15:0]	Error status for the decoded/encoded frame. Error codes are defined in 1.3.2.2	0

6.3.2.1.11 RISC2HOST Argument Registers (MFC_RISC2HOST_ARG3, R/W, Address = 0xF170_0050)

MFC_RISC2HOST_ARG3	Bit	Description	Initial State
MFC_RISC2HOST_ARG3	[31:0]	<CONTINUE_ENC> The size of the output stream	0

6.3.2.1.12 RISC2HOST Argument Registers (MFC_RISC2HOST_ARG4, R/W, Address = 0xF170_0054)

MFC_RISC2HOST_ARG4	Bit	Description	Initial State
MFC_RISC2HOST_ARG4	[31:0]	Reserved	0

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6.3.2.1.13 FIRMWARE Version Register (MFC_FIRMWARE_VERSION, R, Address = 0xF170_0058)

MFC_FIRMWARE_VERSION	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
YEAR	[23:16]	Year : 00~99 (00 means 2000)	0
MONTH	[15:8]	Month : 1~12	0
DAY	[7:0]	Day : 1~31	0

6.3.2.1.14 Debug Information Output Register1 (DBG_INFO_OUTPUT1, R, Address = 0xF170_0064)

DBG_INFO_OUTPUT1	Bit	Description	Initial State
INTERMEDIATE_STAGE_COUNTER	[31:0]	Intermediate stage counter for different stages of MFC firmware. This counter values will have different interpretation for each codec.	0

6.3.2.1.15 Debug Information Output Register2 (DBG_INFO_OUTPUT2, R, Address = 0xF170_0068)

DBG_INFO_OUTPUT2	Bit	Description	Initial State
EXCEPTION_STATUS	[31:0]	The status of the exception handler 0x01 = Bus error handler 0x02 = Illegal instruction handler 0x04 = Tick handler 0x10 = Trap handler 0x20 = Align handler 0x40 = Range handler 0x80 = DTLB miss exception handler 0x100 = ITLB miss exception handler 0x200 = Data page fault exception handler 0x400 = Instruction page fault exception handler	0

6.3.2.1.16 Firmware Status Register (MFC_FIRMWARE_STATUS, R, Address = 0xF170_0080)

MFC_FIRMWARE_STATUS	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
FIRMWARE_STATUS	[0]	0 = Not ready 1 = Ready	0

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6.3.2.2 Error Codes

Error Code	Error Name	Description
<Command control errors>		
1	INVALID_CHANNEL_NUMBER	If the channel used is more than the allowed limit. Currently it should be within range 0-15.
2	INVALID_COMMAND_ID	If the command used is illegal. Please use the commands given in the CHx_INST_ID register specification.
3	CHANNEL_ALREADY_IN_USE	If the channel is already open and host is again trying to open the channel before closing it.
4	CHANNEL_NOT_OPEN_BEFORE_CHANNEL_CLOSE	If the CLOSE_CH is done before OPEN_CH (i.e., at OPEN_CH = 0).
5	OPEN_CH_ERROR_SEQ_START	If the channel is not open. (ERROR in SEQ_START)
6	SEQ_START_ALREADY_CALLED	If SEQ_START is already done and again. SEQ_START is issued for the same channel.
7	OPEN_CH_ERROR_INIT_BUFFERS	If the channel is not open in INIT_BUFFERS
8	SEQ_START_ERROR_INIT_BUFFERS	If SEQ_START is not complete before INIT_BUFFERS.
9	INIT_BUFFER_ALREADY_CALLED	If INIT_BUFFERS is already done and again. INIT_BUFFERS is issued for the same channel.
10	OPEN_CH_ERROR_FRAME_START	If the channel is not open. (ERROR in FRAME_START)
11	SEQ_START_ERROR_FRAME_START	If SEQ_START is not complete before FRAME_START.
12	INIT_BUFFERS_ERROR_FRAME_START	If INIT_BUFFERS is not complete before FRAME_START
13	CODEC_LIMIT_EXCEEDED	Number of codecs are more than 16 (Currently this is not applicable)
20	MEM_ALLOCATION_FAILED	Memory allocation failed in the firmware
25	INSUFFICIENT_CONTEXT_SIZE	Context buffer size is in sufficient
<SEQ_START errors>		
27	UNSUPPORTED_FEATURE_IN_PROFILE	Features like CABAC/Interlace are not supported in baseline profile
28	RESOLUTION_NOT_SUPPORTED	Resolution is not supported
<Decoder fatal errors on SEQ_START>		
52	HEADER_NOT_FOUND	Header not found
<Encoder fatal errors on SEQ_START>		

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Error Code	Error Name	Description
61	RESERVED	Reserved
62	FRAME_RATE_NOT_SUPPORED	When Rate Control is enabled, Frame Rate cannot have a zero value
63	INVALID_QP_VALUE	Invalid Qp value set
64	INVALID_RC_REACTION_ COEFFICIENT	Invalid value for Rate Control reaction parameter. Value of zero is prohibited
65	INVALID_CPB_SIZE_AT_ GIVEN_LEVEL	Invalid value of CPB/VBV size at given level. This violates Annex A in H.264
<INIT_BUFFERS errors>		
71	ALLOC_DPB_SIZE_NOT_ SUFFICIENT	Allocated DPB SIZE is insufficient
72	RESERVED	Reserved
73	RESERVED	Reserved
74	NUM_DPB_OUT_OF_RANGE	NUM_DPB is out of range. It should be equal or greater than MIN_NUM_DPB and equal or smaller than 32.
77	NULL_METADATA_INPUT_POINTER	External metadata input structure address is null
78	NULL_DPB_POINTER	The allocated DPB address is null
79	NULL_OTH_EXT_BUF_ADDR	Other external buffers for decoder are NULL.
80	NULL_MV_POINTER	MV address is null
<Common HW errors>		
81	DIVIDE_BY_ZERO	Divide by zero error
82	BIT_STREAM_BUF_EXHAUST	Bit stream buffer exhausted
83	DESCRIPTOR_BUFFER_ EMPTY	Empty descriptor buffer (valid for H264 and VC1 decoders only)
84	DMA_TX_NOT_COMPLETE	DMA operation not complete
<Decoder HW errors>		
85	MB_HEADER_NOT_DONE	MB header decode not done
86	MB_COEFF_NOT_DONE	MB coeff (entropy decoding)
87	CODEC_SLICE_NOT_DONE	Codec slice done error
88	MFC_CORE_TIME_OUT	Time out happens during the HW processing
89	VC1_BITPLANE_DECODE_ERR	VC1 bit plane decode error
<Encoder HW errors>		
90	VSP_NOT_READY	VSP not ready

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Error Code	Error Name	Description
91	BUFFER_FULL_STATE	Buffer full
<Decoder errors on FRAME_RUN>		
112	RESOLUTION_MISMATCH	GOV has a resolution which exceeds the values in the sequence header
113	NV_QUANT_ERR	Errors in the quantization parameters
114	SYNC_MARKER_ERR	Sync marker error
115	FEATURE_NOT_SUPPORTED	Unsupported feature in the profile
116	MEM_CORRUPTION	MFC core memory corruption
117	INVALID_REFERENCE_FRAME	Refernce frame(s) not available
118	PICTURE_CODING_TYPE_ERR	PICTURE_CODING_TYPE error in MPEG2
119	MV_RANGE_ERR	Invalid Fcode (MV _Range)
120	PICTURE_STRUCTURE_ERR	Picture_structure (FRAME/TOP/BOTTOM field)
121	SLICE_ADDR_INVALID	Invalid slice address
122	NON_PAIRED_FIELD_NOT_SUPPORTED	Non-paired field is not supported
123	NON_FRAME_DATA_RECEIVED	Frame data is not received. Only header (e.g., seq header, SPS/PPS, SEI) is received
124	INCOMPLETE_FRAME	Incomplete frame data is received (e.g., only part of slices are received)
125	NO_BUFFER_RELEASED_FROM_HOST	No Free buffer available. All the buffers are either locked by host or they are anchor frames and cannot be used.
128	NALU_HEADER_ERROR	Invalid NALU Header
129	SPS_PARSE_ERROR	Invalid syntax element in SPS
130	PPS_PARSE_ERROR	Invalid syntax element in PPS
131	SLICE_PARSE_ERROR	Invalid syntax element in slice header
< Common warnings>		
145	COMMAND_FLUSHED	FRAME_START command has been flushed from the command channels 0 and 1
< Decoder warnings>		
150	METADATA_NO_SPACE_NUM_CONCEAL_MB	Out of space for the number of concealed MB metadata output
151	METADATA_NO_SPACE_QP	Out of space for QP metadata output
152	METADATA_NO_SAPCE_CONCEAL_MB	Out of space for concealed MB output
153	METADATA_NO_SPACE_VC1_PARAM	Out of space for VC1 parameter output

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Error Code	Error Name	Description
154	METADATA_NO_SPACE_SEI	Out of space for SEI information output
155	METADATA_NO_SPACE_VUI	Out of space for VUI information output
156	METADATA_NO_SPACE_EXTRA	Out of space for extra data output
157	METADATA_NO_SPACE_DATA_NONE	Out of space for DataNone
158	FRAME_RATE_UNKNOWN	Frame rate unknown
159	ASPECT_RATIO_UNKOWN	Aspect ratio unknown
160	COLOR_PRIMARIES_UNKNOWN	Invalid color primaries
161	TRASNFER_CHAR_UNKWON	Invalid trasnsfer characterstics
162	MATRIX_COEFF_UNKNOWN	Invalid matrix coefficients
163	NON_SEQ_SLICE_ADDR	New slice address is not sequencial with respect to the old one
164	BROKEN_LINK	Current GOV has B pictures whose anchor frame is in the previous GOV
165	FRAME_CONCEALED	Error Concealment done by MFC
166	PROFILE_UNKOWN	Profile unknown
167	LEVEL_UNKOWN	Level unknown
168	BIT_RATE_NOT_SUPPORTED	Bit rate not supported
169	COLOR_DIFF_FORMAT_NOT_SUPPORTED	Color format is not supported
170	NULL_EXTRA_METADATA_POINTER	The allocated memory for extra metadata is null
171	SYNC_POINT_NOT_RECEIVED_STARTED_DECODING	DPB is empty but received a non I/IDR frame. MFC has started decoding from Non IDR
172	NULL_FW_DEBUG_INFO_POINTER	FW debug info address issued is null
173	ALLOC_DEBUG_INFO_SIZE_INSUFFICIENT	Allocated size for debug info is insufficient
<Encoder warnings>		
180	METADATA_NO_SPACE_	Out of space for Macroblock information output.

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Error Code	Error Name	Description
	MB_INFO	(Applicable only for H.264 encoder)
181	METADATA_NO_SPACE_ SLICE_SIZE	Out of space for slice size output
182	RESOLUTION_WARNING	Resoultion setting is not supported for given H.263 encoder profile

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6.3.2.3 Memory Controller Registers

6.3.2.3.1 Channel A DRAM Base Address Register (MFC_MC_DRAMBASE_ADDR_A, R/W, Address = 0xF170_0508)

MFC_MC_DRAMBASE_ADDR_A	Bit	Description	Initial State
MC_DRAMBASE_ADDR_A	[31:17]	The DRAM base address must be aligned at 128KByte. MFC's access range through port A is from DRAMBASE_ADDR_A to DRAMBASE_ADDR_A + 256MByte	0x6980
Reserved	[16:0]	Reserved	0

6.3.2.3.2 Channel B DRAM Base Address Register (MFC_MC_DRAMBASE_ADDR_B, R/W, Address = 0xF170_050C)

MFC_MC_DRAMBASE_ADDR_B	Bit	Description	Initial State
MC_DRAMBASE_ADDR_B	[31:17]	The DRAM base address must be aligned at 128KByte. MFC's access range through port B is from DRAMBASE_ADDR_B to DRAMBASE_ADDR_B + 256MByte	0x1180
Reserved	[16:0]	Reserved	0

6.3.2.3.3 MC (Memory Controller) Status Register (MFC_MC_STATUS, R, Address = 0xF170_0510)

MFC_MC_STATUS	Bit	Description	Initial State
Reserved	[31:2]	Not used	0
MC_BUSY_B	[1]	Busy at port B 0 = Idle 1 = Busy	X
MC_BUSY_A	[0]	Busy at port A 0 = Idle 1 = Busy	X

NOTE: X stands for undetermined.

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6.3.2.4 Common Address Control

Common base address is variously used for each codec. The interpretation of the common base address is varying. Detailed descriptions are shown in 6.3.2.5 and 6.3.2.6 .

Base addresses of common 0~63 are defined for AXI_MEMORY_A, and common 64~127 are defined for AXI_MASTER_B. Base address is determined as follows.

Base address calculation: (MC_DRAMBASE_ADDR) + (MFC_COMMON_BASE_ADDR<<11)

6.3.2.4.1 For Port_A: Common Baseram Register 0 ~ 63

Common Baseram Register 0 ~ 63	Address	Description	R/W	Initial State
MFC_COMMON_BASE_ADDR_0 [16:0]	0xF170_0600	Codec common memory region for start address.	R/W	X
~				
MFC_COMMON_BASE_ADDR_63 [16:0]	0xF170_06FC	Codec common memory region for start address.	R/W	X

6.3.2.4.2 For Port_B: Common Baseram Register 64 ~ 127

Common Baseram Register 64 ~ 127	Address	Description	R/W	Initial State
MFC_COMMON_BASE_ADDR_64 [16:0]	0xF170_0700	Codec common memory region for start address.	R/W	X
~				
MFC_COMMON_BASE_ADDR_127 [16:0]	0xF170_07FC	Codec common memory region for start address.	R/W	X

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6.3.2.5 Buffer Address of Decoder

The base address settings for different standards are described in this section.

- H264 Decoder

Memory Region	Register Name	Description
H264DEC_VERT_NB_MV	MFC_COMMON_BASE_ADDR_35	Vertical Neighbor Motion Vector Buffer
H264DEC_NB_IP	MFC_COMMON_BASE_ADDR_36	Neighbor pixels for Intra Prediction Buffer
H264DEC_LUMA_x	MFC_COMMON_BASE_ADDR_64~95	Luma DPB for master channel A
H264DEC_CHROMA_x	MFC_COMMON_BASE_ADDR_0~31	Chroma DPB for master channel B
H264DEC_MV_x	MFC_COMMON_BASE_ADDR_96~127	MV buffer for H.264

- MPEG4 Decoder

Memory Region	Register Name	Description
DEC_NB_DCAC	MFC_COMMON_BASE_ADDR_35	Neighbor information of stream parser
DEC_UPNB_MV	MFC_COMMON_BASE_ADDR_36	Neighbor information of stream parser
DEC_SUB_ANCHOR_MV	MFC_COMMON_BASE_ADDR_37	Neighbor information of stream parser
OVERLAP_TRANSFORM	MFC_COMMON_BASE_ADDR_38	Information for Motion Compensation
DEC_STX_PARSER	MFC_COMMON_BASE_ADDR_42	Syntax Parser Buffer
DEC_LUMA_x	MFC_COMMON_BASE_ADDR_64~95	Reconstructed luma plane
DEC_CHROMA_x	MFC_COMMON_BASE_ADDR_0~31	Reconstructed chroma plane

- MPEG2 Decoder

Memory Region	Register Name	Description
DEC_LUMA_x	MFC_COMMON_BASE_ADDR_64~95	Reconstructed luma plane
DEC_CHROMA_x	MFC_COMMON_BASE_ADDR_0~31	Reconstructed chroma plane

- H.263 Decoder

Memory Region	Register Name	Description
DEC_NB_DCAC	MFC_COMMON_BASE_ADDR_35	Neighbor information of stream parser
DEC_UPNB_MV	MFC_COMMON_BASE_ADDR_36	Neighbor information of stream parser
DEC_SUB_ANCHOR_MV	MFC_COMMON_BASE_ADDR_37	Neighbor information of stream parser
OVERLAP_TRANSFORM	MFC_COMMON_BASE_ADDR_38	Information for Motion Compensation
DEC_LUMA_x	MFC_COMMON_BASE_ADDR_64~95	Reconstructed luma plane
DEC_CHROMA_x	MFC_COMMON_BASE_ADDR_0~31	Reconstructed chroma plane

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- VC1 Decoder

Memory Region	Register Name	Description
DEC_NB_DCAC	MFC_COMMON_BASE_ADDR_35	Neighbor information of stream parser
DEC_UPNB_MV	MFC_COMMON_BASE_ADDR_36	Neighbor information of stream parser
DEC_SUB_ANCHOR_MV	MFC_COMMON_BASE_ADDR_37	Neighbor information of stream parser
OVERLAP_TRANSFORM	MFC_COMMON_BASE_ADDR_38	Information for Motion Compensation
BITPLANE3	MFC_COMMON_BASE_ADDR_39	BitPlane
BITPLANE2	MFC_COMMON_BASE_ADDR_40	
BITPLANE1	MFC_COMMON_BASE_ADDR_41	
DEC_LUMA_x	MFC_COMMON_BASE_ADDR_64~95	Reconstructed luma plane
DEC_CHROMA_x	MFC_COMMON_BASE_ADDR_0~31	Reconstructed chroma plane

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- Buffer Memory Size for Decoder

Memory Region	Size			
	H.264	MPEG4/H.263	VC1	MPEG2
CH_ES_ADDR	Up to 4MB			
CH_DESC_ADDR	Up to 128KB			
DEC_NB_DCAC	-	16KB	16KB	-
DEC_UPNB_MV	-	68KB	68KB	-
DEC_SUB_ANCHOR_MV	-	136KB	136KB	-
DEC_OVERLAP_TRANSFORM	-	32KB	32KB	-
DEC_BITPLANE3	-	-	2KB	-
DEC_BITPLANE2	-	-	2KB	-
DEC_BITPLANE1	-	-	2KB	-
DEC_STX_PARSER	-	68KB(not needed for H263)	-	-
DEC_LUMA_x	-	align(align(x_size, 128) * align(y_size, 32), 8192)		
DEC_CHROMA_x	-	align(align(x_size, 128) * align(y_size/2, 32), 8192)		
H264DEC_VERT_NB_MV	16KB	-	-	-
H264DEC_NB_IP	32KB	-	-	-
H264DEC_CHROMA_x	align(align(x_size, 128) * align(y_size/2, 32), 8192) + align(align(x_size, 128) * align(y_size/4, 32), 8192)	-	-	-
H264DEC_LUMA_x	align(align(x_size, 128) * align(y_size, 32), 8192)	-	-	-
H264DEC_MV_x	Quarter size of H.264 Luma DPB align(align(x_size, 128) * align(y_size/4, 32), 8192)	-	-	-

NOTE:

1. All linear information in this table should be aligned at 2KB, whereas tile mode information (luma/chroma DPB and H264DEC_MV) should be aligned at 8KB.
2. DPB size did not take into account the QP save area.
3. x ranges 0~31 for LUMA_x, CHROMA_x, MV_x.

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6.3.2.6 Buffer Address of Encoder

- H.264 Encoder

Memory Region	Register Name in User's Manual	Description
ENC_DPB_Y0_ADDR	MFC_COMMON_BASE_ADDR_7	Reconstructed Y0 buffer
ENC_DPB_C0_ADDR	MFC_COMMON_BASE_ADDR_64	Reconstructed C0 buffer
ENC_DPB_Y1_ADDR	MFC_COMMON_BASE_ADDR_8	Reconstructed Y1 buffer
ENC_DPB_C1_ADDR	MFC_COMMON_BASE_ADDR_65	Reconstructed C1 buffer
ENC_DPB_Y2_ADDR	MFC_COMMON_BASE_ADDR_68	Reconstructed Y2 buffer
ENC_DPB_C2_ADDR	MFC_COMMON_BASE_ADDR_66	Reconstructed C2 buffer
ENC_DPB_Y3_ADDR	MFC_COMMON_BASE_ADDR_69	Reconstructed Y3 buffer
ENC_DPB_C3_ADDR	MFC_COMMON_BASE_ADDR_67	Reconstructed C3 buffer
UPPER_MV_ADDR	MFC_COMMON_BASE_ADDR_0	Upper row MV storage region
DIRECT_COLZERO_FLAG_ADDR	MFC_COMMON_BASE_ADDR_4	Direct colocated flag storage region
UPPER_INTRA_MD_ADDR	MFC_COMMON_BASE_ADDR_2	Upper row current pixel data storage region
UPPER_INTRA_PRED_ADDR	MFC_COMMON_BASE_ADDR_80	Upper row pre-filter reconstruction data storage region
NBOR_INFO_MPENC_ADDR	MFC_COMMON_BASE_ADDR_1	Neighbor MB information storage region

- H.263 Encoder

Memory Region	Register Name in User's Manual	Description
ENC_DPB_Y0_ADDR	MFC_COMMON_BASE_ADDR_7	Reconstructed Y0 buffer
ENC_DPB_C0_ADDR	MFC_COMMON_BASE_ADDR_64	Reconstructed C0 buffer
ENC_DPB_Y1_ADDR	MFC_COMMON_BASE_ADDR_8	Reconstructed Y1 buffer
ENC_DPB_C1_ADDR	MFC_COMMON_BASE_ADDR_65	Reconstructed C1 buffer
ENC_DPB_Y2_ADDR	MFC_COMMON_BASE_ADDR_68	Reconstructed Y2 buffer
ENC_DPB_C2_ADDR	MFC_COMMON_BASE_ADDR_66	Reconstructed C2 buffer
ENC_DPB_Y3_ADDR	MFC_COMMON_BASE_ADDR_69	Reconstructed Y3 buffer
ENC_DPB_C3_ADDR	MFC_COMMON_BASE_ADDR_67	Reconstructed C3 buffer
UPPER_MV_ADDR	MFC_COMMON_BASE_ADDR_0	Upper row MV storage region
ACDC_COEF_BASE_ADDR	MFC_COMMON_BASE_ADDR_1	Upper row inverse quantization coefficient storage region

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- MPEG4 Encoder

Memory Region	Register Name in User's Manual	Description
ENC_DPB_Y0_ADDR	MFC_COMMON_BASE_ADDR_7	Reconstructed Y0 buffer
ENC_DPB_C0_ADDR	MFC_COMMON_BASE_ADDR_64	Reconstructed C0 buffer
ENC_DPB_Y1_ADDR	MFC_COMMON_BASE_ADDR_8	Reconstructed Y1 buffer
ENC_DPB_C1_ADDR	MFC_COMMON_BASE_ADDR_65	Reconstructed C1 buffer
ENC_DPB_Y2_ADDR	MFC_COMMON_BASE_ADDR_68	Reconstructed Y2 buffer
ENC_DPB_C2_ADDR	MFC_COMMON_BASE_ADDR_66	Reconstructed C2 buffer
ENC_DPB_Y3_ADDR	MFC_COMMON_BASE_ADDR_69	Reconstructed Y3 buffer
ENC_DPB_C3_ADDR	MFC_COMMON_BASE_ADDR_67	Reconstructed C3 buffer
UPPER_MV_ADDR	MFC_COMMON_BASE_ADDR_0	Upper row MV storage region
DIRECT_COLZERO_FLAG_ADDR	MFC_COMMON_BASE_ADDR_4	Skip flag storage region
ACDC_COEF_BASE_ADDR	MFC_COMMON_BASE_ADDR_1	Upper row inverse quantization coefficient storage region

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- Buffer Memory Size for Encoder

Memory Region	H.264	MPEG4 / H.263
ENC_DPB_Y0_ADDR	align(align(x_size, 128) * align(y_size, 32), 8192)	
ENC_DPB_C0_ADDR	align(align(x_size, 128) * align(y_size/2, 32), 8192)	
ENC_DPB_Y1_ADDR	align(align(x_size, 128) * align(y_size, 32), 8192)	
ENC_DPB_C1_ADDR	align(align(x_size, 128) * align(y_size/2, 32), 8192)	
ENC_DPB_Y2_ADDR	align(align(x_size, 128) * align(y_size, 32), 8192)	
ENC_DPB_C2_ADDR	align(align(x_size, 128) * align(y_size/2, 32), 8192)	
ENC_DPB_Y3_ADDR	align(align(x_size, 128) * align(y_size, 32), 8192)	
ENC_DPB_C3_ADDR	align(align(x_size, 128) * align(y_size/2, 32), 8192)	
CH_SB_ADDR	Configurable. Limit1: Should be aligned at 2KB Limit2: Should be a multiple of 4KB	Configurable. Limit1: Should be aligned at 2KB Limit2: Should be a multiple of 4KB
UPPER_MV_ADDR	align(xMB_size * 2 * 8, 2048) byte	align(xMB_size * 2 * 8, 2048)byte
DIRECT_COLZERO_FLAG_ADDR	align(((xMB_size * yMB_size+7)/8) * 8, 2048) byte	align(((xMB_size * yMB_size+7)/8) * 8, 2048) byte (not required for H263 encoder)
UPPER_INTRA_MD_ADDR	align(xMB_size * 48, 2048) byte	-
UPPER_INTRA_PRED_ADDR	align(1024 * 2 * 8, 2048) byte	-
NBOR_INFO_MPENC_ADDR	CAVLC: align(xMB_size * 8 * 8, 2048) byte CABAC: align(xMB_size * 24 * 8, 2048) byte	-
ACDC_COEF_BASE_ADDR	-	align((x_size/2) * 8, 2048) byte

NOTE:

1. All linear information in this table should be aligned at 2KB, whereas tile mode information (luma/chroma DPB) should be aligned at 8KB.
2. The division operation in the table is an integer division.
3. When 1 reference P is used, the required DPBs are DPB_Y0, DPB_Y1, DPB_C0, and DPB_C1 only. Current luma, chroma buffers are placed in the opposite port.

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6.3.3 CODEC REGISTERS

6.3.3.1 Codec Common Registers

6.3.3.1.1 Picture Width in Pixel Register (MFC_HSIZE_PX, R/W, Address = 0xF170_0818)

MFC_HSIZE_PX	Bit	Description	Initial State
Reserved	[31:13]	Reserved	0
PICTURE_WIDTH	[12:0]	Coded width of a picture	0

6.3.3.1.2 Picture Height in Pixel Register (MFC_VSIZE_PX, R/W, Address = 0xF170_081C)

MFC_VSIZE_PX	Bit	Description	Initial State
Reserved	[31:13]	Reserved	0
PICTURE_HEIGHT	[12:0]	Coded height of a picture (field or frame)	0

6.3.3.1.3 Profile Register (MFC_PROFILE, R/W, Address = 0xF170_0830)

MFC_PROFILE	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
LEVEL	[15:8]	Level in MPEG4 and H.264. In H.264, 31 stands for level 3.1 and 9 stands for level 1b. In MPEG4, 3 stands for level 3, 7 stands for level 3b, and 9 stands for level 0b.	0
Reserved	[7:6]	Reserved	0
PROFILE	[5:0]	<MPEG4> [0]: MPEG4_PROFILE 0 = Simple profile 1 = Advanced simple profile <H.264> [1:0]: Profile 0 = Main profile 1 = High profile 2 = Baseline profile Unspecified bits must set to be 0.	0

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6.3.3.1.4 Picture Structure Register (MFC_PICTURE_STRUCT, R/W, Address = 0xF170_083C)

MFC_PICTURE_STRUCT	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
FIELD	[0]	<H.264, MPEG4> 0 = Frame picture only 1 = Field picture	0

6.3.3.1.5 Loop Filter Control Register (MFC_LF_CONTROL, R/W, Address = 0xF170_0848)

MFC_LF_CONTROL	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0
LF_CONTROL	[1:0]	<H.264> [1:0]: Loop filter disable indicator which corresponds to disable_deblocking_filter_idc 0 = Enable 1 = Disable 2 = Disable at slice boundary <MPEG4> [1]: Reserved [0]: Deblocking filter enable (post filter) 0 = Disable 1 = Enable	0

NOTE:
1. This register can be used by both encoders and decoders
2. This register is not effective for MPEG4 encoder
3. This register returns disable_deblocking_filter_idc from the bitstream for H.264 decoding

6.3.3.1.6 H.264 Loop Filter Alpha Offset Register (MFC_LF_ALPHA_OFF, R/W, Address = 0xF170_084C)

MFC_LF_ALPHA_OFF	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
LF_ALPHA_OFF	[4:0]	Loop filter alpha offset for deblocking filter	0

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6.3.3.1.7 H.264 Loop Filter Beta Offset Register (MFC_LF_BETA_OFF, R/W, Address = 0xF170_0850)

MFC_LF_BETA_OFF	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
LF_BETA_OFF	[4:0]	Loop filter beta offset for deblocking filter	0

6.3.3.1.8 QP Information Offset Register (MFC_QP_OFFSET, R/W, Address = 0xF170_0C30)

MFC_QP_OFFSET	Bit	Description	Initial State
MFC_QP_OFFSET	[31:0]	When MFC_QP_OUT_EN is set, QP information is stored at the offset from the luma DPB address. The unit of the offset is double word (64bits).	0

6.3.3.1.9 QP Information Enable Register (MFC_QP_OUT_EN, R/W, Address = 0xF170_0C34)

MFC_QP_OUT_EN	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
MFC_QP_OUT_EN	[0]	If MFC_QP_OUT_EN is enabled, the quantization value of each macroblock will be stored in the luma DPB area. 0 = QP out disable 1 = QP out enable The address is calculated as follows.	0

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```
x_pos = [0...(img_hsize_mb-1)];
y_pos = frame ? [0...(img_vsize_mb-1)] :
            top     ? [0, 2, 4 ...(img_vsize_mb*2-2)] :
                      [1, 3, 5 ...(img_vsize_mb*2-1)] ;

< I_XSIZE >
        if (img_hsize_mb < 64)                  I_XSIZE = 64
             else if ((img_hsize_mb & 0x3f)!=0) I_XSIZE = ((img_hsize_mb>>6)<<6) + 64
        else                                    I_XSIZE = img_hsize_mb

< I_XSIZE >
        if (frame) begin
              if(img_vsize_mb < 32)             I_YSIZE =    32 else if((img_vsize_mb & 0x1f)!=0)
                                                I_YSIZE = ((img_vsize_mb>>5)<<5) + 32 + 32
                 else                           I_YSIZE = img_vsize_mb + 32
        end
        else begin
              if(img_vsize_mb < 16)             I_YSIZE =    32
              else if((img_vsize_mb & 0x1f)!=0) I_YSIZE = ((img_vsize_mb>>4)<<5) + 32 + 32
               else                             I_YSIZE = (img_vsize_mb<<1) + 32
        end

pixel_x_m1 = I_XSIZE -1 ;
pixel_y_m1 = I_YSIZE -1 ;
roundup_x = ((pixel_x_m1)/16/8 + 1) ;
roundup_y = ((pixel_x_m1)/16/4 + 1) ;

x_addr = x_pos/4;
linear_addr0 = (((y_pos    & 0x1f) <<4) |(x_addr & 0xf ) ) << 2 ;
linear_addr1 = (((y_pos >> 6) & 0xff) * roundup_x + ((x_addr >> 5) & 0x7f)) ;



      if(   ((x_addr >> 5) & 0x1) ==    ((y_pos >> 5) & 0x1))
                        bank_addr = ((x_addr >> 4) & 0x1);
      else
                        bank_addr = 0x2 | ((x_addr >> 4) & 0x1);


physical_addr = DRAM_BASE + DPB_OFFSET + QP_OFFSET + (linear_addr1 <<13) | (bank_addr << 11) |
linear_addr0 ;
qp_save_range = (pixel_y_minus[5]==0) ? pixel_y_minus[14:6] * roundup_x + pixel_x_minus[14:8] + 1 :
                                        roundup_x * roundup_y;
```

NOTE: QP values are set to zero for I_PCM macroblocks in H.264 and skipped macroblocks in VC1.
Host should allocate a physical memory size as follows:
- Memory size = ALIGN(img_hsize_mb, 64) * (ALIGN(img_vsize_mb, 32)+32)
Note that qp_save_range above specifies a virtual address area.

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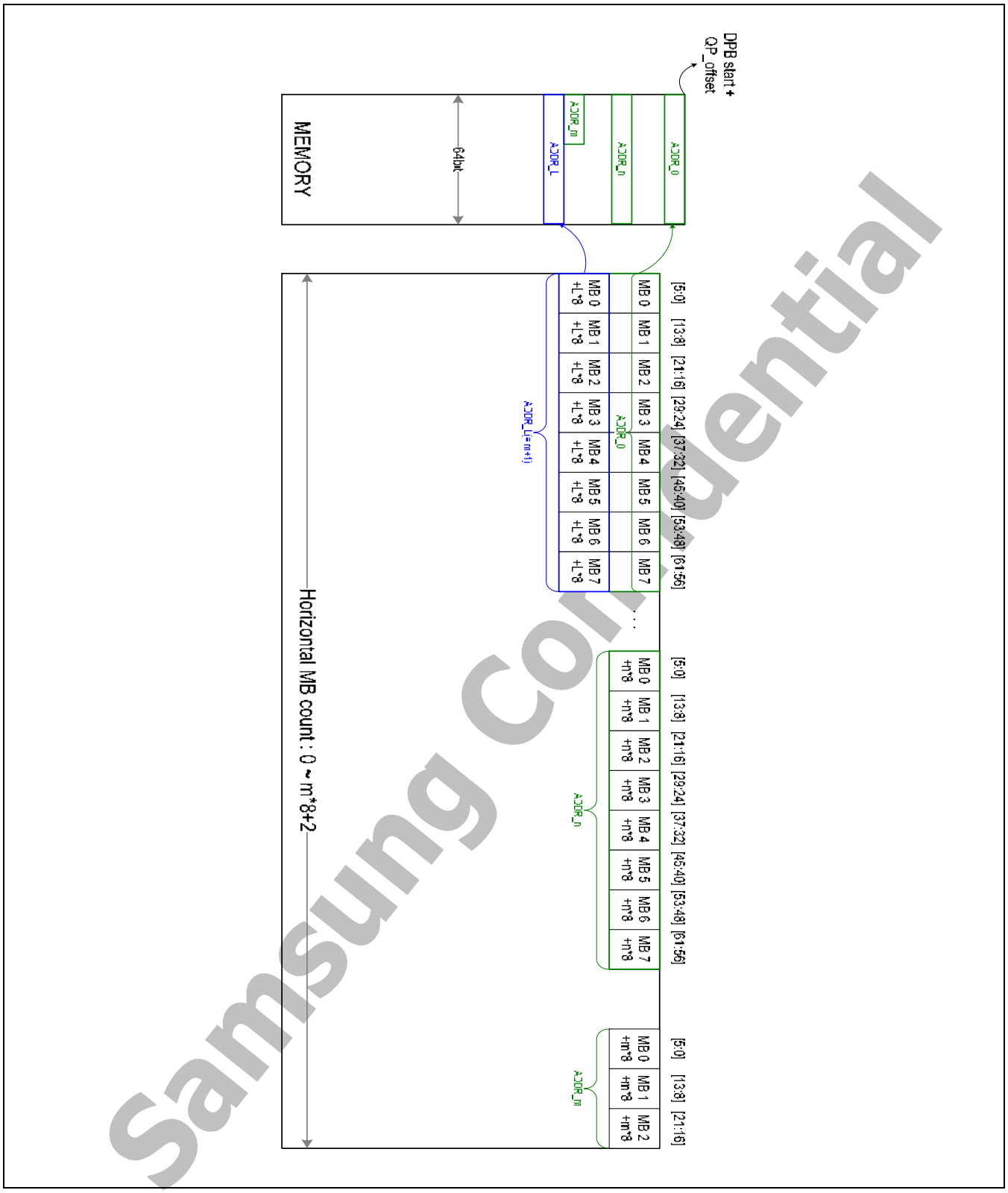

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6.3.3.2 Channel and Stream Interface Registers

There are two sets of channels to communicate between host and MFC. Each channel has two types of registers. One is for response from MFC through MFC_SI_RTN_CHID and 15 MFC_COMMON_SI_RG registers. The other is for command from host through the MFC_SI_CH_INST_ID register and 15 MFC_COMMON_CHx_RG registers.

6.3.3.2.1 Return CH Instance ID Register (MFC_SI_RTN_CHID, R/W, Address = 0xF170_2000)

MFC_SI_RTN_CHID	Bit	Description	Initial State
RTN_CHID	[31:0]	Return channel instance ID which is used to identify which channel's operation is done	0

6.3.3.2.2 Common SI Register 1 ~ 15

- MFC_COMMON_SI_RG_1, R/W, Address = 0xF170_2004
- MFC_COMMON_SI_RG_2, R/W, Address = 0xF170_2008
- MFC_COMMON_SI_RG_3, R/W, Address = 0xF170_200C
- MFC_COMMON_SI_RG_4, R/W, Address = 0xF170_2010
- MFC_COMMON_SI_RG_5, R/W, Address = 0xF170_2014
- MFC_COMMON_SI_RG_6, R/W, Address = 0xF170_2018
- MFC_COMMON_SI_RG_7, R/W, Address = 0xF170_201C
- MFC_COMMON_SI_RG_8, R/W, Address = 0xF170_2020
- MFC_COMMON_SI_RG_9, R/W, Address = 0xF170_2024
- MFC_COMMON_SI_RG_10, R/W, Address = 0xF170_2028
- MFC_COMMON_SI_RG_11, R/W, Address = 0xF170_202C
- MFC_COMMON_SI_RG_12, R/W, Address = 0xF170_2030
- MFC_COMMON_SI_RG_13, R/W, Address = 0xF170_2034
- MFC_COMMON_SI_RG_14, R/W, Address = 0xF170_2038
- MFC_COMMON_SI_RG_15, R/W, Address = 0xF170_203C

MFC_COMMON_SI_RG_ 1 ~ 15	Bit	Description	Initial State
MFC_CH_COMMON_SI_RG_1 ~ 15	[31:0]	For specific meaning of each registers, refer to 6.3.3.3 and 6.3.3.4 .	0

NOTE: Note that the registers from 0xF170_2040 to 0xF170_207C have the same functionality as those from 0xF170_2080 to 0xF170_20BC. The registers from 0xF170_2040 to 0xF170_207C are used for channel 0 and those from 0xF170_2080 to 0xF170_20BC are for channel 1.

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6.3.3.2.3 CH0 Instance ID Register (MFC_SI_CH0_INST_ID, R/W, Address = 0xF170_2040)

MFC_SI_CH0_INST_ID	Bit	Description	Initial State
Reserved	[31:19]	Reserved	0
CH_DEC_TYPE	[18:16]	[1:0]: CH0 control 1 = SEQ_START (sequence header processing) 2 = FRAME_START (frame decoding/encoding) 3 = LAST_SEQ (last frame decoding/encoding) 4 = INIT_BUFFERS (buffer initialization, Decoder only) 5 = FRAME_START_REALLOC (frame decoding for resolution change) 6 = FRAME_BATCH START (frame batch encoding)	
CH_INST_ID	[15:0]	Instance ID for a codec	

6.3.3.2.4 CH1 Instance ID Register (MFC_SI_CH1_INST_ID, R/W, Address = 0xF170_2080)

MFC_SI_CH1_INST_ID	Bit	Description	Initial State
Reserved	[31:19]	Reserved	0
CH_DEC_TYPE	[18:16]	[1:0]: CH1 control 1 = SEQ_START (sequence header processing) 2 = FRAME_START (frame decoding/encoding) 3 = LAST_SEQ (last frame decoding/encoding) 4 = INIT_BUFFERS (buffer initialization. Decoder only) 5 = FRAME_START_REALLOC (frame decoding for resolution change) 6 = FRAME_BATCH START (frame batch encoding)	
CH_INST_ID	[15:0]	Instance ID for Codec	

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6.3.3.2.5 Common CH0 Register 1 ~ 15

- MFC_COMMON_CH0_RG_1, R/W, Address = 0xF170_2044
- MFC_COMMON_CH0_RG_2, R/W, Address = 0xF170_2048
- MFC_COMMON_CH0_RG_3, R/W, Address = 0xF170_204C
- MFC_COMMON_CH0_RG_4, R/W, Address = 0xF170_2050
- MFC_COMMON_CH0_RG_5, R/W, Address = 0xF170_2054
- MFC_COMMON_CH0_RG_6, R/W, Address = 0xF170_2058
- MFC_COMMON_CH0_RG_7, R/W, Address = 0xF170_205C
- MFC_COMMON_CH0_RG_8, R/W, Address = 0xF170_2060
- MFC_COMMON_CH0_RG_9, R/W, Address = 0xF170_2064
- MFC_COMMON_CH0_RG_10, R/W, Address = 0xF170_2068
- MFC_COMMON_CH0_RG_11, R/W, Address = 0xF170_206C
- MFC_COMMON_CH0_RG_12, R/W, Address = 0xF170_2070
- MFC_COMMON_CH0_RG_13, R/W, Address = 0xF170_2074
- MFC_COMMON_CH0_RG_14, R/W, Address = 0xF170_2078
- MFC_COMMON_CH0_RG_15, R/W, Address = 0xF170_207C

MFC_COMMON_CH0_ RG_1 ~ 15	Bit	Description	Initial State
MFC_COMMON_CH0_ RG_1 ~ 15	[31:0]	Host sets the parameters through these registers. For specific meaning of each register, refer to *6.3.3.3* and *6.3.3.4* .	0

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6.3.3.2.6 Common CH1 Register 1 ~ 15

- MFC_COMMON_CH1_RG_1, R/W, Address = 0xF170_2084
- MFC_COMMON_CH1_RG_2, R/W, Address = 0xF170_2088
- MFC_COMMON_CH1_RG_3, R/W, Address = 0xF170_208C
- MFC_COMMON_CH1_RG_4, R/W, Address = 0xF170_2090
- MFC_COMMON_CH1_RG_5, R/W, Address = 0xF170_2094
- MFC_COMMON_CH1_RG_6, R/W, Address = 0xF170_2098
- MFC_COMMON_CH1_RG_7, R/W, Address = 0xF170_209C
- MFC_COMMON_CH1_RG_8, R/W, Address = 0xF170_20A0
- MFC_COMMON_CH1_RG_9, R/W, Address = 0xF170_20A4
- MFC_COMMON_CH1_RG_10, R/W, Address = 0xF170_20A8
- MFC_COMMON_CH1_RG_11, R/W, Address = 0xF170_20AC
- MFC_COMMON_CH1_RG_12, R/W, Address = 0xF170_20B0
- MFC_COMMON_CH1_RG_13, R/W, Address = 0xF170_20B4
- MFC_COMMON_CH1_RG_14, R/W, Address = 0xF170_20B8
- MFC_COMMON_CH1_RG_15, R/W, Address = 0xF170_20BC

MFC_COMMON_CH1_RG_ 1~15	Bit	Description	Initial State
MFC_COMMON_CH1_RG_ 1 ~ 15	[31:0]	While MFC is handling the request on CH0, host can communicate with MFC over CH1. MFC_COMMON_CH1_RG have the same meaning as MFC_COMMON_CH0_RG.	0

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6.3.3.3 Decoder Channel and Stream Interface Registers

6.3.3.3.1 Vertical Resolution Register (MFC_COMMON_SI_RG_1, R, Address = 0xF170_2004)

MFC_COMMON_SI_RG_1	Bit	Description	Initial State
VER_RESOL	[31:0]	Vertical resolution of the current sequence or picture to be displayed. It should be read after decoding sequence header or after decoding a frame (in the case of resolution change).	0

6.3.3.3.2 Horizontal Resolution Register (MFC_COMMON_SI_RG_2, R, Address = 0xF170_2008)

MFC_COMMON_SI_RG_2	Bit	Description	Initial State
HOR_RESOL	[31:0]	Horizontal resolution of the current sequence or picture to be displayed. It should be read after decoding sequence header or after decoding a frame (in the case of resolution change).	0

6.3.3.3.3 Required Buffer Number Register (MFC_COMMON_SI_RG_3, R, Address = 0xF170_200C)

MFC_COMMON_SI_RG_3	Bit	Description	Initial State
MIN_NUM_DPB	[31:0]	Required decoded picture buffer number. After decoding sequence header, MFC sets the minimum number of required DPB buffers.	0

NOTE:

1. H.264: MaxDpbFrames+2 (MaxDpbFrames is defined in the standard)
2. H.263: 3
3. Other codecs: 4
4. The number above is determined by the number of reference buffers, one decoding buffer, and one display buffer

6.3.3.3.4 Display Order Luminance Address Register (MFC_COMMON_SI_RG_4, R, Address = 0xF170_2010)

MFC_COMMON_SI_RG_4	Bit	Description	Initial State
DISPLAY_Y_ADR	[31:0]	Display luminance address in display order	0

6.3.3.3.5 Display Order Chrominance Address Register (MFC_COMMON_SI_RG_5, R, Address = 0xF170_2014)

MFC_COMMON_SI_RG_5	Bit	Description	Initial State
DISPLAY_C_ADR	[31:0]	Display chrominance address in display order	0

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6.3.3.3.6 Decoded Frame Size Register (MFC_COMMON_SI_RG_6, R, Address = 0xF170_2018)

MFC_COMMON_SI_RG_6	Bit	Description	Initial State
MFC_DEC_FRM_SIZE	[31:0]	Consumed number of bytes to decode a frame	0

6.3.3.3.7 Display Status Register (MFC_COMMON_SI_RG_7, R, Address = 0xF170_201C)

MFC_COMMON_SI_RG_7	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0
DISPLAY_STATUS	[5:0]	The status of the decoded picture to be displayed. [5:4] : Resolution change 0 = No change 1 = Resolution increased 2 = Resolution decreased [3] : Progressive/interlace 0 = Progressive frame. 1 = Interlace frame [2:0] : Display status 0 = Decoding only (no display) 1 = Decoding and display. 2 = Display only. 3 = DPB is empty and decoding is finished	0

6.3.3.3.8 Frame Type Register (MFC_COMMON_SI_RG_8, R, Address = 0xF170_2020)

MFC_COMMON_SI_RG_8	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
FRAME_TYPE	[2:0]	This register returns a frame type of a decoded frame 0 = Not coded frame (skipped frame) 1 = I frame 2 = P frame 3 = B frame 4 = Others	0

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6.3.3.3.9 Decoding Order Luminance Address Register (MFC_COMMON_SI_RG_9, R, Address = 0xF170_2024)

MFC_COMMON_SI_RG_9	Bit	Description	Initial State
DECODE_Y_ADR	[31:0]	Luminance address in decoding order	0

6.3.3.3.10 Decoding Order Chrominance Address Register (MFC_COMMON_SI_RG_10, R, Address = 0xF170_2028)

MFC_COMMON_SI_RG_10	Bit	Description	Initial State
DECODE_C_ADR	[31:0]	Chrominance address in decoding order	0

6.3.3.3.11 Decoding Status Register (MFC_COMMON_SI_RG_11, R, Address = 0xF170_202C)

MFC_COMMON_SI_RG_11	Bit	Description	Initial State
Reserved	[31:4]	Reserved	0
DECODE_STATUS	[3:0]	The status of the decoded picture. [3] : Progressive/interlace 0 = Progressive frame. 1 = Interlace frame [2:0] : Decoding status 0 = Decoding only (no display) 1 = Decoding and display. 2 = Display only. 3 = DPB is empty and decoding is finished 4 = No decoding and no display (equivalent to DISPLAY_STATUS=2)	0

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6.3.3.3.12 CH External Stream Buffer Address Register (MFC_COMMON_CHx_RG_1, R/W, Address = 0xF170_2044 or 0xF170_2084)

MFC_COMMON_CHx_RG_1	Bit	Description	Initial State
CH_ES_ADDR	[31:0]	Start address of the CPB of the elementary stream to be decoded	0

NOTE: The address should be in Port_A (i.e., the address should be between MC_DRAMBASE_ADDR_A and MC_DRAMBASE_ADDR_A+256MB).

6.3.3.3.13 CH Decoding Unit Size Register (MFC_COMMON_CHx_RG_2, R/W, Address = 0xF170_2048 or 0xF170_2088)

MFC_COMMON_CHx_RG_2	Bit	Description	Initial State
CH_ES_DEC_UNIT_SIZE	[31:0]	Decoding unit size in the CPB	0

6.3.3.3.14 CH Descriptor Buffer Address (MFC_COMMON_CHx_RG_3, R/W, Address = 0xF170_204C or 0xF170_208C)

MFC_COMMON_CHx_RG_3	Bit	Description	Initial State
CH_DESC_ADDR	[1:0]	Channel descriptor buffer address	0

NOTE: The address should be in Port_A (i.e., the address should be between MC_DRAMBASE_ADDR_A and MC_DRAMBASE_ADDR_A+256MB).

6.3.3.3.15 Reserved (MFC_COMMON_CHx_RG_4, W, Address = 0xF170_2050 or 0xF170_2090)

MFC_COMMON_CHx_RG_4	Bit	Description	Initial State
Reserved	[31:0]	Reserved	0

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6.3.3.3.16 Reserved (MFC_COMMON_CHx_RG_5, W, Address = 0xF170_2054 or 0xF170_2094)

MFC_COMMON_CHx_RG_5	Bit	Description	Initial State
Reserved	[31:0]	Reserved	0

6.3.3.3.17 CPB Size Register (MFC_COMMON_CHx_RG_6, R/W, Address = 0xF170_2058 or 0xF170_ 2098)

MFC_COMMON_CHx_RG_6	Bit	Description	Initial State
CPB_SIZE	[31:0]	CPB size register should be set before SEQ_START and FRAME_START. The maximum CPB size is 4MB.	0

NOTE: CPB_SIZE = align(CH_ES_DEC_UNIT_SIZE+64, pow(2KB)) for H.264 and VC1 decoders when DMX is enabled, where pow(2KB)=1KB, 2KB, 4KB, 8KB, …, 4MB.

6.3.3.3.18 Descriptor Buffer Size Register (MFC_COMMON_CHx_RG_7, R/W, Address = 0xF170_205C or 0xF170_209C)

MFC_COMMON_CHx_RG_7	Bit	Description	Initial State
DESC_SIZE	[31:0]	Descriptor buffer size register should be set before SEQ_START and FRAME_START. The maximum descriptor buffer size is 128KB.	0

6.3.3.3.19 Release Buffer Register (MFC_COMMON_CHx_RG_8, R/W, Address = 0xF170_2060 or 0xF170_20A0)

MFC_COMMON_CHx_RG_8	Bit	Description	Initial State
RELEASE_BUFFER	[31:0]	Release buffer register specifies the availability of each DPB. The nth bit specifies the availability of the nth DPB. 1 means free and 0 means busy.	0

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6.3.3.3.20 Auxiliary Host Command Register (MFC_COMMON_CHx_RG_9, R/W, Address = 0xF170_2064 or 0xF170_20A4)

MFC_COMMON_CHx_RG_9	Bit	Description	Initial State
HOST_WR_ADR	[31:0]	The address points to a space of shared memory consisting of multiple commands which host can read/write. The detailed structure of the shared memory is described in chapter 6.4	0

6.3.3.3.21 DPB Configuration Control Register (MFC_COMMON_CHx_RG_10, R/W, Address = 0xF170_2068 or 0xF170_20A8)

MFC_COMMON_CHx_RG_10	Bit	Description	Initial State
SLICE_IF_ENABLE	[31]	Enable slice interface for decoding 0 = Disable 1 = Enable	0
CONFIG_DELAY_ENABLE	[30]	Enable configurable display delay for H.264 decoding 0 = Disable 1 = Enable	0
DISPLAY_DELAY	[29:16]	Number of frames for display delay. MFC is forced to return frames for display even if DPB is not filled. It is valid for H.264 decoder only.	0
DMX_DISABLE	[15]	Host may generate the descriptor information on behalf of MFC demux. This register is valid for H.264 and VC1 decoders only. 0 = Enable demux so that MFC generates the descriptor information. 1 = Disable demux so that host generates the descriptor information.	
DPB_FLUSH	[14]	Flushing DPB to discard all the output buffers in DPB 0 = Normal operation 1 = Flushing DPB	
NUM_DPB	[13:0]	Number of DPB that host prepared for decoding	0

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NOTE:

1. When demux is disabled, host has to fill out the descriptor buffer for each slice/NALU. For VC1, after constructing all the descriptors, one dummy descriptor needs to be created with start code suffix byte 0x82 (ID [7:0] = 0x82) followed by a zero word to indicate the end of descriptors.
2. For both H264 and VC1, after all descriptor entries (including VC1 dummy descriptor entry), zero word is written to descriptor table to indicate end of descriptors. word is written to descriptor table to indicate end of descriptors.

ID[7:0]	Offset[2:0]	Start_addr[20:0]
9'd0		Unit_size[22:0]
32'd0		
32'd0		

ID: start code suffix byte (first byte after start code: NALU header byte for H.264 and 0x82 for VC1)
Offset: (nal start address) & 0x07
Start_addr: ((nal start address) >> 3) << 1
Unit_size: size of NALU

6.3.3.3.22 Command Sequence Number Register (MFC_COMMON_CHx_RG_11, R/W, Address = 0xF170_206C or 0xF170_20AC)

MFC_COMMON_CHx_ RG_11	Bit	Description	Initial State
CMD_SEQ_NUM	[31:0]	Command sequence number from the host. The sequence number is used for in order processing of commands.	0

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6.3.3.4 Encoder Channel and Stream Interface Registers

6.3.3.4.1 Stream Size Register (MFC_COMMON_SI_RG_1, R, Address = 0xF170_2004)

MFC_COMMON_SI_RG_1	Bit	Description	Initial State
ENC_STREAM_SIZE	[31:0]	Encoded stream size in byte count	0

6.3.3.4.2 Encoded Picture Count Register (MFC_COMMON_SI_RG_2, R, Address = 0xF170_2008)

MFC_COMMON_SI_RG_2	Bit	Description	Initial State
ENC_PICTURE_CNT	[31:0]	Encoded picture count. In the interlaced streams, It increments field by field.	0

6.3.3.4.3 Write Pointer Register (MFC_COMMON_SI_RG_3, R, Address = 0xF170_200C)

MFC_COMMON_SI_RG_3	Bit	Description	Initial State
WRITE_POINTER	[31:0]	Stream buffer write pointer. EDFU updates external memory address at the end of encoding a frame.	0

6.3.3.4.4 Slice type Register (MFC_COMMON_SI_RG_4, R/W, Address = 0xF170_2010)

MFC_COMMON_SI_RG_4	Bit	Description	Initial State
ENC_SLICE_TYPE	[31:0]	0 = Not coded frame 1 = I frame 2 = P frame 3 = B frame 4 = Skipped frame 5 = Others	0

6.3.3.4.5 Encoded Y Address Register (MFC_COMMON_SI_RG_5, R/W, Address = 0xF170_2014)

MFC_COMMON_SI_RG_5	Bit	Description	Initial State
ENCODED_Y_ADDR	[31:0]	The address of the encoded luminance picture	0

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6.3.3.4.6 Encoded C Address Register (MFC_COMMON_SI_RG_6, R/W, Address = 0xF170_2018)

MFC_COMMON_SI_RG_6	Bit	Description	Initial State
ENCODED_C_ADDR	[31:0]	The address of the encoded chrominance picture	0

6.3.3.4.7 CH External Stream Buffer Start Address Register (MFC_COMMON_CHx_RG_1, R/W, Address = 0xF170_2044 or 0xF170_2084)

MFC_COMMON_CHx_RG_1	Bit	Description	Initial State
CH_SB_ADDR	[31:0]	Start address of the stream buffer at encoder.	0

NOTE: The address should be in Port_A (i.e., the address should be between MC_DRAMBASE_ADDR_A and MC_DRAMBASE_ADDR_A+256MB).

6.3.3.4.8 Stream Buffer Size Register (MFC_COMMON_CHx_RG_3, R/W, Address = 0xF170_204C or 0xF170_208C)

MFC_COMMON_CHx_RG_3	Bit	Description	Initial State
BUFFER_SIZE	[31:0]	Buffer size of the encoded stream	0

6.3.3.4.9 Current Y Address Register (MFC_COMMON_CHx_RG_4, R/W, Address = 0xF170_2050 or 0xF170_2090)

MFC_COMMON_CHx_RG_4	Bit	Description	Initial State
CURRENT_Y_ADDR	[31:0]	The address of the current luminance picture to encode	0

NOTE: The address should be in Port_B (i.e., the address should be between MC_DRAMBASE_ADDR_B and MC_DRAMBASE_ADDR_B+256MB).
The buffer address should be aligned as follows.
- Tile mode : align(align(x_size, 128) * y_size, 8192)
- Linear mode : align(align(x_size, 16) * y_size, 2048)

6.3.3.4.10 Current C Address Register (MFC_COMMON_CHx_RG_5, R/W, Address = 0xF170_2054 or F170_2094)

MFC_COMMON_CHx_RG_5	Bit	Description	Initial State
CURRENT_C_ADDR	[31:0]	The address of the current chrominance picture to encode	0

NOTE: The address should be in Port_B (i.e., the address should be between MC_DRAMBASE_ADDR_B and MC_DRAMBASE_ADDR_B+256MB).
The buffer address should be aligned as follows.
- Tile mode : align(align(x_size, 128) * y_size/2, 8192)
- Linear mode : align(align(x_size, 16) * y_size/2, 2048)

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6.3.3.4.11 Frame Insertion Control Register (MFC_COMMON_CHx_RG_6, R/W, Address = 0xF170_2058 or 0xF170_2098)

MFC_COMMON_CHx_RG_6	Bit	Description	Initial State
RESERVED	[31:0]	Reserved	0
NOT_CODED	[1]	Current frame must be encoded into a not coded frame	0
I_FRAME	[0]	Current frame must be encoded into an I frame. It will be effective at the next anchor frame.	0

6.3.3.4.12 Auxiliary Host Command Register (MFC_COMMON_CHx_RG_9, R/W, Address = 0xF170_2064 or 0xF170_20A4)

MFC_COMMON_CHx_RG_9	Bit	Description	Initial State
HOST_WR_ADR	[31:0]	The address points to a space of shared memory consisting of multiple commands which host can read/write. The detailed structure of the shared memory is described in chapter 6.4	0

6.3.3.4.13 Encoder Input Buffer Flush Register (MFC_COMMON_CHx_RG_10, R/W, Address = 0xF170_2068 or 0xF170_20A8)

MFC_COMMON_CHx_RG_10	Bit	Description	Initial State
RESERVED	[31:15]	Reserved	0
INPUT_BUFFER_FLUSH	[14]	Flushing input buffer to discard all frame in the input buffer. 0 = Normal operation 1 = Flushing input buffer	0
RESERVED	[13:0]	Reserved	0

6.3.3.4.14 Command Sequence Number Register (MFC_COMMON_CHx_RG_11, R/W, Address = 0xF170_206C or 0xF170_20AC)

MFC_COMMON_CHx_RG_9	Bit	Description	Initial State
CMD_SEQ_NUM	[31:0]	Command sequence number from the host. The sequence number is used for in order processing of commands.	0

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6.3.4 ENCODING REGISTERS

6.3.4.1 Common Encoder Register

6.3.4.1.1 Picture Type Control Register (ENC_PIC_TYPE_CTRL, R/W, Address = 0xF170_C504)

ENC_PIC_TYPE_CTRL	Bit	Description	Initial State
Reserved	[31:19]	Reserved	0
ENC_PIC_TYPE_ENABLE	[18]	0 = Disable ENC_PIC_TYPE_CTRL 1 = Enable ENC_PIC_TYPE_CTRL[17:0] for picture type setting	0
B_FRM_CTRL	[17:16]	0 = The number of B frames is zero 1 = The number of B frames is one 2 = The number of B frames is two 3 = Reserved	0
I_FRM_CTRL	[15:0]	0 = All P frames 1 = All I frames 2 = I – P – I – P 3 = I – P – P – I N = (N-1) P frames between two I frames	0

6.3.4.1.2 B-Picture Recon Picture Writing Control Register (ENC_B_RECON_WRITE_ON, R/W, Address = 0xF170_C508)

ENC_B_RECON_WRITE_ON	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
B_RECON_ON	[0]	This register is used for debugging. By default, it is set to zero. If it is set, it is required to allocate the required memory. 0 = Disable recon data write at B-frame 1 = Enable recon data write at B-frame	0

NOTE: When B_RECON_ON is enabled, host has to allocate B_FRAME_RECON_LUMA_ADDR (0x062C) and B_FRAME_RECON_CHROMA_ADDR (0x0630). The size should be as follows:
- Sizeof(B_FRAME_RECON_LUMA_ADDR) = align(align(x_size, 128) * align(y_size, 32), 8192)
- Sizeof(B_FRAME_RECON_CHROMA_ADDR) = align(align(x_size, 128) * align(y_size/2, 32), 8192)

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6.3.4.1.3 Multi-slice Control Register (ENC_MSLICE_CTRL, R/W, Address = 0xF170_C50C)

ENC_MSLICE_CTRL	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
MSLICE_MODE	[2:1]	0 = Multi slicing is done by MB count 1 = Multi slicing is done by byte count	0
MSLICE_ENA	[0]	0 = One slice per frame 1 = Enable multi slice or resync marker	0

6.3.4.1.4 Macroblock Number of Multi-slice Register (ENC_MSLICE_MB, R/W, Address = 0xF170_C510)

ENC_MSLICE_MB	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
MSLICE_MB	[15:0]	The number of macroblocks in one slice. Valid if MSLICE_MODE=0 and MSLICE_ENA=1.	0

6.3.4.1.5 Size of Multi-slice Register (ENC_MSLICE_BYTE, R/W, Address = 0xF170_C514)

ENC_MSLICE_BIT	Bit	Description	Initial State
MSLICE_BIT	[31:0]	The number of bit count in one slice. Valid if MSLICE_MODE=1 and MSLICE_ENA=1.	0

NOTE: The minimum size of MSLICE_BIT is 1900bits

6.3.4.1.6 Cyclic Intra Refresh Register (ENC_CIR_CTRL, R/W, Address = 0xF170_C518)

ENC_CIR_CTRL	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
CIR_NUM	[15:0]	Number of intra refresh macroblocks	0

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6.3.4.1.7 Memory Structure Setting Register of Current Frame (ENC_MAP_FOR_CUR, R/W, Address = 0xF170_C51C)

ENC_MAP_FOR_CUR	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0
ENC_MAP_FOR_CUR	[1:0]	Memory structure of the current frame 0 = Linear mode 3 = 64x32 tiled mode	0

6.3.4.1.8 Padding Value Control Register (ENC_PADDING_CTRL, R/W, Address = 0xF170_C520)

ENC_PADDING_CTRL	Bit	Description	Initial State
PAD_CTRL_ON	[31]	0 = Use boundary pixel for current image padding in case that its image size is not a multiple of 16 1 = Use ENC_PADDING_CTRL[23:0] for current image padding	0
Reserved	[30:24]	Reserved	0
CR_PAD_VAL	[23:16]	Value for original CR image's padding when PAD_CTRL_ON is 1.	0
CB_PAD_VAL	[15:8]	Value for original CB image's padding when PAD_CTRL_ON is 1.	0
LUMA_PAD_VAL	[7:0]	Value for original Y image's padding when PAD_CTRL_ON is 1.	0

6.3.4.1.9 Encoder Intra Mode Bias Register (ENC_COMMON_INTRA_BIAS, R/W, Address = 0xF170_C588)

ENC_INT_MASK	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
ENC_COMMON_INTRA_BIAS	[15:0]	The register is used in favor of the intra mode in the weighted macroblock mode decision. Mode decision will be done by comparing 1) inter_cost + ENC_COMMON_INTRA_BIAS and 2) intra_cost. If inter_cost is zero, the mode is always determined to inter macroblock. To disable this option, set ENC_COMMON_INTRA_BIAS to zero.	0

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6.3.4.1.10 Encoder Bi-directional Mode Bias Register (ENC_COMMON_BI_DIRECT_BIAS, R/W, Address = 0xF170_C58C)

ENC_INT_MASK	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
ENC_COMMON_ BI_DIRECT_BIAS	[15:0]	The register is used against the bi-directional mode in the weighted macroblock mode decision. Mode decision will be done by comparing 1) uni_direction_cost and 2) bi_direction_cost + ENC_COMMON_BI_DIRECT_BIAS. If the macroblock type is INTRA, this register is of no effect. To disable this option, set ENC_COMMON_BI_DIRECT_BIAS to zero. This register is effective in MPEG4 encoding only.	0

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6.3.4.2 Rate Control Register

6.3.4.2.1 Rate Control Configuration Register (RC_CONFIG, R/W, Address = 0xF170_C5A0)

RC_CONFIG	Bit	Description	Initial State
Reserved	[31:10]	Reserved	0
FR_RC_EN	[9]	Frame level rate control enable 0 = Disable frame level rate control 1 = Enable frame level rate control	0
MB_RC_EN	[8]	Macroblock level rate control enable. Valid only for H.264 0 = Disable MB level rate control 1 = Enable MB level rate control	0
Reserved	[7:6]	Reserved	0
FRAME_QP	[5:0]	Frame QP (quantization parameter) FRAME_QP is used for the first macroblock QP in a frame. This value should be set in the range of MIN_QP to MAX_QP in RC_QBOUND. The QP of the next macroblocks can be changed as per the value of FR_RC_EN and MB_RC_EN. The interpretation of FRAME_QP is varying as per RC_CONFIG[9:8] as follows. <RC_CONFIG[9:8]> 2'b00: Constant QP is applied to all macroblocks. FRAME_QP is used for I frame. P_FRAME_QP and B_FRAME_QP are used for P and B frames. 2'b01: The QP of the next macroblocks can vary with macroblock adaptive scaling. But it does not take into account the size of generated bits. 2'b10: The QP of the next macroblocks can be changed by the difference between the numbers of target bit and generated bit during the encoding a picture. But macroblock adaptive scaling is not applied. 2'b11: The QP of the next macroblocks can be changed by the difference between the numbers of target bit and generated bit during the encoding a picture. It also can vary with macroblock adaptive scaling.	0

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6.3.4.2.2 RC Frame Rate Register (RC_FRAME_RATE, R/W, Address = 0xF170D0D0)

RC_FRAME_RATE	Bit	Description	Initial State
FRAME_RATE	[31:0]	Frames per second in 1000x scale (e.g., 7500 stands for 7.5 frames/sec). '0' is forbidden. Valid only when frame level RC is enabled.	0

6.3.4.2.3 RC Bit Rate Register (RC_BIT_RATE, R/W, Address = 0xF170_C5A8)

RC_BIT_RATE	Bit	Description	Initial State
BIT_RATE	[31:0]	Bits per second. '0' is forbidden. Valid only when Frame level RC is enabled.	0

6.3.4.2.4 RC Quantization Parameter Boundary Register (RC_QBOUND, R/W, Address = 0xF170_C5AC)

RC_QBOUND	Bit	Description	Initial State
Reserved	[31:14]	Reserved	0
MAX_QP	[13:8]	Maximum quantization parameter. The range is given as follows. - H.264: 0~51 - MPEG4, H.263: 1~31	0
Reserved	[7:6]	Reserved	0
MIN_QP	[5:0]	Minimum quantization parameter. The range is given as follows. - H.264: 0~51 - MPEG4, H.263: 1~31	0

NOTE: MAX_QP must be greater than or equal to MIN_QP.

6.3.4.2.5 Reaction Coefficient Register (RC_RPARA, R/W, Address = 0xF170_C5B0)

RC_RPARA	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
REACT_PARA	[15:0]	Rate control reaction coefficient. '0' is forbidden.	0

NOTE:

1. Valid only when the frame level RC is enabled.
2. For tight CBR, this field must be small (ex. 2 ~ 10).
   For VBR, this field must be large (ex. 100 ~ 1000).
3. It is not recommended to use the greater number than FRAME_RATE * (10^9 / BIT_RATE).

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6.3.4.2.6 Macroblock Level Rate Control Register (RC_MB_CTRL, R/W, Address = 0xF170_C5B4)

RC_MB_CTRL	Bit	Description	Initial State
Reserved	[31: 4]	Reserved	0
DARK_DISABLE	[3]	Disable dark region adaptive feature. 0 = Enable dark region adaptive feature 1 = Disable dark region adaptive feature QP of dark MB may not be smaller than frame QP although it is smooth, static or it has small activity.	0
SMOOTH_DISABLE	[2]	Disable smooth region adaptive feature. 0 = Enable smooth region adaptive feature. 1 = Disable smooth region adaptive feature. QP of smooth MB may be smaller than frame QP.	0
STATIC_DISABLE	[1]	Disable static region adaptive feature. 0 = Enable static region adaptive feature. 1 = Disable static region adaptive feature. QP of static MB may be smaller than frame QP.	0
ACT_DISABLE	[0]	Disable MB activity adaptive feature. 0 = Enable MB activity adaptive feature. 1 = Disable MB activity adaptive feature. QP of MB that has small activity may be smaller than frame QP and QP of MB that has large activity may be larger than frame QP	0

NOTE: Valid only when H.264 and macroblock level RC is enabled.

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6.3.4.3 H.264 Encoder Register

6.3.4.3.1 H.264 Entropy Register (H264_ENC_ENTRP_MODE, R/W, Address = 0xF170_D004)

H264_ENC_ENTRP_MODE	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
H264_ENC_ENTRP_MODE	[0]	0 = CAVLC 1 = CABAC	0

6.3.4.3.2 H.264 Number of Reference Register (H264_ENC_NUM_OF_REF, R/W, Address = 0xF170_D010)

H264_ENC_NUM_OF_REF	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
H264_ENC_P_NUM_OF_REF	[6:5]	The number reference pictures of P-picture. 1 = 1 reference frame 2 = 2 reference frame	0
H264_ENC_NUM_OF_REF	[4:0]	The maximum number of reference pictures. 1 = 1 reference frame 2 = 2 reference frame	0

6.3.4.3.3 H.264 8X8 Transform Enable Flag Register (H264_ENC_TRANS_8X8_FLAG, R/W, Address = 0xF170_D034)

H264_ENC_TRANS_8X8_FLAG	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
ENC_TRANS_8X8_FLAG	[0]	0 = Disable 1 = Enable	0

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6.3.4.4 MPEG4 Encoder Register

6.3.4.4.1 MPEG4 Quarter Pixel Interpolation Register (MPEG4_ENC_QUART_PXL, R/W, Address = 0xF170_E008)

MPEG4_ENC_QUART_PXL	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
MPEG4_QUART_PXL	[0]	0 = Quarter pixel search disable 1 = Quarter pixel search enable	0

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6.4 SHARED MEMORY INTERFACE

As per the growth of the diverse requirements for the codec features and additional enhancements of the MFC firmware, MFC provides the shared memory interface to exchange information with the host. Host is able to get returned parameters or set parameter values through the shared memory. Since the parameters are exchanged through the external memory, there is no limitation of the number of fields. Readers may consider it as a register group but the physical memory is allocated in the external memory.

This section describes the shared memory interface, such as shared memory allocation and the shared memory structure consisting of multiple fields.

6.4.1 HOST INTERFACE

Host has to allocate the shared memory and informs MFC of the buffer pointer through the HOST_WR_ADR register. It is recommended to allocate the shared memory before the sequence header parsing through SEQ_START. Since the number of fields in the shared memory is fixed in 0, host is required to allocate a buffer in the external memory to accommodate them.

Once the shared memory has been allocated, host and MFC are able to exchange information through the shared memory. Host can read and write each field in the shared memory at the byte offset defined in 0.

Following is a pseudo code to initialize the shared memory.

```
// shared mem allocation. Should be done before SEQ_START
shared_mem_ptr = (int *) malloc(SHARED_MEM_SIZE);
host_write_word(HOST_WR_ADR, shared_mem_ptr);
```

Following is a pseudo code to read and write the frame tags.

```
// write frame_tag
host_write_word(shared_mem_ptr+ADR_SET_FRAE_TAG, frame_tag);

// read frame_tag
get_frame_tag = host_read_word(shared_mem_ptr+ADR_GET_FRAME_TAG_TOP);
```

Note that, at the beginning of a stream encoding/decoding, host must initialize all the fields in the shared memory corresponding to that stream to avoid any undefined behaviors.

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6.4.2 SHARED MEMORY STRUCTURE

6.4.2.1 Decoding Control

6.4.2.1.1 Extended Decode Status (EXTENDED_DECODE_STATUS, R, Offset = 0x0000)

EXTENDED_DECODE_ STATUS	Bit	Description	Initial State
Reserved	[31:1]	Reserved	Undef

6.4.2.1.2 Set Frame Tag (SET_FRAME_TAG, W, Offset = 0x0004)

SET_FRAME_TAG	Bit	Description	Initial State
SET_FRAME_TAG	[31:0]	Host sets to set a unique frame ID (e.g., application specific timestamp) for this output buffer.	Undef

6.4.2.1.3 Get Frame Tag Top (GET_FRAME_TAG_TOP, R, Offset = 0x0008)

GET_FRAME_TAG_ TOP	Bit	Description	Initial State
GET_FRAME_TAG_ TOP	[31:0]	MFC sets a frame tag for the output frame corresponding to the one set by host using SET_FRAME_TAG for this frame. Host reads a unique ID on display. This tag returns an application specific ID for the progressive frame. For an interlaced picture, this tag returns an application specific ID for the top field. Note that the value of (-1) indicates that there is no displayable picture.	Undef

6.4.2.1.4 Get Frame Tag Bottom (GET_FRAME_TAG_BOTTOM, R, Offset = 0x000C)

GET_FRAME_TAG_ BOTTOM	Bit	Description	Initial State
GET_FRAME_TAG_ BOTTOM	[31:0]	MFC sets a frame tag for the output frame corresponding to the one set by host using SET_FRAME_TAG for this frame. Host reads the ID for the bottom field. This tag is valid for the interlaced picture only. Note that the value of (-1) indicates that there is no displayable picture or a progressive picture.	Undef

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6.4.2.1.5 Picture Time for Top Field (PIC_TIME_TOP, R, Offset = 0x0010)

PIC_TIME_TOP	Bit	Description	Initial State
PIC_TIME_TOP	[31:0]	Presentation time of an output frame. It is determined by the header information in the bitstream. For an interlaced picture, it returns a presentation time for the top field. The time unit is in ms. However if the standard does not provide presentation time (e.g. H.263 and H.264), it returns a sequence number.	Undef

NOTE: Specific interpretation for each standard is as follows.

1. MPEG2, H.263: Temporal reference
2. MPEG4: VOP time
3. H.264: POC
4. VC1 simple/main profile: zero
5. VC1 advanced profile: Temporal reference frame counter. If it is not present, zero is written.

6.4.2.1.6 Picture Time for Bottom Field (PIC_TIME_BOTTOM, R, Offset = 0x0014)

PIC_TIME_BOTTOM	Bit	Description	Initial State
PIC_TIME_BOTTOM	[31:0]	Presentation time of the bottom field. It is valid for the interlaced picture only. The specific interpretation for each standard is the same as PIC_TIME_TOP.	Undef

6.4.2.1.7 Start Byte Number (START_BYTE_NUM, R/W, Offset = 0x0018)

START_BYTE_NUM	Bit	Description	Initial State
START_BYTE_NUM	[31:0]	An offset of the stream when it is not aligned	Undef

6.4.2.1.8 Cropping Information One (CROP_INFO1, R, Offset = 0x0020)

CROP_INFO1	Bit	Description	Initial State
CROP_RIGHT_OFFSET	[31:16]	Cropping right offset	Undef
CROP_LEFT_OFFSET	[15:0]	Cropping left offset	Undef

6.4.2.1.9 Cropping Information Two (CROP_INFO2, R, Offset = 0x0024)

CROP_INFO2	Bit	Description	Initial State
CROP_BOTTOM_OFFSET	[31:16]	Cropping bottom offset	Undef
CROP_TOP_OFFSET	[15:0]	Cropping top offset	Undef

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6.4.2.1.10 Profile info for displayed picture (DISP_PIC_PROFILE, R, Offset = 0x007C)

DISP_PIC_PROFILE	Bit	Description	Initial State
Reserved	[31:16]	Reserved	Undef
DISP_PIC_LEVEL	[15:8]	Level in MPEG4 and H.264. In H.264, 31 stands for level 3.1 and 9 stands for level 1b. In MPEG4, 3 stands for level 3 and 7 stands for level 3b. In VC1, simple and main profile define. 0 = Low 2 = Medium 4 = High Advanced profile defines : 0 = Level 0 1 = Level 1 2 = Level 2 3 = Level 3 4 = Level 4 In MPEG2, levels are defined as follows: 4 = High 6 = High 1440 8 = Main 10 = Low	Undef
Reserved	[7:5]	Reserved	Undef
DISP_PIC_PROFILE	[4:0]	MPEG4 : 0 = SP 1 = ASP H.264 : 0 = Baseline 1 = Main 2 = High H.263 : 0 = Always (bitstream does not carry profile info) VC1 : 0 = Simple 1 = Main 2 = Advanced MPEG2: 4 = Main 5 = Simple	Undef

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6.4.2.1.11 H.264 Decoder POC_TYPE (H264_POC_TYPE, R, Offset = 0x00B8)

H264_POC_TYPE	Bit	Description	Initial State
H264_POC_TYPE	[31:0]	POC_TYPE of H.264 decoder. If POC_TYPE is 0 or 1, initial display delay is determined by MaxDpbSize in the standard. If POC_TYPE is 2, there is no initial display delay	Undef

NOTE: The actual display delay can be different because of the following reasons.

1. If there are multiple SPSes, MFC returns the POC_TYPE of the first SPS
   If the first frame uses a different SPS, it will result in different initial display delay.
2. If the second IDR frame appears within MaxDpbSize, MFC has to start the DPB buffer flushing which will cause a reduced initial display delay.

6.4.2.1.12 Displayed Picture Frame Type (DISP_PIC_FRAME_TYPE, R, Offset = 0x00C0)

DISP_PIC_FRAME_TYPE	Bit	Description	Initial State
DISP_PIC_FRAME_TYPE	[31:0]	Frame type of a displayed picture 0 = Not coded frame 1 = I frame 2 = P frame 3 = B frame	Undef

6.4.2.1.13 Available Luma DPB Address (FREE_LUMA_DPB, R, Offset = 0x00C4)

FREE_LUMA_DPB	Bit	Description	Initial State
FREE_LUMA_DPB	[31:0]	Free DPB address to which host can copy a DPB. The free DPB can be used to handle not coded frames in VC1 and MPEG4 decoders.	Undef

6.4.2.1.14 Aspect Ratio Information (ASPECT_RATIO_INFO, R, Offset = 0x00C8)

ASPECT_RATIO_INFO	Bit	Description	Initial State
Reserved	[31:4]	Reserved	Undef
ASPECT_RATIO_INFO	[3:0]	1 = Square (1:1) 2 = 625 type for 4:3 picture (12:11) 3 = 525 type for 4:3 picture (10:11) 4 = 625 type stretched for 16:9 picture (16:11) 5 = 525 type stretched for 16:9 picture (40:33) 15 = Extended PAR	Undef

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6.4.2.1.15 Extended Pixel Aspect Ratio (EXTENDED_PAR, R, Offset = 0x00CC)

EXTENDED_PAR	Bit	Description	Initial State
PAR_WIDTH	[31:16]	The value indicates the horizontal size of the sample aspect ratio. It is valid only if ASPECT_RATIO_INFO=15.	Undef
PAR_HEIGHT	[15:0]	The value indicates the vertical size of the sample aspect ratio. It is valid only if ASPECT_RATIO_INFO=15.	Undef

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6.4.2.2 Encoding Control

6.4.2.2.1 Extended Encoder Control (EXT_ENC_CONTROL, W, Offset = 0x0028)

EXT_ENC_CONTROL	Bit	Description	Initial State
VBV_BUFFER_SIZE	[31:16]	VBV buffer size defined by host. The unit is in kilo bytes (i.e., actual buffer size = VBV_BUFFER_SIZE * 1024 bytes). Valid only when FRAME_SKIP_ENABLE=2.	Undef
ASPECT_RATIO_VUI_ENABLE	[15]	0 = Aspect ratio VUI is disabled in H.264 encoding 1 = Aspect ratio VUI is enabled in H.264 encoding	Undef
Reserved	[14:5]	Reserved	Undef
HIERARCHICAL_P_ENABLE	[4]	0 = Hierarchical P frame disable 1 = Hierarchical P frame enable	
SEQ_HEADER_CONTROL	[3]	0 = Sequence header is not generated on the first FRAME_START 1 = Sequence header is generated on both SEQ_START and the first FRAME_START	
FRAME_SKIP_ENABLE	[2:1]	0 = Frame skip is disabled. The chance of the rate overshoot will be increased when the generate bitrate is high. 1 = Frame skip is enabled using maximum buffer size defined by level. 2 = Frame skip is enabled using VBV_BUFFER_SIZE defined by HOST	Undef
HEC_ENABLE	[0]	0 = Header extension code (HEC) is disabled in the MPEG4 encoding 1 = HEC is enabled	Undef

6.4.2.2.2 Encoding Parameter Change (ENC_PARAM_CHANGE, W, Offset = 0x002C)

ENC_PARAM_CHANGE	Bit	Description	Initial State
-	[31:3]	Reserved	Undef
RC_BIT_RATE_ CHANGE	[2]	0 = Normal operation 1 = Target bitrate is changed	Undef
RC_FRAME_RATE_ CHANGE	[1]	0 = Normal operation 1 = Target frame rate is changed	Undef
I_PERIOD_CHANGE	[0]	0 = Normal operation 1 = GOP size is changed	Undef

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6.4.2.2.3 VOP Timing (VOP_TIMING, W, Offset = 0x0030)

VOP_TIMING	Bit	Description	Initial State
VOP_TIMING_ENABLE	[31]	Enable computing vop_time_increment and modulo_time_base in MPEG4	Undef
VOP_TIME_RESOLUTION	[30:16]	Used to compute vop_time_increment and modulo_time_base in MPEG4	Undef
FRAME_DELTA	[15:0]	Used to compute vop_time_increment and modulo_time_base in MPEG4	Undef

6.4.2.2.4 Header Extension Code Period (HEC_PERIOD, W, Offset = 0x0034)

HEC_PERIOD	Bit	Description	Initial State
HEC_PERIOD	[31:0]	Insert a header extenstion code every HEC_PERIOD number of packets in the MPEG4 encoding	Undef

6.4.2.2.5 P Frame QP and B Frame QP (P_B_FRAME_QP, W, Offset = 0x0070)

P_B_FRAME_QP	Bit	Description	Initial State
Reserved	[31:12]	Reserved	Undef
B_FRAME_QP	[11:6]	The value is used for the B frame QP	Undef
P_FRAME_QP	[5:0]	The value is used for the P frame QP	Undef

NOTE: The frame QPs are valid only if FR_RC_EN=0 and MB_RC_EN=0

6.4.2.2.6 Aspect Ratio IDC (ASPECT_RATIO_IDC, W, Offset = 0x0074)

ASPECT_RATIO_IDC	Bit	Description	Initial State
Reserved	[31:8]	Reserved	Undef
ASPECT_RATIO_IDC	[7:0]	VUI aspect ratio IDC for H.264 encoding. The value is defined in VUI Table E-1 in the standard. It is valid only if ASPECT_RATIO_VUI_ENABLE=1.	Undef

6.4.2.2.7 Extended SAR (EXTENDED_SAR, W, Offset = 0x0078)

EXTENDED_SAR	Bit	Description	Initial State
SAR_WIDTH	[31:16]	The value indicates the horizontal size of the sample aspect ratio. It is valid only if ASPECT_RATIO_VUI_ENABLE=1.	Undef
SAR_HEIGHT	[15:0]	The value indicates the vertical size of the sample aspect ratio. It is valid only if ASPECT_RATIO_VUI_ENABLE=1.	Undef

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6.4.2.2.8 New RC Bit Rate (NEW_RC_BIT_RATE, W, Offset = 0x0090)

NEW_RC_BIT_RATE	Bit	Description	Initial State
NEW_RC_BIT_RATE	[31:0]	Updated target bit rate at encoder which has the same format as RC_BIT_RATE (0xC5A8). It is valid only if RC_BIT_RATE_CHANGE=1.	Undef

6.4.2.2.9 New RC Frame Rate (NEW_RC_FRAME_RATE, W, Offset = 0x0094)

NEW_RC_FRAME_RATE	Bit	Description	Initial State
NEW_RC_FRAME_RATE	[31:0]	Updated target frame rate at encoder which has the same format as RC_FRAME_RATE (frames per second in 1000x scale). It is valid only if RC_FRAME_RATE_CHANGE=1.	Undef

6.4.2.2.10 New Intra Period (NEW_I_PERIOD, W, Offset = 0x0098)

NEW_I_PERIOD	Bit	Description	Initial State
NEW_I_PERIOD	[31:0]	Updated intra period at encoder which has the same format as I_FRM_CTRL (0xC504). It is valid only if I_PERIOD_CHANGE=1. 0 = All P frames 1 = All I frames 2 = I – P – I – P 3 = I – P – P – I N = (N-1) P frames between two I frames	Undef

6.4.2.2.11 H264 Intra Period (H264_I_PERIOD, W, Offset = 0x009C)

H264_I_PERIOD	Bit	Description	Initial State
Reserved	[31:17]	Reserved	Undef
H264_I_PERIOD_ENABLE	[16]	Enable I picture (not IDR) for H.264 encoder. This option results in open GOP.	Undef
H264_I_PERIOD_CONFIG	[15:0]	It is valid only if H264_I_PERIOD_ENABLE=1. 0 = All P frames 1 = All I frames 2 = I – P – I – P 3 = I – P – P – I N = (N-1) P frames between two I frames	Undef

NOTE: I and IDR are used differently in H.264. IDR is used for closed GOP, and I is used for open GOP. The interpretation of the MFC registers is as follows.
[H..264 encoding]
- IDR: I_FRAME, I_FRM_CTRL, NEW_I_PERIOD
- I: H264_I_PERIOD
[MPEG4 encoding]

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- I: I_FRAME, I_FRM_CTRL, NEW_I_PERIOD
- There is no concept of IDR in MPEG4

6.4.2.2.12 Rate Control Configuration (RC_CONTROL_CONFIG, W, Offset = 0x00A0)

RC_CONTROL_CONFIG	Bit	Description	Initial State
Reserved	[31:1]	Reserved	Undef
RC_FIXED_TARGET_BIT	[0]	0: Disable 1: Enable	Undef

6.4.2.2.13 Input Structure Address for Batch Encoding (BATCH_INPUT_ ADDR, W, Offset = 0x00A4)

BATCH_INPUT_ ADDR	Bit	Description	Initial State
BATCH_INPUT_ ADDR	[31:0]	Start address of the input structure for batch encoding	Undef

6.4.2.2.14 Output Structure Address for Batch Encoding (BATCH_OUTPUT_ ADDR, W, Offset = 0x00A8)

BATCH_OUTPUT_ ADDR	Bit	Description	Initial State
BATCH_OUTPUT_ ADDR	[31:0]	Start address of the output structure for batch encoding	Undef

6.4.2.2.15 Output Structure Size for Batch Encoding (BATCH_OUTPUT_SIZE, W, Offset = 0x00AC)

BATCH_OUTPUT_SIZE	Bit	Description	Initial State
BATCH_OUTPUT_SIZE	[31:0]	Size of the output structure for batch encoding	Undef

6.4.2.2.16 Hierarchical P frame QP (HIERARCHICAL_P_QP, W, Offset = 0x00E0)

HIERARCHICAL_P_QP	Bit	Description	Initial State
Reserved	[31:18]	Reserved	Undef
T3_FRAME_QP	[17:12]	QP for T3 frames	Undef
T2_FRAME_QP	[11:6]	QP for T2 frames	Undef
T0_FRAME_QP	[5:0]	QP for T0 frames	Undef

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6.4.2.3 Common Control

6.4.2.3.1 Allocated Luma DPB Size Register (ALLOCATED_LUMA_DPB_SIZE, W, Offset = 0x0064)

ALLOCATED_LUMA_DPB_SIZE	Bit	Description	Initial State
ALLOCATED_LUMA_DPB_SIZE	[31:0]	Size of luma DPB that host allocated for decoding. The allocated DPB size has to take into account the tile mode format.	Undef

6.4.2.3.2 Allocated Chroma DPB Size Register (ALLOCATED_ CHROMA _DPB_SIZE, W, Offset = 0x0068)

ALLOCATED_CHROMA_DPB_SIZE	Bit	Description	Initial State
ALLOCATED_CHROMA _DPB_SIZE	[31:0]	Size of chroma DPB that host allocated for decoding. The allocated DPB size has to take into account the tile mode format.	Undef

6.4.2.3.3 Allocated Motion Vector Size Register (ALLOCATED_MV_SIZE, W, Offset = 0x006C)

ALLOCATED_MV_SIZE	Bit	Description	Initial State
ALLOCATED_MV_SIZE	[31:0]	Size of motion vector buffers that host allocated for decoding. The allocated DPB size has to take into account the tile mode format. This is valid for H.264 only.	Undef

6.4.2.3.4 Flush Command Type Register (FLUSH_CMD_TYPE, R, Offset = 0x0080)

FLUSH_CMD_TYPE	Bit	Description	Initial State
FLUSH_CMD_TYPE	[31:0]	0 = Encoder 1 = Decoder	Undef

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6.4.2.3.5 Flush Command Input Buffer 1 Register (FLUSH_CMD_INBUF1, R, Offset = 0x0084)

FLUSH_CMD_INBUF1	Bit	Description	Initial State
FLUSH_CMD_INBUF1	[31:0]	11bit right-shifted address of an input buffer pointer Encoder: Current Y address Decoder: CPB buffer address	Undef

6.4.2.3.6 Flush Command Input Buffer 2 Register (FLUSH_CMD_INBUF2, R, Offset = 0x0088)

FLUSH_CMD_INBUF2	Bit	Description	Initial State
FLUSH_CMD_INBUF2	[31:0]	11bit right-shifted address of an input buffer pointer Encoder: Current C address Decoder: Descriptor buffer address	Undef

6.4.2.3.7 Flush Command Output Buffer Register (FLUSH_CMD_OUTBUF, R, Offset = 0x008C)

FLUSH_CMD_OUTBUF	Bit	Description	Initial State
FLUSH_CMD_OUTBUF	[31:0]	11bit right-shifted address of an output buffer pointer Encoder: Stream buffer start address Decoder: N/A	Undef

6.4.2.3.8 Minimum Luma DPB Size Register (MIN_LUMA_DPB_SIZE, R, Offset = 0x00B0)

MIN_LUMA_DPB_SIZE	Bit	Description	Initial State
MIN_LUMA_DPB_SIZE	[31:0]	The minimum size (in bytes) of luma DPB that host should allocate for decoding. The size takes into account the tile mode format.	Undef

6.4.2.3.9 Minimum Chroma DPB Size Register (MIN_CHROMA_DPB_SIZE, R, Offset = 0x00BC)

MIN_CHROMA_DPB_SIZE	Bit	Description	Initial State
MIN_CHROMA_DPB_SIZE	[31:0]	The minimum size (in bytes) of chroma DPB that host should allocate for decoding. The size takes into account the tile mode format.	Undef

6.4.2.3.10 Debug History Input Register (DBG_HISTORY_INPUT0, W, Offset = 0x00D0)

DBG_HISTORY_INPUT0	Bit	Description	Initial State
ALLOCATED_MEM_SIZE	[31:16]	Size of allocated memory for the stage counter history dump.	Undef
Reserved	[15:1]	Reserved	Undef
ENABLE_DEBUG_HISTORY	[0]	0: Disable debug history 1: Enable debug history	Undef

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6.4.2.3.11 Debug History Input Register (DBG_HISTORY_INPUT1, W, Offset = 0x00D4)

DBG_HISTORY_INPUT1	Bit	Description	Initial State
ALLOCATED_MEM_ADDR	[31:0]	Address of allocated memory for the stage counter history dump.	Undef

6.4.2.3.12 Debug History Output Register (DBG_HISTORY_OUTPUT, R, Offset = 0x00D8)

DBG_HISTORY_OUTPUT	Bit	Description	Initial State
DBG_HISTORY_SIZE	[31:0]	Number of bytes which MFC dumps as the stage counter history.	Undef

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6.4.2.4 Metadata Control

6.4.2.4.1 Metadata Enable (METADATA_ENABLE, W, Offset = 0x0038)

METADATA_ENABLE	Bit	Description	Initial State
Reserved	[31:8]	Reserved	Undef
NUM_CONCEALED_MB_ENABLE	[7]	0: Disable number of concealed macroblock info 1: Enable number of concealed macroblock info	
EXTRADATA_ENABLE	[6]	0 = Disable extra metadata 1 = Enable extra metadata	Undef
ENC_SLICE_SIZE_ENABLE	[5]	0 = Disable slice size info 1 = Enable slice size info	Undef
VUI_ENABLE	[4]	0 = Disable VUI info 1 = Enable VUI info	Undef
SEI_NAL_ENABLE	[3]	0 = Disable SEI NAL info 1 = Enable SEI NAL info	Undef
VC1_PARAM_ENABLE	[2]	0 = Disable VC1 parameter store 1 = Enable VC1 parameter store	Undef
CONCEALED_MB_ENABLE	[1]	0 = Disable concealed macroblock info 1 = Enable concealed macroblock info	Undef
QP_ENABLE	[0]	0 = Disable QP info 1 = Enable QP info	Undef

NOTE: When QP_ENABLE=1, MFC sets MFC_QP_OUT_EN and MFC_QP_OFFSET internally
METADATA_ENABLE and EXT_METADATA_START_ADDR should be set on SEQ_START

6.4.2.4.2 Metadata Status (METADATA_STATUS, R, Offset = 0x003C)

METADATA_STATUS	Bit	Description	Initial State
Reserved	[31:1]	Reserved	Undef
METADATA_STATUS	[0]	0 = Metadata does not exist 1 = Metadata exists	Undef

6.4.2.4.3 Metadata Display Index (METADATA_DISPLAY_INDEX, R, Offset = 0x0040)

METADATA_DISPLAY_INDEX	Bit	Description	Initial State
METADATA_DISPLAY_INDEX	[31:0]	When concealed macroblock or QP is enabled in the metadata info, it has to return the information of the displayed frame, not the decoded frame. It returns the index of metadata in the shared memory.	Undef

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6.4.2.4.4 Metadata Start Address (EXT_METADATA_START_ADDR, W, Offset = 0x0044)

EXT_METADATA_START_ADDR	Bit	Description	Initial State
EXT_METADATA_START_ADDR	[31:0]	The start address of the metadata memory to configure the QP, concealed macroblock number, VC1 parameters, SEI, VUI, and slice size information	Undef

NOTE: The size of EXT_METADATA_START_ADDR buffer is 54words (216bytes).
METADATA_ENABLE and EXT_METADATA_START_ADDR should be set on SEQ_START

6.4.2.4.5 Put Extradata (PUT_EXTRADATA, W, Offset = 0x0048)

PUT_EXTRADATA	Bit	Description	Initial State
Reserved	[31:1]	Reserved	Undef
PUT_EXTRADATA	[0]	Host informs MFC of the existence of extra metadata for each frame decoding. Valid only if EXTRADATA_ENABLE is set. 0 = No extra metadata 1 = Extra metadata exists	Undef

6.4.2.4.6 Extradata Address Register (EXTRADATA_ADDR, W, Offset = 0x004C)

EXTRADATA_ADDR	Bit	Description	Initial State
EXTRADATA_ADDR	[31:0]	Host informs MFC of the address of extra metadata. MFC copies the extra metadata to the shared memory output. MFC will copy only if EXTRADATA_ENABLE and PUT_EXTRADATA are set	Undef

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6.5 METADATA INTERFACE

Shared memory is used to exchange information between the MFC core and an external host. Host should allocate metadata input and output buffers in the shared memory, and inform MFC of the pointer through the EXT_METADATA_START_ADDR register.

The structure of the metadata buffer output is OpenMax compliant which is shown as follows:

```
typedef struct OMX_OTHER_EXTRADATATYPE {
OMX_U32                 nSize;
OMX_VERSIONTYPE         nVersion;
OMX_U32                 nPortIndex;
OMX_EXTRADATATYPE       eType;
OMX_U32                 nDataSize;
OMX_U8                  data[1];
} OMX_OTHER_EXTRADATATYPE;
```

Note that the start and end addresses should be informed through metadata buffer<n> addr and metadata buffer size.

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6.5.1 SHARED MEMORY INTERFACE FOR DECODERS

MFC decoders use the shared memory to report QP, concealed macroblock information, VC1 parameters, SEI, VUI information. *Table 6-1* describes the payload in the shared memory, and *Figure 6-5* shows the shared memory input structure in more detail. The shared memory input structure should be provided to MFC on the INIT_BUFFERS command.

Table 6-1 Payload in the Shared Memory

Element	Payload
Metadata[0]	No more metadata
Metadata[1]	QP information of each decoded macroblocks
Metadata[2]	An error map of concealed macroblock information
Metadata[3]	VC1 parameters
Metadata[4]	SEI NAL information
Metadata[5]	VUI information
Metadata[6]	Number of concealed macroblocks

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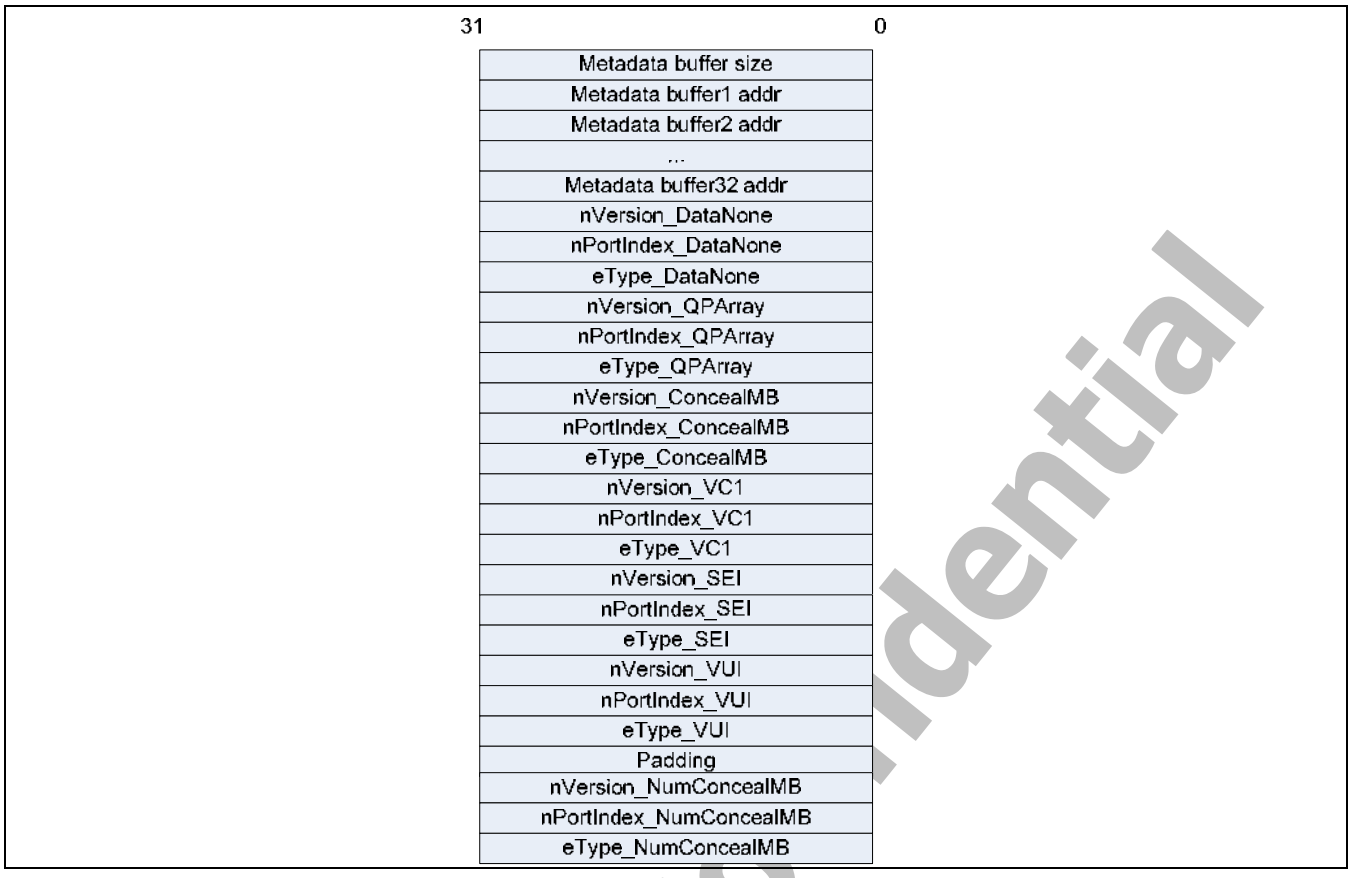

Figure 6-5 Shared Memory Input for Decoders

There is one-to-one mapping between each metadata output buffer and corresponding DPB. Hence it is host's responsibility to allocate NUM_DPB number of metadata buffers with the same size. The remaining metadata buffer addresses are not used in storing metadata. The size is communicated through the first fields in the shared memory input.

However since the VUI information is embedded in the sequence header (SPS in H.264), there is no one-to-one relationship between VUI and metadata buffers. MFC will return the appropriate VUI for a specific frame when there is an SPS change.

Figure 6-6 shows the metadata output in the shared memory for each DPB. In the metadata output structure, the 20bytes header as well as the payload for each field will be present only if the corresponding bits in the METADATA_ENABLE register. However, if the metadata buffer is full, the payload will be discarded.

When the input bitstream consists of one frame worth of data and one or more extra data, it will be copied to the ExtraData metadata. In this case, the address of the extra data is informed through the EXTRADATA_ADDR register.

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Figure 6-7 shows more detailed data structure for the VC1 parameters. The numbers in the parenthesis specify the effective number of bits for each field.

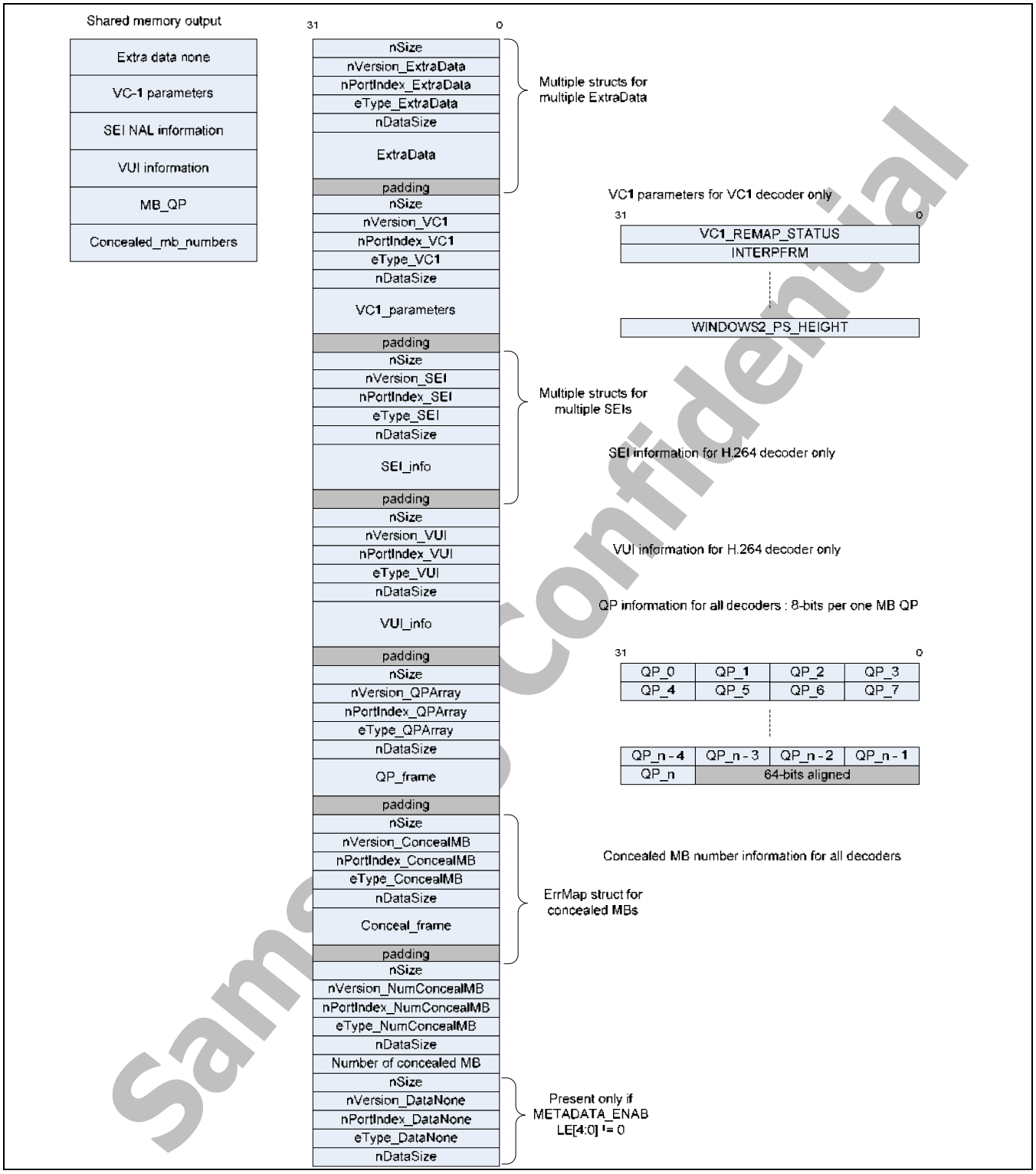

Figure 6-6 Shared Memory Output for Decoders

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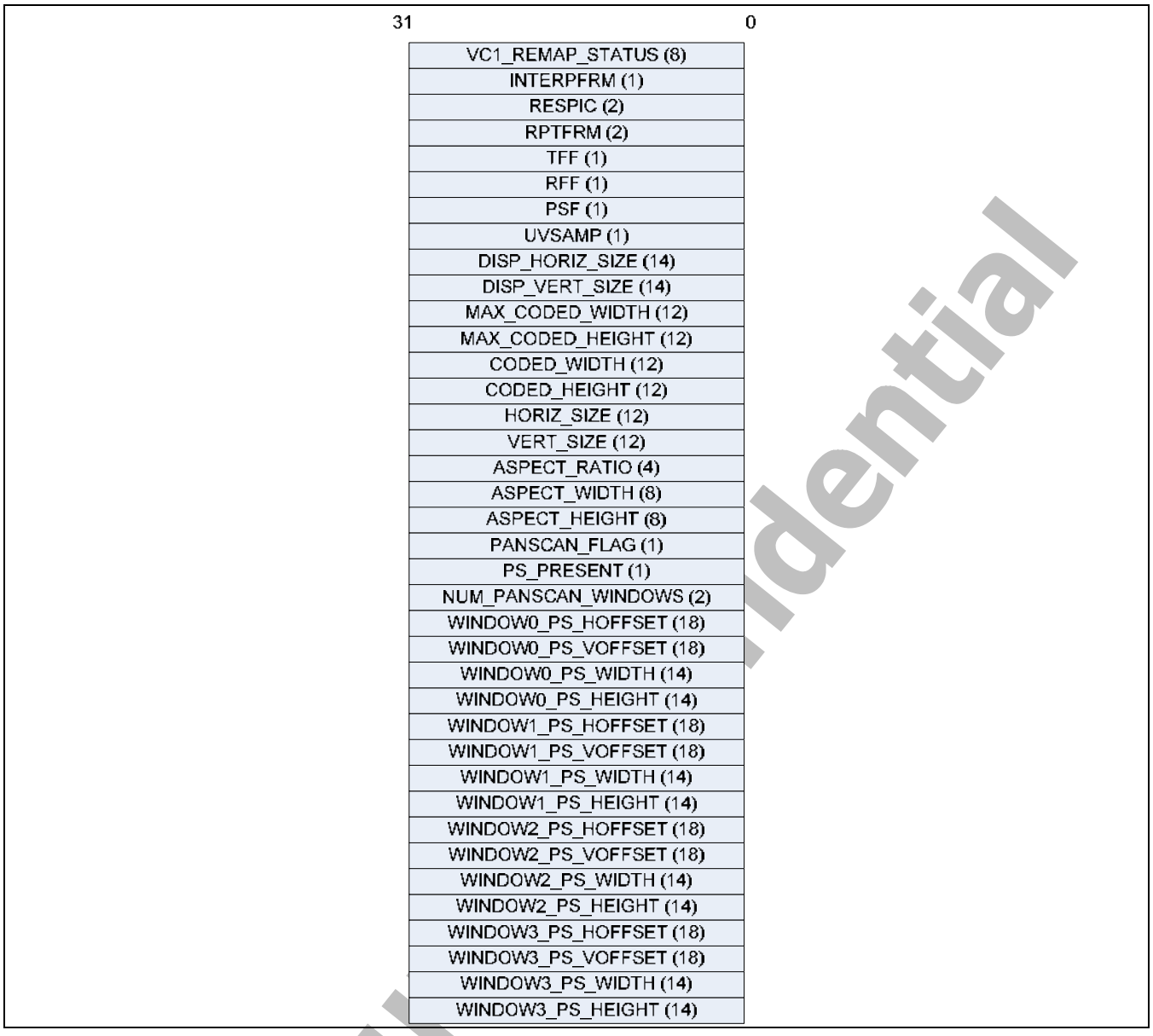

Figure 6-7 VC1 Parameters

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6.5.2 SHARED MEMORY INTERFACE FOR ENCODERS

MFC encoder uses the shared memory to report the slice information when a frame consists of multiple slices.

Figure 6-8 shows the metadata input structure for encoders. The input structure is provided to MFC for each FRAME_START command so that host updates the metadata buffer address accordingly.

Figure 6-9 shows the metadata output for encoders. Currently there is only one metadata field for encoders in which the slice size metadata provides the offset and length information for multiple slices.

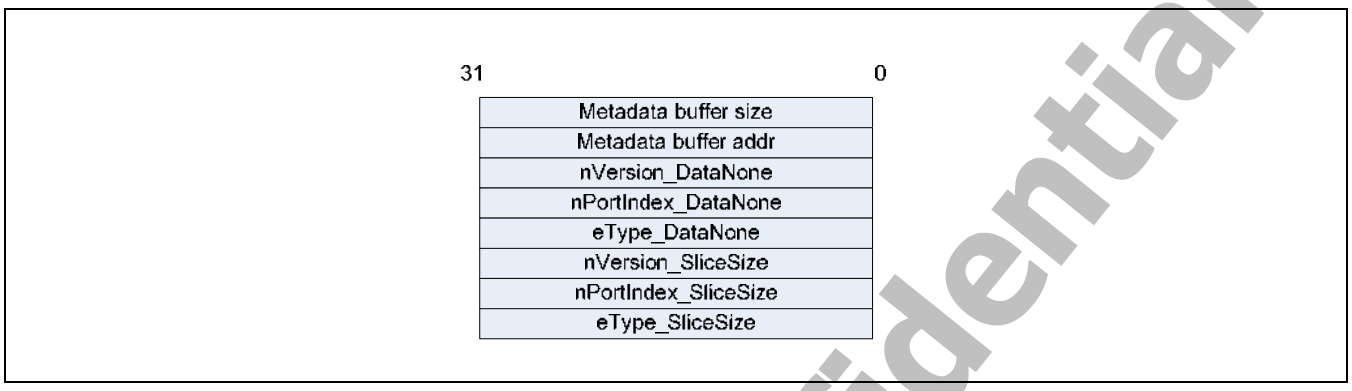

Figure 6-8 Shared Memory Input for Encoders

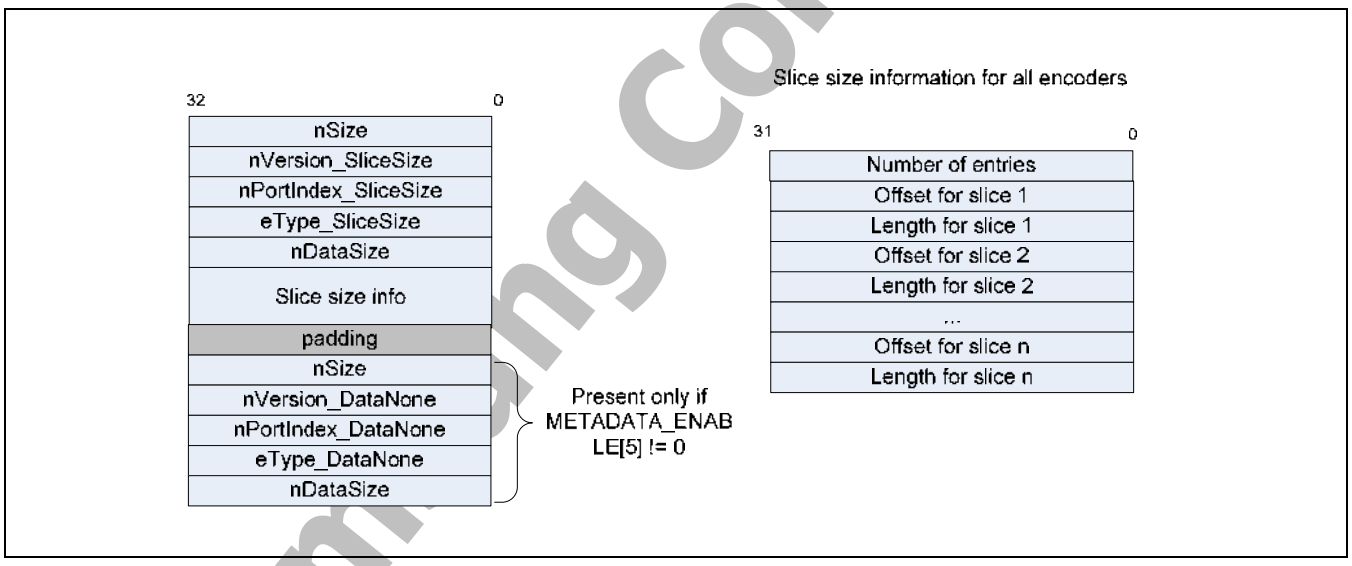

Figure 6-9 Shared Memory Output for Encoders

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6.6 APPENDIX

6.6.1 SUMMARY OF BUFFER REQUIREMENTS

There are different types of buffers in MFC. Memory buffers for the firmware/host interface have different alignment and size requirements than the buffers for the firmware/hardware engine interface.

Type	Address	Size
Linear memory	Alignment: 2KB aligned Format: 11bit right shifted	See 1.3.2.4
	Example: CH_ES_ADDR, CH_DESC_ADDR, DEC_NB_DCAC, etc	
Tiled memory	Alignment: 8KB aligned Format: 11 bit right shifted	Multiple of 8KB
	Example: DEC_LUMA_x, DEC_CHROMA_x, DEC_MV_x	
Shared memory	4byte aligned	Multiple of 4bytes
	Example: HOST_WR_ADDR, EXT_METDATA_START_ADDR, etc	

NOTE:

1. MC_DRAMBASE_ADDR has to be added to compute the physical address
2. Linear memory and shared memory are set as an offset from MC_DRAMBASE_ADDR_A. Whereas tiled memory is set as an offset from MC_DRAMBASE_ADDR_A or MC_DRAMBASE_ADDR_B according to the base address index

NOTE:

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6.6.2 BATCH ENCODING INTERFACE

MFC supports frame batch encoding so that host submits multiple frames in a single command and receives a response. MFC processes the multiple frames and raises an interrupt when all of the frames are encoded.

The batch encoding interface uses the shared memory in which host specifies the following information: the number of frames and a list of information for each frame. Using the information, MFC encodes multiple frames in the encoding order and generates an interrupt along with an output structure which describes details of encoded frames. Required shared memory fields are: BATCH_INTPUT_ADDR, BATCH_OUTPUT_ADDR, and BATCH_OUTPUT_SIZE. The input and output structures are defined as follows:

```
typedef struct
{
        unsigned int data_id;       // FRAME_BATCH_CMD, FRAME_BATCH_RESP
        unsigned int data_size;
        unsigned int number_of_frames;

        struct frame_info_t
        {
                unsigned int cur_luma_addr;
                unsigned int cur_chroma_addr;
                unsigned int set_frame_tag;
                unsigned int vop_timing;
        } frame_info[number_of_frames];

        unsigned int number_of_stream_buffer;
        unsigned int stream_buffer_size;
        unsigned int stream_buffer_address[number_of_stream_buffer];

} input_struct;
```

Figure 6-10 Shared Memory Output for Encoders

```
typedef struct
{
        unsigned int data_id;       // FRAME_BATCH_CMD, FRAME_BATCH_RESP
        unsigned int data_size;     // data size that firmware generated

        unsigned int number_of_frames;
        struct stream_info_t
        {
```

```
                unsigned int stream_info_id;
                unsigned int stream_info_size;
                unsigned int cur_luma_addr;
                unsigned int cur_chroma_addr;
                unsigned int pic_count;
                unsigned int slice_type;
                unsigned int get_frame_tag;
                unsigned int size_of_encoded_streams;
                unsigned int number_of_stream_buffers;
                unsigned int stream_address[number_of_stream_buffers];
        } stream_info[number_of_frames];

        unsigned int number_of_frames_accepted;
        unsigned int number_of_stream_buffers_unused;       // unused output buffers
        unsigned int stream_address_unused[number_of_stream_buffers_unused];

} output_struct;
```

Figure 6-11 Shared Memory Output for Encoders

When host invokes FRAME_BATCH_START, MFC first reads an input structure from the address pointed by BATCH_INTPUT_ADDR. The fields in the input_struct are as follows:

- data_id: FRAME_BATCH_CMD or FRAME_BATCH_RESP
- data_size: The size of input_struct which also includes the size of data_id
- number_of_frames: The number of frames that host wants to encode
- cur_luma_addr: The address of input luma picture that corresponds to CURRENT_Y_ADDR
- cur_chroma_addr: The address of input chroma picture that corresponds to CURRENT_C_ADDR
- set_frame_tag: A frame tag of an input frame. The same definition as SET_FRAME_TAG
- vop_timing: VOP timing of an input frame
- number_of_stream_buffer: The number of output buffers of encoded frames
- stream_buffer_size: The size of an output buffer of encoded frame
- stream_buffer_address: The address of output buffers of encoded frames
-

When MFC completes frame encoding, it generates an output_struct structure which is stored at BATCH_OUTPUT_ADDR with the size of BATCH_OUTPUT_SIZE. The structure provides the details of the encoded bitstreams:

- data_id: FRAME_BATCH_CMD or FRAME_BATCH_RESP
- data_size: The size of output_struct which also includes the size of data_id
- number_of_frames: The number of frames that host received for encoding

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- number_of_frames_accepted: The number of frames that host accepted to complete encoding
- cur_luma_addr: The address of input luma picture that has been encoded
- cur_chroma_addr: The address of input chroma picture that has been encoded
- pic_count: A picture count in display order. pic_count provides information when there is reordering, since MFC encodes input frames in decoding order, not in display order.
- slice_type: The same definition as ENC_SLICE_TYPE
- get_frame_tag: A frame tag of an output frame. The same definition as GET_FRAME_TAG
- size_of_encoded_streams: Size of an encoded bit stream
- number_of_stream_buffers: The number of encoded stream buffers. If the size of generated stream is greater than stream_buffer_size in input_struct, more than one stream buffer will be required
- stream_address: The address of encoded stream buffers
- number_of_stream_buffers_unused: The number of unused stream buffers after an encoding batch
- stream_address_unused: The address of unused stream buffers after an encoding batch

Note that MFC stops encoding when either stream buffer is full or output_struct is full. In either case, number_of_frames_accepted will be smaller than number_of_frames. Host may resubmit the last frames from the previous input_struct as many as unaccepted in output_struct. The resubmitted frames will be encoded continuously.

When number_of_stream_buffer is greater than number_of_frames, it is possible that some of the stream buffers are not used. MFC returns them over number_of_stream_buffers_unused and stream_address_unused. Host may reuse them in the next batch.

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7 TVOUT & VIDEO DAC

7.1 OVERVIEW OF TVOUT AND VIDEO DAC

The TVOUT module supports ITU-R BT.470 and EIA-770 compliant analog TV signals with 1 channel 10-bit DAC. The signal format is CVBS. It also supports EIA-608 compliant closed caption and extended data service, IEC61880 / ITU-R BT.1119 compliant wide screen signaling, and EIA-J CPR1204-1 compliant analog copy generation management system.

7.2 KEY FEATURES OF TVOUT AND VIDEO DAC

The TVOUT module includes following features:

7.2.1 I/O AND CONTROL

ITU-R BT.601 (YCbCr 4:4:4) input format

10-Bit, 4X over sampled CVBS output data to 1-channel 54 MHz DAC

7.2.2 VIDEO STANDARD COMPLIANCES FOR CVBS:

(M) NTSC, NTSC-J

(B/D/G/H/I) PAL, (M) PAL, (N) PAL, (Nc) PAL

PAL-60, NTSC4.43

7.2.3 ANCILLARY DATA INSERTION

EIA-608 compliant Closed Caption(CC) and Extended Data Service(XDS)

IEC61880 / ITU-R BT.1119 compliant Wide Screen Signaling(WSS)

EIA-J CPR1204-1 compliant analog copy generation management system(CGMS-A)

7.2.4 POST PROCESSING

Color Compensation for Invalid RGB Data

Programmable 23-Tap Luma/ Chroma Filters for Luma/ Chroma anti-aliasing for CVBS

Programmable 95-Tap oversampling filter capable of frequency response compensation

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7.3 DATA FLOW

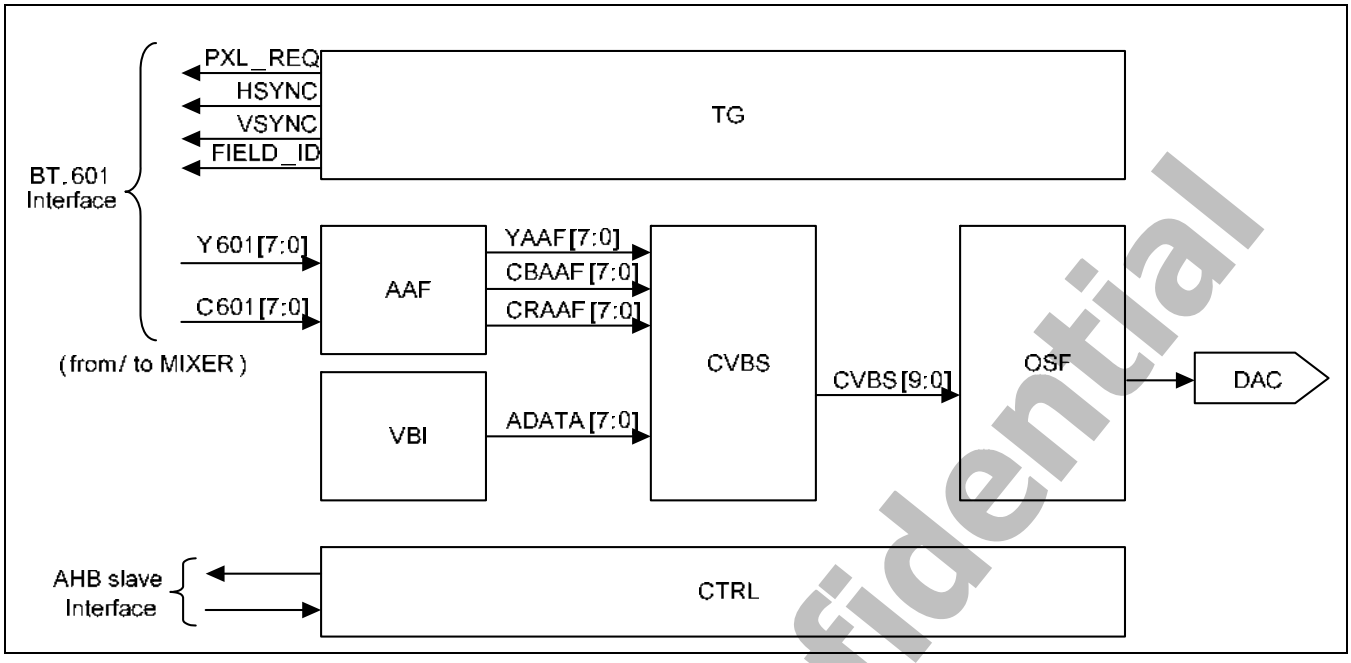

Figure 7-1 Data Flow of TVOUT Module

The TVOUT module is composed of the following data sub-modules:

- TG: Timing Generation
- CVBS: Waveform Generation, QAM Modulation, and YCbCr Video Processing
- AAF: Affine Transformation, luma/ chroma Anti-Aliasing Filter
- OSF: 4x Oversampling Filter
- VBI: Ancillary data insertion during vertical blanking interval
- CTRL: Register Control

NOTE: Image Mixer is directly connected with TVOUT and HDMI. Thus, to complete the connection, you must configure REG_DST_SEL in MIXER_CFG register.

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7.4 TIMING GENERATION (TG MODULE)

The Timing Generation (TG) sub-module generates all the timing information signals required for ITU-R BT.470 compliant TV signals. An internal pixel counter generates horizontal and vertical timing signals and an internal Discrete Time Oscillator (DTO) makes the phase signals of sub-carrier.

There are two kinds of horizontal and vertical timings in TG module, namely:

7.4.1 525/60 HZ

Video standard: NTSC (M), NTSC-J, PAL (M), NTSC 4.43, and PAL 60
Horizontal frequency (FH): 15.734 kHz, 858 samples per line @ 13.5 MHz sample rate
Vertical frequency (FV): 59.94 Hz, 525 lines per frame

7.4.2 625/50 HZ

Video standard: PAL (BGHID), PAL (N), and PAL (Nc)
Horizontal frequency (FH): 15.625 kHz, 864 samples per line @ 13.5 MHz sample rate
Vertical frequency (FV): 50.00 Hz, 625 lines per frame

There are four kinds of discrete timing oscillation for sub-carrier generation in TG module, namely:

7.4.3 3.579545 MHZ

Video standard: NTSC (M) and NTSC-J
Sub-carrier frequency (FSC): 910/4 * FH

7.4.4 4.43361875 MHZ

Video standard: PAL (BGHID), PAL (N), NTSC 4.43, and PAL 60
Sub-carrier frequency (FSC): (1135/4 + 1/625) * FH

7.4.5 3.57561149 MHZ

Video standard: PAL (M)
Sub-carrier frequency (FSC): 909/4 * FH

7.4.6 3.58205625 MHZ

Video standard: PAL (Nc)

Sub-carrier frequency (FSC): (917/4 + 1/625) *

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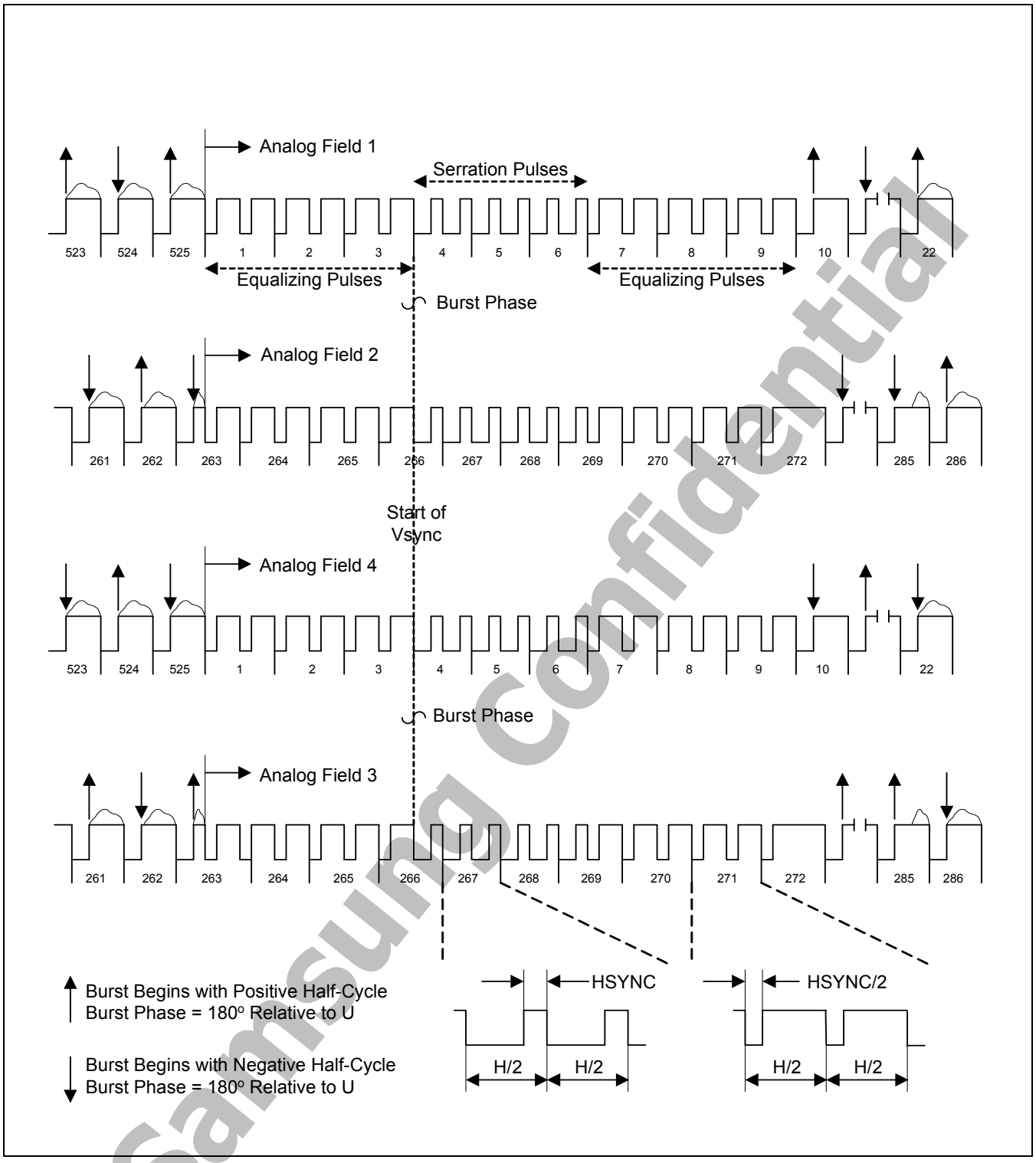

Figure 7-2 Four Field NTSC (M) Sequence and Burst Blanking

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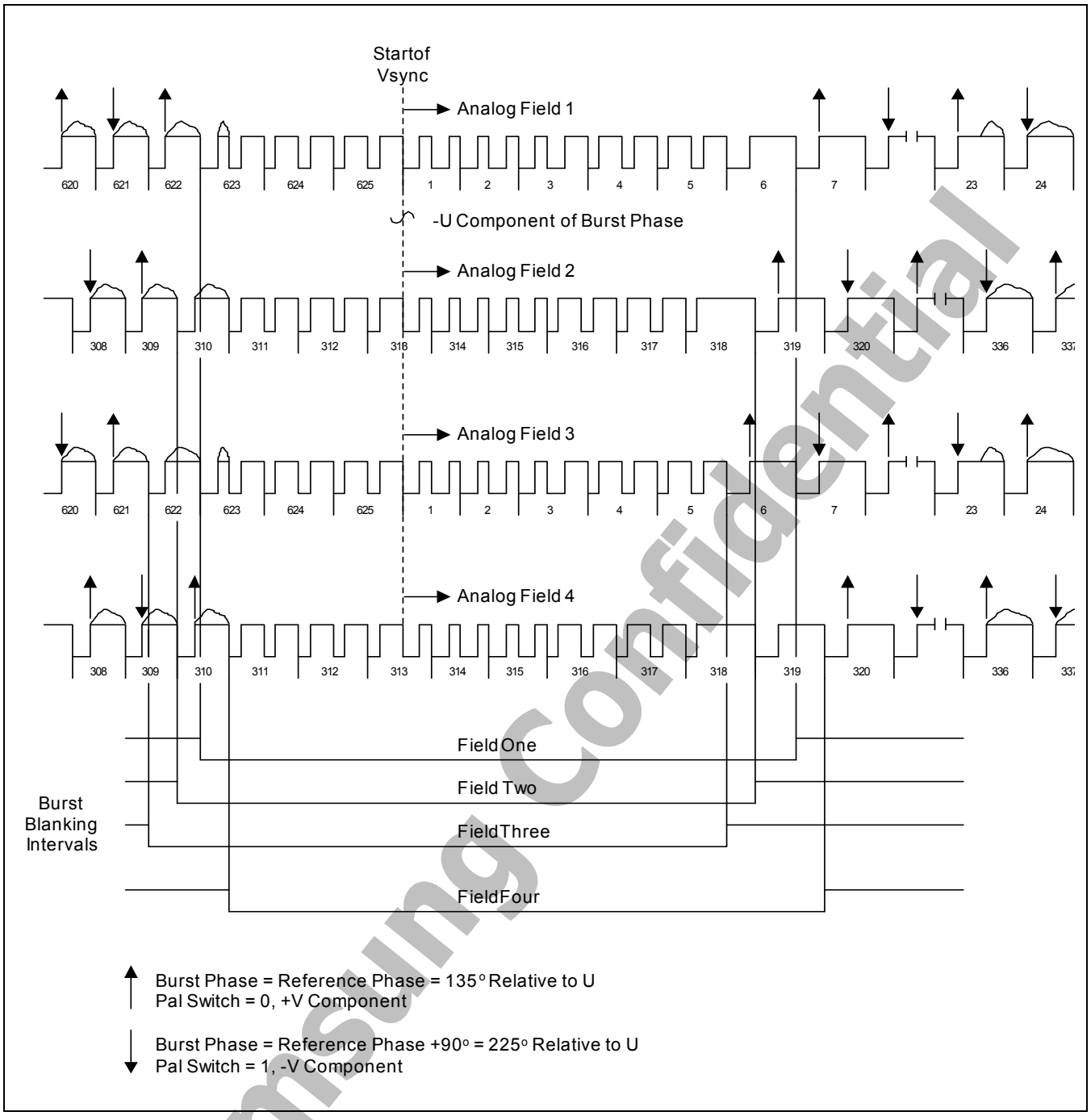

Figure 7-3 Field PAL (BGHIDNc) Sequence and Burst Blanking

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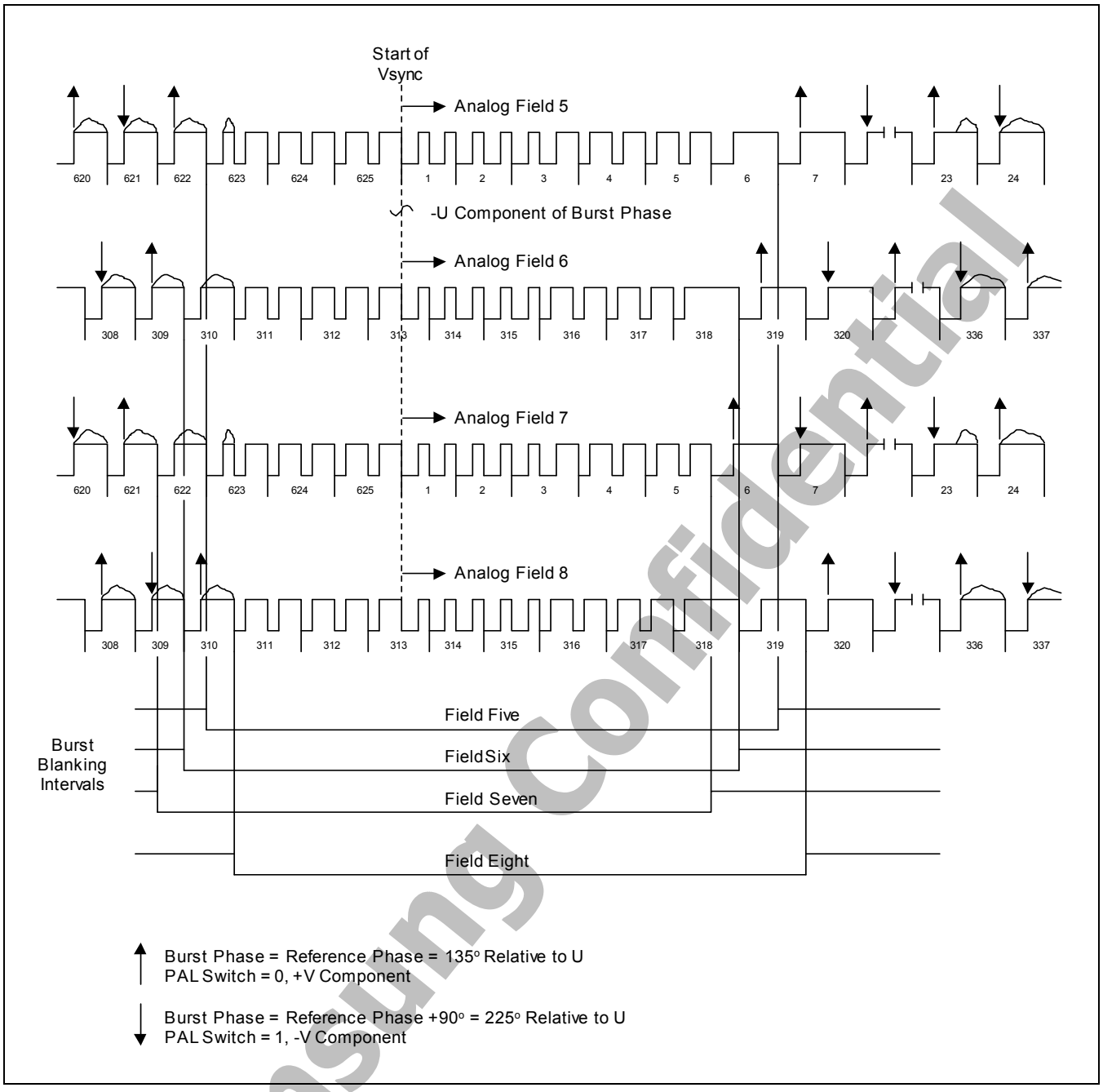

Figure 7-4 Eight Field PAL (BGHIDNc) Sequence and Burst Blanking

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The internal pixel rate is 13.5 MHz which is 1/4 times of 54 MHz video clock which is used for DAC. With 13.5 MHz pixel rate, the horizontal blanking timing and active video timing are defined as follows:

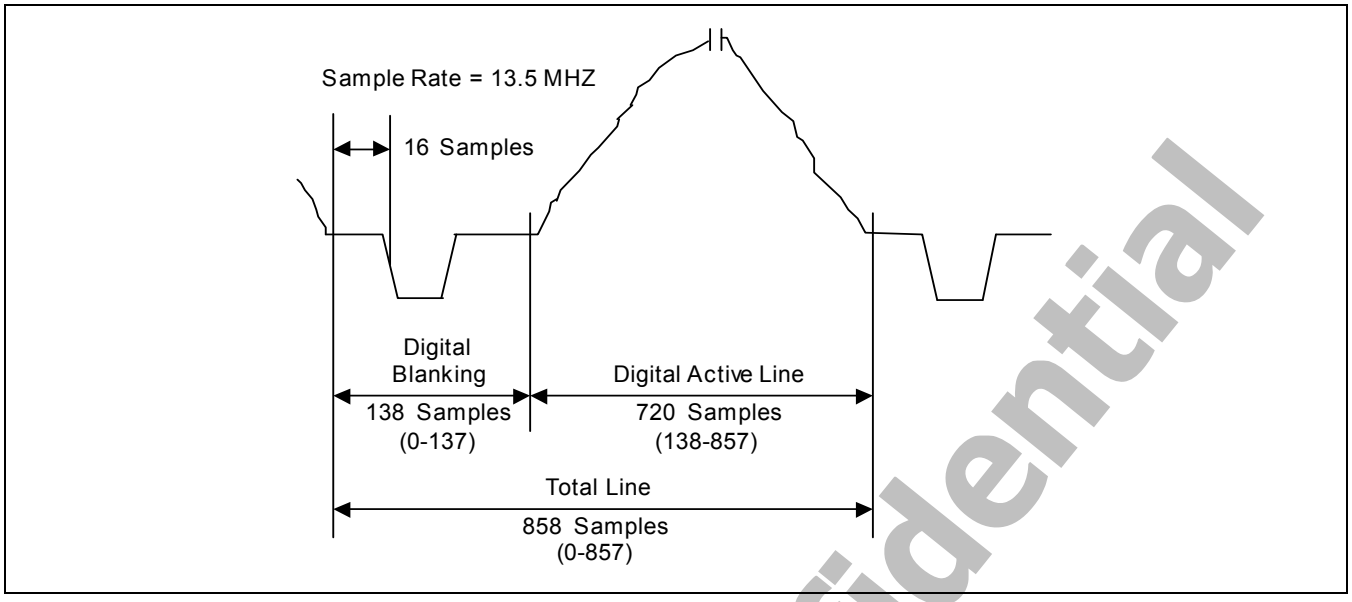

Figure 7-5 Horizontal Blanking and Active Video Timing @ 525/60 Hz

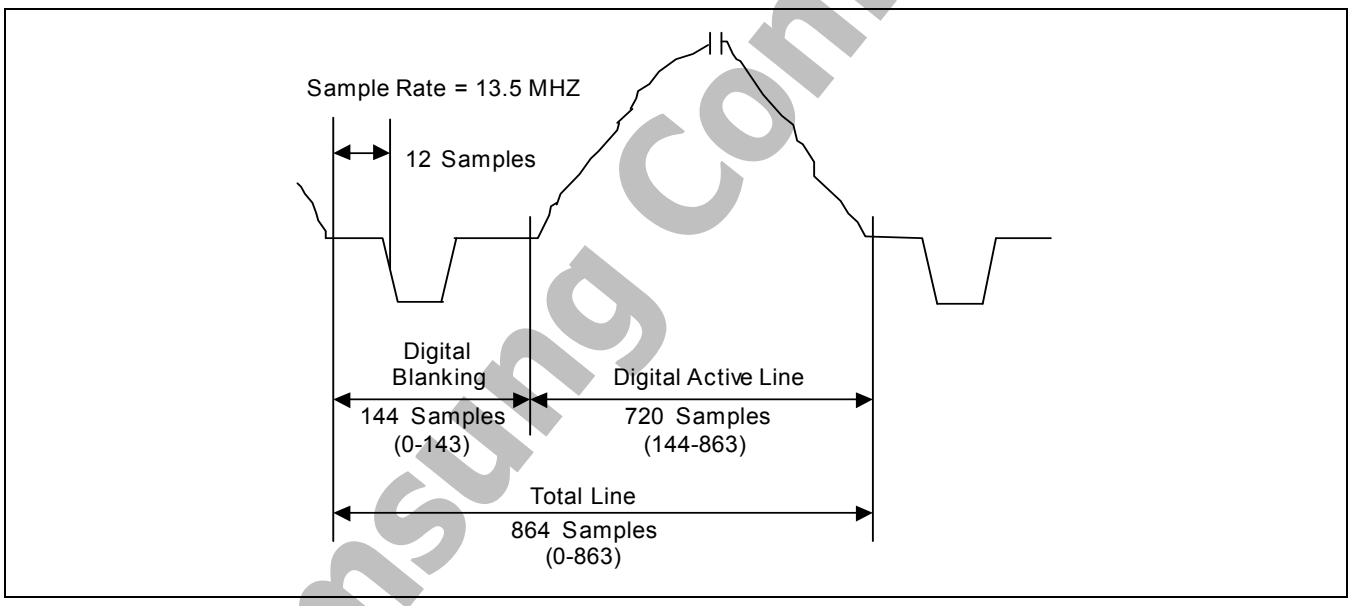

Figure 7-6 Horizontal Blanking and Active Video Timing @ 625/50 Hz

VIDEO [3:0] bits in SDO_CONFIG register controls all the timing signals in TG module. Finally note that all the internal counters and discrete time oscillators operate with 54 MHz video clock. The hsync, vsync, field_id, and data request signals are generated and used internally at 54 MHz rate. If they are delivered to 'DispPipe' module their timings are re-synchronized with 135 MHz system clock.

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7.5 ANTI ALIASING FILTER (AAF MODULE)

The color TV signals are composed of luminance video, chrominance video and audio data which are modulated by different sub-carriers. Hence, some spectral shaping to avoid the aliasing between them is required. ITU-R BT.407 recommends that the luminance data (Y) should be band-limited within 4.2, 5.0, 5.5, or 6.0 MHz with respect to video standards to avoid the crosstalk between audio sub-carrier and the luminance data. It also recommends that the chrominance data (Cb and Cr) should be band-limited within 1.3 MHz to avoid the crosstalk between chrominance sub-carrier and the luminance data. If audio multiplexing is not required, band-limiting of luminance data (Y) may be skipped. Similarly, band-limiting of chrominance data (C) may be skipped at S-video encoding rather than CVBS encoding.

The AAF sub-module in TVOUT provides 23-tap linear FIR filters for spectral shaping of luminance data (Y) and chrominance data (Cb and Cr). The filter responses are fully programmable since filter coefficients themselves are controllable. Since linear FIR filters have symmetric coefficients, 11 coefficients completely defines the filter responses. The registers SDO_Y0, SDO_Y1… and SDO_Y11 are used to control the luminance filter response. The register SDO_CB0, SDO_CB1… SDO_CB11, and SDO_CR0, SDO_CR1… SDO_CR11 are used to control the chrominance Cb and Cr filter responses, respectively.

The *Table 7-1* show typical settings of filter coefficients. Note that there is no filtering on luminance (Y) data. Since many CE devices usually do not output multiplexed audio, filtering on luminance (Y) data is not required. Filter is not normalized and the dc gain of the filter may vary with the video scale. Refer to 3.1.5 SDO Video Scale Configuration Register and 3.1.10 ~ 3.1.45 SDO Anti Aliasing Filter Coefficients.

Table 7-1 Filter Coefficients of Anti-aliasing Filters for Luminance Y

Register	7.5 IRE Setup/ 7:3 Sync	7.5 IRE Setup/ 10:4 Sync	0 IRE Setup/ 7:3 Sync	0 IRE Setup/ 10:4 Sync
SDO_Y0	0	0	0	0
SDO_Y1	0	0	0	0
SDO_Y2	0	0	0	0
SDO_Y3	0	0	0	0
SDO_Y4	0	0	0	0
SDO_Y5	0	0	0	0
SDO_Y6	0	0	0	0
SDO_Y7	0	0	0	0
SDO_Y8	0	0	0	0
SDO_Y9	0	0	0	0
SDO_Y10	0	0	0	0
SDO_Y11	252	25D	281	28F

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Table 7-2 Filter Coefficients of Anti-aliasing Filters for Chrominance Cb

Register	7.5 IRE Setup/ 7:3 Sync	7.5 IRE Setup/ 10:4 Sync	0 IRE Setup/ 7:3 Sync	0 IRE Setup/ 10:4 Sync
SDO_CB0	0	0	0	0
SDO_CB1	0	0	0	0
SDO_CB2	0	0	0	0
SDO_CB3	0	0	0	0
SDO_CB4	0	0	0	0
SDO_CB5	1	1	1	1
SDO_CB6	6	7	7	7
SDO_CB7	13	14	15	15
SDO_CB8	28	28	2A	2B
SDO_CB9	3F	3F	44	45
SDO_CB10	51	52	57	59
SDO_CB11	56	5A	5F	61

Table 7-3 Filter Coefficients of Anti-aliasing Filters for Chrominance Cr

Register	7.5 IRE Setup/ 7:3 Sync	7.5 IRE Setup/ 10:4 Sync	0 IRE Setup/ 7:3 Sync	0 IRE Setup/ 10:4 Sync
SDO_CR0	0	0	0	0
SDO_CR1	0	0	0	0
SDO_CR2	0	0	0	0
SDO_CR3	0	0	0	0
SDO_CR4	0	0	0	0
SDO_CR5	2	1	2	2
SDO_CR6	5	9	A	A
SDO_CR7	18	1C	1D	1E
SDO_CR8	37	39	3C	3D
SDO_CR9	5A	5A	5F	61
SDO_CR10	76	74	7B	7A
SDO_CR11	7E	7E	86	8F

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The following figures show the magnitude and phase responses of CB and CR anti aliasing filters with the above settings. Note that these filters are applied only to CVBS.

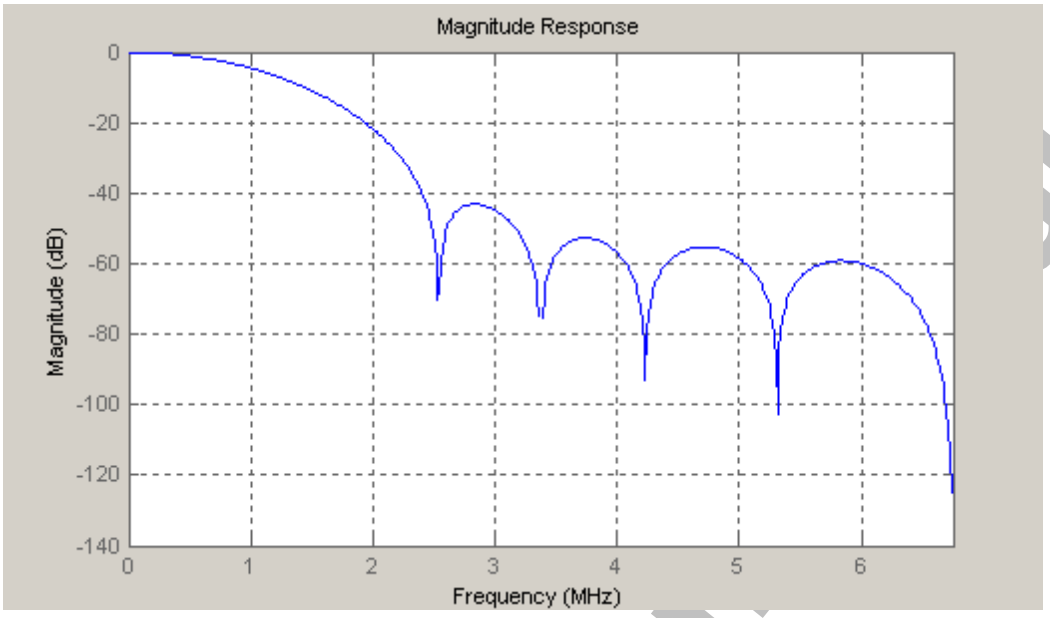

Figure 7-7 Magnitude Response of CB and CR Anti Aliasing Filter @ 13.5 MHz Sampling Rate

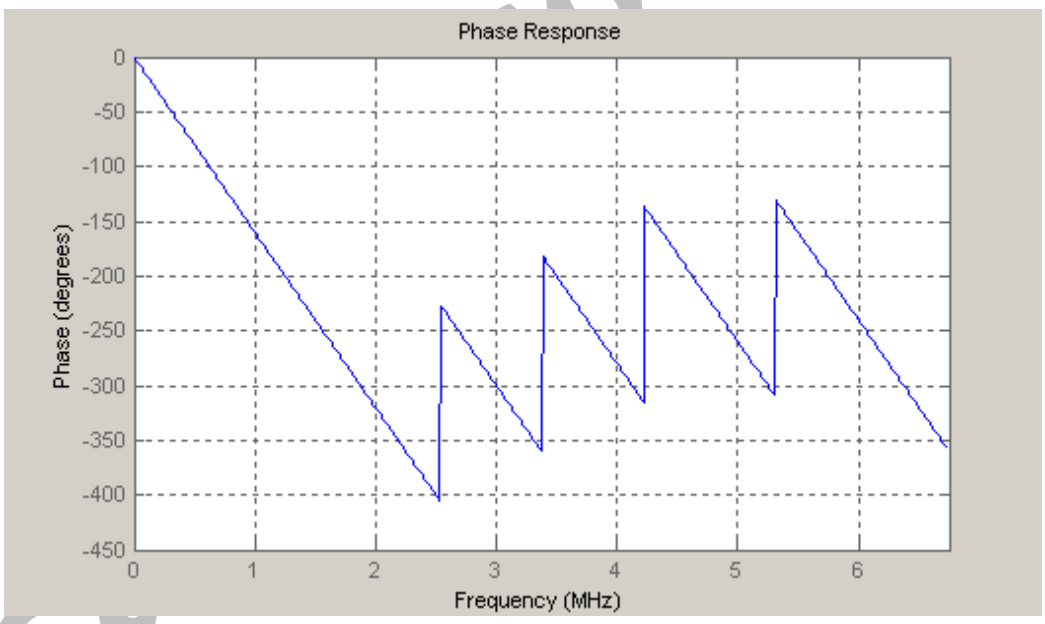

Figure 7-8 Phase Response of CB and CR Anti Aliasing Filter @ 13.5 MHz Sampling Rate

7.6 ANCILLARY DATA INSERTION (VBI MODULE)

The ITU-R BT.470 compliant TV signals include blanking lines, which do not possess video data. Some ancillary data such as closed caption, content information, display aspect ratio control, and copy control information are delivered within these blanking periods. The TVOUT module supports EIA-608 compliant closed caption (CC) and extended data service (XDS) and IEC61880 / ITU-R BT.1119 compliant wide screen signaling (WSS). The VBI sub-module draws the waveform of the ancillary data delivering signals.

The physical waveform of EIA-608 closed caption and extended data service signals is as follows:

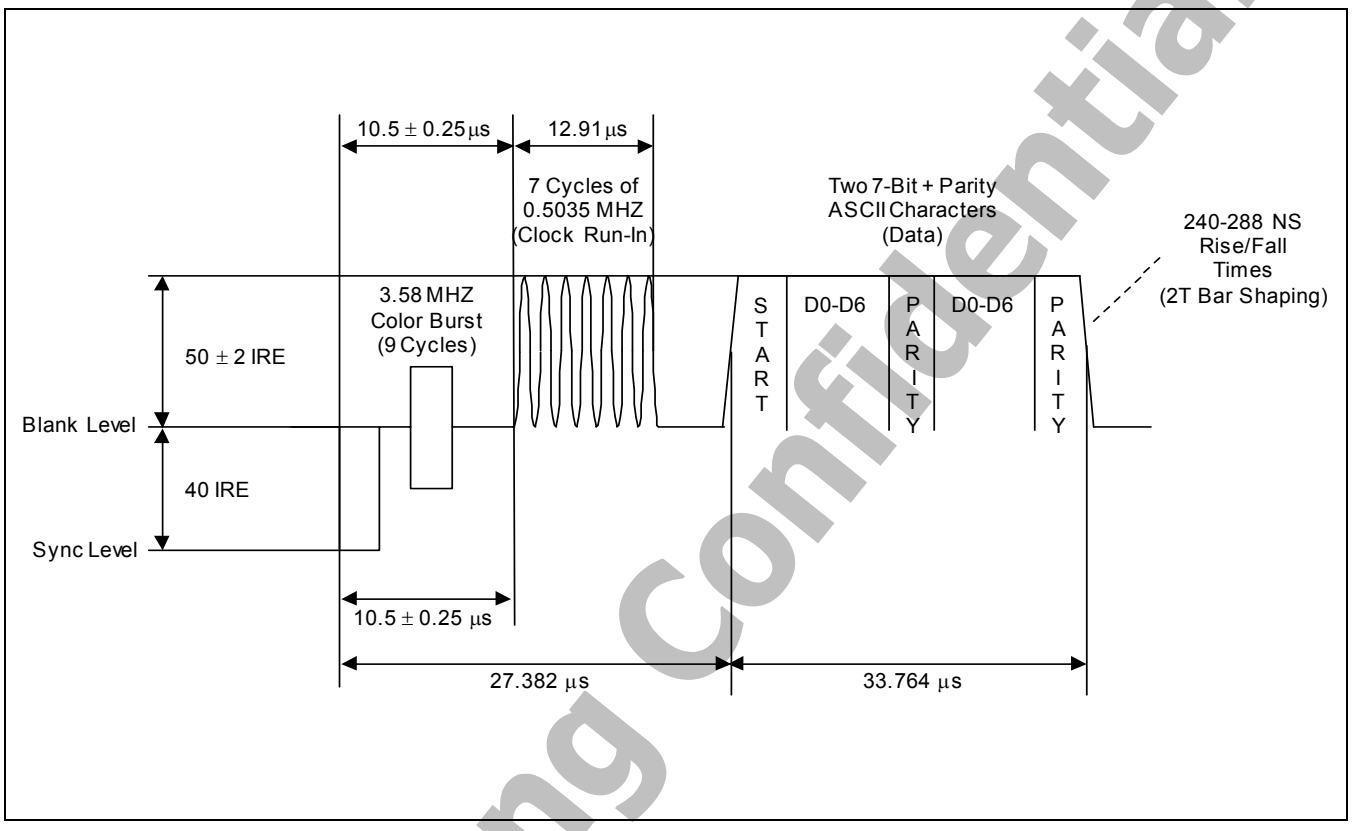

Figure 7-9 EIA-608 Closed Caption and Extended Data Service

This waveform is inserted at the 21'st line of 525/60 standard video. The register SDO_ARMCC is used for carrying the 2 byte data into the waveform including the parity bits. For the CC data and XDS data packet format and its usage, refer to the Recommendation EIA-608, "Recommended Practice for Line 21 Data Service".

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The physical waveform of IEC 61880 compliant wide screen signalling (WSS) signals is as follows:

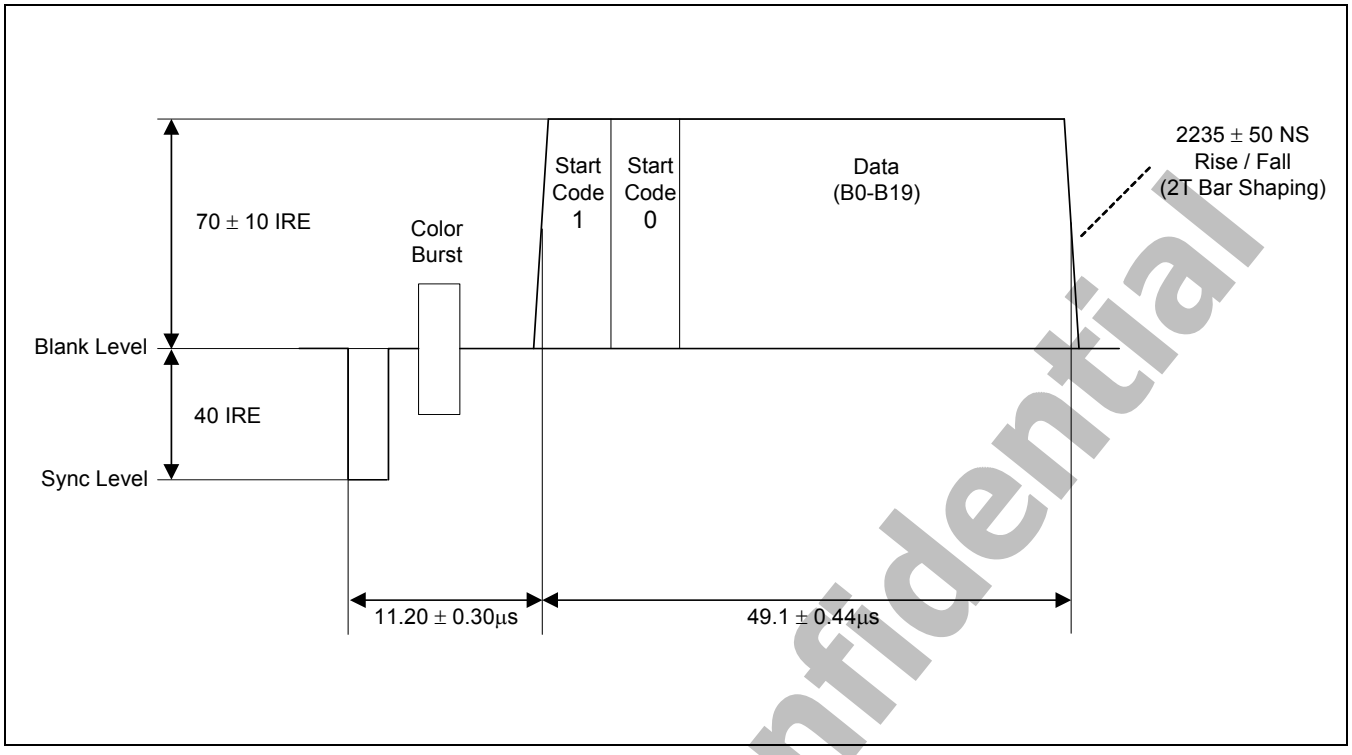

Figure 7-10 IEC 61880 Wide Screen Signaling

This waveform is inserted at the 20-th line of 525/60 standard video. The register SDO_ARMWSS525 is used to carry the 20 bit data into the waveform. Bits {b1, b0} define display aspect ratio control, bit {b7, b6, b5, b4, b3, b2} define copy control information, and bits {b13, b12, b11, b10, b9, b8} is used to specify the reserved signals. Bits {b19, b18, b17, b16, b15, b14} are used for CRC error check.

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The physical waveform of ITU-R BT.1119 compliant Wide Screen Signalling (WSS) signals is as follows:

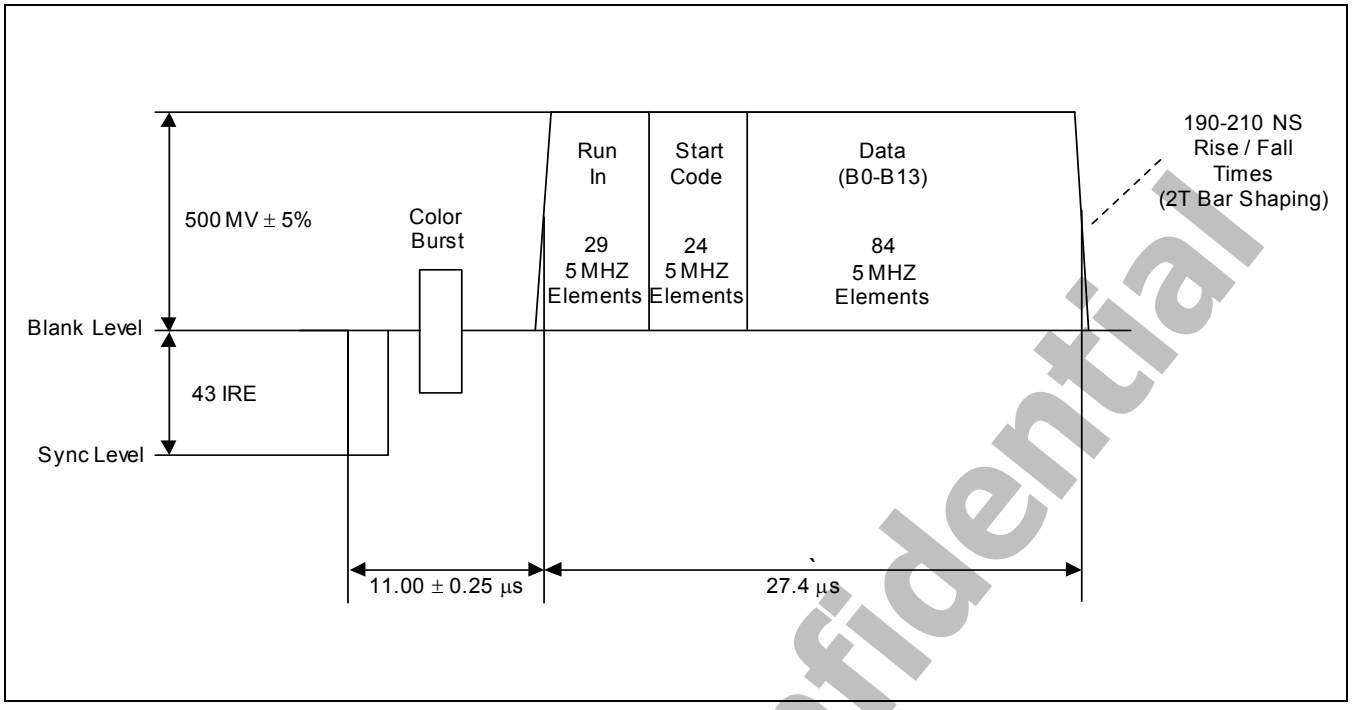

Figure 7-11 ITU-R BT.1119 Wide Screen Signaling

This waveform is inserted at the 23rd line of 625/50 standard video. The register SDO_ARMWSS625 is used for carrying the 14-bit data into the waveform. Bits {b3, b2, b1, b0} specify display aspect ratio control, bits {b7, b6, b5, b4} are used for enhanced TV service, bits {b10, b9, b8} is used for European teletext subtitle control, and bits {b13, b12, b11} are used for copy control.

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7.7 WAVEFORM GENERATION AND CHROMA MODULATION (CVBS MODULE)

The CVBS sub-module combines the timing information and video data to generate the waveforms of ITU-R BT 470 TV signals. Two different data paths do this procedure, namely, one is for luminance data (Y) and the other is for chrominance data (C). For the luminance data path, horizontal/ vertical synchronization pulses are formed and merged to a properly scaled and offset luminance video data (Y). For the chrominance data paths, base band chrominance data (Cb and Cr) are modulated with a sub-carrier FSC along with the video standard, that is:

$C(n) = U(n) * \sin(2\pi FSC * n) + V(n) * \cos(2\pi FSC * n)$,

where U(n) and V(n) denote properly scaled and offset versions of Cb(n) and Cr(n), respectively. Then a pilot sinusoidal waveform, called a burst, is formed and added prior to the start of modulated chrominance data C at each line. At the end of CVBS sub-module data paths, the luminance data (Y) and the chrominance data (C) is merged into one channel and form composite data (CVBS).

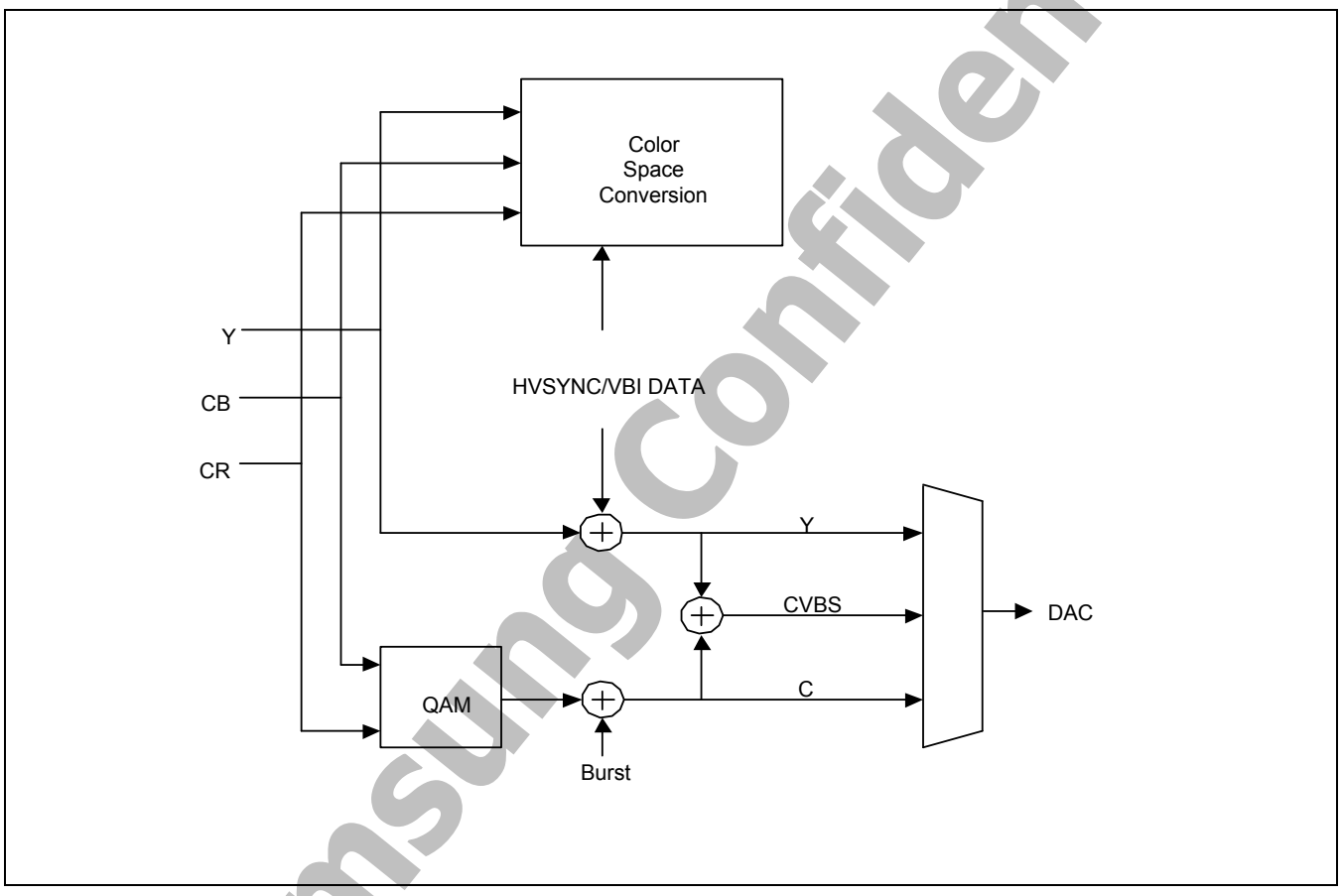

Figure 7-12 Data Flow of CVBS Sub-Module

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The *Figure 7-13* and *Figure 7-14* depict the typical CVBS waveforms generated. Figure show that the setup level and the ratios of video scale to sync depth are different according to video standards. This is same in YPbPr/RGB outputs. The setup level and video-to-sync ratio are controlled by CSETUP, CSYNC, VSETUP and VSYNC bits in SDO_SCALE registers. Note that the configuration of setup level and video-to-sync ratio in our implementation are set regardless of video standards and output format.

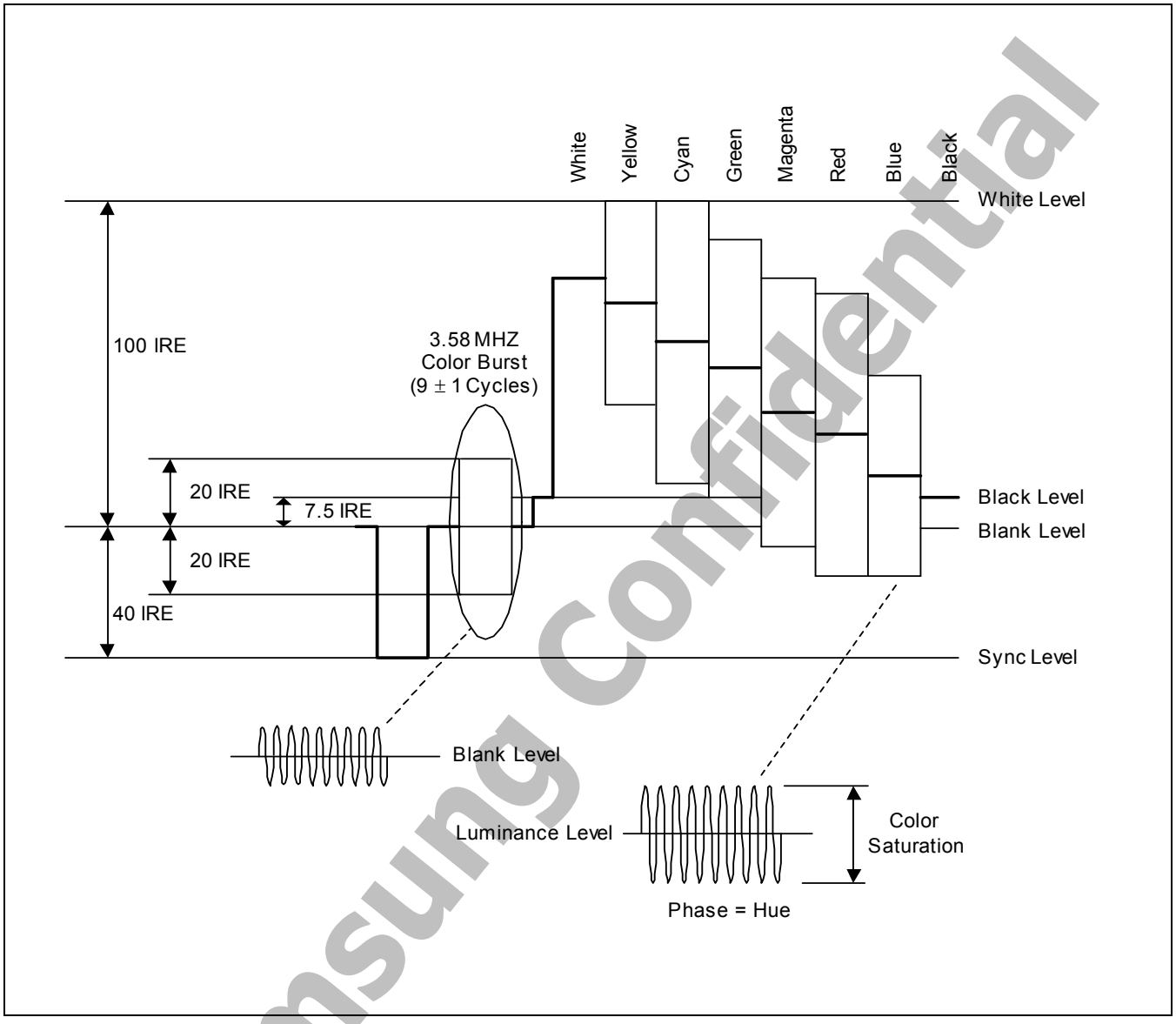

Figure 7-13 NTSC (M) Composite Video Signal with 75% Color Bars

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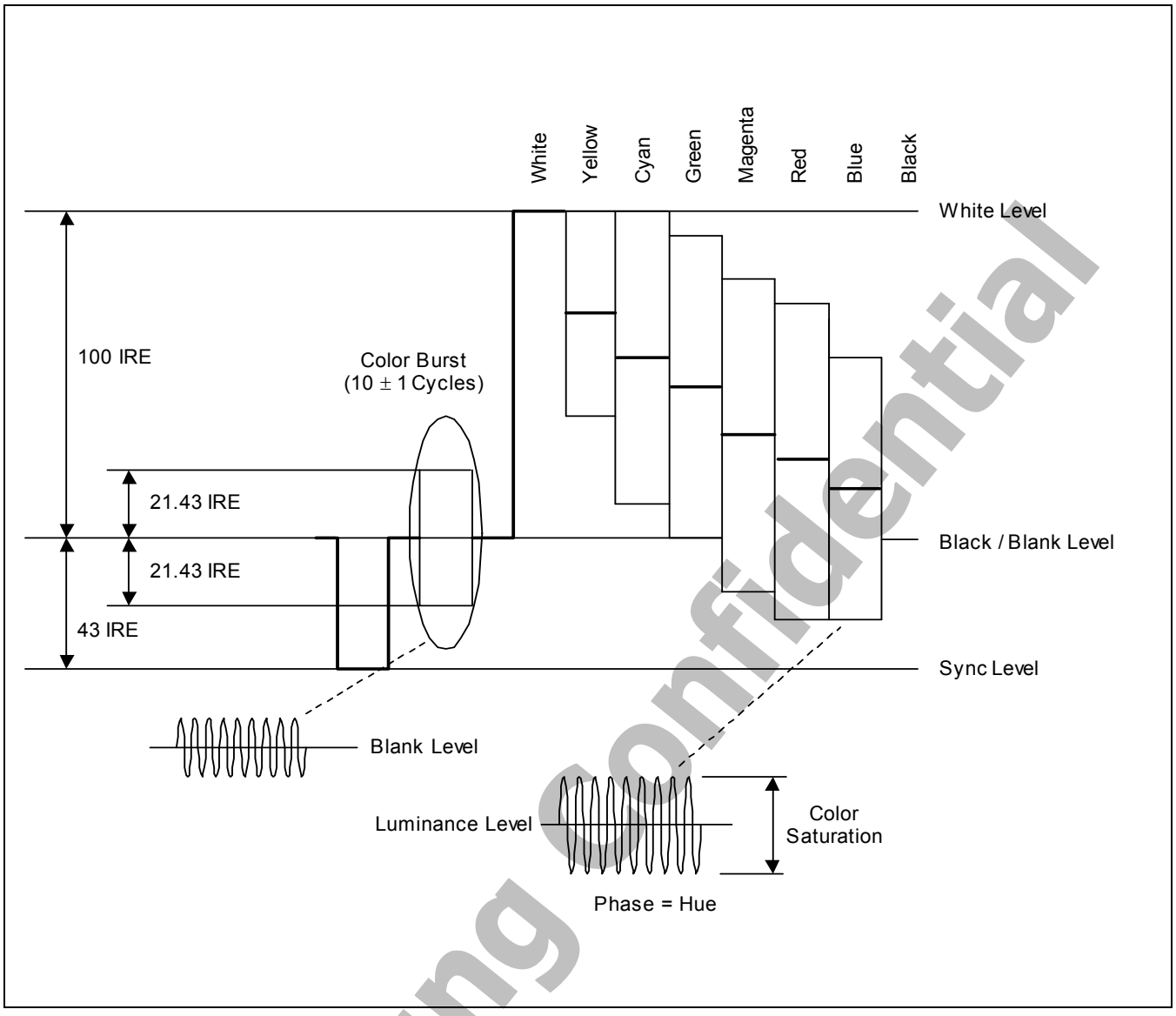

Figure 7-14 PAL (BGHIDNc) Composite Video Signal with 75% Color Bars

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7.8 ILLEGAL COLOR COMPENSATION (CVBS MODULE)

The CVBS sub-module also supports color compensation for illegal RGB data. Video data are usually processed in the YCbCr coordinates. At the result of filtering and scaling, the values of YCbCr can exceed their nominal range and values become invalid when they are transformed into RGB coordinates. This causes unwanted artifacts at display. The Figure illustrates the relation between YCbCr coordinates and RGB coordinates:

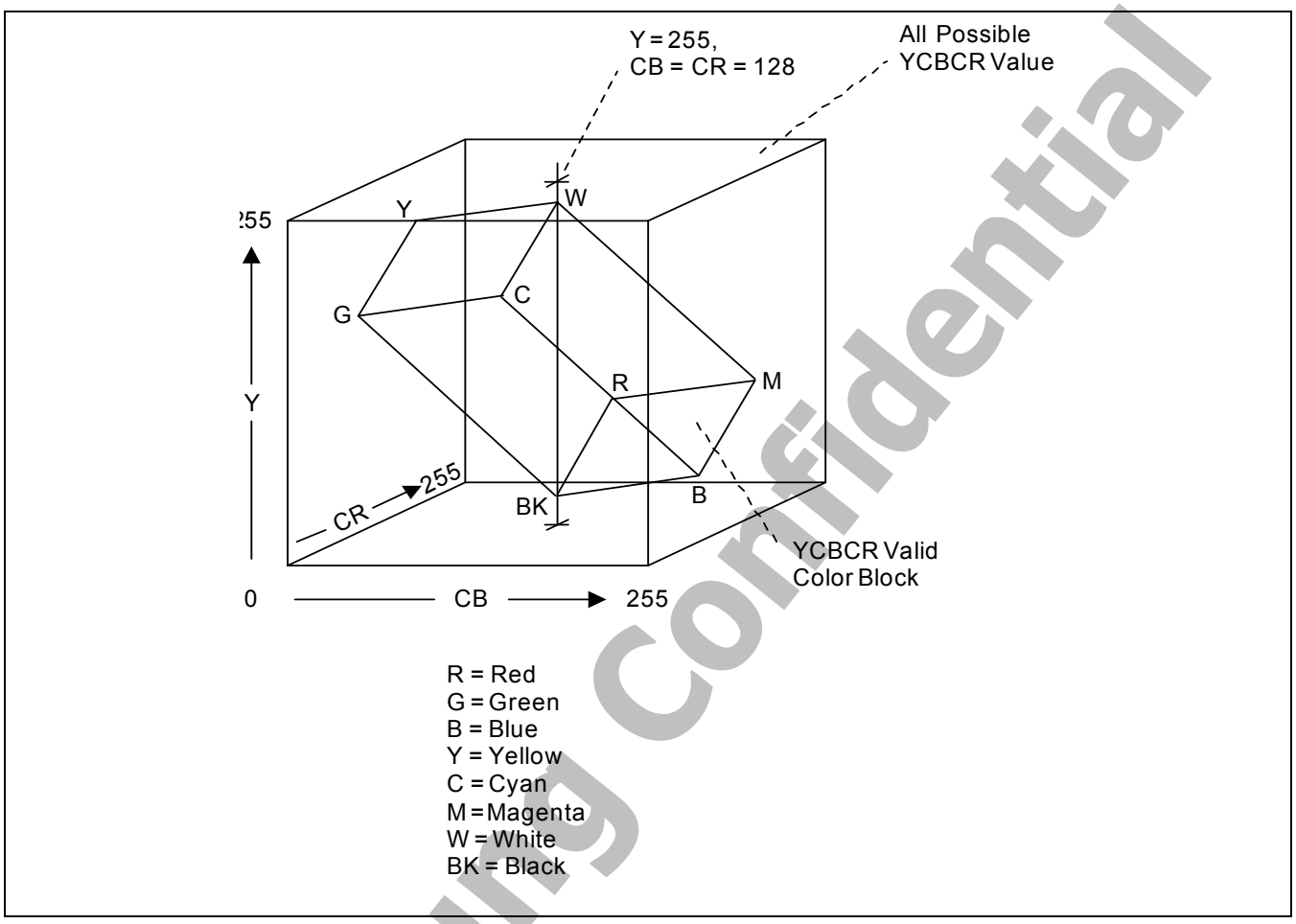

Figure 7-15 Color Cube Comparison

If YCbCr data converted to RGB data outside the RGB cube, the CVBS sub-module compensates the value so that the result falls within the RGB cube. A constant luma and constant hue approach is used for this compensation. The luminance Y is not altered while the chrominance Cb and Cr are limited to the maximum valid values having the same hue as the invalid color prior to limiting. The SDO_RGB_CC register controls the size of RGB cube that determine color compensation range. Meanwhile, if illegal YCbCr data are transformed to CVBS, there might be an overflow which exceeds DAC conversion range. The CVBS sub-module also compensates this error. The SDO_CVBS_CC_Y1, SDO_CVBS_CC_Y2, and SDO_CVBS_CC_C registers are used for the color compensation for CVBS output.

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7.9 OVERSAMPLING & DAC COMPENSATION FILTER (OSF MODULE)

The TVOUT module provides 2x or 4X oversampling filter prior to DAC in order to ease the design of analog anti-image filter circuitry. For interlaced scanning case whose sample rate is 13.5MHz, four times oversampling provides the final output sampling rate as 54Msps (samples per second). For progressive scanning with double sample rate, 27MHz, OSF module performs two times oversampling with the result of also 54Msps.
The DAC has high frequency attenuation which comes from the sin(x)/x characteristic of sample-and-hold nature and can have more attenuation for some specific reasons. As OSF has enough number of taps with programmable coefficients, compensation of such attenuation is done by making the filter response to boost at high frequency.

OSF operates in different ways according to the oversampling ratio; the number of taps and the meanings of the coefficient registers are different for each case.

4x oversampling case: 13.5Msps interlaced mode. It operates as 4-polyphase 95-tap FIR filters. All the coefficient registers (SDO_OSFC00_0~SDO_OSFC23_0) are used.

2x oversampling case: 27Msps progressive mode. It operates as 2-polyphase 47-tap FIR filter. Half of the filter coefficient registers (SDO_OSFC12_0~SDO_OSFC23_0) are used. The remaining values should be set to zero.

The target filter should be a centre symmetric, that is,

Let h(i) a filter coefficient whose index is i.
N is odd number. (For 4x, N = 95 and for 2x, N=47)
h(i) = h(N-i) for i=0~[N/2]-1, where [] means rounding to the nearest integers towards zero.

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Table 7-4 Over-sampling Filter Coefficients Configuration

SDO Register Name(_0,1,2)	registers (_0, 1, 2)	4x Case meaning (N=95)	2x case meaning (N=47)	number of bits (Including Sign Bit)
SDO_OSFC00	osf_coef00	(h[0]+h[2])/2 = (h[94]+h[92])/2	0	8
	osf_coef01	h[1] = h[93]	0	8
SDO_OSFC01	osf_coef02	(h[0]-h[2])/2 = (h[94]–h[92])/2	0	8
	osf_coef03	h[3] = h[91]	0	8
SDO_OSFC02	osf_coef04	(h[4]+h[6])/2 = (h[90]+h[88])/2	0	8
	osf_coef05	h[5] = h[89]	0	8
SDO_OSFC03	osf_coef06	(h[4]-h[6])/2 = (h[90]–h[88])/2	0	8
	osf_coef07	h[7] = h[87]	0	8
SDO_OSFC04	osf_coef08	(h[8]+h[10])/2 = (h[86]+h[84])/2	0	8
	osf_coef09	h[9] = h[85]	0	8
SDO_OSFC05	osf_coef10	(h[8]-h[10])/2 = (h[86]-h[84])/2	0	8
	osf_coef11	h[11] = h[83]	0	8
SDO_OSFC06	osf_coef12	(h[12]+h[14])/2= (h[82]+h[80])/2	0	9
	osf_coef13	h[13] = h[81]	0	9
SDO_OSFC07	osf_coef14	(h[12]-h[14])/2= (h[82]-h[80])/2	0	9
	osf_coef15	h[15] = h[79]	0	9
SDO_OSFC08	osf_coef16	(h[16]+h[18])/2= (h[78]+h[76])/2	0	9
	osf_coef17	h[17] = h[77]	0	9
SDO_OSFC09	osf_coef18	(h[16]-h[18])/2 = (h[78]-h[76])/2	0	9
	osf_coef19	h[19] = h[75]	0	9
SDO_OSFC10	osf_coef20	(h[20]+h[22])/2 = (h[74]+h[72])/2	0	9
	osf_coef21	h[21] = h[73]	0	9
SDO_OSFC11	osf_coef22	(h[20]-h[22])/2 = (h[74]-h[72])/2	0	9
	osf_coef23	h[23] = h[71]	0	9
SDO_OSFC12	osf_coef24	(h[24]+h[26])/2 = (h[70]+h[68])/2	h[0] = h[46]	10
	osf_coef25	h[25] = h[69]	h[1] = h[45]	10
SDO_OSFC13	osf_coef26	(h[24]-h[26])/2 = (h[70]-h[68])/2	h[2] = h[44]	10
	osf_coef27	h[27] = h[67]	h[3] = h[43]	10
SDO_OSFC14	osf_coef28	(h[28]+h[30])/2 = (h[66]+h[64])/2	h[4] = h[42]	10
	osf_coef29	h[29] = h[65]	h[5] = h[41]	10
SDO_OSFC15	osf_coef30	(h[28]-h[30])/2 = (h[66]-h[64])/2	h[6] = h[40]	10

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SDO Register Name(_0,1,2)	registers (_0, 1, 2)	4x Case meaning (N=95)	2x case meaning (N=47)	number of bits (Including Sign Bit)
	osf_coef31	h[31] = h[63]	h[7] = h[39]	10
SDO_OSFC16	osf_coef32	(h[32]+h[34])/2 = (h[62]+h[60])/2	h[8] = h[38]	10
	osf_coef33	h[33] = h[61]	h[9] = h[37]	10
SDO_OSFC17	osf_coef34	(h[32]-h[34])/2 = (h[62]-h[60])/2	h[10] = h[36]	10
	osf_coef35	h[35] = h[59]	h[11] = h[35]	10
SDO_OSFC18	osf_coef36	(h[36]+h[38])/2 = (h[58]+h[56])/2	h[12] = h[34]	10
	osf_coef37	h[37] = h[57]	h[13] = h[33]	10
SDO_OSFC19	osf_coef38	(h[36]-h[38])/2 = (h[58]-h[56])/2	h[14] = h[32]	10
	osf_coef39	h[39] = h[55]	h[15] = h[31]	10
SDO_OSFC20	osf_coef40	(h[40]+h[42])/2 = (h[54]+h[52])/2	h[16] = h[30]	11
	osf_coef41	h[41] = h[53]	h[17] = h[29]	11
SDO_OSFC21	osf_coef42	(h[40]-h[42])/2 = (h[54]-h[52])/2	h[18] = h[28]	11
	osf_coef43	h[43] = h[51]	h[19] = h[27]	11
SDO_OSFC22	osf_coef44	(h[44]+h[46])/2 = (h[50]+h[48])/2	h[20] = h[26]	12
	osf_coef45	h[45] = h[49]	h[21] = h[25]	12
SDO_OSFC23	osf_coef46	(h[44]–h[46])/2 = (h[50]-h[48])/2	h[22] = h[24]	12
	osf_coef47	h[47]	h[23]	12

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7.10 REGISTER CONTROL (CTRL MODULE)

The TVOUT module supports AHB+ slave bus interface for register control. All the registers are synchronized with system bus clock.

7.11 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
XdacCOMP	Output	Compensation Pin. This is a compensation pin for the internal reference amplifier. A 0.1uF ceramic capacitor must be connected between COMP and 3.3V PWR.	XdacCOMP	Dedicated
XdacIREF	Input	Full Scale Adjust control. The full-scale current drive on each of the output channels is determined by the value of a resistor RSET connected between this terminal and GND.	XdacIREF	Dedicated
XdacVREF	Input	Voltage reference for DAC. An Internal voltage reference of nominally 1.22V is provided. Can be driven with an external reference source.	XdacVREF	Dedicated
XdacOUT	Output	DAC current output.	XdacOUT	Dedicated

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7.12 REGISTER DESCRIPTION

7.12.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
SDO_CLKCON	0xF900_0000	R/W	Clock Control Register	0x0000_0000
SDO_CONFIG	0xF900_0008	R/W	Video Standard Configuration Register	0x0024_2430
SDO_SCALE	0xF900_000C	R/W	Video Scale Configuration Register	0x0000_0006
SDO_VBI	0xF900_0014	R/W	VBI Configuration Register	0x0007_77FF
SDO_SCALE_CH0	0xF900_001C	R/W	Scale Control Register for DAC Channel0	0x0000_0800
SDO_YCDELAY	0xF900_0034	R/W	Video Delay Control Register	0x0000_FA00
SDO_SCHLOCK	0xF900_0038	R/W	SCH Phase Control Register	0x0000_0000
SDO_DAC	0xF900_003C	R/W	DAC Configuration Register	0x0000_0000
SDO_FINFO	0xF900_0040	R	Status Register	0x0000_0002
SDO_Y0	0xF900_0044	R/W	Y- AAF 1'st and 23'th Coefficient (AAF : Anti-Aliasing Filter)	0x0000_0000
SDO_Y1	0xF900_0048	R/W	Y- AAF 2'nd and 22'th Coefficient	0x0000_0000
SDO_Y2	0xF900_004C	R/W	Y- AAF 3'rd and 21'th Coefficient	0x0000_0000
SDO_Y3	0xF900_0050	R/W	Y- AAF 4'th and 20'th Coefficient	0x0000_0000
SDO_Y4	0xF900_0054	R/W	Y- AAF 5'th and 19'th Coefficient	0x0000_0000
SDO_Y5	0xF900_0058	R/W	Y- AAF 6'th and 18'th Coefficient	0x0000_0000
SDO_Y6	0xF900_005C	R/W	Y- AAF 7'th and 17'th Coefficient	0x0000_0000
SDO_Y7	0xF900_0060	R/W	Y- AAF 8'th and 16'th Coefficient	0x0000_0000
SDO_Y8	0xF900_0064	R/W	Y - AAF 9'th and 15'th Coefficient	0x0000_0000
SDO_Y9	0xF900_0068	R/W	Y- AAF 10'th and 14'th Coefficient	0x0000_0000
SDO_Y10	0xF900_006C	R/W	Y- AAF 11'th and 13'th Coefficient	0x0000_0000
SDO_Y11	0xF900_0070	R/W	Y- AAF 12'th Coefficient	0x0000_025D
SDO_CB0	0xF900_0080	R/W	CB- AAF 1'st and 23'th Coefficient	0x0000_0000
SDO_CB1	0xF900_0084	R/W	CB- AAF 2'nd and 22'th Coefficient	0x0000_0000
SDO_CB2	0xF900_0088	R/W	CB- AAF 3'rd and 21'th Coefficient	0x0000_0000
SDO_CB3	0xF900_008C	R/W	CB-AAF 4'th and 20'th Coefficient	0x0000_0000
SDO_CB4	0xF900_0090	R/W	CB- AAF 5'th and 19'th Coefficient	0x0000_0000
SDO_CB5	0xF900_0094	R/W	CB- AAF 6'th and 18'th Coefficient	0x0000_0001
SDO_CB6	0xF900_0098	R/W	CB- AAF 7'th and 17'th Coefficient	0x0000_0007
SDO_CB7	0xF900_009C	R/W	CB- AAF 8'th and 16'th Coefficient	0x0000_0014
SDO_CB8	0xF900_00A0	R/W	CB- AAF 9'th and 15'th Coefficient	0x0000_0028
SDO_CB9	0xF900_00A4	R/W	CB- AAF 10'th and 14'th Coefficient	0x0000_003F

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Register	Address	R/W	Description	Reset Value
SDO_CB10	0xF900_00A8	R/W	CB- AAF 11'th and 13'th Coefficient	0x0000_0052
SDO_CB11	0xF900_00AC	R/W	CB- AAF 12'th Coefficient	0x0000_005A
SDO_CR0	0xF900_00C0	R/W	CR- AAF 1'st and 23'th Coefficient	0x0000_0000
SDO_CR1	0xF900_00C4	R/W	CR- AAF 2'nd and 22'th Coefficient	0x0000_0000
SDO_CR2	0xF900_00C8	R/W	CR- AAF 3'rd and 21'th Coefficient	0x0000_0000
SDO_CR3	0xF900_00CC	R/W	CR-AAF 4'th and 20'th Coefficient	0x0000_0000
SDO_CR4	0xF900_00D0	R/W	CR- AAF 5'th and 19'th Coefficient	0x0000_0000
SDO_CR5	0xF900_00D4	R/W	CR- AAF 6'th and 18'th Coefficient	0x0000_0001
SDO_CR6	0xF900_00D8	R/W	CR- AAF 7'th and 17'th Coefficient	0x0000_0009
SDO_CR7	0xF900_00DC	R/W	CR- AAF 8'th and 16'th Coefficient	0x0000_001C
SDO_CR8	0xF900_00E0	R/W	CR- AAF 9'th and 15'th Coefficient	0x0000_0039
SDO_CR9	0xF900_00E4	R/W	CR- AAF 10'th and 14'th Coefficient	0x0000_005A
SDO_CR10	0xF900_00E8	R/W	CR- AAF 11'th and 13'th Coefficient	0x0000_0074
SDO_CR11	0xF900_00EC	R/W	CR- AAF 12'th Coefficient	0x0000_007E
SDO_CCCON	0xF900_0180	R/W	Color Compensation On/ Off Control	0x0000_0000
SDO_YSCALE	0xF900_0184	R/W	Brightness Control for Y	0x0080_0000
SDO_CBSCALE	0xF900_0188	R/W	Hue/ Saturation Control for CB	0x0080_0000
SDO_CRSCALE	0xF900_018C	R/W	Hue/ Saturation Control for CR	0x0000_0080
SDO_CB_CR_OFFSET	0xF900_0190	R/W	Hue/ Sat Offset Control for CB/CR	0x0000_0000
SDO_CVBS_CC_Y1	0xF900_0198	R/W	Color Compensation of CVBS Output	0x0200_0000
SDO_CVBS_CC_Y2	0xF900_019C	R/W	Color Compensation of CVBS Output	0x03FF_0200
SDO_CVBS_CC_C	0xF900_01A0	R/W	Color Compensation of CVBS Output	0x0000_01FF
SDO_OSFC00_0	0xF900_0200	R/W	OverSampling Filter (OSF) Coefficient 1 & 0. of channel #0	0x00FD_00FE
SDO_OSFC01_0	0xF900_0204	R/W	OSF Coefficient 3 & 2 of Channel #0	0x0000_0000
SDO_OSFC02_0	0xF900_0208	R/W	OSF Coefficient 5 & 4 of Channel #0	0x0005_0004
SDO_OSFC03_0	0xF900_020C	R/W	OSF Coefficient 7 & 6 of Channel #0	0x0000_00FF
SDO_OSFC04_0	0xF900_0210	R/W	OSF Coefficient 9 & 8 of Channel #0	0x00F7_00FA
SDO_OSFC05_0	0xF900_0214	R/W	OSF Coefficient 11 & 10 of Channel #0	0x0000_0001
SDO_OSFC06_0	0xF900_0218	R/W	OSF Coefficient 13 & 12 of Channel #0	0x000E_000A
SDO_OSFC07_0	0xF900_021C	R/W	OSF Coefficient 15 & 14 of Channel #0	0x0000_01FF
SDO_OSFC08_0	0xF900_0220	R/W	OSF Coefficient 17 & 16 of Channel #0	0x01EC_01F2
SDO_OSFC09_0	0xF900_0224	R/W	OSF Coefficient 19 & 18 of Channel #0	0x0000_0001
SDO_OSFC10_0	0xF900_0228	R/W	OSF Coefficient 21 & 20 of Channel #0	0x001D_0014
SDO_OSFC11_0	0xF900_022C	R/W	OSF Coefficient 23 & 22 of Channel #0	0x0000_01FE
SDO_OSFC12_0	0xF900_0230	R/W	OSF Coefficient 25 & 24 of Channel #0	0x03D8_03E4
SDO_OSFC13_0	0xF900_0234	R/W	OSF Coefficient 27 & 26 of Channel #0	0x0000_0002

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Register	Address	R/W	Description	Reset Value
SDO_OSFC14_0	0xF900_0238	R/W	OSF Coefficient 29 & 28 of Channel #0	0x0038_0028
SDO_OSFC15_0	0xF900_023C	R/W	OSF Coefficient 31 & 30 of Channel #0	0x0000_03FD
SDO_OSFC16_0	0xF900_0240	R/W	OSF Coefficient 33 & 32 of Channel #0	0x03B0_03C7
SDO_OSFC17_0	0xF900_0244	R/W	OSF Coefficient 35 & 34 of Channel #0	0x0000_0005
SDO_OSFC18_0	0xF900_0248	R/W	OSF Coefficient 37 & 36 of Channel #0	0x0079_0056
SDO_OSFC19_0	0xF900_024C	R/W	OSF Coefficient 39 & 38 of Channel #0	0x0000_03F6
SDO_OSFC20_0	0xF900_0250	R/W	OSF Coefficient 41 & 40 of Channel #0	0x072C_0766
SDO_OSFC21_0	0xF900_0254	R/W	OSF Coefficient 43 & 42 of Channel #0	0x0000_001B
SDO_OSFC22_0	0xF900_0258	R/W	OSF Coefficient 45 & 44 of Channel #0	0x028B_0265
SDO_OSFC23_0	0xF900_025C	R/W	OSF Coefficient 47 & 46 of Channel #0	0x0400_0ECC
SDO_XTALK0	0xF900_0260	R/W	Crosstalk Cancel Coefficient for Ch.0	0x0000_0000
SDO_BB_CTRL	0xF900_026C	R/W	Blackburst Test Control	0x0001_1A00
SDO_IRQ	0xF900_0280	R/W	Interrupt Request Register	0x0000_0000
SDO_IRQMASK	0xF900_0284	R/W	Interrupt Request Enable Register	0x0000_0000
Reserved	0xF900_02C0	R/W	Reserved	0x00FD_00FE
Reserved	0xF900_02C4	R/W	Reserved	0x0000_0000
Reserved	0xF900_02C8	R/W	Reserved	0x0005_0004
Reserved	0xF900_02CC	R/W	Reserved	0x0000_00FF
Reserved	0xF900_02D0	R/W	Reserved	0x00F7_00FA
Reserved	0xF900_02D4	R/W	Reserved	0x0000_0001
Reserved	0xF900_02D8	R/W	Reserved	0x000E_000A
Reserved	0xF900_02DC	R/W	Reserved	0x0000_01FF
Reserved	0xF900_02E0	R/W	Reserved	0x01EC_01F2
Reserved	0xF900_02E4	R/W	Reserved	0x0000_0001
Reserved	0xF900_02E8	R/W	Reserved	0x001D_0014
Reserved	0xF900_02EC	R/W	Reserved	0x0000_01FE
Reserved	0xF900_02F0	R/W	Reserved	0x03D8_03E4
Reserved	0xF900_02F4	R/W	Reserved	0x0000_0002
Reserved	0xF900_02F8	R/W	Reserved	0x0038_0028
Reserved	0xF900_02FC	R/W	Reserved	0x0000_03FD
Reserved	0xF900_0300	R/W	Reserved	0x03B0_03C7
Reserved	0xF900_0304	R/W	Reserved	0x0000_0005
Reserved	0xF900_0308	R/W	Reserved	0x0079_0056
Reserved	0xF900_030C	R/W	Reserved	0x0000_03F6
Reserved	0xF900_0310	R/W	Reserved	0x072C_0766
Reserved	0xF900_0314	R/W	Reserved	0x0000_001B
Reserved	0xF900_0318	R/W	Reserved	0x028B_0265

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Register	Address	R/W	Description	Reset Value
Reserved	0xF900_031C	R/W	Reserved	0x0400_0ECC
Reserved	0xF900_0320	R/W	Reserved	0x00FD_00FE
Reserved	0xF900_0324	R/W	Reserved	0x0000_0000
Reserved	0xF900_0328	R/W	Reserved	0x0005_0004
Reserved	0xF900_032C	R/W	Reserved	0x0000_00FF
Reserved	0xF900_0330	R/W	Reserved	0x00F7_00FA
Reserved	0xF900_0334	R/W	Reserved	0x0000_0001
Reserved	0xF900_0338	R/W	Reserved	0x000E_000A
Reserved	0xF900_033C	R/W	Reserved	0x0000_01FF
Reserved	0xF900_0340	R/W	Reserved	0x01EC_01F2
Reserved	0xF900_0344	R/W	Reserved	0x0000_0001
Reserved	0xF900_0348	R/W	Reserved	0x001D_0014
Reserved	0xF900_034C	R/W	Reserved	0x0000_01FE
Reserved	0xF900_0350	R/W	Reserved	0x03D8_03E4
Reserved	0xF900_0354	R/W	Reserved	0x0000_0002
Reserved	0xF900_0358	R/W	Reserved	0x0038_0028
Reserved	0xF900_035C	R/W	Reserved	0x0000_03FD
Reserved	0xF900_0360	R/W	Reserved	0x03B0_03C7
Reserved	0xF900_0364	R/W	Reserved	0x0000_0005
Reserved	0xF900_0368	R/W	Reserved	0x0079_0056
Reserved	0xF900_036C	R/W	Reserved	0x0000_03F6
Reserved	0xF900_0370	R/W	Reserved	0x072C_0766
Reserved	0xF900_0374	R/W	Reserved	0x0000_001B
Reserved	0xF900_0378	R/W	Reserved	0x028B_0265
Reserved	0xF900_037C	R/W	Reserved	0x0400_0ECC
SDO_ARMCC	0xF900_03C0	R/W	Closed Caption Data Register	0x0000_0000
SDO_ARMWSS525	0xF900_03C4	R/W	WSS 525 Data Register	0x0000_0000
SDO_ARMWSS625	0xF900_03C8	R/W	WSS 625 Data Register	0x0000_0000
SDO_ARMCGMS525	0xF900_03CC	R/W	CGMS-A 525 Data Register	0x0000_0000
SDO_ARMCGMS625	0xF900_03D4	R/W	CGMS-A 625 Data Register	0x0000_0000
SDO_VERSION	0xF900_03D8	R	TVOUT Version Number Read Register	0x0000_000C
Shadow Register Description				
SDO_CC	0xF900_0380	R/W	Closed Caption Data Shadow register	0x0000_0000
SDO_WSS525	0xF900_0384	R/W	WSS 525 Data Shadow Register	0x0000_0000
SDO_WSS625	0xF900_0388	R/W	WSS 625 Data Shadow Register	0x0000_0000
SDO_CGMS525	0xF900_038C	R/W	CGMS-A 525 Data Shadow Register	0x0000_0000

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Register	Address	R/W	Description	Reset Value
SDO_CGMS625	0xF900_0394	R/W	CGMS-A 625 Data Shadow Register	0x0000_0000

NOTE: SDO_ARMCC, SDO_ARMWSS525, SDO_ARMWSS625, SDO_ARMCGMS525, and SDO_ ARMCGMS625 are paired with above shadow registers, respectively, as follows:

- SDO_ARMCC : SDO_CC
- SDO_ARMWSS525 : SDO_WSS525
- SDO_ARMWSS625 : SDO_WSS625
- SDO_ARMCGMS525: SDO_CGMS525
- SDO_ARMCGMS625: SDO_CGMS625

If MCU set values in the source registers with the prefix of SDO_ARMXXX, they are not immediately effective. But the values are copied into the corresponding shadow registers which are named with SDO_XXX. They are effective at the next vertical sync. Then the values become effective during VBI interval at the next field.

Avoid setting direct value to these shadow registers.

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7.12.1.1 SDO Clock Control Register (SDO_CLKCON, R/W, Address = 0xF900_0000)

SDO_CLKCON	Bit	Description	Reset Value
Reserved	[31:5]	Reserved, read as zero, do not modify	0
SDO software reset	[4]	This bit controls software reset of TVOUT. Software reset is active high signal. 0 = No reset 1 = Enables software reset	0
Reserved	[3:2]	Reserved, read as zero, do not modify	
SDO clock down ready (read only)	[1]	Indicates whether host controller can stop the clock for the TVOUT. 0 = Clock-down not ready 1 = Clock-down ready Normally this bit is 0. After SDO_CLKCON [0] bit is 0, if the internal line counter and pixel counter are 0 (just before starting line 1), this bit will be 1.	0
SDO clock on	[0]	This bit determines run/ stop mode of TVOUT. 0 = TVOUT clock off. TVOUT requests for clock down to host controller. If SDO is ready for clock down, SDO_CLKCON [1] bit will be 1. The host controller should stop the clock for the TVOUT after that. 1 = TVOUT clock on. TVOUT starts running. NOTE: Vertical Sync of TVENC's Timing Generator updates the SFRs of Video Processor and Image Mixer. Thus, SFRs are configured before this bit is enabled. The sequence to enable TVSS is as follows: "VP -> MIXER -> TVENC". Also, because of the same reason, the disabling sequence is following as : "VP -> MIXER -> TVNEC".	0

Image Mixer transmits video data to TVENC. To connect Image Mixer and TVENC you must configure REG_DST_SEL at mixer_CFG register (0xF920_ 0004. To synchronous between Image Mixer and TVENC you must configure Image Mixer I/F clock (VCLKHS) and VCLKS (TVENC clock) (fixed by 54MHz). Thus, you must set MIXER_SEL register in CLK_SRC1(0xE010_0204). For more information, refer to CMU chapter.

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7.12.1.2 SDO Video Standard Configuration Register (SDO_CONFIG, R/W, Address = 0xF900_0008)

SDO_CONFIG	Bit	Description	Initial State
Reserved	[31:22]	Reserved, read as zero, do not modify	0
Reserved	[21:20]	Reserved, read as zero, do not modify	2
Reserved	[19:18]	Reserved, read as zero, do not modify	1
Reserved	[17:16]	Reserved, read as zero, do not modify	0
Reserved	[15:14]	Reserved, read as zero, do not modify	0
Reserved	[13:12]	Reserved, read as zero, do not modify	2
Reserved	[11:10]	Reserved, read as zero, do not modify	1
Selection of Video Mux for DAC	[9:8]	0 = CVBS signal 1 = Y signal 2 = C signal	0
Reserved	[7]	Reserved, read as zero, do not modify	0
Reserved	[6]	Reserved, read as zero, do not modify	0
Reserved	[5]	Reserved, read as zero, do not modify	1
Reserved	[4]	Reserved, read as zero, do not modify	1
Selection of Video Standard	[3:0]	0 = NTSC (M) 1 = PAL (M) 2 = PAL (BGHID) 3 = PAL (N) 4 = PAL (Nc) 8 = NTSC 4.43 9 = PAL 60	0

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7.12.1.3 SDO Video Scale Configuration Register (SDO_SCALE, R/W, Address = 0xF900_000C)

SDO_SCALE	Bit	Description	Initial State
Reserved	[31:4]	Reserved, read as zero, do not modify	0
Reserved	[3]	Reserved, read as zero, do not modify	0
Reserved	[2]	Reserved, read as zero, do not modify	1
Setup Level Selection for Composite	[1]	0 = 0 IRE 1 = 7.5 IRE This setting is valid if bit[6] of SDO_CONFIG register is set to composite.	1
Video-to-Sync Ratio Selection for Composite	[0]	0 = 10:4 1 = 7:3 This setting is valid if bit[6] of SDO_CONFIG register is set to composite.	0

NOTE: The Table 7-5 and Table 7-6 according to the value of bit [3:2]

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7.12.1.4 SDO VBI Configuration Register (SDO_VBI, R/W, Address = 0xF900_0014)

SDO_VBI	Bit	Description	Initial State
Reserved	[31:15]	Reserved, read as zero, do not modify	E
Wide Screen Signaling Configuration for CVBS Channel	[14]	If the Selection of Video Standard in SDO_CONFIG Register is set to NTSC (M), PAL (M), PAL 60, or NTSC 4.43, 0 = No Ancillary Data Insertion 1 = 525 line WSS Insertion at 20H and 283H Otherwise, 0 = No Ancillary Data Insertion 1 = 625 line WSS Insertion at 23H This setting is valid if the bit [6] of SDO_CONFIG register is set to composite	1
Closed Caption Configuration for CVBS Channel	[13:12]	If the Selection of Video Standard in SDO_CONFIG Register is set to NTSC (M), PAL (M), PAL 60, or NTSC 4.43, 0 = No Ancillary Data Insertion 1 = US Closed Caption Insertion at 21H 2 = US Closed Caption Insertion at 21H and 284H 3 = Reserved for Other Use Otherwise, No Ancillary Data Insertion. (NOTE) This setting is valid if the bit [6] of SDO_CONFIG register is set to composite. Note: European closed caption is not supported.	3
Reserved	[11]	Reserved, read as zero, do not modify	0
Reserved	[10]	Reserved, read as zero, do not modify	1
Reserved	[9:8]	Reserved, read as zero, do not modify	3
Reserved	[7]	Reserved, read as zero, do not modify	1
Reserved	[6]	Reserved, read as zero, do not modify	1
Reserved	[5:4]	Reserved, read as zero, do not modify	3
Reserved	[3]	Reserved, read as zero, do not modify	1
Reserved	[2]	Reserved, read as zero, do not modify	1
Reserved	[1:0]	Reserved, read as zero, do not modify	3

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7.12.1.5 SDO Channel #0 Scale Control Register (SDO_SCALE_CH0, R/W, Address = 0xF900_001C)

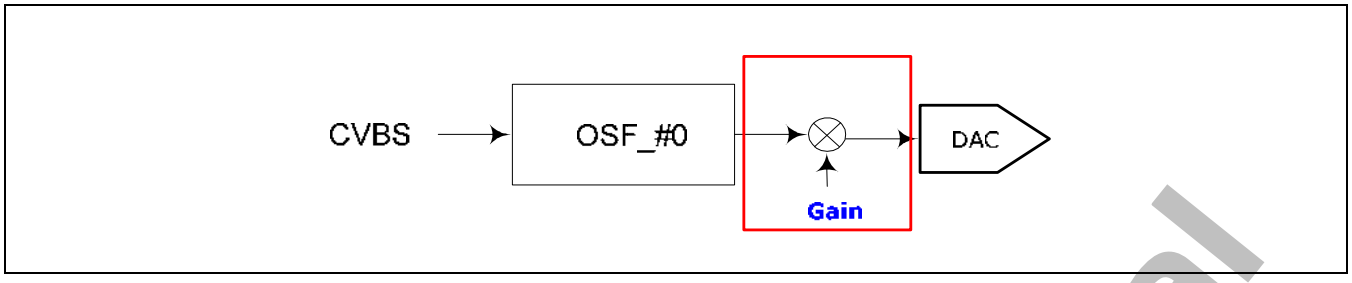

Figure 7-16 Individual Gain & Offset Control for DAC Channel Balancing

SDO_SCALE_CH0	Bit	Description	Initial State
Reserved	[31:26]	Reserved, read as zero, do not modify	0
Offset of Channel 0 Signal Scale Conversion	[25:16]	Function F(x) = (X+Offset) * Gain 0x1FF = +511 … 0x001 = +1 0x000 = 0 0x3FF = -1 … 0x200 = -512 This setting is valid if the bit [6] of SDO_CONFIG register is set to component.	000
Reserved	[15:12]	Reserved, read as zero, do not modify	0
Gain of Channel 0 Signal Scale Conversion	[11:0]	Function F(x) = (X+Offset) * Gain 0x000 = x0.0 … 0x400 = x0.5 … 0x800 = x1.0 … 0xC00 = x1.5 … 0xFFF = x1.999512, (2048*2 – 1)/2048 This setting is valid if the bit [6] of SDO_CONFIG register is set to component.	800

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7.12.1.6 SDO Video Delay Control Register (SDO_YCDELAY, R/W, Address = 0xF900_0034)

SDO_YCDELAY	Bit	Description	Initial State
Reserved	[31:20]	Reserved, read as zero, do not modify	0
Delay of Y Signal with Respect to C Signal	[19:16]	0x0 = 0.000 usec 0x1 = 0.074 usec … 0xF = 1.111 usec	0
Offset of Video Active Start Position	[15:8]	0x3F = +4.667 usec … 0x01 = +0.074 usec 0x00 = 0.000 usec 0xFF = -0.074 usec … 0x40 = -4.741 usec	FA
Offset of Video Active End Position	[7:0]	0x3F = +4.667 usec … 0x01 = +0.074 usec 0x00 = 0.000 usec 0xFF = -0.074 usec … 0x40 = -4.741 usec	00

7.12.1.7 SDO SCH Phase Control Register (SDO_SCHLOCK, R/W, Address = 0xF900_0038)

SDO_SCHLOCK	Bit	Description	Initial State
Reserved	[31:1]	Reserved, read as zero, do not modify	0
Color Sub-Carrier Phase Adjustment	[0]	0 = Never adjusted 1 = Every field is adjusted such that color sub-carrier frequency and horizontal frequency are locked to each other.	0

7.12.1.8 SDO DAC Configuration Register (SDO_DAC, R/W, Address = 0xF900_003C)

SDO_DAC	Bit	Description	Initial State
Reserved	[31:1]	Reserved, read as zero, do not modify	0
Power Down for DAC	[0]	0 = DAC power down 1 = DAC power on	0

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7.12.1.9 SDO Status Register (SDO_FINFO, R, Address = 0xF900_0040)

SDO_FINFO	Bit	Description	Initial State
Reserved	[31:26]	Reserved, read as zero, do not modify	0
Field Counter Modulo 1001	[25:16]	This counter is used for 59.94/60.0 Hz field rate conversion.	0
Reserved	[15:2]	Reserved, read as zero, do not modify	0
Field ID	[1]	0 = Top field 1 = Bottom field	1
Field ID with Progressive/ Interlaced Indication	[0]	If the SDO_CONFIG register is set to interlaced, 0 = Top field 1 = Bottom field. If the SDO_CONFIG register is set to progressive, this bit would be fixed to zero	0

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7.12.1.10 SDO Anti-Aliasing Filter Coefficients (SDO_Y0, R/W, Address = 0xF900_0044)
7.12.1.11 SDO Anti-Aliasing Filter Coefficients (SDO_Y1, R/W, Address = 0xF900_0048)
7.12.1.12 SDO Anti-Aliasing Filter Coefficients (SDO_Y2, R/W, Address = 0xF900_004C)
7.12.1.13 SDO Anti-Aliasing Filter Coefficients (SDO_Y3, R/W, Address = 0xF900_0050)
7.12.1.14 SDO Anti-Aliasing Filter Coefficients (SDO_Y4, R/W, Address = 0xF900_0054)
7.12.1.15 SDO Anti-Aliasing Filter Coefficients (SDO_Y5, R/W, Address = 0xF900_0058)
7.12.1.16 SDO Anti-Aliasing Filter Coefficients (SDO_Y6, R/W, Address = 0xF900_005C)
7.12.1.17 SDO Anti-Aliasing Filter Coefficients (SDO_Y7, R/W, Address = 0xF900_0060)
7.12.1.18 SDO Anti-Aliasing Filter Coefficients (SDO_Y8, R/W, Address = 0xF900_0064)
7.12.1.19 SDO Anti-Aliasing Filter Coefficients (SDO_Y9, R/W, Address = 0xF900_0068)
7.12.1.20 SDO Anti-Aliasing Filter Coefficients (SDO_Y10, R/W, Address = 0xF900_006C)
7.12.1.21 SDO Anti-Aliasing Filter Coefficients (SDO_Y11, R/W, Address = 0xF900_0070)
7.12.1.22 SDO Anti-Aliasing Filter Coefficients (SDO_CB0, R/W, Address = 0xF900_0080)
7.12.1.23 SDO Anti-Aliasing Filter Coefficients (SDO_CB1, R/W, Address = 0xF900_0084)
7.12.1.24 SDO Anti-Aliasing Filter Coefficients (SDO_CB2, R/W, Address = 0xF900_0088)
7.12.1.25 SDO Anti-Aliasing Filter Coefficients (SDO_CB3, R/W, Address = 0xF900_008C)
7.12.1.26 SDO Anti-Aliasing Filter Coefficients (SDO_CB4, R/W, Address = 0xF900_0090)
7.12.1.27 SDO Anti-Aliasing Filter Coefficients (SDO_CB5, R/W, Address = 0xF900_0094)
7.12.1.28 SDO Anti-Aliasing Filter Coefficients (SDO_CB6, R/W, Address = 0xF900_0098)
7.12.1.29 SDO Anti-Aliasing Filter Coefficients (SDO_CB7, R/W, Address = 0xF900_009C)
7.12.1.30 SDO Anti-Aliasing Filter Coefficients (SDO_CB8, R/W, Address = 0xF900_00A0)
7.12.1.31 SDO Anti-Aliasing Filter Coefficients (SDO_CB9, R/W, Address = 0xF900_00A4)
7.12.1.32 SDO Anti-Aliasing Filter Coefficients (SDO_CB10, R/W, Address = 0xF900_00A8)
7.12.1.33 SDO Anti-Aliasing Filter Coefficients (SDO_CB11, R/W, Address = 0xF900_00AC)
7.12.1.34 SDO Anti-Aliasing Filter Coefficients (SDO_CR0, R/W, Address = 0xF900_00C0)
7.12.1.35 SDO Anti-Aliasing Filter Coefficients (SDO_CR1, R/W, Address = 0xF900_00C4)
7.12.1.36 SDO Anti-Aliasing Filter Coefficients (SDO_CR2, R/W, Address = 0xF900_00C8)
7.12.1.37 SDO Anti-Aliasing Filter Coefficients (SDO_CR3, R/W, Address = 0xF900_00CC)
7.12.1.38 SDO Anti-Aliasing Filter Coefficients (SDO_CR4, R/W, Address = 0xF900_00D0)
7.12.1.39 SDO Anti-Aliasing Filter Coefficients (SDO_CR5, R/W, Address = 0xF900_00D4)
7.12.1.40 SDO Anti-Aliasing Filter Coefficients (SDO_CR6, R/W, Address = 0xF900_00D8)
7.12.1.41 SDO Anti-Aliasing Filter Coefficients (SDO_CR7, R/W, Address = 0xF900_00DC)
7.12.1.42 SDO Anti-Aliasing Filter Coefficients (SDO_CR8, R/W, Address = 0xF900_00E0)
7.12.1.43 SDO Anti-Aliasing Filter Coefficients (SDO_CR9, R/W, Address = 0xF900_00E4)
7.12.1.44 SDO Anti-Aliasing Filter Coefficients (SDO_CR10, R/W, Address = 0xF900_00E8)
7.12.1.45 SDO Anti-Aliasing Filter Coefficients (SDO_CR11, R/W, Address = 0xF900_00EC)

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SDO_Yn / SDO_CBn / SDO_CRn	Bit	Description	Initial State
Reserved	[31:11]	Reserved, read as zero, do not modify	0
11 Bit Signed Filter Coefficients	[10:0]	Setting values of anti-aliasing filter coefficients is constrained in such a way that total sum of filter coefficients should be equal to a predefined constant. Otherwise, DC component of filter output would be re-scaled from the original one. The value of the constant depends on the setting of SDO_SCALE register :for Y channel, 0x251, at 7.5 IRE setup and 7:3 ratio 0x25D, at 7.5 IRE setup and 10:4 ratio 0x281, at 0 IRE setup and 7:3 ratio 0x28F, at 0 IRE setup and 7:3 ratio,for CB channel, 0x1F3, at 7.5 IRE setup and 7:3 ratio 0x200, at 7.5 IRE setup and 10:4 ratio 0x21E, at 0 IRE setup and 7:3 ratio 0x228, at 0 IRE setup and 7:3 ratio, and for CR channel, 0x2C0, at 7.5 IRE setup and 7:3 ratio 0x2D1, at 7.5 IRE setup and 10:4 ratio 0x2C0, at 0 IRE setup and 7:3 ratio 0x30D, at 0 IRE setup and 7:3 ratio. This setting is valid if the bit [6] of SDO_CONFIG register is set to composite. The setting of Y Filter is applied only to CVBS output.	The reset values are set for the case of ITU-R BT.470 compliant NTSC signal which has 7.5 IRE setup and 10:4 video-to-sync ratio. Refer to “1.15 RESISTERS DESCRIPTION”.

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7.12.1.46 SDO Color Compensation On/Off Control (SDO_CCCON, R/W, Address = 0xF900_0180)

SDO_CCCON	Bit	Description	Initial State
Reserved	[31:5]	Reserved, read as zero, do not modify	0
On/Off Control of Brightness/ Hue/Saturation Adjustment	[4]	0 = On 1 = Bypass This setting enables/ disables the brightness/ hue/ saturation controls which are controlled by SDO_YSCALE, SDO_CBSCALE, and SDO_CRSCALE.	0
Reserved	[3]	Reserved, read as zero, do not modify	0
Reserved	[2]	Reserved, read as zero, do not modify	0
Reserved	[1]	Reserved, read as zero, do not modify	0
On/Off Control of CVBS Color Compensation	[0]	0 = On 1 = Bypass The CVBS color compensation imposes a saturation operation on the CVBS data. Values which exceed DAC conversion range 0~1023, in 10 bit resolution, would be saturated.	0

7.12.1.47 SDO Brightness Control for Y (SDO_YSCALE, R/W, Address = 0xF900_0184)

SDO_YSCALE	Bit	Description	Initial State
Reserved	[31:24]	Reserved, read as zero, do not modify	0
Gain of Brightness Control with	[23:16]	F(Y) = Gain * Y + Offset 0x00 = 0.0 … 0x80 = 1.0 … 0xFF = 1.992188, (128*2 – 1)/128 This setting is valid for all the CVBS/Y/C/YpbPr/RGB outputs.	80
Reserved	[15:9]	Reserved, read as zero, do not modify	0
Offset of Brightness Control with	[8:0]	F(Y) = Gain * Y + Offset 0x0FF = +255 … 0x001 = +1 0x000 = 0 0x1FF = -1 … 0x100 = -256 This setting is valid for all the CVBS/Y/C/YpbPr/RGB outputs.	00

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7.12.1.48 SDO Hue/Saturation Control for CB (SDO_CBSCALE, R/W, Address = 0xF900_0188)

SDO_CBSCALE	Bit	Description	Initial State
Reserved	[31:25]	Reserved, read as zero, do not modify	0
Gain0_CB	[24:16]	Gain0 of Hue/Saturation Control of CB with F(CB,CR) = CB * Gain0 + CR * Gain1 + Offset 0x0FF = 1.992188, (128*2 – 1)/128 … 0x080 = 1.0 … 0x000 = 0.0 … 0x180 = -1.0 … 0x100 = -2.0 This setting is valid for all the CVBS/Y/C/YpbPr/RGB outputs.	80
Reserved	[15:9]	Reserved, read as zero, do not modify	0
Gain1_CB	[8:0]	Gain1 of Hue/Saturation Control of CB with F(CB,CR) = CB * Gain0 + CR * Gain1 + Offset 0x0FF = 1.992188, (128*2 – 1)/128 … 0x080 = 1.0 … 0x000 = 0.0 … 0x180 = -1.0 … 0x100 = -2.0 This setting is valid for all the CVBS/Y/C/YpbPr/RGB outputs.	00

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7.12.1.49 SDO Hue/Saturation Control for CR (SDO_CRSCALE, R/W, Address = 0xF900_018C)

SDO_CRSCALE	Bit	Description	Initial State
Reserved	[31:25]	Reserved, read as zero, do not modify	0
Gain0_CR	[24:16]	Gain0 of Hue/Saturation Control of CR with F(CB,CR) = CB * Gain0 + CR * Gain1 + Offset 0x0FF = 1.992188, (128*2 – 1)/128 … 0x080 = 1.0 … 0x000 = 0.0 … 0x180 = -1.0 … 0x100 = -2.0 This setting is valid for all the CVBS/Y/C/YpbPr/RGB outputs.	00
Reserved	[15:9]	Reserved, read as zero, do not modify	0
Gain1_CR	[8:0]	Gain1 of Hue/Saturation Control of CR with F(CB,CR) = CB * Gain0 + CR * Gain1 + Offset 0x0FF = 1.992188, (128*2 – 1)/128 … 0x080 = 1.0 … 0x000 = 0.0 … 0x180 = -1.0 … 0x100 = -2.0 This setting is valid for all the CVBS/Y/C/YpbPr/RGB outputs.	80

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7.12.1.50 SDO Hue/Saturation Control for CB/CR (SDO_CB_CR_OFFSET, R/W, Address = 0xF900_0190)

SDO_CB_CR_OFFSET	Bit	Description	Initial State
Reserved	[31:26]	Reserved, read as zero, do not modify	0
Offset_CR	[25:16]	Offset of Hue/Saturation Control of CR with 0x1FF = +511 … 0x001 = +1 0x000 = 0 0x3FF = -1 … 0x200 = -512 This setting is valid for all the CVBS/Y/C/YpbPr/RGB outputs.	00
Reserved	[15:10]	Reserved, read as zero, do not modify	0
Offset_CB	[9:0]	Offset of Hue/Saturation Control of CB with 0x1FF = +511 … 0x001 = +1 0x000 = 0 0x3FF = -1 … 0x200 = -512 This setting is valid for all the CVBS/Y/C/YpbPr/RGB outputs.	00

7.12.1.51 Color Compensation Control Register for CVBS Output (SDO_CVBS_CC_Y1, R/W, Address = 0xF900_0198)

SDO_CVBS_CC_Y1	Bit	Description	Initial State
Reserved	[31:26]	Reserved, read as zero, do not modify	0
Y_Lower_Mid_CVBS_Corn	[25:16]	Lower Mid Y Boundary of Legal CVBS Corn 0x3FF = 1023 … 0x000 = 0	200
Reserved	[15:10]	Reserved, read as zero, do not modify	0
Y_Bottom_CVBS_Corn	[9:0]	Bottom Y Boundary of Legal CVBS Corn 0x3FF = 1023 … 0x000 = 0	000

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7.12.1.52 Color Compensation Control Register for CVBS Output (SDO_CVBS_CC_Y2, R/W, Address = 0xF900_019C)

SDO_CVBS_CC_Y2	Bit	Description	Initial State
Reserved	[31:26]	Reserved, read as zero, do not modify	0
Y_Top_CVBS_Corn	[25:16]	Top Y Boundary of Legal CVBS Corn 0x3FF = 1023 … 0x000 = 0	3FF
-	[15:10]	Reserved, read as zero, do not modify	0
Y_Upper_Mid_CVBS_Corn	[9:0]	Upper mid Y Boundary of Legal CVBS Corn 0x3FF = 1023 … 0x000 = 0	200

7.12.1.53 Color Compensation Control Register for CVBS Output (SDO_CVBS_CC_C, R/W, Address = 0xF900_01A0)

SDO_CVBS_CC_C	Bit	Description	Initial State
Reserved	[31:9]	Reserved, read as zero, do not modify	0
Radius_CVBS_Corn	[8:0]	Radius of Legal CVBS Corn 0x1FF = 511 … 0x000 = 0	1FF
It should be set such that Y_Top_CVBS_Corn >= Y_Upper_Mid_CVBS_Corn >= Y_Lower_Mid_CVBS_Corn >= Y_Bottom_CVBS_Corn. It is highly recommended for users not to alter their reset values. This setting is valid if SDO_CCCON [0] is set to 'On'.			

7.12.1.54 SDO 525 Line Component Front/Back Porch Position Control Register (SDO_CSC_525_PORCH, R/W, Address = 0xF900_01B0)

SDO_CSC_525_PORCH	Bit	Description	Initial State
Reserved	[31:26]	Reserved, read as zero, do not modify	0
525 line back-porch position	[25:16]	Back-porch start position	8A
Reserved	[15:10]	Reserved, read as zero, do not modify	0
525 line front-porch position	[9:0]	Front-porch start position	359
- Resolution in progressive: 1/27MHz, - resolution in interlaced: 1/13.5MHz - Compare line count value with porch position			

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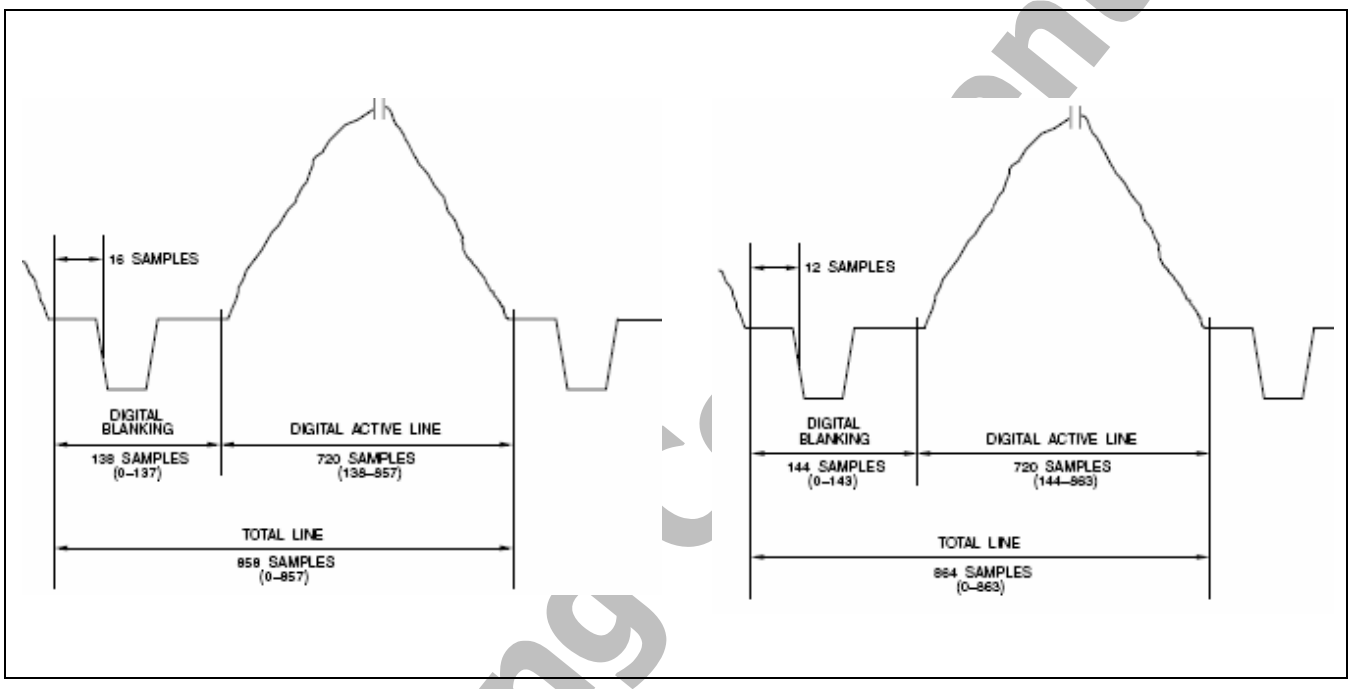
7.12.1.55 SDO 625 Line Component Front/Back Porch Position Control Resigter(SDO_CSC_625_PORCH, R/W, Address = 0xF900_01B4)

SDO_CSC_625_PORCH	Bit	Description	Initial State
Reserved	[31:26]	Reserved, read as zero, do not modify	0
625 line back-porch position	[25:16]	Back-porch start position	96
Reserved	[15:10]	Reserved, read as zero, do not modify	0
625 line front-porch position	[9:0]	Front-porch start position	35C
- Resolution in progressive : 1/27MHz, - resolution in interlaced : 1/13.5MHz - Compare line count value with porch position			



* One Line Count Value of 525 Line

* One Line Count Value of 625 Line

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7.12.1.56 SDO Oversampling #0 Filter Coefficient (SDO_OSFC00_0, R/W, Address = 0xF900_0200)

SDO_OSFCN_0 (N is 00~23)	Bit	Description	Initial State
osf_coef(2xN+1)	[23:16]~ [27:16]	(2xN+1)'th oversampling filter coefficient. Signed 8~12bit integer. Actual value is osf_coef/(210)	Refer to below table
osf_coef(2xN)	[7:0] ~[11:0]	(2xN)'th oversampling filter coefficient. Signed 8~12bit integer. Actual value is osf_coef/(210)	

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7.12.1.57 SDO Oversampling #0 Filter Coefficient (SDO_OSFC01_0, R/W, Address = 0xF900_0204)
7.12.1.58 SDO Oversampling #0 Filter Coefficient (SDO_OSFC02_0, R/W, Address = 0xF900_0208)
7.12.1.59 SDO Oversampling #0 Filter Coefficient (SDO_OSFC03_0, R/W, Address = 0xF900_020C)
7.12.1.60 SDO Oversampling #0 Filter Coefficient (SDO_OSFC04_0, R/W, Address = 0xF900_0210)
7.12.1.61 SDO Oversampling #0 Filter Coefficient (SDO_OSFC05_0, R/W, Address = 0xF900_0214)
7.12.1.62 SDO Oversampling #0 Filter Coefficient (SDO_OSFC06_0, R/W, Address = 0xF900_0218)
7.12.1.63 SDO Oversampling #0 Filter Coefficient (SDO_OSFC07_0, R/W, Address = 0xF900_021C)
7.12.1.64 SDO Oversampling #0 Filter Coefficient (SDO_OSFC08_0, R/W, Address = 0xF900_0220)
7.12.1.65 SDO Oversampling #0 Filter Coefficient (SDO_OSFC09_0, R/W, Address = 0xF900_0224)
7.12.1.66 SDO Oversampling #0 Filter Coefficient (SDO_OSFC10_0, R/W, Address = 0xF900_0228)
7.12.1.67 SDO Oversampling #0 Filter Coefficient (SDO_OSFC11_0, R/W, Address = 0xF900_022C)
7.12.1.68 SDO Oversampling #0 Filter Coefficient (SDO_OSFC12_0, R/W, Address = 0xF900_0230)
7.12.1.69 SDO Oversampling #0 Filter Coefficient (SDO_OSFC13_0, R/W, Address = 0xF900_0234)
7.12.1.70 SDO Oversampling #0 Filter Coefficient (SDO_OSFC14_0, R/W, Address = 0xF900_0238)
7.12.1.71 SDO Oversampling #0 Filter Coefficient (SDO_OSFC15_0, R/W, Address = 0xF900_023C)
7.12.1.72 SDO Oversampling #0 Filter Coefficient (SDO_OSFC16_0, R/W, Address = 0xF900_0240)
7.12.1.73 SDO Oversampling #0 Filter Coefficient (SDO_OSFC17_0, R/W, Address = 0xF900_0244)
7.12.1.74 SDO Oversampling #0 Filter Coefficient (SDO_OSFC18_0, R/W, Address = 0xF900_0248)
7.12.1.75 SDO Oversampling #0 Filter Coefficient (SDO_OSFC19_0, R/W, Address = 0xF900_024C)
7.12.1.76 SDO Oversampling #0 Filter Coefficient (SDO_OSFC20_0, R/W, Address = 0xF900_0250)
7.12.1.77 SDO Oversampling #0 Filter Coefficient (SDO_OSFC21_0, R/W, Address = 0xF900_0254)
7.12.1.78 SDO Oversampling #0 Filter Coefficient (SDO_OSFC22_0, R/W, Address = 0xF900_0258)
7.12.1.79 SDO Oversampling #0 Filter Coefficient (SDO_OSFC23_0, R/W, Address = 0xF900_025C)

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7.12.1.80 SDO Oversampling #1 Filter Coefficient (SDO_OSFC00_1, R/W, Address = 0xF900_ 02C0)

SDO_OSFCN_1 (N is 00~23)	Bit	Description	Initial State
osf_coef(2xN+1)	[23:16]~[27:16]	(2xN+1)'th oversampling filter coefficient. Signed 8~12bit integer. Actual value is osf_coef/(210)	Refer to below table
osf_coef(2xN)	[7:0] ~[11:0]	(2xN)'th oversampling filter coefficient. Signed 8~12bit integer. Actual value is osf_coef/(210)	

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7.12.1.81 SDO Oversampling #1 Filter Coefficient (SDO_OSFC01_1, R/W, Address = 0xF900_02C4)
7.12.1.82 SDO Oversampling #1 Filter Coefficient (SDO_OSFC02_1, R/W, Address = 0xF900_02C8)
7.12.1.83 SDO Oversampling #1 Filter Coefficient (SDO_OSFC03_1, R/W, Address = 0xF900_02CC)
7.12.1.84 SDO Oversampling #1 Filter Coefficient (SDO_OSFC04_1, R/W, Address = 0xF900_02D0)
7.12.1.85 SDO Oversampling #1 Filter Coefficient (SDO_OSFC05_1, R/W, Address = 0xF900_02D4)
7.12.1.86 SDO Oversampling #1 Filter Coefficient (SDO_OSFC06_1, R/W, Address = 0xF900_02D8)
7.12.1.87 SDO Oversampling #1 Filter Coefficient (SDO_OSFC07_1, R/W, Address = 0xF900_02DC)
7.12.1.88 SDO Oversampling #1 Filter Coefficient (SDO_OSFC08_1, R/W, Address = 0xF900_02E0)
7.12.1.89 SDO Oversampling #1 Filter Coefficient (SDO_OSFC09_1, R/W, Address = 0xF900_02E4)
7.12.1.90 SDO Oversampling #1 Filter Coefficient (SDO_OSFC10_1, R/W, Address = 0xF900_02E8)
7.12.1.91 SDO Oversampling #1 Filter Coefficient (SDO_OSFC11_1, R/W, Address = 0xF900_02EC)
7.12.1.92 SDO Oversampling #1 Filter Coefficient (SDO_OSFC12_1, R/W, Address = 0xF900_02F0)
7.12.1.93 SDO Oversampling #1 Filter Coefficient (SDO_OSFC13_1, R/W, Address = 0xF900_02F4)
7.12.1.94 SDO Oversampling #1 Filter Coefficient (SDO_OSFC14_1, R/W, Address = 0xF900_02F8)
7.12.1.95 SDO Oversampling #1 Filter Coefficient (SDO_OSFC15_1, R/W, Address = 0xF900_02FC)
7.12.1.96 SDO Oversampling #1 Filter Coefficient (SDO_OSFC16_1, R/W, Address = 0xF900_0300)
7.12.1.97 SDO Oversampling #1 Filter Coefficient (SDO_OSFC17_1, R/W, Address = 0xF900_0304)
7.12.1.98 SDO Oversampling #1 Filter Coefficient (SDO_OSFC18_1, R/W, Address = 0xF900_0308)
7.12.1.99 SDO Oversampling #1 Filter Coefficient (SDO_OSFC19_1, R/W, Address = 0xF900_030C)
7.12.1.100 SDO Oversampling #1 Filter Coefficient (SDO_OSFC20_1, R/W, Address = 0xF900_0310)
7.12.1.101 SDO Oversampling #1 Filter Coefficient (SDO_OSFC21_1, R/W, Address = 0xF900_0314)
7.12.1.102 SDO Oversampling #1 Filter Coefficient (SDO_OSFC22_1, R/W, Address = 0xF900_0318)
7.12.1.103 SDO Oversampling #1 Filter Coefficient (SDO_OSFC23_1, R/W, Address = 0xF900_031C)

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7.12.1.104 SDO Oversampling #2 filter coefficient (SDO_OSFC00_2, R/W, Address = 0xF900_ 0320)

SDO_OSFCN_2 (N is 00~23)	Bit	Description	Reset Value
osf_coef(2xN+1)	[23:16]~[27:16]	(2xN+1)'th oversampling filter coefficient. Signed 8~12bit integer. Actual value is osf_coef/(210)	Refer to below table
osf_coef(2xN)	[7:0] ~[11:0]	(2xN)'th oversampling filter coefficient. Signed 8~12bit integer. Actual value is osf_coef/(210)	

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7.12.1.105 SDO Oversampling #2 Filter Coefficient (SDO_OSFC01_2, R/W, Address = 0xF900_0324)
7.12.1.106 SDO Oversampling #2 Filter Coefficient (SDO_OSFC02_2, R/W, Address = 0xF900_0328)
7.12.1.107 SDO Oversampling #2 Filter Coefficient (SDO_OSFC03_2, R/W, Address = 0xF900_032C)
7.12.1.108 SDO Oversampling #2 Filter Coefficient (SDO_OSFC04_2, R/W, Address = 0xF900_0330)
7.12.1.109 SDO Oversampling #2 Filter Coefficient (SDO_OSFC05_2, R/W, Address = 0xF900_0334)
7.12.1.110 SDO Oversampling #2 Filter Coefficient (SDO_OSFC06_2, R/W, Address = 0xF900_0338)
7.12.1.111 SDO Oversampling #2 Filter Coefficient (SDO_OSFC07_2, R/W, Address = 0xF900_033C)
7.12.1.112 SDO Oversampling #2 Filter Coefficient (SDO_OSFC08_2, R/W, Address = 0xF900_0340)
7.12.1.113 SDO Oversampling #2 Filter Coefficient (SDO_OSFC09_2, R/W, Address = 0xF900_0344)
7.12.1.114 SDO Oversampling #2 Filter Coefficient (SDO_OSFC10_2, R/W, Address = 0xF900_0348)
7.12.1.115 SDO Oversampling #2 Filter Coefficient (SDO_OSFC11_2, R/W, Address = 0xF900_034C)
7.12.1.116 SDO Oversampling #2 Filter Coefficient (SDO_OSFC12_2, R/W, Address = 0xF900_0350)
7.12.1.117 SDO Oversampling #2 Filter Coefficient (SDO_OSFC13_2, R/W, Address = 0xF900_0354)
7.12.1.118 SDO Oversampling #2 Filter Coefficient (SDO_OSFC14_2, R/W, Address = 0xF900_0358)
7.12.1.119 SDO Oversampling #2 Filter Coefficient (SDO_OSFC15_2, R/W, Address = 0xF900_035C)
7.12.1.120 SDO Oversampling #2 Filter Coefficient (SDO_OSFC16_2, R/W, Address = 0xF900_0360)
7.12.1.121 SDO Oversampling #2 Filter Coefficient (SDO_OSFC17_2, R/W, Address = 0xF900_0364)
7.12.1.122 SDO Oversampling #2 Filter Coefficient (SDO_OSFC18_2, R/W, Address = 0xF900_0368)
7.12.1.123 SDO Oversampling #2 Filter Coefficient (SDO_OSFC19_2, R/W, Address = 0xF900_036C)
7.12.1.124 SDO Oversampling #2 Filter Coefficient (SDO_OSFC20_2, R/W, Address = 0xF900_0370)
7.12.1.125 SDO Oversampling #2 Filter Coefficient (SDO_OSFC21_2, R/W, Address = 0xF900_0374)
7.12.1.126 SDO Oversampling #2 Filter Coefficient (SDO_OSFC22_2, R/W, Address = 0xF900_0378)
7.12.1.127 SDO Oversampling #2 Filter Coefficient (SDO_OSFC23_2, R/W, Address = 0xF900_037C)

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4x Oversampling Case Coefficient (Flat response up to 6MHz) – Default reset value

Coefficient	Value	Coefficient	Value	Coefficient	Value
osf_coef00	-2	osf_coef16	-14	osf_coef32	-57
osf_coef01	-3	osf_coef17	-20	osf_coef33	-80
osf_coef02	0	osf_coef18	1	osf_coef34	5
osf_coef03	0	osf_coef19	0	osf_coef35	0
osf_coef04	4	osf_coef20	20	osf_coef36	86
osf_coef05	5	osf_coef21	29	osf_coef37	121
osf_coef06	-1	osf_coef22	-2	osf_coef38	-10
osf_coef07	0	osf_coef23	0	osf_coef39	0
osf_coef08	-6	osf_coef24	-28	osf_coef40	-154
osf_coef09	-9	osf_coef25	-40	osf_coef41	-212
osf_coef10	1	osf_coef26	2	osf_coef42	27
osf_coef11	0	osf_coef27	0	osf_coef43	0
osf_coef12	10	osf_coef28	40	osf_coef44	613
osf_coef13	14	osf_coef29	56	osf_coef45	651
osf_coef14	-1	osf_coef30	-3	osf_coef46	-308
osf_coef15	0	osf_coef31	0	osf_coef47	1024

2x Oversampling Case Coefficient (Flat response up to 12MHz)

Coefficient	Value	Coefficient	Value	Coefficient	Value
osf_coef00	0	osf_coef16	0	osf_coef32	-19
osf_coef01	0	osf_coef17	0	osf_coef33	0
osf_coef02	0	osf_coef18	0	osf_coef34	28
osf_coef03	0	osf_coef19	0	osf_coef35	0
osf_coef04	0	osf_coef20	0	osf_coef36	-39
osf_coef05	0	osf_coef21	0	osf_coef37	0
osf_coef06	0	osf_coef22	0	osf_coef38	55
osf_coef07	0	osf_coef23	0	osf_coef39	0
osf_coef08	0	osf_coef24	-3	osf_coef40	-79
osf_coef09	0	osf_coef25	0	osf_coef41	0
osf_coef10	0	osf_coef26	5	osf_coef42	120
osf_coef11	0	osf_coef27	0	osf_coef43	0
osf_coef12	0	osf_coef28	-8	osf_coef44	-211
osf_coef13	0	osf_coef29	0	osf_coef45	0
osf_coef14	0	osf_coef30	13	osf_coef46	650
osf_coef15	0	osf_coef31	0	osf_coef47	1024

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7.12.1.128 SDO Channel Crosstalk Cancellation Coefficient for Ch. 0 (SDO_XTALK0, R/W, Address = 0xF900_0260)

SDO_XTALK0	Bit	Description	Initial State
Reserved	[31:24]	Reserved, read as zero, do not modify	0
xtalk_coef02	[23:16]	Signed 8 bit integer. Actual value is xtalk_coef02/(210) 0x7F : 0.124 0x7E : 0.123 … 0x01 : 0.000977 0x00 : 0.000000 0xFF :-0.000977 0xFE :-0.001953 ... 0x81 :-0.124 0x80 : -0.125	00
Reserved	[15:8]	Reserved, read as zero, do not modify	0
xtalk_coef01	[7:0]	Same as xtalk_coef01	00

7.12.1.129 SDO Black Burst Control Register (SDO_BB_CTRL, R/W, Address = 0xF900_026C)

SDO_BB_CTRL	Bit	Description	Initial State
Reserved	[31:18]	Reserved, read as zero, do not modify	0
ref_bb_level	[17:8]	Black level setting value. It specifies the level during horizontal active video for black burst signal. The recommended values are NTSC : 0x11A (include 7.5 IRE setup) PAL : 0xFB (without setup)	0x11A
Reserved	[7:6]	Reserved, read as zero, do not modify	0
sel_bb_chan	[5:4]	Black burst (BB) test channel selection DAC0 DAC1 DAC2 00 = CVBS BB BB 01 = BB CVBS BB 10 = BB BB CVBS 11 = Reserved	00
Reserved	[3:1]	Reserved, read as zero, do not modify	0
BB mode	[0]	Black burst test mode enable. If set, entire bit fields in SDO_CONFIG register except ‘Selection of Video Mux for DAC 0, 1, and 2’ bit are discarded and SDO enters black burst test mode. In order to enable black burst test, ‘Selection of Video Mux for DAC 0, 1, and 2’ bit has to be set to zero.	0

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7.12.1.130 SDO Interrupt Request Register (SDO_IRQ, R/W, Address = 0xF900_0280)

SDO_IRQ	Bit	Description	Initial State
Reserved	[31:1]	Reserved, read as zero, do not modify	0
Vsync Interrupt Request	[0]	0 = No interrupt 1 Interrupt request pending (This interrupt is requested if TVOUT module generates the falling edge of vertical synchronization pulses at each field. Write 1 to reset this bit.(Writing '0' has no effect).	0

7.12.1.131 SDO Interrupt Request Masking Register (SDO_IRQMASK, R/W, Address = 0xF900_0284)

SDO_IRQMASK	Bit	Description	Initial State
Reserved	[31:1]	Reserved, read as zero, do not modify	0
Vsync Interrupt Request Masking	[0]	0 = Enables Interrupt request 1 = Disables Interrupt request (The status pending bit of SDO Interrupt Request Register is asserted even if the request is disabled. Only the request to MCU will be disabled.)	0

7.12.1.132 SDO Closed Caption Data Registers (SDO_ARMCC, R/W, Address = 0xF900_03C0)

SDO_ARMCC	Bit	Description	Initial State
Reserved	[31:16]	Reserved, read as zero, do not modify	0
Display Control Character of Closed Caption Data	[15:8]	Bit alignment of the Display Control Character register is in their incoming order. The first incoming bit becomes LSB, i.e. Display Control Character [7:0] = {p, b6, b5, b4, b3, b2, b1, b0}, where bn represents data bit with their incoming order n, and p denotes their odd parity bit.	0
Non Display Control Character of Closed Caption Data	[7:0]	Bit alignment of the Non Display Control Character register is in their incoming order. The first incoming bit becomes LSB, i.e. Non Display Control Character [7:0] = {p, b6, b5, b4, b3, b2, b1, b0}, where bn represents data bit with their incoming order n, and p denotes their odd parity bit.	0

NOTE: This register is used for European Caption as well as US Closed Caption.

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7.12.1.133 SDO WSS 525 Data Registers (SDO_ARMWSS525, R/W, Address = 0xF900_03C4)

SDO_ARMWSS525	Bit	Description	Initial State
Reserved	[31:20]	Reserved, read as zero, do not modify	0
CRC of WSS 525 Data	[19:14]	Bit alignment of the CRC register is according to their incoming order. The first incoming bit becomes LSB, i.e. CRC [19:14] = {b19, b18, b17, b16, b15, b14}, where bn represents data bit with their incoming order n. The CRC used is X^6+ X + 1, all preset to 1.	0
Word 2 of WSS 525 Data	[13:6]	Bit alignment of the Word 2 register is according to their incoming order. The first incoming bit becomes LSB, i.e. Word 2 [13:6] = {b13, b12, b11, b10, b9, b8, b7, b6}, where bn represents data bit with their incoming order n. The Word 2 data are used for copy control: b7, b6 : 00 copying permitted 01 one copy permitted 10 reserved 11 no permission to copy b9 b8 : (reserved) b10 : 0 not analog pre-recorded medium 1 analog pre-recorded medium b13, b12, b11 : (reserved)	0
Word 1 of WSS 525 Data	[5:2]	Bit alignment of the Word 1 register is according to their incoming order. The first incoming bit becomes LSB, i.e. Word 1 [5:2] = {b5, b4, b3, b2}, where bn represents data bit with their incoming order n. The Word 1 data are used to indicate the existence of Word 2 data: b5, b4, b3, b2 : 0000 = copy control information 1111 = default	0
Word 0 of WSS 525 Data	[1:0]	Bit alignment of the Word 0 register is according to their incoming order. The first incoming bit becomes LSB, i.e. Word 0 [1:0] = {b1, b0}, where bn represents data bit with their incoming order n. The Word 0 data are used for display aspect ratio control: b1, b0 : 00 4:3 aspect ratio normal 01 16:9 aspect ratio anamorphic 10 4:3 aspect ratio letterbox 11 reserved	0

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7.12.1.134 SDO WSS 625 Data Registers (SDO_ARMWSS625, R/W, Address = 0xF900_03C8)

SDO_ARMWSS625	Bit	Description	Initial State
Reserved	[31:14]	Reserved, read as zero, do not modify	0
Group D of WSS 625 Data	[13:11]	Bit alignment of the Group D register is according to their incoming order. The first incoming bit becomes LSB, i.e. Group D [13:11] = {b13, b12, b11}, where bn represents data bit with their incoming order n. The Group D data are used for surround sound and copy control: b11 : surround sound no yes b12 : copyright no copyright asserted or unknown copyright asserted b13 : copy protection copying not restricted copying restricted	0
Group C of WSS 625 Data	[10:8]	Bit alignment of the Group C register is according to their incoming order. The first incoming bit becomes LSB, i.e. Group C [10:8] = {b10, b9, b8}, where bn represents data bit with their incoming order n. The Group C data are used for subtitles: b8 : teletext subtitles 0 no 1 yes b10 , b9 : open subtitles 00 no 01 inside active picture 10 outside active picture 11 reserved	0

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SDO_ARMWSS625	Bit	Description	Initial State
Group B of WSS 625 Data	[7:4]	Bit alignment of the Group B register is according to their incoming order. The first incoming bit becomes LSB, i.e. Group B [7:4] = {b7, b6, b5, b4}, where bn represents data bit with their incoming order n. The Group B data are used for enhanced video services: b4 : mode 0 camera mode 1 film mode b5 : color encoding normal PAL Motion Adaptive ColorPlus b6 : helper signals not present present b7 : fixed to 0	0
Group A of WSS 625 Data	[3:0]	Bit alignment of the Group A register is according to their incoming order. The first incoming bit becomes LSB, i.e. Group A [3:0] = {b3, b2, b1, b0}, where bn represents data bit with their incoming order n. The Group A data are used for display aspect ratio control: b3, b2 b1, b0 : 1000 4:3 full format - 576 lines 0001 14:9 letterbox center 504 lines 0010 14:9 letterbox top 504 lines 1011 16:9 letterbox center 430 lines 0100 16:9 letterbox top 430 lines 1101 >16:9 letterbox center - 1110 14:9 full format center 576 lines 0111 16:9 anamorphic - 576 lines	0

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7.12.1.135 SDO CGMS-A 525 Data Registers (SDO_ARMCGMS525, R/W, Address = 0xF900_03CC)

SDO_ARMCGMS525	Bit	Description	Initial State
Reserved	[31:20]	Reserved, read as zero, do not modify	0
CRC of CGMS-A 525 Data	[19:14]	Bit alignment of the CRC register is according to their incoming order. The first incoming bit becomes LSB, i.e. CRC [19:14] = {b19, b18, b17, b16, b15, b14}, where bn represents data bit with their incoming order n. The CRC used is X^6+ X + 1, all preset to 1.	0
Word 2 of CGMS-A 525 Data	[13:6]	Bit alignment of the Word 2 register is according to their incoming order. The first incoming bit becomes LSB, i.e. Word 2 [13:6] = {b13, b12, b11, b10, b9, b8, b7, b6}, where bn represents data bit with their incoming order n. The Word 2 data are used for copy control: b7, b6 : 00 copying permitted 01 one copy permitted 10 reserved 11 no copying permitted b9 b8 : (reserved) b10 : 0 not analog pre-recorded medium 1 analog pre-recorded medium b13, b12, b11 : (reserved)	0
Word 1 of CGMS-A 525 Data	[5:2]	Bit alignment of the Word 1 register is according to their incoming order. The first incoming bit becomes LSB, i.e. Word 1 [5:2] = {b5, b4, b3, b2}, where bn represents data bit with their incoming order n. The Word 1 data are used to indicate the existence of Word 2 data: b5, b4, b3, b2 : 0000 copy control information 1111 default	0

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SDO_ARMCGMS525	Bit	Description	Initial State
Word 0 of CGMS-A 525 Data	[1:0]	Bit alignment of the Word 0 register is according to their incoming order. The first incoming bit becomes LSB, i.e. Word 0 [1:0] = {b1, b0}, where bn represents data bit with their incoming order n. The Word 0 data are used for display aspect ratio control: b1, b0 : 00 4:3 aspect ratio normal 01 16:9 aspect ratio anamorphic 10 4:3 aspect ratio letterbox 11 reserved	0

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7.12.1.136 SDO CGMS-A 625 Data Registers (SDO_ARMCGMS625, R/W, Address = 0xF900_03D4)

SDO_ARMCGMS625	Bit	Description	Initial State
Reserved	[31:14]	Reserved, read as zero, do not modify	0
Group D of CGMS-A 625 Data	[13:11]	Bit alignment of the Group D register is according to their incoming order. The first incoming bit becomes LSB, i.e. Group D [13:11] = {b13, b12, b11}, where bn represents data bit with their incoming order n. The Group D data are used for surround sound and copy control: b11 : surround sound no yes b12 : copyright no copyright asserted or unknown copyright asserted b13 : copy protection copying not restricted copying restricted	0
Group C of CGMS-A 625 Data	[10:8]	Bit alignment of the Group C register is according to their incoming order. The first incoming bit becomes LSB, i.e. Group C [10:8] = {b10, b9, b8}, where bn represents data bit with their incoming order n. The Group C data are used for subtitles: b8 : teletext subtitles 0 no 1 yes b10 , b9 : open subtitles 00 no 01 inside active picture 10 outside active picture 11 reserved	0

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SDO_ARMCGMS625	Bit	Description	Initial State
Group B of CGMS-A 625 Data	[7:4]	Bit alignment of the Group B register is according to their incoming order. The first incoming bit becomes LSB, i.e. Group B [7:4] = {b7, b6, b5, b4}, where bn represents data bit with their incoming order n. The Group B data are used for enhanced video services: b4 : mode 0 camera mode 1 film mode b5 : color encoding normal PAL Motion Adaptive ColorPlus b6 : helper signals not present present B7 : fixed to 0	0
Group A of CGMS-A 625 Data	[3:0]	Bit alignment of the Group A register is according to their incoming order. The first incoming bit becomes LSB, i.e. Group A [3:0] = {b3, b2, b1, b0}, where bn represents data bit with their incoming order n. The Group A data are used for display aspect ratio control: b3, b2 b1, b0 : 1000 4:3 full format - 576 lines 0001 14:9 letterbox center 504 lines 0010 14:9 letterbox top 504 lines 1011 16:9 letterbox center 430 lines 0100 16:9 letterbox top 430 lines 1101 >16:9 letterbox center - 1110 14:9 full format center 576 lines 0111 16:9 anamorphic - 576 lines	0

7.12.1.137 SDO Version Register (SDO_VERSION, R, Address = 0xF900_03D8)

SDO_VERSION	Bit	Description	Initial State
TVOUT version number	[31:0]	Read only register of TVOUT version number	C

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7.12.2 SHADOW REGISTERS

7.12.2.1 SDO Closed Caption Data Shadow Register (SDO_CC, R/W, Address = 0xF900_0380)

SDO_CC	Bit	Description	Initial State
Reserved	[31:16]	Reserved, read as zero, do not modify	0
Display Control Character of Closed Caption Data	[15:8]	If MCU set values of SDO_ARMCC, the values are copied into this shadow register at the next vertical sync interrupt. Do not set values to this shadow register.	0
Non Display Control Character of Closed Caption Data	[7:0]		0

7.12.2.2 SDO WSS 525 Data Shadow Registers (SDO_WSS525, R/W, Address = 0xF900_0384)

SDO_WSS525	Bit	Description	Initial State
Reserved	[31:20]	Reserved, read as zero, do not modify	0
CRC of WSS 525 Data	[19:14]	If MCU set values of SDO_ARMWSS525, the values are copied into this shadow register at the next vertical sync interrupt. Do not set values to this shadow register.	0
Word 2 of WSS 525 Data	[13:6]		0
Word 1 of WSS 525 Data	[5:2]		0
Word 0 of WSS 525 Data	[1:0]		0

7.12.2.3 SDO WSS 625 Data Shadow Registers (SDO_WSS625, R/W, Address = 0xF900_0388)

SDO_ARMWSS625	Bit	Description	Initial State
Reserved	[31:14]	Reserved, read as zero, do not modify	0
Group D of WSS 625 Data	[13:11]	If MCU set values of SDO_ARMWSS625, the values are copied into this shadow register at the next vertical sync interrupt. Do not set values to this shadow register.	0
Group C of WSS 625 Data	[10:8]		0
Group B of WSS 625 Data	[7:4]		0
Group A of WSS 625 Data	[3:0]		0

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7.12.2.4 SDO CGMS-A 525 Data Shadow Registers (SDO_CGMS525, R/W, Address = 0xF900_038C)

SDO_CGMS525	Bit	Description	Initial State
Reserved	[31:20]	Reserved, read as zero, do not modify	0
CRC of CGMS-A 525 Data	[19:14]	If MCU set values of SDO_ARMCGMS525, the values are copied into this shadow register at the next vertical sync interrupt. Do not set values to this shadow register.	0
Word 2 of CGMS-A 525 Data	[13:6]		0
Word 1 of CGMS-A 525 Data	[5:2]		0
Word 0 of CGMS-A 525 Data	[1:0]		0

7.12.2.5 SDO CGMS-A 625 Data Registers (SDO_CGMS625, R/W, Address = 0xF900_0394)

SDO_CGMS625	Bit	Description	Initial State
Reserved	[31:14]	Reserved, read as zero, do not modify	0
Group D of CGMS-A 625 Data	[13:11]	If MCU set values of SDO_ARMCGMS625, the values are copied into this shadow register at the next vertical sync interrupt. Do not set values to this shadow register.	0
Group C of CGMS-A 625 Data	[10:8]		0
Group B of CGMS-A 625 Data	[7:4]		0
Group A of CGMS-A 625 Data	[3:0]		0

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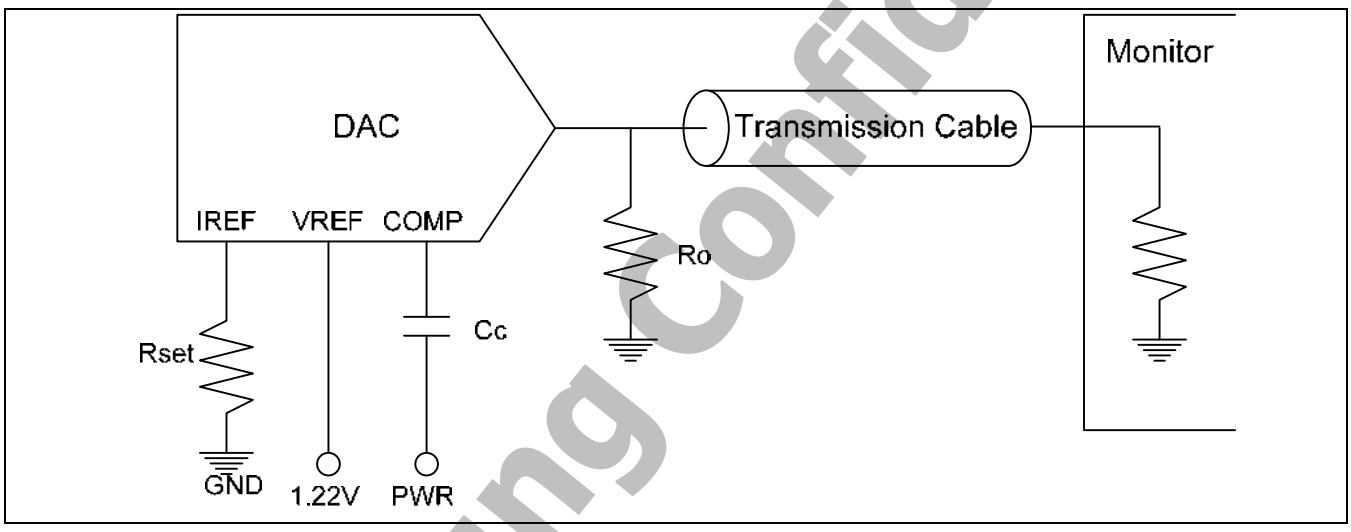
7.13 VIDEO DAC

7.13.1 GENERAL DESCRIPTION

The DAC is a 10-bit 1channel CMOS Digital-to-Analog converter for general applications.
Its maximum conversion rate is 54MHz. It operates at analog power, 2.7V to 3.3V and provides full scale output currents of 26.7mA at one channel with 75 ohm load for 1.3V.
The DAC has a power down mode to reduce power consumption during inactive periods.

7.13.2 FEATURES

- Maximum 54MHz Update Rate.
- 10-bit Current Output DAC
- 1.3Vpp Triple Output Compliance Range
- Internal Voltage Reference
- Fine Full Scale control: 91.1% ~ 114.8%
- Power Down Mode



7.13.3 CORE PORT DESCRIPTION

Table 7-5 Port Description of Video DAC

Name	Width	I/O	Description
VREF	-	AI	Voltage reference for DAC. An Internal voltage reference of nominally 1.22V is provided. Is driven with an external reference source.
IREF	-	AI	Full Scale Adjust control. The full-scale current drive on each of the output channels is determined by the value of a resistor RSET connected between this terminal and AVSS30A1.
IOUT1, IOUT2, IOUT3	-	AO	DAC current output. Full scale output is achieved if all input bits are set to binary 1.

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COMP	-	AO	Compensation Pin. This is a compensation pin for the internal reference amplifier. A 0.1uF ceramic capacitor(Tolerance ±10%) must be connected between COMP and AVDD30A1.

I/O Type Abbreviation.

- AI: Analog Input, DI: Digital Input, AO: Analog Output, AP: Analog Power, AG: Analog Ground,
- DP: Digital Power, DG: Digital Ground, LP: Logic Power, LG: Logic Ground

7.13.4 FULL SCALE VOLTAGE MODIFICATION

Table 7-6 Recommended RSET and RO According to Full Scale Voltage

Full Scale Voltage	RSET	RO
1.3V	1.2k(Tolerance ±1%) [ohm]	75(Tolerance ±5%) [ohm]
1.0V	1.54k(Tolerance ±1%) [ohm]	75(Tolerance ±5%) [ohm]

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7.14 APPENDIX

7.14.1 VERTICAL BAR PHEOMENON

The goal of oversampling filter in TVOUT module is to obtain 54MHz sample-rate data for DAC from 13.5MHz/ 27MHz source sample-rate. The quality of interpolation result using FIR filter depends on the number of FIR filter taps. Unfortunately, ideal interpolation filter needs infinite number of taps, which cannot be implemented. Thus, practical consideration into the trade-off between interpolation quality and computational complexity is needed.

In TV application, it is the sub-carrier waveform that is the most sensitive to the quality of interpolation filter. Source rate of 13.5MHz for CVBS output is too coarse to represent the shape of sub-carrier and the quality of interpolation highly affects the shape of resulting 54 MHz sub-carriers. The error of sub-carrier induced by non-ideal interpolation filter is basically implies distortions in chrominance components. However, in the case of CVBS signal, the chrominance component and the luminance component are together to be mixed and transmitted via one channel. Then, parts of the interpolation error appears in luminance parts if the CVBS signal is separated into luminance component and chrominance components by the comb filter of TV decoder. According to an analysis on this interpolation error, the error pattern is repeated with a frequency of 102.3 kHz and the error spectrum is highly concentrated around 102.3 kHz. Thus, most of interpolation error is classified into luminance part by TV decoder and this error is shown in the shape of brightness distortion in TV monitor.

The oversampling filter in S5PV210 adopts 95-tap interpolation for CVBS signal in order to minimize the vertical bar phenomenon. Compared to 47-tap interpolation of legacy TVOUT version, the peak of vertical bar reduces by about 0.1 IRE assuming the use of 6th order Butterworth analog interpolation filter.

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8 VIDEO PROCESSOR

8.1 OVERVIEW OF VIDEO PROCESSOR

Video processor (VP) is responsible for video scaling, de-interlacing, and video post processing of TV-out data path. VP reads reconstructed YCbCr 4:2:0 video sequences from DRAM, processes the sequence, and sends it to MIXER on-the-fly as shown in *Figure 8-1*.

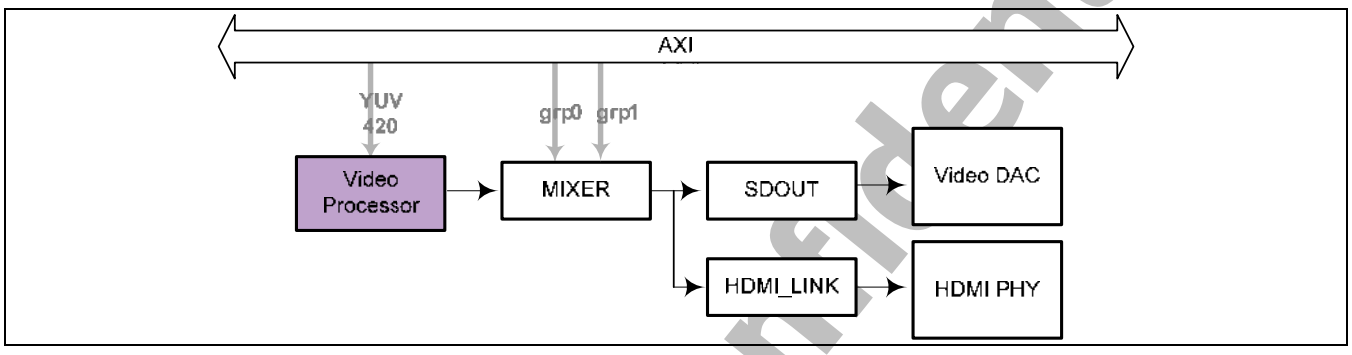

Figure 8-1 Video Data Path

8.1.1 KEY FEATURES OF VIDEO PROCESSOR

Input YCbCr sequence of VP is up to 1920x1080@30Hz. Basic features of VP are as follows:

- Supports BOB / TILE (YUV420 NV12 type, Note: refer to MFC user's manual for TILE)
- Input source size up to 1920x1080 (min : 32x4)
- Produces YCbCr 4:4:4 outputs to help MIXER to blend video and graphics
- Supports 1/4X to 16X vertical scaling with 4-tap/16-phase poly-phase filter
- Supports 1/4X to 16X horizontal scaling with 8-tap/16-phase poly-phase filter
- Supports Pan & Scan, Letterbox, and NTSC/PAL conversion using scaling
- Supports Flexible scaled video positioning within display area
- Supports 1/16 pixel resolution Pan&Scan mode
- Supports Flexible post video processing
  - Color saturation, Brightness/ Contrast enhancement, Edge enhancement for SDTV
  - Color space conversion between BT.601 and BT.709

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8.2 BLOCK DIAGRAM OF VIDEO PROCESSOR

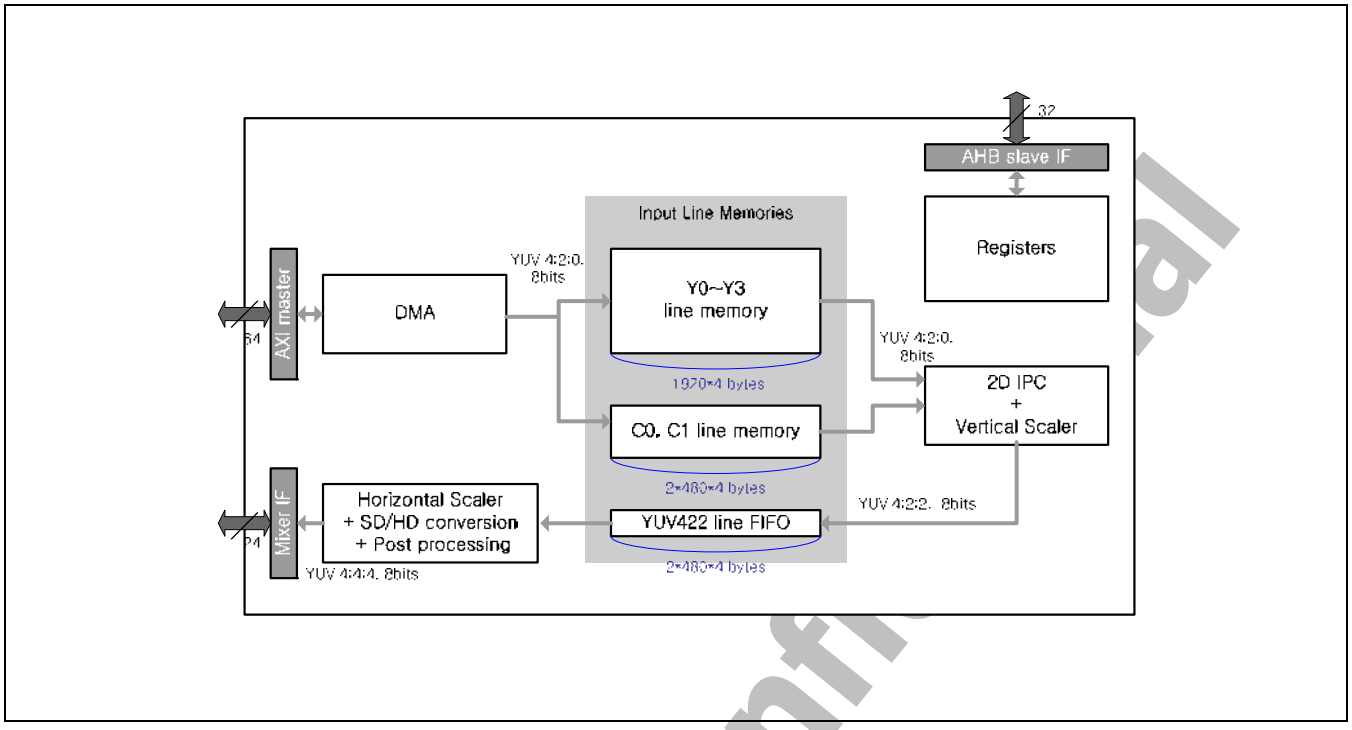

Figure 8-2 Block Diagram of Video Processor

Components in video processor:

- DMA: DMA reads the image from memory
- Input Line Memory: It stores data to process the image.
- Registers: The configuration of Video Processor
- 2D-IPC and Vertical Scaler: It performs IPC and vertical scaling.
- Horizontal Scaler: Horizontal scaling and post processing

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8.3 FUNCTION DESCRIPTION OF VIDEO PROCESSOR

8.3.1 BOB IN VIDEO PROCESSOR

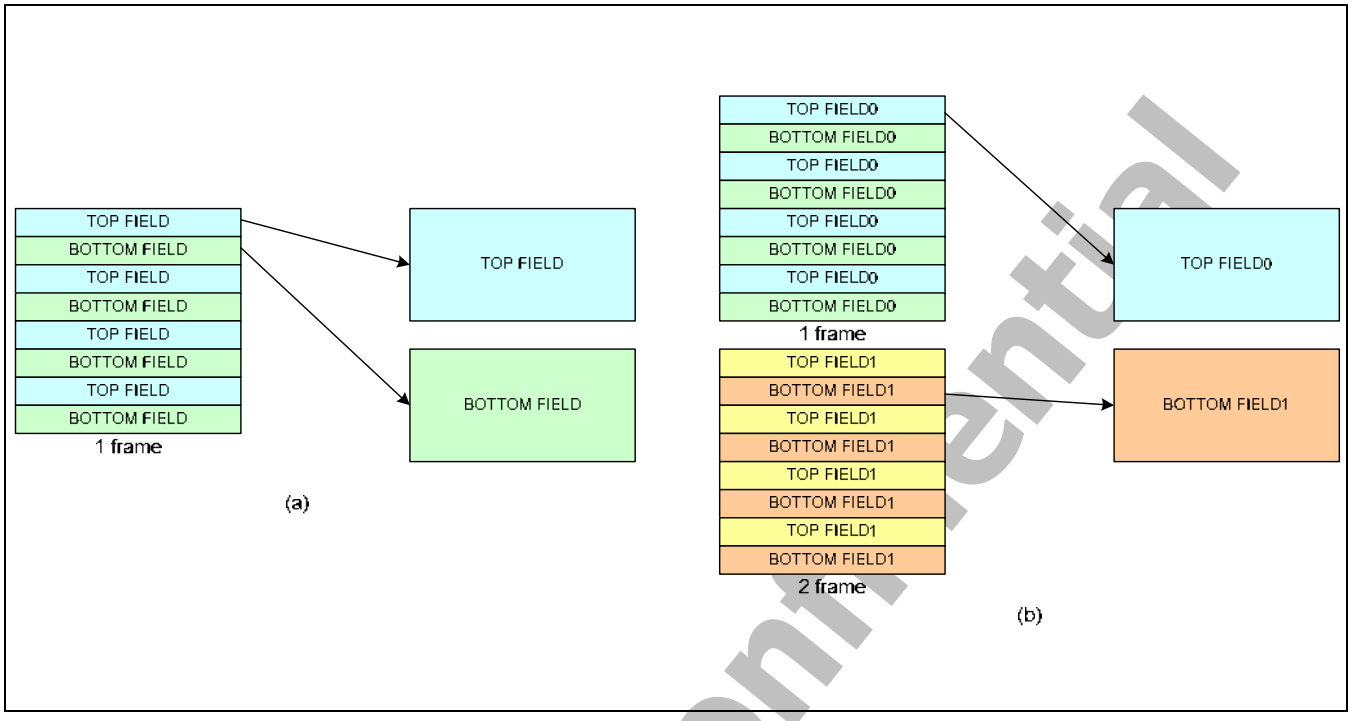

Figure 8-3 Data Type for BOB

In some applications, it is necessary to display an interlaced video signal on a non-interlaced display. Thus, some form of “de-interlacing” or “progressive can conversion” is required. Video mode is one of fundamental de-interlacing algorithm. Video mode de-interlacing can be further broken down into inter-filed and intra-field processing. Particular, Intra-field processing in video mode is the simplest method to generate additional scan lines using only information in the original field. The computer industry has coined this technique as “BOB”.

BOB in VP consists of Intra-field or inter-field. Inter-field comes from a frame as shown in *Figure 8-3*(a). Also, Intra-field comes from two frames as shown in *Figure 8-3* (b).

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8.3.2 NTERLACE TO PROGRESSIVE CONVERSION

Interlace to Progressive Conversion (IPC) plays role to convert interlaced to progressive. It is distinguished with vertical x2 scale.

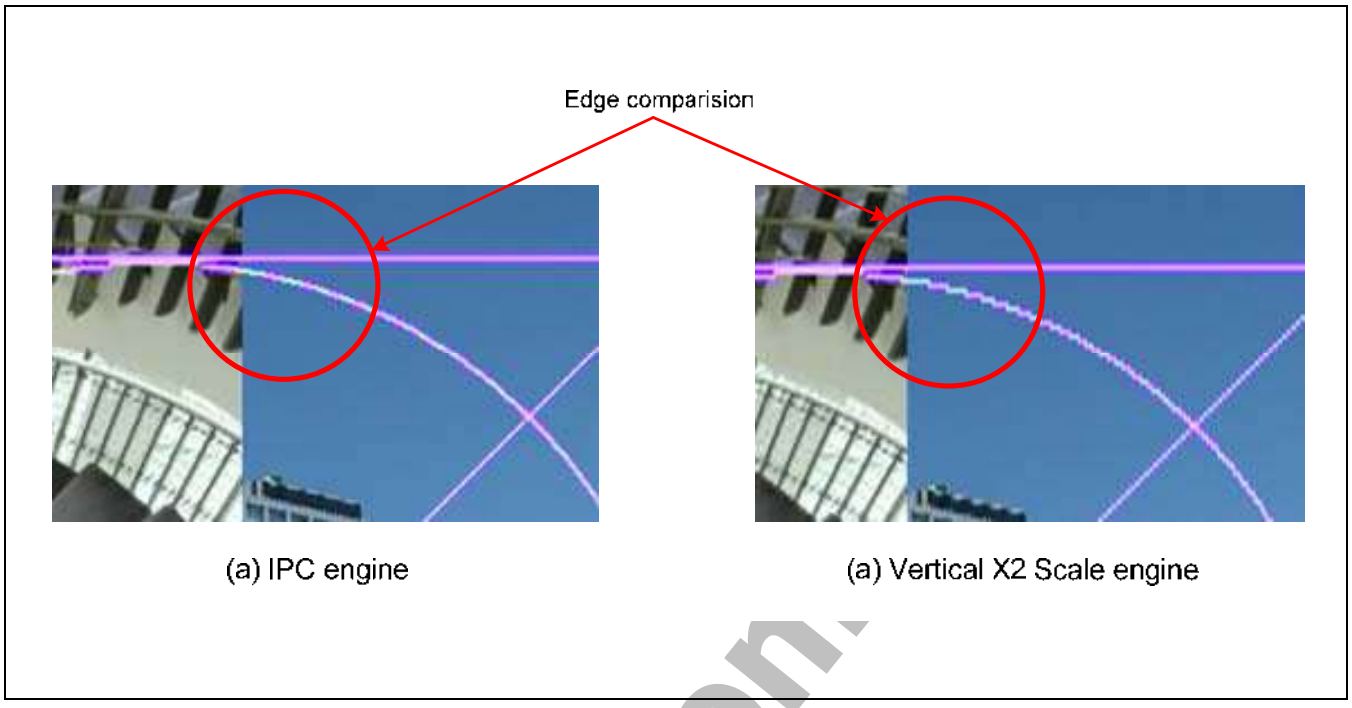

Figure 8-4 Difference Between IPC and X2 Scale-up

IPC engine executes “Edge Detection Function” which is based on the edge diagnosis method. This enables IPC to estimate edge line and display more natural image.

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8.4 REGISTER DESCRIPTION

8.4.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
VP_ENABLE	0xF910_0000	R/W	Specifies the Power-Down Ready & Enable	0x0000_0002
VP_SRESET	0xF910_0004	R/W	Specifies the Software Reset	0x0000_0000
VP_SHADOW_UPDATE	0xF910_0008	R/W	Specifies the Shadow Register Update Enable	0x0000_0000
VP_FIELD_ID	0xF910_000C	R/W	Specifies the Field ID of the “Source” Image	0x0000_0000
VP_MODE	0xF910_0010	R/W	Specifies the VP Operation Mode	0x0000_0000
VP_IMG_SIZE_Y	0xF910_0014	R/W	Specifies the Luminance Date Size	0x0000_0000
VP_IMG_SIZE_C	0xF910_0018	R/W	Specifies the Chrominance Date Size	0x0000_0000
VP_TOP_Y_PTR	0xF910_0028	R/W	Specifies the Base Address for Y of Top Field (Frame)	0x0000_0000
VP_BOT_Y_PTR	0xF910_002C	R/W	Specifies the Base Address for Y of Bottom Field	0x0000_0000
VP_TOP_C_PTR	0xF910_0030	R/W	Specifies the Base Address for C of Top Field(frame)	0x0000_0000
VP_BOT_C_PTR	0xF910_0034	R/W	Specifies the Base Address for C of Bottom Field	0x0000_0000
VP_ENDIAN_MODE	0xF910_03CC	R/W	Specifies the Big/Little Endian Mode Selection	0x0000_0000
VP_SRC_H_POSITION	0xF910_0044	R/W	Specifies the Horizontal Offset in the Source Image	0x0000_0000
VP_SRC_V_POSITION	0xF910_0048	R/W	Specifies the Vertical Offset in the Source Image	0x0000_0000
VP_SRC_WIDTH	0xF910_004C	R/W	Specifies the Width of the Source Image	0x0000_0000
VP_SRC_HEIGHT	0xF910_0050	R/W	Specifies the Height of the Source Image	0x0000_0000
VP_DST_H_POSITION	0xF910_0054	R/W	Specifies the Horizontal Offset in the Display	0x0000_0000
VP_DST_V_POSITION	0xF910_0058	R/W	Specifies the Vertical Offset in the Display	0x0000_0000
VP_DST_WIDTH	0xF910_005C	R/W	Specifies the Width of the Display	0x0000_0000
VP_DST_HEIGHT	0xF910_0060	R/W	Specifies the Height of the Display	0x0000_0000
VP_H_RATIO	0xF910_0064	R/W	Specifies the Horizontal Zoom Ratio of SRC:DST	0x0000_0000
VP_V_RATIO	0xF910_0068	R/W	Specifies the Vertical Zoom Ratio of SRC:DST	0x0000_0000

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Register	Address	R/W	Description	Reset Value
VP_POLY8_Y0_LL	0xF910_006C	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y0_LH	0xF910_0070	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y0_HL	0xF910_0074	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y0_HH	0xF910_0078	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y1_LL	0xF910_007C	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y1_LH	0xF910_0080	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y1_HL	0xF910_0084	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y1_HH	0xF910_0088	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y2_LL	0xF910_008C	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y2_LH	0xF910_0090	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y2_HL	0xF910_0094	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y2_HH	0xF910_0098	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y3_LL	0xF910_009C	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y3_LH	0xF910_00A0	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY8_Y3_HL	0xF910_00A4	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000

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Register	Address	R/W	Description	Reset Value
VP_POLY8_Y3_HH	0xF910_00A8	R/W	Specifies the 8-Tap Poly-phase Filter Coefficients for Luminance Horizontal Scaling	0x0000_0000
VP_POLY4_Y0_LL	0xF910_00EC	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y0_LH	0xF910_00F0	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y0_HL	0xF910_00F4	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y0_HH	0xF910_00F8	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y1_LL	0xF910_00FC	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y1_LH	0xF910_0100	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y1_HL	0xF910_0104	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y1_HH	0xF910_0108	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y2_LL	0xF910_010C	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y2_LH	0xF910_0110	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y2_HL	0xF910_0114	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y2_HH	0xF910_0118	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y3_LL	0xF910_011C	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y3_LH	0xF910_0120	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000

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Register	Address	R/W	Description	Reset Value
VP_POLY4_Y3_HL	0xF910_0124	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_Y3_HH	0xF910_0128	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Luminance Vertical Scaling	0x0000_0000
VP_POLY4_C0_LL	0xF910_012C	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Chrominance Horizontal Scaling	0x0000_0000
VP_POLY4_C0_LH	0xF910_0130	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Chrominance Horizontal Scaling	0x0000_0000
VP_POLY4_C0_HL	0xF910_0134	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Chrominance Horizontal Scaling	0x0000_0000
VP_POLY4_C0_HH	0xF910_0138	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Chrominance Horizontal Scaling	0x0000_0000
VP_POLY4_C1_LL	0xF910_013C	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Chrominance Horizontal Scaling	0x0000_0000
VP_POLY4_C1_LH	0xF910_0140	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Chrominance Horizontal Scaling	0x0000_0000
VP_POLY4_C1_HL	0xF910_0144	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Chrominance Horizontal Scaling	0x0000_0000
VP_POLY4_C1_HH	0xF910_0148	R/W	Specifies the 4-Tap Poly-phase Filter Coefficients for Chrominance Horizontal Scaling	0x0000_0000
PP_CSC_Y2Y_COEF	0xF910_01D4	R/W	Specifies the Y to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_CB2Y_COEF	0xF910_01D8	R/W	Specifies the CB to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_CR2Y_COEF	0xF910_01DC	R/W	Specifies the CR to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_Y2CB_COEF	0xF910_01E0	R/W	Specifies the Y to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_CB2CB_COEF	0xF910_01E4	R/W	Specifies the CB to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_CR2CB_COEF	0xF910_01F0	R/W	Specifies the CR to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_Y2CR_COEF	0xF910_01EC	R/W	Specifies the Y to Y CSC Coefficient Setting	0x0000_0000

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Register	Address	R/W	Description	Reset Value
PP_CSC_CB2CR_COEF	0xF910_01E8	R/W	Specifies the CB to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_CR2CR_COEF	0xF910_01F4	R/W	Specifies the CR to Y CSC Coefficient Setting	0x0000_0000
PP_BYPASS	0xF910_0200	R/W	Specifies the Disable the Post Image Processor	0x0000_0001
PP_SATURATION	0xF910_020C	R/W	Specifies the Color Saturation Factor	0x0000_0080
PP_SHARPNESS	0xF910_0210	R/W	Specifies the Control for the Edge Enhancement	0x0000_0500
PP_LINE_EQ0	0xF910_0218	R/W	Specifies the Line Equation for Contrast Duration “0”	0x0000_0000
PP_LINE_EQ1	0xF910_021C	R/W	Specifies the Line Equation for Contrast Duration “1”	0x0000_0000
PP_LINE_EQ2	0xF910_0220	R/W	Specifies the Line Equation for Contrast Duration “2”	0x0000_0000
PP_LINE_EQ3	0xF910_0224	R/W	Specifies the Line Equation for Contrast Duration “3”	0x0000_0000
PP_LINE_EQ4	0xF910_0228	R/W	Specifies the Line Equation for Contrast Duration “4”	0x0000_0000
PP_LINE_EQ5	0xF910_022C	R/W	Specifies the Line Equation for Contrast Duration “5”	0x0000_0000
PP_LINE_EQ6	0xF910_0230	R/W	Specifies the Line Equation for Contrast Duration “6”	0x0000_0000
PP_LINE_EQ7	0xF910_0234	R/W	Specifies the Line Equation for Contrast Duration “7”	0x0000_0000
PP_BRIGHT_OFFSET	0xF910_0238	R/W	Specifies the Brightness Offset Control for Y	0x0000_0000
PP_CSC_EN	0xF910_023C	R/W	Specifies the Color Space Conversion Control	0x0000_0002
VP_VERSION_INFO	0xF910_03FC	R	Specifies the VP Version Information	0x0000_0011
Shadow Register Description				
VP_FIELD_ID_S	0xF910_016C	R	Specifies the Field ID of the “Source” Image	0x0000_0000
VP_MODE_S	0xF910_0170	R	Specifies the VP Operation Mode	0x0000_0000
VP_IMG_SIZE_Y_S	0xF910_0174	R	Specifies the Luminance Date Tiled Size	0x0000_0000
VP_IMG_SIZE_C_S	0xF910_0178	R	Specifies the Chrominance Date Tiled Size	0x0000_0000
VP_TOP_Y_PTR_S	0xF910_0190	R	Specifies the Base Address for Y of Top Field	0x0000_0000
VP_BOT_Y_PTR_S	0xF910_0194	R	Specifies the Base Address for Y of Bottom Field	0x0000_0000

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Register	Address	R/W	Description	Reset Value
VP_TOP_C_PTR_S	0xF910_0198	R	Specifies the Base Address for C of Top Frame	0x0000_0000
VP_BOT_C_PTR_S	0xF910_019C	R	Specifies the Base Address for C of Bottom field	0x0000_0000
VP_ENDIAN_MODE_S	0xF910_03EC	R	Specifies the Big/ Little Endian Mode Selection	0x0000_0000
VP_SRC_H_POSITION_S	0xF910_01AC	R	Specifies the Horizontal Offset in the Source Image	0x0000_0000
VP_SRC_V_POSITION_S	0xF910_01B0	R	Specifies the Vertical Offset in the Source Image	0x0000_0000
VP_SRC_WIDTH_S	0xF910_01B4	R	Specifies the Width of the Source Image	0x0000_0000
VP_SRC_HEIGHT_S	0xF910_01B8	R	Specifies the Height of the Source Image	0x0000_0000
VP_DST_H_POSITION_S	0xF910_01BC	R	Specifies the Horizontal Offset in the Display	0x0000_0000
VP_DST_V_POSITION_S	0xF910_01C0	R	Specifies the Vertical Offset in the Display	0x0000_0000
VP_DST_WIDTH_S	0xF910_01C4	R	Specifies the Width of the Display	0x0000_0000
VP_DST_HEIGHT_S	0xF910_01C8	R	Specifies the Height of the Display	0x0000_0000
VP_H_RATIO_S	0xF910_01CC	R	Specifies the Horizontal Zoom Ratio of SRC:DST	0x0000_0000
VP_V_RATIO_S	0xF910_01D0	R	Specifies the Vertical Zoom Ratio of SRC:DST	0x0000_0000
PP_BYPASS_S	0xF910_0258	R	Specifies the Disable the Post Image Processor	0x0000_0000
PP_SATURATION_S	0xF910_025C	R	Specifies the Color Saturation Factor	0x0000_0000
PP_SHARPNESS_S	0xF910_0260	R	Specifies the Control for the Edge Enhancement	0x0000_0000
PP_LINE_EQ0_S	0xF910_0268	R	Specifies the Line Equation for Contrast Duration “0”	0x0000_0000
PP_LINE_EQ1_S	0xF910_026C	R	Specifies the Line Equation for Contrast Duration “1”	0x0000_0000
PP_LINE_EQ2_S	0xF910_0270	R	Specifies the Line Equation for Contrast Duration “2”	0x0000_0000
PP_LINE_EQ3_S	0xF910_0274	R	Specifies the Line Equation for Contrast Duration “3”	0x0000_0000
PP_LINE_EQ4_S	0xF910_0278	R	Specifies the Line Equation for Contrast Duration “4”	0x0000_0000
PP_LINE_EQ5_S	0xF910_027C	R	Specifies the Line Equation for Contrast Duration “5”	0x0000_0000
PP_LINE_EQ6_S	0xF910_0280	R	Specifies the Line Equation for Contrast Duration “6”	0x0000_0000

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Register	Address	R/W	Description	Reset Value
PP_LINE_EQ7_S	0xF910_0284	R	Specifies the Line Equation for Contrast Duration “7”	0x0000_0000
PP_BRIGHT_OFFSET_S	0xF910_0288	R	Specifies the Brightness Offset Control for Y	0x0000_0000
PP_CSC_EN_S	0xF910_028C	R	Specifies the Color Space Conversion Control	0x0000_0000
PP_CSC_Y2Y_COEF_S	0xF910_0290	R	Specifies the Y to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_CB2Y_COEF_S	0xF910_0294	R	Specifies the CB to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_CR2Y_COEF_S	0xF910_0298	R	Specifies the CR to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_Y2CB_COEF_S	0xF910_029C	R	Specifies the Y to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_CB2CB_COEF_S	0xF910_02A0	R	Specifies the CB to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_CR2CB_COEF_S	0xF910_02AC	R	Specifies the CR to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_Y2CR_COEF_S	0xF910_02A8	R	Specifies the Y to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_CB2CR_COEF_S	0xF910_02A4	R	Specifies the CB to Y CSC Coefficient Setting	0x0000_0000
PP_CSC_CR2CR_COEF_S	0xF910_02B0	R	Specifies the CR to Y CSC Coefficient Setting	0x0000_0000

Video processor has special registers called “Shadow Register”. Software set the appropriate values to VP registers and this information are copied to the corresponding shadow registers if V-SYNC is invoked. Video processor is actually working according to these shadow registers.

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8.4.1.1 Video Processor Enable/Disable Control Register (VP_ENABLE, Address = 0xF910_0000)

VP_ENABLE	Bit	Description	R/W	Initial State
Reserved	[31:3]	Reserved, read as zero, do not modify	R/W	0
VP_ON_S	[2]	This bit is read-only. Shadow bit of the bit [0]	R	0
VP_OPERATION_STATUS	[1]	This bit is read-only. 0 = VP is operating. 1 = VP is idle mode.	R	1
VP_ON	[0]	This bit is read-write. 0 = Disables 1 = Enables Note: The SFRs of Video Processor and Image Mixer is updated by Vertical Sync of TVENC's Timing Generator. Thus, SFRs are configured before this bit is enabled. The sequence to enable TVSS is as follows: "VP -> MIXER TVENC(HDMI)". Also, because SFRs are updated by Verical Sync, the disabling sequence is following as : "VP -> MIXER -> TVNEC(HDMI)".	R/W	0

8.4.1.2 Video Processor Software Reset (VP_SRESET, R/W, Address = 0xF910_0004)

VP_SRESET	Bit	Description	Initial State
Reserved	[31:1]	Reserved, read as zero, do not modify	0
VP_SRESET	[0]	0 = Software reset is set and the last soft reset is complete. 1 = VP is processing software reset sequence.	0

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8.4.1.3 Video Processor Shadow Register Update Enable Control Register (VP_SHADOW_UPDATE, W, Address = 0xF910_0008)

VP_SHADOW_UPDATE	Bit	Description	Initial State
Reserved	[31:1]	Reserved, read as zero, do not modify	0
VP_SHADOW_UPDATE	[0]	0 = Shadow registers are not updated at the rising edge of vertical sync. 1 = Shadow registers are updated and this register is cleared by H/W at the rising edge of vertical sync. (Shadow registers are listed in SHADOW REGISTER MAP table)	0

8.4.1.4 Video Processor Input Field ID Control Register (VP_FIELD_ID, R/W, Address = 0xF910_000C)

VP_FIELD_ID	Bit	Description	Initial State
Reserved	[31:1]	Reserved, read as zero, do not modify	0
VP_FILED_ID	[0]	When VP_MODE[2] is set to 'high', this bit shows current FIELD information. Else, when VP_MODE[2] is set to 'low', this controls the pointer of top and bottom field. 0 = Top field 1 = Bottom field	0

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8.4.1.5 Video Processor Operation Mode Control Register (VP_MODE, R/W, Address = 0xF910_0010)

VP_MODE	Bit	Description	Initial State
RTQoSTH	[31:24]	RTQoS threshold level configure. The Video Processor has the 192-depth internal DMA FIFO. Thus, you can adjust FIFO threshold level. 0 = Not available 1 ~ 191 = Threshold level 192 ~ 255 = Reserved	0
Reserved	[23:6]	Reserved, read as zero, do not modify	0
LINE_SKIP	[5]	This bit can control DMA operation. If it is set to '1', DMA skips a line per two lines while it reads line data. 0 = OFF 1 = ON	0
MEM_MODE	[4]	0 = Linear Mode 1 = Tile Mode (refer to MFC user's manual)	0
CROMA_EXPANSION	[3]	If it is set to '0', only refer to the chrominance of TOP filed. But set to '1', it uses the chrominance both TOP and BOTTOM. 0 = Using only C_TOP_PTR 1 = Using both C_TOP_PTR and C_BOT_PTR	0
FIELD_ID_AUTO_TOGGLING	[2]	0 = FIELD_ID is defined by user 1 = FIELD_ID is automatically toggled by V_SYNC DMA base address is changed by this bit. Note: VP_FIELD_ID_S register is toggled if this bit is 1, not VP_FIELD_ID	0
2D_IPC	[1]	Interlace to progressive conversion. VP displays progressive scan as using one filed image 0 = Disables 2D-IPC 1 = Enables 2D-IPC	0
Reserved	[0]	Reserved. It must be '0'	0

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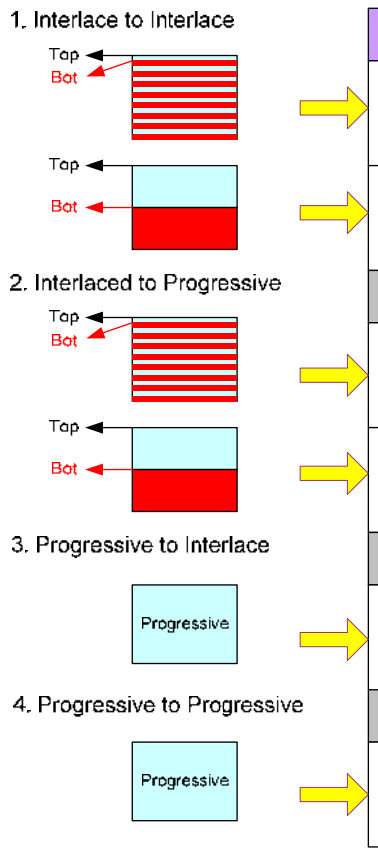
The guide of configuration



LINE_SKIP	2D_IPC	FIELD_ID_AUTO_TOGGLE	FIELD_ID	Output
1 (On)	0 (Disable)	1 (Auto)	don't care	VSYNC, Field ID
0 (Off)	0 (Disable)	1 (Auto)	don't care	
1 (On)	1 (Enable)	0 (By user)	0 : Top 1 : Bottom	VSYNC, Field ID
0 (Off)	1 (Enable)	0 (By user)	0 : Top 1 : Bottom	
1 (On)	0 (Disable)	1 (Auto)	don't care	VSYNC, Field ID
0 (Off)	0 (Disable)	0 (By user)	0 : Top 1 : Bottom	VSYNC, Field ID

Figure 8-5 Examples of Usage Cases

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8.4.1.6 Video Processor Luminance Image Size Control Register (VP_IMG_SIZE_Y, R/W, Address = 0xF910_0014)

VP_IMG_SIZE_Y	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
VP_IMG_HSIZE_Y	[29:16]	Horizontal size of image (8~8192). (Without minus 1). LSB [2:0] must be 3'b000 for 64-bit interface. Zero value and values greater than 8192 are not allowed.	0
Reserved	[15:14]	Reserved, read as zero, do not modify	0
VP_IMG_VSIZE_Y	[13:0]	Vertical size of image (1 ~ 8192)	0

8.4.1.7 Video Processor Chrominance Image Size Control Register (VP_IMG_SIZE_C, R/W, Address = 0xF910_0018)

VP_ IMG _SIZE_C	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
VP_IMG_HSIZE_C	[29:16]	Horizontal size of image (8~8192). (Without minus 1). LSB [2:0] must be 3'b000 for 64-bit interface. Zero value and values greater than 8192 are not allowed.	0
Reserved	[15:14]	Reserved, read as zero, do not modify	0
VP_IMG_VSIZE_C	[13:0]	Vertical size of image (1 ~ 8192)	0

8.4.1.8 Video Processor Top Luminance Picture Pointer Control Register (VP_TOP_Y_PTR, R/W, Address = 0xF910_0028)

VP_TOP_Y_PTR	Bit	Description	Initial State
VP_TOP_Y_PTR	[31:0]	Base address for luminance of top field. It should be integer multiples of 8. (LSB[2:0] must be 3'b000)	0

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8.4.1.9 Video Processor Bottom Luminance Picture Pointer Control Register (VP_BOT_Y_PTR, R/W, Address = 0xF910_002C)

VP_TOP_C_PTR	Bit	Description	Initial State
VP_BOT_Y_PTR	[31:0]	Base address for luminance of bottom field. It should be integer multiples of 8. (LSB[2:0] must be 3'b000) If TILE mode is enable, VP_BOT_Y_PTR = VP_TOP_Y_PTR + 0x40	0

8.4.1.10 Video Processor Top Chrominance Picture Pointer Control Register (VP_TOP_C_PTR, R/W, Address = 0xF910_0030)

VP_CR_PTR	Bit	Description	Initial State
VP_TOP_C_PTR	[31:0]	Base address for chrominance of top field. It should be integer multiples of 8. (LSB[2:0] must be 3'b000)	0

8.4.1.11 Video Processor Bottom Chrominance Picture Pointer Control Register (VP_BOT_C_PTR, R/W, Address = 0xF910_0034)

VP_BOT_Y_PTR	Bit	Description	Initial State
VP_BOT_C_PTR	[31:0]	Base address for chrominance of bottom field. It should be integer multiples of 8. (LSB[2:0] must be 3'b000) If TILE mode is enable, VP_BOT_C_PTR = VP_TOP_C_PTR + 0x40	0

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8.4.1.12 Video Processor Picture Endian Mode Control Register (VP_ENDIAN_MODE, R/W, Address = 0xF910_03CC)

VP_ENDIAN_MODE	Bit	Description	Initial State
Reserved	[31:1]	Reserved, read as zero, do not modify	0
VP_ENDIAN_MODE	[0]	0 = Big Endian 1 = Little Endian Refer to *Figure 8-6*	0

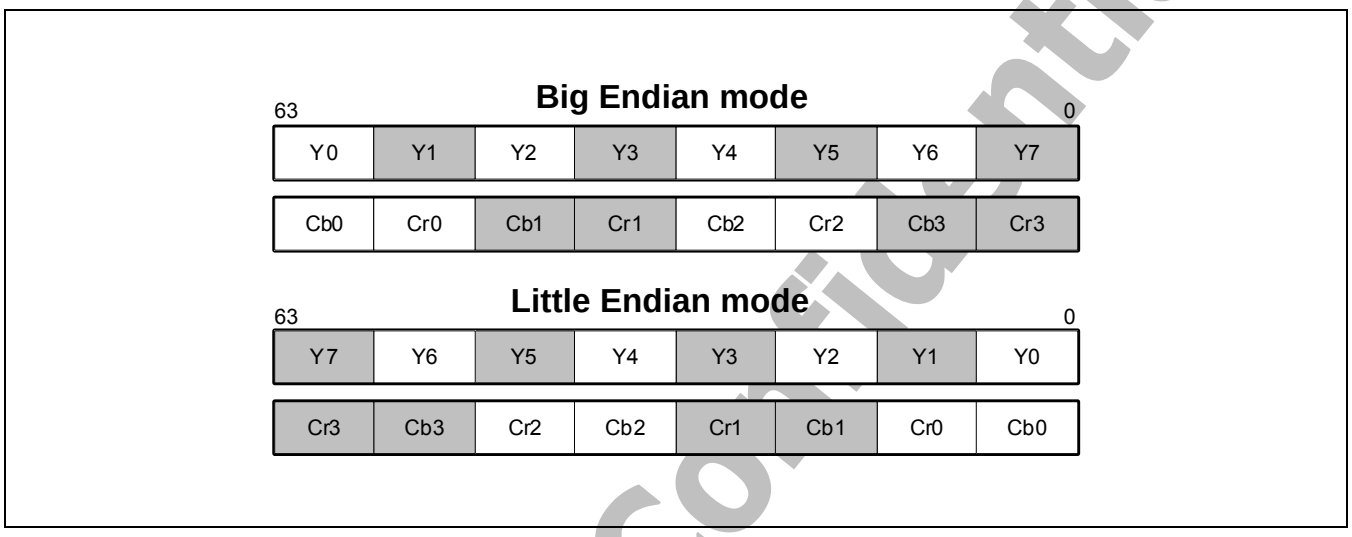

Figure 8-6 Endian Mode

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8.4.1.13 Video Processor Horizontal Offset of Source Image Control Register (VP_SRC_H_POSITION, R/W, Address = 0xF910_0044)

VP_SRC_H_POSITION	Bit	Description	Initial State
Reserved	[31:15]	Reserved, read as zero, do not modify	0
VP_SRC_H_POSITION	[14:0]	Horizontal offset in the source image - (11.4) format * For source image cropping, VP_SRC_H_POSITION + VP_SRC_WIDTH should be less than or equal to VP_IMG_HSIZE_Y Note: (11.4) format means that - '11' is an integer. - '4' is a fraction. Example) In case of H Position = 4 4(0x4(h) = 0100(b)) is integer. Due to 4-bit fraction, 0100(b) is had to do 4 time left shift operation. As a result, register value is 4 * 2^4 = 64 = 0x40.	0

8.4.1.14 Video Processor Vertical Offset of Source Image Control Register (VP_SRC_V_POSITION, R/W, Address = 0xF910_0048)

VP_SRC_V_POSITION	Bit	Description	Initial State
Reserved	[31:10]	Reserved, read as zero, do not modify	0
VP_SRC_V_POSITION	[10:0]	Vertical offset in the source image. This value should be in the range between 0 and VP_SRC_HEIGHT. If LINE_SKIP is 1, VP_SRC_V_POSITION should be a half of that if LINE_SKIP is 0.	0

8.4.1.15 Video Processor Width of Source Image Control Register (VP_SRC_WIDTH, R/W, Address = 0xF910_004C)

VP_SRC_WIDTH	Bit	Description	Initial State
Reserved	[31:11]	Reserved, read as zero, do not modify	0
VP_SRC_WIDTH	[10:0]	Width of the source image (MIN: 32)	0

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8.4.1.16 Video Processor Height of Source Image Control Register (VP_SRC_HEIGHT, R/W, Address = 0xF910_0050)

VP_SRC_HEIGHT	Bit	Description	Initial State
Reserved	[31:10]	Reserved, read as zero, do not modify	0
VP_SRC_HEIGHT	[10:0]	Height of the source image If LINE_SKIP is 1, VP_SRC_HEIGHT should be a half of that if LINE_SKIP is 0. (MIN: 4)	0

8.4.1.17 Video Processor Horizontal Offset of Destination Image Control Register (VP_DST_H_POSITION, R/W, Address = 0xF910_0054)

VP_DST_H_POSITION	Bit	Description	Initial State
Reserved	[31:11]	Reserved, read as zero, do not modify	0
VP_DST_H_POSITION	[10:0]	Horizontal offset in the display	0

8.4.1.18 Video Processor Vertical Offset of Destination Image Control Register (VP_DST_V_POSITION, R/W, Address = 0xF910_0058)

VP_DST_V_POSITION	Bit	Description	Initial State
Reserved	[31:10]	Reserved, read as zero, do not modify	0
VP_DST_V_POSITION	[10:0]	Vertical offset in the display	0

8.4.1.19 Video Processor Width of Destination Image Control Register (VP_DST_WIDTH, R/W, Address = 0xF910_005C)

VP_DST_WIDTH	Bit	Description	Initial State
Reserved	[31:11]	Reserved, read as zero, do not modify	0
VP_DST_WIDTH	[10:0]	Width of the display	0

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8.4.1.20 Video Processor Height of Destination Image Control Register (VP_DST_HEIGHT, R/W, Address = 0xF910_0060)

VP_DST_HEIGHT	Bit	Description	Initial State
Reserved	[31:10]	Reserved, read as zero, do not modify	0
VP_DST_HEIGHT	[10:0]	Height of the display	0

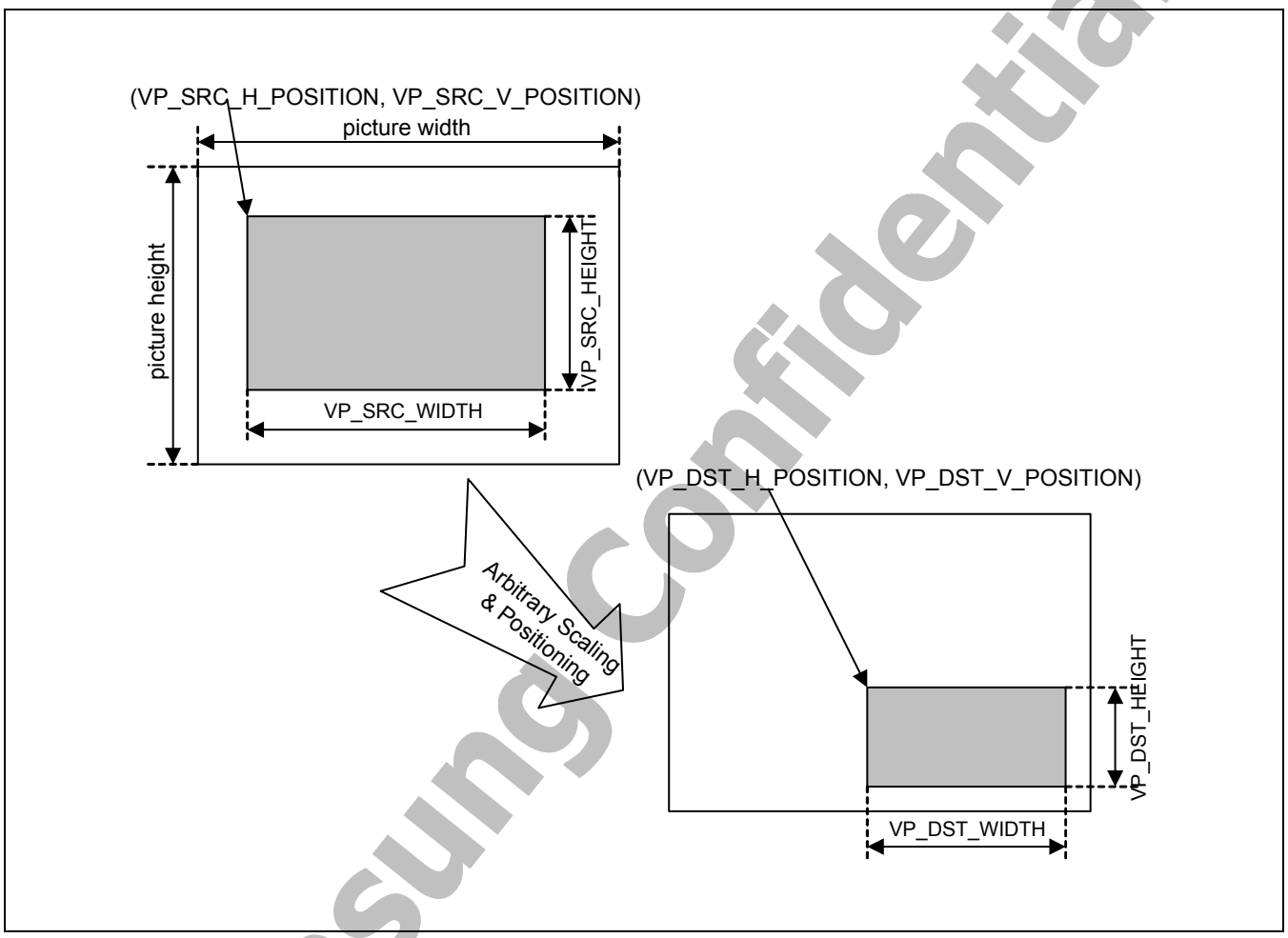

Figure 8-7 Video Scaling & Positioning on TV Display

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8.4.1.21 Video Processor Horizontal Zoom Ratio (VP_H_RATIO, R/W, Address = 0xF910_0064)

VP_H_RATIO	Bit	Description	Initial State
Reserved	[31:19]	Reserved, read as zero, do not modify	0
VP_H_RATIO	[18:0]	Horizontal zoom ratio of SRC:DST - 3.16 format Note: (3.16) format means that - '3' is an integer. - '16' is a fraction. Example) SRC : DST = 1 : 2 Because of 16-bit fraction, it is had to do 16 time left shift operation. As a result, register value is 1/2 * 2^16 = 0x8000	0

8.4.1.22 Video Processor Vertical Zoom Ratio (VP_V_RATIO, R/W, Address = 0xF910_0068)

VP_V_RATIO	Bit	Description	Initial State
Reserved	[31:19]	Reserved, read as zero, do not modify	0
VP_V_RATIO	[18:0]	Vertical zoom ratio of SRC:DST - 3.16 format This register should be as follows. (1) BOB mode, IPC disable VP_V_RATIO = SRC / DST (2) BOB mode, IPC enable VP_V_RATIO = 2 * SRC / DST (This is because destination line number is doubled by de-interlacing process itself) Note: (3.16) format means that - '3' is an integer. - '16' is a fraction. Example) SRC: DST = 1 : 2 Due to 16-bit fraction, it had to do 16 time left shift operation. As a result, register value is 1/2 * 2^16 = 0x8000	0

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8.4.1.23 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y0_LL, R/W, Address = 0xF910_006C

VP_POLY8_Y0_LL	Bit	Description	Initial State
Reserved	[31:27]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph0	[26:24]	Poly-phase Filter Coefficients	0
Reserved	[23:19]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph1	[18:16]	Poly-phase Filter Coefficients	0
Reserved	[15:11]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph2	[10:8]	Poly-phase Filter Coefficients	0
Reserved	[7:3]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph3	[2:0]	Poly-phase Filter Coefficients	0

8.4.1.24 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y0_LH, R/W, Address = 0xF910_0070)

VP_POLY8_Y0_LH	Bit	Description	Initial State
Reserved	[31:27]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph4	[26:24]	Poly-phase Filter Coefficients	0
Reserved	[23:19]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph5	[18:16]	Poly-phase Filter Coefficients	0
Reserved	[15:11]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph6	[10:8]	Poly-phase Filter Coefficients	0
Reserved	[7:3]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph7	[2:0]	Poly-phase Filter Coefficients	0

8.4.1.25 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y0_HL, R/W, Address = 0xF910_0074)

VP_POLY8_Y0_HL	Bit	Description	Initial State
Reserved	[31:27]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph8	[26:24]	Poly-phase Filter Coefficients	0
Reserved	[23:19]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph9	[18:16]	Poly-phase Filter Coefficients	0
Reserved	[15:11]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph10	[10:8]	Poly-phase Filter Coefficients	0
Reserved	[7:3]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph11	[2:0]	Poly-phase Filter Coefficients	0

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8.4.1.26 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y0_HH, R/W, Address = 0xF910_0078)

VP_POLY8_Y0_HH	Bit	Description	Initial State
Reserved	[31:27]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph12	[26:24]	Poly-phase Filter Coefficients	0
Reserved	[23:19]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph13	[18:16]	Poly-phase Filter Coefficients	0
Reserved	[15:11]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph14	[10:8]	Poly-phase Filter Coefficients	0
Reserved	[7:3]	Reserved, read as zero, do not modify	0
vp_poly8_y0_ph15	[2:0]	Poly-phase Filter Coefficients	0

8.4.1.27 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y1_LL, R/W, Address = 0xF910_007C)

VP_POLY8_Y1_LL	Bit	Description	Initial State
Reserved	[31:29]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph0	[28:24]	Poly-phase Filter Coefficients	0
Reserved	[23:21]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph1	[20:16]	Poly-phase Filter Coefficients	0
Reserved	[15:13]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph2	[12:8]	Poly-phase Filter Coefficients	0
Reserved	[7:5]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph3	[4:0]	Poly-phase Filter Coefficients	0

8.4.1.28 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y1_LH, R/W, Address = 0xF910_0080)

VP_POLY8_Y1_LH	Bit	Description	Initial State
Reserved	[31:29]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph4	[28:24]	Poly-phase Filter Coefficients	0
Reserved	[23:21]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph5	[20:16]	Poly-phase Filter Coefficients	0
Reserved	[15:13]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph6	[12:8]	Poly-phase Filter Coefficients	0
Reserved	[7:5]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph7	[4:0]	Poly-phase Filter Coefficients	0

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8.4.1.29 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y1_HL, R/W, Address = 0xF910_0084)

VP_POLY8_Y1_HL	Bit	Description	Initial State
Reserved	[31:29]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph8	[28:24]	Poly-phase Filter Coefficients	0
Reserved	[23:21]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph9	[20:16]	Poly-phase Filter Coefficients	0
Reserved	[15:13]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph10	[12:8]	Poly-phase Filter Coefficients	0
Reserved	[7:5]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph11	[4:0]	Poly-phase Filter Coefficients	0

8.4.1.30 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y1_HH, R/W, Address = 0xF910_0088)

VP_POLY8_Y1_HH	Bit	Description	Initial State
Reserved	[31:29]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph12	[28:24]	Poly-phase Filter Coefficients	0
Reserved	[23:21]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph13	[20:16]	Poly-phase Filter Coefficients	0
Reserved	[15:13]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph14	[12:8]	Poly-phase Filter Coefficients	0
Reserved	[7:5]	Reserved, read as zero, do not modify	0
vp_poly8_y1_ph15	[4:0]	Poly-phase Filter Coefficients	0

8.4.1.31 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y2_LL, R/W, Address = 0xF910_008C)

VP_POLY8_Y2_LL	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph0	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph1	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph2	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph3	[6:0]	Poly-phase Filter Coefficients	0

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8.4.1.32 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y2_LH, R/W, Address = 0xF910_0090)

VP_POLY8_Y2_LH	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph4	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph5	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph6	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph7	[6:0]	Poly-phase Filter Coefficients	0

8.4.1.33 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y2_HL, R/W, Address = 0xF910_0094)

VP_POLY8_Y2_HL	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph8	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph9	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph10	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph11	[6:0]	Poly-phase Filter Coefficients	0

8.4.1.34 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y2_HH, R/W, Address = 0xF910_0098)

VP_POLY8_Y2_HH	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph12	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph13	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph14	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly8_y2_ph15	[6:0]	Poly-phase Filter Coefficients	0

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8.4.1.35 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y3_LL, R/W, Address = 0xF910_009C)

VP_POLY8_Y3_LL	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph0	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph1	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph2	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph3	[6:0]	Poly-phase Filter Coefficients	0

8.4.1.36 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y3_LH R/W, Address = 0xF910_00A0)

VP_POLY8_Y3_LH	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph4	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph5	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph6	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph7	[6:0]	Poly-phase Filter Coefficients	0

8.4.1.37 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y3_HL, R/W, Address = 0xF910_00A4)

VP_POLY8_Y3_HL	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph8	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph9	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph10	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph11	[6:0]	Poly-phase Filter Coefficients	0

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8.4.1.38 Video Processor Luminance 8-tap Poly-phase Filter Coefficients (VP_POLY8_Y3_HH, R/W, Address = 0xF910_00A8)

VP_POLY8_Y3_HH	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph12	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph13	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph14	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly8_y3_ph15	[6:0]	Poly-phase Filter Coefficients	0

8.4.1.39 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y0_LL, R/W, Address = 0xF910_00EC)

VP_POLY4_Y0_LL	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph0	[29:24]	Poly-phase Filter Coefficients	0
Reserved	[23:22]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph1	[21:16]	Poly-phase Filter Coefficients	0
Reserved	[15:14]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph2	[13:8]	Poly-phase Filter Coefficients	0
Reserved	[7:6]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph3	[5:0]	Poly-phase Filter Coefficients	0

8.4.1.40 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y0_LH, R/W, Address = 0xF910_00F0)

VP_POLY4_Y0_LH	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph4	[29:24]	Poly-phase Filter Coefficients	0
Reserved	[23:22]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph5	[21:16]	Poly-phase Filter Coefficients	0
Reserved	[15:14]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph6	[13:8]	Poly-phase Filter Coefficients	0
Reserved	[7:6]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph7	[5:0]	Poly-phase Filter Coefficients	0

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8.4.1.41 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y0_HL, R/W, Address = 0xF910_00F4)

VP_POLY4_Y0_HL	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph8	[29:24]	Poly-phase Filter Coefficients	0
Reserved	[23:22]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph9	[21:16]	Poly-phase Filter Coefficients	0
Reserved	[15:14]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph10	[13:8]	Poly-phase Filter Coefficients	0
Reserved	[7:6]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph11	[5:0]	Poly-phase Filter Coefficients	0

8.4.1.42 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y0_HH, R/W, Address = 0xF910_00F8)

VP_POLY4_Y0_HH	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph12	[29:24]	Poly-phase Filter Coefficients	0
Reserved	[23:22]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph13	[21:16]	Poly-phase Filter Coefficients	0
Reserved	[15:14]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph14	[13:8]	Poly-phase Filter Coefficients	0
Reserved	[7:6]	Reserved, read as zero, do not modify	0
vp_poly4_y0_ph15	[5:0]	Poly-phase Filter Coefficients	0

8.4.1.43 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y1_LL, R/W, Address = 0xF910_00FC)

VP_POLY4_Y1_LL	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph0	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph1	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph2	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph3	[6:0]	Poly-phase Filter Coefficients	0

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8.4.1.44 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y1_LH, R/W, Address = 0xF910_0100)

VP_POLY4_Y1_LH	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph4	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph5	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph6	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph7	[6:0]	Poly-phase Filter Coefficients	0

8.4.1.45 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y1_HL, R/W, Address = 0xF910_0104)

VP_POLY4_Y1_HL	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph8	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph9	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph10	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph11	[6:0]	Poly-phase Filter Coefficients	0

8.4.1.46 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y1_HH, R/W, Address = 0xF910_0108)

VP_POLY4_Y1_HH	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph12	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph13	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph14	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly4_y1_ph15	[6:0]	Poly-phase Filter Coefficients	0

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8.4.1.47 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y2_LL, R/W, Address = 0xF910_010C)

VP_POLY4_Y2_LL	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph0	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph1	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph2	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph3	[6:0]	Poly-phase Filter Coefficients	0

8.4.1.48 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y2_LH, R/W, Address = 0xF910_0110)

VP_POLY4_Y2_LH	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph4	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph5	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph6	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph7	[6:0]	Poly-phase Filter Coefficients	0

8.4.1.49 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y2_HL, R/W, Address = 0xF910_0114)

VP_POLY4_Y2_HL	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph8	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph9	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph10	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph11	[6:0]	Poly-phase Filter Coefficients	0

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8.4.1.50 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y2_HH, R/W, Address = 0xF910_0118)

VP_POLY4_Y2_HH	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph12	[30:24]	Poly-phase Filter Coefficients	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph13	[22:16]	Poly-phase Filter Coefficients	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph14	[14:8]	Poly-phase Filter Coefficients	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly4_y2_ph15	[6:0]	Poly-phase Filter Coefficients	0

8.4.1.51 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y3_LL, R/W, Address = 0xF910_011C)

VP_POLY4_Y3_LL	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph0	[29:24]	Poly-phase Filter Coefficients	0
Reserved	[23:22]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph1	[21:16]	Poly-phase Filter Coefficients	0
Reserved	[15:14]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph2	[13:8]	Poly-phase Filter Coefficients	0
Reserved	[7:6]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph3	[5:0]	Poly-phase Filter Coefficients	0

8.4.1.52 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y3_LH, R/W, Address = 0xF910_0120)

VP_POLY4_Y3_LH	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph4	[29:24]	Poly-phase Filter Coefficients	0
Reserved	[23:22]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph5	[21:16]	Poly-phase Filter Coefficients	0
Reserved	[15:14]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph6	[13:8]	Poly-phase Filter Coefficients	0
Reserved	[7:6]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph7	[5:0]	Poly-phase Filter Coefficients	0

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8.4.1.53 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y3_HL, R/W, Address = 0xF910_0124)

VP_POLY4_Y3_HL	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph8	[29:24]	Poly-phase Filter Coefficients	0
Reserved	[23:22]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph9	[21:16]	Poly-phase Filter Coefficients	0
Reserved	[15:14]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph10	[13:8]	Poly-phase Filter Coefficients	0
Reserved	[7:6]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph11	[5:0]	Poly-phase Filter Coefficients	0

8.4.1.54 Video Processor Luminance 4-tap Poly-phase Filter Coefficients (VP_POLY4_Y3_HH, R/W, Address = 0xF910_0128)

VP_POLY4_Y3_LL	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph12	[29:24]	Poly-phase Filter Coefficients	0
Reserved	[23:22]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph13	[21:16]	Poly-phase Filter Coefficients	0
Reserved	[15:14]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph14	[13:8]	Poly-phase Filter Coefficients	0
Reserved	[7:6]	Reserved, read as zero, do not modify	0
vp_poly4_y3_ph15	[5:0]	Poly-phase Filter Coefficients	0

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8.4.1.55 Video Processor Chrominance 4-tap Poly-phase Filter Coefficients (VP_POLY4_C0_LL, R/W, Address = 0xF910_012C)

Unlike VP_POLY4_Y registers, there are only a half of the coefficient registers for horizontal Chroma Scaler. The coefficients are assumed to be symmetric so that only half of them are kept. Some parts of them are unsigned integer and the other parts are signed integer. You must be careful while setting them.

VP_POLY4_C0_LL	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph0	[30:24]	Signed 7-bit integer (-64~63)	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph1	[22:16]	Signed 7-bit integer (-64~63)	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph2	[14:8]	Signed 7-bit integer (-64~63)	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph3	[6:0]	Signed 7-bit integer (-64~63)	0

8.4.1.56 Video Processor Chrominance 4-tap Poly-phase Filter Coefficients (VP_POLY4_C0_LH, R/W, Address = 0xF910_0130)

VP_POLY4_C0_LH	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph4	[29:24]	Signed 6-bit integer (-32~31)	0
Reserved	[23:22]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph5	[21:16]	Signed 6-bit integer (-32~31)	0
Reserved	[15:14]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph6	[13:8]	Signed 6-bit integer (-32~31)	0
Reserved	[7:6]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph7	[5:0]	Signed 6-bit integer (-32~31)	0

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8.4.1.57 Video Processor Chrominance 4-tap Poly-phase Filter Coefficients (VP_POLY4_C0_HL, R/W, Address = 0xF910_0134)

VP_POLY4_C0_HL	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph8	[29:24]	Signed 6-bit integer (-32~31)	0
Reserved	[23:22]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph9	[21:16]	Signed 6-bit integer (-32~31)	0
Reserved	[15:14]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph10	[13:8]	Signed 6-bit integer (-32~31)	0
Reserved	[7:6]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph11	[5:0]	Signed 6-bit integer (-32~31)	0

8.4.1.58 Video Processor Chrominance 4-tap Poly-phase Filter Coefficients (VP_POLY4_C0_HH, R/W, Address = 0xF910_0138)

VP_POLY4_C0_HH	Bit	Description	Initial State
Reserved	[31:29]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph12	[28:24]	Signed 5-bit integer (-16~15)	0
Reserved	[23:21]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph13	[20:16]	Signed 5-bit integer (-16~15)	0
Reserved	[15:13]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph14	[12:8]	Signed 5-bit integer (-16~15)	0
Reserved	[7:5]	Reserved, read as zero, do not modify	0
vp_poly4_c0_ph15	[4:0]	Signed 5-bit integer (-16~15)	0

8.4.1.59 Video Processor Chrominance 4-tap Poly-phase Filter Coefficients (VP_POLY4_C1_LL, R/W, Address = 0xF910_013C)

VP_POLY4_C1_LL	Bit	Description	Initial State
vp_poly4_c1_ph0	[31:24]	Unsigned 8-bit integer (0~255)	0
vp_poly4_c1_ph1	[23:16]	Unsigned 8-bit integer (0~255)	0
vp_poly4_c1_ph2	[15:8]	Unsigned 8-bit integer (0~255)	0
vp_poly4_c1_ph3	[7:0]	Unsigned 8-bit integer (0~255)	0

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8.4.1.60 Video Processor Chrominance 4-tap Poly-phase Filter Coefficients (VP_POLY4_C1_LH, R/W, Address = 0xF910_0140)

VP_POLY4_C1_LH	Bit	Description	Initial State
vp_poly4_c1_ph4	[31:24]	Unsigned 8-bit integer (0~255)	0
vp_poly4_c1_ph5	[23:16]	Unsigned 8-bit integer (0~255)	0
vp_poly4_c1_ph6	[15:8]	Unsigned 8-bit integer (0~255)	0
vp_poly4_c1_ph7	[7:0]	Unsigned 8-bit integer (0~255)	0

8.4.1.61 Video Processor Chrominance 4-tap Poly-phase Filter Coefficients (VP_POLY4_C1_HL, R/W, Address = 0xF910_0144)

VP_POLY4_C1_HL	Bit	Description	Initial State
vp_poly4_c1_ph8	[31:24]	Unsigned 8-bit integer (0~255)	0
vp_poly4_c1_ph9	[23:16]	Signed 8-bit integer (-128~127)	0
vp_poly4_c1_ph10	[15:8]	Signed 8-bit integer (-128~127)	0
vp_poly4_c1_ph11	[7:0]	Signed 8-bit integer (-128~127)	0

8.4.1.62 Video Processor Chrominance 4-tap Poly-phase Filter Coefficients (VP_POLY4_C1_HH, R/W, Address = 0xF910_0148)

VP_POLY4_C1_HH	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	0
vp_poly4_c1_ph12	[30:24]	Signed 7-bit integer (-64~63)	0
Reserved	[23]	Reserved, read as zero, do not modify	0
vp_poly4_c1_ph13	[22:16]	Signed 7-bit integer (-64~63)	0
Reserved	[15]	Reserved, read as zero, do not modify	0
vp_poly4_c1_ph14	[14:8]	Signed 7-bit integer (-64~63)	0
Reserved	[7]	Reserved, read as zero, do not modify	0
vp_poly4_c1_ph15	[6:0]	Signed 7-bit integer (-64~63)	0

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8.4.1.63 Video Processor Post-processing Color Space Conversion Coefficient Register (PP_CSC_Y2Y_COEF, R/W, Address = 0xF910_01D4)

- BT.601 to BT.709 Color Space Conversion Matrix
  - Y709 = 1.0 * Y601 – 0.118188 * Cb601 – 0.212685 * Cr601
  - Cb709 = 0.0 * Y601 + 1.018640 * Cb601 – 0.114618 * Cr601
  - Cr709 = 0.0 * Y601 + 0.075049 * Cb601 + 1.025327 * Cr601

- BT.709 to BT.601 Color Space Conversion Matrix
  - Y601 = 1.0 * Y709 + 0.101579 * Cb709 + 0.196076 * Cr709
  - Cb601 = 0.0 * Y709 + 0.989854 * Cb709 – 0.110653 * Cr709
  - Cr601 = 0.0 * Y709 – 0.072453 * Cb709 + 0.983398 * Cr709

- Above all equations are written without interface offsets of +16 for Luminance and +128 for Chrominance.
- CSC module calculates above all equations without +128 offset for Chrominance, and generates final CSC results with +128 offset.
- In case of two Luminance equations, +16 offset is selectable by control register (PP_CSC_EN [1]). If Y offset (+16) exists in matrix input data, the coefficient of above equations should be redefined.

PP_CSC_Y2Y_COEF	Bit	Description	Initial State
Reserved	[31:12]	Reserved, read as zero, do not modify	0
PP_CSC_Y2Y_COEF	[11:0]	BT.601 to BT.709 (or BT.709 to BT.601) CSC coefficient for Y to Y [11]: Sign bit [10]: Integer bit [9:0]: Fraction bit 0x7FF: 1.999 … 0x400: 1.0 … 0x0: 0 0xFFF: - 0.0001 … 0xC00: - 1.0 … 0x800: - 2.0	0

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8.4.1.64 Video Processor Post-processing Color Space Conversion Coefficient Register (PP_CSC_CB2Y_COEF, R/W, Address = 0xF910_01D8)

PP_CSC_CB2Y_COEF	Bit	Description	Initial State
Reserved	[31:12]	Reserved, read as zero, do not modify	0
PP_CSC_CB2Y_COEF	[11:0]	BT.601 to BT.709 (or BT.709 to BT.601) CSC coefficient for CB to Y	0

8.4.1.65 Video Processor Post-processing Color Space Conversion Coefficient Register (PP_CSC_CR2Y_COEF, R/W, Address = 0xF910_01DC)

PP_CSC_CR2Y_COEF	Bit	Description	Initial State
Reserved	[31:12]	Reserved, read as zero, do not modify	0
PP_CSC_CR2Y_COEF	[11:0]	BT.601 to BT.709 (or BT.709 to BT.601) CSC coefficient for CR to Y	0

8.4.1.66 Video Processor Post-processing Color Space Conversion Coefficient Register (PP_CSC_Y2CB_COEF, R/W, Address = 0xF910_01E0)

PP_CSC_Y2CB_COEF	Bit	Description	Initial State
Reserved	[31:12]	Reserved, read as zero, do not modify	0
PP_CSC_Y2CB_COEF	[11:0]	BT.601 to BT.709 (or BT.709 to BT.601) CSC coefficient for Y to CB	0

8.4.1.67 Video Processor Post-processing Color Space Conversion Coefficient Register (PP_CSC_CB2CB_COEF, R/W, Address = 0xF910_01E4)

PP_CSC_CB2CB_COEF	Bit	Description	Initial State
Reserved	[31:12]	Reserved, read as zero, do not modify	0
PP_CSC_CB2CB_COEF	[11:0]	BT.601 to BT.709 (or BT.709 to BT.601) CSC coefficient for CB to CB	0

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8.4.1.68 Video Processor Post-processing Color Space Conversion Coefficient Register (PP_CSC_CR2CB_COEF, R/W, Address = 0xF910_01F0)

PP_CSC_CR2CB_COEF	Bit	Description	Initial State
Reserved	[31:12]	Reserved, read as zero, do not modify	0
PP_CSC_CR2CB_COEF	[11:0]	BT.601 to BT.709 (or BT.709 to BT.601) CSC coefficient for CR to CB	0

8.4.1.69 Video Processor Post-processing Color Space Conversion Coefficient Register (PP_CSC_Y2CR_COEF, R/W, Address = 0xF910_01EC)

PP_CSC_Y2CR_COEF	Bit	Description	Initial State
Reserved	[31:12]	Reserved, read as zero, do not modify	0
PP_CSC_Y2CR_COEF	[11:0]	BT.601 to BT.709 (or BT.709 to BT.601) CSC coefficient for Y to CR	0

8.4.1.70 Video Processor Post-processing Color Space Conversion Coefficient Register (PP_CSC_CB2CR_COEF, R/W, Address = 0xF910_01E8)

PP_CSC_CB2CR_COEF	Bit	Description	Initial State
Reserved	[31:12]	Reserved, read as zero, do not modify	0
PP_CSC_CB2CR_COEF	[11:0]	BT.601 to BT.709 (or BT.709 to BT.601) CSC coefficient for CB to CR	0

8.4.1.71 Video Processor Post-processing Color Space Conversion Coefficient Register (PP_CSC_CR2CR_COEF, R/W, Address = 0xF910_01F4)

PP_CSC_CR2CR_COEF	Bit	Description	Initial State
Reserved	[31:12]	Reserved, read as zero, do not modify	0
PP_CSC_CR2CR_COEF	[11:0]	BT.601 to BT.709 (or BT.709 to BT.601) CSC coefficient for CR to CR	0

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8.4.1.72 Video Processor Post-processing Image Bypass Mode Control Register (PP_BYPASS, R/W, Address = 0xF910_0200)

PP_BYPASS	Bit	Description	Initial State
Reserved	[31:1]	Reserved, read as zero, do not modify	0
PP_BYPASS	[0]	Disables the post image processor This is only for SDTV. We don't recommend you to use functions for HDTV. (Post image processor executes color saturation control, sharpness enhancement, contrast and brightness control.) 0 = Enables 1 = Disables (default)	1

8.4.1.73 Video Processor Color Saturation Control Register (PP_SATURATION, R/W, Address = 0xF910_020C)

PP_SATURATION	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read as zero, do not modify	0
PP_SATURATION	[7:0]	Color saturation factor (Unsigned 1.7 format) 0x00 = 0.0 … 0x80 = 1.0 … 0xFF = 1.992188, (128*2 – 1)/128	80

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8.4.1.74 Video Processor Picture Sharpness Control Register (PP_SHARPNESS, R/W, Address = 0xF910_0210)

PP_SHARPNESS	Bit	Description	Initial State
Reserved	[31:2]	Reserved, read as zero, do not modify	0
PP_TH_HNOISE	[15:8]	Threshold value setting to decide minimum vertical edge value	0x5
Reserved	[7:2]	Reserved, read as zero, do not modify	0
PP_SHARPNESS	[1:0]	Control for the edge enhancement 0 = No effect 1 = Minimum edge enhancement 2 = Moderate edge enhancement 3 = Maximum edge enhancement	0

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8.4.1.75 Video Processor Brightness & Contrast Control Register (PP_LINE_EQ0 ~ PP_LINE_EQ7)

- PP_LINE_EQ0, R/W, Address = 0xF910_0218
- PP_LINE_EQ1, R/W, Address = 0xF910_021C
- PP_LINE_EQ2, R/W, Address = 0xF910_0220
- PP_LINE_EQ3, R/W, Address = 0xF910_0224
- PP_LINE_EQ4, R/W, Address = 0xF910_0228
- PP_LINE_EQ5, R/W, Address = 0xF910_022C
- PP_LINE_EQ6, R/W, Address = 0xF910_0230
- PP_LINE_EQ7, R/W, Address = 0xF910_0234

PP_LINE_EQx	Bit	Description	Initial State
Reserved	[31:24]	Reserved, read as zero, do not modify	0
LINE_INTC	[23:8]	Intercept, signed 9.7 format Note: (9.7) format means that - '1' is a signed bit. - '8' is a integer. - '7' is a fraction. Example) INTC = 3 Due to 7-bit fraction, it is had to do 7 time left shift operation. As a result, register value is 3 * 2^7 = 0x18000	0
LINE_SLOPE	[7:0]	Slope, unsigned 1.7 format. (Due to1-bit integer, LINE_SLOPE has range from 0 to 1.9921875.) Note: (1.7) format means that - '1' is a integer - '7' is a fraction. Example) LINE_SLOPE = 0.5 = 1*2^(-1) Because of 7-bit fraction, it is had to do 7 time left shift operation. As a result, register value is 1/2 * 2^7 = 0x40	0

NOTE: 8 equations are related with Figure 8-8 Input luminance value between 0 ~ 255 is divide by 8 steps. Each of them is matched with each of 8 equations. Thus, we can make the new curve of the contrast and luminance as using 8 equation's combination. Each equation is matched like the following :
- PP_LINE_EQ0 = LINE_SLOPE0 * Y + LINE_INTC0 (0≤Y≤31)
- PP_LINE_EQ1 = LINE_SLOPE1 * Y + LINE_INTC1 (32≤Y≤63)
- PP_LINE_EQ2 = LINE_SLOPE2 * Y + LINE_INTC2 (64≤Y≤95)
- PP_LINE_EQ3 = LINE_SLOPE3 * Y + LINE_INTC3 (96≤Y≤127)
- PP_LINE_EQ4 = LINE_SLOPE4 * Y + LINE_INTC4 (128≤Y≤159)
- PP_LINE_EQ5 = LINE_SLOPE5 * Y + LINE_INTC5 (160≤Y≤191)
- PP_LINE_EQ6 = LINE_SLOPE6 * Y + LINE_INTC6 (192≤Y<223)
- PP_LINE_EQ7 = LINE_SLOPE7 * Y + LINE_INTC7 (224≤Y≤255)

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8.4.1.76 Video Processor Brightness offset Control Register for Y (PP_BRIGHT_OFFSET, R/W, Address = 0xF910_0238)

PP_BRIGHT_OFFSET	Bit	Description	Initial State
Reserved	[31:9]	Reserved, read as zero, do not modify	0
PP_BRIGHT_OFFSET	[8:0]	Offset for Y brightness control (Signed 1.8 format) Bright enhanced Y = Org Y + BRIGHT_OFFSET 0xFF : +255 … 0x1 : + 1 0x0 : 0 0x1FF : – 1 … 0x100 : - 256	0

NOTE: Figure 8-8 shows examples of how VP controls brightness and contrast of image sequence using PP_LINE_EQ0 ~ PP_LINE_EQ7 registers and PP_BRIGHT_OFFSET register. Input to output luminance mapping curve is approximated by 8 sub-lines described by PP_LINE_EQ0 ~ PP_LINE_EQ7. Consequently, brightness and contrast is controlled in very flexible way.

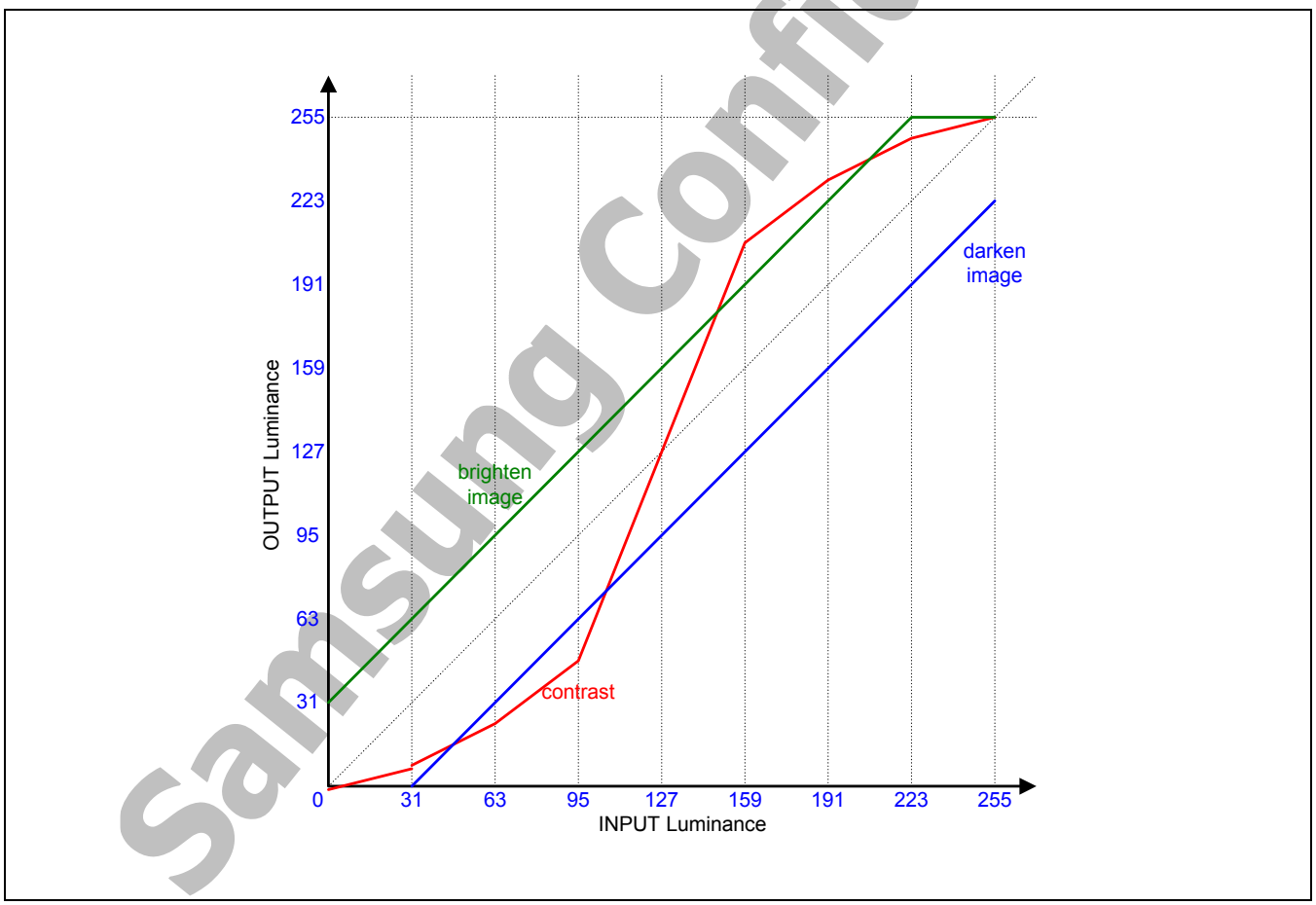

Figure 8-8 Image Brightness & Contrast Control

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8.4.1.77 Video Processor Color Space Conversion Control Register (PP_CSC_EN, R/W, Address = 0xF910_023C)

PP_CSC_EN	Bit	Description	Initial State
Reserved	[31:2]	Reserved, read as zero, do not modify	0

SUB_Y_OFFSET_EN	[1]	Y offset control for color space conversion
		If (SUB_Y_OFFSET_EN == 1)
		Y' = (Y-16)*Y2Y_coef + (Cb-128)*Cb2Y_coef + (Cr-128)* Cr2Y_coef
		Cb' = (Y-16)*Y2Cb_coef + (Cb-128)*Cb2Cb_coef + (Cr-128)*Cr2Cb_coef
		Cr' = (Y-16)*Y2Cr_coef + (Cb-128)*Cb2Cr_coef + (Cr-128)*Cr2Cr_coef
		Else
		Y' = Y*Y2Y_coef + (Cb-128)*Cb2Y_coef + (Cr-128)* Cr2Y_coef
		Cb' = Y*Y2Cb_coef + (Cb-128)*Cb2Cb_coef + (Cr-128)*Cr2Cb_coef
		Cr' = Y*Y2Cr_coef + (Cb-128)*Cb2Cr_coef + (Cr-128)*Cr2Cr_coef
			1

CSC_EN	[0]	Color space conversion enable control 0 = Disable 1 = Enable	0

8.4.1.78 Video Processor Version Information Register (VP_VERSION_INFO, R, Address = 0xF910_03FC)

VP_VERSION_INFO	Bit	Description	Initial State
VERSION_INFO	[31:0]	VP version information	0x0000_0010

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8.4.2 THE IDEA OF POLY-PHASE FILTERING IN VIDEO PROCESSOR

Figure 8-9 shows basic concept of poly-phase filtering in video processor in case of 4-tap vertical luminance filter. Pixels highlighted in grey color are from decoded pictures and used to interpolate the dotted pixels, which are transferred to MIXER. The vertical positions of pixels to be interpolated are calculated with VP_SRC_V_POSITION and VP_V_RATIO. Once the vertical position is calculated, the nearest pixel phase (with 1/16 resolution) and which pixels are used for interpolation are decided.

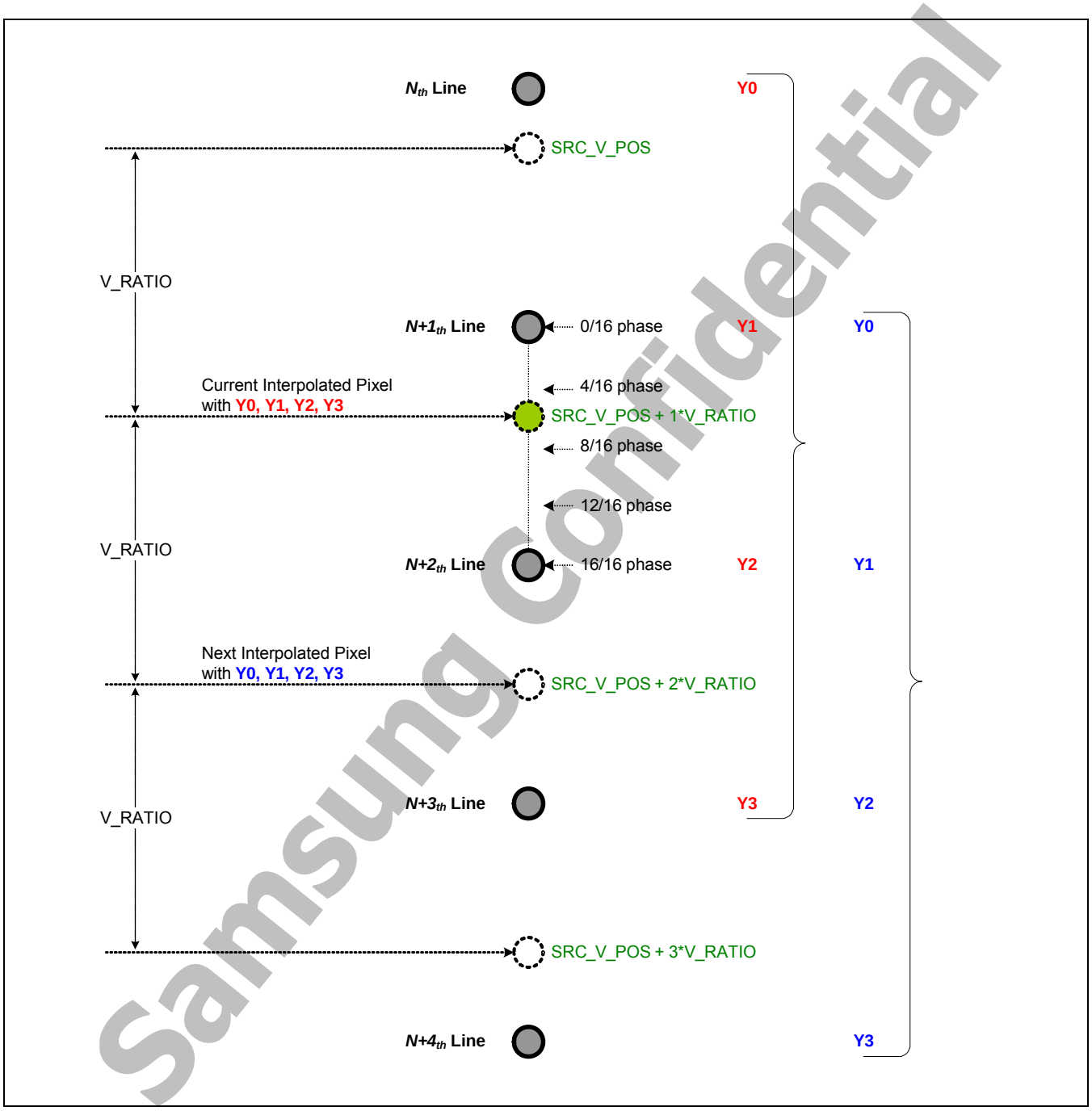

Figure 8-9 4-Tap Vertical Poly-phase Filter

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If the calculated vertical position is 10.45, for example, pixels of 9th, 10th, 11th, and 12th lines are used for poly-phase filtering and the pixel phase is 7/16, which means the filter coefficients are vp_poly4_y0_ph7, vp_poly4_y1_ph7, vp_poly4_y2_ph7, and vp_poly4_y3_ph7.

8-tap luminance horizontal poly-phase filter and 4-tap chrominance horizontal poly-phase filter use the exact same scheme.

At the boundaries of pictures (top, bottom, left, and right), some pixels in filter window are not available. In this case, value of the nearest pixel is repeated as shown in *Figure 8-10*.

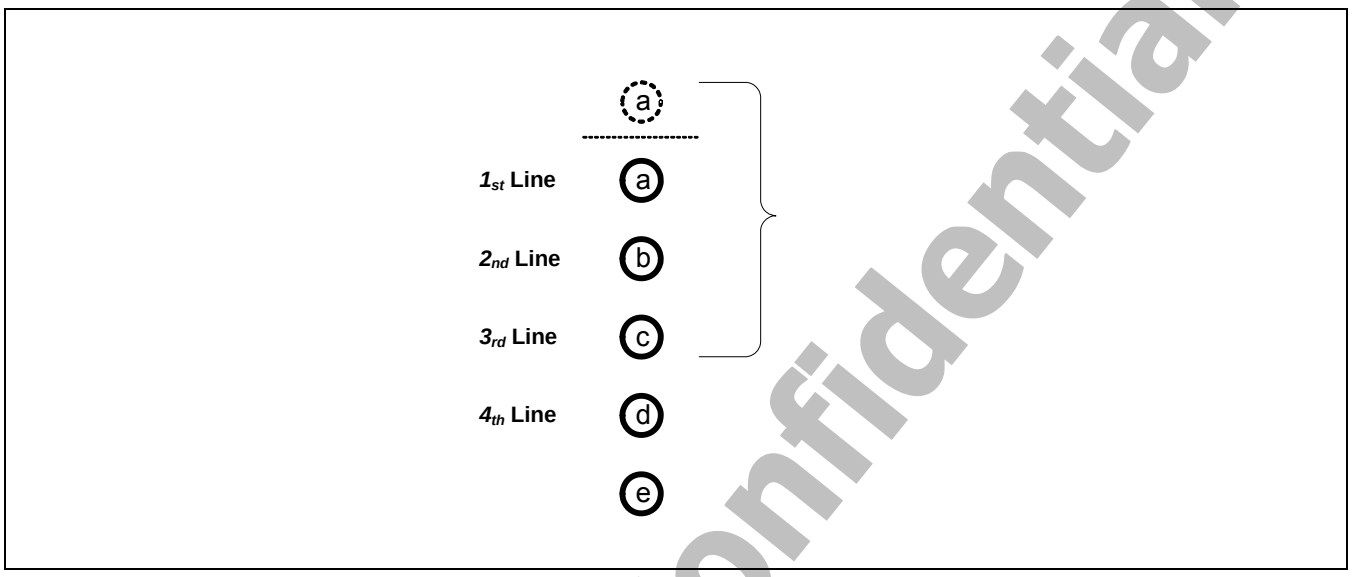

Figure 8-10 Pixel Repetition at Picture Boundary

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9 MIXER

9.1 OVERVIEW OF MIXER

Mixer overlaps or blends the input data such as graphic, video, background and sends the result data to the TVOUT module. The TVOUT module generates all the video control signals.

Graphic data is transferred to the mixer from External DRAM memory via AXI interface. However, the video data is transferred to the mixer via direct connection with pre-defined protocol. The data generated from mixer is directly transferred to TVENC/HDMI module for the real time transfer.

9.1.1 KEY FEATURES OF MIXER

- Supports AXI Master & AHB Slave Interface
- AXI Master interface for graphic layer data fetch
- AHB Slave interface for control register setup
- Supports Little/ Big Endian for graphic layers data
- [Input]
- Multiple Layers
  - Background layer
  - Graphic0 layer
  - Graphic1 layer
  - Video layer
- Input Control features
  - Blending between each layer
  - Selectable graphic layer frame buffer
  - Enable/disable each layer
  - Source cropping for graphic layer
- [Output]
- Overlapped and blended input layers
- YCbCr 4:4:4 / RGB 8:8:8
- Supports interlaced/ progressive scan
- Supports 480i/p, 576i/p, 720p and 1080i/1080p display sizing (1080p is 30Hz.)
- [Graphic0,1 Layer]
- Source: External DRAM frame buffer memory

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- Color Format : differently configurable between each graphic layer
  - 16bpp Direct RGB[565]
  - 16bpp Direct ARGB[1555]
  - 16bpp Direct ARGB[4444]
  - 32bpp Direct ARGB[8888]
- Maximum graphic layer size
  - 480i/p: 720x480 pixels
  - 576i/p: 720x576 pixels
  - 720p: 1280x720 pixels
  - 1080i/p: 1920x1080 pixel
- Blending
  - Maximum 256 level pixel and layer blending
  - Separately configurable layer blending factor between each layer
- Scale
  - Vertical line duplication : x2
  - Horizontal win-scale : x2
- [Video Layer]
- Source: Video processor module
- Color Format: 24bpp Direct YCbCr [888]
- Maximum Resolution
  - 480i/p: 720x480 pixels
  - 576i/p: 720x576 pixels
  - 720p: 1280x720 pixels
  - 1080i/p: 1920x1080 pixels
- The xvYcc limiter is supported.
- [Background layer]
- Source: Configuration register
- Lowest layer
- Layer ordering
- Background → (Video ↔ Graphic0 ↔ Graphic1)
- Video layer and 2 graphic layers are fully ordered and blended
- Blending
- Pixel blending and Layer blending
- Alpha blending
- Pre-multiplied blending

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9.1.2 BLOCK DIAGRAM OF MIXER

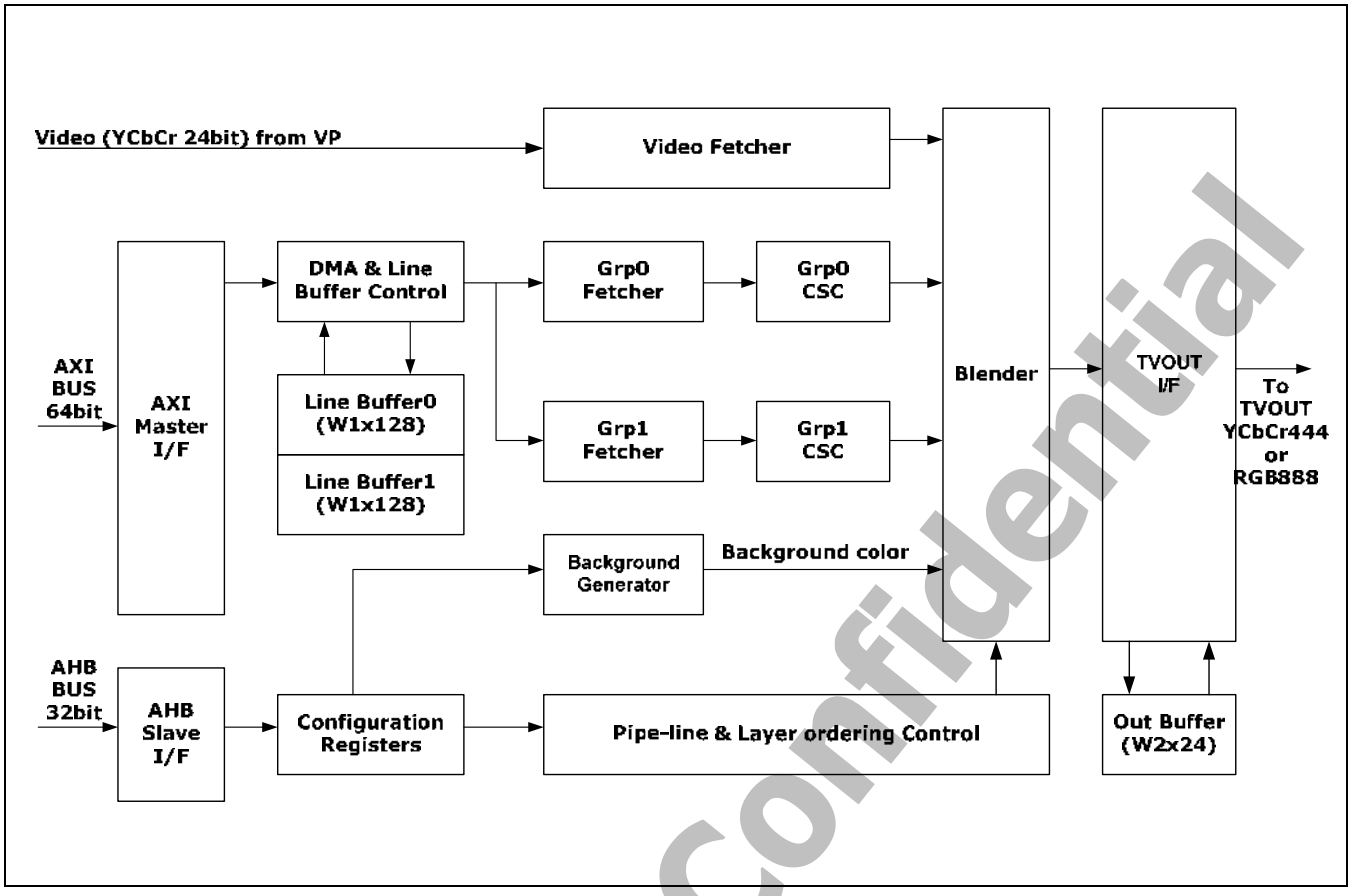

Figure 9-1 Block Diagram of Mixer

AXI Master I/F and DMA & Line Buffer Control: This block fetches data from the memory and stores data in Line Buffer0/1 block.

AHB Slave I/F and Configuration Registers: This block is SFRs to control the mixer.

Video Fetcher: This block fetches data from VP module.

Grp0/1 fetcher and Grp0/1 CSC: Grp0/1 fetchers pop up data from Line Buffer0/1 and delivers image data to Blender block through the color space converters (Grp0/1 CSC).

Background Generator: This block generates background patterns according to configurations.

Blender: The role of this block is to mix 4 image-layers such as Video, Graphic0/1 and Back-ground.

TVOUT I/F: This block temporally stores data from the Blender until either TVENC or HDMI requests data.

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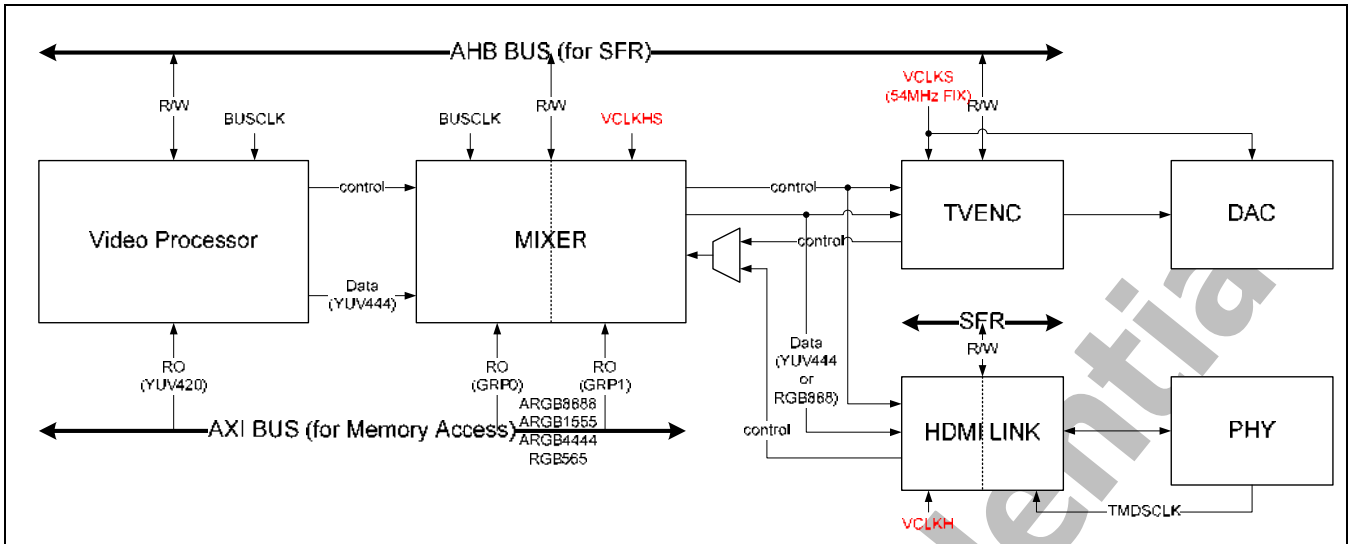
9.1.3 VIDEO CLOCK RELATION



VCLKHS(or VCLKH) usage frequency

Vertical Freq.	Format	Pixel Freq.
59.94 Hz	480P	27MHz (or 54MHz)
	720P	74.175MHz
	1080I	74.175MHz
60.00 Hz	480P	27.027MHz (or 54.054MHz)
	720P	74.250MHz
	1080I	74.250MHz
50.00 Hz	576P	27MHz (or 54MHz)
	720P	74.250MHz
	1080I	74.250MHz
29.97Hz	1080P	74.175MHz
30Hz	1080P	74.250MHz
25Hz	1080P	74.250MHz
Summary		27MHz
		27.027MHz
		54MHz
		54.054MHz
		74.175MHz
		74.250MHz

Figure 9-2 TV Sub-System Block Diagram and Usage Frequency

There are two paths from mixer to TVENC and HDMI. It is selected exclusively at the Clock Controller (refer to REG_DST_SEL at mixer_CFG register (0xF920_ 0004)). When TV-out is selected, Mixer I/F clock (VCLKHS) and VCLKS (TVENC clock) is fixed by 54MHz. Thus, you must set MIXER_SEL register in CLK_SRC1(0xE010_0204) for more information, refer to CMU chapter. Else, in HDMI-out selection, REG_DST_SEL register is configured properly. Then, you set the same clock configuration between MIXER I/F clock (VCLKHS) and VCLKH(HDMI pixel clock). The clock which is generated by embedded PLL in HDMI PHY must be selected using usage frequency table (refer to VCLKHS(or VCLKH. You can configure clock source through CLK_SRC1 register.

9.2 REGISTER DESCRIPTION

9.2.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
Mixer Global Setting				
MIXER_STATUS	0xF920_0000	R/W	Specifies the Status of MIXER Operation	0x0000_0006
MIXER_CFG	0xF920_0004	R/W	Specifies the MIXER Mode Setting	0x0000_0000
Mixer Interrupt				
MIXER_INT_EN	0xF920_0008	R/W	Specifies the Interrupt Enable	0x0000_0000
MIXER_INT_STATUS	0xF920_000C	R/W	Specifies the Interrupt Status	0x0000_0000
Video & Blender Configuration				
MIXER_LAYER_CFG	0xF920_0010	R/W	Specifies the Video & Graphic Layer Priority and On/ Off	0x0000_0000
MIXER_VIDEO_CFG	0xF920_0014	R/W	Specifies the Video Layer Configuration	0x0000_0000
MIXER_VIDEO_LIMITER_PARA_CFG	0xF920_0018	R/W	Specifies the parameter of video layer limiter configuration	0xEB10_F010
Graphic0 Layer Configuration				
MIXER_GRAPHIC0_CFG	0xF920_0020	R/W	Specifies the Graphic Layer0 Configuration	0x0000_0000
MIXER_GRAPHIC0_BASE	0xF920_0024	R/W	Specifies the Base Address for Graphic Layer0	0x0000_0000
MIXER_GRAPHIC0_SPAN	0xF920_0028	R/W	Specifies the Span for Graphic Layer0	0x0000_0000
MIXER_GRAPHIC0_SXY	0xF920_002C	R/W	Specifies the Source X/Y Positions for Graphic Layer0	0x0000_0000
MIXER_GRAPHIC0_WH	0xF920_0030	R/W	Specifies the Width/ Height for Graphic Layer0	0x0000_0000
MIXER_GRAPHIC0_DXY	0xF920_0034	R/W	Specifies the Destination X/Y Positions for Graphic Layer0	0x0000_0000
MIXER_GRAPHIC0_BLANK	0xF920_0038	R/W	Specifies the Blank Pixel Value for Graphic Layer0	0x0000_0000
Graphic1 Layer Configuration				
MIXER_GRAPHIC1_CFG	0xF920_0040	R/W	Specifies the Graphic Layer1 Configuration	0x0000_0000
MIXER_GRAPHIC1_BASE	0xF920_0044	R/W	Specifies the Base Address for Graphic Layer1	0x0000_0000
MIXER_GRAPHIC1_SPAN	0xF920_0048	R/W	Specifies the Span for Graphic Layer1	0x0000_0000
MIXER_GRAPHIC1_SXY	0xF920_004C	R/W	Specifies the Source X/Y Positions for Graphic Layer1	0x0000_0000

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Register	Address	R/W	Description	Reset Value
MIXER_GRAPHIC1_WH	0xF920_0050	R/W	Specifies the Width/ Height for Graphic Layer1	0x0000_0000
MIXER_GRAPHIC1_DXY	0xF920_0054	R/W	Specifies the Destination X/Y Positions for Graphic Layer1	0x0000_0000
MIXER_GRAPHIC1_BLANK	0xF920_0058	R/W	Specifies the Blank Pixel Value for Graphic Layer1	0x0000_0000
Background Layer Configuration				
MIXER_BG_COLOR0	0xF920_0064	R/W	Specifies the Background Color of First Point	0x0000_0000
MIXER_BG_COLOR1	0xF920_0068	R/W	Specifies the Background Color of Second Point	0x0000_0000
MIXER_BG_COLOR2	0xF920_006C	R/W	Specifies the Background Color of Last Point	0x0000_0000
Color Space Conversion Coefficient				
MIXER_CM_COEFF_Y	0xF920_0080	R/W	Specifies the Scaled Color Space Conversion (RGB to Y) Coefficient for Graphic Layer	0x0844_0832
MIXER_CM_COEFF_CB	0xF920_0084	R/W	Specifies the Scaled Color Space Conversion (RGB to CB) Coefficient for Graphic Layer	0x3b5d_b0e1
MIXER_CM_COEFF_CR	0xF920_0088	R/W	Specifies the Scaled Color Space Conversion (RGB to Cr) Coefficient for Graphic Layer	0x0e1d_13dc
Mixer Global Setting Shadowing Register				
MIXER_STATUS_S	0xF920_2000	R	Specifies the Status of MIXER Operation (Shadow)	0x0000_0006
MIXER_CFG_S	0xF920_2004	R	Specifies the MIXER Mode Setting (Shadow)	0x0000_0000
Video & Blender Configuration Shadowing Register				
MIXER_LAYER_CFG_S	0xF920_2010	R	Specifies the Video & Graphic Layer Priority and On/ Off (Shadow)	0x0000_0000
MIXER_VIDEO_CFG_S	0xF920_2014	R	Specifies the Video Layer Configuration (Shadow)	0x0000_0000
MIXER_VIDEO_LIMITER_PARA_CFG_S	0xF920_2018	R	Specifies the The parameter of video layer limiter configuration	0xEB10_F010
Graphic0 Layer Configuration Shadowing Register				
MIXER_GRAPHIC0_CFG_S	0xF920_2020	R	Specifies the Graphic Layer0 Configuration (Shadow)	0x0000_0000
MIXER_GRAPHIC0_BASE_S	0xF920_2024	R	Specifies the Graphic0 Base Address (Shadow)	0x0000_0000
MIXER_GRAPHIC0_SPAN_S	0xF920_2028	R	Specifies the Graphic0 Span (Shadow)	0x0000_0000

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Register	Address	R/W	Description	Reset Value
MIXER_GRAPHIC0_SXY_S	0xF920_202C	R	Specifies the Graphic0 Source X/Y Coordinates (Shadow)	0x0000_0000
MIXER_GRAPHIC0_WH_S	0xF920_2030	R	Specifies the Graphic0 Width/ Height (Shadow)	0x0000_0000
MIXER_GRAPHIC0_DXY_S	0xF920_2034	R	Specifies the Graphic0 Destination X/Y Coordinates (Shadow)	0x0000_0000
MIXER_GRAPHIC0_BLANK_PIXEL_S	0xF920_2038	R	Specifies the Graphic0 Blank Pixel (Shadow)	0x0000_0000
Graphic1 Layer Configuration Shadowing Register				
MIXER_GRAPHIC1_CFG_S	0xF920_2040	R	Specifies the Graphic Layer1 Configuration (Shadow)	0x0000_0000
MIXER_GRAPHIC1_BASE_S	0xF920_2044	R	Specifies the Graphic1 Base Address (Shadow)	0x0000_0000
MIXER_GRAPHIC1_SPAN_S	0xF920_2048	R	Specifies the Graphic1 Span (Shadow)	0x0000_0000
MIXER_GRAPHIC1_SXY_S	0xF920_204C	R	Specifies the Graphic1 Source X/Y Coordinates (Shadow)	0x0000_0000
MIXER_GRAPHIC1_WH_S	0xF920_2050	R	Specifies the Graphic1 Width/ Height (Shadow)	0x0000_0000
MIXER_GRAPHIC1_DXY_S	0xF920_2054	R	Specifies the Graphic1 Destination X/Y Coordinates (Shadow)	0x0000_0000
MIXER_GRAPHIC1_BLANK_PIXEL_S	0xF920_2058	R	Specifies the Graphic1 Blank Pixel (Shadow)	0x0000_0000
Background Layer Configuration Shadowing Register				
MIXER_BG_COLOR0_S	0xF020_2064	R	Specifies the Background First Color (Shadow)	0x0000_0000
MIXER_BG_COLOR1_S	0xF920_2068	R	Specifies the Background Second Color (Shadow)	0x0000_0000
MIXER_BG_COLOR2_S	0xF920_206C	R	Specifies the Background Last Color (Shadow)	0x0000_0000
Version Register				
MIXER_VER	0xF920_0100	R	Specifies the Mixer Version	0x0000_0010

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9.2.2 SHADOW REGISTERS (READ ONLY)

If SYNC_ENABLE signal is set to 1, the written values to internal registers are not directly applied to the mixer operation. They are temporarily stored in the internal register and waits for next v_sync signal. After the v_sync signal occurs, the stored internal register values are updated to the shadow registers.

In interlaced display mode, the shadow registers are updated only at top-field. In progressive display mode, the shadow registers are updated at every v_sync.

9.2.2.1 Mixer_Status Register (MIXER_STATUS, R/W, Address = 0xF920_0000)

MIXER_STATUS	Bit	Description	Initial State
Reserved	[31:8]	Reserved, read as zero, do not modify	0
16_BURST_MODE	[7]	16 burst mode(64Bit Bus) enabled in DMA 1 = 16Beat Burst Mode 0 = 8Beat Burst Mode	0
Reserved	[6:4]	Reserved.	0
BIG_ENDIAN	[3]	0 = Little Endian Source Format 1 = Big Endian Source Format	0
SYNC_ENABLE	[2]	0 = Values set by user will not be applied to the mixer operation although v_sync is detected. 1 = Values set by user can be applied to the mixer operation after v_sync detected.	1
MIXER_OPERATION_STATUS	[1]	This bit is read-only. 0 = MIXER is operating. 1 = MIXER is idle mode. Note: If you want to stop operation, make REG_RUN "0" and check this bit whether it is "1"	1
REG_RUN	[0]	The mixer operation control. This register is also updated after V_SYNC. 0 = Mixer stops. 1 = Mixer starts processing. Note: The SFRs of Video Processor and Image Mixer is updated by Vertical Sync of TVENC's Timing Generator. Thus, SFRs are configured before this bit is enabled. The sequence to enable TVSS is as follows: "VP -> MIXER -> TVENC(HDMI)". Also, because SFRs are updated by Verical Sync, the disabling sequence is following as: "VP -> MIXER -> TVNEC(HDMI)".	0

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9.2.2.2 MIXER_CFG REGISTER (MIXER_CFG, R/W, Address = 0xF920_0004)

MIXER_CFG	Bit	Description	Initial State
Reserved	[31:11]	Reserved, read as zero, do not modify	0
REG_RGB_FORMAT	[10:9]	The RGB's range selection 0 = RGB601 , 0 ~ 255 1 = RGB601 , 16 ~ 235 2 = RGB709 , 0 ~ 255 3 = RGB709 , 16 ~ 235	0
REG_OUT_TYPE	[8]	The mixer's output type selection 0 = YCbCr444 1 = RGB888	0
REG_DST_SEL	[7]	The display IP selection 0 = TV Out 1 = HDMI Out	0
REG_HD_MODE	[6]	720p or 1080i selection 0 = 720p 1 = 1080i/1080p Note: 1080i = REG_SCAN_MODE is '0' 1080p = REG_SCAN_MODE is '1'	0
REG_GRAPHIC1_EN	[5]	Graphic1 layer display control bit. 0 = Disable 1 = Enable	0
REG_GRAPHIC0_EN	[4]	Graphic0 layer display control bit. 0 = Disable 1 = Enable	0
REG_VIDEO_EN	[3]	Video layer display control bit. 0 = Disable 1 = Enable	0
REG_SCAN_MODE	[2]	Display scanning mode of TV. 0 = Interlaced mode 1 = Progressive mode	0
REG_NTSC_PAL	[1]	Display standard of TV. If you set this bit '0' and set REG_SCAN_MODE '1', output has to be call 480p standard. This is only valid when REG_HD_SD is "0". 0 = NTSC (720x480) 1 = PAL (720x576)	0
REG_HD_SD	[0]	HD or SD selection 0 = SD 1 = HD If REG_HD_SD is 1, REG_HD_MODE = 0 for 720p REG_HD_MODE = 1 for 1080i.	0

NOTE: All changes to this register are valid on a vertical sync signal of next frame.

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	Wide	Narrow
CSCY2R (601)	R = Y + 1.371(Cr-128) G = Y – 0.698(Cr-128) – 0.336(Cb-128) B = Y + 1.732(Cb-128)	R = 1.164(Y-16) + 1.596(Cr-128) G = 1.164(Y-16) – 0.813(Cr-128) – 0.391(Cb-128) B = 1.164(Y-16) + 2.018(Cb-128)
CSCY2R (709)	R = Y + 1.540(Cr-128) G = Y – 0.459(Cr-128) – 0.183(Cb-128) B = Y + 1.816(Cb-128)	R = 1.164(Y-16) + 1.793(Cr-128) G = 1.164(Y-16) – 0.534(Cr-128) – 0.213(Cb-128) B = 1.164(Y-16) + 2.115(Cb-128)

NOTE: This table refers to Video Demystified(Keith Jack).

9.2.2.3 MIXER_INT_EN Register (MIXER_INT_EN, R/W, Address = 0xF920_0008)

MIXER_INTR	Bit	Description	Initial State
Reserved	[31:12]	Reserved, read as zero, do not modify	0
INT_EN_VSYNC	[11]	The vertical sync. interrupt enable. (Write only) 0 = Disable interrupt 1 = Enable interrupt	0
INT_EN_VP	[10]	The VP underflow interrupt enable. 0 = Disables interrupt 1 = Enables interrupt Setting this bit to '0' disables only the interrupt request to host controller. It does not mask the change of the MIXER_INT_STATUS[10] bit status	0
INT_EN_GRP1	[9]	The graphic layer1 line buffer underflow interrupt enable. 0 = Disables interrupt 1 = Enables interrupt Setting this bit to '0' disables only the interrupt request to host controller. It does not mask the change of the MIXER_INT_STATUS[9] bit status	0
INT_EN_GRP0	[8]	The graphic layer0 line buffer underflow interrupt enable. 0 = Disables interrupt 1 = Enables interrupt Setting this bit to '0' disables only the interrupt request to host controller. It does not mask the change of the MIXER_INT_STATUS[8] bit status	0
Reserved	[7:0]	Reserved.	0

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9.2.2.4 MIXER_INT_STATUS Register (MIXER_INT_STATUS, R/W, Address = 0xF920_000C)

MIXER_INTR	Bit	Description	Initial State
Reserved	[31:11]	Reserved, read as zero, do not modify	0
INT_CLEAR_VSYNC	[11]	The vertical sync. inerrupt clear bit. (Write only) 1 = Interrupt is cleared. Write '1' to this bit clears the interrupt. Also, Write '1' to this bit before you set INT_EN_VSYNC.	0
INT_STATUS_VP	[10]	The VP underflow interrupts status. 0 = Interrupt is not fired 1 = Interrupt is fired Writing ‘1’ to this bit clears the interrupt. This interrupt is automatically asserted by line buffer controller if underflow is generated in line buffer.	0
INT_STATUS_GRP1	[9]	The graphic layer1 line buffer underflow interrupt status. 0 = Interrupt is not fired 1 = Interrupt is fired Writing ‘1’ to this bit clears the interrupt. This interrupt is automatically asserted by line buffer controller if underflow is generated in line buffer.	0
INT_STATUS_GRP0	[8]	The graphic layer0 line buffer underflow interrupt status. 0 = Interrupt is not fired 1 = Interrupt is fired Writing ‘1’ to this bit clears the interrupt. This interrupt is automatically asserted by line buffer controller if underflow is generated in line buffer.	0
Reserved	[7:1]	Reserved, read as zero, do not modify	0
INT_STATUS_VSYNC	[0]	The vertical sync. status. (Read only) 0 = Interrupt is not fired. 1 = Interrupt is fired. Note : If INT_STATUS_VSYNC & !INT_STATUS_VP & !INT_STATUS_GRP1 & !INT_STATUS_GRP0 is high, The vertical sync. is fired.	

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9.2.2.5 MIXER_LAYER_CFG Register (MIXER_LAYER_CFG, R/W, Address = 0xF920_0010)

The priority value for video and each graphic layer can be set. The priority field is used to determine the priority of a graphic layer. The graphic layer of higher value has the higher priority. This field is also used as on/off switch. If one field is set to zero, the corresponding graphic layer is not displayed. If some layers have the same value, the priority is like this: graphic layer 1 > graphic layer 0 > video. The priority is only determined by difference of priority's value. For example, case1 and case 2 have the same effect.

- Case1: GRP1 priority is 2 , GRP0 priority 3 , Video Priority 1
- Case2: GRP1 priority is 14 , GRP0 priority 15 , Video Priority 13

MIXER_LAYER_CFG	Bit	Description	Initial State
Reserved	[31:12]	Reserved, read as zero, do not modify	0
Graphic layer 1 priority	[11:8]	15 ~ 1 = the priority value 0 = Hides the graphic layer 1	0
Graphic layer 0 priority	[7:4]	15 ~ 1 = the priority value 0 = Hides the graphic layer 0	0
Video layer priority	[3:0]	15 ~ 1 = the priority value 0 = Hides the video layer 0	0

NOTE: All the changes of this register are valid on a vertical sync signal of next frame when SYNC_ENABLE flag is set to one. The "Hide" means that layer data is ready but is not displayed.

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9.2.2.6 MIXER_VIDEO_CFG Register (MIXER_VIDEO_CFG, R/W, Address = 0xF920_0014)

MIXER_VIDEO_CFG	Bit	Description	Initial State
Reserved	[31:18]	Reserved, read as zero, do not modify	0
REG_LIMITER_EN	[17]	YUV limiter for xvYcc 0 = Disables 1 = Enables	0
REG_BLEND_EN	[16]	If set to 1, it enables the blending of the entire video layer onto the lower layer using the blending factor, REG_ALPHA_VID.	0
Reserved	[15:8]	Reserved, read as zero, do not modify	0
REG_ALPHA_VID	[7:0]	Video layer blending factor. This factor is used over all the pixels in the video layer to blend with lower layer. α * video_layer_pixel_value + (1 – α) * lower_layer_pixel_value If REG_ALPHA_VID is 0, α is 0. If REG_ALPHA_VID is not 0, α = (REG_ALPHA_VID + 1)/256.	0

NOTE: All changes to this register are valid on a vertical sync signal of next frame.

9.2.2.7 MIXER_VIDEO_LIMITER_PARA_CFG Register (MIXER_VIDEO_LIMITER_PARA_CFG, R/W, Address = 0xF920_0018)

MIXER_VIDEO_LIMITER_PARA_CFG	Bit	Description	Initial State
REG_PARA_Y_UPPER	[31:24]	Upper bound for Y parameter of the limiter	0xEB
REG_PARA_Y_LOWER	[23:16]	Lower bound for Y parameter of the limiter	0x10
REG_PARA_C_UPPER	[15:8]	Upper bound for C parameter of the limiter	0xF0
REG_PARA_C_LOWER	[7:0]	Lower bound for C parameter of the limiter	0x10

NOTE: All changes to this register are valid on a vertical sync signal of next frame.

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9.2.2.8 MIXER_GRAPHIC0_CFG Register (MIXER_GRAPHIC0_CFG, R/W, Address = 0xF920_0020)

MIXER_GRAPHIC0_CFG	Bit	Description	Initial State
RTQoS_GRP0	[31:23]	Real time QoS configuration. The size of graphic layer0 FIFO is 480depth(The each of level is 128bit) 0 = RTQoS Disable 1 ~ 480 = QoS threshold level 481 ~ = Reserved	0
Reserved	[22]	Reserved	0
BLANK_CHANGE0	[21]	0 = Blank key (color key) is enable. 1 = Blank key (color key) is disable.	0
PRE_MUL_MODE0	[20]	Pre Multiplied_blending mode in graphic layer0. 1 = Pre-Multiplied mode 0 = Normal mode In this mode, graphic pixel data must be pre-multiplied with graphic pixel alpha. In pre-multiplied mode, REG_PIXEL0_BLEND_EN must be enabled. Graphic and lower layer blending factor. This factor is used all over the pixels in the graphic and lower layer to blend with. A blending factor(α) is as follows depending on the a layer blending factor and a pixel blending factor values: See *Table 9-1.*	0
Reserved	[19:18]	Reserved, read as zero	
REG_WIN0_BLEND_EN	[17]	Blending by a blending factor set by REG_ALPHA_WIN0 register on all over the graphic layer0.	0
REG_PIXEL0_BLEND_EN	[16]	Blending by a blending factor of each pixel is enabled in graphic layer0.	0
Reserved	[15:12]	Reserved, read as zero	0

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MIXER_GRAPHIC0_CFG	Bit	Description	Initial State
EG_COLOR_FORMAT0	[11:8]	Graphic layer0 color format. 0 = Reserved 1 = Reserved 2 = Reserved 3 = Reserved 4 = RGB 565 5 = ARGB 1555 6 = ARGB 4444 7 = ARGB 8888 8 = Reserved 9 = Reserved A = Reserved B = Reserved C = Reserved D = Reserved E = Reserved F = Reserved	0
REG_ALPHA_WIN0	[7:0]	Graphic layer0 and lower layer blending factor. This factor is used all over the pixels in the graphic and lower layer to blend with. A blending factor(α) is as follows depending on the a layer blending factor and a pixel blending factor values: α * graphic_layer_pixel_value + (1 – α) * lower_layer_pixel_value See *Table 9-1*. If REG_ALPHA_WIN0 is 0, blending_factor_layer is 0. If REG_ALPHA_WIN0 is not 0, blending_factor_layer = (REG_ALPHA_WIN + 1) / 256. If A(blending factor of each pixel) is 0, blending_factor_each_pixel is 0 If A(blending factor of each pixel) is not 0, blending_factor_each_pixel = (A + 1) / 256. The pixel blending factors comes from the pixel in direct modes except the direct 16bpp 565 format.	0

NOTE: All the changes of this register are valid on a vertical sync signal of next frame.

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9.2.2.9 MIXER_GRAPHIC1_CFG Register (MIXER_GRAPHIC1_CFG, R/W, Address = 0xF920_0040)

MIXER_GRAPHIC1_CFG	Bit	Description	Initial State
RTQoS_GRP1	[31:23]	Real time QoS configuration. The size of graphic layer0 FIFO is 480depth(The each of level is 128bit) 0 = RTQoS Disable 1 ~ 480 = QoS threshold level 481 ~ = Reserved	0
Reserved	[22]	Reserved	0
BLANK_CHANGE1	[21]	0 = Blank key (color key) is enable. 1 = Blank key (color key) is disable.	0
PRE_MUL_MODE1	[20]	Pre Multiplied_blending mode in graphic layer1. 1 = Pre-Multiplied mode 0 = Normal mode In this mode, graphic pixel data must be pre-multiplied with graphic pixel alpha. In pre-multiplied mode, REG_PIXEL1_BLEND_EN must be enabled. Graphic and lower layer blending factor. This factor is used all over the pixels in the graphic and lower layer to blend with. A blending factor(α) is as follows depending on the a layer blending factor and a pixel blending factor values: See *Table 9-1* .	0
Reserved	[19:18]	Reserved, read as zero	0
REG_WIN1_BLEND_EN	[17]	Blending by a blending factor set by REG_ALPHA_WIN1 register on all over the graphic layer1.	0
REG_PIXEL1_BLEND_EN	[16]	Blending by a blending factor of each pixel is enabled in graphic layer1.	0
Reserved	[15:12]	Reserved, read as zero	0

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MIXER_GRAPHIC1_CFG	Bit	Description	Initial State
REG_COLOR_FORMAT1	[11:8]	Graphic layer1 color format. 0 = Reserved 1 = Reserved 2 = Reserved 3 = Reserved 4 = RGB 565 5 = ARGB 1555 6 = ARGB 4444 7 = ARGB 8888 8 = Reserved 9 = Reserved A = Reserved B = Reserved C = Reserved D = Reserved E = Reserved F = Reserved	0
REG_ALPHA_WIN1	[7:0]	Graphic layer1 and lower layer blending factor. This factor is used all over the pixels in the graphic and lower layer to blend with. A blending factor(α) is as follows depending on the a layer blending factor and a pixel blending factor values: α * graphic_layer_pixel_value + (1 – α) * lower_layer_pixel_value See *Table 9-1*. If REG_ALPHA_WIN1 is 0, blending_factor_layer is 0. If REG_ALPHA_WIN1 is not 0, blending_factor_layer = (REG_ALPHA_WIN + 1) / 256. If A(blending factor of each pixel) is 0, blending_factor_each_pixel is 0 If A(blending factor of each pixel) is not 0, blending_factor_each_pixel = (A + 1) / 256. The pixel blending factors comes from the pixel in direct modes except the direct 16bpp 565 format.	0

NOTE: All the changes of this register are valid on a vertical sync signal of next frame.

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Table 9-1 Graphic Blending-factor Alpha in Case of Normal Mode

MIXER_GRAPHICx_CFG. REG_WINx_BLEND_EN	MIXER_GRAPHICx_CFGx. REG_PIXELx_BLEND_EN	Alpha Value (Blending factor of each pixel)
0	0	1
0	1	blending_factor_each_pixel(A)
1	0	blending_factor_layer (MIXER_GRAPHICn_CFG[7:0])
1	1	blending_factor_layer * blending_factor_each_pixel

Table 9-2 Graphic Blending Method

Pixel Blend	Window Blend	Normal Mode	Pre Multiplied Mode
0	0	-	-
0	1	Alpha_gw * graphic_pixel + (1 - alpha_gw) * lower layer	Alpha_gw * graphic_pixel + (1 - alpha_gw) * lower layer
1	0	Alpha_gp * graphic_pixel + (1 - alpha_gp) * lower layer	graphic_pixel + (1 - alpha_gp) * lower layer
1	1	(Alpha_gp * alpha_gw) * graphic_pixel + (1 - alpha_gp * alpha_gw) * lower layer	alpha_gw * graphic_pixel + (1 - alpha_gp * alpha_gw) * lower layer

In pre-multiplied mode, the input graphic data is multiplied by the pixel blending factor (alpha_gp) and truncated to the size of source format bits. For example, although the result of the multiplication of 8-bit data by 8-bit pixel blending factor is 16 bits which is the first term of the blending equation in the *Table 9-2. N*ormal mode, the supplied data is truncated to 8 bits that results the loss of the lower significant 8bits during calculation. In direct 32bpp modes, this loss data cannot be distinguished visually (+/- 1difference). But in direct 16bpp modes, the loss data can make visually different result from the original. For example, in 4633 direct mode, the pre-multiplied Cb data is truncated to 3 bits that result in the difference value from +15 to -15. This difference range can result to visual difference. You cannot reduce the error that is resulted from the 3 bits input source. Thus, it is recommended to use the 32bpp mode to use the pre-multiplied mode.

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9.2.2.10 MIXER_GRAPHIC0_BASE, R/W, Address = 0xF920_0024, MIXER_GRAPHIC1_BASE, R/W, Address = 0xF920_0044

MIXER_GRAPHICn_BASE	Bit	Description	Initial State
REG_GRAPHICn_BASE	[31:0]	Base address of frame buffer for graphic layer. This address should be word aligned, so least 2 significant bits [1:0] will be set 2'b00 automatically	0

9.2.2.11 MIXER_GRAPHIC0_SPAN, R/W, Address = 0xF920_0028, MIXER_GRAPHIC1_SPAN, R/W, Address = 0xF920_0048

MIXER_GRAPHICn_SPAN	Bit	Description	Initial State
Reserved	[31:15]	Reserved, read as zero, do not modify	0
REG_GRAPHICn_SPAN	[14:0]	Horizontal pixel interval between line and line in graphic layer's source image Note: SPAN is the number of the original image's horizontal pixel count. For example, 640x480's span is '640'. It is not related to BPP(bit per pixel).	0

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9.2.2.12 MIXER_GRAPHIC0_WH, R/W, Address = 0xF920_0030, MIXER_GRAPHIC1_WH, R/W, Address = 0xF920_0050

MIXER_GRAPHICn_ WH	Bit	Description	Initial State
Reserved	[31:29]	Reserved, read as zero, do not modify	0
REG_H_SCALEn	[28]	Horizontal scaling Configuration 0 = Not Available 1 = X2 Scaling-Up	0
Reserved	[27]	Reserved, read as zero, do not modify	0
REG_GRAPHICn_W	[26:16]	Width of graphic layer (pixel unit)	0
Reserved	[15:13]	Reserved, read as zero, do not modify	0
REG_V_SCALEn	[12]	Vertical Duplication Configuration 0 = Not Available 1 = X2 Duplication	0
Reserved	[11]	Reserved, read as zero, do not modify	0
REG_GRAPHICn_H	[10:0]	Height of graphic layer (pixel unit).	0

NOTE: All the changes of this register are valid on a vertical sync signal of next frame.
When specifying the X coordinates and the width of a graphic layer, it should be located inside the display region, for example, 720x480 region in NTSC display mode and 720x576 region in PAL display. The coordinates (x, y) and the size (width, height) should be based on the progressive mode although it is interlaced display mode.
Graphic width and height should be larger than 0 if the corresponding REG_GRAPHICx_EN field(MIXER_CFG[5], MIXER_CFG[4]) is set to 1.

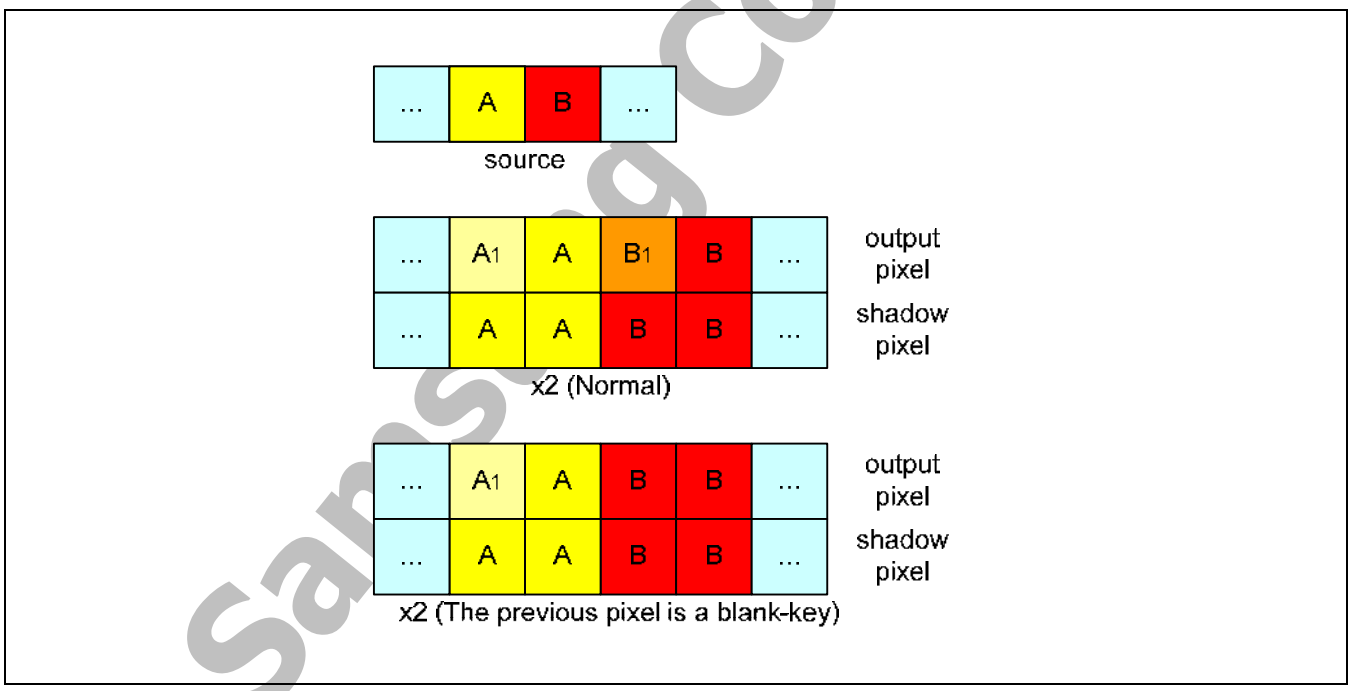

Figure 9-3 Mixer Horizontal Scale and Blank-key

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9.2.2.13 MIXER_GRAPHIC0_XY, R/W, Address = 0xF920_002C, MIXER_GRAPHIC1_SXY, R/W, Address = 0xF920_004C

MIXER_GRAPHICn_XY	Bit	Description	Initial State
Reserved	[31:27]	Reserved, read as zero, do not modify	0
REG_GRAPHICn_SX	[26:16]	X coordinate of upper left corner of graphic layer in source frame (pixel unit). Allowed range = 0 ~ 719 at SD mode = 0 ~ 1279 at HD mode(720p) = 0 ~ 1919 at HD mode(1080i/p)	0
Reserved	[15:11]	Reserved, read as zero, do not modify	0
REG_GRAPHICn_SY	[10:0]	Y coordinate of upper left corner of graphic layer in source frame (pixel unit). Allowed range = 0 ~ 479 at NTSC mode = 0 ~ 575 at PAL mode = 0 ~ 719 at HD mode(720p) = 0 ~ 1079 at HD mode(1080i/p)	0

9.2.2.14 MIXER_GRAPHIC0_DXY, R/W, Address = 0xF920_0034, MIXER_GRAPHIC1_DXY, R/W, Address = 0xF920_0054

MIXER_GRAPHICn_DXY	Bit	Description	Initial State
Reserved	[31:27]	Reserved, read as zero, do not modify	0
REG_GRAPHICn_DX	[26:16]	X coordinate of upper left corner of graphic layer in destination frame (pixel unit). Allowed range = 0 ~ 719 at SD mode = 0 ~ 1279 at HD mode(720p) = 0 ~ 1919 at HD mode(1080i/p)	0
Reserved	[15:11]	Reserved, read as zero, do not modify	0
REG_GRAPHICn_DY	[10:0]	Y coordinate of upper left corner of graphic layer in destination frame (pixel unit). Allowed range = 0 ~ 479 at NTSC mode = 0 ~ 575 at PAL mode = 0 ~ 719 at HD mode(720p) = 0 ~ 1079 at HD mode(1080i/p)	0

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9.2.2.15 MIXER_GRAPHIC0_BLANK, R/W, Address = 0xF920_0038, MIXER_GRAPHIC1_BLANK, R/W, Address = 0xF920_0058

MIXER_GRAPHICn_BLANK	Bit	Description	Initial State
REG_GRAPHICn_BLANK	[31:0]	Blank pixel value for graphic layerN Note: When blanked pixel is ARGB, entire register value must be same with pixel value including alpha value.	0

9.2.2.16 MIXER_BG_COLOR0, R/W, Address = 0xF920_0064, MIXER_BG_COLOR1, R/W, Address = 0xF920_0068, MIXER_BG_COLOR2, R/W, Address = 0xF920_006C

MIXER_BG_COLOR0/1/2	Bit	Description	Initial State
-	[31:24]	Reserved, read as zero, do not modify	0
Y	[23:16]	Y component of background color	0
Cb	[15:8]	Cb component of background color	0
Cr	[7:0]	Cr component of background color	0

NOTE: You can choose proper YCbCr value for BT.601 or BT.709.

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9.2.2.17 MIXER_COLOR_SPACE_CONVERSION_COEF_Y Register (MIXER_CM_COEFF_Y, R/W, Address = 0xF920 0080)

MIXER_CM_COEFF_Y	Bit	Description	Initial State
Reserved	[31]	Reserved, read as zero, do not modify	
WIDE_SEL	[30]	0 = Narrow 1 = Wide	0
REG_COEFF_00	[29:20]	Scaled color space conversion coefficient (C_{00}). [29]: Sign-bit [28:20]: Fractional bit (Default and Recommended value : 0.257 in decimal)	0x84
REG_COEFF_10	[19:10]	Scaled color space conversion coefficient (C_{10}). [19]: Sign-bit [18:10]: Fractional bit (Default and Recommended value : 0.504 in decimal)	0x102
REG_COEFF_20	[9:0]	Scaled color space conversion coefficient (C_{20}). [9]: Sign-bit [8:0]: Fractional bit (Default and Recommended value : 0.098 in decimal)	0x32

NOTE: RGB to YCbCr Conversion Equations

RGB data with 16-235 range

Y601 = 0.299R + 0.587G + 0.114B
Cb = -0.172R – 0.339G + 0.511B + 128
Cr = 0.511R – 0.428G – 0.083B + 128

Y709 = 0.213R + 0.715G + 0.072B
Cb = -0.117R – 0.394G + 0.511B + 128
Cr = 0.511R – 0.464G – 0.047B + 128

RGB data with 0-255 range

Y601 = 0.257R + 0.504G + 0.098B + 16
Cb = -0.148R – 0.291G + 0.439B + 128
Cr = 0.439R – 0.368G – 0.071B + 128

Y709 = 0.183R + 0.614G + 0.062B + 16
Cb = -0.101R - 0.338G + 0.439B + 128
Cr = 0.439 – 0.399G – 0.040B + 128

Fraction Number (Example, 1bit is Signed bit and 9bits are Fraction Bit)

0.098 = 0.5* ’0’ + 0.25* ’0’ + 0.125* ‘0’ + 0.0625* ‘1’ + 0.03125* ‘1’ + 0.015625* ‘0’ + 0.0078125* ‘0’ + 0.00390625* ‘1’ + 0.001953125* ‘0’ = 0(signed bit) 0 0 0 1 1 0 0 1 0 = 0x032

-0.148 -> First of all, let’s think about 0.148
0. 148 = 0.5* ’0’ + 0.25* ’0’ + 0.125* ‘1’ + 0.0625* ‘0’ + 0.03125* ‘0’ + 0.015625* ‘1’ + 0.0078125* ‘0’ + 0.00390625* ‘1’ + 0.001953125* ‘1’ = 0(signed bit) 0 0 1 0 0 1 0 1 1 = 10’b0001001011

Now, to change the number from 0.148 to -0.148, we have to derive 2’s compliment of 0.148

10’b 0 0 0 1 0 0 1 0 1 1 -> 10’b 1 1 1 0 1 1 0 1 0 0 (bitwise invert) + 1 = 10’b 1 1 1 0 1 1 0 1 0 1 = 0x3B5

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9.2.2.18 MIXER_COLOR_SPACE_CONVERSION_COEF_CB Register (MIXER_CM_COEFF_CB, R/W, Address = 0xF920_0084)

MIXER_CM_COEFF_CB	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
REG_COEFF_01	[29:20]	Scaled color space conversion coefficient (C_{01}). [29]: Sign-bit [28:20]: Fractional bit (Default value: -0.0742785 in decimal) (Recommended value: -0.148 in decimal, 0x3b5 in hexa-decimal)	0x3b4
REG_COEFF_11	[19:10]	Scaled color space conversion coefficient (C_{11}). [19]: Sign-bit [18:10]: Fractional bit (Default value: -0.1455078125 in decimal) (Recommended value: -0.291 in decimal, 0x36c in hexa-decimal)	0x36b
REG_COEFF_21	[9:0]	Scaled color space conversion coefficient (C_{21}). [9]: Sign-bit [8:0]: Fractional bit (Default and Recommended value: 0.439 in decimal)	0xe1

9.2.2.19 MIXER_COLOR_SPACE_CONVERSION_COEF_CR Register (MIXER_CM_COEFF_Cr, R/W, Address = 0xF920_0088)

MIXER_CM_COEFF_CR	Bit	Description	Initial State
Reserved	[31:30]	Reserved, read as zero, do not modify	0
REG_COEFF_02	[29:20]	Scaled color space conversion coefficient (C_{02}). [29]: Sign-bit [28:20]: Fractional bit (Default and Recommended value: 0.439 in decimal)	0xe1
REG_COEFF_12	[19:10]	Scaled color space conversion coefficient (C_{12}). [19]: Sign-bit [18:10]: Fractional bit (Default and Recommended value: -0.368 in decimal)	0x344
REG_COEFF_22	[9:0]	Scaled color space conversion coefficient (C_{22}). [9]: Sign-bit [8:0]: Fractional bits (Default and Recommended value: -0.071 in decimal)	0x3dc

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9.3 LAYERS

Mixer blends all the image sources such as video layer, graphic layer, and background layer and transfers the blended pixel data to TVNEC/HDMI. Set layer's priority value to select the order of the blending operation. Video and 2 graphic layers can be fully ordered and blended. The background layer is always the lowest layer.

- Background → (Video ↔ Graphic0 ↔ Graphic1)

Video layer and graphic layer are enabled or disabled by the register setting. The blending factor differs layer by layer like following:

- Background layer: No blending factor, as it is the lowest layer.
- Video layer: Video layer has one blending factor that is applied to all the pixels in the video layer. MIXER_VIDEO_CFG [7:0](REG_ALPHA_VID) is the blending factor. The video blending is enabled or disabled.
- Graphic0 layer: Graphic0 layer supports pixel blending and window blending. Pixel blending factors are applied
  pixel-by-pixel although window blending factor is applied all the pixels in the graphic layer. These two blending factors are applied simultaneously to a pixel.
- Graphic1 layer: Graphic1 layer supports pixel blending and window blending. Pixel blending factors are applied pixel-by-pixel although window blending factor is applied on all the pixels in the graphic layer. These two blending factors are applied simultaneously to a pixel.

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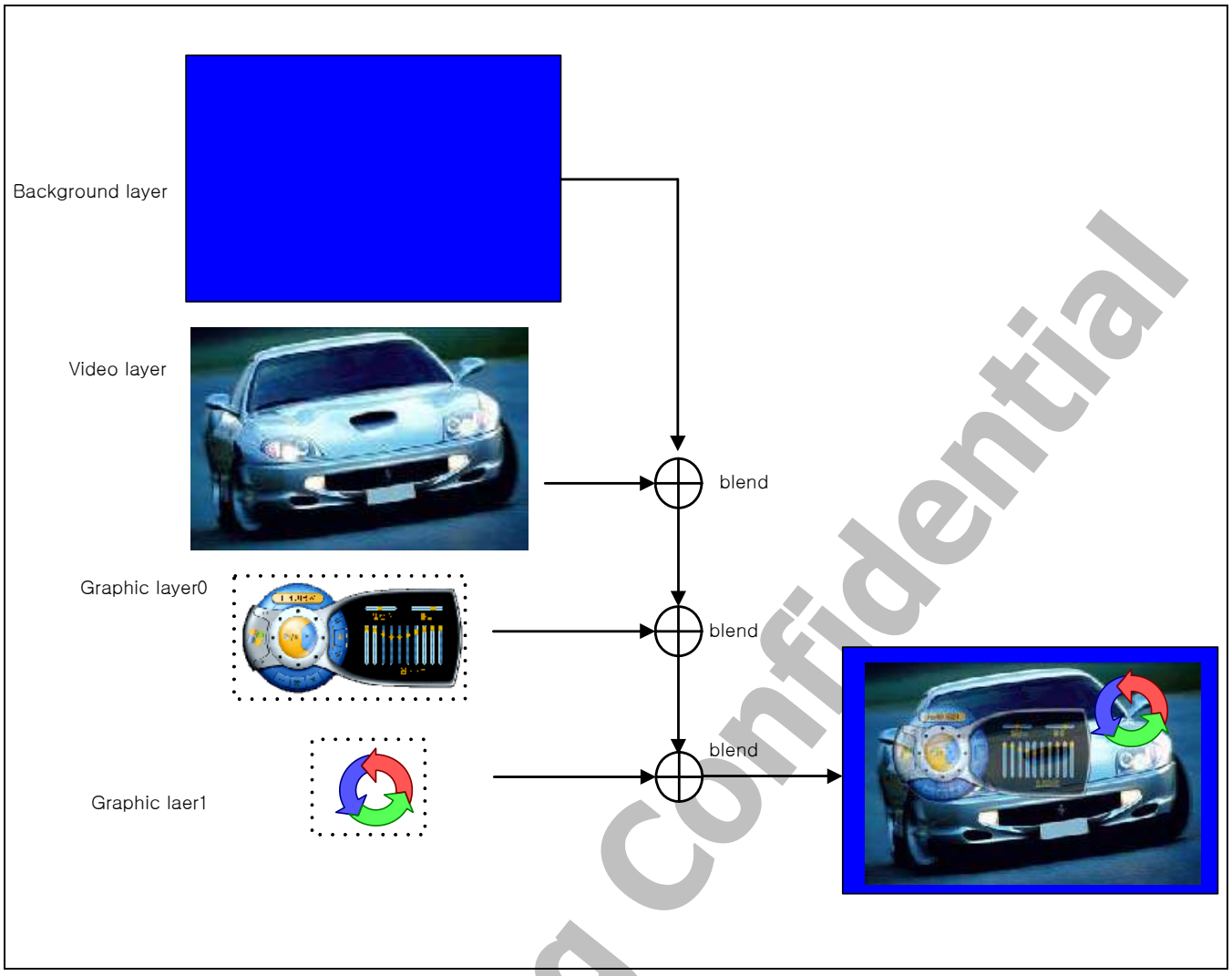

Figure 9-4 Mixer Blending

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9.3.1 VIDEO LAYER

Video data is directly transferred from Video Processor to Mixer in YCbCr [888] 4:4:4 formats. As the Video Processor scales the source image in letterbox mode, the display region of the video data is smaller than the screen size. In this case, background layer is seen in the blank region.

9.3.2 GRAPHIC LAYER

ARM or Graphic Accelerator generates the graphic source data in the external memory and they are transferred to Mixer by AXI access. Mixer supports the following graphic formats.

- 16bpp RGB [565]
- 16bpp ARGB [1555]
- 16bpp ARGB [4444]
- 32bpp ARGB [8888]

In 16/32-bpp direct modes, the value of a pixel data directly indicates the RGB but the bit width for R, G, and B are different for each mode. For 16bpp direct ARGB [4444] mode, the RGB component is assigned to 16 bit length like the following.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
alpha factor				R				G				B			

Figure 9-5 16bpp ARGB Example

The internal data path is processed with YCbCr[888] format, therefore RGB format is converted to YCbCr by color matrix conversion.

If the bit-per-pixel (BPP) of color format is smaller than 8 bits, that value is used after expanding (Refer *Figure 9-6* example (ARGB [1555])).

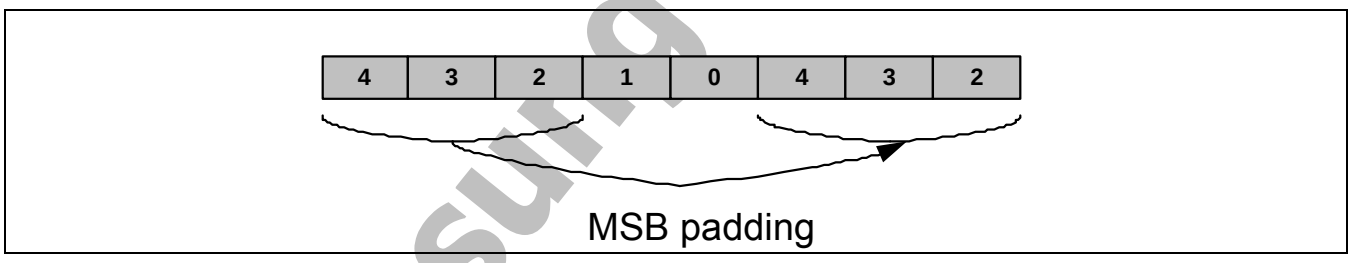

Figure 9-6 Example of Expanding

Mixer supports up to two graphic layers and one video layer. Each layer is enabled or disabled and user can configure the priority between layers. There is each blending factor between layers. The graphic layers has different color format.

When specifying the X/Y coordinates and the width/height of a graphic layer, the graphic layers should be located in the display region (720x480 in NTSC display mode, 720x576 in PAL display mode, 1280x720p/1920x1080i&p in HD display mode). The Mixer does not support the clipping operation for the pixels that are displayed out of screen.

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9.3.3 BLANK PIXEL

Blank pixel data in graphic layer is a pixel data that is transparent to the lower layer. You can define a blank pixel data in the register (MIXER_GRAPHICn_BLANK) and if the graphic data is same as the blank pixel value, a lower image is seen instead of the blank pixel.

9.3.4 SOURCE DATA IN MEMORY

As the graphic data comes from the external memory through the bus, the memory format for the source data is dependent on the bus system endian. In little endian system, the lower 8 bits are stored in the lower address.

The source data format in the Mixer is aligned in little endian or big endian format. This different endian format is applicable to the graphic data.

Mixer supports many graphic formats. The register format of the supported source formats is shown in *Figure 9-7*. The following picture shows the pixels in a display that is seen through human eyes.

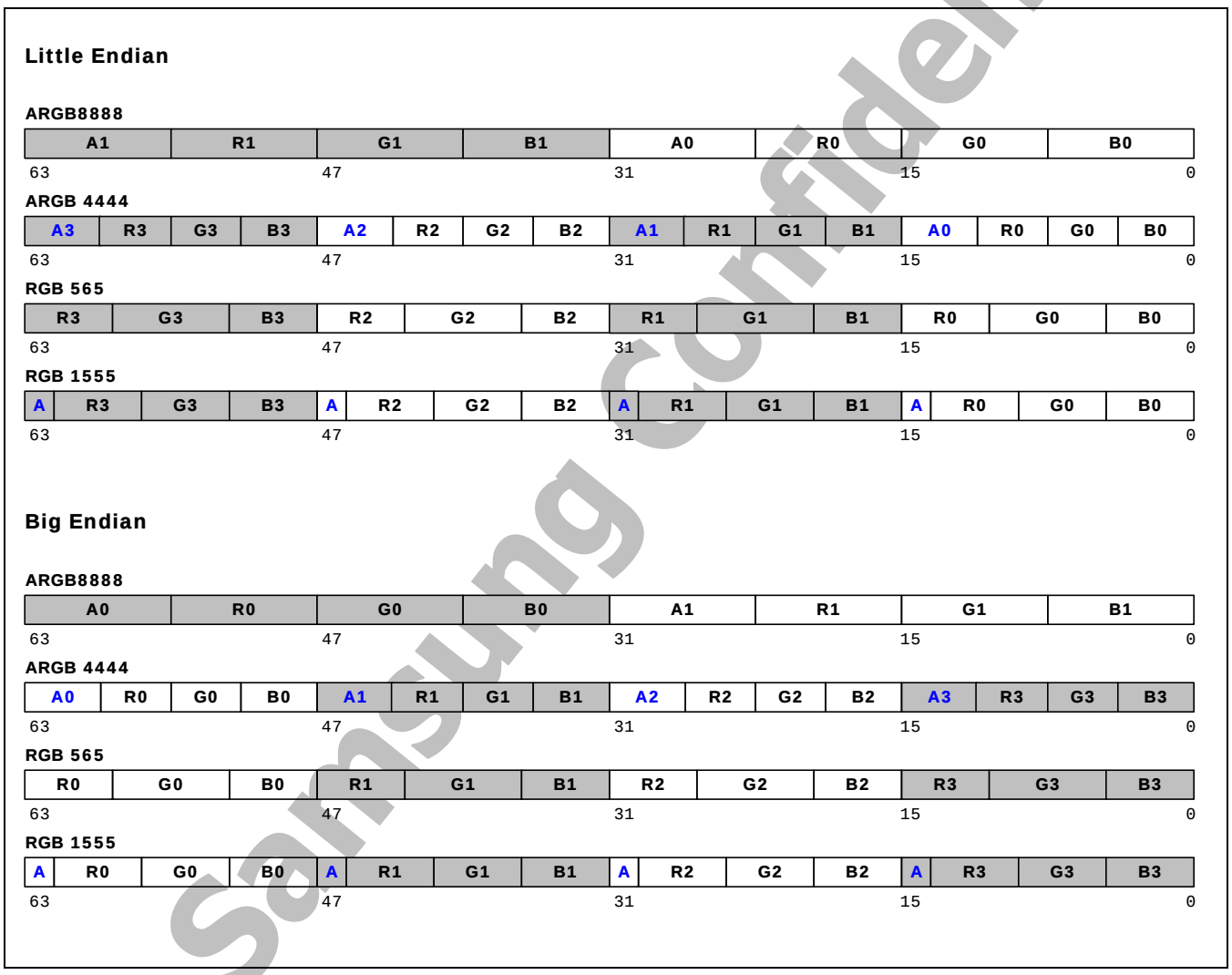

Figure 9-7 Graphic Data Format in Memory

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Pixels with lower X coordinates are located from the left. These pixel data are represented by different digital data depending on the graphic format setting. For example, one graphic pixel is represented by 16-bit digital data in 16 BPP mode. If these pixels are processed in the Mixer, the word format to represent these pixels is different depending on the endian format.

In the big endian mode, the pixel with lower X coordinate is positioned to the MSB parts in the 64-bit register of Mixer. However, in the little endian mode, the pixel with lower X coordinate is positioned to the LSB parts in the 64-bit register.

9.3.5 BACKGROUND LAYER

If there is no video or graphic, background color is seen in the display region. Use YCbCr[888] format to set the background color in the register.

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10 HIGH-DEFINITION MULTIMEDIA INTERFACE

10.1 OVERVIEW OF HIGH-DEFINITION MULTIMEDIA INTERFACE

The High-Definition Multimedia Interface (HDMI) 1.3 Tx Subsystem V1.0 comprises an HDMI Tx Core with I2S/ SPDIF input interface, CEC block, and HDCP Key Block.

10.1.1 KEY FEATURES OF HDMI

The key features of HDMI include:

- Complies with HDMI 1.3, HDCP 1.1, and DVI 1.0

Supports the following video formats:

- 480p @59.94Hz/ 60Hz, 576p @50Hz
- 720p @50Hz/ 59.94Hz/ 60Hz
- 1080i @50Hz/ 59.94Hz/ 60Hz
- 1080p @25Hz/ 29.97Hz/ 30Hz
- Other various formats up to 74.25 MHz Pixel Clock

Supports Color Format: 4:4:4 RGB/ YCbCr

Supports Bit Per Color: 8-bit

Supports CEC function

Contains an Integrated HDCP Encryption Engine for Video/ Audio content protection

Does not include DDC

- There is a dedicated I2C for DDC in S5PV210 peripheral Bus

Supports audio RX transmission when I2S in audio sub-system is either master or slave mode.

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10.1.2 BLOCK DIAGRAM OF HDMI

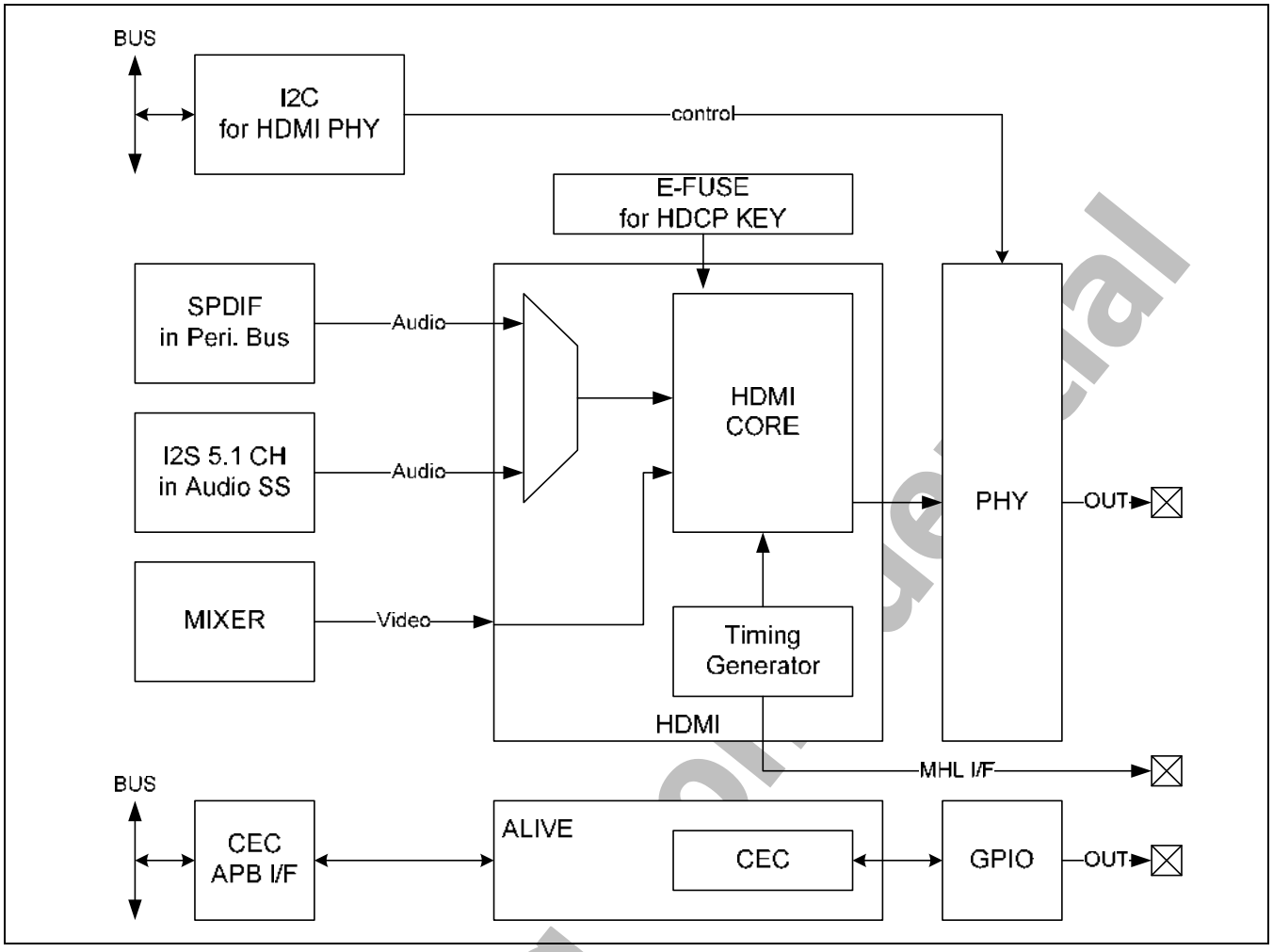

Figure 10-1 Block Diagram of HDMI

HDMI TX V1.3 consists of several blocks, each with a unique function. For instance, the Mixer specifies the source image of HDMI. It transmits image data, which can be either RGB888 or YUV444. Before it works, you must set the pixel clock properly. The ratio of pixel clock depends on the output resolution. You can configure both CMU and HDMI_PHY.

SPDIF in peripheral bus and I2S 5.1 channel in Audio sub-system feed audio data in HDMI TX V1.3. For more information, refer to SPDIF and I2S datasheets.

HDMI TX V1.3 in S5PV210 supports embedded HDCP key system. S5PV210 does not allow access to HDCP key.

A dedicated I2C is used to configure HDMI PHY. In addition, the HDMI PHY generates pixel and TMDS clock through I2C.

The CEC block is separate from HDMI TX, and is used by wake-up source in S5PV210. It belongs to the ALIVE block and communicates with external CEC through bi-directional GPIO.

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10.1.3 BLOCK DIAGRAM OF HDMI SUB-SYSTEM IN S5PV210

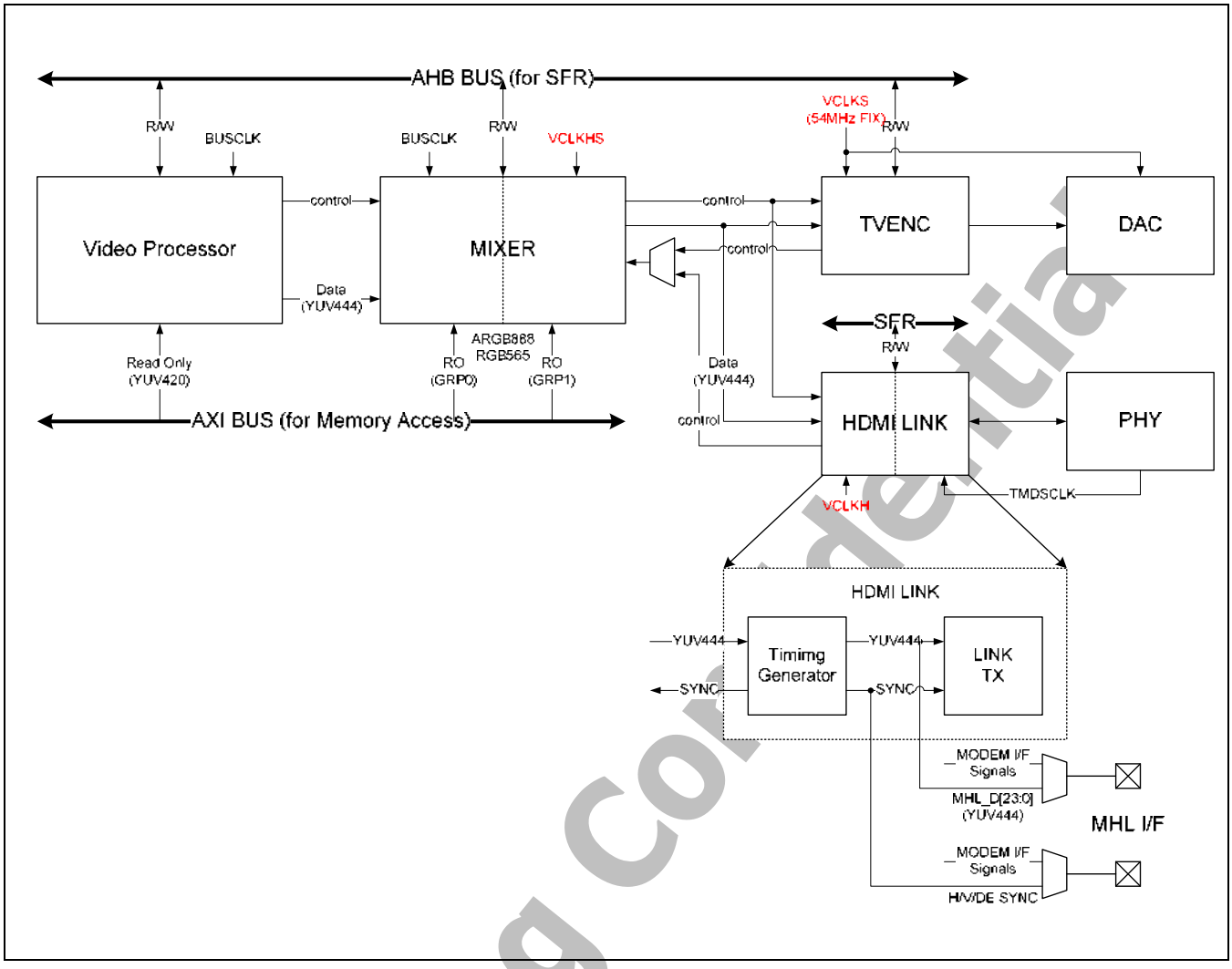

Figure 10-2 Block Diagram of HDMI SUB-System in S5PV210

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10.1.4 BLOCK DIAGRAM OF HDCP KEY MANAGEMENT

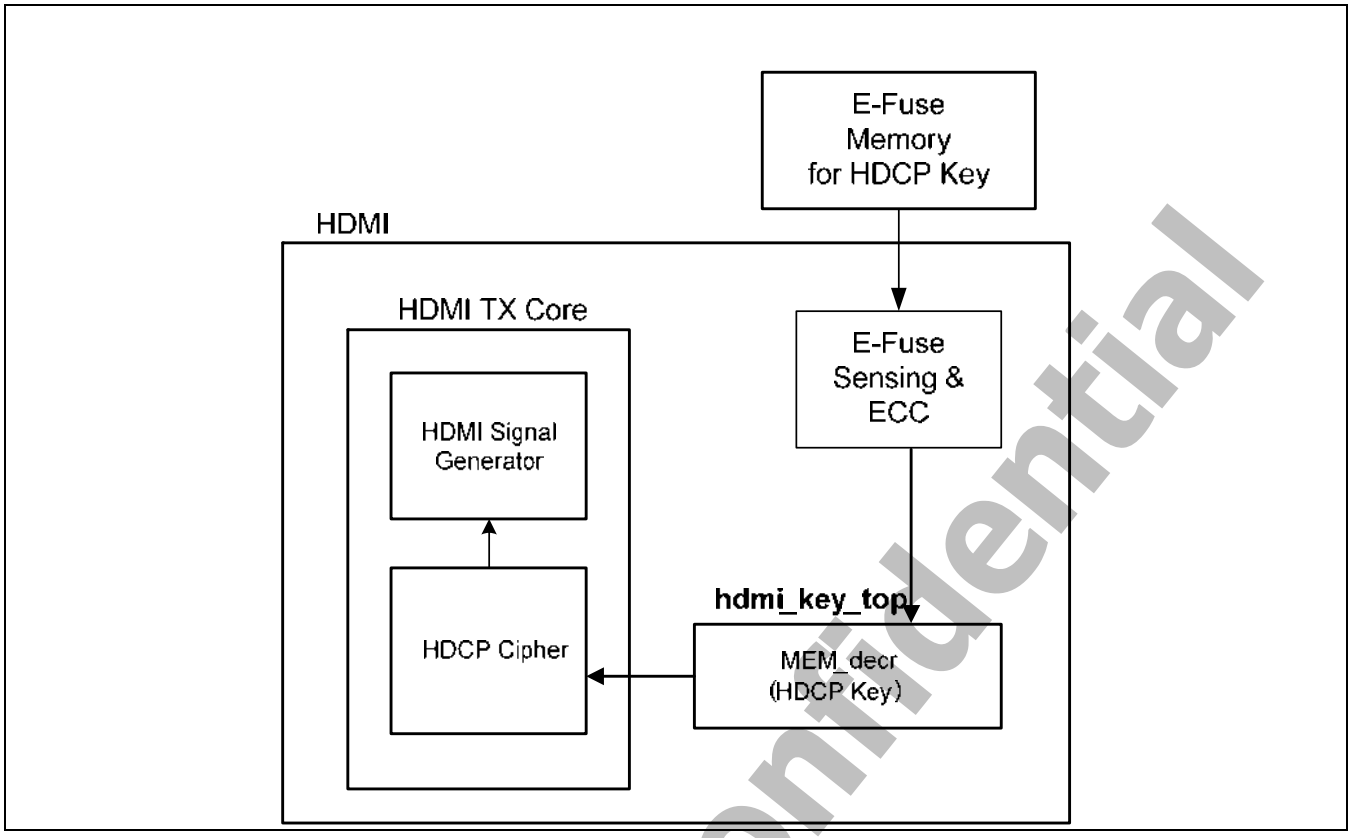

Figure 10-3 Block Diagram of HDCP Key Management

S5PV210 supports embedded HDCP key system. The HDCP key value is fused during fabrication, based on customers' request. S5PV210 strictly prohibits access to HDCP key value from any method. After S5PV210 boot up, the HDCP key is loaded using SFR from E-FUSE memory (HDCP_E_FUSE_CTRL, 0xFA16_000, [0] bit).

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10.1.5 VIDEO INPUT TIMING GUIDE FOR HDMI TIMING GENERATOR

Table 10-1 HDMI LINK Timing Generator Configuration Guide

	720x480p	720x576p	1280x720p	1920x1080i	1920x1080p
TG_H_FSZ_L(0xFA15_0018)	0x5a	0x60	0x72	0x98	0x98
TG_H_FSZ_H(0xFA15_001C)	0x03	0x03	0x06	0x08	0x08
TG_HACT_ST_L(0xFA15_0020)	0x8a	0x90	0x72	0x18	0x18
TG_HACT_ST_H(0XFA15_0024)	0x00	0x00	0x01	0x01	0x01
TG_HACT_SZ_L(0xFA15_0028)	0xd0	0xd0	0x00	0x80	0x80
TG_HACT_SZ_H(0xFA15_002C)	0x02	0x02	0x05	0x07	0x07
TG_V_FSZ_L(0xFA15_0030)	0x0d	0x71	0xee	0x65	0x65
TG_V_FSZ_H(0xFA15_0034)	0x02	0x02	0x02	0x04	0x04
TG_VSYNC_L(0xFA15_0038)	0x01	0x01	0x01	0x01	0x01
TG_VSYNC_H(0xFA15_003C)	0x00	0x00	0x00	0x00	0x00
TG_VSYNC2_L(0xFA15_0040)	Reset value	Reset value	Reset value	0x33	Reset value
TG_VSYNC2_H(0xFA15_0044)	Reset value	Reset value	Reset value	0x02	Reset value
TG_VACT_ST_L(0xFA15_0048)	0x2d	0x31	0x1e	0x16	0x2d
TG_VACT_ST_H(0xFA15_004C)	0x00	0x00	0x00	0x00	0x00
TG_VACT_SZ_L(0xFA15_0050)	0xe0	0xe0	0xd0	0x1c	0x38
TG_VACT_SZ_H(0xFA15_0054)	0x01	0x01	0x02	0x02	0x04
TG_FIELD_CHG_L(0xFA15_0058)	Reset value	Reset value	Reset value	0x33	Reset value
TG_FIELD_CHG_H(0xFA15_005C)	Reset value	Reset value	Reset value	0x02	Reset value
TG_VACT_ST2_L(0xFA15_0060)	Reset value	Reset value	Reset value	0x49	Reset value
TG_VACT_ST2_H(0xFA15_0064)	Reset value	Reset value	Reset value	0x02	Reset value
TG_VSYNC_TOP_HDMI_L (0xFA15_0078)	0x01	0x01	0x01	0x01	0x01
TG_VSYNC_TOP_HDMI_H (0xFA15_007C)	0x00	0x00	0x00	0x00	0x00
TG_VSYNC_BOT_HDMI_L (0xFA15_0080)	Reset value	Reset value	Reset value	0x33	Reset value
TG_VSYNC_BOT_HDMI_H (0xFA15_0084)	Reset value	Reset value	Reset value	0x02	Reset value
TG_FIELD_TOP_HDMI_L (0xFA15_0088)	0x01	0x01	0x01	0x01	0x01
TG_FIELD_TOP_HDMI_H (0xFA15_008C)	0x00	0x00	0x00	0x00	0x00

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	720x480p	720x576p	1280x720p	1920x1080i	1920x1080p
TG_FIELD_BOT_HDMI_L (0xFA15_0090)	Reset value	Reset value	Reset value	0x33	Reset value
TG_FIELD_BOT_HDMI_H (0xFA15_0094)	Reset value	Reset value	Reset value	0x02	Reset value

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10.1.6 HDMI PHY CONFIGURATION

HDMI PHY is configured using a dedicated I2C, which is only used in TX mode. The address of HDMI PHY is 0x70. The sequence of I2C data is shown in *Figure 10-4*.

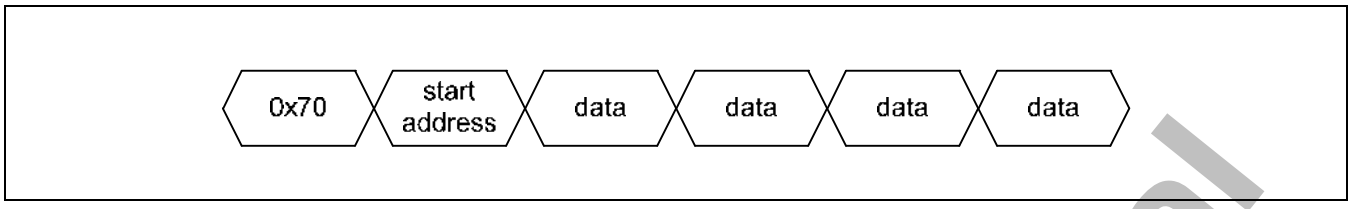

Figure 10-4 Sequence of I2C Data

We recommend following sequence for HDMI PHY configuration

1) Clock path change : CLK_SRC1 [0]_bit (0xE010_0204) is set to "0" (SCLK_PIXEL)

2) HDMI PHY configuration through I2C : refer to below table.

3) HDMI LINK core reset : CORE_RSTOUT [0]_bit (0xFA10_0020) is set to "0" for 100us.

4) PHY ready check

5) Clock path change : CLK_SRC1 [0]_bit (0xE010_0204) is set to "1" (SCLK_HDMIPHY)

Upper sequence is prior to configuration of VP, MIXER and HDMI LINK.

Due to the security policy, below table's configuration is only opened, as shown in *Table 10-2*.

Table 10-2 HDMI PHY Configuration Table for 27MHz OSC_In

Addr	27MHz (Pixel Clock Ratio)	27.027MHz	74.176MHz	74.25MHz
	8b	8b	8b	8b
0x01	05h	05h	05h	05h
0x02	00h	00h	00h	00h
0x03	D8h	D8h	D8h	D8h
0x04	10h	10h	10h	10h
0x05	1Ch	9Ch	9Ch	1Ch
0x06	30h	02h	56h	30h
0x07	40h	32h	5Bh	40h
0x08	6Bh	6Bh	6Bh	6Bh
0x09	10h	10h	10h	10h
0x0A	02h	02h	01h	01h
0x0B	52h	52h	52h	52h
0x0C	4Fh	4Fh	BFh	7Fh

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Addr	27MHz (Pixel Clock Ratio)	27.027MHz	74.176MHz	74.25MHz
	8b	8b	8b	8b
0x0D	F1h	F1h	F1h	F3h
0x0E	54h	54h	54h	54h
0x0F	78h	78h	A5h	A5h
0x10	84h	84h	84h	84h
0x11	00h	00h	00h	00h
0x12	00h	00h	00h	20h
0x13	38h	38h	38h	38h
0x14	00h	00h	00h	00h
0x15	08h	08h	08h	08h
0x16	10h	10h	10h	10h
0x17	E0h	E0h	E0h	E0h
0x18	22h	22h	22h	22h
0x19	40h	40h	40h	40h
0x1A	FFh	FFh	B9h	B9h
0x1B	26h	26h	26h	26h
0x1C	00h	00h	01h	01h
0x1D	00h	00h	00h	00h
0x1E	00h	00h	00h	00h
0x1F	80h	80h	80h	80h

Address 0x1f specifies the PHY_START control. If PHY is configured, the address 0x1f must be 0x0.

NOTE: It can be various configurations which depend on PCB environment.

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Table 10-3 HDMI PHY Configuration Table for 24MHz OSC_In

Addr	27MHz (Pixel Clock Ratio)	27.027MHz	74.176MHz	74.25MHz
	8b	8b	8b	8b
0x01	05h	05h	05h	05h
0x02	00h	00h	00h	00h
0x03	D8h	D4h	D8h	D8h
0x04	10h	10h	10h	10h
0x05	1Ch	9Ch	9Ch	9Ch
0x06	30h	09h	EFh	F8h
0x07	40h	64h	5Bh	40h
0x08	6Bh	6Bh	6Dh	6Ah
0x09	10h	10h	10h	10h
0x0A	02h	02h	01h	01h
0x0B	52h	52h	52h	52h
0x0C	DFh	DFh	EFh	FFh
0x0D	F2h	F2h	F3h	F1h
0x0E	54h	54h	54h	54h
0x0F	87h	87h	B9h	BAh
0x10	84h	84h	84h	84h
0x11	00h	00h	00h	00h
0x12	30h	30h	30h	10h
0x13	38h	38h	38h	38h
0x14	00h	00h	00h	00h
0x15	08h	08h	08h	08h
0x16	10h	10h	10h	10h
0x17	E0h	E0h	E0h	E0h
0x18	22h	22h	22h	22h
0x19	40h	40h	40h	40h
0x1A	E3h	E2h	A5h	A4h
0x1B	26h	26h	26h	26h
0x1C	00h	00h	01h	01h
0x1D	00h	00h	00h	00h
0x1E	00h	00h	00h	00h
0x1F	80h	80h	80h	80h

Address 0x1f specifies the PHY_START control. If PHY is configured, the address 0x1f must be 0x0.

NOTE: It can be various configurations which depend on PCB environment.

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10.1.7 SELECTED I2C REGISTER CONTROL

Name	Code	Description
Reference Clock Selection (Reg 12 bit[4])	0	External Crystal
	1	Internal Oscillator Input(XXTI or XusbXTI)
	It selects reference clock between external crystal and internal oscillator input.	
Pixel Clock Selection (Reg 12 bit[7])	0	Internally generated pixel clock by internal video pll
	1	Externally supplied pixel clock by external VPLL. (refer to Figure 10-5)
	The internal video pll can be used for pixel clock generation. If the externally supplied pixel clock is used, the internal video pll can be configured as jitter-filter pll or by-passed. Because of clock-jitter, we recommend the internal video pll.	
Power Down	0	Operation mode
	1	Power-down mode
	REG01 bit[5] : Bias power down REG01 bit[7] : Sigma delta modulator clock generator power down REG05 bit[5] : PLL power down REG17 bit[0] : PCG power down REG17 bit[1] : TX power down	
TMDS Data Amplitude Control (Reg 18 bit[3:0])	4'b1111	Maximum amplitude
	4'b0000	Minimum amplitude
	TMDS data amplitude control	
TMDS Clock Amplitude Control (Reg 18 bit[7:4])	4'b1111	Maximum amplitude
	4'b0000	Minimum amplitude
	TMDS clock amplitude control	
TMDS Data Pre-emphasis Control (Reg 19 bit[2:0])	3'b000	No pre-emphasis
	3'b111	Max pre-emphasis
	TMDS data pre-emphasis	
Oscillator Pad Control (Reg 19 bit[7:6])	2'b01	Oscillator pad is on.
	2'b10	Oscillator pad is off.
	Oscillator pad control	
PHY Mode Set Done (Reg 0x1F bit[7])	0	Mode setting is in progress
	1	Mode setting is done
	For PHY mode setting without reset, this bit is used as mode setting status flag. If this bit is "0", mode setting through I2C is in progress. If all setting is done, this bit should be set "1" again.	

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10.1.8 I/O DESCRIPTION OF HDMI PHY

Pin Name	Pin Function	Description
XhdmiTX0P	Output	TMDS output data pairs.
XhdmiTX0N	Output	
XhdmiTX1P	Output	
XhdmiTX1N	Output	
XhdmiTX2P	Output	
XhdmiTX2N	Output	
XhdmiTXCP	Output	TMDS output clock pair.
XhdmiTXCN	Output	
XhdmiREXT	Input	External Reference Resistor. External reference resistor input. A 4.6K, 1% resistor is connected to ground.
XhdmiXTI	Input	Reference Clock Input. Crystal oscillator input. It is used to generate internal clock signals. It's nominal frequency is 27MHz.
XhdmiXTO	Output	Reference Clock Output. Crystal oscillator output.

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10.1.9 BLOCK DIAGRAM OF CLOCK STRATEGY FOR HDMI TX

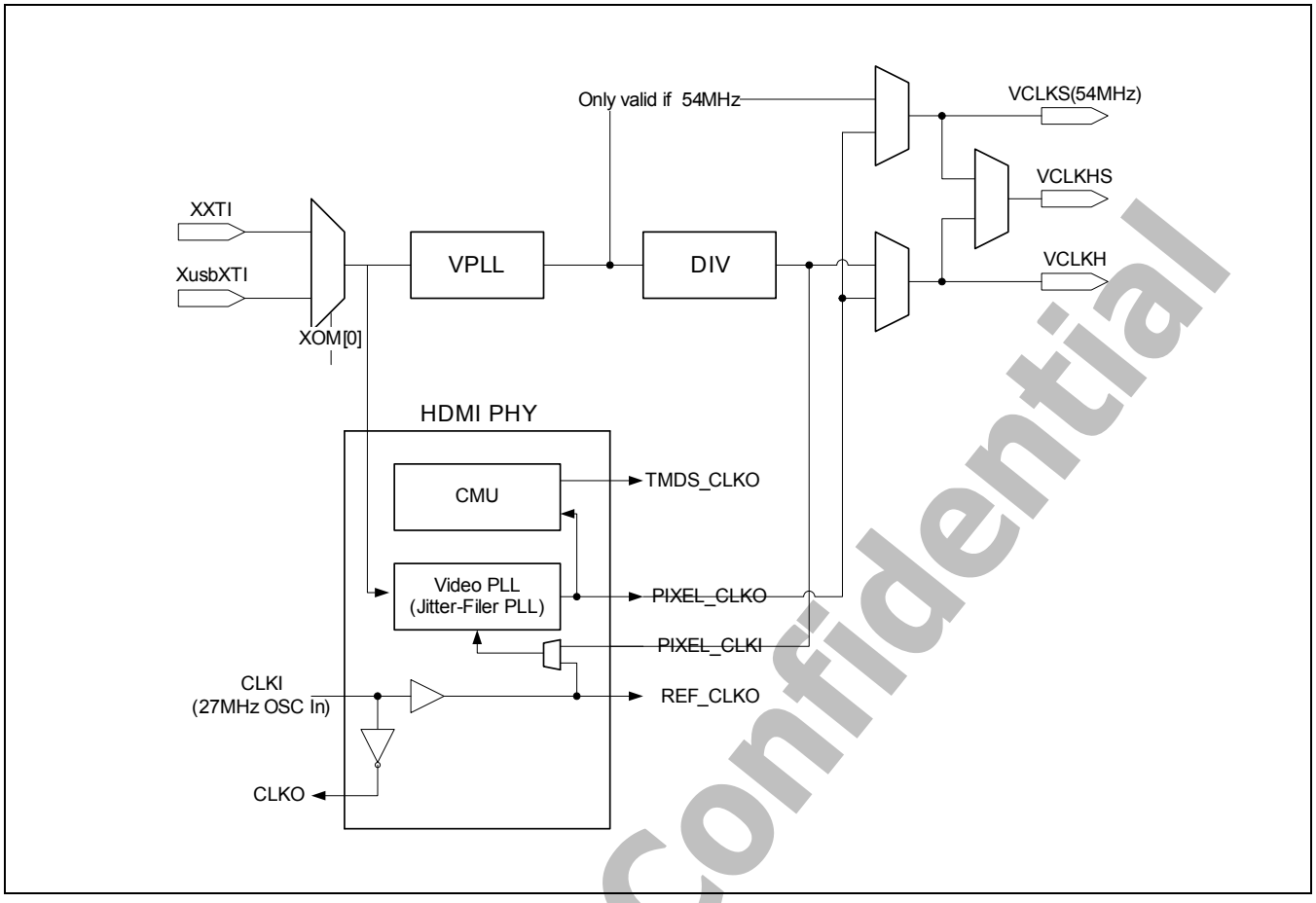

Figure 10-5 Block Diagram of HDMI TX Clock Scheme in S5PV210

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The HDMI link part uses pixel and TMDS clock. Pixel and TMDS clocks are from HDMI PHY. You must configure it before use. VCLKHS (MIXER pixel clock) and VCLKH (HDMI pixel clock) are synchronous. Thus, the same clock is fed through VCLKHS and VCLKH. For pixel frequency, refer to *Figure 10-6*.

VCLKHS(or VCLKH) usage frequency

Vertical Freq.	Format	Pixel Freq.
59.94 Hz	480P	27MHz (or 54MHz)
	720P	74.175MHz
	1080I	74.175MHz
60.00 Hz	480P	27.027MHz (or 54.054MHz)
	720P	74.250MHz
	1080I	74.250MHz
50.00 Hz	576P	27MHz (or 54MHz)
	720P	74.250MHz
	1080I	74.250MHz
29.97Hz	1080P	74.175MHz
30Hz	1080P	74.250MHz
25Hz	1080P	74.250MHz
Summary		27MHz
		27.027MHz
		54MHz
		54.054MHz
		74.175MHz
		74.250MHz

Figure 10-6 Frequency Summary in Use

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10.2 SPDIF (AUXILIARY INFORMATION)

10.2.1 FRAME FORMAT

A frame is composed of two sub-frames. The transmission rate of frames corresponds exactly to the source sampling frequency. In the 2-channel operation mode, the samples taken from both channels are transmitted by time multiplexing in consecutive sub-frames.

Usually, sub-frames related to channel 1 (left or “A” channel in stereophonic operation and primary channel in monophonic operation) use preamble M. However, the preamble is changed to preamble B once every 192 frames. This unit is composed of 192 frames. It defines the block structure used to organize the channel status information.

On the other hand, sub-frames of channel 2 (right or “B” in stereophonic operation and secondary channel in monophonic operation) always use preamble W. In single channel operation mode and broadcasting studio environment, the frame format is identical to 2-channel mode. The data is only carried in channel 1. In the sub-frames allocated to channel 2, time slot 28 (validity flag) is set to logical “1” (invalid).

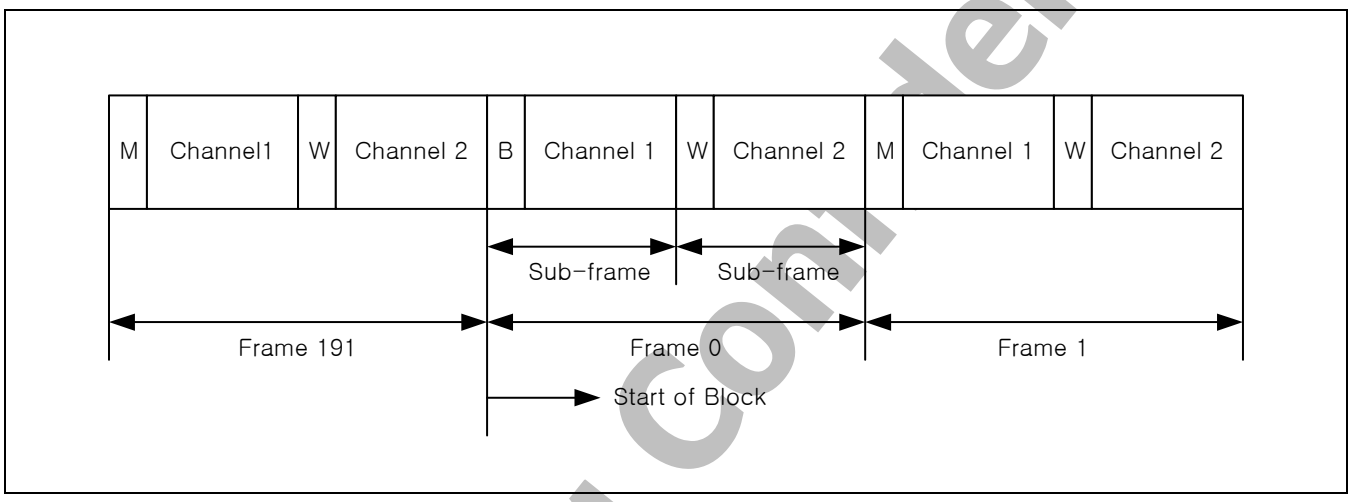

Figure 10-7 Frame Format

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10.2.1.1 Sub-frame Format (IEC 60958)

Each sub-frame is divided into 32 time slots numbered from 0 to 31. Time slots from 0 to 3 carry one of the three permitted preambles. These slots affect the synchronization of sub-frames, frames, and blocks. Time slots from 4 to 27 carry the audio sample word in linear 2's complement representation.

The most significant bit (MSB) is carried by time slot 27. When a 24-bit coding range is used, the least significant bit (LSB) is in the time slot 4.

When a 20-bit coding range is sufficient, the LSB is in the time slot 8, and time slots from 4 to 7 may be used for other applications. Under these circumstances, the bits in the time slots 4 to 7 are designated auxiliary sample bits.

If the source provides fewer bits than what the interface allows (24 or 20), the unused LSBs are set to a logical "0". By this procedure, the equipment using different numbers of bits can be connected together.

- Time slot 28 carries the validity flag associated with audio sample word. This flag is set to logical "0" if the audio sample is reliable.
- Time slot 29 carries one bit of user data associated with audio channel that is transmitted in the same sub-frame. The default value of user bit is logical "0".
- Time slot 30 carries one bit of channel status words associated with audio channel that is transmitted in the same sub-frame.
- Time slot 31 carries a parity bit such that time slots from 4 to 31 (inclusive) will carry an even number of ones and an even number of zeros.

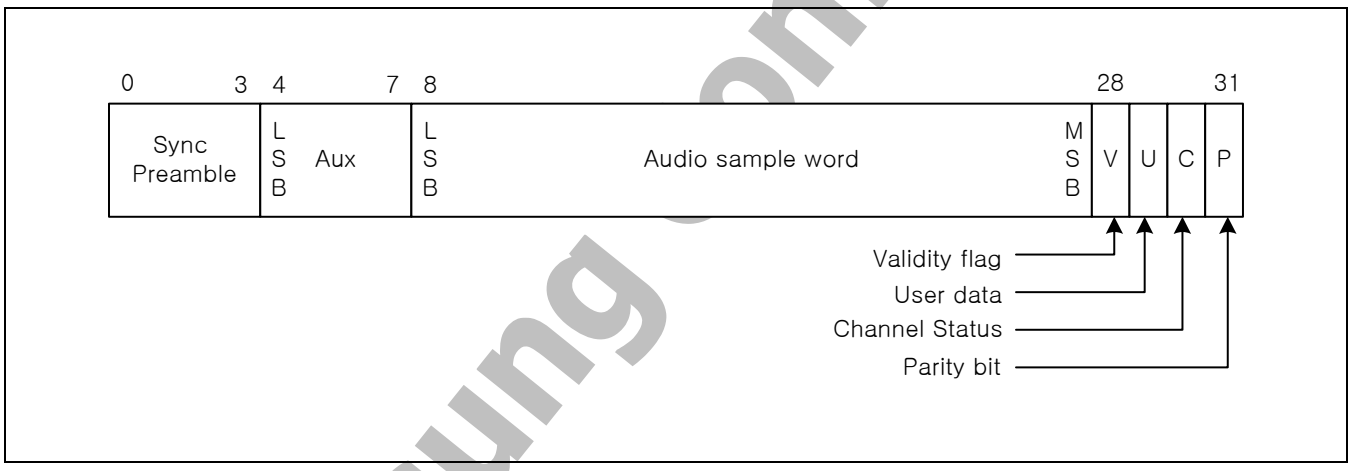

Figure 10-8 Sub-frame Format

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10.2.1.2 Channel Status Block (IEC-60958-3)

Channel Status Block specifies the aggregation of Channel Status bit in each sub-frame, as shown in *Figure 10-9*. As one frame consists of 192 frames, one channel status block can be obtained for one channel.

This block holds the information of the stream being transmitted such as application, stream type, sampling frequency, word length, and so on.

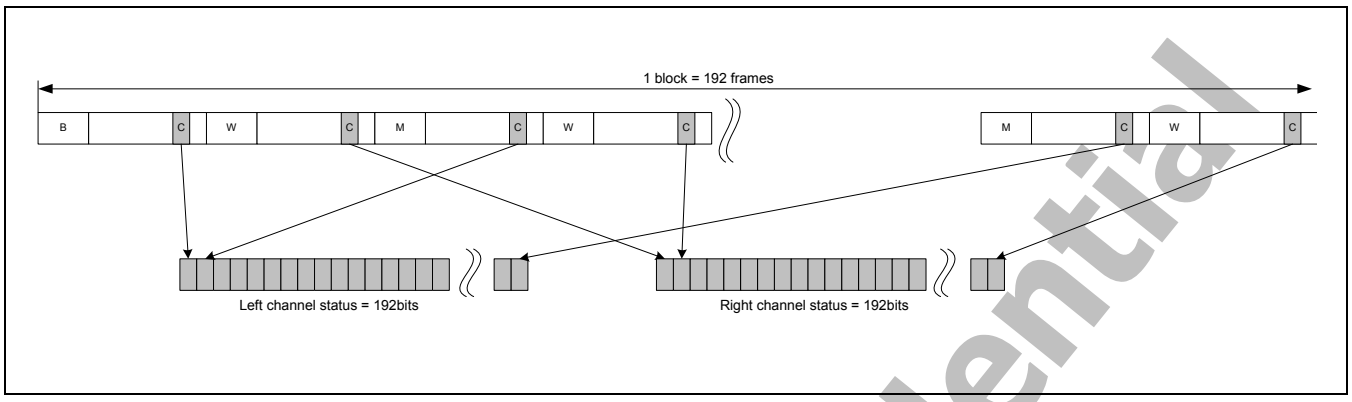

Figure 10-9 Channel Status Block Extract from SPDIF Stream

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Byte									
0		a = "0"	b = "0"	c	d			Mode = "0 0"	
	bit	0	1	2	3	4	5	6	7
1		Category code							
	bit	8	9	10	11	12	13	14	15
2		Source number				Channel number			
	bit	16	17	18	19	20	21	22	23
3		Sampling frequency				Clock accuracy			
	bit	24	25	26	27	28	29	30	31
4		Word length				Original sampling frequency			
	bit	32	33	34	35	36	37	38	39
5									
	bit	40	41	42	43	44	45	46	47
6									
	bit	48	49	50	51	52	53	54	55
7									
	bit	56	57	58	59	60	61	62	63
8									
	bit	64	65	66	67	68	69	70	71
9									
	bit	72	73	74	75	76	77	78	79
10									
	bit	80	81	82	83	84	85	86	87
11									
	bit	88	89	90	91	92	93	94	95
12									
	bit	96	97	98	99	100	101	102	103
13									
	bit	104	105	106	107	108	109	110	111
14									
	bit	112	113	114	115	116	117	118	119
15									
	bit	120	121	122	123	124	125	126	127
16									
	bit	128	129	130	131	132	133	134	135
17									
	bit	136	137	138	139	140	141	142	143
18									
	bit	144	145	146	147	148	149	150	151
19									
	bit	152	153	154	155	156	157	158	159
20									
	bit	160	161	162	163	164	165	166	167
21									
	bit	168	169	170	171	172	173	174	175
22									
	bit	176	177	178	179	180	181	182	183
23									
	bit	184	185	186	187	188	189	190	191
		a: use of channel status block. b: linear PCM identification.				c: copyright information. d: additional format information.			

Figure 10-10 Channel Status Block

10.2.1.3 Channel Coding

Time slots from 4 to 31 are encoded in bi-phase mark to:

- Minimize the DC component on transmission line
- Facilitate clock recovery from the data stream
- Make the interface insensitive to polarity of connections

Each bit that needs to be transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logical “0” and different from the first if the bit is logical “1”.

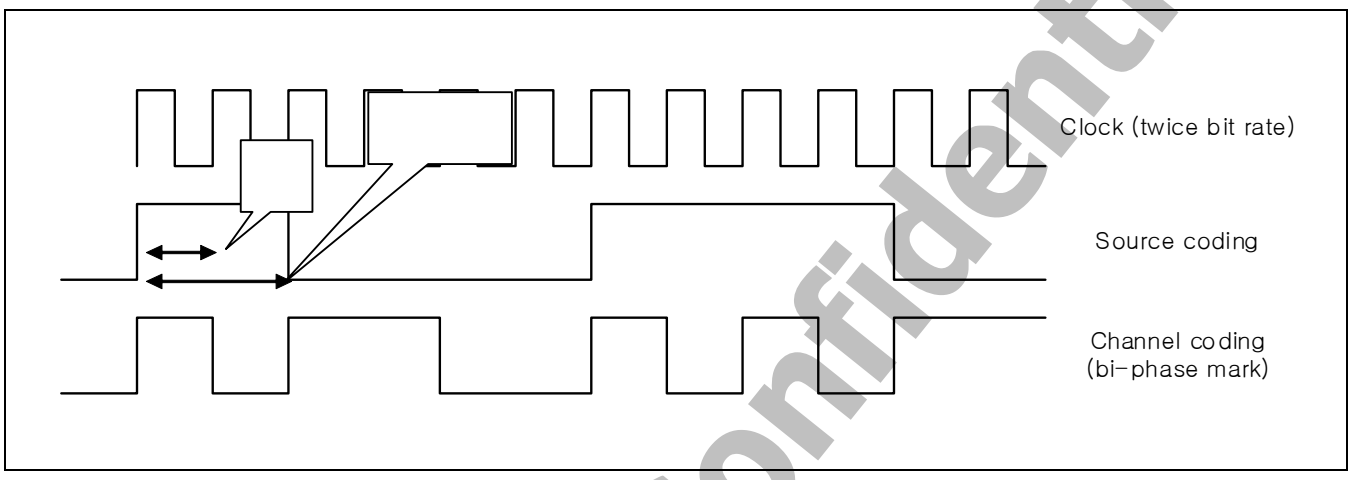

Figure 10-11 Channel coding

10.2.1.4 Preamble

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks. A set of three preambles is used. These preambles are transmitted in the time allocated to four time slots (time slots 0 to 3) and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol. Like bi-phase code, these preambles are DC independent and provide clock recovery. They differ in at least two states from any valid bi-phase sequence.

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10.2.1.5 Non-Linear PCM Encoded Source (IEC 61937)

The non-linear PCM encoded audio bitstream is transferred using the basic 16-bit data area of the IEC 60958 subframes, that is, in time slots from 12 to 27. Each IEC 60958 frame transfers 32-bits of non-PCM data in consumer application mode.

When the SPDIF bitstream conveys linear PCM audio, the symbol frequency is 64 times the PCM sampling frequency (32 time slots per PCM sample times two channels).

When the interface transmits non-linear PCM encoded audio bitstream, the symbol frequency is 64 times the sampling rate of the encoded audio within that bitstream.

In case the interface containing audio with low sampling frequency conveys a non-linear PCM encoded audio bitstream, the symbol frequency is 128 times the sampling rate of the encoded audio within that bitstream.

Each data burst contains a burst-preamble consisting of four 16-bit words (Pa, Pb, Pc, and Pd); followed by the burst-payload that contains data of an encoded audio frame.

The burst-preamble consists of four mandatory fields. Pa and Pb represent a synchronization word; Pc gives information about the type of data and some information/ control for the receiver; and Pd gives the length of the burst-payload, limited to 216(=65,535) bits.

The four preamble words are contained in two sequential SPDIF frames. The frame beginning the data-burst contains preamble word Pa in sub-frame 1 and Pb in sub-frame 2. The next frame contains Pc in sub-frame 1 and Pd in sub-frame 2. When placed into a SPDIF sub-frame, the MSB of a 16-bit burst-preamble is placed into time slot 27 and the LSB is placed into time slot 12.

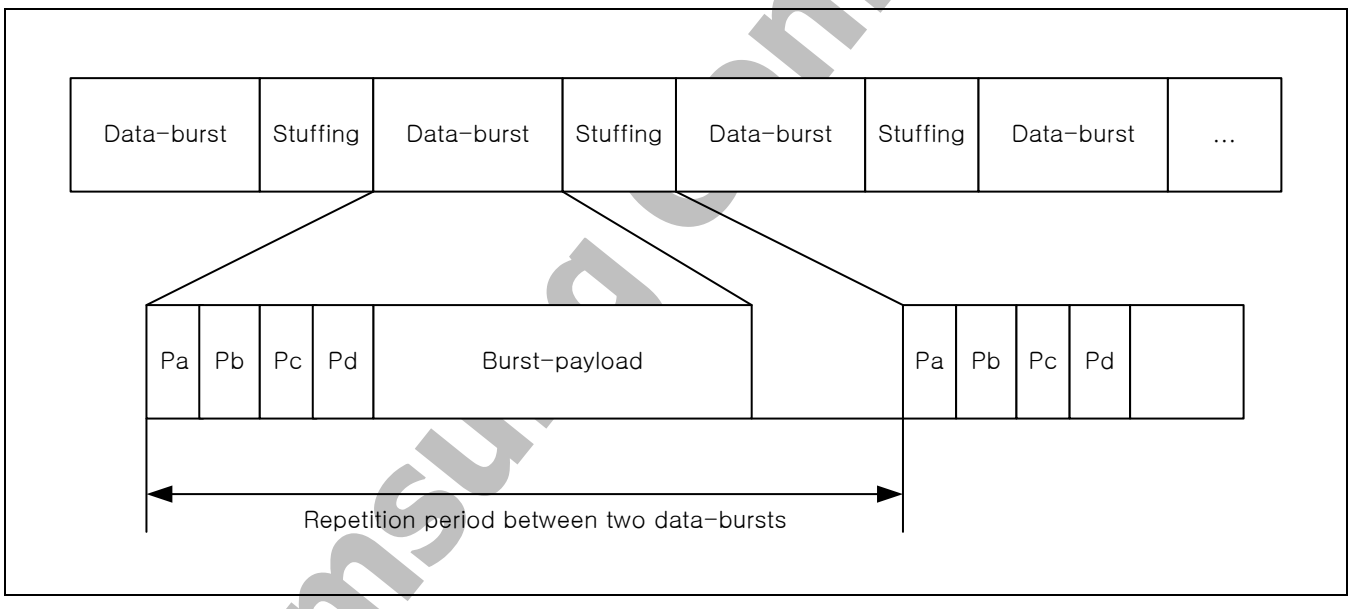

Figure 10-12 Non-linear PCM Format

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10.3 REGISTRS DESCRIPTION

The register address map of HDMI 1.3 Tx Subsystem is divided into register address space of sub-modules, as shown in *Table 10-4*.

Table 10-4 Register Address Map

Register Base	Address	Description
CTRL_BASE	0xFA10_0000	Specifies the controller register base address.
HDMI_CORE_BASE	0xFA11_0000	Specifies the HDMI register base address.
SPDIF_BASE	0xFA13_0000	Specifies the SPDIF receiver register base address.
I2S_BASE	0xFA14_0000	Specifies the I2S receiver register base address.
TG_BASE	0xFA15_0000	Specifies the HDMI timing generator register base address.
eFUSE_BASE	0xFA16_0000	Specifies the e-fuse related register base address.
CEC_BASE	0xE1B0_0000	Specifies the CEC register base address.

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10.3.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
Control Registers				
INTC_CON	0xFA10_0000	R/W	Specifies the interrupt control register.	0x00
INTC_FLAG	0xFA10_0004	R/W	Specifies the interrupt flag register.	0x00
HDCP_KEY_LOAD	0xFA10_0008	R	Specifies the HDCP key status.	0x00
HPD_STATUS	0xFA10_000C	R	Specifies the value of HPD signal.	0x00
AUDIO_CLKSEL	0xFA10_0010	R/W	Selects the audio system clock.	0x00
PHY_RSTOUT	0xFA10_0014	R/W	Specifies the HDMI PHY reset out.	0x00
PHY_VPLL	0xFA10_0018	R	Specifies the HDMI PHY VPLL monitor.	0x00
PHY_CMU	0xFA10_001C	R	Specifies the HDMI PHY CMU monitor.	0x00
CORE_RSTOUT	0xFA10_0020	R/W	Specifies the HDMI TX core software reset.	0x01
HDMI Core Registers (Control Registers)				
HDMI_CON_0	0xFA11_0000	R/W	Specifies the HDMI system control register 0.	0x00
HDMI_CON_1	0xFA11_0004	R/W	Specifies the HDMI system control register 1.	0x00
HDMI_CON_2	0xFA11_0008	R/W	Specifies the HDMI system control register 2.	0x00
STATUS	0xFA11_0010	R/W	Specifies the HDMI system status register.	0x00
PHY_STATUS	0xFA11_0014	R	Specifies the PHY status register.	0x00
STATUS_EN	0xFA11_0020	R/W	Specifies the HDMI system status enable register.	0x00
HPD	0xFA11_0030	R/W	Specifies the HPD control register.	0x00
MODE_SEL	0xFA11_0040	R/W	Selects the HDMI/ DVI mode.	0x00
ENC_EN	0xFA11_0044	R/W	Specifies the HDCP encryption enable register.	0x00
HDMI Core Registers (Video Related Registers)				
BLUE_SCREEN_0	0xFA11_0050	R/W	Specifies the pixel values for blue screen.	0x00
BLUE_SCREEN_1	0xFA11_0054	R/W	Specifies the pixel values for blue screen.	0x00
BLUE_SCREEN_2	0xFA11_0058	R/W	Specifies the pixel values for blue screen.	0x00
HDMI_YMAX	0xFA11_0060	R/W	Specifies the maximum Y (or R, G, B) pixel value.	0xeb
HDMI_YMIN	0xFA11_0064	R/W	Specifies the minimum Y (or R, G, B) pixel value.	0x10
HDMI_CMAX	0xFA11_0068	R/W	Specifies the maximum Cb/ Cr pixel value.	0xf0
HDMI_CMIN	0xFA11_006C	R/W	Specifies the minimum Cb/ Cr pixel value.	0x10
H_BLANK_0	0xFA11_00A0	R/W	Specifies the horizontal blanking setting.	0x00
H_BLANK_1	0xFA11_00A4	R/W	Specifies the horizontal blanking setting.	0x00
V_BLANK_0	0xFA11_00B0	R/W	Specifies the vertical blanking setting.	0x00
V_BLANK_1	0xFA11_00B4	R/W	Specifies the vertical blanking setting.	0x00

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Register	Address	R/W	Description	Reset Value
V_BLANK_2	0xFA11_00B8	R/W	Specifies the vertical blanking setting.	0x00
H_V_LINE_0	0xFA11_00C0	R/W	Specifies the horizontal and vertical line setting.	0x00
H_V_LINE_1	0xFA11_00C4	R/W	Specifies the horizontal and vertical line setting.	0x00
H_V_LINE_2	0xFA11_00C8	R/W	Specifies the horizontal and vertical line setting.	0x00
VSYNC_POL	0xFA11_00E4	R/W	Specifies the vertical sync polarity control register.	0x00
INT_PRO_MODE	0xFA11_00E8	R/W	Specifies the Interlace/ Progressive control register.	0x00
V_BLANK_F_0	0xFA11_0110	R/W	Specifies the vertical blanking setting for bottom field.	0x00
V_BLANK_F_1	0xFA11_0114	R/W	Specifies the vertical blanking setting for bottom field.	0x00
V_BLANK_F_2	0xFA11_0118	R/W	Specifies the vertical blanking setting for bottom field.	0x00
H_SYNC_GEN_0	0xFA11_0120	R/W	Specifies the horizontal sync generation setting.	0x00
H_SYNC_GEN_1	0xFA11_0124	R/W	Specifies the horizontal sync generation setting.	0x00
H_SYNC_GEN_2	0xFA11_0128	R/W	Specifies the horizontal sync generation setting.	0x00
V_SYNC_GEN1_0	0xFA11_0130	R/W	Specifies the vertical sync generation for top field or frame.	0x01
V_SYNC_GEN1_1	0xFA11_0134	R/W	Specifies the vertical sync generation for top field or frame.	0x10
V_SYNC_GEN1_2	0xFA11_0138	R/W	Specifies the vertical sync generation for top field or frame.	0x00
V_SYNC_GEN2_0	0xFA11_0140	R/W	Specifies the vertical sync generation for bottom field – vertical position.	0x01
V_SYNC_GEN2_1	0xFA11_0144	R/W	Specifies the vertical sync generation for bottom field – vertical position.	0x10
V_SYNC_GEN2_2	0xFA11_0148	R/W	Specifies the vertical sync generation for bottom field – vertical position.	0x00
V_SYNC_GEN3_0	0xFA11_0150	R/W	Specifies the vertical sync generation for bottom field – horizontal position.	0x01
V_SYNC_GEN3_1	0xFA11_0154	R/W	Specifies the vertical sync generation for bottom field – horizontal position.	0x10
V_SYNC_GEN3_2	0xFA11_0158	R/W	Specifies the vertical sync generation for bottom field – horizontal position.	0x00
HDMI Core Registers (Audio Related Registers)				

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Register	Address	R/W	Description	Reset Value
ASP_CON	0xFA11_0160	R/W	Specifies the ASP packet control register.	0x00
ASP_SP_FLAT	0xFA11_0164	R/W	Specifies the ASP packet sp_flat bit control.	0x00
ASP_CHCFG0	0xFA11_0170	R/W	Specifies the ASP audio channel configuration.	0x08
ASP_CHCFG1	0xFA11_0174	R/W	Specifies the ASP audio channel configuration.	0x1a
ASP_CHCFG2	0xFA11_0178	R/W	Specifies the ASP audio channel configuration.	0x2c
ASP_CHCFG3	0xFA11_017C	R/W	Specifies the ASP audio channel configuration.	0x3e
ACR_CON	0xFA11_0180	R/W	Specifies the ACR packet control register.	0x00
ACR_MCTS0	0xFA11_0184	R/W	Specifies the measured CTS value.	0x01
ACR_MCTS1	0xFA11_0188	R/W	Specifies the measured CTS value.	0x00
ACR_MCTS2	0xFA11_018C	R/W	Specifies the measured CTS value.	0x00
ACR_CTS0	0xFA11_0190	R/W	Specifies the CTS value for fixed CTS transmission mode.	0xe8
ACR_CTS1	0xFA11_0194	R/W	Specifies the CTS value for fixed CTS transmission mode.	0x03
ACR_CTS2	0xFA11_0198	R/W	Specifies the CTS value for fixed CTS transmission mode.	0x00
ACR_N0	0xFA11_01A0	R/W	Specifies the N value for ACR packet.	0xe8
ACR_N1	0xFA11_01A4	R/W	Specifies the N value for ACR packet.	0x03
ACR_N2	0xFA11_01A8	R/W	Specifies the N value for ACR packet.	0x00
ACR_LSB2	0xFA11_01B0	R/W	Specifies the alternate LSB for fixed CTS transmission mode.	0x00
ACR_TXCNT	0xFA11_01B4	R/W	Specifies the number of ACR packet transmission per frame.	0x1f
ACR_TXINTERVAL	0xFA11_01B8	R/W	Specifies the interval for ACR packet transmission.	0x63
ACR_CTS_OFFSET	0xFA11_01BC	R/W	Specifies the CTS offset for measured CTS mode.	0x00
HDMI Core Registers (Packet Related Registers)				
GCP_CON	0xFA11_01C0	R/W	Specifies the ACR packet control register.	0x04
GCP_BYTE1	0xFA11_01D0	R/W	Specifies the GCP packet body.	0x00
GCP_BYTE2	0xFA11_01D4	R/W	Specifies the GCP packet body.	0x00
GCP_BYTE3	0xFA11_01D8	R/W	Specifies the GCP packet body.	0x00
ACP_CON	0xFA11_01E0	R/W	Specifies the ACP packet control register.	0x00
ACP_TYPE	0xFA11_01F0	R/W	Specifies the ACP packet header.	0x00

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Register	Address	R/W	Description	Reset Value
ACP_DATA00~16	0xFA11_0200 ~ 0xFA11_0240	R/W	Specifies the ACP packet body.	0x00
ISRC_CON	0xFA11_0250	R/W	Specifies the ACR packet control register.	0x00
ISRC1_HEADER1	0xFA11_0264	R/W	Specifies the ISCR1 packet header.	0x00
ISRC1_DATA00~15	0xFA11_0270 ~ 0xFA11_02AC	R/W	Specifies the ISRC1 packet body.	0x00
ISRC2_DATA00~15	0xFA11_02B0 ~ 0xFA11_02EC	R/W	Specifies the ISRC2 packet body.	0x00
AVI_CON	0xFA11_0300	R/W	Specifies the AVI packet control register.	0x00
AVI_CHECK_SUM	0xFA11_0310	R/W	Specifies the AVI packet checksum.	0x00
AVI_BYTE01~13	0xFA11_0320 ~ 0xFA11_0350	R/W	Specifies the AVI packet body.	0x00
AUI_CON	0xFA11_0360	R/W	Specifies the AUI packet control register.	0x00
AUI_CHECK_SUM	0xFA11_0370	R/W	Specifies the AUI packet checksum.	0x00
AUI_BYTE1~5	0xFA11_0380 ~ 0xFA11_0390	R/W	Specifies the AUI packet body.	0x00
MPG_CON	0xFA11_03A0	R/W	Specifies the ACR packet control register.	0x00
MPG_CHECK_SUM	0xFA11_03B0	R/W	Specifies the MPG packet checksum.	0x00
MPG_BYTE1~5	0xFA11_03C0 ~ 0xFA11_03D0	R/W	Specifies the MPG packet body.	0x00
SPD_CON	0xFA11_0400	R/W	Specifies the SPD packet control register.	0x00
SPD_HEADER0	0xFA11_0410	R/W	Specifies the SPD packet header.	0x00
SPD_HEADER1	0xFA11_0414	R/W	Specifies the SPD packet header.	0x00
SPD_HEADER2	0xFA11_0418	R/W	Specifies the SPD packet header.	0x00
SPD_DATA00~27	0xFA11_0420 ~ 0xFA11_048C	R/W	Specifies the SPD packet body.	0x00
HDMI Core Registers (HDCP Related Register)				
HDCP_SHA1_00~19	0xFA11_0600 ~ 0xFA11_064C	R/W	Specifies the SHA-1 value from repeater.	0x00
HDCP_KSV_LIST_0 ~4	0xFA11_0650 ~ 0xFA11_0660	R/W	Specifies the KSV list from repeater.	0x00
HDCP_KSV_LIST_CON	0xFA11_0664	R/W	Controls the KSV list.	0x01

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Register	Address	R/W	Description	Reset Value
HDCP_SHA_RESULT	0xFA11_0670	R/W	Specifies the SHA-1 checking result register.	0x00
HDCP_CTRL1	0xFA11_0680	R/W	Specifies the HDCP control register1.	0x00
HDCP_CTRL2	0xFA11_0684	R/W	Specifies the HDCP control register2.	0x00
HDCP_CHECK_RESULT	0xFA11_0690	R/W	Checks the result of Ri and Pj values.	0x00
HDCP_BKSV_0~4	0xFA11_06A0 ~ 0xFA11_06B0	R/W	Specifies the KSV of Rx.	0x00
HDCP_AKSV_0~4	0xFA11_06C0 ~ 0xFA11_06D0	R/W	Specifies the KSV of Tx.	0x00
HDCP_An_0~7	0xFA11_06E0 ~ 0xFA11_06FC	R/W	Specifies the An value.	0x00
HDCP_BCAPS	0xFA11_0700	R/W	Specifies the BCAPS from Rx.	0x00
HDCP_BSTATUS_0	0xFA11_0710	R/W	Specifies the BSTATUS from Rx.	0x00
HDCP_BSTATUS_1	0xFA11_0714	R/W	Specifies the BSTATUS from Rx.	0x00
HDCP_Ri_0	0xFA11_0740	R/W	Specifies the Ri value of Tx.	0x00
HDCP_Ri_1	0xFA11_0744	R/W	Specifies the Ri value of Tx.	0x00
HDCP_I2C_INT	0xFA11_0780	R/W	Specifies the I2C interrupt flag.	0x00
HDCP_AN_INT	0xFA11_0790	R/W	Specifies the An value ready interrupt flag.	0x00
HDCP_WATCGDOG_INT	0xFA11_07A0	R/W	Specifies the Watchdog interrupt flag.	0x00
HDCP_Ri_INT	0xFA11_07B0	R/W	Specifies the Ri value update interrupt flag.	0x00
HDCP_Ri_Compare_0	0xFA11_07D0	R/W	Specifies the HDCP Ri interrupt frame number index register 0.	0x80
HDCP_Ri_Compare_1	0xFA11_07D4	R/W	Specifies the HDCP Ri interrupt frame number index register 1.	0x7f
HDCP_Frame_Count	0xFA11_07E0	R	Specifies the current value of frame count index in the hardware.	0x00
GAMUT_CON	0xFA11_0500	R/W	Specifies the GAMUT packet control register.	0x00
GAMUT_HEADER0	0xFA11_0504	R/W	Specifies the GAMUT packet header.	0x00
GAMUT_HEADER1	0xFA11_0508	R/W	Specifies the GAMUT packet header.	0x00
GAMUT_HEADER2	0xFA11_050C	R/W	Specifies the GAMUT packet header.	0x00
GAMUT_DATA00~27	0xFA11_0510 ~ 0xFA11_057C	R/W	Specifies the GAMUT packet body.	0x00
-	0xFA11_05C0	R/W	Reserved. Do not modify this.	0x00

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Register	Address	R/W	Description	Reset Value
VIDEO_PATTERN_GEN	0xFA11_05C4	R/W	Specifies the video pattern generation register.	0x00
HPD_GEN	0xFA11_05C8	R/W	Specifies the HPD duration value register.	0x01
SPDIF Registers				
SPDIFIN_CLK_CTRL	0xFA13_0000	R/W	Specifies the SPDIFIN clock control register.	0x02
SPDIFIN_OP_CTRL	0xFA13_0004	R/W	Specifies the SPDIFIN operation control register 1.	0x00
SPDIFIN_IRQ_MASK	0xFA13_0008	R/W	Specifies the SPDIFIN interrupt request mask register.	0x00
SPDIFIN_IRQ_STATUS	0xFA13_000C	R/W	Specifies the SPDIFIN interrupt request status register.	0x00
SPDIFIN_CONFIG_1	0xFA13_0010	R/W	Specifies the SPDIFIN configuration register 1.	0x02
SPDIFIN_CONFIG_2	0xFA13_0014	R/W	Specifies the SPDIFIN configuration register 2.	0x00
-	0xFA13_0018	-	Reserved	-
-	0xFA13_001C	-	Reserved	-
SPDIFIN_USER_VALUE_1	0xFA13_0020	R/W	Specifies the SPDIFIN user value register 1.	0x00
SPDIFIN_USER_VALUE_2	0xFA13_0024	R/W	Specifies the SPDIFIN user value register 2.	0x00
SPDIFIN_USER_VALUE_3	0xFA13_0028	R/W	Specifies the SPDIFIN user value register 3.	0x00
SPDIFIN_USER_VALUE_4	0xFA13_002C	R/W	Specifies the SPDIFIN user value register 4.	0x00
SPDIFIN_CH_STATUS_0_1	0xFA13_0030	R	Specifies the SPDIFIN channel status register 0-1.	0x00
SPDIFIN_CH_STATUS_0_2	0xFA13_0034	R	Specifies the SPDIFIN channel status register 0-2.	0x00
SPDIFIN_CH_STATUS_0_3	0xFA13_0038	R	Specifies the SPDIFIN channel status register 0-3.	0x00
SPDIFIN_CH_STATUS_0_4	0xFA13_003C	R	Specifies the SPDIFIN channel status register 0-4.	0x00
SPDIFIN_CH_STATUS_1	0xFA13_0040	R	Specifies the SPDIFIN channel status register 1.	0x00
-	0xFA13_0044	-	Reserved	-
SPDIFIN_FRAME_PERIOD_1	0xFA13_0048	R	Specifies the SPDIFIN frame period register 1.	0x00
SPDIFIN_FRAME_PERIOD_2	0xFA13_004C	R	Specifies the SPDIFIN frame period register 2.	0x00
SPDIFIN_Pc_INFO_1	0xFA13_0050	R	Specifies the SPDIFIN PC info register 1.	0x00

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Register	Address	R/W	Description	Reset Value
SPDIFIN_Pc_INFO_2	0xFA13_0054	R	Specifies the SPDIFIN PC info register 2.	0x00
SPDIFIN_Pd_INFO_1	0xFA13_0058	R	Specifies the SPDIFIN PD info register 1.	0x00
SPDIFIN_Pd_INFO_2	0xFA13_005C	R	Specifies the SPDIFIN PD Info Register 2.	0x00
SPDIFIN_DATA_BUF_0_1	0xFA13_0060	R	Specifies the SPDIFIN data buffer register 0_1.	0x00
SPDIFIN_DATA_BUF_0_2	0xFA13_0064	R	Specifies the SPDIFIN data buffer register 0_2.	0x00
SPDIFIN_DATA_BUF_0_3	0xFA13_0068	R	Specifies the SPDIFIN data buffer register 0_3.	0x00
SPDIFIN_USER_BUF_0	0xFA13_006C	R	Specifies the SPDIFIN user buffer register 0.	0x00
SPDIFIN_DATA_BUF_1_1	0xFA13_0070	R	Specifies the SPDIFIN data buffer register 1_1.	0x00
SPDIFIN_DATA_BUF_1_2	0xFA13_0074	R	Specifies the SPDIFIN data buffer register 1_2.	0x00
SPDIFIN_DATA_BUF_1_3	0xFA13_0078	R	Specifies the SPDIFIN data buffer register 1_3.	0x00
SPDIFIN_USER_BUF_1	0xFA13_007C	R	Specifies the SPDIFIN user buffer register 1.	0x00
I2S Registers				
I2S_CLK_CON	0xFA14_0000	R/W	Specifies the I2S clock enable register.	0x00
I2S_CON_1	0xFA14_0004	R/W	Specifies the I2S control register 1.	0x00
I2S_CON_2	0xFA14_0008	R/W	Specifies the I2S control register 2.	0x16
I2S_PIN_SEL_0	0xFA14_000C	R/W	Specifies the I2S input pin selection register 0.	0x77
I2S_PIN_SEL_1	0xFA14_0010	R/W	Specifies the I2S input pin selection register 1.	0x77
I2S_PIN_SEL_2	0xFA14_0014	R/W	Specifies the I2S input pin selection register 2.	0x77
I2S_PIN_SEL_3	0xFA14_0018	R/W	Specifies the I2S input pin selection register 3.	0x07
I2S_DSD_CON	0xFA14_001C	R/W	Specifies the I2S DSD control register.	0x02
I2S_IN_MUX_CON	0xFA14_0020	R/W	Specifies the I2S In/ Mux control register.	0x60
I2S_CH_ST_CON	0xFA14_0024	R/W	Specifies the I2S channel status control register.	0x00
I2S_CH_ST_0	0xFA14_0028	R/W	Specifies the I2S channel status block 0.	0x00
I2S_CH_ST_1	0xFA14_002C	R/W	Specifies the I2S channel status block 1.	0x00
I2S_CH_ST_2	0xFA14_0030	R/W	Specifies the I2S channel status block 2.	0x00

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Register	Address	R/W	Description	Reset Value
I2S_CH_ST_3	0xFA14_0034	R/W	Specifies the I2S channel status block 3.	0x00
I2S_CH_ST_4	0xFA14_0038	R/W	Specifies the I2S channel status block 4.	0x00
I2S_CH_ST_SH_0	0xFA14_003C	R	Specifies the I2S channel status block shadow register 0.	0x00
I2S_CH_ST_SH_1	0xFA14_0040	R	Specifies the I2S channel status block shadow register 1.	0x00
I2S_CH_ST_SH_2	0xFA14_0044	R	Specifies the I2S channel status block shadow register 2.	0x00
I2S_CH_ST_SH_3	0xFA14_0048	R	Specifies the I2S channel status block shadow register 3.	0x00
I2S_CH_ST_SH_4	0xFA14_004C	R	Specifies the I2S channel status block shadow register 4.	0x00
I2S_VD_DATA	0xFA14_0050	R/W	Specifies the I2S audio sample validity register.	0x00
I2S_MUX_CH	0xFA14_0054	R/W	Specifies the I2S channel enable register.	0x03
I2S_MUX_CUV	0xFA14_0058	R/W	Specifies the I2S CUV enable register.	0x03
I2S_IRQ_MASK	0xFA14_005C	R/W	Specifies the I2S interrupt request mask register.	0x00
I2S_IRQ_STATUS	0xFA14_0060	R/W	Specifies the I2S interrupt request status register.	0x00
I2S_CH0_L_0	0xFA14_0064	R	Specifies the I2S PCM output data register.	0x00
I2S_CH0_L_1	0xFA14_0068	R	Specifies the I2S PCM output data register.	0x00
I2S_CH0_L_2	0xFA14_006C	R	Specifies the I2S PCM output data register.	0x00
I2S_CH0_L_3	0xFA14_0070	R	Specifies the I2S PCM output data register.	0x00
I2S_CH0_R_0	0xFA14_0074	R	Specifies the I2S PCM output data register.	0x00
I2S_CH0_R_1	0xFA14_0078	R	Specifies the I2S PCM output data register.	0x00
I2S_CH0_R_2	0xFA14_007C	R	Specifies the I2S PCM output data register.	0x00
I2S_CH0_R_3	0xFA14_0080	R	Specifies the I2S PCM output data register.	0x00
I2S_CH1_L_0	0xFA14_0084	R	Specifies the I2S PCM output data register.	0x00
I2S_CH1_L_1	0xFA14_0088	R	Specifies the I2S PCM output data register.	0x00
I2S_CH1_L_2	0xFA14_008C	R	Specifies the I2S PCM output data register.	0x00
I2S_CH1_L_3	0xFA14_0090	R	Specifies the I2S PCM output data register.	0x00
I2S_CH1_R_0	0xFA14_0094	R	Specifies the I2S PCM output data register.	0x00
I2S_CH1_R_1	0xFA14_0098	R	Specifies the I2S PCM output data register.	0x00
I2S_CH1_R_2	0xFA14_009C	R	Specifies the I2S PCM output data register.	0x00
I2S_CH1_R_3	0xFA14_00A0	R	Specifies the I2S PCM output data register.	0x00
I2S_CH2_L_0	0xFA14_00A4	R	Specifies the I2S PCM output data register.	0x00
I2S_CH2_L_1	0xFA14_00A8	R	Specifies the I2S PCM output data register.	0x00
I2S_CH2_L_2	0xFA14_00AC	R	Specifies the I2S PCM output data register.	0x00

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Register	Address	R/W	Description	Reset Value
I2S_CH2_L_3	0xFA14_00B0	R	Specifies the I2S PCM output data register.	0x00
I2S_CH2_R_0	0xFA14_00B4	R	Specifies the I2S PCM output data register.	0x00
I2S_CH2_R_1	0xFA14_00B8	R	Specifies the I2S PCM output data register.	0x00
I2S_CH2_R_2	0xFA14_00BC	R	Specifies the I2S PCM output data register.	0x00
I2S_Ch2_R_3	0xFA14_00C0	R	Specifies the I2S PCM output data register.	0x00
I2S_CH3_L_0	0xFA14_00C4	R	Specifies the I2S PCM output data register.	0x00
I2S_CH3_L_1	0xFA14_00C8	R	Specifies the I2S PCM output data register.	0x00
I2S_CH3_L_2	0xFA14_00CC	R	Specifies the I2S PCM output data register.	0x00
I2S_CH3_R_0	0xFA14_00D0	R	Specifies the I2S PCM output data register.	0x00
I2S_CH3_R_1	0xFA14_00D4	R	Specifies the I2S PCM output data register.	0x00
I2S_CH3_R_2	0xFA14_00D8	R	Specifies the I2S PCM output data register.	0x00
I2S_CUV_L_R	0xFA14_00DC	R	Specifies the I2S CUV output data register.	0x00
Timing Generator Registers (TG Configure/Status Registers)				
TG_CMD	0xFA15_0000	R/W	Specifies the command register.	0x00
TG_H_FSZ_L	0xFA15_0018	R/W	Specifies the horizontal full size.	0x72
TG_H_FSZ_H	0xFA15_001C	R/W	Specifies the horizontal full size.	0x06
TG_HACT_ST_L	0xFA15_0020	R/W	Specifies the horizontal active start.	0x05
TG_ HACT_ST_H	0xFA15_0024	R/W	Specifies the horizontal active start.	0x01
TG_ HACT_SZ_L	0xFA15_0028	R/W	Specifies the horizontal active size.	0x00
TG_ HACT_SZ_H	0xFA15_002C	R/W	Specifies the horizontal active size.	0x05
TG_V_FSZ_L	0xFA15_0030	R/W	Specifies the vertical full line size.	0xEE
TG_V_FSZ_H	0xFA15_0034	R/W	Specifies the vertical full line size.	0x02
TG_VSYNC_L	0xFA15_0038	R/W	Specifies the vertical sync position.	0x01
TG_VSYNC_H	0xFA15_003C	R/W	Specifies the vertical sync position.	0x00
TG_VSYNC2_L	0xFA15_0040	R/W	Specifies the vertical sync position for bottom field.	0x33
TG_VSYNC2_H	0xFA15_0044	R/W	Specifies the vertical sync position for bottom field.	0x02
TG_VACT_ST_L	0xFA15_0048	R/W	Specifies the vertical sync active start position.	0x1a
TG_VACT_ST_H	0xFA15_004C	R/W	Specifies the vertical sync active start position.	0x00
TG_VACT_SZ_L	0xFA15_0050	R/W	Specifies the vertical active size.	0xd0
TG_VACT_SZ_H	0xFA15_0054	R/W	Specifies the vertical active size.	0x02
TG_FIELD_CHG_L	0xFA15_0058	R/W	Specifies the HDMI field change position.	0x33
TG_FIELD_CHG_H	0xFA15_005C	R/W	Specifies the HDMI field change position.	0x02
TG_VACT_ST2_L	0xFA15_0060	R/W	Specifies the HDMI vertical active start position for bottom field.	0x48

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Register	Address	R/W	Description	Reset Value
TG_VACT_ST2_H	0xFA15_0064	R/W	Specifies the HDMI vertical active start position for bottom field.	0x02
TG_VSYNC_TOP_HDMI_L	0xFA15_0078	R/W	Specifies the HDMI VSYNC position for top field.	0x01
TG_VSYNC_TOP_HDMI_H	0xFA15_007C	R/W	Specifies the HDMI VSYNC position for top field.	0x00
TG_VSYNC_BOT_HDMI_L	0xFA15_0080	R/W	Specifies the HDMI VSYNC position for bottom field.	0x01
TG_VSYNC_BOT_HDMI_H	0xFA15_0084	R/W	Specifies the HDMI VSYNC position for bottom field.	0x00
TG_FIELD_TOP_HDMI_L	0xFA15_0088	R/W	Specifies the HDMI top field start position.	0x01
TG_FIELD_TOP_HDMI_H	0xFA15_008C	R/W	Specifies the HDMI top field start position.	0x00
TG_FIELD_BOT_HDMI_L	0xFA15_0090	R/W	Specifies the HDMI bottom field start position.	0X33
TG_FIELD_BOT_HDMI_H	0xFA15_0094	R/W	Specifies the HDMI bottom field start position.	0x02
MHL_HSYNC_WIDTH	0xFA15_017C	R/W	Specifies the HSYNC width configuration.	0x0F
MHL_VSYNC_WIDTH	0xFA15_0180	R/W	Specifies the VSYNC width configuration.	0x01
MHL_CLK_INV	0xFA15_0184	R/W	Specifies the MHL clock-out inversion.	0x00

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10.3.2 CONTROL REGISTER

10.3.2.1 Control Register (INTC_CON, R/W, Address = 0xFA10_0000)

INTC_CON	Bit	Description	Initial State
IntrPol	[7]	Specifies the interrupt polarity. 0 = Active high 1 = Active low	0
IntrEnGlobal	[6]	0 = Disables all interrupts 1 = Enables or disables interrupts by INTC_CON5:0]	0
IntrEnI2S	[5]	Enables I2S interrupt. 0 = Disables 1 = Enables	0
IntrEnCEC	[4]	Enables CEC interrupt. 0 = Disables 1 = Enables	0
IntrEnHPDplug	[3]	Enables HPD plugged interrupt. 0 = Disables 1 = Enables	0
IntrEnHPDunplug	[2]	Enables HPD unplugged interrupt. 0 = Disables 1 = Enables	0
IntrEnSPDIF	[1]	Enables SPDIF interrupt. 0 = Disables 1 = Enables	0
IntrEnHDCP	[0]	Enables HDCP interrupt. 0 = Disables 1 = Enables	0

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10.3.2.2 Control Register (INTC_FLAG, R/W, Address = 0xFA10_0004)

INTC_FLAG	Bit	Description	Initial State
-	[7:6]	Reserved	2b00
IntrI2S	[5]	Specifies the I2S interrupt flag (read only). 0 = Interrupt does not occur 1 = Interrupt occurs	0
IntrCEC	[4]	Specifies the CEC interrupt flag (read only). 0 = Interrupt does not occur 1 = Interrupt occurs	0
IntrHPDplug	[3]	Specifies the HPD plugged interrupt flag. If it is written by 1, it is cleared. 0 = Interrupt does not occur 1 = HPD plugged interrupt occurs	0
IntrHPDunplug	[2]	Specifies the HPD unplugged interrupt flag. If it is written by 1, it is cleared. 0 = Interrupt does not occur 1 = HPD unplugged interrupt occurs	0
IntrSPDIF	[1]	Specifies the SPDIF interrupt flag (read only). 0 = Interrupt does not occur 1 = Interrupt occurs	0
IntrHDCP	[0]	Specifies the HDCP interrupt flag (read only). 0 = Interrupt does not occur 1 = Interrupt occurs	0

10.3.2.3 Control Register (HDCP_KEY_LOAD_DONE, R, Address = 0xFA10_0008)

HDCP_KEY_LOAD_DONE	Bit	Description	Initial State
-	[7:1]	Reserved	7b0000000
HDCP_KEY_LOAD_DONE	[0]	Loads the HDCP key from e-fuse. 0 = Not available 1 = Completes loading HDCP key from e-fuse	0

10.3.2.4 Control Register (HPD_STATUS, R, Address = 0xFA10_000C)

HPD_STATUS	Bit	Description	Initial State
-	[7:1]	Reserved	0x00
HPD_Value	[0]	Specifies the value of HPD signal. 0 = Unplugged 1 = Plugged	0

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10.3.2.5 Control Register (AUDIO_CLKSEL, R/W, Address = 0xFA10_0010)

AUDIO_CLKSEL	Bit	Description	Initial State
-	[7:1]	Reserved	0x00
AUDIO_CLK	[0]	Specifies the clock selection of Audio system (Must be higher than 512*fs). 0 = PCLK 1 = SPDIF clock Note: For audio data capture, the frequency of audio clock is higher than 512*fs[Hz]. If the frequency of audio clock is less than 512fs[Hz], audio data may be missed. Thus, if the frequency of PCLK is below 512fs[Hz], select SPDIF clock after it makes the frequency of SPDIF clock be higher than 512fs[Hz].	0

10.3.2.6 Control Register (HDMI_PHY_RSTOUT, R/W, Address = 0xFA10_0014)

PHY_RSTOUT	Bit	Description	Initial State
-	[7:1]	Reserved	0x00
RSTOUT	[0]	Specifies the HDMI PHY Software Reset out (active high). 0 = Normal 1 = Reset	0

10.3.2.7 Control Register (HDMI_PHY_VPLL, R, Address = 0xFA10_0018)

PHY_VPLL	Bit	Description	Initial State
VPLL_LOCK	[7]	Specifies the HDMI PHY VPLL Locking.	0x0
-	[6:4]	Reserved	0x0
VPLL_CODE	[3:0]	Specifies the HDMI PHY VPLL Code.	0x0

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10.3.2.8 Control Register (HDMI_PHY_CMU, R, Address = 0xFA10_001C)

PHY_CMU	Bit	Description	Initial State
CMU_LOCK	[7]	Specifies the HDMI PHY CMU Locking.	0x0
-	[6:4]	Reserved	0x0
CMU_CODE	[3:0]	Specifies the HDMI PHY CMU Code.	0x0

10.3.2.9 Control Register (HDMI_CORE_RSTOUT, R/W, Address = 0xFA10_0020)

CORE_RSTOUT	Bit	Description	Initial State
-	[7:1]	Reserved	0x00
RSTOUT	[0]	Specifies the HDMI TX core software reset out (active low). 1 = Normal 0 = Reset	0x1

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10.3.3 HDMI CORE REGISTER

10.3.3.1 Control Registers (HDMI_CON_0, R/W, Address = 0xFA11_0000)

HDMI_CON_0	Bit	Description	Initial State
MHL_CLK_En	[7]	Controls the MHL interface clock. 0 = Disables 1 = Enables	0
MHL_En	[6]	Enables the MHL interface. 0 = Disables 1 = Enables	0
Blue_Scr_En	[5]	Enables blue screen mode. When set, the input video pixels are discarded and blue screen register values are transmitted for all video data period. 0 = Disables 1 = Enables	0
Encoding_Option	[4]	Specifies the 10-bit TMDS encoding bit order option. 0 = Reverses the bit order during 10-bit encoding (to be set to 1 when connecting to TMDS PHY 1.3) 1 = Retains the bit order as is	0
-	[3]	Reserved	0
Asp_E	[2]	Generates audio sample packet. This bit is only valid when SYSTEM_EN is set. 0 = Discards audio sample 1 = Generates audio sample packet after receiving the audio sample	0
-	[1]	Reserved	0
System_En	[0]	Enables HDMI system. 0 = No op 1 = Enables HDMI	0

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10.3.3.2 Control Registers (HDMI_CON_1, R/W, Address = 0xFA11_0004)

HDMI_CON_1	Bit	Description	Initial State
-	[7]	Reserved	0
Pxl_Lmt_Ctrl	[6:5]	Controls the pixel value limitation. 2b00 = By-pass (Does not limit the pixel value) 2b01 = RGB mode Every channel's video input pixels are limited based on YMAX and YMIN register values. 2b10 = YCbCr mode The value of I_VIDEO_G is limited based on YMAX and YMIN register values. The values of I_VIDEO_B and I_VIDEO_R are limited based on CMAX and CMIN register values. 2b11 = Reserved	3b00
-	[4:2]	Reserved	3b000
-	[1:0]	Reserved	0

10.3.3.3 Control Registers (HDMI_CON_2, R/W, Address = 0xFA11_0008)

HDMI_CON_2	Bit	Description	Initial State
-	[7:6]	Reserved	3b00
Vid_Period_En	[5]	Controls the video preamble. 0 = Video preamble is applied (HDMI mode) 1 = Video preamble is not applied (DVI mode)	0
-	[4:2]	Reserved	3b000
Dvi_ Band_En	[1]	In DIV mode, the leading guard band is not used. 0 = Guard band is applied (HDMI mode) 1 = Guard band is not applied (DVI mode)	0
-	[0]	Reserved	0

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10.3.3.4 Control Registers (STATUS, S/W, Address = 0xFA11_0010)

STATUS	Bit	Description	Initial State
Authen_Ack	[7]	When HDCP is authenticated, this read-only bit occurs. It keeps the authentication signal without interruption. It is not cleared at all. This bit specifies just one delayed signal of authen_ack from HDCP block. It is not an interrupt source. 0 = Not authenticated 1 = Authenticated	0
Aud_Fifo_Ovf	[6]	If audio FIFO overflows, this bit is set. Once set, it should be cleared by the host. 0 = Not full 1 = Full	0
	[5]	Reserved	0
Update_Ri_Int	[4]	Specifies the Ri interrupt status bit. If it is written by 1, it is cleared. 0 = Interrupt does not occur 1 = Interrupt occurs	0
-	[3]	Reserved	0
An_Write_Int	[2]	Indicates that {An} random value is ready. If it is written by 1, it is cleared. 0 = Interrupt does not occur 1 = Interrupt occurs	0
Watchdog_Int	[1]	Indicates that the 2nd part of HDCP authentication protocol is initiated, and CPU should set a watchdog timer to check 5 seconds interval. If it is written by 1, it is cleared. 0 = Interrupt does not occur 1 = Interrupt occurs	0
I2c_Init_Int	[0]	Indicates that the 1st part of HDCP authentication protocol can start. If it is written by 1, it is cleared. 0 = Interrupt does not occur 1 = Interrupt occurs	0

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10.3.3.5 Control Registers (PHY_STATUS, R, Address = 0xFA11_0014)

PHY_STATUS	Bit	Description	Initial State
-	[7:1]	Reserved	7b0000000
Phy_Ready	[0]	Indicates that PHY is ready to receive the HDMI signals from link. 0 = Not Ready 1 = Ready	0

10.3.3.6 Control Registers (STATUS_EN, R/W, Address = 0xFA11_0020)

STATUS_EN	Bit	Description	Initial State
-	[7]	Reserved	0
Aud_Fido_Ovf_Ee	[6]	Enables audio buffer overflow interrupt. If it is set to '1', interrupt assertion is written on status registers. 0 = Disables 1 = Enables	0
-	[5]	Reserved	0
Update_Ri_Int_En	[4]	Enables UPDATE_RI_INT interrupt. 0 = Disables 1 = Enables	0
-	[3]	Reserved	0
An_Write_Int_En	[2]	Enables AN_WRITE_INT interrupt. 0 = Disables 1 = Enables	0
Watchdog_Int_En	[1]	Enables WATCHDOG_INT interrupt. 0 = Disables 1 = Enables	0
I2c_Int_En	[0]	Enables I2C_INT interrupt. 0 = Disables 1 = Enables	0

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10.3.3.7 Control Registers (HPD, R/W, Address = 0xFA11_0030)

HPD	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
Sw_Hpd	[1]	If HPD_SEL bit is set, this SW_HPD signal is used for HPD (HDMI/ DVI cable plugging). However, if this bit is set to low during HDMI transmission, status machines in HDCP core are reset. Note that other HDCP register values are not influenced. 0 = Low (unplugged) 1 = High (plugged)	0
Hpd_Sel	[0]	It this bit is cleared, the I_HPD signal from the I/O port is used for HPD. If set, the SW_HPD signal is used for HPD. 0 = HPD signal 1 = SW_HPD internal HPD signal	0

NOTE: If ENC_EN (0xFA11_0044) is disabled (not using HDCP), HPD must be controlled by S/W. If you don't use S/W control, it is possible that HDMI core works abnormally.

10.3.3.8 Control Registers (MODE_SEL, R/W, Address = 0xFA11_0040)

MODE_SEL	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
Hdmi_Mode	[1]	Selects a mode. 0 = Disables 1 = Enables	0
Dvi_Mode	[0]	Selects a mode. 0 = Disables 1 = Enables	0

* DVI mode gets a higher priority than HDMI.

10.3.3.9 Control Registers (ENC_EN, R/W, Address = 0xFA11_0044)

ENC_EN	Bit	Description	Initial State
-	[7:1]	Reserved	7b0000000
Hdcp_Enc_En	[0]	If this bit is set, the HDCP encryption is applied. Before setting this bit, the HDCP authentication process has to be completed. 0 = Encryption disables 1 = Encryption enables	0

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10.3.3.10 Video Related Register (BLUESCREEN_0/1/2)

- BLUESCREEN_0, R/W, Address = 0xFA11_0050
- BLUE_SCREEN_1, R/W, Address = 0xFA11_0054
- BLUE_SCREEN_2, R/W, Address = 0xFA11_0058

BLUESCREEN_0/1/2	Bit	Description	Initial State
BLUESCREEN_0	[7:0]	Specifies the Channel 0 color setting (Cb or B).	0x0
BLUESCREEN_1	[7:0]	Specifies the Channel 1 color setting (Y or G).	0x0
BLUESCREEN_2	[7:0]	Specifies the Channel 2 color setting (Cr or R).	0x0

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10.3.3.11 Video Related Register (HDMI_YMAX / HDMI_YMIN / HDMI_CMAX / HDMI_CMIN)

- HDMI_YMAX, R/W, Address = 0xFA11_0060
- HDMI_YMIN, R/W, Address = 0xFA11_0064
- HDMI_CMAX, R/W, Address = 0xFA11_0068
- HDMI_CMIN, R/W, Address = 0xFA11_006C

(HDMI_YMAX / HDMI_YMIN / HDMI_CMAX / HDMI_CMIN	Bit	Description	Initial State

HDMI_YMAX
HDMI_YMIN
HDMI_CMAX
HDMI_CMIN
	[7:0]
	[7:0]
	[7:0]
	[7:0]
		These registers are used based upon the PX_LMT_CTRL bits in HDMI_CON_1 register.
		
		For RGB mode
		if (i_video_x > HDMI_YMAX x 16)
		output = HDMI_YMAX x 16
		else if (i_video_x < HDMI_YMIN x 16)
		output = HDMI_YMIN x 16
		else output = i_video_x
		
		For YCbCr mode, the Y input is dealt in a similar way as shown above.
		
		For Cb and Cr values,
		if (i_video_x > HDMI_CMAX x 16)
		output = HDMI_CMAX x 16
		else if (i_video_x < HDMI_CMIN x 16)
		output = HDMI_CMIN x 16
		else output = i_video_x
		
		Note: The value 16 in each line compensates the difference of bit width between the input pixel and register value.
			0xEB
			0x10
			0xF0
			0x10

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10.3.3.12 Video Related Register (H_BLANK_0/1)

- H_BLANK_0, R/W, Address = 0xFA11_00A0
- H_BLANK_1, R/W, Address = 0xFA11_00A4

H_BLANK_0/1	Bit	Description	Initial State
-	[15:10]	Reserved	6b000000
H_BLANK	[9:0]	Specifies the clock cycles of horizontal blanking size. For more details on H_BLANK, refer to “Reference CEA-861D”.	0x000

60Hz	720x480p	1280x720p	1920x1080i	1920x1080p
H_BLANK	138(8Ah)	370(172h)	280(118h)	280(118h)
50Hz	**720x576p**	**1280x720p**	**1920x1080i**	**1920x1080p**
H_BLANK	144(90h)	700(2bch)	720(2d0h)	720(2d0h)

NOTE: 1080p is 25/29.97/30Hz.

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10.3.3.13 Video Related Register (V_BLANK_0/1/2)

- V_BLANK_0, R/W, Address = 0xFA11_00B0
- V_BLANK_1, R/W, Address = 0xFA11_00B4
- V_BLANK_2, R/W, Address = 0xFA11_00B8

V_BLANK_0/1/2	Bit	Description	Initial State
-	[23:22]	Reserved	0x0
V1_BLANK	[21:11]	Specifies the vertical blanking line size (front part). For more details on V1_BLANK, refer to “Reference CEA-861D”.	0x000
V2_BLANK	[10:0]	Specifies V1_BLANK+Active Lines (end part). This value is the same as V_LINE value for progressive mode. For interlace mode, use the reference value as mentioned in the table below. For more details on V2_BLANK, refer to “CEA-861D”.	0x000

60Hz	720x480p	1280x720p	1920x1080i	1920x1080p
V2_BLANK	525(d)	750(d)	562(d)	1125(d)
V1_BLANK	45(d)	30(d)	22(d)	45(d)
V_BLANK	16a0d(h)	f2ee(h)	b232(h)	1_6c65(h)
50Hz	**720x576p**	**1280x720p**	**1920x1080i**	**1920x1080p**
V2_BLANK	625(d)	750(d)	562(d)	1125(d)
V1_BLANK	49(d)	30(d)	22(d)	45(d)
V_BLANK	18a71(h)	F2ee(h)	B232(h)	1_6c65(h)

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10.3.3.14 Video Related Register (H_V_LINE_0/1/2)

- H_V_LINE_0, R/W, Address = 0xFA11_00C0
- H_V_LINE_1, R/W, Address = 0xFA11_00C4
- H_V_LINE_2, R/W, Address = 0xFA11_00C8

H_V_LINE_0/1/2	Bit	Description	Initial State
H_LINE	[23:12]	Specifies the horizontal line length. For more details on H_LINE, refer to “Reference CEA-861D”.	0x000
V_LINE	[11:0]	Specifies the vertical line length. For more details on V_LINE, refer to “Reference CEA-861D”.	0x000

60Hz	720x480p	1280x720p	1920x1080i	1920x1080p
V_LINE	525(d)	750(d)	1125(d)	1125(d)
H_LINE	858(d)	1650(d)	2200(d)	2200(d)
H_V_LINE	35a20d(h)	6722ee(h)	898465(h)	898465(h)
50Hz	**720x576p**	**1280x720p**	**1920x1080i**	**1920x1080p**
V_LINE	625(d)	750(d)	1125(d)	1125(d)
H_LINE	864(d)	1980(d)	2640(d)	2640(d)
H_V_LINE	360271(h)	7bc2ee(h)	a50465(h)	a50465(h)

10.3.3.15 Video Related Register (VSYNC_POL, R/W, Address = 0xFA11_00E4)

VSYNC_POL	Bit	Description	Initial State
-	[7:1]	Reserved	0x00
V_Sync_Pol_Sel	[0]	Specifies the start point detection polarity selection bit. The sync shapes for 720p or 1080i are different from 480p and 576p. They have inverted shapes. 0 = Active high 1 = Active low	0

50/ 60 Hz	720x480p	720x576p	1280x720p	1920x1080i	1920x1080p
VSYNC_POL	1	1	0	0	0

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10.3.3.16 Video Related Register (INT_PRO_MODE, R/W, Address = 0xFA11_00E8)

INT_PRO_MODE	Bit	Description	Initial State
-	[7:1]	Reserved	7b0000000
INT_PRO_MODE	[0]	Selects the interlaced or progressive mode. For more details on INT_PRO_MODE, refer to “Reference CEA-861D”. 0 = progressive 1 = interlaced	0

10.3.3.17 Video Related Register (V_BLANK_F_0/1/2)

- V_BLANK_F_0, R/W, Address = 0xFA11_0110
- V_BLANK_F_1, R/W, Address = 0xFA11_0114
- V_BLANK_F_2, R/W, Address = 0xFA11_0118

V_BLANK_F_0/1/2	Bit	Description	Initial State
-	[23:22]	Reserved	0x0
V_BOT_END	[21:11]	In the interlace mode, v_blank length of even and odd field is different. This register specifies the end position of bottom field’s active region. For more details on V_BOT_END, refer to “Reference CEA-861D”.	0x000
V_BOT_ST	[10:0]	Specifies the start position of bottom field’s active region. This value is the same as V_LINE value for interlace mode. For progressive mode, this value is not used. For more details on V_BOT_ST, refer to “Reference CEA-861D”.	0x000

* The above register only affects the interlace mode.

50/ 60 Hz	720x480p	720x576p	1280x720p	1920x1080i	1920x1080p
V_BOT_ST V_BOT_END V_BLANK_F	Don’t care	Don’t care	Don’t care	585(d) 1125(d) 232a49(h)	Don’t care

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10.3.3.18 Video Related Register (H_SYNC_GEN_0/1/2)

- H_SYNC_GEN_0, R/W, Address = 0xFA11_0120
- H_SYNC_GEN_1, R/W, Address = 0xFA11_0124
- H_SYNC_GEN_2, R/W, Address = 0xFA11_0128

H_SYNC_GEN_0/1/2	Bit	Description	Initial State
-	[23:21]	Reserved	0x0
Hsync_Pol	[20]	Inverts the generated signal to meet the modes. In 720p and 1080i modes, you don't need to invert the signal. Other modes need to be inverted. For more details on Hsync_Pol, refer to "Reference CEA-861D". 0 = Active high 1 = Active low	0
Hsync_Edn	[19:10]	Sets the end point of H sync. For more details on Hsync_Edn, refer to "Reference CEA-861D".	0x000
Hsync_Start	[9:0]	Sets the start point of H sync. For more details on Hsync_Start, refer to "Reference CEA-861D".	0x000

60Hz	720x480p	1280x720p	1920x1080i	1920x1080p
HSYNC_START	14(d)	108(d)	86(d)	86(d)
HSYNC_END	76(d)	148(d)	130(d)	130(d)
HSYNC_POL	1	0	0	0
H_SYNC_GEN	11300e(h)	2506c(h)	20856(h)	20856(h)
50Hz	**720x576p**	**1280x720p**	**1920x1080i**	**1920x1080p**
HSYNC_START	10(d)	438(d)	526(d)	526(d)
HSYNC_END	74(d)	478(d)	570(d)	570(d)
HSYNC_POL	1	0	0	0
H_SYNC_GEN	11280a(h)	779b6(h)	8ea0e(h)	8ea0e(h)

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10.3.3.19 Video Related Register (V_SYNC_GEN1_0/1/2)

Progressive mode only has one v_sync, whereas interlace mode has two. This register is used for generating first v_sync in both cases.

- V_SYNC_GEN1_0, R/W, Address = 0xFA11_0130
- V_SYNC_GEN1_1, R/W, Address = 0xFA11_0134
- V_SYNC_GEN1_2, R/W, Address = 0xFA11_0138

V_SYNC_GEN1_0/1/2	Bit	Description	Initial State
Vsync_T_St	[23:12]	Specifies the top field (or frame) V sync start line number. For more details on Vsync_T_St, refer to “Reference CEA-861D”.	0x001
Vsync_T_End	[11:0]	Specifies the top field (or frame) V sync end line number. For more details on Vsync_T_End, refer to “Reference CEA-861D”.	0x001

50/ 60 Hz	720x480p	720x576p	1280x720p	1920x1080i	1920x1080p
VSYNC_T_END	15(d)	10(d)	10(d)	7(d)	9(d)
VSYNC_T_ST	9(d)	5(d)	5(d)	2(d)	4(d)
V_SYNC_GEN1	900f(h)	500a(h)	500a(h)	2007(h)	4009(h)

10.3.3.20 Video Related Register (V_SYNC_GEN2_0/1/2)

Progressive mode only has one v_sync, whereas interlace mode has two. This register is used for generating second v_sync of interlace case.

- V_SYNC_GEN2_0, R/W, Address = 0xFA11_0140
- V_SYNC_GEN2_1, R/W, Address = 0xFA11_0144
- V_SYNC_GEN2_2, R/W, Address = 0xFA11_0148

V_SYNC_GEN2_0/1/2	Bit	Description	Initial State
Vsync_B_St	[23:12]	Specifies the bottom field V sync start line number. For more details on Vsync_B_St, refer to “Reference CEA-861D”.	0x001
Vsync_B_End	[11:0]	Specifies the bottom field V sync end line number. For more details on Vsync_B_End, refer to “Reference CEA-861D”.	0x001

50/ 60 Hz	1920x1080i	Other cases
VSYNC_B_END	569(d)	Don’t care
VSYNC_B_ST	564(d)	
V_SYNC_GEN2	234239(h)	

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10.3.3.21 Video Related Register (V_SYNC_GEN3_0/1/2)

Progressive mode has only one v_sync, whereas interlace mode has two. This register is used for generating second v_sync of interlace case.

- V_SYNC_GEN3_0, R/W, Address = 0xFA11_0150
- V_SYNC_GEN3_1, R/W, Address = 0xFA11_0154
- V_SYNC_GEN3_2, R/W, Address = 0xFA11_0158

V_SYNC_GEN3_0/1/2	Bit	Description	Initial State
Vsync_H_Pos_St	[23:12]	Specifies the bottom field V sync start transition point. For more details on Vsync_H_Pos_St, refer to “Reference CEA-861D”.	0x001
Vsync_H_Pos_End	[11:0]	Specifies the bottom field V sync end transition point. For more details on Vsync_H_Pos_End, refer to “Reference CEA-861D”.	0x001

60 Hz	1920x1080i	Other cases
VSYNC_H_POS_ST VSYNC_H_POS_END V_SYNC_GEN3	1188(d) 1188(d) 4A44A4(h)	Don’t care
50 Hz	**1920x1080i**	**Other cases**
VSYNC_H_POS_ST VSYNC_H_POS_END V_SYNC_GEN3	1848(d) 1848(d) 738738(h)	Don’t care

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10.3.3.22 Audio Related Packet Register (ASP_CON, R/W, Address = 0xFA11_0160)

ASP_CON	Bit	Description	Initial State
DST_Double	[7]	Specifies the DST double.	0
Aud_Type	[6:5]	Specifies the packet type instead of audio type. 00 = Audio Sample Packet 01 = One-bit audio packet 10 = HBR packet 11 = DST packet	2b00
Aud_Mode	[4]	Selects the two channel or multi-channel mode. This bit is also used for layout bit in ASP header. 0 = Two channel mode 1 = Multi-channel mode Set this bit to transmit HBR packets.	0
SP_Pre	[3:0]	Controls sub-packet usage for multi-channel mode only. When using two channel mode, this register value is not used. [0]: AUDIO0 control (0: disable, 1: enable) [1]: AUDIO1 control (0: disable, 1: enable) [2]: AUDIO2 control (0: disable, 1: enable) [3]: AUDIO3 control (0: disable, 1: enable)	4b0000

10.3.3.23 Audio Related Packet Register (ASP_SP_FLAT, R/W, Address = 0xFA11_0164)

ASP_SP_FLAT	Bit	Description	Initial State
-	[7:4]	Reserved	4b0000
SP_Flat	[3:0]	Specifies the sp_flat or sample_invalid value for ASP header. For more information on SP_Flat, refer to the HDMI specification v1.3 (5.3.4 and 5.3.9).	0x0

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10.3.3.24 Audio Related Packet Register (ASP_CHCFG0/1/2/3)

- ASP_CHCFG0, R/W, Address = 0xFA11_0170
- ASP_CHCFG1, R/W, Address = 0xFA11_0174
- ASP_CHCFG2, R/W, Address = 0xFA11_0178
- ASP_CHCFG3, R/W, Address = 0xFA11_017C

ASP_CHCFG0/1/2/3	Bit	Description	Initial State
-	[31:30]	Reserved	2b00
Spk3R_Sel	[29:27]	Selects the audio channel for subpacket 3 right channel data in multi-channel mode. 000 = i_pcm0L is used for sub packet 3 left channel 001 = i_pcm0R is used for sub packet 3 right channel 010 = i_pcm1L is used for sub packet 3 left channel 011 = i_pcm1R is used for sub packet 3 right channel 100 = i_pcm2L is used for sub packet 3 left channel 101 = i_pcm2R is used for sub packet 3 right channel 110 = i_pcm3L is used for sub packet 3 left channel 111 = i_pcm3R is used for sub packet 3 right channel	3b111
Spk3L_Sel	[26:24]	Selects the audio channel for subpacket 3 left channel data in multi-channel mode. The meaning is the same as SPK3R_SEL.	3b110
-	[23:22]	Reserved	2b00
Spk2R_Sel	[21:19]	Selects the audio channel for subpacket 2 right channel data in multi-channel mode. The meaning is the same as SPK2R_SEL.	3b101
Spk2L_Sel	[18:16]	Selects the audio channel selection for subpacket 2 left channel data in multi-channel mode. The meaning is the same as SPK2R_SEL.	3b100
-	[15:14]	Reserved	2b00
SPK1R_SEL	[13:11]	Selects the audio channel for subpacket 1 right channel data in multi-channel mode. The meaning is the same as SPK1R_SEL.	3b011
Spk1L_Sel	[10:8]	Selects the audio channel for subpacket 1 left channel data in multi-channel mode. The meaning is the same as SPK1R_SEL.	3b010
-	[7:6]	Reserved	2b00
Spk0R_Sel	[5:3]	Selects the audio channel for subpacket 0 right channel data in multi-channel mode. The meaning is the same as SPK0R_SEL.	3b001
Spk0L_Sel	[2:0]	Selects the audio channel selection for subpacket 0 left channel data in multi-channel mode. The meaning is the same as SPK0R_SEL.	3b000

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10.3.3.25 Audio Related Packet Register (ACR_CON, R/W, Address = 0xFA11_0180)

ACR_CON	Bit	Description	Initial State
-	[7:5]	Reserved	3b000
Alt_Cts_Rate	[4:3]	In some audio formats, the CTS value can be changed alternately. CTS value 1 = ACR_CTS[19:0] CTS value 2 = {ARC_CTS[19:8], ACR_LSB2} These two values can be transmitted alternately at the ratio of this register setting. 00 = Always CTS value 1 01 = 1:1 (CTS value 1: CTS value2) 10 = 2:1 (CTS value 1: CTS value2) 11 = 3:1 (CTS value 1: CTS value2) Measured CTS mode, this value is not used.	2b00
ACR_Tx_Mode	[2:0]	000 = Does not transfer (Tx) the ACR packet. 001 = Tx once – Transmits ACR packet once; anytime available after this value is set. After transmitting, these bits are reset to all zero. 010 = Tx ACR_TXCNT times during every VBI period 011 = Tx by counting i_clk_vid for a given CTS value in the ACR_CTS0~2 registers. 100 = Measured CTS mode. Makes ACR packet with CTS value by counting TMDS clock for Fs x 128 / N duration. In this case, the 7 LSBs of N value (ACR_N register) should be all zero.	3b000

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10.3.3.26 Audio Related Packet Register (ACR_MCTS0/1/2)

- ACR_MCTS0, R, Address = 0xFA11_0184
- ACR_MCTS1, R, Address = 0xFA11_0188
- ACR_MCTS2, R, Address = 0xFA11_018C

ACR_MCTS0/1/2	Bit	Description	Initial State
-	[23:20]	Reserved	0x0
ACR_MCTS	[19:0]	Specifies the TMDS clock cycles for N[19:7] number of audio sample inputs. Only valid when measured CTS mode is set on ACR_CON register.	0x00001

10.3.3.27 Audio Related Packet Register (ACR_CTS0/1/2)

- ACR_CTS0, R/W, Address = 0xFA11_0190
- ACR_CTS1, R/W, Address = 0xFA11_0194
- ACR_CTS2, R/W, Address = 0xFA11_0198

ACR_CTS0/1/2	Bit	Description	Initial State
-	[23:20]	Reserved	0x0
ACR_CTS	[19:0]	Specifies the CTS value for transmission mode other than ‘measured CTS’ mode.	0x0003E8

10.3.3.28 Audio Related Packet Register (ACR_N0/1/2)

- ACR_N0, R/W, Address = 0xFA11_01A0
- ACR_N1, R/W, Address = 0xFA11_01A4
- ACR_N2, R/W, Address = 0xFA11_01A8

ACR_N0/1/2	Bit	Description	Initial State
-	[23:20]	Reserved	0
ACR_N	[19:0]	Specifies the N value in ACR packet.	0x003E8

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10.3.3.29 Audio Related Packet Register (ACR_LSB2, R/W, Address = 0xFA11_01B0)

ACR_LSB2	Bit	Description	Initial State
ACR_LSB2	[7:0]	Specifies the alternate CTS least significant byte. For more information, see ALT_CTS_RATE in ACR_CON register.	0x00

10.3.3.30 Audio Related Packet Register (ACR_TXCNT, R/W, Address = 0xFA11_01B4)

ACR_TXCNT	Bit	Description	Initial State
-	[7:5]	Reserved	0
ACR_TXCNT	[4:0]	If ACR_TX_MODE is '10', the ACR packet will be transmitted 'ACR_TXCNT + 1' times per VBI period. ALT_CTS_RATE is also applied. This register is only valid if ACR_TX_MODE is '10'.	0x1F

10.3.3.31 Audio Related Packet Register (ACR_TXINTERVAL, R/W, Address = 0xFA11_01B8)

ACR_TXINTERVAL	Bit	Description	Initial State
ACR_TX_INTERVAL	[7:0]	If ACR_TX_MODE is '10', the ACR packet will be transmitted ACR_TXCNT times during VBI. This register specifies the number of cycles between each ACR packets and avoids continuous transmission in more than 18 packets within single DI band. It is only valid if ACR_TX_MODE is '10'.	0x63

10.3.3.32 Audio Related Packet Register (ACR_CTS_OFFSET, R/W, Address = 0xFA11_01BC)

ACR_CTS_OFFSET	Bit	Description	Initial State
ACR_CTS_OFFSET	[7:0]	If 'measured CTS mode' is used, the CTS value will be measured by counting the TMDS clock for a given duration. This value is added to measured CTS value. It is 8-bit signed integer, so subtraction is possible.	0x00

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10.3.3.33 Audio Related Packet Register (GCP_CON, R/W, Address = 0xFA11_01C0)

GCP_CON	Bit	Description	Initial State
-	[7:3]	Reserved	5b00000
ENABLE_1st_VSYNC	[3]	For interlace mode, enable this bit to transfer the GCP packet on the 1st VSYNC in a frame. 0 = Does not transfer GCP packet 1 = Transfers the GCP packet On the other hand, for progressive mode, GCP packet is transferred regardless of this bit, that is, GCP packet in progressive mode is transferred every vsync if GCP_CON is 2b1x.	1b0
ENABLE_2nd_VSYNC	[2]	For interlace mode, enable this bit to transfer the GCP packet on the 2nd VSYNC in a frame. 0 = Does not transfer GCP packet 1 = Transfers GCP packet	1b1
GCP_CON	[1:0]	00 = Does not transmit 01 = Transmits once 1x = Transmits every vsync Transmits GCP packet within 384 cycles after active vsync.	2b00

10.3.3.34 Audio Related Packet Register (GCP_BYTE1, R/W, Address = 0xFA11_01D0)

GCP_BYTE1	Bit	Description	Initial State
GCP_BYTE1	[7:0]	Specifies the GCP packet's first data byte. It is either 0x10 (Clear AVMUTE) or 0x01 (Set AVMUTE). For more information, refer to Table 5-17 of HDMI specification.	0x00

10.3.3.35 Audio Related Packet Register (GCP_BYTE2, R/W, Address = 0xFA11_01D4)

GCP_BYTE2	Bit	Description	Initial State
PP	[7:4]	Specifies the Packing Phase (PP). This bit is read only.	0x0
CD	[3:0]	Only supports 24bit mode. 0100 : 24 bit Ohters : Reserved	0x0

10.3.3.36 Audio Related Packet Register (GCP_BYTE3, R/W, Address = 0xFA11_01D8)

GCP_BYTE3	Bit	Description	Initial State
-	[7:1]	Reserved	7b0000000
GCP_BYTE3	[0]	Specifies the default state.	0

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10.3.3.37 ACP Packet Register (ACP_CON, R/W, Address = 0xFA11_01E0)

ACP_CON	Bit	Description	Initial State
ACP_FR_RATE	[7:3]	Transmits the ACP packet once per every ACP_FR_RATE+1 frames (or fields).	5b00000
-	[2]	Reserved	0
ACP_TX_CON	[1:0]	00 = Does not transmit 01 = Transmits once 1x = Transmits every vsync with ACP_FR_RATE	2b00

10.3.3.38 ACP Packet Register (ACP_TYPE, R/W, Address = 0xFA11_01F0)

ACP_TYPE	Bit	Description	Initial State
ACP_TYPE	[7:0]	Specifies the HB1 of ACP packet header. For more information, see Table 5-18 in HDMI v1.3 specification.	0x00

10.3.3.39 ACP Packet Register (ACP_DATA00~16)

- ACP_DATA00, R/W, Address = 0xFA11_0200
- ACP_DATA01, R/W, Address = 0xFA11_0204
- ACP_DATA02, R/W, Address = 0xFA11_0208
- ACP_DATA03, R/W, Address = 0xFA11_020C
- ACP_DATA04, R/W, Address = 0xFA11_0210
- ACP_DATA05, R/W, Address = 0xFA11_0214
- ACP_DATA06, R/W, Address = 0xFA11_0218
- ACP_DATA07, R/W, Address = 0xFA11_021C
- ACP_DATA08, R/W, Address = 0xFA11_0220
- ACP_DATA09, R/W, Address = 0xFA11_0224
- ACP_DATA10, R/W, Address = 0xFA11_0228
- ACP_DATA11, R/W, Address = 0xFA11_022C
- ACP_DATA12, R/W, Address = 0xFA11_0230
- ACP_DATA13, R/W, Address = 0xFA11_0234
- ACP_DATA14, R/W, Address = 0xFA11_0238
- ACP_DATA15, R/W, Address = 0xFA11_023C
- ACP_DATA16, R/W, Address = 0xFA11_0240

ACP_DATA00~16	Bit	Description	Initial State
ACP_DATA00~16	[7:0]	Specifies the ACP packet body data registers (PB0~PB16 of ACP packet body). For more information, see Section 9.3 in HDMI v1.3 specification.	0x00

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10.3.3.40 ISRC1/2 Packet Register (ISRC_CON, R/W, Address = 0xFA11_0250)

ISRC_CON	Bit	Description	Initial State
ISRC_FR_RATE	[7:3]	Transmits ISRC1 (with or without ISRC2) packet once every ISRC_FR_RATE+1 frames (or fields).	5b00000
ISRC2_EN	[2]	Transmits ISRC2 packet with ISRC1 packet.	0
ISRC_TX_CON	[1:0]	00 = Does not transmit 01 = Transmits once 1x = Transmits every vsync with ISRC_FR_RATE	2b00

10.3.3.41 ISRC1/2 Packet Register (ISRC1_HEADER1, R/W, Address = 0xFA11_0264)

ISRC1_HEADER1	Bit	Description	Initial State
ISRC_Cont	[7]	See Table 5-20 in HDMI v1.3specification.	0
ISRC_Valid	[6]	See Table 5-20 in HDMI v1.3 specification.	0
-	[5:3]	Reserved	3b000
ISRC status	[2:0]	See Table 5-20 in HDMI v1.3 specification.	3b000

10.3.3.42 ISRC1/2 Packet Register (ISRC1_DATA 00~15)

- ISRC1_DATA 00, R/W, Address = 0xFA11_0270
- ISRC1_DATA 01, R/W, Address = 0xFA11_0274
- ISRC1_DATA 02, R/W, Address = 0xFA11_0278
- ISRC1_DATA 03, R/W, Address = 0xFA11_027C
- ISRC1_DATA 04, R/W, Address = 0xFA11_0280
- ISRC1_DATA 05, R/W, Address = 0xFA11_0284
- ISRC1_DATA 06, R/W, Address = 0xFA11_0288
- ISRC1_DATA 07, R/W, Address = 0xFA11_028C
- ISRC1_DATA 08, R/W, Address = 0xFA11_0290
- ISRC1_DATA 09, R/W, Address = 0xFA11_0294
- ISRC1_DATA 10, R/W, Address = 0xFA11_0298
- ISRC1_DATA 11, R/W, Address = 0xFA11_029C
- ISRC1_DATA 12, R/W, Address = 0xFA11_02A0
- ISRC1_DATA 13, R/W, Address = 0xFA11_02A4
- ISRC1_DATA 14, R/W, Address = 0xFA11_02A8
- ISRC1_DATA 15, R/W, Address = 0xFA11_02AC

ISRC1_DATA 00~15	Bit	Description	Initial State
ISRC1_DATA00~15	[7:0]	Specifies the ISRC2 packet body data (PB0~15 of ISRC2 packet body). For more information, see Table 5-21 in HDMI v1.3 specification.	0x00

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10.3.3.43 ISRC1/2 Packet Register (ISRC2_DATA 00~15)

- ISRC2_DATA 00, R/W, Address = 0xFA11_02B0
- ISRC2_DATA 01, R/W, Address = 0xFA11_02B4
- ISRC2_DATA 02, R/W, Address = 0xFA11_02B8
- ISRC2_DATA 03, R/W, Address = 0xFA11_02B8
- ISRC2_DATA 04, R/W, Address = 0xFA11_02C0
- ISRC2_DATA 05, R/W, Address = 0xFA11_02C4
- ISRC2_DATA 06, R/W, Address = 0xFA11_02C8
- ISRC2_DATA 07, R/W, Address = 0xFA11_02CC
- ISRC2_DATA 08, R/W, Address = 0xFA11_02D0
- ISRC2_DATA 09, R/W, Address = 0xFA11_02D4
- ISRC2_DATA 10, R/W, Address = 0xFA11_02D8
- ISRC2_DATA 11, R/W, Address = 0xFA11_02DC
- ISRC2_DATA 12, R/W, Address = 0xFA11_02E0
- ISRC2_DATA 13, R/W, Address = 0xFA11_02E4
- ISRC2_DATA 14, R/W, Address = 0xFA11_02E8
- ISRC2_DATA 15, R/W, Address = 0xFA11_02EC

ISRC2_DATA 00~15	Bit	Description	Initial State
ISRC2_DATA00~15	[7:0]	Specifies the ISRC2 packet body data (PB0~15 of ISRC2 packet body). For more information, see Table 5-23 in HDMI v1.3 specification.	0x00

10.3.3.44 AVI InfoFrame Register (AVI_CON, R/W, Address = 0xFA11_0300)

AVI_CON	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
AVI_TX_CON	[1:0]	00 = Does not transmit 01 = Transmits once 1x = Transmits every vsync	2b00

10.3.3.45 AVI InfoFrame Register (AVI_CHECK_SUM, R/W, Address = 0xFA11_0310)

AVI_CHECK_SUM	Bit	Description	Initial State
AVI_CHECK_SUM	[7:0]	Specifies the AVI InfoFrame checksum byte (PB0 byte of AVI packet body).	0x00

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10.3.3.46 AVI InfoFrame Register (AVI_DATA01~13)

- AVI_DATA01, R/W, Address = 0xFA11_0320
- AVI_DATA02, R/W, Address = 0xFA11_0324
- AVI_DATA03, R/W, Address = 0xFA11_0328
- AVI_DATA04, R/W, Address = 0xFA11_032C
- AVI_DATA05, R/W, Address = 0xFA11_0330
- AVI_DATA06, R/W, Address = 0xFA11_0334
- AVI_DATA07, R/W, Address = 0xFA11_0338
- AVI_DATA08, R/W, Address = 0xFA11_033C
- AVI_DATA09, R/W, Address = 0xFA11_0340
- AVI_DATA10, R/W, Address = 0xFA11_0344
- AVI_DATA11, R/W, Address = 0xFA11_0348
- AVI_DATA12, R/W, Address = 0xFA11_034C
- AVI_DATA13, R/W, Address = 0xFA11_0350

AVI_DATA01~ AVI_DATA13	Bit	Description	Initial State
AVI_DATA01~ AVI_DATA13	[7:0]	Specifies the AVI Infoframe packet data registers (PB1~PB13 bytes of AVI packet body).	0x00

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10.3.3.47 Audio InfoFrame Register (AUI_CON, R/W, Address = 0xFA11_0360)

AUI_CON	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
AUI_TX_CON	[1:0]	00 = Does not transmit 01 = Transmits once 1x = Transmits every vsync	2b00

10.3.3.48 Audio InfoFrame Register (AUI_CHECK_SUM, R/W, Address = 0xFA11_0370)

AUI_CHECK_SUM	Bit	Description	Initial State
AUI_CHECK_SUM	[7:0]	Specifies the AUI checksum data (PB0 byte of AUI packet body).	0x00

10.3.3.49 Audio InfoFrame Register (AUI_DATA1~5)

- AUI_DATA1, R/W, Address = 0xFA11_0380
- AUI_DATA2, R/W, Address = 0xFA11_0384
- AUI_DATA3, R/W, Address = 0xFA11_0388
- AUI_DATA4, R/W, Address = 0xFA11_038C
- AUI_DATA5, R/W, Address = 0xFA11_0390

AUI_DATA1~AUI_DATA5	Bit	Description	Initial State
AUI_BYTE1 ~ AUI_BYTE5	[7:0]	Specifies the AUI packet body (PB1~PB5 bytes of AUI packet body). Note: AUI_BYTE5 is matched as: Write: AUI_BYTE5[7:3] Read: AUI_BYTE5[4:0]	0x00

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10.3.3.50 MPEG Source InfoFrame (MPG_CON, R/W, Address = 0xFA11_03A0)

MPG_CON	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
MPG_TX_CON	[1:0]	00 = Does not transmit 01 = Transmits once 1x = Transmits every vsync	2b00

10.3.3.51 MPEG Source InfoFrame (MPG_CHECK_SUM, R/W, Address = 0xFA11_03B0)

MPG_CHECK_SUM	Bit	Description	Initial State
MPG_CHECK_SUM	[7:0]	Specifies the MPG infoframe checksum register (PB0 byte of MPG packet body).	0x00

10.3.3.52 MPEG Source InfoFrame (MPG_DATA1~5)

- MPG_DATA1, R/W, Address = 0xFA11_03C0
- MPG_DATA2, R/W, Address = 0xFA11_03C4
- MPG_DATA3, R/W, Address = 0xFA11_03C8
- MPG_DATA4, R/W, Address = 0xFA11_03CC
- MPG_DATA5, R/W, Address = 0xFA11_03D0

MPG_DATA1~MPG_DATA5	Bit	Description	Initial State
MPG_DTAT1~ MPG_DATA5	[7:0]	Specifies the MPG Infoframe packet data (PB1~PB5 bytes of MPG packet body).	all zeros

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These registers can be used for Source Product Descriptor (SPD) packet transmission. Furthermore, they consist of full configurable header and packet body registers (3 bytes header register and 28 bytes packet body registers), so that they can be used for transmission of any type of packet.

10.3.3.53 Source Product Descriptor Infoframe (SPD_CON, R/W, Address = 0xFA11_0400)

SPD_CON	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
SPD_TX_CON	[1:0]	00 = Does not transmit 01 = Transmits once 1x = Transmits every vsync	2b00

10.3.3.54 Source Product Descriptor Infoframe (SPD_HEADER0/1/2)

- SPD_HEADER0, R/W, Address = 0xFA11_0410
- SPD_HEADER1, R/W, Address = 0xFA11_0414
- SPD_HEADER2, R/W, Address = 0xFA11_0418

SPD_HEADER0/1/2	Bit	Description	Initial State
SPD_HEADER0	[7:0]	Specifies the HB0 byte of SPD packet header.	0x00
SPD_HEADER1	[7:0]	Specifies the HB1 byte of SPD packet header.	0x00
PD_HEADER2	[7:0]	Specifies the HB2 byte of SPD packet header.	0x00

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10.3.3.55 Source Product Descriptor Infoframe (SPD_DATA00~27)

- SPD_DATA00, R/W, Address = 0xFA11_0420
- SPD_DATA01, R/W, Address = 0xFA11_0424
- SPD_DATA02, R/W, Address = 0xFA11_0428
- SPD_DATA03, R/W, Address = 0xFA11_042C
- SPD_DATA04, R/W, Address = 0xFA11_0430
- SPD_DATA05, R/W, Address = 0xFA11_0434
- SPD_DATA06, R/W, Address = 0xFA11_0438
- SPD_DATA07, R/W, Address = 0xFA11_043C
- SPD_DATA08, R/W, Address = 0xFA11_0440
- SPD_DATA09, R/W, Address = 0xFA11_0444
- SPD_DATA10, R/W, Address = 0xFA11_0448
- SPD_DATA11, R/W, Address = 0xFA11_044C
- SPD_DATA12, R/W, Address = 0xFA11_0450
- SPD_DATA13, R/W, Address = 0xFA11_0454
- SPD_DATA14, R/W, Address = 0xFA11_0458
- SPD_DATA15, R/W, Address = 0xFA11_045C
- SPD_DATA16, R/W, Address = 0xFA11_0460
- SPD_DATA17, R/W, Address = 0xFA11_0464
- SPD_DATA18, R/W, Address = 0xFA11_0468
- SPD_DATA19, R/W, Address = 0xFA11_046C
- SPD_DATA20, R/W, Address = 0xFA11_0470
- SPD_DATA21, R/W, Address = 0xFA11_0474
- SPD_DATA22, R/W, Address = 0xFA11_0478
- SPD_DATA23, R/W, Address = 0xFA11_047C
- SPD_DATA24, R/W, Address = 0xFA11_0480
- SPD_DATA25, R/W, Address = 0xFA11_0484
- SPD_DATA26, R/W, Address = 0xFA11_0488
- SPD_DATA27, R/W, Address = 0xFA11_048C

SPD_DATA00~27	Bit	Description	Initial State
SPD_DATA00 ~ SPD_DATA27	[7:0]	Specifies the SPD packet data registers (PB0~PB27 bytes).	0x00

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10.3.3.56 HDCP Register Description (HDCP_SHA1_00~19)

- HDCP_SHA1_00, R/W, Address = 0xFA11_0600
- HDCP_SHA1_01, R/W, Address = 0xFA11_0604
- HDCP_SHA1_02, R/W, Address = 0xFA11_0608
- HDCP_SHA1_03, R/W, Address = 0xFA11_060C
- HDCP_SHA1_04, R/W, Address = 0xFA11_0610
- HDCP_SHA1_05, R/W, Address = 0xFA11_0614
- HDCP_SHA1_06, R/W, Address = 0xFA11_0618
- HDCP_SHA1_07, R/W, Address = 0xFA11_061C
- HDCP_SHA1_08, R/W, Address = 0xFA11_0620
- HDCP_SHA1_09, R/W, Address = 0xFA11_0624
- HDCP_SHA1_10, R/W, Address = 0xFA11_0628
- HDCP_SHA1_11, R/W, Address = 0xFA11_062C
- HDCP_SHA1_12, R/W, Address = 0xFA11_0630
- HDCP_SHA1_13, R/W, Address = 0xFA11_0634
- HDCP_SHA1_14, R/W, Address = 0xFA11_0638
- HDCP_SHA1_15, R/W, Address = 0xFA11_063C
- HDCP_SHA1_16, R/W, Address = 0xFA11_0640
- HDCP_SHA1_17, R/W, Address = 0xFA11_0644
- HDCP_SHA1_18, R/W, Address = 0xFA11_0648
- HDCP_SHA1_19, R/W, Address = 0xFA11_064C

HDCP_SHA1_00~19	Bit	Description	Initial State
HDCP_SHA1	[159:0]	Specifies the SHA-1 value of 160-bit HDCP repeater (LSB first). These registers are readable but they are not modified by HDCP H/W.	All zeros

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10.3.3.57 HDCP Register Description (HDCP_SHA_RESULT, R/W, Address = 0xFA11_0670)

HDCP_SHA_RESULT	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
Hdcp_Sha_Valid_Ready	[1]	Indicates that the HW performed the SHA comparison. Must be cleared by SW by writing 0. 0 = Not ready 1 = Ready	0
Hdcp_Sha_Valid	[0]	Indicates that the SHA-1 comparison succeeds. Must be cleared by SW by writing 0. 0 = Valid 1 = Not valid	0

10.3.3.58 HDCP Register Description (HDCP_KSV_LIST_0~4)

- HDCP_KSV_LIST_0, R/W, Address = 0xFA11_0650
- HDCP_KSV_LIST_1, R/W, Address = 0xFA11_0654
- HDCP_KSV_LIST_2, R/W, Address = 0xFA11_0658
- HDCP_KSV_LIST_3, R/W, Address = 0xFA11_065C
- HDCP_KSV_LIST_4, R/W, Address = 0xFA11_0660

HDCP_KSV_LIST_0~4	Bit	Description	Initial State
HDCP_KSV_LIST	[39:0]	Specifies little endian addressing and one KSV value from the HDCP repeater's KSV list. These registers are readable.	All zeros

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10.3.3.59 HDCP Register Description (HDCP_KSV_LIST_CON, R/W, Address = 0xFA11_0664)

HDCP_KSV_LIST_CON	Bit	Description	Initial State
-	[7:4]	Reserved	4b0000
Hdcp_Ksv_Write_Done	[3]	After writing KSV data into HDCP_KSV_LIST_X registers and then writing “1” to this register, the HW processes the written KSV value and clears this bit to “0”. 0 = Does not write 1 = Writes KSV data into HDCP_KSV_LIST_X registers and then writes “1” to this register	0
Hdcp_Ksv_List_Empty	[2]	If the number of KSV list is zero, set this value to enable the SHA-1 module calculate without KSV list. 0 = Not empty 1 = Empty	0
Hdcp_Ksv_End	[1]	Indicates that current KSV value in HDCP_KSV_LIST_X registers is the last one. 0 = Not End 1 = End	0
Hdcp_Ksv_Read	[0]	After writing KSV data in HDCP_KSV_LIST_X registers, the HDCP SHA-1 module keeps the KSV value in internal buffer and sets this flag to ‘1’ for notifying it has been read. After setting the flag to ‘1’, the SW clears to ‘0’ at the same time when writing the HDCP_KSV_WRITE_DONE bit for next KSV list value. 0 = Not Read 1 = Read	1

10.3.3.60 HDCP Register Description (HDCP_CTRL1, R/W, Address = 0xFA11_0680)

HDCP_CTRL1	Bit	Description	Initial State
-	[7:4]	Reserved	4b0000
-	[3]	Reserved	0
Timeout	[2]	Sets if Rx is the repeater and its KSV list is not ready until five seconds. 0 = Not timeout 1 = Timeout (KSV Ready bit in the HDCP_BCAPS register is not high until five seconds) and re-starts the 1st authentication. Refer to Figure 2-6 in the HDCP 1.3 specification.	0
CP_Desired	[1]	Enables HDCP. 0 = Not Desired 1 = Desired	0
-	[0]	Reserved	0

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10.3.3.61 HDCP Register Description (HDCP_CTRL2, R/W, Address = 0xFA11_0684)

HDCP_CTRL2	Bit	Description	Initial State
-	[7:1]	Reserved	7b0000000
Revocation_Set	[0]	Specifies the KSV list that is on the revocation list. Setting this bit fails the 2nd authentication. 0 = Does not set revocation 1 = Sets revocation	0

10.3.3.62 HDCP Register Description (HDCP_CHECK_RESULT, R/W, Address = 0xFA11_0690)

HDCP_CHECK_RESULT	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
Ri_Match_Result	[1:0]	Writes the result of comparison between Ri of Rx and Tx as the following values: (Ri : Tx, Ri' : Rx) Must be cleared by SW after setting 10 or 11 before next Ri interrupt occurs. 0x = Don't care 10 = Ri ≠ Ri' 11 = Ri = Ri'	2b00

10.3.3.63 HDCP Register Description (HDCP_BKSV0~4)

- HDCP_BKSV0, R/W, Address = 0xFA11_06A0
- HDCP_BKSV1, R/W, Address = 0xFA11_06A4
- HDCP_BKSV2, R/W, Address = 0xFA11_06A8
- HDCP_BKSV3, R/W, Address = 0xFA11_06AC
- HDCP_BKSV4, R/W, Address = 0xFA11_06B0

HDCP_BKSV0~4	Bit	Description	Initial State
HDCP_BKSV	[39:0]	Specifies the key selection vector (KSV) value from the receiver.	All zeros

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10.3.3.64 HDCP Register Description (HDCP_AKSV0~4)

- HDCP_AKSV0, R, Address = 0xFA11_06C0
- HDCP_AKSV1, R, Address = 0xFA11_06C4
- HDCP_AKSV2, R, Address = 0xFA11_06C8
- HDCP_AKSV3, R, Address = 0xFA11_06CC
- HDCP_AKSV4, R, Address = 0xFA11_06D0

HDCP_AKSV0~4	Bit	Description	Initial State
HDCP_AKSV	[39:0]	Specifies the KSV value of transmitter.	All zeros

10.3.3.65 HDCP Register Description (HDCP_An_0~7)

- HDCP_An_0, R, Address = 0xFA11_06E0
- HDCP_An_1, R, Address = 0xFA11_06E4
- HDCP_An_2, R, Address = 0xFA11_06E8
- HDCP_An_3, R, Address = 0xFA11_06EC
- HDCP_An_4, R, Address = 0xFA11_06F0
- HDCP_An_5, R, Address = 0xFA11_06F4
- HDCP_An_6, R, Address = 0xFA11_06F8
- HDCP_An_7, R, Address = 0xFA11_06FC

HDCP_An_0~7	Bit	Description	Initial State
HDCP_An	[63:0]	Specifies the 64-bit random number generated by Tx (An).	All zeros

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10.3.3.66 HDCP Register Description (HDCP_BCAPS, R/W, Address = 0xFA11_0700)

HDCP_BCAPS	Bit	Description	Initial State
-	[7]	Reserved	0
Repeater	[6]	Specifies the receiver that supports downstream connections. 0 = Not Repeater 1 = Repeater	0
Ready	[5]	Indicates KSV FIFO, SHA-1 is calculation ready. 0 = Not Ready 1 = Ready	0
Fast	[4]	Specifies the receiver devices that support 400KHz transfer. 0 = Not Fast 1 = Fast	0
Reserved	[3:2]	Must be 0.	0
1.1_Features	[1]	Supports EESS, advance cipher, and enhanced link verification. 0 = Does not set 1 = Sets	0
Fast_Reauthentication	[0]	Specifies all HDMI receivers that are capable of reauthentication. 0 = Does not set 1 = Sets	0

10.3.3.67 HDCP Register Description (HDCP_BSTATUS_0/1)

- HDCP_BSTATUS_0, R/W, Address = 0xFA11_0710
- HDCP_BSTATUS_1, R/W, Address = 0xFA11_0714

HDCP_BSTATUS_0/1	Bit	Description	Initial State
-	[15:13]	Reserved	3b000
Hdmi_Mode	[12]	Specifies the HDMI mode. If set, HDCP works in HDMI mode.	0
Max_Cascade_Exceeded	[11]	Specifies the topology error.	0
Depth	[10:8]	Specifies the cascade depth.	3b000
Max_Devs_Exceeded	[7]	Indicates the topology error. 0 = No Error 1 = Error	0
Device_Count	[6:0]	Specifies the total number of attached downstream devices.	0

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10.3.3.68 HDCP Register Description (HDCP_Ri_0/1)

- HDCP_Ri_0, R, Address = 0xFA11_0740
- HDCP_Ri_1, R, Address = 0xFA11_0744

HDCP_Ri_0/1	Bit	Description	Initial State
HDCP_Ri	[15:0]	Specifies the HDCP Ri value of transmitter.	0x0000

10.3.3.69 HDCP Register Description (HDCP_I2C_INT, R/W, Address = 0xFA11_0780)

HDCP_I2C_INT	Bit	Description	Initial State
-	[7:1]	Reserved	7b0000000
HDCP_I2C_INT	[0]	Specifies the HDCP I2C interrupt status (active high). It indicates the start of I2C transaction if it is set. After active, it should be cleared by S/W by writing 0. 0 = Does not occur 1 = Occurs	0

10.3.3.70 HDCP Register Description (HDCP_AN_INT, R/W, Address = 0xFA11_0790)

HDCP_AN_INT	Bit	Description	Initial State
-	[7:1]	Reserved	7b0000000
HDCP_AN_INT	[0]	Specifies the HDCP An Interrupt status (active high). If An value is available, it is set. After active, it should be cleared by S/W by writing 0. 0 = Does not occur 1 = Occurs	0

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10.3.3.71 HDCP Register Description (HDCP_WATCHDOG_INT, R/W, Address = 0xFA11_07A0)

HDCP_WATCHDOG_INT	Bit	Description	Initial State
-	[7:1]	Reserved	7b0000000
HDCP_WATCHDOG_INT	[0]	Specifies the HDCP watchdog interrupt status (active high). If the repeater bit value is set after 1st authentication success, this bit is set. After active, it should be cleared by S/W by writing 0. 0 = Does not occur 1 = Occurs	0

10.3.3.72 HDCP Register Description (HDCP_RI_INT, R/W, Address = 0xFA11_07B0)

HDCP_RI_INT	Bit	Description	Initial State
-	[7:1]	Reserved	7b0000000
HDCP_Ri_INT	[0]	If Ri value is updated internally (at every 128 video frames), it is set to high. After set, it should be cleared by S/W by writing 0. 0 = Does not occur 1 = Occurs	0

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10.3.3.73 Ri Check Register (HDCP_Ri_Compare_0, R/W, Address = 0xFA11_07D0)

HDCP_Ri_Compare_0	Bit	Description	Initial State
Enable	[7]	Enables the interrupt for this frame number index.	1
Frame Number index	[6:0]	If the frame count reaches “frame number index”, an Ri link integrity check interrupt occurs.	7b0000000

10.3.3.74 Ri Check Register (HDCP_Ri_Compare_1, R/W, Address = 0xFA11_07D4)

HDCP_Ri_Compare_1	Bit	Description	Initial State
Enable	[7]	Enables the interrupt for this frame number index.	0
Frame Number index	[6:0]	If the frame count reaches “frame number index”, an Ri Link integrity check interrupt occurs.	7b1111111

10.3.3.75 Ri Check Register (HDCP_Frame_Count, R, Address = 0xFA11_07E0)

HDCP_Frame_Count	Bit	Description	Initial State
-	[7]	Reserved	0
Frame Count	[6:0]	Specifies the current value of frame count index in hardware.	7b0000000

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10.3.3.76 Gamut Metadata Packet Register (GAMUT_CON, R/W, Address = 0xFA11_0500)

GAMUT_CON	Bit	Description	Initial State
-	[7:2]	Reserved	6b00000
GAMUT_CON	[1:0]	00 = Does not transmit 01 = Transmits once 1x = Transmits every vsync	2b00

10.3.3.77 Gamut Metadata Packet Register (GAMUT_HEADER0, R/W, Address = 0xFA11_0504)

GAMUT_HEADER0	Bit	Description	Initial State
HB0	[7:0]	Specifies the HB0 value in Table 5-30. For more information, refer to HDMI 1.3 specification.	0x00

10.3.3.78 Gamut Metadata Packet Register (GAMUT_HEADER1, R/W, Address = 0xFA11_0508)

GAMUT_HEADER1	Bit	Description	Initial State
Next_Field	[7]	Indicates the effectiveness of GBD carried in this packet on the next video field.	0
GBD_profile	[6:4]	Specifies the transmission profile number (only profile 0 is supported).	3b000
Affected_Gamut_Seq_Num	[3:0]	Indicates which video fields are relevant for this metadata.	4b0000

10.3.3.79 Gamut Metadata Packet Register (GAMUT_HEADER2, R/W, Address = 0xFA11_050C)

GAMUT_HEADER2	Bit	Description	Initial State
No_Crnt_GBD	[7]	Indicates that there is no gamut metadata available for the currently transmitted video.	0
Reserved	[6]	Reserved	0
Packet_Seq	[5:4]	Indicates whether this packet is first, intermediate, last, or the only packet in a gamut metadata packet sequence.	2b00
Current_Gamut_Seq_Num	[3:0]	Indicates the gamut number of the currently transmitted video stream.	4b0000

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10.3.3.80 Gamut Metadata Packet Register (GAMUT_METADATA0~27)

- GAMUT_METADATA0, R/W, Address = 0xFA11_0510
- GAMUT_METADATA0, R/W, Address = 0xFA11_0514
- GAMUT_METADATA2, R/W, Address = 0xFA11_0518
- GAMUT_METADATA3, R/W, Address = 0xFA11_051C
- GAMUT_METADATA4, R/W, Address = 0xFA11_0520
- GAMUT_METADATA5, R/W, Address = 0xFA11_0524
- GAMUT_METADATA6, R/W, Address = 0xFA11_0528
- GAMUT_METADATA7, R/W, Address = 0xFA11_052C
- GAMUT_METADATA8, R/W, Address = 0xFA11_0530
- GAMUT_METADATA9, R/W, Address = 0xFA11_0534
- GAMUT_METADATA10, R/W, Address = 0xFA11_0538
- GAMUT_METADATA11, R/W, Address = 0xFA11_053C
- GAMUT_METADATA12, R/W, Address = 0xFA11_0540
- GAMUT_METADATA13, R/W, Address = 0xFA11_0544
- GAMUT_METADATA14, R/W, Address = 0xFA11_0548
- GAMUT_METADATA15, R/W, Address = 0xFA11_054C
- GAMUT_METADATA16, R/W, Address = 0xFA11_0550
- GAMUT_METADATA17, R/W, Address = 0xFA11_0554
- GAMUT_METADATA18, R/W, Address = 0xFA11_0558
- GAMUT_METADATA19, R/W, Address = 0xFA11_055C
- GAMUT_METADATA20, R/W, Address = 0xFA11_0560
- GAMUT_METADATA21, R/W, Address = 0xFA11_0564
- GAMUT_METADATA22, R/W, Address = 0xFA11_0568
- GAMUT_METADATA23, R/W, Address = 0xFA11_056C
- GAMUT_METADATA24, R/W, Address = 0xFA11_0570
- GAMUT_METADATA25, R/W, Address = 0xFA11_0574
- GAMUT_METADATA26, R/W, Address = 0xFA11_0578
- GAMUT_METADATA27, R/W, Address = 0xFA11_057C

GAMUT_METADATA	Bit	Description	Initial State
GAMUT_METADATA0~ GAMUT_METADATA27	[7:0]	Specifies the gamut metadata packet body for P0 transmission profile.	0x00

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10.3.3.81 Video Mode Register (VIDEO_PATTERN_GEN, R/W, Address = 0xFA11_05C4)

VIDEO_PATTERN_GEN	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
Ext_Video_En	[1]	0 = Ext off 1 = Ext on	0
Video Pattern Enable	[0]	0 = Disables 1 = Uses internally generated video pattern	0

10.3.3.82 Video Mode Register (HPD_GEN, R/W, Address = 0xFA11_05C8)

HPD_GEN	Bit	Description	Initial State
HPD_Duration	[7:0]	Specifies the number of cycles for determining stable HPD input. Internal count = TMDS clock * HPD_Duration * 16 (cycles) Default value = 0x1 (16 TMDS clock cycles)	0x01

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10.3.4 SPDIF REGISTER

10.3.4.1 SPDIF Register (SPDIFIN_CLK_CTRL, R/W, Address = 0xFA13_0000)

SPDIFIN_CLK_CTRL	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
ready_clk_down	[1]	0 = Enables clock 1 = Readies for disabling clock (default)	1
power_on	[0]	0 = Disables clock (default) 1 = Activates clock If this bit is reset, SPDIFIN stops checking the input signal just before the next 'subframe' of SPDIF signal format and waits for the 'acknowledge' signal from HDMI for unresolved previous 'request' towards HDMI. It then asserts 'ready_clk_down' as high. To initialize internal states, assert software reset, that is, SPDIFIN_OP_CTRL. op_ctrl=00b right after activating clock again.	0

The spdif_clk is gated by an external clock gating module for low-power. Disabling the clock should not cause stalling of HDMI data transfer. Therefore, the system processor requests disabling of the clock by setting the power_on register to low and the module acknowledges this request by setting the ready_clk_down register to high after a current transaction on the I2C bus, and HDMI is finished. The module must not commence a new bus transaction until the system processor sets the power_on register to high again.

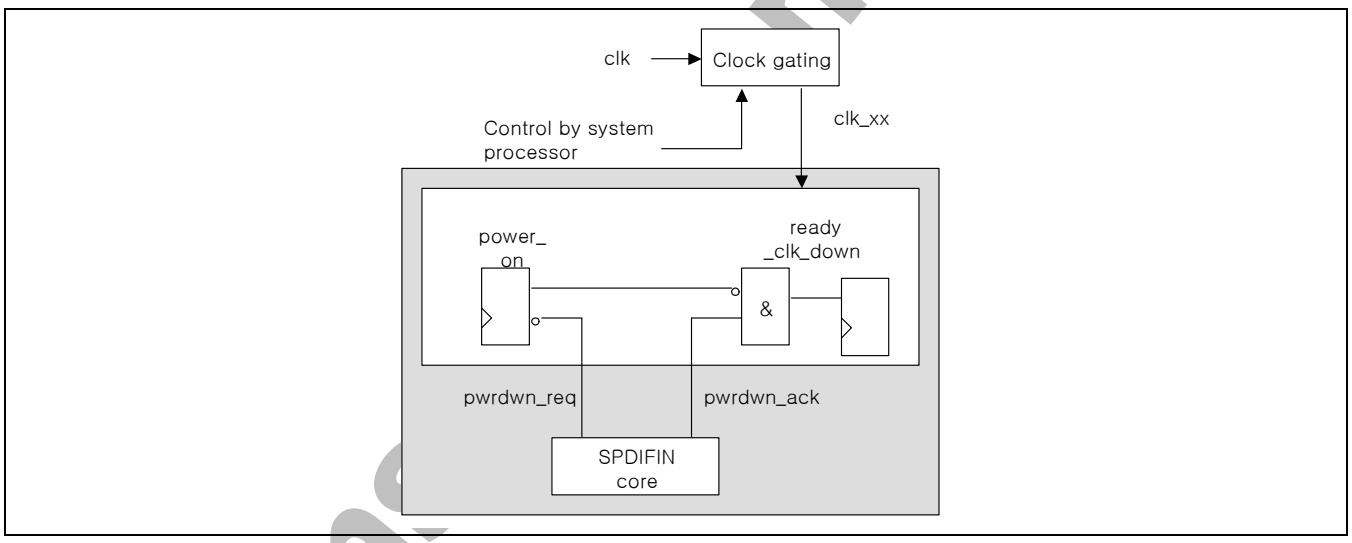

Figure 10-13 Structure of Power Down Circuit

The system processor switches off clk_xx when the ready_clk_down bit is one and the power_on bit is zero.

The system processor switches on the clock at any time. After having switched on clk_xx, the system processor sets the power_on bit to 1, which forces the ready_clk_down bit to zero.

Once the reset clock of SPDIFIN is switched off, the power_on bit is set to zero and the ready_clk_down bit is set to one.

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10.3.4.2 SPDIF Registers (SPDIFIN_OP_CTRL, R/W, Address = 0xFA13_0004)

SPDIFIN_OP_CTRL	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
op_ctrl	[1:0]	00b = Specifies the software reset 01b = Specifies the status checking mode (run) 11b = Specifies the status checking and HDMI operation modes (run with HDMI) Others = Undefined, do not use 00b = During a software reset, all state machines are set to the idle or init state and all internal registers are set to their initial values. Interrupt status registers are cleared, all other registers that are writable by the system processor keep their values. 01b = This command should be asserted after SPDIFIN_CLK_CTRL.power_on is set. SPDIFIN starts the clock recovery. When recovery is done, SPDIFIN detects preambles of SPDIF signal format and stream data header, abnormal time signal input, abnormal signal input, and also reports these status via interrupts in SPDIFIN_IRQ_STATUS. 11b = Specifies the “01b” case operations, checks internal buffer overflow, and writes received data, which can be either audio sample word of PCM or payload of stream. Data will be transferred via HDMI. - Assert ‘op_ctrl’=11b after SPDIFIN_IRQ_STATUS. ch_status_recovered_ir is asserted at least once for linear PCM data. - Assert ‘op_ctrl’=11b after SPDIFIN_IRQ_STATUS. stream_header_detected_ir is asserted at least once for non-linear PCM stream data.	0

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10.3.4.3 SPDIF Register (SPDIFIN_IRQ_MASK, R/W, Address = 0xFA13_0008)

SPDIFIN_IRQ_MASK	Bit	Description	Initial State
buf_overflow_ir_en	[7]	Specifies the mask bit for Interrupt 7.	0
-	[6]	Reserved	0
-	[5]	Reserved	0
stream_header_detected_ir_en	[4]	Specifies the mask bit for Interrupt 4.	0
stream_header_not_detected_ir_en	[3]	Specifies the mask bit for Interrupt 3.	0
wrong_preamble_ir_en	[2]	Specifies the mask bit for Interrupt 2.	0
ch_status_recovered_ir_en	[1]	Specifies the mask bit for Interrupt 1.	0
wrong_signal_ir_en	[0]	Specifies the mask bit for Interrupt 0.	0
For every bit: 0 = Disables interrupt generation 1 = Enables interrupt generation			

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10.3.4.4 SPDIF Register (SPDIFIN_IRQ_STATUS, R/W, Address = 0xFA13_000C)

SPDIFIN_IRQ_STATUS	Bit	Description	Initial State
buf_overflow_ir	[7]	0 = No interrupt 1 = Internal buffer overflow SPDIFIN internal buffer(s) (SPDIFIN_DATA_BUF_x) overflows if HDMI fails to transfer data from buffer(s) to memory on time. - This interrupt is asserted only if SPDIFIN_OP_CTRL.op_ctrl is set to “011”. - If this interrupt is not handled, SPDIFIN overwrites the next subframe data to internal data buffer (SPDIFIN_DATA_BUF_x) and continues data transfer via HDMI.	0
-	[6]	Reserved	0
-	[5]	Reserved	0
stream_header_detected_ir	[4]	0 = No interrupt 1 = Detects stream data header (Pa~Pd) - This interrupt is asserted if SPDIFIN_OP_CTRL.op_ctrl is equal to 001b or 011b. - Cases for interrupt Case1: Initially after power_on Case2: Next stream header at right time if receiving stream data with SPDIFIN_CONFIG.data_type set as ‘stream mode’ Case3: Initially detects stream header if receiving stream data with SPDIFIN_CONFIG.data_type is set as ‘PCM mode’	0
stream_header_not_detected_ir	[3]	0 = No interrupt 1 = Does not detect stream data header for 4096 repetition time - This interrupt will be asserted if SPDIFIN_OP_CTRL.op_ctrl is equal to 001b or 011b. - Cases for interrupt Case1: Initially after power_on Case2: SPDIFIN receives the stream but is unable to find the next stream header for 4096 repetition time since previous stream header Case3: Is unable to find stream header for 4096 repetition time since previous reset of repetition time counter after previous interrupt of ‘stream_header_not_detected_ir’.	0

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SPDIFIN_IRQ_STATUS	Bit	Description	Initial State
wrong_preamble_ir	[2]	0 = No interrupt 1 = Detects preamble but indicates a problem with the detected time - This interrupt is asserted when SPDIFIN_OP_CTRL.op_ctrl is equal to 001b or 011b. - Meaningless until ch_status_recovered_ir is asserted initially after SPDIFIN_OP_CTRL.op_ctrl=01b - Cases for interrupt Case1: Detects preamble in the middle of a subframe audio sample word time Case2: Does not detect the next preamble at exact time after a subframe duration Case3: Does not detect preamble B (or M or W) but detects other preamble at that time	0
ch_status_recovered_ir	[1]	0 = No interrupt 1 = Recovered channel status Detects two consecutive B-preambles; thus recovers 192-bit wide channel status. - Only supports consumer mode, so only 36-bits are reconstructed. If you want to see the channel status bits through SPDIFIN_CH_STATUS_x, read two consecutive 'ch_status_recovered_ir' and the register each time. If these two channel status values are the same, you can rely on that value.	0
wrong_signal_ir	[0]	0 = No interrupt 1 = Clock recovery fails Cannot recover the clock from input due to tolerable range violation (unlock), no signal from outside, or non-biphase in non-preamble duration. - Meaningless until ch_status_recovered_ir is asserted initially after SPDIFIN_OP_CTRL.op_ctrl=01b.	0
For every bit, the following holds: Reading returns interrupt request status. Writing '0' has no effect. Writing '1' clears the interrupt request.			
1) Detection of stream header Waits for matching of Pa, Pb and 0xF872, 0x4E1F respectively. Waits for repetition time (from decoded PC value or user-defined PC in SPDIFIN_USER_VALUE.repetition_time_manual, based on SPDIFIN_CONFIG. PcPd_value_mode) Check for matching of Pa, Pb on right time.			

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10.3.4.5 SPDIF Register (SPDIFIN_CONFIG_1, R/W, Address = 0xFA13_0010)

SPDIFIN_CONFIG_1	Bit	Description	Initial State
-	[7]	Reserved	0
noise_filter_samples	[6]	0 = Filtering with three consecutive samples 1 = Filtering with two consecutive samples Noise filtering is done for over-sampled SPDIF input signal. This operation will be done as follows: If 'noise_filter_samples' is 0, three consecutive over-sampled signals are regarded as high or low only if those samples are all high or all low respectively. If one or two samples are low or high for three over-sample duration, those noise-filtered signals will keep the previous value. If 'noise_filter_samples' is 1, two consecutive over-sampled signals are regarded as a high or low only if those samples are all high or low respectively. This setting can be used for reduced over-sampling ratio; recommended over-sampling ratio is 10 (see also 'clk_divisor').	0
-	[5]	Reserved (Must be '0')	0
PcPd_value_mode	[4]	0 = Automatically sets 1 = Manually sets If '0' is used for automatic setting, Pc and Pd values are chosen by value of Pc and Pd from decoded stream header, as reported in SPDIFIN_Px_INFO. If you set this register, the receiver will use SPDIFIN_USER_VALUE[31:16] and SPDIFIN_USER_VALUE[15:4] values as Pc and Pd respectively, instead of decoded data from stream header, as reported in SPDIFIN_Px_INFO. If the (cf) burst payload length is automatically or manually set, it affects the data size to be written in memory via HDMI—by dumping the full sub-frame for last bit in burst payload length. For example, if burst payload length is 257-bit, that is, 16 sub-frames * 16-bit + 1-bit, then HDMI will write data in 17 consecutive sub-frames.	0
word_length_value_ mode	[3]	0 = Automatically sets 1 = Manually sets If '0' is used for automatic setting, the word length value will be chosen by value of channel status from decoded SPDIF format, as reported in SPDIFIN_CH_STATUS_1.word_length. If user sets this register, the receiver will use SPDIFIN_USER_VALUE[3:0] value as word length instead of decoded data from channel status, as reported in SPDIFIN_CH_STATUS_1.word_length.	0

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SPDIFIN_CONFIG_1	Bit	Description	Initial State
U_V_C_P_report	[2]	0 = Neglects ‘user_bit’, ‘validity_bit’, ’channel status’, and ‘parity_bit’ of SPDIF format. 1 = Reports ‘user_bit’, ‘validity_bit’, ‘channel status’, and ‘parity_bit’ of SPDIF format The report will be delivered via HDMI for each sub-frame. Valid only if SPDIFIN_CONFIG. data_align is set for 32-bit mode. For more information, see SPDIFIN_DATA_BUF_x.	0
-	[1]	Reserved (Must be ‘1’)	1
data_align	[0]	0 = 16-bit mode 1 = 32-bit mode 16-bit: Only takes 16-bits from MSB in a sub-frame of SPDIF format, and then concatenates two consecutive 16-bit data in one 32-bit register of SPDIFIN_DATA_BUF_x. 32-bit: Only takes data from one subframe with zero padding to MSB part. For example, 0x00ffffff for 24-bit data. With stream mode, set ‘word_length_value_mode’ as 1 and set SPDIFIN_USER_VALUE.word_length_manual as 3b000. - These two modes will be applied to both modes of SPDIFIN_CONFIG.data_type, that is, PCM or stream. For more information, see SPDIFIN_DATA_BUF_x.	0

10.3.4.6 SPDIF Register (SPDIFIN_CONFIG_2, R/W, Address = 0xFA13_0014)

SPDIFIN_CONFIG_2	Bit	Description	Initial State
-	[7:4]	Reserved	0x0
clk_divisor	[3:0]	SPDIFIN_internal_clock = system_clock / (clk_divisor + 1) (SPDIFIN_internal_clock ≤ 135 Mhz) SPDIFIN over-samples the SPDIF input signal with internal clock that is divided from system clock. Recommended over-sampling ratio is 8~10, thus the following calculation holds: Recommended SPDIFIN_internal_clock = Sampling Frequency of SPDIF Input Signal * 64-bits * 10 times over-sampling For example, 48 kHz * 64-bits * 10 times over-sampling = 31 Mhz.	0x0

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10.3.4.7 SPDIF Register (SPDIFIN_USER_VALUE_1, R/W, Address = 0xFA13_0020)

SPDIFIN_USER_VALUE_1	Bit	Description	Initial State
repetition_time_manual_low	[7:4]	Specifies the repetition time[3:0]. Repetition_time_manual register has 12-bits value. This register is low by 4-bits. It counts one block of stream data and is valid only if SPDIFIN_CONFIG.PcPd_value_mode is set for manual mode. Unit: frames (1 frame = 2 sub-frames) of SPDIF format. The value should be actual repetition time minus one. For example, if you want to manually set the repetition time as 1536, you should write 1535.	0x0
word_length_manual	[3:0]	Specifies the word length. Used as size for transferring data to memory via HDMI; valid only when SPDIFIN_CONFIG.word_length_value_mode is set for manual mode. For more information, see SPDIFIN_DATA_BUF_x. [0] is 1 [0] is 0 [3:1] 101: 24-bits 20-bits 001: 23-bits 19-bits 010: 22-bits 18-bits 011: 21-bits 17-bits 100: 20-bits 16-bits	0x0

10.3.4.8 SPDIF Register (SPDIFIN_USER_VALUE_2, R/W, Address = 0xFA13_0024)

SPDIFIN_USER_VALUE_2	Bit	Description	Initial State
repetition_time_manual_high	[7:0]	Specifies the repetition time[11:4]. Repetition_time_manual register has 12-bits value. This register is high by 8-bits. Counts one block of stream data; valid only if SPDIFIN_CONFIG.PcPd_value_mode is set for manual mode. Unit: frames (1 frame = 2 sub-frames) of SPDIF format The value should be actual repetition time minus one. For example, if you want to manually set the repetition time as 1536, you should write 1535.	0x00

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10.3.4.9 SPDIF Register (SPDIFIN_USER_VALUE_3, R/W, Address = 0xFA13_0028)

SPDIFIN_USER_VALUE_3	Bit	Description	Initial State
burst_payload_length_manual_low	[7:0]	Specifies the burst_payload_length_manual[7:0]. Burst_payload_length register has 16-bits value. This register is low by 8-bits Valid only if SPDIFIN_CONFIG.PcPd_value_mode is set for manual mode. Unit: bits	0

10.3.4.10 SPDIF Register (SPDIFIN_USER_VALUE_4, R/W, Address = 0xFA13_002C)

SPDIFIN_USER_VALUE_4	Bit	Description	Initial State
burst_payload_length_manual_ high	[7:0]	Specifies the burst_payload_length_manual[15:8]. Burst_payload_length register has 16-bits value. This register is high by 8-bits. Valid only if SPDIFIN_CONFIG.PcPd_value_mode is set for manual mode. Unit: bits.	0

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The channel status registers are updated every 192 frames (1 block) of SPDIF format only for consumer mode.

10.3.4.11 Channel Status Register (SPDIFIN_CH_STATUS_0_1, R, Address = 0xFA13_0030)

SPDIFIN_CH_STATUS_0_1	Bit	Description	Initial State
channel_status_mode	[7:6]	00 = Mode 0 others = Reserved	2b00
emphasis	[5:3]	000 = Emphasis not indicated 100 = Emphasis – CD type	3b000
copyright_assertion	[2]	0 = Copyright 1 = No copyright	0
audio_sample_word	[1]	0 = Linear PCM 1 = Non-linear PCM	0
channel_status_block	[0]	0 = Consumer format 1 = Professional format	0
This register is updated every 192 frames (1 block) of SPDIF format. SPDIFIN_CH_STATUS_0_1 [7:0] is the matched internal register SPDIFIN_CH_STATUS_0 [7:0].			

10.3.4.12 Channel Status Register (SPDIFIN_CH_STATUS_0_2, R, Address = 0xFA13_0034)

SPDIFIN_CH_STATUS_0_2	Bit	Description	Initial State
category_code	[7:0]	Equipment type: [8:15] CD player: 1000_0000 DAT player: 1100_000L DCC player: 1100_001L Mini disc: 1001_001L (L: information about generation status of the material)	0x00

10.3.4.13 Channel Status Register (SPDIFIN_CH_STATUS_0_3, R, Address = 0xFA13_0038)

SPDIFIN_CH_STATUS_0_3	Bit	Description	Initial State
channel_number	[7:4]	Specifies the channel number (Bit 20 is LSB).	0x0
source_number	[3:0]	Specifies the source number (Bit 16 is LSB).	0x0

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10.3.4.14 Channel Status Register (SPDIFIN_CH_STATUS_0_4, R, Address = 0xFA13_003C)

SPDIFIN_CH_STATUS_0_4	Bit	Description	Initial State
-	[7:6]	Reserved	2b00
clock_accuracy	[5:4]	Specifies the clock accuracy. 00 = level II, ±1000ppm 01 = level I, ±50ppm 10 = level III, variable pitch shifted	2b00
sampling_frequency	[3:0]	Specifies the sampling frequency. 0100 = 22.05kHz 0000 = 44.1kHz 1000 = 88.2kHz 1100 = 176.4kHz 0110 = 24kHz 0010 = 48kHz 1010 = 96kHz 1110 = 192kHz 0011 = 32kHz	0x0

10.3.4.15 Channel Status Register (SPDIFIN_CH_STATUS_1, R, Address = 0xFA13_0040)

SPDIFIN_CH_STATUS_1	Bit	Description	Initial State
-	[7:4]	Reserved	0x0
word_length	[3:1]	Specifies the word length. (field_size = 1) (field_size = 0) 000 = not indicated not indicated 101 = 24-bits 20-bits 100 = 23-bits 19-bits 010 = 22-bits 18-bits 110 = 21-bits 17-bits 001 = 20-bits 16-bits	3b000
field_size	[0]	Specifies the field size. 0 = Maximum length 20-bits 1 = Maximum length 24-bits	0

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10.3.4.16 SPDIFIN Info Register (SPDIFIN_CH_STATUS_1, R, Address = 0xFA13_0048)

SPDIFIN_CH_STATUS_1	Bit	Description	Initial State
frame_cnt_low	[7:0]	Specifies the frame count value [7:0]. Frame_cnt register has 16-bits value. This is low by 8-bits. The period of a frame (two sub-frames) and register is updated every two sub-frames. It will be measured by 'SPDIFIN_internal_clk' made with SPDIFIN_CONFIG.clk_divisor. Unit: SPDIF_internal_clk cycles Recommended value for locking incoming signals: Over 0x220 (8.5timesx64-bits)	0x00

10.3.4.17 SPDIFIN Info Register (SPDIFIN_CH_STATUS_2, R, Address = 0xFA13_004C)

SPDIFIN_CH_STATUS_2	Bit	Description	Initial State
frame_cnt_high	[7:0]	Specifies the frame count value [15:8]. Frame_cnt register has 16-bits value. This is high by 8-bits. The period of a frame (two sub-frames) and register is updated every two sub-frames. It is measured by 'SPDIFIN_internal_clk' made with SPDIFIN_CONFIG.clk_divisor. Unit: SPDIF_internal_clk cycles Recommended value for locking incoming signals: Over 0x220 (8.5timesx64-bits)	0x0

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10.3.4.18 SPDIFIN Info Register (SPDIFIN_Pc_INFO_1, R, Address = 0xFA13_0050)

SPDIFIN_Pc_INFO_1	Bit	Description	Initial State
error_flag	[7]	0 = Valid burst payload 1 = Burst payload may contain errors	0
-	[6:5]	Reserved	2b00
compressed_data_type	[4:0]	0d = Null data 1d = Dolby AC-3 2d = Reserved 3d = Pause 4d = MPEG-1 layer 1 5d = MPEG-1 layer 2 or 3 or MPEG-2 w/o extension 6d = MPEG-2 w/ extension 7d = Reserved 8d = MPEG-2 layer 1 low sampling freq. 9d = MPEG-2 layer 2 or 3 low sampling freq. 10d = Reserved 11d, 12d, 13d = DTS 14d~31d = Reserved	5b00000

10.3.4.19 SPDIFIN Info Register (SPDIFIN_Pc_INFO_2, R, Address = 0xFA13_0054)

SPDIFIN_Pc_INFO_2	Bit	Description	Initial State
bit_stream_number	[7:5]	Specifies the bit stream number.	3b000
data_type_dependent_info	[4:0]	Specifies the data type dependent information.	5b00000

10.3.4.20 SPDIFIN Info Register (SPDIFIN_Pd_INFO_1, R, Address = 0xFA13_0058)

SPDIFIN_Pd_INFO_1	Bit	Description	Initial State
burst_payload_length_low	[7:0]	Specifies the length of burst payload [7:0] (Unit: bits).	0x00

10.3.4.21 SPDIFIN Info Register (SPDIFIN_Pd_INFO_2, R, Address = 0xFA13_005C)

SPDIFIN_Pd_INFO_2	Bit	Description	Initial State
burst_payload_length_high	[7:0]	Specifies the length of burst payload [15:8] (Unit: bits).	0x00

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10.3.4.22 SPDIFIN Info Register (SPDIFIN_DATA_BUF0_1/2/3)

- SPDIFIN_DATA_BUF_0_1, R, Address = 0xFA13_0060
- SPDIFIN_DATA_BUF_0_2, R, Address = 0xFA13_0064
- SPDIFIN_DATA_BUF_0_3, R, Address = 0xFA13_0068

SPDIFIN_DATA_BUF0_1/2/3	Bit	Description	Initial State
received_data_0_1 received_data_0_2 received_data_0_3	[7:0] [7:0] [7:0]	Specifies the PCM or stream data for 1st burst of HDMI. SPDIFIN_DATA_BUF_0_1 = SPDIFIN_DATA_BUF_0[7:0] SPDIFIN_DATA_BUF_0_2 = SPDIFIN_DATA_BUF_0[15:8] SPDIFIN_DATA_BUF_0_3 = SPDIFIN_DATA_BUF_0[23:16] If SPDIFIN_CONFIG.data_align is '0' for 16-bit, received_data is equal to {data_(N)th, data_(N+1)th}. If SPDIFIN_CONFIG.data_align is '1' for 32-bit, received_data is equal to {U, V, C, P, zero-padding, and data[n:0]}. If SPDIFIN_CONFIG.U_V_P_report is '0', received_data is equal to {zero-padding, data[n:0]}. , where, 'n' is dependent on SPDIFIN_CH_STATUS_1 and word_length if SPDIFIN_CONFIG. data_type is 0 for PCM. 'n' is equal to 15 if SPDIFIN_CONFIG.data_type is 1 for stream. If SPDIFIN_CONFIG.HDMI_burst_size is 1 burst, HDMI accesses only this data register.	0x00

10.3.4.23 SPDIFIN Info Register (SPDIFIN_USER_BUF_0, R, Address = 0xFA13_006C)

SPDIFIN_USER_BUF_0	Bit	Description	Initial State
received_data_user_0	[7:4]	Specifies the user bit of 1st burst of HDMI received_data[7:4] = SPDIFIN_DATA_BUF_0[31:28].	0x0
-	[3:0]	Reserved	0x0

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10.3.4.24 SPDIFIN Info Register (SPDIFIN_DATA_BUF1_1/2/3)

- SPDIFIN_DATA_BUF_1_1, R, Address = 0xFA13_0070
- SPDIFIN_DATA_BUF_1_2, R, Address = 0xFA13_0074
- SPDIFIN_DATA_BUF_1_3, R, Address = 0xFA13_0078

SPDIFIN_DATA_BUF1_1/2/3	Bit	Description	Initial State
received_data_data_1_1 received_data_data_1_2 received_data_data_1_3	[7:0] [7:0] [7:0]	Specifies the PCM or stream data for 2nd burst of HDMI. SPDIFIN_DATA_BUF_0_1 = SPDIFIN_DATA_BUF_0[7:0] SPDIFIN_DATA_BUF_0_2 = SPDIFIN_DATA_BUF_0[15:8] SPDIFIN_DATA_BUF_0_3 = SPDIFIN_DATA_BUF_0[23:16] If SPDIFIN_CONFIG.data_align is '0' for 16-bit, received_data is equal to {data_(N)th, data_(N+1)th}. If SPDIFIN_CONFIG.data_align is '1' for 32-bit, received_data is equal to {U, V, C, P, zero-padding, data[n:0]}. If SPDIFIN_CONFIG.U_V_P_report is '0', received_data is equal to {zero-padding, data[n:0]}. , where 'n' is dependent on SPDIFIN_CH_STATUS_1 and word_length if SPDIFIN_CONFIG. data_type is '0' for PCM. 'n' is equal to 15 if SPDIFIN_CONFIG.data_type is '1' for stream. If SPDIFIN_CONFIG.HDMI_burst_size is 1 burst, HDMI accesses only this data register.	0x00

10.3.4.25 SPDIFIN Info Register (SPDIFIN_USER_BUF_1, R, Address = 0xFA13_007C)

SPDIFIN_USER_BUF_1	Bit	Description	Initial State
received_data_user_1	[7:4]	Specifies the user bit of 2nd burst of HDMI received_data[7:4] = SPDIFIN_DATA_BUF_1[31:28]	0x0
-	[3:0]	Reserved	0x0

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10.3.5 I2S REGISTER

10.3.5.1 I2S Register (I2S_CLK_CON, R/W, Address = 0xFA14_0000)

I2S_CLK_CON	Bit	Description	Initial State
-	[7:1]	Reserved	0
i2s_en	[0]	Enables the I2S clock. 0 = I2S will be disabled (default) 1 = I2S will be activated Sets i2s_en after other registers are configured. If you want to reset the I2S, this register is 0 → 1.	0

10.3.5.2 I2S Register (I2S_CON_1, R/W, Address = 0xFA14_0004)

I2S_CON_1	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
r_sc_pol	[1]	Specifies the SDATA is synchronous to 0 = SCLK falling edge 1 = SCLK rising edge	0
r_ch_pol	[0]	Specifies the LRCLK polarity. 0 = Left channel for low polarity 1 = Left channel for high polarity	0

10.3.5.3 I2S Register (I2S_CON_2, R/W, Address = 0xFA14_0008)

I2S_CON_2	Bit	Description	Initial State
-	[7]	Reserved	0
mlsb	[6]	0 = MSB first mode 1 = LSB first mode	0
bit_ch	[5:4]	Specifies the bit clock per frame (Frame = left + right). 2b00 = 32fs 2b01 = 48fs 2b10 = Reserved	2b01
data_num	[3:2]	Specifies the serial data bit per channel. 2b01 = 16-bit 2b10 = 20-bit 2b11 = 24-bit	2b01
i2s_mode	[1:0]	2b00 = I2S basic format 2b10 = left justified format 2b11 = right justified format	2b10

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10.3.5.4 I2S Register (I2S_PIN_SEL_0, R/W, Address = 0xFA14_000C)

I2S_PIN_SEL_0	Bit	Description	Initial State
-	[7]	Reserved	0
pin_sel_1	[6:4]	Selects the SCLK (I2S). 3b111 = i_i2s_in[1] 3b110 = i_i2s_in[6] 3b101 = i_i2s_in[5] 3b100 = i_i2s_in[4] 3b011 = i_i2s_in[3] 3b010 = i_i2s_in[2] 3b001 = i_i2s_in[1] 3b000 = i_i2s_in[0] Note: SCLK is selected with i_i2s_in[5](0x101).	3b111
-	[3]	Reserved	0
pin_sel_0	[2:0]	Selects the LRCK (I2S). 3b111 = i_i2s_in[0] 3b110 = i_i2s_in[6] 3b101 = i_i2s_in[5] 3b100 = i_i2s_in[4] 3b011 = i_i2s_in[3] 3b010 = i_i2s_in[2] 3b001 = i_i2s_in[1] 3b000 = i_i2s_in[0] Note: LRCK is selected with i_i2s_in[6](0x110).	3b111

10.3.5.5 I2S Register (I2S_PIN_SEL_1, R/W, Address = 0xFA14_0010)

I2S_PIN_SEL_1	Bit	Description	Initial State
-	[7]	Reserved	0
pin_sel_3	[6:4]	Selects the SDATA_1 (I2S). 3b111 = i_i2s_in[3] 3b110 = i_i2s_in[6] 3b101 = i_i2s_in[5] 3b100 = i_i2s_in[4] 3b011 = i_i2s_in[3] 3b010 = i_i2s_in[2] 3b001 = i_i2s_in[1] 3b000 = i_i2s_in[0] Note: SDATA_1 is selected with i_i2s_in[3](0x011).	3b111
-	[3]	0	0
pin_sel_2	[2:0]	Selects the SDATA_0 (I2S). 3b111 = i_i2s_in[2] 3b110 = i_i2s_in[6] 3b101 = i_i2s_in[5] 3b100 = i_i2s_in[4] 3b011 = i_i2s_in[3] 3b010 = i_i2s_in[2] 3b001 = i_i2s_in[1] 3b000 = i_i2s_in[0] Note: SDATA_0 is selected with i_i2s_in[4](0x100).	3b111

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10.3.5.6 I2S Register (I2S_PIN_SEL_2, R/W, Address = 0xFA14_0014)

I2S_PIN_SEL_2	Bit	Description	Initial State
-	[7]	Reserved	0
pin_sel_5	[6:4]	Selects the SDATA_3 (I2S). 3b111 = i_i2s_in[5] 3b110 = i_i2s_in[6] 3b101 = i_i2s_in[5] 3b100 = i_i2s_in[4] 3b011 = i_i2s_in[3] 3b010 = i_i2s_in[2] 3b001 = i_i2s_in[1] 3b000 = i_i2s_in[0] Note: SDATA_3 is selected with i_i2s_in[1](0x001).	3b111
-	[3]	0	0
pin_sel_4	[2:0]	Selects the SDATA_2 (I2S). 3b111 = i_i2s_in[4] 3b110 = i_i2s_in[6] 3b101 = i_i2s_in[5] 3b100 = i_i2s_in[4] 3b011 = i_i2s_in[3] 3b010 = i_i2s_in[2] 3b001 = i_i2s_in[1] 3b000 = i_i2s_in[0] Note: SDATA_2 is selected with i_i2s_in[2](0x010).	3b111

10.3.5.7 I2S Register (I2S_PIN_SEL_3, R/W, Address = 0xFA14_0018)

I2S_PIN_SEL_3	Bit	Description	Initial State
-	[7:3]	Reserved	0
pin_sel_6	[2:0]	Selects the DSD_D5(DSD). 3b111 = i_i2s_in[6] 3b110 = i_i2s_in[6] 3b101 = i_i2s_in[5] 3b100 = i_i2s_in[4] 3b011 = i_i2s_in[3] 3b010 = i_i2s_in[2] 3b001 = i_i2s_in[1] 3b000 = i_i2s_in[0] Note: DSD_D5 is selected with i_i2s_in[0](0x000).	3b111

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10.3.5.8 I2S Register (I2S_DSD_CON, R/W, Address = 0xFA14_001C)

I2S_DSD_CON	Bit	Description	Initial State
-	[7:2]	Reserved	0
r_dsd_pol	[1]	1 = DSD_DATA changes at DSD_CLK rising edge 0 = DSD_DATA changes at DSD_CLK falling edge	1
dsd_en	[0]	1 = Enables DSD module 0 = Disables DSD module	0

10.3.5.9 I2S Register (I2S_IN_MUX_CON, R/W, Address = 0xFA14_0020)

I2S_IN_MUX_CON	Bit	Description	Initial State
f_num	[7:5]	Specifies the number of stage of noise filter for I2S input pins. 000 = no filtering 001 = 2-stage filter 010 = 3-stage filter 011 = 4-stage filter 100 = 5-stage filter Others = Reserved	3b011
in_en	[4]	Enables i2s_in, which is a sub-module at the input stage. 0 = Disables i2s_in module 1 = Enables i2s_in module If disabled, all output data is '0'.	0
audio_sel	[3:2]	Selects the audio. 2b00 = Enables SPDIF audio data 2b01 = Enables I2S audio data 2b10 = Enables DSD audio data	0
CUV_sel	[1]	Selects the CUV. 0 = Enables SPDIF CUV data 1 = Enables I2S CUV data	0
mux_en	[0]	Enables i2s_mux, which is a sub-module for audio selection. 0 = Disables i2s_mux module 1 = Enables i2s_mux module If disabled, all output data is '0'.	0

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10.3.5.10 Channel Status Register (I2S_CH_ST_CON, R/W, Address = 0xFA14_0024)

I2S_CH_ST_CON	Bit	Description	Initial State
-	[7:1]	Reserved	0
channel_status_reload	[0]	0 = Updates the shadow channel status registers 1 = Sets this bit to update the shadow channel status registers with the values updated in I2S_CH_ST_0 ~ I2S_CH_ST_4. This bit is cleared if the shadow channel status registers are updated.	0

Channel status information needs to be applied to the audio stream at the IEC 60958 block boundary. For this synchronization, there are two register sets for channel status block. You can set the channel status registers, I2S_CH_ST_0~I2S_CH_ST_4, while the I2S Rx module still refers to the shadow channel status registers, I2S_CH_ST_SH_0~ I2S_CH_ST_CH4.

To reflect the user configuration in the channel status registers, set 'channel_status_reload' bit in I2S_CH_ST_CON, then I2S Rx module copies the channel status registers into the shadow channel status registers at the beginning of an IEC-60958 block.

10.3.5.11 Channel Status Register (I2S_CH_ST_0, I2S_CH_ST_SH_0)

- I2S_CH_ST_0, R/W, Address = 0xFA14_0028
- I2S_CH_ST_SH_0, R, Address = 0xFA14_003C

I2S_CH_ST_0, I2S_CH_ST_SH_0	Bit	Description	Initial State
channel_status_mode	[7:6]	2b00 = Mode 0 Others = Reserved	0
emphasis	[5:3]	If bit1 = 0, 3b000 = 2 audio channels without pre-emphasis* 3b001 = 2 audio channels with 50us/ 15us pre-emphasis If bit1 = 1, 3b000 = default state	0
copyright	[2]	0 = Copyright 1 = No copyright	0
audio_sample_word	[1]	0 = linear PCM 1 = Non-linear PCM	0
channel_status_block	[0]	0 = Consumer format 1 = Professional format	0

NOTE: The bits listed here in channel status registers look swapped from those in IEC-60958-3 specification, as the bit order is different (LSB is right-most bit).

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10.3.5.12 Channel Status Register (I2S_CH_ST_1, I2S_CH_ST_SH_1)

- I2S_CH_ST_1, R/W, Address = 0xFA14_002C
- I2S_CH_ST_SH_1, R, Address = 0xFA14_0040

I2S_CH_ST_1, I2S_CH_ST_SH_1	Bit	Description	Initial State
category	[7:0]	Specifies the equipment type. CD player: 0000_0001 DAT player: L000_0011 DCC player: L100_0011 Mini disc: L100_1001 (L: information about generation status of the material)	0

10.3.5.13 Channel Status Register (I2S_CH_ST_2, I2S_CH_ST_SH_2)

- I2S_CH_ST_2, R/W, Address = 0xFA14_0030
- I2S_CH_ST_SH_2, R, Address = 0xFA14_0044

I2S_CH_ST_2, I2S_CH_ST_SH_2	Bit	Description	Initial State
channel_number	[7:4]	Specifies the channel number. Note: bit4 is LSB.	0
source_number	[3:0]	Specifies the source number. Note: bit0 is LSB.	0

10.3.5.14 Channel Status Register (I2S_CH_ST_3, I2S_CH_ST_SH_3)

- I2S_CH_ST_3, R/W, Address = 0xFA14_0034
- I2S_CH_ST_SH_3, R, Address = 0xFA14_0048

I2S_CH_ST_3, I2S_CH_ST_SH_3	Bit	Description	Initial State
-	[7:6]	Reserved	2b00
Clock_Accuracy	[5:4]	Specifies the clock accuracy, as specified in IEC-60958-3. 2b01 = Level I, ±50 ppm 2b00 = Level II, ±1000 ppm 2b10 = Level III, variable pitch shifted	2b00
Sampling_Frequency	[3:0]	Specifies the sampling frequency, as specified in IEC-60958-3. 4b0000 = 44.1 kHz 4b0010 = 48 kHz 4b0011 = 32 kHz 4b1010 = 96 kHz …	0

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10.3.5.15 Channel Status Register (I2S_CH_ST_4, I2S_CH_ST_SH_4)

- I2S_CH_ST_4, R/W, Address = 0xFA14_0038
- I2S_CH_ST_SH_4, R, Address = 0xFA14_004C

I2S_CH_ST_4, I2S_CH_ST_SH_4	Bit	Description	Initial State
Org_Sampling_Freq	[7:4]	Specifies the original sampling frequency. 4b1111 = 44.1KHz 4b0111 = 88.2KHz 4b1011 = 22.05KHz 4b0011 = 176.4KHz … For other frequencies, refer to the original sampling frequency specified in IEC-60958-3.	0x0
Word_Length	[3:1]	Specifies the word length. Max. length 24-bits 20-bits 3b000 = not defined not defined 3b001 = 20-bits 16-bits 3b010 = 22-bits 18-bits 3b100 = 23-bits 19-bits 3b101 = 24-bits 20-bits 3b110 = 21-bits 17-bits	3b000
Max_Word_Length	[0]	Specifies the maximum sample word length. 1 = 24-bits 0 = 20-bits	0

10.3.5.16 Channel Status Register (I2S_VD_DATA, R/W, Address = 0xFA14_0050)

I2S_VD_DATA	Bit	Description	Initial State
-	[7:1]	Reserved	7b0000000
validity_flag	[0]	Specifies the validity bit. 0 = Audio sample is reliable 1 = Audio sample is unreliable	0

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10.3.5.17 MUX Control Register (I2S_MUX_CH, R/W, Address = 0xFA14_0054)

I2S_MUX_CH	Bit	Description	Initial State
CH3_R_en	[7]	0 = Disables channel 3 right audio data output 1 = Enables channel 3 right audio data output	0
CH3_L_en	[6]	0 = Disables channel 3 left audio data output 1 = Enables channel 3 left audio data output	0
CH2_R_en	[5]	0 = Disables channel 2 right audio data output 1 = Enables channel 2 right audio data output	0
CH2_L_en	[4]	0 = Disables channel 2 left audio data output 1 = Enables channel 2 left audio data output	0
CH1_R_en	[3]	0 = Disables channel 1 right audio data output 1 = Enables channel 1 right audio data output	0
CH1_L_en	[2]	0 = Disables channel 1 left audio data output 1 = Enables channel 1 left audio data output	0
CH0_R_en	[1]	0 = Disables channel 0 right audio data output 1 = Enables channel 0 right audio data output	1
CH0_L_en	[0]	0 = Disables channel 0 left audio data output 1 = Enables channel 0 left audio data output	1

10.3.5.18 MUX Control Register (I2S_MUX_CUV, R/W, Address = 0xFA14_0058)

I2S_MUX_CUV	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
CUV_R_en	[1]	0 = Disables right channel CUV data 1 = Enables right channel CUV data	1
CUV_L_en	[0]	0 = Disables left channel CUV data 1 = Enables left channel CUV data	1

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10.3.5.19 Interrupt Control Register (I2S_IRQ_MASK, R/W, Address = 0xFA14_005C)

I2S_IRQ_MASK	Bit	Description	Initial State
-	[7:2]	Reserved	6b000000
int_2_mask	[1]	Disables interrupt request by int_2 interrupt. 0 = Disables int_2 interrupt 1 = Enables int_2 interrupt	0
-	[0]	Reserved	0

10.3.5.20 Interrupt Control Register (I2S_IRQ_STATUS, R/W, Address = 0xFA14_0060)

I2S_IRQ_STATUS	Bit	Description	Initial State
-	[7:2]	Reserved	0
int_2	[1]	Specifies the interrupt status, that is, the wrong register setting. This interrupt is asserted if the I2S_CON_2.bit_ch is set to 32fs, while I2S_CON_2.data_num is set to either 20-bit or 24-bit. According to the wrong register setting, some audio data MSB bits may be removed. The audio data is not available.	0
-	[0]	Reserved	0
For bit[1], the following holds: Reading returns the interrupt request status. **Warning:** 0: Has no effect. 1: Clears the interrupt request.			

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10.3.5.21 Output Buffer Register (I2S_CHX_Y_Z, R, Address = 0xFA14_0064~0xFA14_00D8)

I2S_CHX_Y_Z	Bit	Description	Initial State
I2S_CHX_Y_Z	[7:0]	Specifies the PCM output data from I2S Rx module. X = Channel = 0, 1, 2 Y = Left/Right = L, R Z = Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

10.3.5.22 Output Buffer Register (I2S_CUV_L_R, R, Address = 0xFA14_00DC)

I2S_CUV_L_R	Bit	Description	Initial State
-	[7]	Reserved	0
CUV_R	[6:4]	Specifies the VUCP data of right channel. CUV_R[3:0] = {valid bit, user bit, channel state bit, parity bit}	3b000
-	[3]	Reserved	0
CUV_L	[2:0]	Specifies the VUCP data of left channel. CUV_L[3:0] = {valid bit, user bit, channel state bit, parity bit}	3b000

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10.3.6 TIMING GENERATOR REGISTER (TG CONFIGURE/STATUS REGISTER)

10.3.6.1 TG Command Register (TG_CMD, R/W, Address = 0xFA15_0000)

TG_CMD	Bit	Description	Initial State
Reserved	[7:5]	Reserved	000
getsync_type	[4]	Specifies the timing correction enable bit. If this bit is set, the input VSYNC timing error relative to output VSYNC is corrected. 0 = Disables 1 = Enables	0
getsync_en	[3]	Enables BT656 input synchronization.	0
Reserved	[2]	Reserved	0
field_en	[1]	Enables field mode. For 1080i, this should be enabled.	0
tg_en	[0]	Specifies the TG global enable bit.	0

10.3.6.2 Horizontal Full Size (TG_H_FSZ_L, R/W, Address = 0xFA15_0018)

TG_H_FSZ_L	Bit	Description	Initial State
TG_H_FSZ_L	[7:0]	Specifies the horizontal full size (1~8191) (Lower part).	0x72

10.3.6.3 Horizontal Full Size (TG_H_FSZ_H, R/W, Address = 0xFA15_001C)

TG_H_FSZ_H	Bit	Description	Initial State
Reserved	[7:5]	Reserved	0x0
TG_H_FSZ_H	[4:0]	Specifies the horizontal full size (1~8191) (Upper part).	0x6

10.3.6.4 Horizontal Active Start Position (TG_HACT_ST_L, R/W, Address = 0xFA15_0020)

TG_HACT_ST_L	Bit	Description	Initial State
TG_HACT_ST_L	[7:0]	Specifies the horizontal active start position (1~4095) (Lower part).	0x05

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10.3.6.5 Horizontal Active Start Position (TG_HACT_ST_H, R/W, Address = 0xFA15_0024)

TG_HACT_ST_H	Bit	Description	Initial State
Reserved	[7:4]	Reserved	0x0
TG_HACT_ST_H	[3:0]	Specifies the horizontal active start position (1~4095) (Upper part).	0x1

10.3.6.6 Horizontal Active Size (TG_HACT_SZ_L, R/W, Address = 0xFA15_0028)

TG_HACT_SZ_L	Bit	Description	Initial State
TG_HACT_SZ_L	[7:0]	Specifies the horizontal active size (0~4095) (Lower part).	0x00

10.3.6.7 Horizontal Active Size (TG_HACT_SZ_H, R/W, Address = 0xFA15_002C)

TG_HACT_SZ_H	Bit	Description	Initial State
Reserved	[7:4]	Reserved	0x0
TG_HACT_SZ_H	[3:0]	Specifies the horizontal active size (0~4095) (Upper part).	0x5

10.3.6.8 Vertical Full Size (TG_V_FSZ_L, R/W, Address = 0xFA15_0030)

TG_V_FSZ_L	Bit	Description	Initial State
TG_V_FSZ_L	[7:0]	Specifies the vertical full size (1~2047) (Lower part).	0xEE

10.3.6.9 Vertical Full Size (TG_V_FSZ_H, R/W, Address = 0xFA15_0034)

TG_V_FSZ_H	Bit	Description	Initial State
Reserved	[7:3]	Reserved	0x0
TG_V_FSZ_H	[2:0]	Specifies the vertical full size (1~2047) (Upper part).	0x2

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10.3.6.10 VSYNC Position (TG_VSYNC_L, R/W, Address = 0xFA15_0038)

TG_VSYNC_L	Bit	Description	Initial State
TG_VSYNC_L	[7:0]	Specifies the vertical sync position. If field enable is set, this bit takes the top field vsync position (1~2047) (Lower part).	0x01

10.3.6.11 VSYNC Position (TG_VSYNC_H, R/W, Address = 0xFA15_003C)

TG_VSYNC_H	Bit	Description	Initial State
Reserved	[7:3]	Reserved	0x0
TG_VSYNC_H	[2:0]	Specifies the vertical sync position. If field enable is set, this bit takes the top field vsync position (1~2047) (Upper part).	0x0

10.3.6.12 Bottom Field VSYNC Position (TG_VSYNC2_L, R/W, Address = 0xFA15_0040)

TG_VSYNC2_L	Bit	Description	Initial State
TG_VSYNC2_L	[7:0]	Specifies the vertical sync position for bottom field (1~2047) (Lower part).	0x33

10.3.6.13 Bottom Field VSYNC Position (TG_VSYNC2_H, R/W, Address = 0xFA15_0044)

TG_VSYNC2_H	Bit	Description	Initial State
Reserved	[7:0]	Reserved	0x0
TG_VSYNC2_H	[2:0]	Specifies the vertical sync position for bottom field (1~2047) (Upper part).	0x2

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10.3.6.14 Vertical Active Start Position (G_VACT_ST_L, R/W, Address = 0xFA15_0048)

TG_VACT_ST_L	Bit	Description	Initial State
TG_VACT_ST_L	[7:0]	Specifies the vertical active start position (1~2047) (Lower part).	0x1a

10.3.6.15 Vertical Active Start Position (TG_TACT_ST_H, R/W, Address = 0xFA15_004C)

TG_VACT_ST_H	Bit	Description	Initial State
Reserved	[7:3]	Reserved	0x0
TG_VACT_ST_H	[2:0]	Specifies the vertical active start position (1~2047) (Upper part).	0x0

10.3.6.16 Vertical Active Size (TG_VACT_SZ_L, R/W, Address = 0xFA15_0050)

TG_VACT_SZ_L	Bit	Description	Initial State
TG_VACT_SZ_L	[7:0]	Specifies the vertical active size (0~2047) (Lower part).	0xD0

10.3.6.17 Vertical Active Size (TG_TACT_SZ_H, R/W, Address = 0xFA15_0054)

TG_VACT_SZ_H	Bit	Description	Initial State
Reserved	[7:3]	Reserved	0x0
TG_VACT_SZ_H	[2:0]	Specifies the vertical active size (0~2047) (Upper part).	0x2

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10.3.6.18 Field Change Position (TG_FIELD_CHG_L, R/W, Address = 0xFA15_0058)

TG_FIELD_CHG_L	Bit	Description	Initial State
TG_FIELD_CHG_L	[7:0]	Specifies the HDMI field position. (Lower part).	0x33

10.3.6.19 Field Change Position (TG_FIELD_CHG_H, R/W, Address = 0xFA15_005C)

TG_FIELD_CHG_H	Bit	Description	Initial State
Reserved	[7:3]	Reserved	0x0
TG_FIELD_CHG_H	[2:0]	Specifies the HDMI field position. (Upper part).	0x2

10.3.6.20 Bottom Field Vertical Active Start Position (TG_VACT_ST2_L, R/W, Address = 0xFA15_0060)

TG_VACT_ST2_L	Bit	Description	Initial State
TG_VACT_ST2_L	[7:0]	Specifies the HDMI vertical active start position for bottom field (Lower part).	0x48

10.3.6.21 Bottom Field VSYNC Position for HDMI (TG_VACT_ST2_H, R/W, Address = 0xFA15_0064)

TG_ VACT_ST2_H	Bit	Description	Initial State
Reserved	[7:3]	Reserved	0x0
TG_VACT_ST2_L	[2:0]	Specifies the HDMI vertical active start position for bottom field (Upper part).	0x2

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10.3.6.22 VSYNC Position for HDMI (TG_VSYNC_TOP_HDMI_L, R/W, Address = 0xFA15_0078)

TG_VSYNC_TOP_HDMI_L	Bit	Description	Initial State
TG_VSYNC_TOP_HDMI_L	[7:0]	Specifies the HDMI VSYNC position for top field (Lower part).	0x01

10.3.6.23 VSYNC Position for HDMI (TG_VSYNC_TOP_HDMI_H, R/W, Address = 0xFA15_007C)

TG_VSYNC_TOP_HDMI_H	Bit	Description	Initial State
Reserved	[7:3]	Reserved	0x0
TG_VSYNC_TOP_HDMI_H	[2:0]	Specifies the HDMI VSYNC position for top field (Upper part).	0x0

10.3.6.24 Bottom Field VSYNC Position for HDMI (TG_VSYNC_BOT_HDMI_L, R/W, Address = 0xFA15_0080)

TG_VSYNC_BOT_HDMI_L	Bit	Description	Initial State
TG_VSYNC_BOT_HDMI_L	[7:0]	Specifies the HDMI VSYNC position for bottom field (Lower part).	0x01

10.3.6.25 Bottom Field VSYNC Position for HDMI (TG_VSYNC_BOT_HDMI_H, R/W, Address = 0xFA15_0084)

TG_VSYNC_BOT_HDMI_H	Bit	Description	Initial State
Reserved	[7:3]	Reserved	0x0
TG_VSYNC_BOT_HDMI_H	[2:0]	Specifies the HDMI VSYNC position for bottom field (Upper part).	0x0

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10.3.6.26 Top Field Change Start Position for HDMI (TG_FIELD_TOP_HDMI_L, R/W, Address = 0xFA15_0088)

TG_FIELD_TOP_HDMI_L	Bit	Description	Initial State
TG_FIELD_TOP_HDMI_L	[7:0]	Specifies the HDMI top field start position (Lower part).	0x01

10.3.6.27 Top Field Change Start Position for HDMI (TG_FIELD_TOP_HDMI_H, R/W, Address = 0xFA15_008C)

TG_FIELD_TOP_HDMI_H	Bit	Description	Initial State
Reserved	[7:3]	Reserved	0x0
TG_FIELD_TOP_HDMI_H	[2:0]	Specifies the HDMI top field start position (Upper part).	0x0

10.3.6.28 Bottom Field Change Start Position for HDMI (TG_FIELD_BOT_HDMI_L, R/W, Address = 0xFA15_0090)

TG_FIELD_BOT_HDMI_L	Bit	Description	Initial State
TG_FIELD_BOT_HDMI_L	[7:0]	Specifies the HDMI bottom field start position (Lower part).	0x33

10.3.6.29 Bottom Field VSYNC Start Position for HDMI (TG_FIELD_BOT_HDMI_H, R/W, Address = 0xFA15_0094)

TG_FIELD_BOT_HDMI_H	Bit	Description	Initial State
Reserved	[7:3]	Reserved	0x0
TG_FIELD_BOT_HDMI_H	[2:0]	Specifies the HDMI bottom field start position (Upper part).	0x2

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10.3.6.30 HSYNC width Configuration for MHL Interface (MHL_HSYNC_WIDTH, R/W, Address = 0xFA15_017C)

MHL_HSYNC_WIDTH	Bit	Description	Initial State
MHL_HSYNC_WIDTH	[7:0]	Specifies the HSYNC width for MHL interface (Unit: pixel clock). The HSYNC width is MHL_HSYNC_WIDTH + 1.	0xF

10.3.6.31 VSYNC width Configuration for MHL Interface (MHL_VSYNC_WIDTH, R/W, Address = 0xFA15_0180)

MHL_VSYNC_WIDTH	Bit	Description	Initial State
MHL_VSYNC_WIDTH	[7:0]	Specifies the VSYNC width for MHL interface (Unit: line).	0x1

10.3.6.32 RGB Clock Inversion for MHL Interface (MHL_CLK_INV, R/W, Address = 0xFA15_0184)

MHL_CLK_INV	Bit	Description	Initial State
MHL_CLK_INV	[0]	Specifies the clock out inversion for MHL interface. 0 = Normal 1 = Inversion	0x0

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10.3.6.33 HDCP E-FUSE Control Register (HDCP_E_FUSE_CTRL, W, Address = 0xFA16_0000)

HDCP_E_FUSE_CTRL	Bit	Description	Initial State
-	[7:1]	Reserved	4b0000
HDCP_KEY_READ	[0]	0 = Normal 1 = To read HDCP key from e-fuse.	0

10.3.6.34 HDCP E-FUSE Control Register (HDCP_E_FUSE_STATUS, R, Address = 0xFA16_0004)

HDCP_E_FUSE_STATUS	Bit	Description	Initial State
-	[7:3]	Reserved	4b0000
EFUSE_ECC_FAIL	[2]	0 = Normal 1 = ECC fail	
EFUSE_ECC_BUSY	[1]	0 = Not busy 1 = Busy	
EFUSE_ECC_DONE	[0]	0 = Normal 1 = ECC done	0

10.3.6.35 HDCP E-FUSE Control Register (EFUSE_ADDR_WIDTH, R/W, Address = 0xFA16_0008)

EFUSE_ADDR_WIDTH	Bit	Description	Initial State
EFUSE_ADDR_WIDTH	[7:0]	Specifies the address width (Unit: HDMI link PCLK, default: 83MHz, 12n).	0x14

10.3.6.36 HDCP E-FUSE Control Register (EFUSE_SIGDEV_ASSERT, R/W, Address = 0xFA16_000C)

EFUSE_SIGDEV_ASSERT	Bit	Description	Initial State
EFUSE_SIGDEV_ASSERT	[7:0]	Specifies the SIGDEV asserting position (Unit: HDMI Link PCLK, default: 83MHz, 12n).	0x0

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10.3.6.37 HDCP E-FUSE Control Register (EFUSE_SIGDEV_DE-ASSERT, R/W, Address = 0xFA16_0010)

EFUSE_SIGDEV_DEASSERT	Bit	Description	Initial State
EFUSE_SIGDEV_DEASSERT	[7:0]	Specifies the SIGDEV de-asserting position (Unit: HDMI Link PCLK, default: 83MHz, 12n)	0x8

10.3.6.38 HDCP E-FUSE Control Register (EFUSE_PRCHG_ASSERT, R/W, Address = 0xFA16_0014)

EFUSE_PRCHG_ASSERT	Bit	Description	Initial State
EFUSE_PRCHG_ASSERT	[7:0]	Specifies the PRCHG asserting position (Unit: HDMI Link PCLK, default: 83MHz, 12n)	0x0

10.3.6.39 HDCP E-FUSE Control Register (EFUSE_PRCHG_DE-ASSERT, R/W, Address = 0xFA16_0018)

EFUSE_PRCHG_DE-ASSERT	Bit	Description	Initial State
EFUSE_PRCHG_DEASSERT	[7:0]	Specifies the PRCHG de-asserting position (Unit: HDMI link PCLK, default: 83MHz, 12n).	0xC

10.3.6.40 HDCP E-FUSE Control Register (EFUSE_FSET_ASSERT, R/W, Address = 0xFA16_001C)

EFUSE_FSET_ASSERT	Bit	Description	Initial State
EFUSE_FSET_ASSERT	[7:0]	Specifies the FSET asserting position (Unit: HDMI link PCLK, default: 83MHz, 12n)	0x4

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10.3.6.41 HDCP E-FUSE Control Register (EFUSE_FSET_DE-ASSERT, R/W, Address = 0xFA16_0020)

EFUSE_FSET_DEASSERT	Bit	Description	Initial State
EFUSE_FSET_DEASSERT	[7:0]	Specifies the FSET de-asserting position (Unit: HDMI link PCLK, default: 83MHz, 12n)	0x10

10.3.6.42 HDCP E-FUSE Control Register (EFUSE_SENSING, R/W, Address = 0xFA16_0024)

EFUSE_SENSING	Bit	Description	Initial State
EFUSE_SENSING	[7:0]	Specifies the sensing width (Unit: HDMI link PCLK, default: 83MHz, 12n).	0x14

10.3.6.43 HDCP E-FUSE Control Register (EFUSE_SCK_ASSERT, R/W, Address = 0xFA16_0028)

EFUSE_SCK_ASSERT	Bit	Description	Initial State
EFUSE_SCK_ASSERT	[7:0]	Specifies the SCK asserting position (Unit: HDMI link PCLK, default: 83MHz, 12n)	0x4

10.3.6.44 HDCP E-FUSE Control Register (EFUSE_SCK_DEASSERT, R/W, Address = 0xFA16_002C)

EFUSE_SCK_DEASSERT	Bit	Description	Initial State
EFUSE_SCK_DEASSERT	[7:0]	Specifies the SCK de-asserting position (Unit: HDMI link PCLK, default: 83MHz, 12n)	0xC

10.3.6.45 HDCP E-FUSE Control Register (EFUSE_SDOUT_OFFSET, R/W, Address = 0xFA16_0030)

EFUSE_SDOUT_OFFSET	Bit	Description	Initial State
EFUSE_SDOUT_OFFSET	[7:0]	Specifies the SDOUT offset (Unit: HDMI link PCLK, default: 83MHz, 12n)	0x10

10.3.6.46 HDCP E-FUSE Control Register (EFUSE_READ_OFFSET, R/W, Address = 0xFA16_0034)

EFUSE_READ_OFFSET	Bit	Description	Initial State
EFUSE_READ_OFFSET	[7:0]	Specifies the READ Offset (Unit: HDMI link PCLK, default: 83MHz, 12n).	0x14

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10.3.6.47 CEC Configure Register (CEC_TX_STATUS_0, R, Address = 0xE1B0_0000)

CEC_TX_STATUS_0	Bit	Description	Initial State
-	[7:4]	Reserved	4b0000
Tx_Error	[3]	Specifies the CEC Tx_Error interrupt flag. This bit field also specifies the status of Tx_Error interrupt and is valid only if Tx_Done bit is set. 0 = No error occurs 1 = An error occurs during CEC Tx transfer It will be cleared - if set to 0 by Tx_Enable bit of CEC_TX_CTRL register - if set Clear_Intr_Tx_Done or Clear_Intr_Tx_Error bit in CEC_INTR_CLEAR register	0
Tx_Done	[2]	Specifies the CEC Tx_Done interrupt flag. This bit field also specifies the status of Tx_Done interrupt. 0 = Running or idle 1 = Finishes CEC Tx transfer It will be cleared - if Tx_Enable bit of CEC_TX_CTRL_0 is reset - if Clear_Intr_Tx_Done or Clear_Intr_Tx_Error bit in CEC_INTR_CLEAR register is set	0
Tx_Transferring	[1]	If TX-Running is set, this field is valid. 0 = Tx waits for the CEC Bus 1 = CEC Tx transfers data via CEC Bus	0
Tx_Running	[0]	0 = Tx Idle 1 = Enables CEC Tx, and waits for the CEC bus or transfers the message.	0

10.3.6.48 CEC Configure Register (CEC_TX_STATUS_1, R, Address = 0xE1B0_0004)

CEC_TX_STATUS_1	Bit	Description	Initial State
Tx_Bytes_Transferred	[7:0]	Specifies the number of blocks transferred (1 byte = 1 block in a CEC message). After sending the CEC message, this field will be updated. It will be cleared if Clear_Intr_Tx_Done or Clear_Intr_Tx_Error bit is set in CEC_Intr_Clear register.	0

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10.3.6.49 CEC Configure Register (CEC_RX_STATUS_0, R, Address = 0xE1B0_0008)

CEC_RX_STATUS_0	Bit	Description	Initial State
-	[7:5]	Reserved	3b000
Rx_BCast	[4]	Specifies the broadcast message flag. 0 = Received CEC message is the address to a single device 1 = Received CEC message is the broadcast message It will be cleared - if Rx_Enable bit of CEC_RX_CTRL_0 is reset - if Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_INTR_CLEAR register is set	0
Rx_Error	[3]	Specifies the CEC Rx_Error interrupt flag. This bit field also specifies the status of Rx_Error interrupt and is valid only if Rx_Done bit is set. 0 = No error occurs 1 = An error occurs while receiving a CEC message It will be cleared - if Rx_Enable bit of CEC_RX_CTRL_0 is reset - if Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_INTR_CLEAR register is set	0
Rx_Done	[2]	Specifies the CEC Rx done interrupt flag. This bit field also specifies the status of Rx_Done interrupt. 0 = Running or Idle 1 = Finishes CEC Rx transfer It will be cleared: - if Rx_Enable bit of CEC_RX_CTRL_0 is reset - if Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_INTR_CLEAR register is set	0
Rx_Receiving	[1]	0 = Rx waits for a CEC message 1 = Rx receives data via CEC bus	0
Rx_Running	[0]	0 = Disables Rx 1 = Enables CEC Rx and waits for a message on the CEC bus	0

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10.3.6.50 CEC Configure Register (CEC_RX_STATUS_1, R, Address = 0xE1B0_000C)

CEC_RX_STATUS_1	Bit	Description	Initial State
Rx_Bytes_Received	[7:0]	Specifies the number of blocks received (1 byte = 1 block in a CEC message). After receiving the CEC message, the field will be updated. It will be cleared if Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_Intr_Clear register is set.	0

10.3.6.51 CEC Configure Register (CEC_INTR_MASK, R/W, Address = 0xE1B0_0010)

CEC_INTR_MASK	Bit	Description	Initial State
-	[7:6]	Reserved	2b00
Mask_Intr_Rx_Error	[5]	Specifies the Rx_Error interrupt mask bit. 0 = Enables 1 = Disables	0
Mask_Intr_Rx_Done	[4]	Specifies the Rx_Done interrupt mask bit. 0 = Enables 1 = Disables	0
-	[3:2]	Reserved	2b00
Mask_Intr_Tx_Error	[1]	Specifies the Tx_Error interrupt mask bit. 0 = Enables 1 = Disables	0
Mask_Intr_Tx_Done	[0]	Specifies the Tx_Done interrupt mask bit. 0 = Enables 1 = Disables	0

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10.3.6.52 CEC Configure Register (CEC_INTR_CLEAR, R/W, Address = 0xE1B0_0014)

CEC_INTR_CLEAR	Bit	Description	Initial State
-	[7:6]	Reserved	2b00
Clear_Intr_Rx_Error	[5]	Specifies the Rx_Error interrupt clear bit. 0 = No effect 1 = Clears Rx_Error and Rx_Bytes_Received fields in CEC_RX_STATUS_0 and 1 registers. It will be cleared after one clock.	0
Clear_Intr_Rx_Done	[4]	Specifies the Rx_Done interrupt clear bit. 0 = No effect 1 = Clears Rx_Done and Rx_Bytes_Received fields in CEC_RX_STATUS_0 and 1 registers. Resets to 0 after one clock.	0
-	[3:2]	Reserved	2b00
Clear_Intr_Tx_Error	[1]	Specifies the Tx_Error interrupt clear bit. 0 = No effect 1 = Clears Tx_Error and Tx_Bytes_Received fields in CEC_TX_STATUS_0 and 1 registers. Resets to 0 after one clock.	0
Clear_Intr_Tx_Done	[0]	Specifies the Tx_Done interrupt clear bit. 0 = No effect 1 = Clears Tx_Done and Tx_Bytes_Received fields in CEC_TX_STATUS_0 and 1 registers. Resets to 0 after one clock.	0

10.3.6.53 CEC Configure Register (CEC_LOGIC_ADDR, R/W, Address = 0xE1B0_0020)

CEC_LOGIC_ADDR	Bit	Description	Initial State
-	[7:4]	Reserved	4b0000
Logic_Addr	[3:0]	Specifies the HDMI Tx logical address (0~15).	4b0000

10.3.6.54 CEC Configure Register (CEC_ DIVISOR_0 ~ CEC_ DIVISOR_3, R/W, Address = 0xE1B0_0030)

CEC_ DIVISOR_0~ CEC_ DIVISOR_3	Bit	Description	Initial State
CEC_Divisor	[7:0]	Specifies the divisor used in counting 0.05ms period. This divisor should satisfy the following equation: (CEC_DIVISOR+1) x (clock cycle time(ns)) = 0.05ms Note: To apply CEC_Divisor, it should be '0' for Tx_Reset and Rx_Reset, while Tx_Start and Rx_Start are '0'.	0

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10.3.6.55 Tx Related Register (CEC_TX_CTRL, R/W, Address = 0xE1B0_0040)

CEC_TX_CTRL	Bit	Description	Initial State
Reset	[7]	Specifies the CEC Tx reset bit. 0 = No effect 1 = Immediately resets CEC Tx related registers and state machines to its reset value. Resets to 0 after one clock.	0
Tx_Retrans_Num	[6:4]	Specifies the number of retransmissions tried (according to CEC specification on page CEC-13). Based on the specification, this value should be set to 5.	3b001
-	[3:2]	Reserved	2b00
Tx_BCast	[1]	Specifies the CEC Tx broadcast message bit. This bit also specifies the CEC message in CEC_TX_BUFFER_00~15, which is directly addressed (addressed to a single device) or broadcast. This bit determines whether a block transfer is acknowledged or not (according to ACK scheme in CEC specification (section CEC 6.1.2)) 0 = Directly addressed message 1 = Broadcast message	0
Tx_Start	[0]	Specifies the CEC Tx start bit. 0 = Tx idle 1 = Starts CEC message transfer (Resets to 0 after start)	0

10.3.6.56 Tx Related Register (CEC_TX_BYTE_NUM, R/W, Address = 0xE1B0_0044)

CEC_TX_BYTE_NUM	Bit	Description	Initial State
Tx_Byte_Num	[7:0]	Specifies the number of blocks in a message that has to be sent (1 byte = 1 block in a CEC message).	0

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10.3.6.57 Tx Related Register (CEC_TX_STATUS_2, R, Address = 0xE1B0_0060)

CEC_TX_STATUS_2	Bit	Description	Initial State
Tx_Wait	[7]	Specifies the CEC Tx signal free time waiting flag bit. 0 = Tx is in other state 1 = CEC Tx waits for signal free time (stops sending messages after earlier attempts to send message).	0
Tx_Sending_Start_Bit	[6]	Specifies the CEC Tx start bit sending flag bit. 0 = Tx is in other state 1 = CEC Tx sends a start bit	0
Tx_Sending_Hdr_Blk	[5]	Specifies the CEC Tx header block sending flag bit. 0 = Tx is in other state 1 = CEC Tx sends the header block	0
Tx_Sending_Data_Blk	[4]	Specifies the CEC Tx data block sending flag bit. 0 = Tx is in other state 1 = CEC Tx sends data blocks	0
Tx_Latest_Initiator	[3]	Specifies the CEC Tx last initiator flag bit. 0 = This device is not the latest initiator on the CEC bus 1 = This CEC device is the latest initiator to send a CEC message; no other CEC device sends a message. It will be cleared if Rx detects a start bit on the CEC line or sets Tx_Enable bit of CEC_Tx_Ctrl_0 (that is becomes a new initiator)	0
-	[2:0]	Reserved	3b000

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10.3.6.58 Tx Related Register (CEC_TX_STATUS_3, R, Address = 0xE1B0_0064)

CEC_TX_STATUS_3	Bit	Description	Initial State
Reserved	[7]	Reserved	0
Tx_Wait_SFT_Succ	[6]	Specifies the CEC Tx signal free time for successive message transfer waiting flag bit. 0 = Tx is in other state 1 = Tx waits for signal free time (SFT) with a precondition that Tx is the most recent initiator on the CEC bus and wants to send another frame immediately after its previous frame (SFT ≥ 7x2.4ms).	0
Tx_Wait_SFT_New	[5]	Specifies the CEC Tx signal free time for a new initiator waiting flag bit. 0 = Tx is in other state 1 = Tx waits for SFT with a precondition that Tx is the new initiator and wants to send a frame (SFT ≥ 5x2.4ms).	0
Tx_Wait_SFT_Retran	[4]	Specifies the CEC Tx signal free time for a new initiator waiting flag bit. 0 = Tx is in other state 1 = Tx waits for SFT with a precondition (the precondition is that Tx should attempt to retransmit the message (SFT ≥ 3 x2.4ms))	0
Tx_Retrans_Cnt	[3:1]	Specifies the current retransmission count. If ‘0’, no retransmission occurs. It will be cleared if Clear_Intr_Tx_Done or Clear_Intr_Tx_Error bit in CEC_Intr_Clear register is set.	3b000
Tx_ACK_Failed	[0]	Specifies the CEC Tx acknowledge failed flag bit. 0 = Tx is in the other state 1 = Tx is not acknowledged. This bit is set if - ACK bit in a block is logical 1 in a directly addressed message - ACK bit in a block is logical 0 in a broadcast message	0

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10.3.6.59 Tx Related Register (CEC_TX_BUFFER_0 ~ 15)

- CEC_ TX_BUFFER_0, R/W, Address = 0xE1B0_0080
- CEC_ TX_BUFFER_1, R/W, Address = 0xE1B0_0084
- CEC_ TX_BUFFER_2, R/W, Address = 0xE1B0_0088
- CEC_ TX_BUFFER_3, R/W, Address = 0xE1B0_008C
- CEC_ TX_BUFFER_4, R/W, Address = 0xE1B0_0090
- CEC_ TX_BUFFER_5, R/W, Address = 0xE1B0_0094
- CEC_ TX_BUFFER_6, R/W, Address = 0xE1B0_0098
- CEC_ TX_BUFFER_7, R/W, Address = 0xE1B0_009C
- CEC_ TX_BUFFER_8, R/W, Address = 0xE1B0_00A0
- CEC_ TX_BUFFER_9, R/W, Address = 0xE1B0_00A4
- CEC_ TX_BUFFER_10, R/W, Address = 0xE1B0_00A8
- CEC_ TX_BUFFER_11, R/W, Address = 0xE1B0_00AC
- CEC_ TX_BUFFER_12, R/W, Address = 0xE1B0_00B0
- CEC_ TX_BUFFER_13, R/W, Address = 0xE1B0_00B4
- CEC_ TX_BUFFER_14, R/W, Address = 0xE1B0_00B8
- CEC_ TX_BUFFER_15, R/W, Address = 0xE1B0_00BC

CEC_ TX_BUFFER_0~ CEC_ TX_BUFFER_15	Bit	Description	Initial State
Tx_Block_0 ~ Tx_Block_15	[7:0]	Specifies the byte #0 ~ #15 of CEC message. Each byte corresponds to a block in a message. Block_0 is the header block and block_1 ~15 are data blocks. Note: The initiator and destination logical address in a header block should be written by software.	0

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10.3.6.60 Rx Related Register (CEC_ RX_CTRL, R/W, Address = E1B0_00C0)

CEC_RX_CTRL_0	Bit	Description	Initial State
Reset	[7]	Specifies the CEC Rx reset bit. 0 = No effect 1 = Immediately resets CEC Rx related registers and state machines to its reset value. It will be cleared after one clock	0
Check_Sampling_Error	[6]	Specifies the CEC Rx sampling error check enable bit. 0 = Does not check sampling error 1 = Checks sampling error while receiving data bits CEC Rx samples the CEC bus three times (at 1.00, 1.05, and 1.10 ms) and checks whether the three samples are identical.	0
Check_Low_Time_Error	[5]	Specifies the CEC Rx low-time error check enable bit. 0 = Does not check low-time error 1 = Checks low-time error while receiving data bits In receiving each bit from the CEC bus, CEC Rx checks the duration of logical 0 from the starting of one bit transfer (falling edge on the CEC bus). Rx checks whether the duration is longer than the maximum time the CEC bus can be in logical 0 (max 1.7 ms).	0
Check_Start_Bit_Error	[4]	Specifies the CEC Rx start bit error check enable bit 0 = Does not check start bit error. 1 = Checks start bit error while receiving a start bit. After receiving a start bit from the CEC bus, CEC Rx checks the duration of logical 0 and 1 of start bit (as specified in CEC specification on page CEC-8). Rx checks whether the duration meets the specification.	0
-	[3:2]	Reserved	2b00
Rx_Host_Busy	[1]	Specifies the CEC Rx host busy bit. 0 = Rx receives incoming message and sends acknowledgement. 1 = A host processor is unavailable to receive and process CEC messages. Rx sends “not acknowledged” signal to a message initiator to indicate that a host processor is unavailable and to receive and process CEC messages.	0
Rx_Enable	[0]	Specifies the CEC Rx start bit. 0 = Disables Rx 1 = Enables CEC Rx module to receive a message This bit is cleared after receiving a message.	0

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10.3.6.61 Rx Related Register (CEC_ RX_STATUS_2, R, Address = 0xE1B0_00E0)

CEC_RX_STATUS_2	Bit	Description	Initial State
Rx_Waiting	[7]	Specifies the CEC Rx waiting flag bit. 0 = Rx is in other state 1 = CEC Rx waits for a message	0
Rx_Receiving_Start_Bit	[6]	Specifies the CEC Rx start bit receiving flag bit. 0 = Rx is in other state 1 = CEC Rx receives a start bit	0
Rx_Receiving_Hdr_Blk	[5]	Specifies the CEC Rx header block receiving flag bit. 0 = Rx is in other state 1 = CEC Rx receives a header block	0
Rx_Receiving_Data_Blk	[4]	Specifies the CEC Rx data block receiving flag bit. 0 = Rx is in other state 1 = CEC Rx receives data blocks	0
-	[3:0]	Reserved	4b0000

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10.3.6.62 Rx Related Register (CEC_ RX_STATUS_3, R, Address = 0xE1B0_00E4)

CEC_RX_STATUS_3	Bit	Description	Initial State
-	[7]	Reserved	0
Sampling_Error	[6]	Specifies the CEC Rx sampling error flag bit. 0 = No sampling error occurs 1 = A sampling error occurs while receiving a message CEC Rx samples the CEC bus three times (at 1.00, 1.05, and 1.10 ms) and sets this bit if Check_Sampling_Error bit in CEC_RX_CTRL_0 is set and if three samples are not identical. It will be cleared if Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_INTR_CLEAR register is set to 0.	0
Low_Time_Error	[5]	Specifies the CEC Rx low-time error flag bit. 0 = No low-time error occurs 1 = A low-time error occurs while receiving a message While receiving each bit from the CEC bus, CEC Rx checks the duration of logical 0 from the start of one-bit transfer (falling edge on the CEC bus). If the duration is longer than the maximum time, the CEC bus can be logical 0 (maximum 1.7 ms). CEC RX sets this bit. This bit field will be set to 0 if Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_INTR_CLEAR register is set.	0
Start_Bit_Error	[4]	Specifies the CEC Rx start bit error flag bit. 0 = No start bit error occurs 1 = A start bit error occurs while receiving a message While receiving a start bit from the CEC bus, CEC Rx checks the duration of logical 0 and 1 of a starting bit (as specified in CEC spec. page CEC-8). If the duration does not meet the spec., CEC RX sets this bit. This bit field will be set to 0 if Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_INTR_CLEAR register is set.	0
-	[3:1]	Reserved	3b000
CEC_Line_Error	[0]	Specifies the CEC Rx line error flag bit. 0 = No line error occurs 1 = A start bit error line occurs while receiving a message In CEC spec. page CEC-13, CEC line error occurs in a period when two consecutive falling edges is smaller than a minimum data bit period. Rx checks for this condition, and if it occurs, it sends the line error notification, that is, sends logical 0 for more than 1.4~1.6 times of the nominal data bit period (2.4ms). This bit will be cleared: - if Rx_Enable bit of CEC_RX_CTRL_0 is set - if Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in	0

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CEC_RX_STATUS_3	Bit	Description	Initial State
		CEC_INTR_CLEAR register is set	

10.3.6.63 Rx Related Register (CEC_RX_BUFFER_0 ~ CEC_RX_BUFFER_15)

- CEC_RX_BUFFER_0, R, Address = 0xE1B0_0100
- CEC_RX_BUFFER_1, R, Address = 0xE1B0_0104
- CEC_RX_BUFFER_2, R, Address = 0xE1B0_0108
- CEC_RX_BUFFER_3, R, Address = 0xE1B0_010C
- CEC_RX_BUFFER_4, R, Address = 0xE1B0_0110
- CEC_RX_BUFFER_5, R, Address = 0xE1B0_0114
- CEC_RX_BUFFER_6, R, Address = 0xE1B0_0118
- CEC_RX_BUFFER_7, R, Address = 0xE1B0_011C
- CEC_RX_BUFFER_8, R, Address = 0xE1B0_0120
- CEC_RX_BUFFER_9, R, Address = 0xE1B0_0124
- CEC_RX_BUFFER_10, R, Address = 0xE1B0_0128
- CEC_RX_BUFFER_11, R, Address = 0xE1B0_012C
- CEC_RX_BUFFER_12, R, Address = 0xE1B0_0130
- CEC_RX_BUFFER_13, R, Address = 0xE1B0_0134
- CEC_RX_BUFFER_14, R, Address = 0xE1B0_0138
- CEC_RX_BUFFER_15, R, Address = 0xE1B0_013C

CEC_RX_BUFFER_0~ CEC_RX_BUFFER_15	Bit	Description	Initial State
Rx_Block_0 ~ Rx_Block_15	[7:0]	Specifies byte #0 ~ #15 of CEC message. Each byte corresponds to a block in a message. Block_0 is the header block and Block_1 ~15 are data blocks.	0

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10.3.6.64 Input Filtering Register (CEC_ FILTER_CTRL, R/W, Address = 0xE1B0_0180)

CEC_FILTER_CTRL	Bit	Description	Initial State
Filter_Cur_Val	[7]	Specifies the CEC filter current value bit. Indicates current value fed to CEC Tx, Rx. If the filter is enabled, this bit specifies the latest value on the CEC bus that is stable for more than Filter_Th cycles.	1
-	[6:1]	Reserved	6b000000
Filter_Enable	[0]	Specifies the CEC filter enable bit. 0 = Disables filter. Directly passes CEC input to CEC Tx, Rx. 1 = Enables filter. Filter propagates signals stable for more Filter_Th cycles.	1

10.3.6.65 Input Filtering Register (CEC_ FILTER_TH, R/W, Address = 0xE1B0_0184)

CEC_FILTER_TH	Bit	Description	Initial State
Filter_Th	[7:0]	Specifies the filter threshold value. If the filter is enabled, it filters out signals that are less stable than Filter_Th cycles.	8b00000011

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11 IMAGE ROTATOR

11.1 OVERVIEW OF IMAGE ROTATOR

Image Rotator performs rotating/flipping image data. It is composed of Rotate FSM, Rotate Buffer, AMBA 3.0 AXI master and APB slave interface, and Register files. Overall features are summarized as follows.

11.2 KEY FEATURES OF IMAGE ROTATOR

The features of image rotator include:

- Image format: YCbCr 4:2:2(interleave), YCbCr 4:2:0(non-interleave, 2-plane and 3-plane), RGB565 and RGB888 (unpacked)
- Rotate degree: 0, 90, 180, and 270 with flip vertical and flip horizontal
- Windows offset function
- Image size: up to 64K by 64K (The maximum sizes are different from the types of image format)
- Image size restriction: memory size shouldn't exceed 16-bit address size. For example, RGB888 has a size limitation up to 14-bit image size, only [13:0] is valid and [15:14] are ignored.

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11.3 BLOCK DIAGRAM OF IMAGE ROTATOR

The *Figure 11-1* shows the block diagram of Image Rotator.

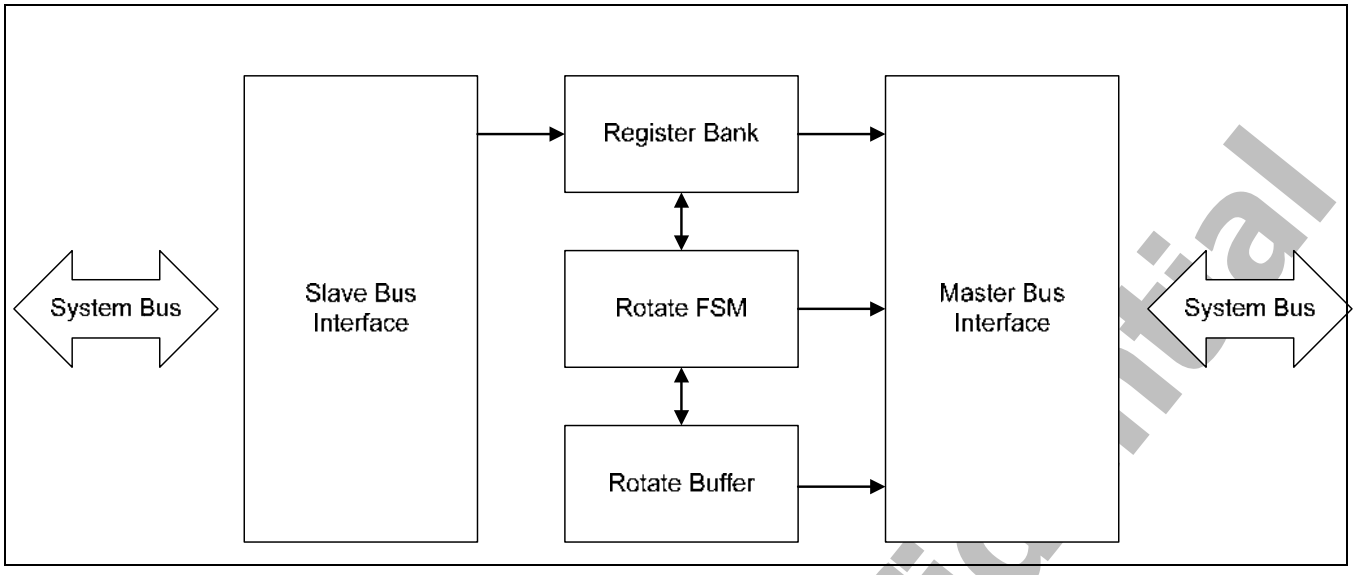

Figure 11-1 Image Rotator Block Diagram

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11.4 SUPPORTED IMAGE ROTATION FUNCTIONS

The *Figure 11-2* shows the rotation functions supported by Image Rotator.

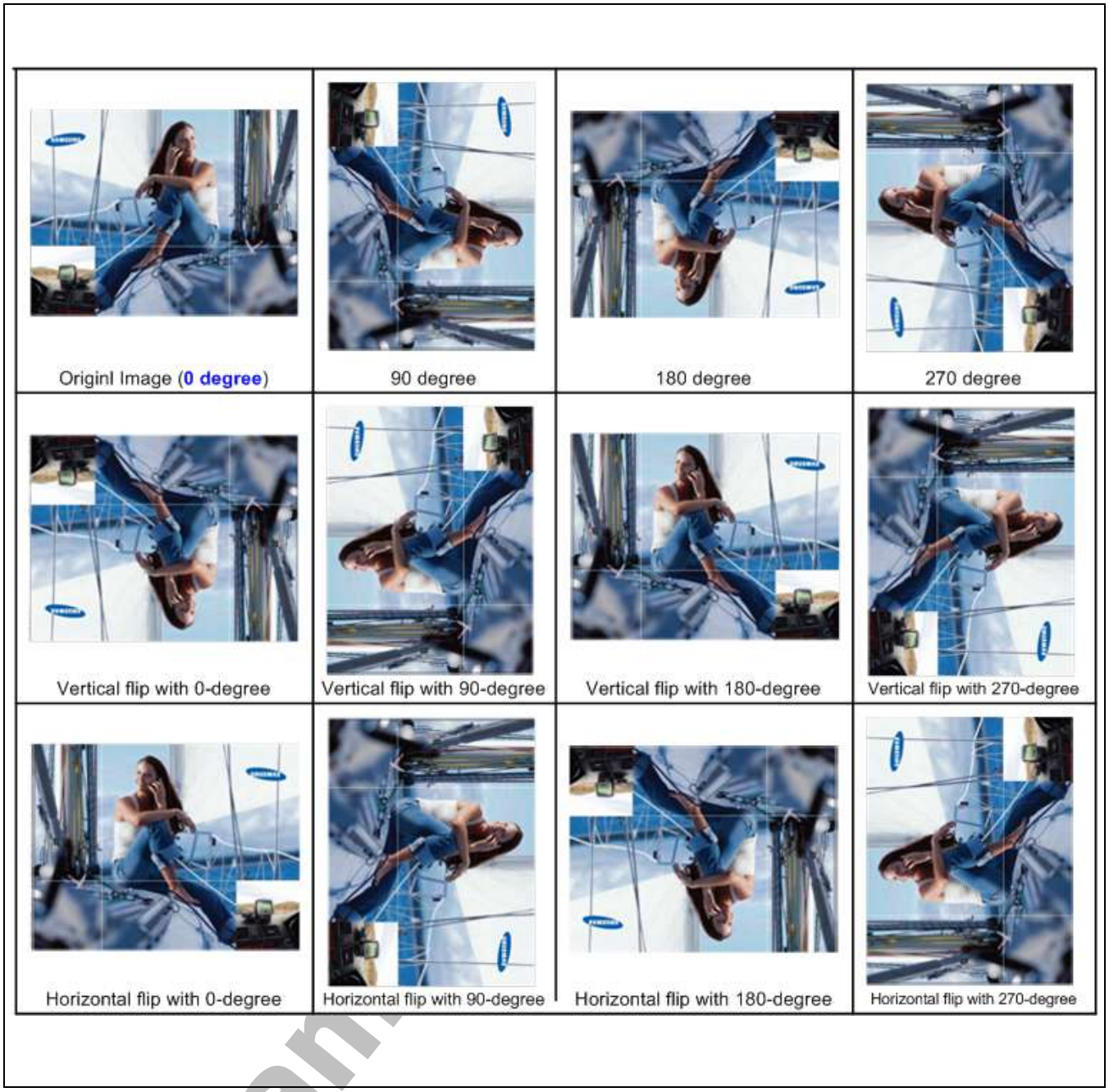

Figure 11-2 Ported Image Rotation Functions

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11.5 IMAGE ROTATION WITH WINDOWS OFFSET

Image rotator supports image rotation with window offset function. It is useful function to move from a small portion of a large image, to move in a portion of a large image.

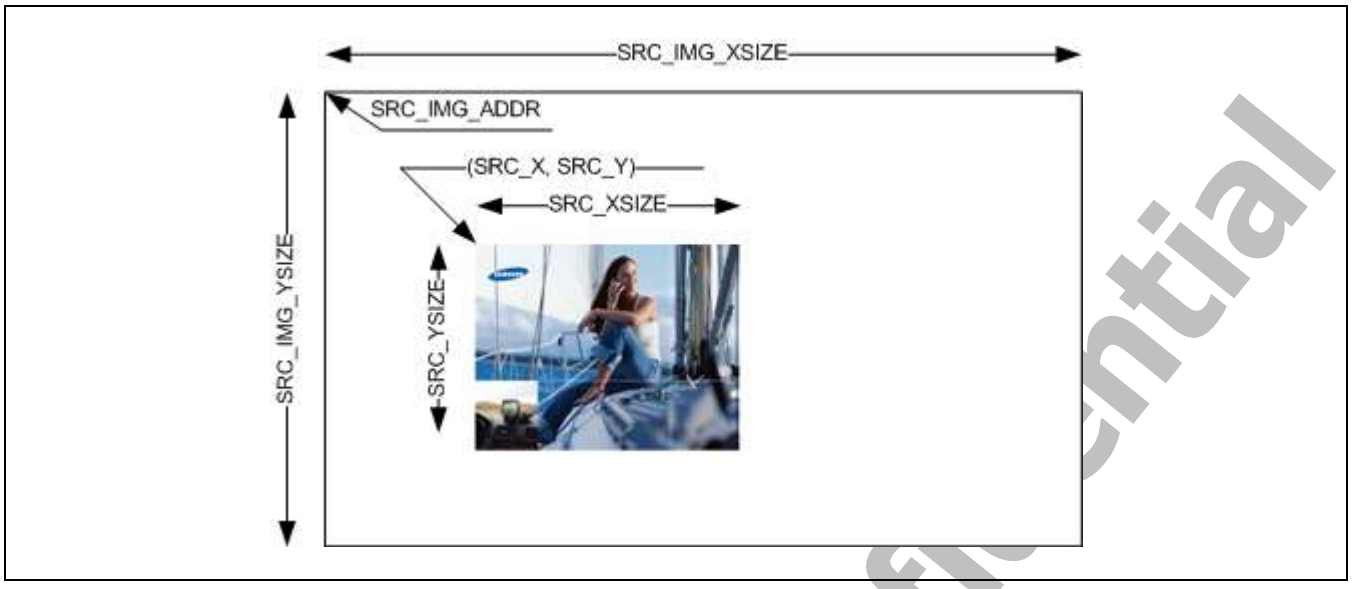

Figure 11-3 Source Image Example (with window offset function)

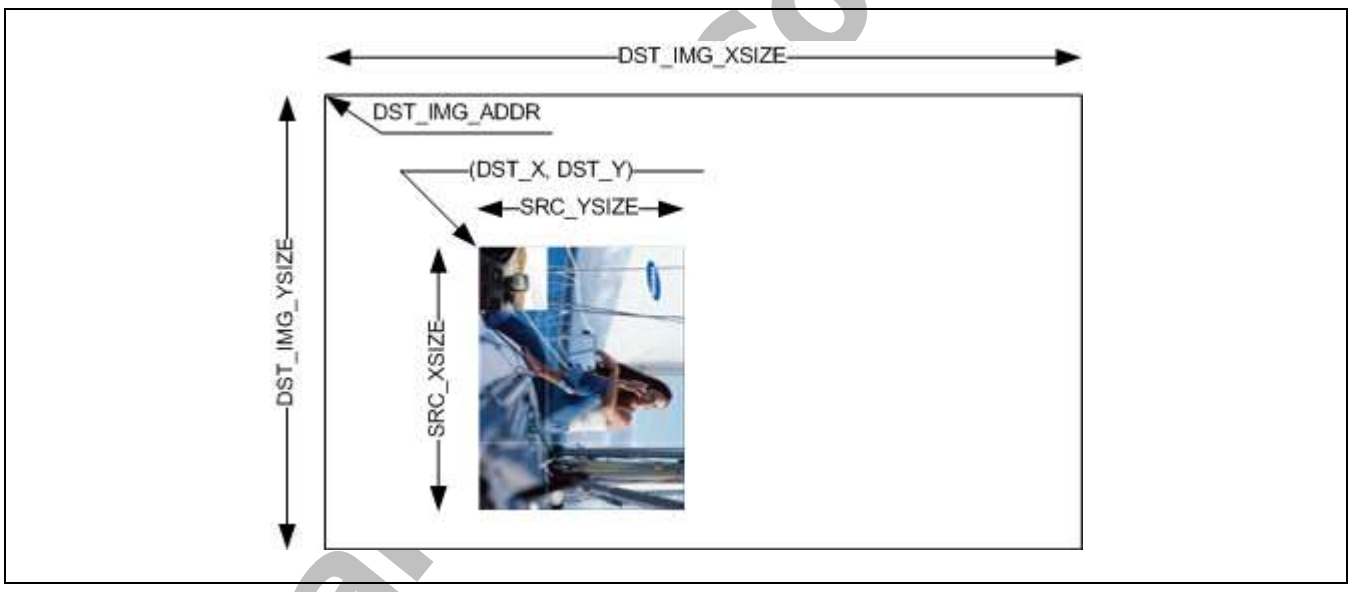

Figure 11-4 Destination Image Example (90 degree rotated with window offset function)

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11.6 PROGRAMMING GUIDE

11.6.1 RESISTER SETTING

All registers with CONTROL register except CONTROL [0] should set for proper operation previously, and User should set CONTROL [0] bit for starting image rotator.

11.6.2 RESTRICTIONS ON THE IMAGE SIZE

Image rotator has some restrictions on the image size. User should not violate these restrictions.

- Image base address:
  The bit [2:0] should be zero for the SRCADDRREG0/1/2 and DSTADDRREG0/1/2 registers.
- Image size: SRCIMGSIZE and DSTIMGSIZE should be set as follows,

Image Format	Minimum Size	Maximum Size
RGB888	8 x 8	16K x 16K
RGB565	16 x 16	32K x 32K
YCbCr422	16 x 16	32K x 32K
YCbCr420 2-Plane	32 x 32	64K x 64K (in case of Y components)
YCbCr420 3-Plane	64 x 32	64K x 64K (in case of Y components)

- Image coordinates to be rotated:
  SRC_XY and DST_XY should set as follows,

Image Formats	Image Size Restrictions
RGB888	X and Y pixel size should be multiple of 2.
RGB565	X and Y pixel size should be multiple of 4.
YCbCr422	X and Y pixel size should be multiple of 4.
YCbCr420 2-Plane	X and Y pixel size should be multiple of 8.
YCbCr420 3-Plane	X and Y pixel size should be multiple of 16.

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11.7 REGISTER DESCRIPTION

11.7.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
CONFIG	0xFA30_0000	R/W	Rotator Configuration	0x0000_0000
CONTROL	0xFA30_0010	R/W	Rotator Image0 Control	0x0000_0000
STATUS	0xFA30_0020	R	Rotator Status	0x0000_0000
SRCBASEADDR0	0xFA30_0030	R/W	Rotator Source Image Base Address	0x0000_0000
SRCBASEADDR1	0xFA30_0034	R/W	Rotator Source Image Base Address	0x0000_0000
SRCBASEADDR2	0xFA30_0038	R/W	Rotator Source Image Base Address	0x0000_0000
SRCIMGSIZE	0xFA30_003C	R/W	Rotator Source Image X, Y Size	0x0000_0000
SRC_XY	0xFA30_0040	R/W	Rotator Source Image X, Y Coordinates	0x0000_0000
SRCROTSIZE	0xFA30_0044	R/W	Rotator Source Image Rotation Size	0x0000_0000
DSTBASEADDR0	0xFA30_0050	R/W	Rotator Destination Image Base Address	0x0000_0000
DSTBASEADDR1	0xFA30_0054	R/W	Rotator Destination Image Base Address	0x0000_0000
DSTBASEADDR2	0xFA30_0058	R/W	Rotator Destination Image Base Address	0x0000_0000
DSTIMGSIZE	0xFA30_005C	R/W	Rotator Destination Image X, Y Size	0x0000_0000
DST_XY	0xFA30_0060	R/W	Rotator Destination Image X, Y Coordinates	0x0000_0000

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11.7.1.1 Rotator Configuration Register (CONFIG, R/W, Address= 0xFA30_0000)

CONFIG	Bit	Description	Initial State
Reserved	[31:9]	Reserved	000_0000b
Enable Interrupt	[9]	Interrupt enable to indicate illegally configured setting 0 = Disables interrupt 1 = Enables interrupt Note: In this case, rotator doesn't work.	1b
Enable Interrupt	[8]	Interrupt enable to indicate that a image rotation is finished 0 = Disables interrupt 1 = Enables interrupt	0b
Reserved	[7:0]	Reserved	0x00

11.7.1.2 Rotator Control Register (CONTROL, R/W, Address= 0xFA30_0010)

CONTROL	Bit	Description	Initial State
Reserved	[31:11]	Reserved	0x0000
Pattern Writing	[16]	Write pattern to fill a destination image with a designated pattern 0 = Disable pattern writing 1 = Enable pattern writing Note: if this bit set, the information of a source image is ignored.	0b
Reserved	[15:11]	Reserved	00000b
Input Image Format	[10:8]	Input image format to be rotated 000 = YCbCr 4:2:0(3-plane) 001 = YCbCr 4:2:0(2-plane) 010 = Reserved 011 = YCbCr 4:2:2 (interleave) 100 = RGB565 110 = RGB888 (Unpacked) 111 = Reverved	000b
Flip Direction	[7:6]	Flip direction 0x = No flip 10 = Flip vertical 11 = Flip horizontal	00b
Rotation Degree	[5:4]	Rotation degree 00 = 0 degree 01 = 90 degree 10 = 180 degree 11 = 270 degree	00b
Reserved	[3:1]	Reserved	000b
Start Rotate	[0]	Rotate enable signal. Whenever this bit set, Rotator starts the operation. This bit is cleared if rotator starts to move an image. 1 = Start rotate operation	0b

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11.7.1.3 Rotator Status Register (STATAUS, R, Address = 0xFA30_0020)

STATREG	Bit	Description	Initial State
Reserved	[31:10]	Reserved	0x00
Interrupt Pending	[9]	This bit is set if the SFR set illegally. Writing '1' makes this bit clear.	1b
Interrupt Pending	[8]	This bit is set if an image rotation is complete. Writing '1' makes this bit clear.	0b
Reserved	[3:1]	Reserved	0x00
Rotator status	[1:0]	These bits show the rotator operation status. 00 = IDLE status 01 = Reserved 10 = Rotating a image (BUSY) 11 = Rotating a image, and has one more job to rotate (BUSY)	00b

11.7.1.4 Rotator Source Image Base Address Register 0 (SRCBASEADDR0, R/W, Address = 0xFA30_0030)

SRCADDRREG0	Bit	Description	Initial State
SRC_IMG_ADDR	[31:0]	Base address of source image for RGB or Y component	0x0000_0000

11.7.1.5 Rotator Source Image Base Address Register 1 (SRCBASEADDR1, R/W, Address = 0xFA30_0034)

SRCADDRREG1	Bit	Description	Initial State
SRC_IMG_ADDR	[31:0]	Base Address of source image for Cb component.	0x0000_0000

11.7.1.6 Rotator Source Image Base Address Register 2 (SRCBASEADDR2, R/W, Address = 0xFA30_0038)

SRCADDRREG2	Bit	Description	Initial State
SRC_IMG_ADDR	[31:0]	Base Address of source image for Cr component.	0x0000_0000

11.7.1.7 Rotator Source Base Image Size Register (SRCIMGSIZE, R/W, Address = 0xFA30_003C)

SRCIMGSIZE	Bit	Description	Initial State
SRC_YSIZE	[31:16]	Vertical pixel size of a source image	0x0000
SRC_XSIZE	[15:0]	Horizontal pixel size of a source image	0x0000

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11.7.1.8 Rotator Source Image Coordinates Register (SRC_XY, R/W, Address = 0xFA30_0040)

SRC_XY	Bit	Description	Initial State
SRC_Y	[31:16]	The pixel coordinates on Y-axis of a image to be rotated	0x0000
SRC_X	[15:0]	The pixel coordinates on X-axis of a image to be rotated	0x0000

11.7.1.9 Rotator Source Base Rotation Size Register (SRCROTSIZE, R/W, Address = 0xFA30_0044)

SRCROTSIZE	Bit	Description	Initial State
SRC_YSIZE	[31:16]	Vertical pixel size of a image to be rotated	0x0000
SRC_XSIZE	[15:0]	Horizontal pixel size of a image to be rotated	0x0000

11.7.1.10 Rotator Destination Image Base Address Register 0 (DSTBASEADDR0, R/W, Address = 0xFA30_0050)

DSTBASEADDR0	Bit	Description	Initial State
DST_IMG_ADDR	[31:0]	Address of destination image for RGB or Y component.	0x0000_0000

11.7.1.11 Rotator Destination Image Base Address Register 1 (DSTBASEADDR1, R/W, Address = 0xFA30_0054)

DSTBASEADDR1	Bit	Description	Initial State
DST_IMG_ADDR	[31:0]	Address of destination image for CB component.	0x0000_0000

11.7.1.12 Rotator Destination Image Base Address Register 2 (DSTBASEADDR2, R/W, Address = 0xFA30_0058)

DSTBASEADDR2	Bit	Description	Initial State
DST_IMG_ADDR	[31:0]	Address of destination image for Cr component.	0x0000_0000

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11.7.1.13 Rotator Destination Base Image Size Register (DSTIMGSIZE, R/W, Address = 0xFA30_005C)

DSTIMGSIZE	Bit	Description	Initial State
DST_YSIZE	[31:16]	Vertical pixel size of a target image	0x0000
DST_XSIZE	[15:0]	Horizontal pixel size of a target image	0x0000

11.7.1.14 Rotator Destination Image Coordinates Register (DST_XY, R/W, Address = 0xFA30_0060)

DST_XY	Bit	Description	Initial State
DST_Y	[31:16]	The pixel coordinates on Y-axis of a image to be rotated	0x0000
DST_X	[15:0]	The pixel coordinates on X-axis of a image to be rotated	0x0000

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12 JPEG

12.1 OVERVIEW OF JPEG CODEC

JPEG codec compresses the original raw image and decompress the JPEG encoded image. It performs all functions required for image compression/ decompression such as Discrete Cosine Transform (DCT), Quantization and Huffman coding. It comprises of control circuit, DCT/Quantization, Huffman codec, marker process block and AHB interface control as shown in *Figure 12-1*. It is possible to set the operation modes and conditions such as the Huffman table number and restart interval value into internal control registers.

12.2 KEY FEATURES OF JPEG CODEC

- Compression/ decompression up to 8192x8192
- Minimum Image size for compression/decompression is 32x32
- Supports following format of compression (Refer to figure 9.13-1)
  - Input raw image: YCbCr4:2:2 or RGB565
  - Output JPEG file: Baseline JPEG of YCbCr4:2:2 or YCbCr4:2:0
  - Supports following format of decompression
  - Input JPEG file: Baseline JPEG of YCbCr4:4:4, YCbCr4:2:2, YCbCr4:2:0, gray
  - Output raw image: YCbCr4:2:2 or YCbCr4:2:0
- Supports general-purpose color-space converter
- Support Baseline JPEG. (Progressive mode does not operate.)

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12.3 BLOCK DIAGRAM OF JPEG CODEC

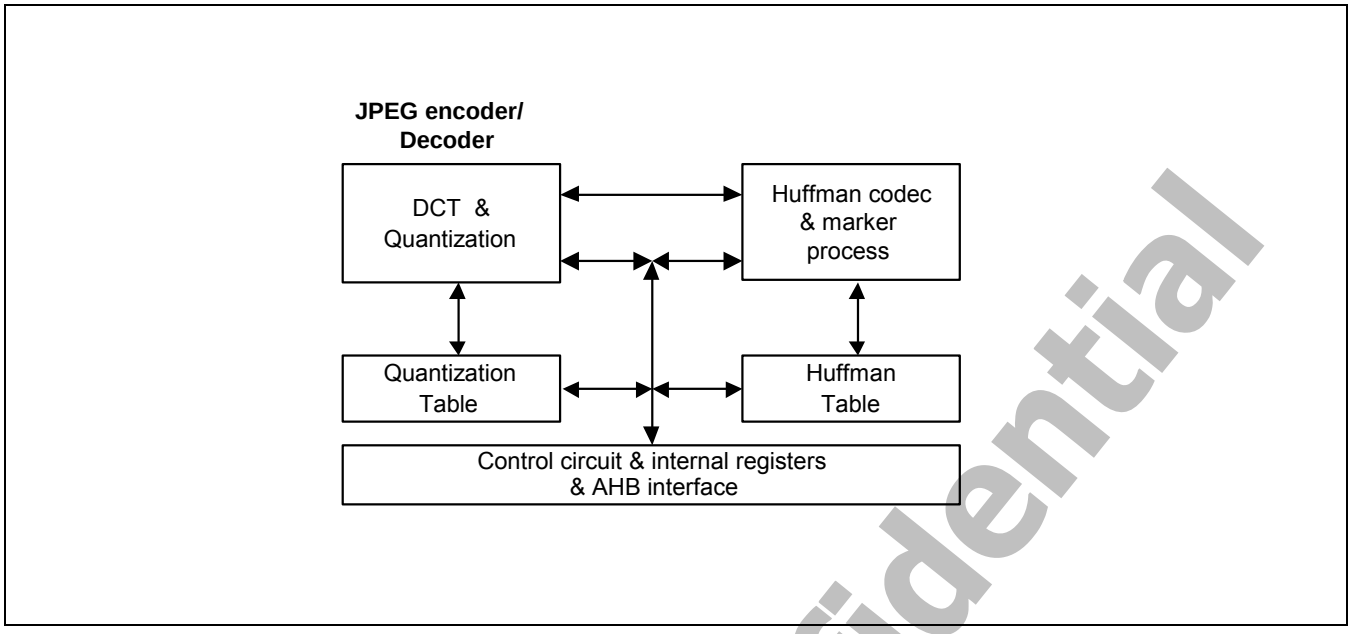

Figure 12-1 JPEG

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12.4 BLOCK DIAGRAM IN/OUT DATA FORMAT

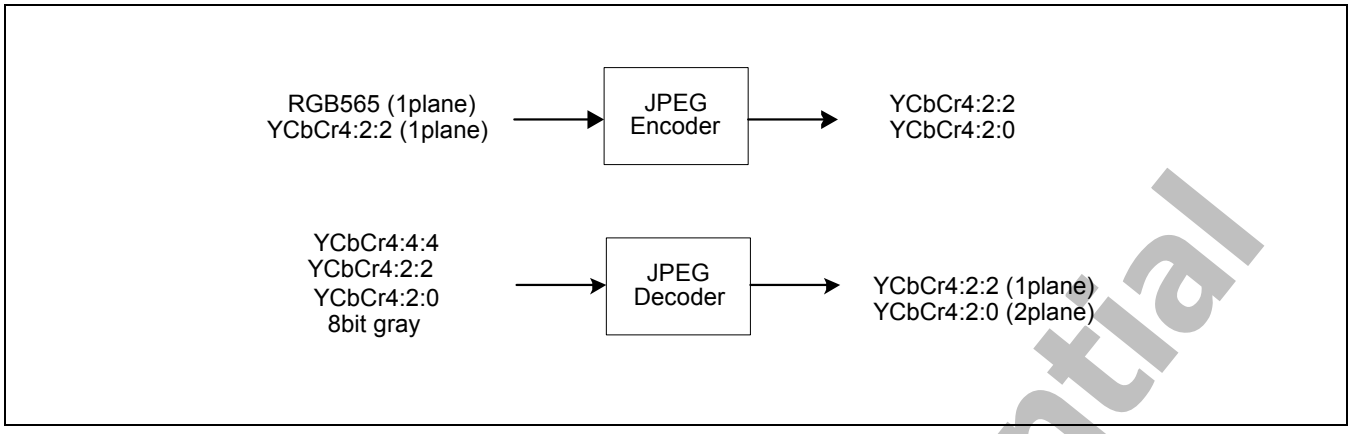

Figure 12-2 JPEG In/Output Data Format

12.4.1 CONTROL CIRCUIT AND AHB INTERFACE

This block sets and initializes the operation mode with internal registers. Use this register to set the operation modes and conditions such as Huffman table number and restart interval value.

12.4.2 DCT/ QUANTIZATION

During compression, it transforms 8x8 image data to DCT coefficients. Then the quantization process is performed over DCT coefficients by utilizing the quantization tables. During decompression, dequantization is done and then a DCT coefficient is transformed into image data.

12.4.3 HUFFMAN CODER AND MARKER PROCESS

During compression, Huffman encoding is performed based on the Huffman table and marker process generates the JPEG bit stream. During decompression, marker process parses a JPEG file and Huffman decoding is done.

12.4.4 QUANTIZATION TABLE

It is the place to store quantization tables.

12.4.5 HUFFMAN TABLE

It is the place to store Huffman tables.

12.4.6 PERFORMANCE

JPEG IP supports compression/ decompression of image file with size up to 8192x8192.
Supported minimum size is 32x32.

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12.5 DESCRIPTION OF SUPPORTED COLOR FORMAT

JPEG supports several color formats during compression/ decompression.

12.5.1 IN COMPRESSION MODE

Before compression starts, raw image data must be in main memory. The raw image data address is specified in IMGADR register. The raw images are stored in interleaved YCbCr4:2:2 or RGB565 color format as shown in *Figure 12-3*. After compression is complete, result file is baseline JPEG in YCbCr4:2:0 or YCbCr4:2:2 format with interleaved scan. Therefore color space conversion (RGB→YCbCr) and decimation of chrominance component is necessary. JPEG IP has its own color space converter. COEF1, COEF2 and COEF3 register sets the coefficients of color space converter. Decimation of JPEG IP is downsampling process. For example, decimation from YCbCr4:2:2 to YCbCr4:2:0 needs 2:1 vertical downsampling for Cb and Cr component as shown in *Figure 12-4*.

12.5.2 IN DECOMPRESSION MODE

In decompression mode, input file is baseline JPEG in YCbCr4:4:4, YCbCr4:2:2, YCbCr4:2:0, gray with interleaved scan and output raw image has interleaved YCbCr4:2:2 or YCbCr4:2:0 formats. Therefore for input file with YCbCr format, decimation and interpolation process is done during decompression. In this case, decimation is same as downsampling and interpolation is sample-and-hold (repetition of recent value) process. Each operation is described in *Figure 12-3.* The result of gray format JPEG file input is YCbCr4:2:2 or YCbCr4:2:0 raw images. This raw images have Y component, which is result of decompression, and Cb and Cr component with "128" value.

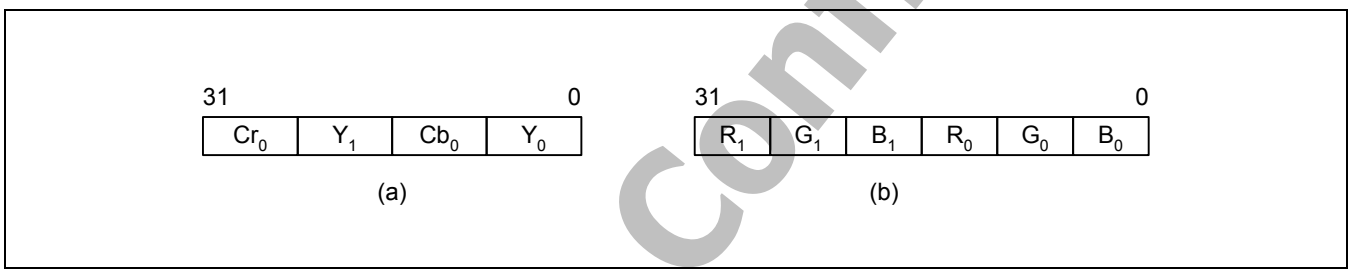

Figure 12-3 Raw Image Format in Memory (a) YCbCr4:2:2 (b) RGB5:6:5

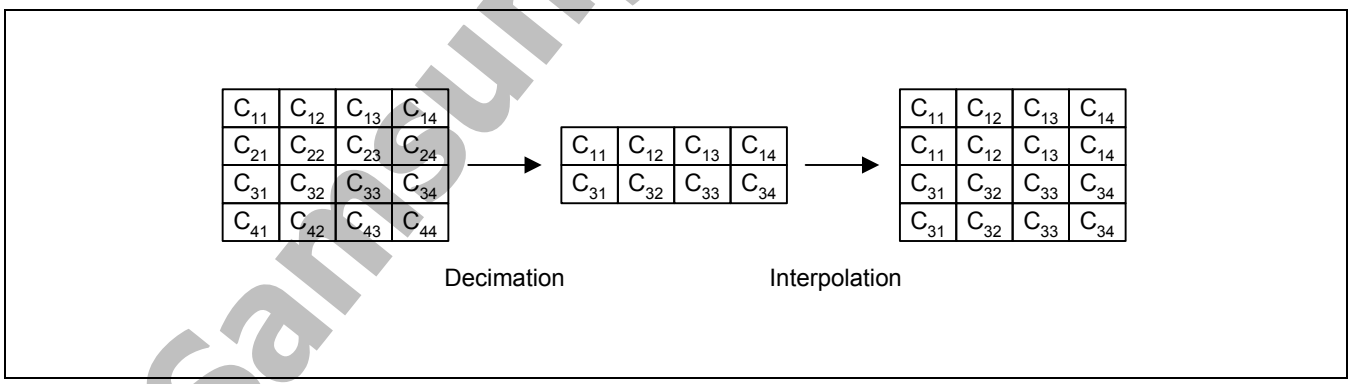

Figure 12-4 Decimation and 1:2 Interpolation in Vertical Direction

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Figure 12-5 illustrates the input format of YCbCr4:2:2. This JPEG codec supports type (a).

If input YCbCr4:2:2 format is type (b), decoder does not work.

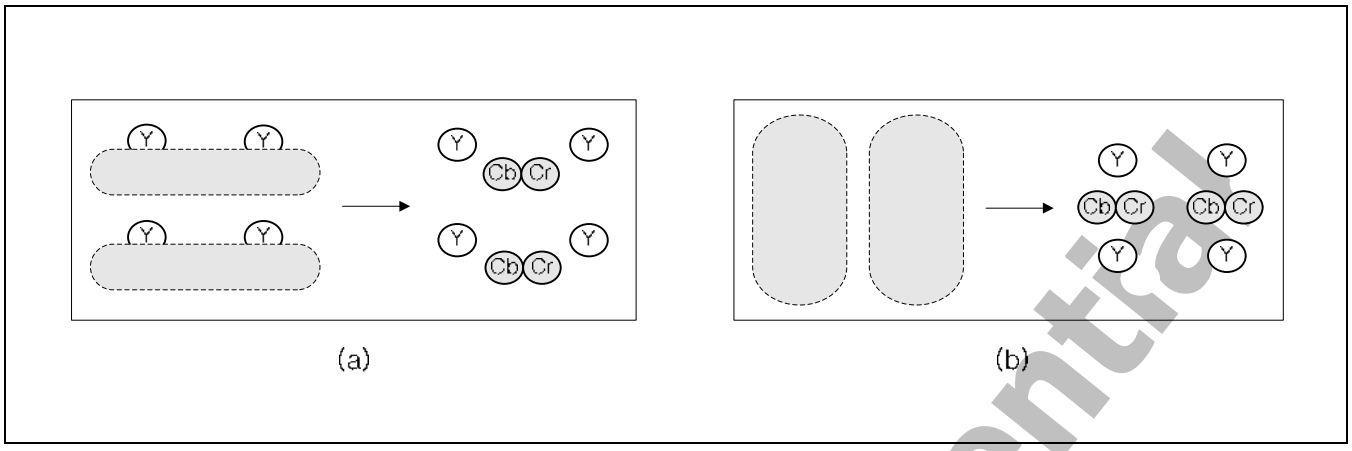

Figure 12-5 YCbCr4:2:2 Color Format

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12.6 PROCESS

12.6.1 REGISTER ACCESS

The registers are modified:

After reset, until a new job starts, or

After the generation of the process completion interruption signal, until a new job starts.
Other conditions indicate that the core is in the normal operation, thus, register modification is not allowed.

12.6.2 TABLE ACCESS

Four Huffman tables (AC & DC, 2 tables for each) and four quantization tables must be configured before compression. To set any quantization table and Huffman table, first access the corresponding table entry register. Then write transfers should follow. To understand the write transfer, refer to *Figure 12-6*. The access order for each table is shown below.

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64

Figure 12-6 Access Order in Quantizer Table

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12.6.3 STARTING PROCESS

Process start signal from the scheduler instructs to start compression or decompression process of one picture after setting various registers. After getting the start signal, the core processing starts and then JPGOPR register is read as 1. Operation cannot be guaranteed if the start signal is issued again during processing.

Table 12-1 Registers that Must be Configured Before Compression

Registers	Description	At comp	At Decomp
JPGMOD	Process Mode Register	Essential	Essential
QTBL	Quantization Table Number Register	Essential	--
JPGDRI_U	Reset Interval Registers (upper 8bit)	Essential	--
JPGDRI_L	Reset Interval Registers (lower 8bit)	Essential	
JPGY_U	Vertical Size Register (upper 8bit)	Essential	
JPGY_L	Vertical Size Register (lower 8bit)	Essential	
JPGX_U	Horizontal Size Register (upper 8bit)	Essential	
JPGX_L	Horizontal Size Register (lower 8bit)	Essential	
QTBL0	Quantizer Table0 Entries Register.	Essential	--
QTBL1	Quantizer Table1 Entry Register	Essential	--
QTBL2	Quantizer Table2 Entry Register	Essential	--
QTBL3	Quantizer Table3 Entry Register	Essential	--
OUTFORM	Output Color Format of Decompression	--	Essential
ENC_STREAM_INTSE	Compressed Stream Size Interrupt Setting Register	Essential	--
HDTBL0, HDCTBLG0	DC Huffman Table0 Entry Register	Essential	--
HACTBL0, HACTBLG0	AC Huffman Table0 Entry Register	Essential	--
HDCTBL1, HDCTBLG1	DC Huffman Table1 Entry Register	Essential	--
HACTBL1, HACTBLG1	AC Huffman Table1 Entry Register	Essential	--

Contents of registers in *Table 12-1* will be changed in following cases.

1. After user writes the registers again.
2. After reset operation is done.
3. After decompression of arbitrary JPEG file. In this case, the registers have the value from header of input JPEG file after header parsing process.

Except in the above cases, it is possible to process next picture by only performing the process start signal after process of a picture is completed.

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12.6.4 PROCESS FOR IMAGE SIZE

Size of images in JPEG file has to be a specific value, which is the multiple of block size because JPEG file is composed of blocks. If image size in JPEG file header is not multiple of block size, actual image size in the file is the minimum among values which are the multiple of the block size and larger than the value in the header, but decoder shows cropped image with the size in file header. Minimum size for compression and decompression process is double of Block Size. Color format determines the block size as described in *Table 12-2.*

Table 12-2 Relationship between Block Size and Color Format

Color format	MCU Block size (WxH)	Minimum size
YCbCr4:4:4	8x8	16x8 or 8x16
YCbCr4:2:2	16x8	32x8 or 16x16
YCbCr4:2:0	16x16	32x16 or 16x32
Gray (Y only)	8x8	16x8 or 8x16

1. Decompression
   Input JPEG file has information about color format, width and height of the image in the frame header. User knows the information about the JPEG file after header parsing process. Actual raw image size after decompression is the minimum among the values which are the multiple of block size (known from color format) and larger than or equal to the image size in the header. For example, if JPEG file is YCbCr4:2:0 format and its size is 170x170, actual size of decompressed raw image is 176x176.

2. Proper process such as cropping is needed to display or store the result raw image in the width and height of the file header.

3. Compression
   Width and height of input raw image must be the multiple of the block size corresponding to the output JPEG color format. If input raw image has arbitrary size, use padding process to modify the size to the multiple of block size. The modified size is the minimum values which are the multiple of the block size and larger than or equal to the original value. However, register setting value of width and height for compression must be the original value.

12.6.5 PROCESS FOR INPUT STREAM SIZE

For decompression of an illegal JPEG stream, JPEG core does not recognize the end of the stream if some important markers are damaged. Therefore, it is necessary to notify the input stream size to JPEG core.

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12.6.6 INTERRUPT SIGNAL

Interrupt signal is generated under the following conditions, and the JPGINTST register identifies causes:

1. Compression or decompression process for one picture is complete,
2. Internal timer counting ends before completion of compression or decompression.
3. During compression, the byte size of output stream is larger than the predefined bound size in ENC_STREAM_BOUND.

In condition 1, the normal process is finished. To clear the interrupt request, read the JPGINTST register and JPGOPR register. If there is no encoding or decoding error, JPGINTST must be read as 0x40. If another value is read, the operation result may not be correct.

In condition 2, TIMER_INT_STAT is read as 1 and it is cleared by writing 1 in TIMER_INT_STAT register. In this case, JPEG requires reset or S/W reset before next operation.

In condition 3, ENC_STREAM_INT_STAT is read as 1, JPEG operation is stopped and there is no further memory access by JPEG. This interrupt is cleared by writing 1 in ENC_STREAM_INT_STAT register. In this case, JPEG needs reset or S/W reset before next operation.

12.6.7 INTERRUPT SETTING

If this JPGINTSE register is set, it invokes the interrupt when the input file for decompression is illegal.

To enable timer interrupt, set TIMER_INT_EN to 1 before start or restart.

To deal with an illegal input jpeg file for decompression, set RSTm_INT_EN , DATA_NUM_INT_EN or FINAL MCU_NUM_INT_EN.

To enable compressed stream size interrupt, set ENC_STREAM_INT_EN to 1 before starting compression.

12.6.8 S/W RESET

JPEG IP has a register for S/W reset. Steps to perform S/W reset:

1. Set 1 in the SW_RESET register.
2. Wait until SW_RESET register value changes to 0.
3. After the value changes to 0, set the proper register for next operation and start the operation.

If JPEG core is terminated abnormally or holds operation, S/W reset is needed to start new operation.

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12.6.9 MARKER PROCESS

The following markers are generated during compression.

Table 12-3 Markers in JPEG Codec

Marker	Codes (hex)	Description
SOI	FFD8	Start of image
SOF0	FFC0	Baseline JPEG
SOS	FFDA	Start of scan
DQT	FFDB	Define quantization table
DHT	FFC4	Define Huffman table
DRI	FFDD	Define restart interval
RSTm	FFD0~FFD7	Restart with module 8 count “m”
EOI	FFD9	End of image

The markers *Table 12-3* are subject to process during decompression. The other markers except SOF1~SOFF and JPG are ignored.

12.6.10 BITSTREAM OF COMPRESSED FILE

The created JPEG bit stream is shown in *Figure 12-7*. In the figure, ECS is an acronym of ‘entropy-coded segment’, which is a sequence of entropy-coded bytes.

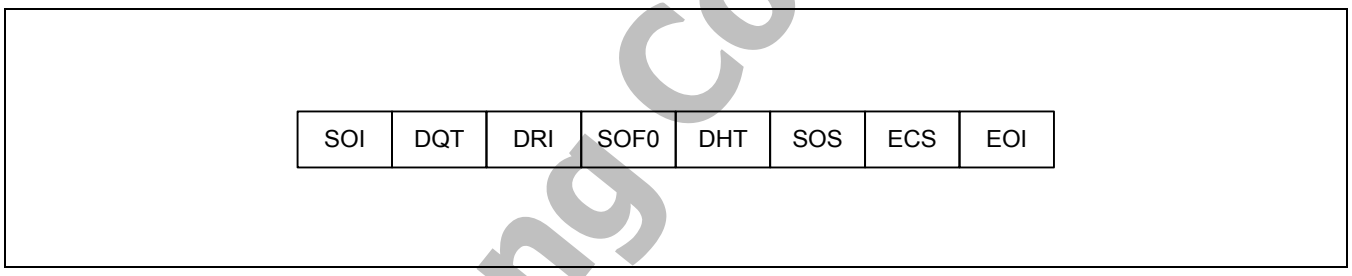

Figure 12-7 Bitstream of Compressed File

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12.6.11 JPEG COMPRESSION FLOW

This is a pseudo instruction set that indicates the write or read on specific registers. It is assumed that the Huffman and quantization tables were written already.

```
// JPEG encoder initialization

Write SW_RESET      0x1
Write JPGCLKCON     0x1
Write JPGCMOD       0x20          // Mode selection
Write JPGMOD        0x1           // Encoding and YCbCr4:2:2
Write JPGDRI        0x0           // No DRI if 0. Set an appropriate value.
Write QTBL          0x0           // Choose the appropriate table index for Huffman & Quantization
tables.
Write JPGY_U        0x0           // Vertical resolution Upper byte
Write JPGY_L        0x0           // Vertical resolution Lower byte
Write JPGX_U        0x0           // Horizontal resolution Upper byte
Write JPGX_L        0x0           // Horizontal resolution Lower byte
Write IMGADR        0x1000_0000   // Address for an image to compress
Write JPGADR        0x1001_0000   // Address for the compressed JPEG file
Write COEF1         0x4D_971E     // Color converter coefficients
Write COEF2         0x2c_5783     // Color converter coefficients
Write COEF3         0x83_6e13     // Color converter coefficients

// Encoding start.

Write JSTART        0x1

// After interrupt is detected, clear the pending register

Read JPGCNT_U                     // Read the file size in bytes
Read JPGCNT_M                     // Read the file size in bytes
Read JPGCNT_L                     // Read the file size in bytes
Read JPGINTST                     // It must be read 0x40.

Write JPGCOM        0x4           // Clear interrupt

Read JPGOPR                       // It must be read zero.
```

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12.6.12 JPEG DECOMPRESSION FLOW

This is a pseudo instruction set that indicates the write or read on specific registers.

```
// JPEG decoder initialization
Write SW_RESET          0x1
Write JPGCLKCON         0x1
Write JPGMOD            0x8          // Decoding mode
Write JPGINTSE          0x0          // Interrupt setting
Write OUTFORM           0x1          // Output raw image is YCbCr4:2:0
Write IMGADR            0x1000_0000  // Address for a decompressed raw image
Write JPGADR            0x1001_0000  // Address for a JPEG file to decompress
// Decoding operation start
Write JSTART            0x1
// After interrupt is detected, clear the pending register
Read JPGINTST                        // It must be read 0x40.(it means normal end)
Write JPGCOM            0x4          // Clear interrupt
Read JPGOPR                          // It must be read 0x0.
```

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12.7 REGISTER DESCRIPTION

12.7.1 REGISTER MAP

JPEG has the control registers as shown in *Table 12-4* and table assignment in *Table 12-6*.

Table 12-4 JPEG Codec Control Registers

Register	Address	R/W	Description	Reset Value
JPGMOD	0xFB60_0000	R/W	Specifies the Sub-sampling mode register	0x0000_0000
JPGOPR	0xFB60_0004	R	Specifies the operation status register	0x0000_0000
QTBL	0xFB60_0008	R/W	Specifies the Quantization Table Number Register	0x0000_0000
HTBL	0xFB60_000C	R/W	Specifies the Huffman table number register	0x0000_0000
JPGDRI_U	0xFB60_0010	R/W	Specifies the MCU, which inserts RST marker(upper 8-bit)	0x0000_0000
JPGDRI_L	0xFB60_0014	R/W	Specifies the MCU, which inserts RST marker (lower 8-bit)	0x0000_0000
JPGY_U	0xFB60_0018	R/W	Specifies the vertical resolution (upper 8-bit)	0x0000_0000
JPGY_L	0xFB60_001C	R/W	Specifies the vertical resolution (lower 8-bit)	0x0000_0000
JPGX_U	0xFB60_0020	R/W	Specifies the Horizontal resolution (upper 8-bit)	0x0000_0000
JPGX_L	0xFB60_0024	R/W	Specifies the Horizontal resolution (lower 8-bit)	0x0000_0000
JPGCNT_U	0xFB60_0028	R	Specifies the amount of the compressed data in bytes (upper 8-bit)	0x0000_0000
JPGCNT_M	0xFB60_002C	R	Specifies the amount of the compressed data in bytes (middle 8-bit)	0x0000_0000
JPGCNT_L	0xFB60_0030	R	Specifies the amount of the compressed data in bytes (lower 8-bit)	0x0000_0000
JPGINTSE	0xFB60_0034	R/W	Specifies the Interrupt Setting Register	0x0000_0000
JPGINTST	0xFB60_0038	R	Specifies the Interrupt Status Register	0x0000_0000
Reserved	0xFB60_003C ……. 0xFB60_0048	-	-	-
JPGCOM	0xFB60_004C	W	Specifies the command register	0x0000_0000
IMGADR	0xFB60_0050	R/W	Specifies the source or destination image address	0x0000_0000
Reserved	0xFB60_0054	-	-	-
JPGADR	0xFB60_0058	R/W	Specifies the source or destination JPEG file address	0x0000_0000

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Register	Address	R/W	Description	Reset Value
COEF1	0xFB60_005C	R/W	Specifies the coefficient values for RGB ↔ YCbCr Converter	0x0000_0000
COEF2	0xFB60_0060	R/W	Specifies the coefficient values for RGB ↔ YCbCr Converter	0x0000_0000
COEF3	0xFB60_0064	R/W	Specifies the coefficient values for RGB ↔ YCbCr converter	0x0000_0000
JPGCMOD	0xFB60_0068	R/W	Specifies the Mode Selection and Core Clock Setting	0x0000_0020
JPGCLKCON	0xFB60_006C	R/W	Specifies the Power On/ Off and clock down control	0x0000_0002
JSTART	0xFB60_0070	W	Specifies the start compression or decompression	0x0000_0000
Reserved	0xFB60_0074	W		0x0000_0000
SW_RESET	0xFB60_0078	R/W	Specifies the S/W reset	0x0000_0000
TIMER_SE	0xFB60_007C	R/W	Specifies the internal timer setting register	0x7FFF_FFFF
TIMER_ST	0xFB60_0080	R/W	Specifies the internal timer status register	0x7FFF_FFFF
COMSTAT	0xFB60_0084	R	Specifies the command status register	0x0000_0000
OUTFORM	0xFB60_0088	R/W	Specifies the output color format of decompression	0x0000_0000
VERSION	0xFB60_008C	R	Specifies the version register	0x0000_0003
Reserved	0xFB60_0090	-	-	-
ENC_STREAM_INTSE	0xFB60_0098	R/W	Specifies the compressed stream size interrupt setting register	0x00FF_FFE0
ENC_STREAM_INTST	0xFB60_009C	R/W	Specifies the compressed stream size interrupt status register	0x0000_0000
QTBL0	0xFB60_0400 ……. 0xFB60_04FC	R/W	Specifies the quantization table 0	0x0000_0000
QTBL1	0xFB60_0500 ……. 0xFB60_05FC	R/W	Specifies the quantization table 1	0x0000_0000
QTBL2	0xFB60_0600 ……. 0xFB60_06FC	R/W	Specifies the quantization table 2	0x0000_0000
QTBL3	0xFB60_0700 ……. 0xFB60_07FC	R/W	Specifies the quantization table 3	0x0000_0000
HDCTBL0	0xFB60_0800 ……. 0xFB60_083C	W	Specifies the Huffman DC Table 0 - the number of code per code length	0x0000_0000

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Register	Address	R/W	Description	Reset Value
HDCTBLG0	0xFB60_0840 ……. 0xFB60_086C	W	Specifies the Huffman DC Table 0 - Group number of the order for occurrence	0x0000_0000
HACTBL0	0xFB60_0880 ……. 0xFB60_08BC	W	Specifies the Huffman AC Table 0 - the number of code per code length	0x0000_0000
HACTBLG0	0xFB60_08C0 ……. 0xFB60_0B44	W	Specifies the Huffman AC Table 0 - Group number of the order for occurrence	0x0000_0000
HDCTBL1	0xFB60_0C00 ……. 0xFB60_0C3C	W	Specifies the Huffman DC Table 1 - the number of code per code length	0x0000_0000
HDCTBLG1	0xFB60_0C40 ……. 0xFB60_0C6C	W	Specifies the Huffman DC Table 1 - Group number of the order for occurrence	0x0000_0000
HACTBL1	0xFB60_0C80 ……. 0xFB60_0CBC	W	Specifies the Huffman AC Table 1 - the number of code per code length	0x0000_0000
HACTBLG1	0xFB60_0CC0 ……. 0xFB60_0F44	W	Specifies the Huffman AC Table 1 - Group number of the order for occurrence	0x0000_0000

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12.7.1.1 JPEG Mode Register (JPGMOD, R/W, Address = 0xFB60_0000)

JPGMOD	Bit	Description	Initial State
Reserved	[31:4]	Reserved but it should be 0x0	0
PROC_MODE	[3]	Process mode. 0 = Compression process. 1 = Decompression process.	0
SUBSAMPLING_MODE	[2:0]	Sub sampling mode 0x0 = chroma 4:4:4 format 0x1 = chroma 4:2:2 format. 0x2 = chroma 4:2:0 format 0x3 = Gray format (Single Component) Others are reserved. During decompression, these are read-only. During compression, only 0x1 or 0x2 are allowed.	0

12.7.1.2 JPEG Operation Status Register (JPGOPR, R, Address = 0xFB60_0004)

JPGOPR	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
JPGOPR	[0]	0 = JPEG is not operating. 1 = JPEG is operating.	0

12.7.1.3 Quantization Table Number Register (QTBL, R/W, Address = 0xFB60_0008)

QTBL	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
QT_NUM4	[7:6]	Quantization table number for 4^{th} component.	0
QT_NUM3	[5:4]	Quantization table number for 3^{nd} component.	0
QT_NUM2	[3:2]	Quantization table number for 2^{nd} component	0
QT_NUM1	[1:0]	Quantization table number for 1^{st} component.	0

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12.7.1.4 Huffman Table Number Register (HTBL, R/W, Address = 0xFB60_000C)

HTBL	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
HT_NUM4_AC	[7]	Huffman table number for 4th color component AC	0
HT_NUM4_DC	[6]	Huffman table number for 4th color component DC.	0
HT_NUM3_AC	[5]	Huffman table number for 3rd color component AC.	0
HT_NUM3_DC	[4]	Huffman table number for 3rd color component DC.	0
HT_NUM2_AC	[3]	Huffman table number for 2nd color component AC.	0
HT_NUM2_DC	[2]	Huffman table number for 2nd color component DC.	0
HT_NUM1_AC	[1]	Huffman table number for 1st color component AC.	0
HT_NUM1_DC	[0]	Huffman table number for 1st color component DC.	0

12.7.1.5 JPEG Restart Interval Upper byte Register (JPGDRI_U, R/W, Address = 0xFB60_0010)

JPGDRI_U	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
JPGDRI_U	[7:0]	This is a restart interval that identifies the distance between two adjacent Restart Maker (RST) in terms of Minimum Coded Unit (MCU). It is valid in compression mode. If JPGDRI is set to 0, Define Restart Interval Marker (DRI) and RST is not inserted.	0

12.7.1.6 JPEG Restart Interval Lower byte Register (JPGDRI_L, R/W, Address = 0xFB60_0014)

JPGDRI_L	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
JPGDRI_L	[7:0]	It is a restart interval that identifies the distance between two adjacent Restart Maker (RST) in terms of Minimum Coded Unit (MCU). It is valid in compression mode. If JPGDRI is set to 0, Define Restart Interval Marker (DRI) and RST is not inserted.	0

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12.7.1.7 JPEG Vertical Resolution Upper byte Register (JPGY_U, R/W, Address = 0xFB60_0018)

JPGY_U	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
VER_RES	[15:0]	Upper byte of the Image size value in the vertical direction. You are not allowed to Set 0. This register is read-only during decompression.	0

12.7.1.8 JPEG Vertical Resolution Lower byte Register (JPGY_L, R/W, Address = 0xFB60_001C)

JPGY_L	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
VER_RES	[15:0]	Lower byte of the Image size value in the vertical direction. You are not allowed to Set 0. This register is read-only during decompression.	0

12.7.1.9 JPEG Horizontal Resolution Upper byte Register (JPGX_U, R/W, Address = 0xFB60_0020)

JPGX_U	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
HOR_RES	[15:0]	Upper byte of the Image size value in the horizontal direction. You are not allowed to Set 0. This register is read-only during decompression.	0

12.7.1.10 JPEG Horizontal Resolution Lower byte Register (JPGX_L, R/W, Address = 0xFB60_0024)

JPGX_L	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0
HOR_RES	[15:0]	Lower byte of the Image size value in the horizontal direction. You are not allowed to Set 0. This register is read-only during decompression.	0

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12.7.1.11 JPEG Byte Count Upper byte Register (JPGCNT_U, R, Address = 0xFB60_0028)

JPGCNT_U	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
BYTE_CNT	[23:0]	Upper byte of the count value the width of 24bits of the amount of compression data. Value of the register will be clear when processing starts. This register is valid in compression mode.	0x00_0000

12.7.1.12 JPEG Byte Count Middle byte Register (JPGCNT_M, R, Address = 0xFB60_002C)

JPGCNT_M	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
BYTE_CNT	[23:0]	Middle byte of the count value the width of 24bits of the amount of compression data. Value of the register will be clear when processing starts. This register is valid in compression mode.	0x00_0000

12.7.1.13 JPEG Byte Count Lower byte Register (JPGCNT_L, R, Address = 0xFB60_0030)

JPGCNT_L	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
BYTE_CNT	[23:0]	Lower byte of the count value the width of 24bits of the amount of compression data. Value of the register will be clear when processing starts. This register is valid in compression mode.	0x00_0000

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12.7.1.14 JPEG Interrupt Setting Register (JPGINTSE, R/W, Address = 0xFB60_0034)

JPGINTSE	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
RSTm_INT_EN	[7]	The bit which decides whether interrupt is allowed or not, in case there is abnormality in restart interval period, data number in Huffman coding segments during decompression process. In case it is not set, error code will not be returned.	0
DATA_NUM_INT_EN	[6]	The bit which decides whether interrupt is allowed or not, in case there is abnormality in total data number in Huffman coding segments at decompression process. In case it is not set, error code will not be returned.	0
FINAL_MCU_NUM_INT_EN	[5]	The bit which decides whether interrupt is allowed or not, in case there is abnormality in final MCU data number in Huffman coding segments at decompression process. In case it is not set, error code will not be returned.	0
Reserved	[4:0]	Reserved, but should be 0x0	0

12.7.1.15 JPEG Interrupt Status Register (JPGINTST, R, Address = 0xFB60_0038)

JPGINTST	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
RESULT_STAT	[6]	Result status. 0 = Processing was finished abnormally. 1 = Processing was done normally	0
STREAM_STAT	[5]	Bitstream error status. Valid during decompression only. 0 = There is no syntax error on the compressed file. 1 = There is syntax error on the compressed file.	0
Reserved	[4:0]	Reserved	0

12.7.1.16 JPEG command Register (JPGCOM, W, Address = 0xFB60_004C)

JPGCOM	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0
INT_RELEASE	[2]	Interrupt signal release. When Interrupt occurs , set ‘1’ If you set ‘1’, Interrupt is canceled.	0
Reserved	[1:0]	Reserved but should be 0x0	0

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12.7.1.17 Raw Image Data R/W Address Register (IMGADR, R/W, Address = 0xFB60_0050)

IMGADR	Bit	Description	Initial State
IMG_ADR	[31:0]	It is start address of raw image data. Value for this register has to be multiple of 32. In compression mode, raw image before compression is read from this address. In decompression mode, raw image after decompression is stored from address.	0

12.7.1.18 JPEG File R/W Address Register (JPGADR, R/W, Address = 0xFB60_0058)

JPGADR	Bit	Description	Initial State
JPG_ADR	[31:0]	It is start address of JPEG file data. Value for this register has to be multiple of 32. In compression mode, JPEG file after compression is stored from this address. In decompression mode, JPEG file before compression is read from this address.	0

12.7.1.19 Coefficient for RGB-to-YCbCr Converter Register (COEF1, R/W, Address = 0xFB60_005C)

COEF1	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
COEF11	[23:16]	Coefficient value of COEF11	0
COEF12	[15:8]	Coefficient value of COEF12	0
COEF13	[7:0]	Coefficient value of COEF13	0

12.7.1.20 Coefficient for RGB-to-YCbCr Converter Register (COEF2, R/W, Address = 0xFB60_0060)

COEF2	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
COEF21	[23:16]	Coefficient value of COEF21	0
COEF22	[15:8]	Coefficient value of COEF22	0
COEF23	[7:0]	Coefficient value of COEF23	0

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12.7.1.21 Coefficient for RGB-to-YCbCr Converter Register (COEF3, R/W, Address = 0xFB60_0064)

COEF3	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0
COEF31	[23:16]	Coefficient value of COEF31	0
COEF32	[15:8]	Coefficient value of COEF32	0
COEF33	[7:0]	Coefficient value of COEF33	0

The expression of 8-bit COEFxx is like following. For example, if COEFxx is set as 1100_0000b, the decimal value of COEFxx is 0.75. (= 0.5 + 0.25)

Table 12-5 Bitwise Expression of COEFxx

Bit	7	6	5	4	3	2	1	0
Value	0.5	0.25	0.125	0.0625	0.03125	0.015625	0.0078125	0.00390625

$$\begin{pmatrix} Y \\ Cb \\ Cr \end{pmatrix} = \begin{pmatrix} +COEF11 & +COEF12 & +COEF13 \\ -COEF21 & -COEF22 & +COEF23 \\ +COEF31 & -COEF32 & -COEF33 \end{pmatrix} \times \begin{pmatrix} R \\ G \\ B \end{pmatrix} + \begin{pmatrix} c1 \\ 128 \\ 128 \end{pmatrix}$$

12.7.1.22 JPEG Color Mode Register (JPGCMOD, R/W, Address = 0xFB60_0068)

JPGCMOD	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
MOD_SEL	[7:5]	Color space of input raw image 0x1 = YCbCr4:2:2 0x2 = RGB 565 Others are reserved.	1
Reserved	[4:2]	It must be set 0x0.	0
MODE_Y16	[1]	Y_16 selector for Y component 0 = c1 = 0 1 = c1 = 16 c1 is used in RGB-to-YCbCr converter, refer to Table 12-5 Bitwise Expression of COEFxx.	0
Reserved	[0]	Reserved, but should be 0x0	0

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12.7.1.23 JPEG Clock Control Register (JPGCLKCON, R/W, Address = 0xFB60_006C)

JPGCLKCON	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0
CLK_DOWN_READY	[1]	0 = Clock is enabled. 1 = JPEG is ready for disabling clock (Default). This value is changed to 1 if POWER_ON is set as 0 and JPEG is not working. This value is changed to 0 if POWER_ON is set as 1. If this value is 1, JSTART command is ineffective. This bit is read only.	1
POWER_ON	[0]	0 = Disables Clock (Default). 1 = Activates Clock.	0

12.7.1.24 JPEG Start Register (JSTART, W, Address = 0xFB60_0070)

JSTART	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
JSTART	[0]	To start compression/ decompression, set this value to 1. After one clock, it is cleared with 0 internally. Before starting operation, you must set essential registers.	0

12.7.1.25 JPEG SW Reset Register (SW_RESET, R/W, Address = 0xFB60_0078)

SW_RESET	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
SW_RESET	[0]	Writing 1 resets JPEG IP. Before reset finishes, its value is kept as 1. After reset is done, it is cleared with 0 internally. Therefore it is necessary to check this value is 0 before setting registers and starting operation.	0

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12.7.1.26 JPEG Timer Setting Register (TIME_SE, R/W, Address = 0xFB60_007C)

TIMER_SE	Bit	Description	Initial State
TIMER_INT_EN	[31]	0 = Disables Interrupt by timer. 1= Enables Interrupt by timer.	0
TIMER_INIT	[30:0]	Target counting value is stored in this register. After start or restart, timer starts to down-count from this value to 0.	0x7FFF_FFFF

12.7.1.27 JPEG Timer Status Register (TIMER_ST, R/W, Address = 0xFB60_0080)

TIMER_ST	Bit	Description	Initial State
TIMER_INT_STAT	[31]	Timer interrupt status. If timer interrupt is enabled and timer counting value reaches 0, it is set 1. Writing 1 clears this value. Writing 0 has no effect.	0
TIMER_CNT	[30:0]	Timer counting value. If start or restart, it is initiated by TIMER_INIT value and starts to down-count. If JPEG operation finishes before end of counting, it holds the counter value at that time. This bit is read only.	0x7FFF_FFFF

12.7.1.28 JPEG Decompression Output Format Register (OUTFORM, R/W, Address = 0xFB60_0088)

OUTFORM	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
DEC_OUT_FORMAT	[0]	Output color format of decompressed raw image during decompression. 0 = YCbCr 4:2:2 1 = YCbCr 4:2:0	0

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12.7.1.29 JPEG Version Register (VERSION, R, Address = 0xFB60_008C)

VERSION	Bit	Description	Initial State
VERSION	[31:0]	Version Register	0x0003_0001

12.7.1.30 JPEG Compressed Stream Size Interrupt Setting Register (ENC_STREAM_INTSE, R/W, Address = 0xFB60_0098)

TIMER_SE	Bit	Description	Initial State
Reserved	[31:25]	Reserved	0
ENC_STREAM_INT_EN	[24]	0 = Disables Compressed stream size interrupt. 1 = Enables Compressed stream size interrupt.	0
ENC_STREAM_BOUND	[23:0]	The upper bound of the byte size of output compressed stream is stored in this register. This value should be multiple of 32.	0xFF_FFE0

12.7.1.31 JPEG Compressed Stream Size Interrupt Status Register (ENC_STREAM_INTST, R/W, Address = 0xFB60_009C)

TIMER_ST	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
ENC_STREAM_INT_ STAT	[0]	Compressed stream size interrupt status. If the byte size of output compressed stream is larger than the size predefined in ENC_STREAM_BOUND, it is set 1. Writing 1 clears this value. Writing 0 has no effect.	0

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12.7.2 JPEG HUFFMAN AND QUANTIZATION REGISTER TABLES

Each data uses the least significant 8 bits of 32-bit register.

Table 12-6 JPEG Codec Table Assignment

Register	Address	R/W	Description	Reset Value
QTBL0	0xFB60_0400 0xFB60_0404 ……. 0xFB60 _04FC	W	Quantization of table number 0 (64 data with the distance of 4 on address)	0x0000 0000 for 64 each data
QTBL1	0xFB60_0500 0xFB60_0504 …… 0xFB60 _05FC	W	Quantization of table number 1 (64 data with the distance of 4 on address)	0x0000 0000 for 64 each data
QTBL2	0xFB60_0600 0xFB60_0604 …… 0xFB60_06FC	W	Quantization of table number 2 (64 data with the distance of 4 on address)	0x0000 0000 for 64 each data
QTBL3	0xFB60_0700 0xFB60_0704 …… 0xFB60_07FC	W	Quantization of table number 3 (64 data with the distance of 4 on address)	0x0000 0000 for 64 each data
HDCTBL0	0xFB60_0800 0xFB60_0804 …… 0xFB60_083C	W	JPEG DC Huffman Table 0 Register The number of code per code length (16 data with the distance of 4 on address)	-
HDCTBLG0	0xFB60_0840 0xFB60_0844 …… 0xFB60_086C	W	JPEG DC Huffman Table 0 Register Group number of the order for occurrence (12 data with the distance of 4 on address)	-
HACTBL0	0xFB60_0880 0xFB60_0884 …… 0xFB60_08BC	W	JPEG AC Huffman Table 0 Register The number of code per code length (16 data with the distance of 4 on address)	-
HACTBLG0	0xFB60_08C0 0xFB60_08C4 …… 0xFB60_0B44	W	JPEG AC Huffman Table 0 Register Group number of the order for occurrence/ Group number (162 data with the distance of 4 on address)	-
HDCTBL1	0xFB60_0C00 0xFB60_0C04 …… 0xFB60_0C3C	W	JPEG DC Huffman Table 1 Register The number of code per code length (16 data with the distance of 4 on address)	-

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Register	Address	R/W	Description	Reset Value
HDCTBLG1	0xFB60_0C40 0xFB60_0C44 …… 0xFB60_0C6C	W	JPEG DC Huffman Table 1 Register Group number of the order for occurrence (12 data with the distance of 4 on address)	-
HACTBL1	0xFB60_0C80 0xFB60_0C84 ….. 0xFB60_0CBC	W	JPEG AC Huffman Table 1 Register The number of code per code length (16 data with the distance of 4 on address)	-
HACTBLG1	0xFB60_0CC0 0xFB60_0CC4 …… 0xFB60_0F44	W	JPEG AC Huffman Table 1 Register Group number of the order for occurrence/ Group number (162 data with the distance of 4 on address)	-

Each data uses the least significant 8 bits of 32-bit register.

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13 G2D

13.1 INTRODUCTION

FIMG-2D is a 2D graphics accelerator that supports Bit Block Transfer (BitBLT).

Rendering a primitive takes two steps: 1) configure the rendering parameters, such as foreground color and the coordinate data, by setting the drawing-context registers; 2) start the rendering process by setting the relevant command registers accordingly.

13.2 FEATURES

- Primitives
  - BitBLT
    - Stretched BitBLT support (Nearest sampling using Bresnham algorithm)
    - Memory to Screen
    - Memory to Memory
    - Reverse Addressing (X Positive/Negative, Y Positive/Negative)
- Per-pixel Operation
  - Maximum 8000x8000 image size
  - Window Clipping
  - 90° /180° /270° Rotation
  - X-flip/Y-flip
  - Totally 4-operand Raster Operation (ROP4)
    - Mask, Pattern, Source, Destination
  - Alpha Blending
    - Alpha Blending with a user-specified constant alpha
    - Per-pixel Alpha Blending
    - Alpha Blending with both a constant alpha and per-pixel alpha
  - Color Key
- Data Format
  - 16/24/32-bpp, Packed 24bpp color format support
- Supports up to 222 MHz core clock
- Core clock must be faster than APB clock

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13.3 COLOR FORMAT CONVERSION

FIMG-2D V3.0 supports eight color formats: XRGB_8888, ARGB_8888, RGB_565, XRGB_1555, ARGB_1555, XRGB_4444, ARGB_4444, and PACKED_RGB_888. The structure of each color format is illustrated in the figure below. FIMG-2D V3.0 supports four channel orders: ARGB, RGBA, ABGR, and BGRA.

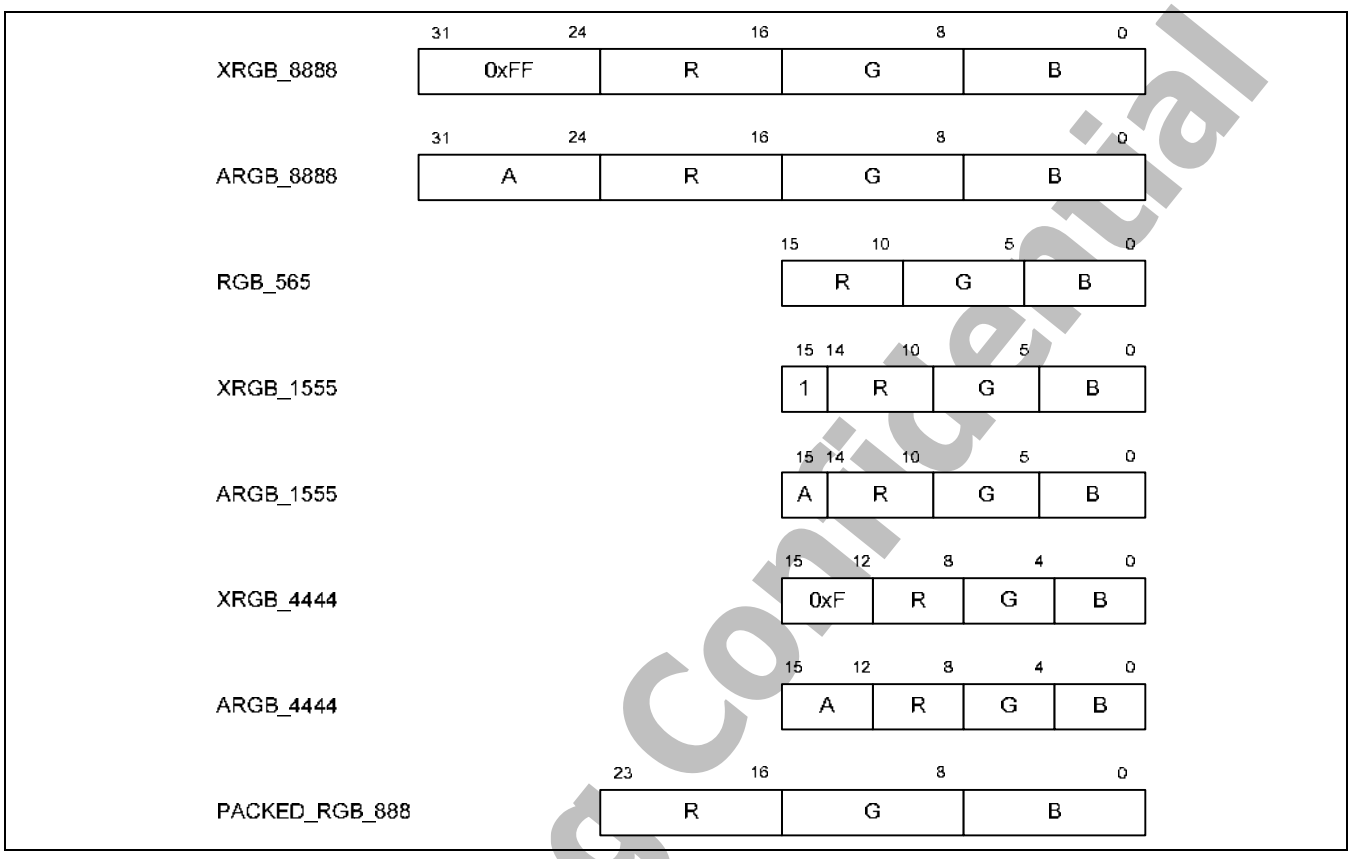

Figure 13-1 Color Format

The internal computations use ARGB_8888 format. All data (source, destination, foreground, background, blue-screen, pattern) are converted to ARGB_8888 format before computation, and the final result are converted to the color format specified by DST_COLOR_MODE_REG before writing to frame buffer.

When a 16-bit color data is converted to 32-bit, the expanded color data is made by the following rule: the data of each field is shifted (8 – x) bits to left, where x is the bit-width of the field. The least significant x bits of the new field data are padded with the most significant x bits of the original field data. For example, if the R value in RGB_565 format is 5'b11010, it will be converted to 8'b11010110, with three LSBs padded with three MSBs (3'b110) from the original R value. Note that, the A field in RGBA_5551 and ARGB_1555 only has one bit, so it is converted to either 8'b00000000 or 8'b11111111 (A=1'b1).

When a 32-bit color data is converted to 16-bit, the data of each field is truncated to x bits, where x is the bit-width of the field in the new color format. For example, if the R value in ARGB_8888 format is 8'b11001110, it will be converted to 5'b11001 in the RGB_565 format, with the three LSBs discarded. Note that, if the A field of the 32-bit color data is not 0, the A field in ARGB_1555 will be 1'b1; otherwise, 1'b0.

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13.4 RENDERING PIPELINE

The rendering pipeline of FIMG-2D V3.0 is illustrated in *Figure 13-2*. The functionality and related registers of each stage are introduced in detail in the rest of this chapter.

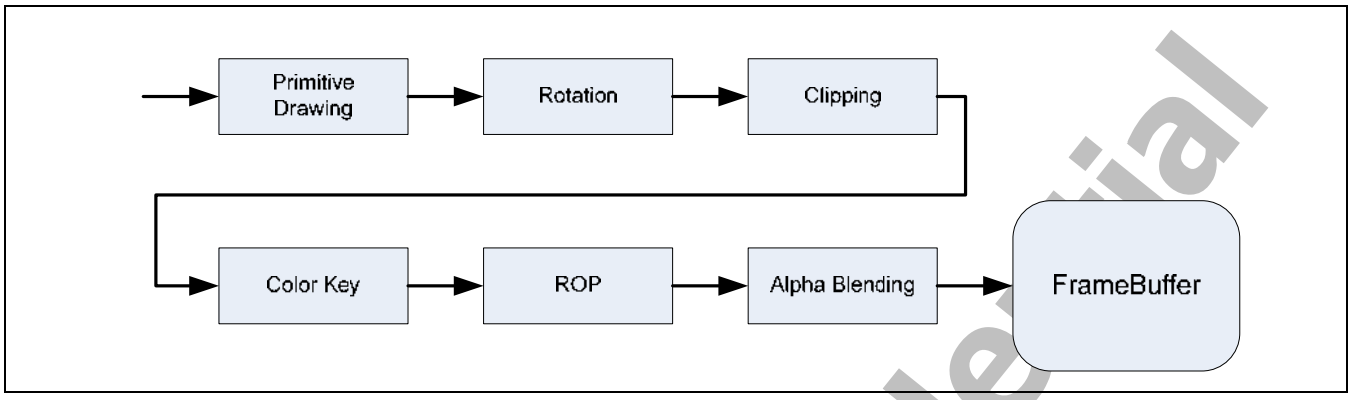

Figure 13-2 FIMG-2D Rendering Pipeline

13.4.1 PRIMITIVE DRAWING

Primitive Drawing determines the pixels to fill, and pass their coordinates to the next stage for further operations.

FIMG-2D V3.0 supports bit block transfer.

13.4.1.1 Bit Block Transfer

A Bit Block Transfer is a transformation of a rectangular block of pixels. Typical applications include copying the off-screen pixel data to frame buffer, selecting one of two raster operations by mask value, combining to bitmap patterns by the selected raster operation, changing the dimension of a rectangular image and so on.

Stretch Bit Block Transfer is implemented using Bresnham algorithm and nearest sampling.

13.4.1.1.1 On-Screen Rendering

On-screen bit block transfer copies a rectangular block of pixels on screen to another position on the same screen. Note that on-screen rendering has the following restriction:

- SRC_BASE_ADDR_REG = DST_BASE_ADDR_REG
- SRC_SIZE_REG = DST_SIZE_REG
- SRC_COLOR_MODE_REG = DST_COLOR_MODE_REG

13.4.1.1.2 Off-Screen Rendering

Off-screen bit block transfer copies pixel data from off-screen memory to frame buffer. Color format conversion is performed automatically if SRC_COLOR_MODE_REG differs from DST_COLOR_MODE_REG.

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13.4.1.1.3 Transparent Mode

FIMG-2D V3.0 can render image in Transparent Mode. In this mode, the pixels having the same color with blue screen color (BS_COLOR_REG) are discarded, resulting in a transparent effect. The function of Transparent Mode is illustrated in the images below, in which the BS_COLOR_REG is set to white.

FIMG-2D V3.0 also support Blue Screen Mode, in which the pixels having the same color with blue screen color (BS_COLOR_REG) are replaced by the background color (BG_COLOR_REG).

FIMG-2D V3.0 supports both memory-to-memory mode and memory-to-screen mode of BLT.

13.4.1.1.4 Related Registers

SRC_LEFT_TOP_REG	Coordinate of the leftmost topmost coordinate of the source image.
SRC_RIGHT_BOTTOM_REG	Coordinate of the rightmost bottommost coordinate of the source image.
SRC_SELECT_REG	Select one of the following cases - 2'b00: normal mode (source image in the memory), 2'b01: foreground color, 2'b10: background color.
DST_LEFT_TOP_REG	Coordinate of the leftmost topmost coordinate of the destination image.
DST_RIGHT_BOTTOM_REG	Coordinate of the rightmost bottommost coordinate of the destination image.
DST_SELECT_REG	Select one of the following cases - 2'b00: normal mode (destination image in the memory), 2'b01: foreground color, 2'b10: background color.
SRC_BASE_ADDR_REG	The base address of the source image (when normal mode is used in SRC_SELECT_REG).
DST_BASE_ADDR_REG	The base address of the destination image (usually the frame buffer base address).
SRC_SIZE_REG	The width and height of the source image.
DST_SIZE_REG	The width and height of the destination image.
SRC_COLOR_MODE_REG	The color format and channel order of the source image.
DST_COLOR_MODE_REG	The color format and channel order of the destination image.
FG_COLOR_REG	Foreground color value.
BG_COLOR_REG	Background color value.
BS_COLOR_REG	Blue screen color value.
BITBLT_COMMAND_REG	Enable/disable Transparent Mode or Blue Screen Mode.

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13.4.2 ROTATION AND ADDRESSING DIRECTION (FLIP)

The pixels can be rotated by 90 degree clockwise or flipped around X-axis or Y-axis. The flip operation can be performed by direction of source read and destination read. The effects of rotation and flip options are summarized in the following table and illustrated in *Figure 13-3*.

13.4.2.1.1 Related Registers

ROTATE_REG	Enable 90 degree rotation
SRC_MSK_DIRECT_REG	Addressing direction of source/mask memory to read
DST_PAT_DIRECT_REG	Addressing direction of destination/pattern memory to read and write

13.4.2.1.2 Rotation Effect

0°	Rotated X = Original X Rotated Y = Original Y
90°	Rotated X = Original Y Rotated Y = Original Width - 1 - Original X

13.4.2.1.3 Addressing Direction Effect

	Effect
Src X Direction = Dst X Direction	No flip over X axis
Src X Direction ≠ Dst X Direction	Horizontal flip
Src Y Direction = Dst Y Direction	No flip over Y axis
Src Y Direction ≠ Dst Y Direction	Vertical flip

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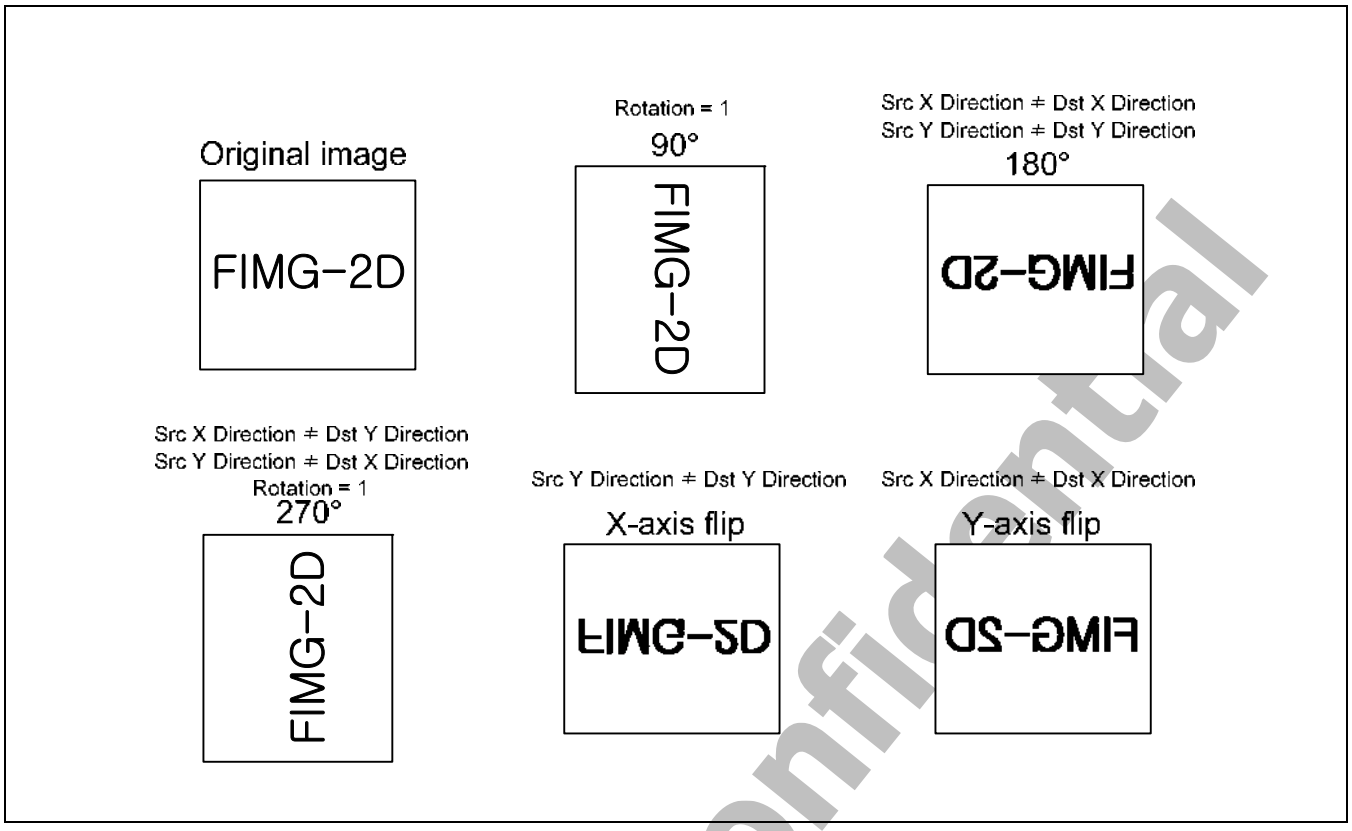

Figure 13-3 Rotation and Flip Example

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13.4.3 CLIPPING

Clipping discards the pixels (after rotation) outside the clipping window. The discarded pixels will not go through the rest of rendering pipelines.

Note that the clipping windows must reside totally inside the screen. Setting the clipping window the same size with the screen will disable the clipping effect, and a clipping window bigger than the screen size is not allowed.

13.4.3.1.1 Related Registers

BITBLT_COMMAND_REG	Enable/disable Clipping Window (CWEn Field)
CW_LT_REG	Coordinate of the leftmost topmost point of the clipping window
CW_RB_REG	Coordinate of the rightmost bottommost point of the clipping window

13.4.4 COLOR KEY

The Color Key conditionally discards a pixel based on the outcome of a comparison between the color value of this pixel of the source/destination image and the DR(min)/DR(max) values. If each field (R, G, B, A) of the color value falls in the range of [DR(min), DR(max)], this pixel is passed to the next stage; otherwise, discarded. User can disable the stencil test on a specific field by clearing the corresponding bits in COLORKEY_CNTL.

13.4.4.1.1 Related Registers

SRC_COLORKEY_CTRL_REG	Source Stencil Test configurations, such as enable/disable the test and so on.
SRC_COLORKEY_DR_MIN_REG	Set the source DR(min) value for each field
SRC_COLORKEY_DR_MAX_REG	Set the source DR(max) value for each field
DST_COLORKEY_CTRL_REG	Destination Stencil Test configurations, such as enable/disable the test and so on.
DST_COLORKEY_DR_MIN_REG	Set the DR(min) value for each field
DST_COLORKEY_DR_MAX_REG	Set the DR(max) value for each field

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13.4.5 RASTER OPERATION

Raster operation performs Boolean operations on four operands: Mask, third operand, source, and destination according to two 8-bit-ROP3 values specified by the user. User can choose unmasked ROP3 value and masked ROP3 value with binary mask image. Mask should be the same size as source image.

The following table is the truth table of ROP3.

Third Operand	Source	Destination	ROP Value
0	0	0	Bit0
0	0	1	Bit1
0	1	0	Bit2
0	1	1	Bit3
1	0	0	Bit4
1	0	1	Bit5
1	1	0	Bit6
1	1	1	Bit7

The third operand can be pattern, foreground color, or background color; configurable by THIRD_OPERAND_REG.

The pattern supports all the format of source image or destination image. The following equation is used to calculate the pattern pixel coordinate (x, y):

- X = (PatternOffsetX + x) % PatternWidth
- Y = (PatternOffsetY + y) % PatternHeight,

  where PatternOffsetY and PatternOffsetX are the offset value specified in register PAT_OFFSET_REG, and PatternWidth and PatternHeight are size of the pattern specified in register PAT_SIZE_REG

Here are some examples on how to use the ROP3 value to perform the operations:

- Final Data = Source. Only the Source data matter, so ROP Value = “0xCC”.
- Final Data = Destination. Only the Destination data matter, so ROP Value = “0xAA”.
- Final Data = Pattern. Only the Pattern data matter, so ROP Value = “0xF0”.
- Final Data = Source AND Destination. ROP Value = “0xCC” & “0xAA” = “0x88”
- Final Data = Source OR Pattern. ROP Value = “0xCC” | “0xF0” = “0xFC”.

Note that the Raster Operation only applies on Red, Green and, Blue fields of the color data; the Alpha field will not be affected.

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13.4.5.1.1 Related Registers

PAT_BASE_ADDR_REG	Base address of the pattern image
PAT_SIZE_REG	Size of the pattern
PAT_COLOR_MODE_REG	Color channel order and color format of the pattern
PAT_OFFSET_REG	Coordinate offset of the pattern
MASK_BASE_ADDR_REG	Base address of the mask image
THIRD_OPERAND_REG	Third operand selection for unmasked ROP3 and masked ROP3
ROP4_REG	ROP4 Value

13.4.6 ALPHA BLENDING

Alpha Blending combines the source color and the destination color in the frame buffer to get the new destination color. Alpha Blending equation is decided by source alpha value and user-specified alpha value.

13.4.6.1.1 Related Registers

BITBLT_COMMAND_REG	Alpha blending configurations: alpha blending disable/enable, fading disable/enable.
ALPHA_REG	Alpha value and fading offset value.

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13.5 REGISTER DESCRIPTION

13.5.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
General Registers				
SOFT_RESET_REG	0xFA00_0000	W	Software reset register	0x0000_0000
INTEN_REG	0xFA00_0004	R/W	Interrupt Enable register	0x0000_0000
INTC_PEND_REG	0xFA00_000C	R/W	Interrupt Control Pending register	0x0000_0000
FIFO_STAT_REG	0xFA00_0010	R	Command FIFO Status register	0x0000_0001
AXI_ID_MODE_REG	0xFA00_0014	R/W	AXI Read ID Mode register	0x0000_0000
CACHECTL_REG	0xFA00_0018	R/W	Cache & Buffer clear register	0x0000_0000
Command Registers				
BITBLT_START_REG	0xFA00_0100	W	BitBLT Start register	-
BITBLT_COMMAND_REG	0xFA00_0104	R/W	Command register for BitBLT	0x0000_0000
Parameter Setting Registers (Rotate & Direction)				
ROTATE_REG	0xFA00_0200	R/W	Rotation register	0x0000_0000
SRC_MSK_DIRECT_REG	0xFA00_0204	R/W	Source and Mask Direction register	0x0000_0000
DST_PAT_DIRECT_REG	0xFA00_0208	R/W	Destination and Pattern Direction register	0x0000_0000
Parameter Setting Registers (Source)				
SRC_SELECT_REG	0xFA00_0300	R/W	Source Image Selection register	0x0000_0000
SRC_BASE_ADDR_REG	0xFA00_0304	R/W	Source Image Base Address register	0x0000_0000
SRC_STRIDE_REG	0xFA00_0308	R/W	Source Stride register	0x0000_0000
SRC_COLOR_MODE_REG	0xFA00_030C	R/W	Source Image Color Mode register	0x0000_0000
SRC_LEFT_TOP_REG	0xFA00_0310	R/W	Source Left Top Coordinate register	0x0000_0000
SRC_RIGHT_BOTTOM_REG	0xFA00_0314	R/W	Source Right Bottom Coordinate register	0x0000_0000
Parameter Setting Registers (Destination)				
DST_SELECT_REG	0xFA00_0400	R/W	Destination Image Selection register	0x0000_0000
DST_BASE_ADDR_REG	0xFA00_0404	R/W	Destination Image Base Address register	0x0000_0000
DST_STRIDE_REG	0xFA00_0408	R/W	Destination Stride register	0x0000_0000
DST_COLOR_MODE_REG	0xFA00_040C	R/W	Destination Image Color Mode register	0x0000_0000

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Register	Address	R/W	Description	Reset Value
DST_LEFT_TOP_ REG	0xFA00_0410	R/W	Destination Left Top Coordinate register	0x0000_0000
DST_RIGHT_ BOTTOM_REG	0xFA00_0414	R/W	Destination Right Bottom Coordinate register	0x0000_0000
Parameter Setting Registers (Pattern)				
PAT_BASE_ ADDR_REG	0xFA00_0500	R/W	Pattern Image Base Address register	0x0000_0000
PAT_SIZE_REG	0xFA00_0504	R/W	Pattern Image Size register	0x0001_0001
PAT_COLOR_ MODE_REG	0xFA00_0508	R/W	Pattern Image Color Mode register	0x0000_0000
PAT_OFFSET_REG	0xFA00_050C	R/W	Pattern Left Top Coordinate register	0x0000_0000
PAT_STRIDE_REG	0xFA00_0510	R/W	Pattern Stride register	0x0000_0000
Parameter Setting Registers (Mask)				
MASK_BASE_ADDR _REG	0xFA00_0520	R/W	Mask Base Address register	0x0000_0000
MASK_STRIDE_ REG	0xFA00_0524	R/W	Mask Stride register	0x0000_0000
Parameter Setting Registers (Clipping Window)				
CW_LT_REG	0xFA00_0600	R/W	LeftTop coordinates of Clip Window	0x0000_0000
CW_RB_REG	0xFA00_0604	R/W	RightBottom coordinates of Clip Window	0x0000_0000
Parameter Setting Registers (ROP & Alpha Setting)				
THIRD_OPERAND_ REG	0xFA00_0610	R/W	Third Operand Selection register	0x0000_0000
ROP4_REG	0xFA00_0614	R/W	Raster Operation register	0x0000_0000
ALPHA_REG	0xFA00_0618	R/W	Alpha value, Fading offset value	0x0000_0000
Parameter Setting Registers (Color)				
FG_COLOR_REG	0xFA00_0700	R/W	Foreground Color register	0x0000_0000
BG_COLOR_REG	0xFA00_0704	R/W	Background Color register	0x0000_0000
BS_COLOR_REG	0xFA00_0708	R/W	Blue Screen Color register	0x0000_0000
Parameter Setting Registers (Color Key)				
SRC_COLORKEY_ CTRL_REG	0xFA00_0710	R/W	Source Colorkey control register	0x0000_0000
SRC_COLORKEY_ DR_MIN_REG	0xFA00_0714	R/W	Source Colorkey Decision Reference Minimum register	0x0000_0000
SRC_COLORKEY_ DR_MAX_REG	0xFA00_0718	R/W	Source Colorkey Decision Reference Maximum register	0xFFFF_FFFF
DST_COLORKEY_ CTRL_REG	0xFA00_071C	R/W	Destination Colorkey control register	0x0000_0000
DST_COLORKEY_	0xFA00_0720	R/W	Destination Colorkey Decision Reference	0x0000_0000

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Register	Address	R/W	Description	Reset Value
DR_MIN_REG			Minimum register	
DST_COLORKEY_ DR_MAX_REG	0xFA00_0724	R/W	Destination Colorkey Decision Reference Maximum register	0xFFFF_FFFF

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13.5.2 GENERAL REGISTERS

13.5.2.1 Software Reset Register (SOFT_RESET_REG, W, Address = 0xFA00_0000)

SOFT_RESET_REG	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0x0
R	[0]	Software Reset Write to this bit results in a one-cycle reset signal to FIMG2D graphics engine. Every command register and parameter setting register will be assigned the “Reset Value”,	0x0

13.5.2.2 Interrupt Enable Register (INTEN_REG, R/W, Address = 0xFA00_0004)

INTEN_REG	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0x0
INT_TYPE	[1]	Must be set to 0 (cannot be 1)	0x0
CF	[0]	Command Finished interrupt enable. If this bit is set, when the graphics engine finishes the execution of command, an interrupt occurs, and the INTP_CMD_FIN flag in INTC_PEND_REG will be set.	0x0

13.5.2.3 Interrupt Pending Register (INTC_PEND_REG, R/W, Address = 0xFA00_000C)

INTC_PEND_REG	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0x0
INTP_CMD_FIN	[0]	Command Finished interrupt flag. Writing ‘1’ to this bit clears this flag It is recommended to clear this bit before Start_BitBLT because of previous Start_BitBLT’s residue	0x0

13.5.2.4 FIFO Status Register (FIFO_STAT_REG, R, Address = 0xFA00_0010)

FIFO_STAT_REG	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0x0
CMD_FIN	[0]	1 = The graphics engine finishes the execution of command. 0 = In the middle of rendering process.	0x1

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13.5.2.5 AXI ID Mode Register (AXI_ID_MODE_REG, R/W, Address = 0xFA00_0014)

AXI_ID_MODE_REG	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0x0
AXI_RD_ID_MODE	[0]	This bit is for out of ordering of AXI Master Read. If this bit is set, the several read port of this engine have each AXI RID on only one AXI MASTER I/F 1 = Multiple ID (out of order) 0 = Single ID fixing on 4'b0 (In order)	0x0

13.5.2.6 Cache Control Register (CACHECTL_REG, R/W, Address = 0xFA00_0018)

CACHECTL_REG	Bit	Description	Initial State
Reserved	[31:3]	Reserved	0x0
PATCACHE_CLEAR	[2]	Pattern cache clear (Automatically set to 0b after a cycle) This bit is used to invalidate the contents of pattern cache. 0 = Default stages; pattern cache invalidation unchanged 1 = Pattern cache starts invalidation	0x0
SRCBUFFER_CLEAR	[1]	Source buffer clear (Automatically set to 0b after a cycle) This bit is used to invalidate the contents of source buffer. 0 = Default stages; source buffer invalidation unchanged 1 = Source buffer starts invalidation	0x0
MASKBUFFER_CLEAR	[0]	Mask buffer clear (Automatically set to 0b after a cycle) This bit is used to invalidate the contents of mask buffer. 0 = Default stages; Mask buffer invalidation unchanged 1 = Mask buffer starts invalidation	0x0

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13.5.3 COMMAND REGISTERS

13.5.3.1 BitBLT Start Register (BITBLT_START_REG, W, Address = 0xFA00_0100)

BITBLT_START_REG	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0x0
Start_BitBLT	[0]	Start BitBLT Operation. When this bit is set, it is automatically clear after one clock cycle.	0x0

13.5.3.2 BitBLT Command Register (BITBLT_COMMAND_REG, R/W, Address = 0xFA00_0104)

BITBLT_COMMAND_REG	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x0
SrcNonPreBlendMode	[23:22]	Source Non-premultiplied 2'b00: Disable 2'b01: Alpha Blend with Constant Alpha 2'b10: Alpha Blend with PerPixel Alpha 2'b11: Reserved	0x0
AlphaBlendMode	[21:20]	Alpha Blending Mode 2'b00: No Alpha Blending 2'b01: Alpha Blending 2'b10: Fading 2'b11: Reserved	0x0
Reserved	[19:18]	Reserved	0x0
ColorKeyMode	[17:16]	2'b00: Disable colorkey 2'b01: Enable source colorkey 2'b10: Enable destination colorkey 2'b11: Enable source colorkey and destination colorkey	0x0
Reserved	[15:14]	Reserved	0x0
Transparent Mode	[13:12]	2'b00: Opaque Mode 2'b01: Transparent Mode 2'b10: BlueScreen Mode 2'b11: Reserved	0x0
Reserved	[11:9]	Reserved	0x0
CWEn	[8]	Enable Clipping Window	0x0
Reserved	[7:5]	Reserved	0x0
StretchEn	[4]	Enable Stretch Mode	0x0
Reserved	[3:1]	Reserved	0x0
MaskEn	[0]	Enable Mask Operand (ROP4 Operation)	0x0

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13.5.4 PARAMETER SETTING REGISTERS (ROTATION & DIRECTION)

13.5.4.1 Rotation Register (ROTATE_REG, R/W, Address = 0xFA00_0200)

ROTATE_REG	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0x0
Rotate	[0]	0 = No rotation 1 = 90 degree rotation	0x0

13.5.4.2 Source and Mask Direction Register (SRC_MSK_DIRECT_REG, R/W, Address = 0xFA00_0204)

SRC_MSK_DIRECT_REG	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0x0
MskYDirect	[5]	0 = Y positive 1 = Y negative	0x0
MskXDirect	[4]	0 = X positive 1 = X negative	0x0
Reserved	[3:2]	Reserved	0x0
SrcYDirect	[1]	0 = Y positive 1 = Y negative	0x0
SrcXDirect	[0]	0 = X positive 1 = X negative	0x0

NOTE: Mask direction is usually same as source direction.

13.5.4.3 Destination and Pattern Direction Register(DST_PAT_DIRECT_REG, R/W, Address = 0xFA00_0208)

DST_PAT_DIRECT_REG	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0x0
PatYDirect	[5]	0 = Y positive 1 = Y negative	0x0
PatXDirect	[4]	0 = X positive 1 = X negative	0x0
Reserved	[3:2]	Reserved	0x0
DstYDirect	[1]	0 = Y positive 1 = Y negative	0x0
DstXDirect	[0]	0 = X positive 1 = X negative	0x0

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13.5.5 PARAMETER SETTING REGISTERS (SOURCE)

13.5.5.1 Source Image Selection Register (SRC_SELECT_REG, W, Address = 0xFA00_0300)

SRC_SELECT_REG	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0x0
SrcSelect	[1:0]	Select Source 2'b00: Normal Mode(Using source image in the external memory) 2'b01: Using foreground color as source image 2'b10: Using background color as source image 2'b11: Reserved	0x0

13.5.5.2 Source Image Base Address Register (SRC_BASE_ADDR_REG, W, Address = 0xFA00_0304)

SRC_BASE_ADDR_REG	Bit	Description	Initial State
SrcAddr	[31:0]	Base address of the source image	0x0

13.5.5.3 Source Stride Register (SRC_STRIDE_REG, R/W, Address = 0xFA00_0308)

SRC_STRIDE_REG	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0
SrcStride	[15:0]	Source stride (2's complement value)	0x0

13.5.5.4 Source Image Color Mode Register (SRC_COLOR_MODE_REG, R/W, Address = 0xFA00_030C)

SRC_COLOR_MODE_REG	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0x0
SrcChannelOrder	[5:4]	2'b00: {A,X}RGB 2'b01: RGB{A,X} 2'b10: {A,X}BGR 2'b11: BGR{A,X}	0x0
Reserved	[3]	Reserved	0x0
SrcColorFormat	[2:0]	3'b000: XRGB_8888 3'b001: ARGB_8888 3'b010: RGB_565 3'b011: XRGB_1555 3'b100: ARGB_1555 3'b101: XRGB_4444 3'b110: ARGB_4444 3'b111: PACKED_RGB_888	0x0

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13.5.5.5 Source Left Top Coordinate Register (SRC_LEFT_TOP_REG, R/W, Address = 0xFA00_0310)

SRC_LEFT_TOP_REG	Bit	Description	Initial State
Reserved	[31:29]	Reserved	0x0
SrcTopY	[28:16]	Left Top Y Coordinate of Source Image Range: 0 ~ 8000 (Requirement: SrcTopY < SrcBottomY)	0x0
Reserved	[15:13]	Reserved	0x0
SrcLeftX	[12:0]	Left Top X Coordinate of Source Image Range: 0 ~ 8000 (Requirement: SrcLeftX < SrcRightX)	0x0

13.5.5.6 Source Right Bottom Coordinate Register (SRC_RIGHT_BOTTOM_REG, R/W, Address = 0xFA00_0314)

SRC_RIGHT_ BOTTOM_REG	Bit	Description	Initial State
Reserved	[31:29]	Reserved	0x0
SrcBottomY	[28:16]	Right Bottom Y Coordinate of Source Image Range: 0 ~ 8000	0x0
Reserved	[15:13]	Reserved	0x0
SrcRightX	[12:0]	Right Bottom X Coordinate of Source Image Range: 0 ~ 8000	0x0

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13.5.6 PARAMETER SETTING REGISTERS (DESTINATION)

13.5.6.1 Destination Image Selection Register (DST_SELECT_REG, W, Address = 0xFA00_0400)

DST_SELECT_REG	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0x0
DstSelect	[1:0]	Select Destination 2'b00: Normal Mode(Using destination image in the external memory) 2'b01: Using foreground color as destination image 2'b10: Using background color as destination image 2'b11: Reserved	0x0

13.5.6.2 Destination Image Base Address Register (DST_BASE_ADDR_REG, W, Address = 0xFA00_0404)

DST_BASE_ADDR_REG	Bit	Description	Initial State
DstAddr	[31:0]	Base address of the destination image	0x0

13.5.6.3 Destination Stride Register (DST_STRIDE_REG, R/W, Address = 0xFA00_0408)

DST_STRIDE_REG	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0
DstStride	[15:0]	Destination stride (2's complement value).	0x0

13.5.6.4 Destination Image Color Mode Register(DST _COLOR_MODE_REG, R/W, Address = 0xFA00_040C)

DST_COLOR_MODE_REG	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0x0
DstChannelOrder	[5:4]	2'b00: {A,X}RGB 2'b01: RGB{A,X} 2'b10: {A,X}BGR 2'b11: BGR{A,X}	0x0
Reserved	[3]	Reserved	0x0
DstColorFormat	[2:0]	3'b000: XRGB_8888 3'b001: ARGB_8888 3'b010: RGB_565 3'b011: XRGB_1555 3'b100: ARGB_1555 3'b101: XRGB_4444 3'b110: ARGB_4444 3'b111: PACKED_RGB_888	0x0

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13.5.6.5 Destination Left Top Coordinate Register (DST _LEFT_TOP_REG, R/W, Address = 0xFA00_0410)

DST_LEFT_TOP_REG	Bit	Description	Initial State
Reserved	[31:29]	Reserved	0x0
DstTopY	[28:16]	Left Top Y Coordinate of destination image Range: 0 ~ 8000 (Requirement: DstTopY < DstBottomY)	0x0
Reserved	[15:13]	Reserved	0x0
DstLeftX	[12:0]	Left Top X Coordinate of destination image Range: 0 ~ 8000 (Requirement: DstLeftX < DstRightX)	0x0

13.5.6.6 Destination Right Bottom Coordinate Register (DST _RIGHT_BOTTOM_REG, R/W, Address = 0xFA00_0414)

DST_RIGHT_ BOTTOM_REG	Bit	Description	Initial State
Reserved	[31:29]	Reserved	0x0
DstBottomY	[28:16]	Right Bottom Y Coordinate of destination image Range: 0 ~ 8000	0x0
Reserved	[15:13]	Reserved	0x0
DstRightX	[12:0]	Right Bottom X Coordinate of destination image Range: 0 ~ 8000	0x0

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13.5.7 PARAMETER SETTING REGISTERS (PATTERN)

13.5.7.1 Pattern Image Base Address Register (PAT_BASE_ADDR_REG, W, Address = 0xFA00_0500)

PAT_BASE_ADDR_REG	Bit	Description	Initial State
PatAddr	[31:0]	Base address of the pattern image	0x0

13.5.7.2 Pattern Image Size Register (PAT_SIZE_REG, R/W, Address = 0xFA00_0504)

PAT_SIZE_REG	Bit	Description	Initial State
Reserved	[31:29]	Reserved	0x0
PatHeight	[28:16]	Height of pattern image. Range: 1 ~ 8000	0x1
Reserved	[15:13]	Reserved	0x0
PatWidth	[12:0]	Width of pattern image. Range: 1 ~ 8000.	0x1

13.5.7.3 Pattern Image Color Mode Register (PAT_COLOR_MODE_REG, R/W, Address = 0xFA00_0508)

PAT_COLOR_MODE_REG	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0x0
PatChannelOrder	[5:4]	2'b00: {A,X}RGB 2'b01: RGB{A,X} 2'b10: {A,X}BGR 2'b11: BGR{A,X}	0x0
Reserved	[3]	Reserved	0x0
PatColorFormat	[2:0]	3'b000: XRGB_8888 3'b001: ARGB_8888 3'b010: RGB_565 3'b011: XRGB_1555 3'b100: ARGB_1555 3'b101: XRGB_4444 3'b110: ARGB_4444 3'b111: PACKED_RGB_888	0x0

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13.5.7.4 Pattern Offset Register (PAT_OFFSET_REG, R/W, Address = 0xFA00_050C)

PAT_OFFSET_REG	Bit	Description	Initial State
Reserved	[31:29]	Reserved	0x0
PatOffsetY	[28:16]	Y value of pattern offset. Range: 1 ~ 8000	0x0
Reserved	[15:13]	Reserved	0x0
PatOffsetX	[12:0]	X value of pattern offset. Range: 1 ~ 8000.	0x0

13.5.7.5 Pattern Stride Register (PAT_STRIDE_REG, R/W, Address = 0xFA00_0510)

PAT_STRIDE_REG	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0
PatStride	[15:0]	Pattern stride (2's complement value)	0x0

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13.5.8 PARAMETER SETTING REGISTERS (MASK)

13.5.8.1 Mask Base Address Register (MASK_BASE_ADDR_REG, W, Address = 0xFA00_0520)

MASK_BASE_ ADDR_REG	Bit	Description	Initial State
MaskAddr	[31:0]	Base address of the mask image	0x0

13.5.8.2 Mask Stride Register (MASK_STRIDE_REG, R/W, Address = 0xFA00_0524)

MASK_STRIDE_REG	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0
MaskStride	[15:0]	Mask stride (2's complement value).	0x0

NOTE: - MaskLeftX, MaskTopY, MaskRightX, and MaskBottomY are same as source image
- FIMG-2D V3.0 supports only 1bpp mask image format.

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13.5.9 PARAMETER SETTING REGISTERS (CLIPPING WINDOW)

13.5.9.1 LeftTop Clipping Window Register (CW_LT_REG, R/W, Address = 0xFA00_0600)

CW_LT_REG	Bit	Description	Initial State
Reserved	[31:29]	Reserved	0x0
CWTopY	[28:16]	Top Y Clipping Window Requirement: DstTopY <= CWTopY < CWBottomY	0x0
Reserved	[15:13]	Reserved	0x0
CWLeftX	[12:0]	Left X Coordinate of Clipping Window. Requirement: DstLeftX <= CWLeftX < CWRightX	0x0

13.5.9.2 RightBottom Clipping Window Register (CW_RB_REG, R/W, Address = 0xFA00_0604)

CW_RB_REG	Bit	Description	Initial State
Reserved	[31:29]	Reserved	0x0
CWBottomY	[28:16]	Bottom Y Clipping Window Requirement: CWBottomY <= DstBottomY	0x0
Reserved	[15:13]	Reserved	0x0
CWRightX	[12:0]	Right X Clipping Window Requirement: CWRightX <= DstRightX	0x0

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13.5.10 PARAMETER SETTING REGISTERS (ROP & ALPHA SETTING)

13.5.10.1 Third Operand Selection Register (THIRD_OPERAND_REG, R/W, Address = 0xFA00_0610)

THIRD_OPERAND_REG	Bit	Description	Initial State
Reserved	[31:6]	Reserved	0x0
MaskedSelect	[5:4]	2'00: Pattern 2'01: Foreground color 2'10: Background color Others: Reserved	0x0
Reserved	[3:2]	Reserved	-
UnmaskedSelect	[1:0]	2'00: Pattern 2'01: Foreground color 2'10: Background color Others: Reserved	0x0

13.5.10.2 Raster Operation Register (ROP4_REG, R/W, Address = 0xFA00_0614)

ROP4_REG	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0
MaskedROP3	[15:8]	Raster Operation Value	0x0
UnmaskedROP3	[7:0]	Raster Operation Value	0x0

13.5.10.3 Alpha Register (ALPHA_REG, R/W, Address = 0xFA00_0618)

ALPHA_REG	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0
FadingOffset	[15:8]	Fading Offset Value	0x0
AlphaValue	[7:0]	Alpha Value	0x0

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13.5.11 PARAMETER SETTING REGISTERS (COLOR)

13.5.11.1 Foreground Color Register (FG_COLOR_REG, R/W, Address = 0xFA00_0700)

The color format of the foreground color is the same as the destination color format.

FG_COLOR_REG	Bit	Description	Initial State
ForegroundColor	[31:0]	Foreground Color Value. The alpha field of the foreground color will be discarded.	0x0

13.5.11.2 Background Color Register (BG_COLOR_REG, R/W, Address = 0xFA00_0704)

The color format of the background color is the same as the destination color format.

BG_COLOR_REG	Bit	Description	Initial State
BackgroundColor	[31:0]	Background Color Value. The alpha field of the background color will be discarded.	0x0

13.5.11.3 BlueScreen Color Register (BS_COLOR_REG, R/W, Address = 0xFA00_0708)

The color format of the bluescreen color is generally the same as the source color format.

But if the source color is selected as the foreground color or the background color, the color format of the bluescreen color is the destination color format because the color format of the foreground and the background are the destination color format.

BS_COLOR_REG	Bit	Description	Initial State
BlueScreenColor	[31:0]	BlueScreen Color Value. The alpha field of the blue screen color will be discarded.	0x0

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13.5.12 PARAMETER SETTING REGISTERS (COLOR KEY)

13.5.12.1 Source Colorkey Control Register (SRC_COLORKEY_CTRL_REG, R/W, Address = 0xFA00_0710)

SRC_COLORKEY_ CTRL_REG	Bit	Description	Initial State
Reserved	[31:17]	Reserved	0x0
SrcStencilInv	[16]	0 = Normal stencil test 1 = Inversed stencil test	0x0
Reserved	[15:13]	Reserved	
SrcStencilOnA	[12]	0 = Stencil Test Off for A value 1 = Stencil Test On for A value	0x0
Reserved	[11:9]	Reserved	
SrcStencilOnR	[8]	0 = Stencil Test Off for R value 1 = Stencil Test On for R value	0x0
Reserved	[7:5]	Reserved	
SrcStencilOnG	[4]	0 = Stencil Test Off for G value 1 = Stencil Test On for G value	0x0
Reserved	[3:1]	Reserved	
SrcStencilOnB	[0]	0 = Stencil Test Off for B value 1 = Stencil Test On for B value	0x0

13.5.12.2 Source Colorkey Decision Reference Minimum Register (SRC_COLORKEY _DR_MIN_REG, R/W, Address = 0xFA00_0714)

The color format of source colorkey decision reference register is generally the same as the source color format.

But if the source color is selected as the foreground color or the background color, the color format of source colorkey register is the destination color format because the color format of the foreground and the background are the destination color format.

SRC_COLORKEY _DR_MIN_REG	Bit	Description	Initial State
SrcDRMinA	[31:24]	Alpha DR MIN value	0x0
SrcDRMinR	[23:16]	Red DR MIN value	0x0
SrcDRMinG	[15:8]	Green DR MIN value	0x0
SrcDRMinB	[7:0]	Blue DR MIN value	0x0

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13.5.12.3 Source Colorkey Decision Reference Maximum Register (SRC_COLORKEY _DR_MAX_REG, R/W, Address = 0xFA00_0718)

The color format of source colorkey decision reference register is generally the same as the source color format.

But if the source color is selected as the foreground color or the background color, the color format of source colorkey register is the destination color format because the color format of the foreground and the background are the destination color format.

SRC_COLORKEY _DR_MAX_REG	Bit	Description	Initial State
SrcDRMaxA	[31:24]	Alpha DR MAX value	0xFF
SrcDRMaxR	[23:16]	Red DR MAX value	0xFF
SrcDRMaxG	[15:8]	Green DR MAX value	0xFF
SrcDRMaxB	[7:0]	Blue DR MAX value	0xFF

13.5.12.4 Destination Colorkey Control Register (DST_COLORKEY_CTRL_REG, R/W, Address = 0xFA00_071C)

DST_COLORKEY_ CTRL_REG	Bit	Description	Initial State
Reserved	[31:17]	Reserved	0x0
DstStencilInv	[16]	0 = Normal stencil test 1 = Inversed stencil test	0x0
Reserved	[15:13]	Reserved	
DstStencilOnA	[12]	0 = Stencil Test Off for A value 1 = Stencil Test On for A value	0x0
Reserved	[11:9]	Reserved	
DstStencilOnR	[8]	0 = Stencil Test Off for R value 1 = Stencil Test On for R value	0x0
Reserved	[7:5]	Reserved	
DstStencilOnG	[4]	0 = Stencil Test Off for G value 1 = Stencil Test On for G value	0x0
Reserved	[3:1]	Reserved	
DstStencilOnB	[0]	0 = Stencil Test Off for B value 1 = Stencil Test On for B value	0x0

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13.5.12.5 Destination Colorkey Decision Reference Minimum Register (DST_COLORKEY_DR_MIN_REG, R/W, Address = 0xFA00_0720)

The color format of destination colorkey decision reference register is the same as the destination color format.

DST_COLORKEY_DR_MIN_REG	Bit	Description	Initial State
DstDRMinA	[31:24]	Alpha DR MIN value	0x0
DstDRMinR	[23:16]	Red DR MIN value	0x0
DstDRMinG	[15:8]	Green DR MIN value	0x0
DstDRMinB	[7:0]	Blue DR MIN value	0x0

13.5.12.6 Destination Colorkey Decision Reference Maximum Register (DST_COLORKEY_MAX_REG, R/W, Address = 0xFA00_0724)

The color format of destination colorkey decision reference register is the same as the destination color format.

DST_COLORKEY_MAX_REG	Bit	Description	Initial State
DstDRMaxA	[31:24]	Alpha DR MAX value	0xFF
DstDRMaxR	[23:16]	Red DR MAX value	0xFF
DstDRMaxG	[15:8]	Green DR MAX value	0xFF
DstDRMaxB	[7:0]	Blue DR MAX value	0xFF

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Section 10

AUDIO / ETC

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1 AUDIO SUBSYSTEM

1.1 OVERVIEW OF THE AUDIO SUBSYSTEM

The audio subsystem is a special subsystem that supports playback of sound with low power. In other words, this subsystem is used to increase the playback time. It consists of a reconfigurable processor (RP) DSP core, I2S (v5.1) including AHB master port, and 214KB SRAM. Combined with low power scheme, the S5PV210 is designed to play audio with extremely low power.

1.2 KEY FEATURES OF AUDIO SUBSYSTEM

The key features of audio subsystem include:

- Renders low power music play
- Small and adequate for audio application RP
- Supports various audio codecs
- Contains I2S (including AHB master port) to get data from subsystem internal SRAM
- Contains totally 214KB SRAM (160KB continuous) for audio subsystem's internal and external usage

* To know more about the available audio codecs, contact SEC.

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1.3 INPUT/ OUTPUT DESCRIPTION

Signal	I/O	Description	Pad	Type
Xi2s0SCLK	I/O	Specifies bit clock input.	Xi2s0SCLK	Dedicated
Xi2s0LRCLK	I/O	Specifies LR channel clock input.	Xi2s0LRCLK	Dedicated
Xi2s0CDCLK	I/O	Specifies codec clock out.	Xi2s0CDCLK	Dedicated
Xi2s0SDI	I	Specifies I2S serial data input.	Xi2s0SDI	Dedicated
Xi2s0SDO0	O	Specifies I2S serial data out 0.	Xi2s0SDO0	Dedicated
Xi2s0SDO1	O	Specifies I2S serial data out 1.	Xi2s0SDO1	Dedicated
Xi2s0SDO2	O	Specifies I2S serial data out 2.	Xi2s0SDO2	Dedicated

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1.4 BLOCK DIAGRAM OF AUDIO SUBSYSTEM

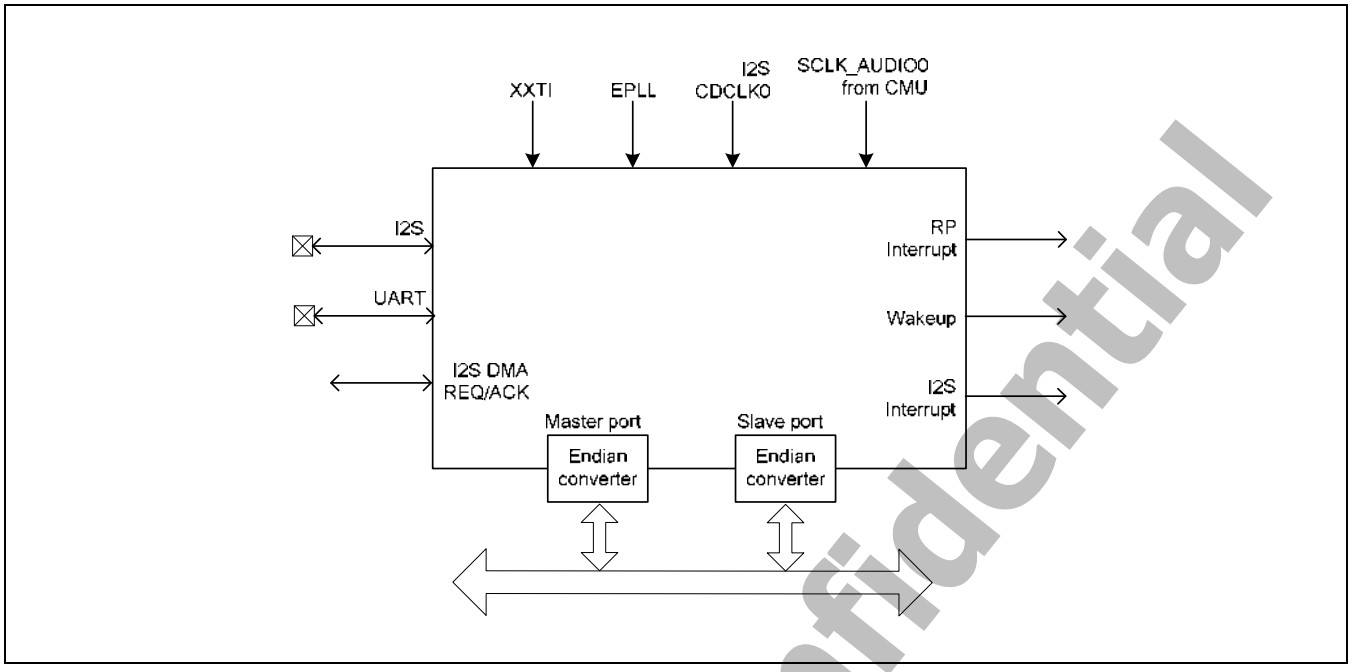

Figure 1-1 Block Diagram of Audio Subsystem

There are two modes for turning the power on and off, namely, normal mode and deep-idle mode.

Both audio subsystem and TOP (S5PV210) work in the Normal mode. However, to save power, you can turn off the TOP. Turning off the TOP means that the S5PV210 goes into the Deep-idle mode. In this mode, the audio subsystem can remain on. The audio subsystem can wake up the TOP (S5PV210) from deep-idle mode, using wake up source such as RP and I2S V51.

The audio subsystem receives four kinds of clock from CMU, namely, XXTI, EPLL, I2SCDCLK0, and SCLK_AUDIO0. The XXTI is a selected clock between main OSC(XXTI) and USB OSC(XusbXTI) which is selected by OM[0].

XXTI, EPLL, and I2SCDCLK0 can be supplied to the audio subsystem when the audio system is on and TOP (S5PV210) is off.

The internal RP uses big-endian scheme, while the external audio subsystem uses little-endian scheme. Therefore, endian converters are used to convert data ordering without using ARM or RP.

Audio subsystem comprises of I2S V5.1 and its own interrupt, and DMA REQ/ ACK ports.

The master port accesses DRAM and IRAM using bus-master modules in audio subsystem.

On the other hand, the slave port accesses all modules in audio subsystem using external audio subsystem modules. All bus-master modules in S5PV210 can assess modules in audio subsystem (excluding RP core).

UART for RP debugging and UART pad are muxed with system UART2. For more information, refer to GPIO User's Manual.

NOTE: For more information about power modes such as Deep-idle, refer to Power Management Unit (PMU) User's Manual.

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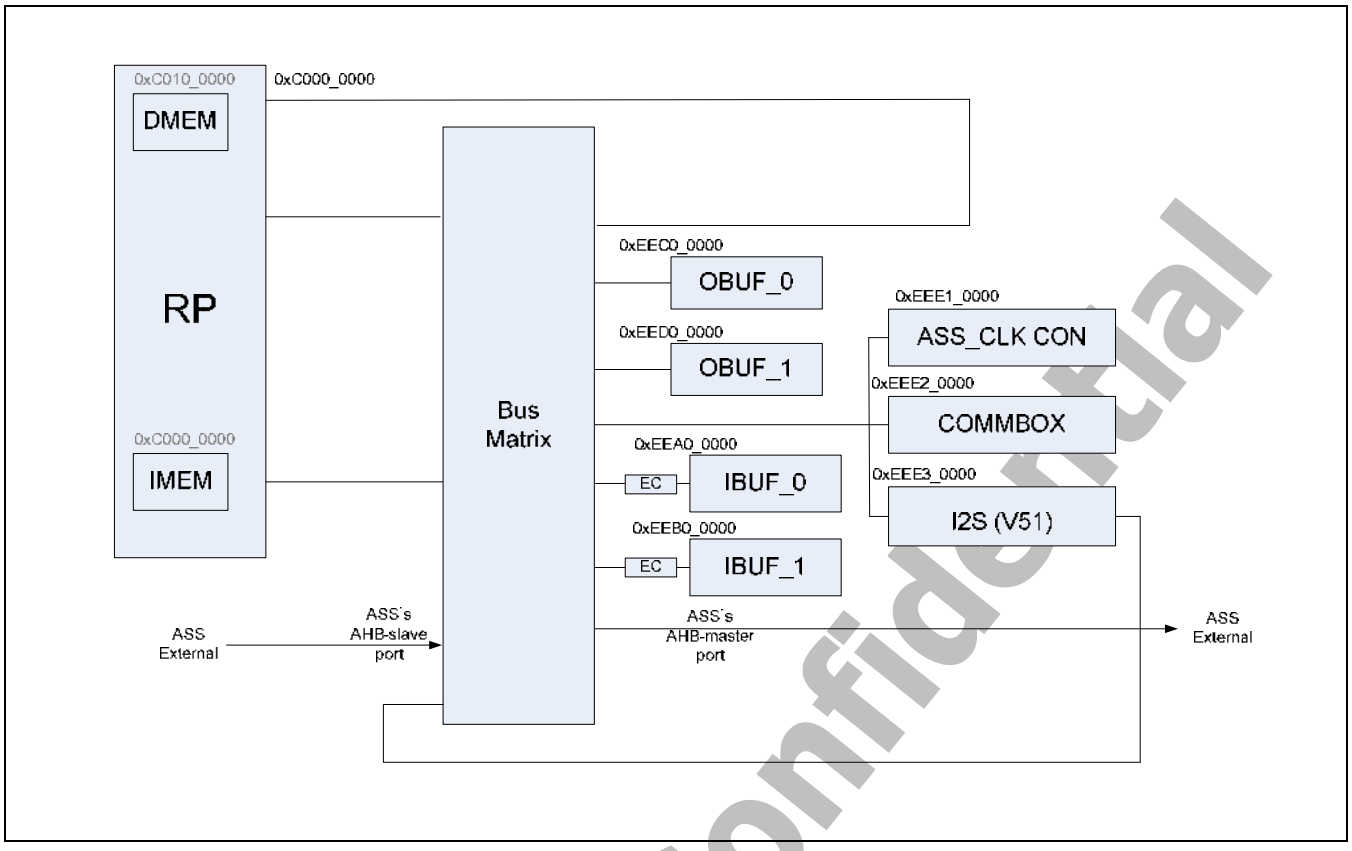

Figure 1-2 Audio Subsystem Block Diagram

The audio subsystem comprises of the following blocks:

- RP: Specifies the DSP core, which is an audio-dedicated DSP for S5PV210.
- IMEM and DMEM: IMEM is used for instruction cache of RP, while DMEM is used for data memory of RP. If RP is not used, the external modules in audio subsystem use IMEM and DMEM for SRAM (IMEM: 64KB and DMEM: 96KB).
- IBUF_0, IBUF_1: Specifies input buffers 0 and 1. 18KB is allocated for each input buffers in RP. These buffers are used by external audio subsystem as data reservoir. There are Endian Converters (ECs) besides IBUF_0 and IBUF_1.
- OBUF_0, OBUF_1: Specifies output buffers 0 and 1. 9KB is allocated for each output buffers in RP. These buffers can be used by external audio subsystem as data reservoir.
- ASS_CLKCON: Specifies the internal clock controller in audio subsystem.
- COMMBOX: Specifies the communication channel between ARM and RP.
- I2S V51: Specifies the main I2S module of S5PV210.

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1.5 FUNCTIONAL DESCRIPTION

1.5.1 RECONFIGURABLE PROCESSOR

Reconfigurable Processor (RP) is a Samsung proprietary configurable DSP core. RP in S5PV210 is configured for low power audio applications.

1.5.2 ASS CLK CON

ASS CLK CON specifies the clock controller for audio subsystem. It also provides clock for modules in the audio subsystem.

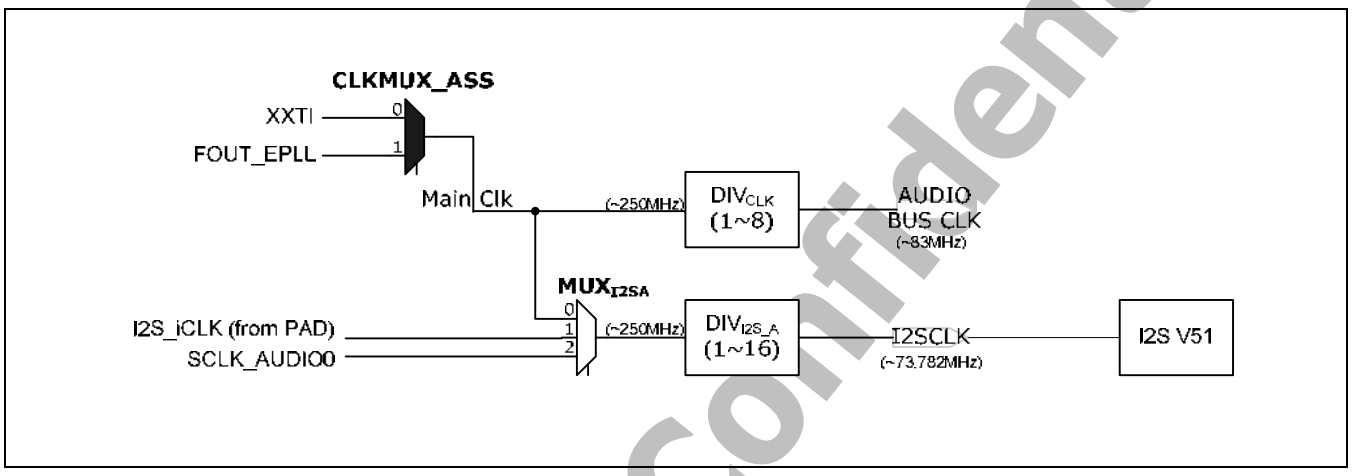

Figure 1-3 Clock Controller in Audio Subsystem

CLKMUX_ASS can be changed at any time. However, it should stop running before MUXI2S_A is changed. The value of divider can also be changed at any time.

1.5.3 COMMBOX

COMMBOX specifies the communication box. It denotes the SFR communication channel between ARM and RP.

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1.5.4 I2S_V51

The major difference between I2S V3.2 and I2S V5.1 lies in the presence of small AHB DMA. The previous version of I2S did not allow the audio data to be played without external DMA. I2S V5.1 allows the audio data to play with its own DMA. I2S DMA issues only 32-bit single read transaction.

I2S V5.1 comprises of an interrupt request signal to wake up ARM if S5PV210 is in the Idle and Deep-idle modes. Interrupt request signal occurs if the pre-defined configuration of I2S DMA operations is complete. After CPU wakes up, CPU prepares, generates, and saves the next audio data to be played in SRAM at audio subsystem. Then CPU is powered off again to save power.

For more information, refer to the I2S_V51 User's Manual.

1.5.5 SRAM

The total memory size in audio subsystem is 214KB SRAM, out of which 64KB is reserved for IMEM, 96KB is reserved for DMEM, 36KB is reserved for IBUF0 and IBUF1, and 18KB is reserved for OBUF0 and OBUF1. These memories can be accessed by both internal and external modules in audio subsystem.

For more information on how to use this SRAM for low power music play, refer to Section 6, "Programming Guide". If low power audio functionality is not needed, 214KB SRAM can be used as data reservoir.

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1.6 REGISTER DESCRIPTION

1.6.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
Audio Subsystem Internal Memory				
IMEM	0xC000_0000 ~0xC000_FFFC	R/W	For RP, instruction cache For external audio subsystem, 64KB SRAM	-
DMEM	ARM decode mode (MISC SFR[3]=0) 0xC001_0000 ~0xC002_7FFC RP decode mode (MISC SFR[3]=1) 0xC010_0000 ~0xC011_7FFC	R/W	For RP, data memory For external audio subsystem, 96KB SRAM	-
IBUF0	0xEEA0_0000 ~ 0xEEA0_47FC	R/W	For RP, input buffer 0 For external audio subsystem, 18KB SRAM	-
IBUF1	0xEEB0_0000 ~0xEEB0_47FC	R/W	For RP, input buffer 1 For external audio subsystem, 18KB SRAM	-
OBUF0	0xEEC0_0000 ~0xEEC0_23FC	R/W	For RP, output buffer 0 For external audio subsystem, 9KB SRAM	-
OBUF1	0xEED0_0000 ~0xEED0_23FC	R/W	For RP, output buffer 1 For external audio subsystem, 9KB SRAM	-
Audio Subsystem CLK CON				
ASS CLK SRC	0xEEE1_0000	R/W	Specifies the clock source select register.	0x0
ASS CLK DIV	0xEEE1_0004	R/W	Specifies the clock divider register.	0x0
ASS CLK GATE	0xEEE1_0008	R/W	Specifies the clock gate register.	0x7f
Commbox				
ASS_INTR	0xEEE2_0000	R/W	Specifies the interrupt from audio subsystem to ARM. Also, it can be used as wake up source.	0x0
SW_DEFINE00	0xEEE2_0004	R/W	Specifies an SFR that can be freely used in the application.	0x0
SW_DEFINE01	0xEEE2_0008	R/W	Specifies an SFR that can be freely used in the application.	0x0
SW_DEFINE02	0xEEE2_000C	R/W	Specifies an SFR that can be freely used in the application.	0x0
SW_DEFINE03	0xEEE2_0010	R/W	Specifies an SFR that can be freely used in the application.	0x0
INST_START_ ADDR	0xEEE2_0014	R/W	Specifies the instruction code start address for external booting.	0x0
SW_DEFINE04	0xEEE2_0018	R/W	Specifies an SFR that can be freely used in the application.	0x0

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Register	Address	R/W	Description	Reset Value
RESET	0xEEE2_0100	R/W	Specifies the software reset of audio sub-system.	0x1
RP_PENDING	0xEEE2_0104	R/W	Specifies the pending control of RP.	0x1
FRM_SIZE	0xEEE2_0108	R/W	Specifies the frame size (word) per output buffer (OBUF0, 1). Upper 20-bits can be used freely.	0x0
SW_DEFINE05	0xEEE2_010C	R/W	Specifies an SFR that can be freely used in the application.	0x0
SW_DEFINE06	0xEEE2_0110	R/W	Specifies an SFR that can be freely used in the application.	0x0
SW_DEFINE07	0xEEE2_0114	R/W	Specifies an SFR that can be freely used in the application.	0x0
SW_DEFINE08	0xEEE2_0118	R/W	Specifies an SFR that can be freely used in the application.	0x0
SW_DEFINE09	0xEEE2_011C	R/W	Specifies an SFR that can be freely used in the application.	0x0
SW_DEFINE10	0xEEE2_0120	R/W	Specifies an SFR that can be freely used in the application.	0x0
SW_DEFINE11	0xEEE2_0124	R/W	Specifies an SFR that can be freely used in the application.	0x0
SW_DEFINE12	0xEEE2_0128	R/W	Specifies an SFR that can be freely used in the application.	0x0
RP_BOOT	0xEEE2_012C	R/W	Controls the RP booting type. Upper 31 bits can be used freely.	0x0
SW_DEFINE13	0xEEE2_0130	R/W	Specifies an SFR that can be freely used in the application.	0x0
SW_DEFINE14	0xEEE2_0134	R/W	Specifies an SFR that can be freely used in the application.	0x0
SW_DEFINE15	0xEEE2_0138	R/W	Specifies an SFR that can be freely used in the application.	0x0
PAD_PDN_ CTRL	0xEEE2_0204	R/W	Controls GPIO PDN for power down.	0x0
MISC	0xEEE2_0208	R/W	Specifies the endian converter. Also, selects the audio decoder.	0x0

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1.6.2 AUDIO SUBSYSTEM CLK CON

To set the registers of audio subsystem CLK CON, refer to *Figure 1-3*.

1.6.2.1 Audio Subsystem Clock Source Register (Audio Subsystem CLK SRC, R/W, Address = 0xEEE1_0000)

AUDIO SUBSYSTEM CLK SRC	Bit	Description	Initial State
Reserved	[31:4]	Reserved	0
MUX_{I2S_A}	[3:2]	10 = SCLK_AUDIO0 01 = IISCDCLK0 (from PAD) 00 = Main CLK	0
Reserved	[1]	This bit must be set as 0	0
CLKMUX_ASS	[0]	1 = FOUT_EPLL 0 = XXTI	0

1.6.2.2 Audio Subsystem Clock Divider Register (Audio Subsystem CLK DIV, R/W, Address = 0xEEE1_0004)

AUDIO SUBSYSTEM CLK DIV	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
I2S_A_RATIO	[7:4]	Specifies the I2S_A clock divider ratio. I2SCLK = $MOUT_{I2S_A}$ / (I2S_A_RATIO+1)	0
AUDIO_BUS_CLK_ RATIO	[3:0]	Specifies the AUD_BUS clock divider ratio. AUDIO_BUS_CLK = $MOUT_{BUS}$ / (AUD_BUS_RATIO+1)	0

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1.6.2.3 Audio Subsystem Clock Gate Register (Audio Subsystem CLK GATE R/W, Address = 0xEEE1_0008)

AUDIO SUBSYSTEM CLK GATE	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
CLK_I2S	[6]	Specifies the gating clock of I2SCLK to I2S (0: mask, 1: pass).	1
AUDIO_BUS_CLK_I2S	[5]	Specifies the gating AUDIO BUS CLK to I2S (0: mask, 1: pass).	1
AUDIO_BUS_CLK_UART	[4]	Specifies the gating AUDIO BUS CLK to UART (0: mask, 1: pass).	1
AUDIO_BUS_CLK_HWA	[3]	Specifies the gating AUDIO BUS CLK to HWA (0: mask, 1: pass).	1
AUDIO_BUS_CLK_DMA	[2]	Specifies the gating AUDIO BUS CLK to DMA (0: mask, 1: pass).	1
AUDIO_BUS_CLK_BUF	[1]	Specifies the gating AUDIO BUS CLK to BUF (IBUF0, 1/ OBUF0, 1) (0: mask, 1: pass).	1
AUDIO_BUS_CLK_RP	[0]	Specifies the gating AUDIO BUS CLK to RP (including IMEM and DMEM) (0: mask, 1: pass).	1

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1.6.3 COMMBOX

Each SW_DEFINE is a 32-bit register, and can be freely used for application.

1.6.3.1 Audio Subsystem Interrupt Register (ASS_INTR, R/W, Address = 0xEEE2_0000)

ASS_INTR	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
Interrupt	[0]	1 = Interrupt and wake-up 0 = No action	0

1.6.3.2 Instruction Start Address Register (INST_START_ADDR, R/W, Address = 0xEEE2_0014)

INST_START_ADDR	Bit	Description	Initial State
Address	[31:0]	Specifies the instruction code start address for external booting.	0

1.6.3.3 Reset Register (RESET, R/W, Address = 0xEEE2_0100)

RESET	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
Reset	[0]	1 = No action 0 = Resets and returns to 1 after two clock cycles	1

1.6.3.4 RP Pending Register (RP_PENDING, R/W, Address = 0xEEE2_0104)

RP_PENDING	Bit	Description	Initial State
Reserved	[31:1]	Reserved	0
Pending	[0]	1 = RP pending 0 = RP running	1

1.6.3.5 FRAME Size Register (FRM_SIZE, R/W, Address = 0xEEE2_0108)

FRM_SIZE	Bit	Description	Initial State
SW_DEFINE	[31:12]	Specifies an SFR that can be freely used in the application.	0
Frame size	[11:0]	Specifies the frame size (word) per output buffer.	0

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1.6.3.6 RP Boot Register (RP_BOOT, R/W, Address = 0xEEE2_012C)

RP_BOOT	Bit	Description	Initial State
SW_DEFINE	[31:1]	Specifies an SFR that can be freely used in the application.	0
RP boot	[0]	1 = Internal (Instruction is located in IMEM) 0 = External (Instruction is located in DRAM and start address is defined at INST_START_ADDR SFR)	0

At ARM decode mode, RP boot bit must be 1.

1.6.3.7 PAD Power Down Control Register (PAD_PDN_CTRL, R/W, Address = 0xEEE2_0204)

GPIO PDN controls power down. The value of each PAD set by this SFR is maintained at Sleep power mode.

PAD_PDN_CTRL	Bit	Description	Initial State
Reserved	[31:9]	Reserved	0
SDO_PDN[2]	[8]	Configure output value of I2S0 SDO[2] PAD 0 = Output 0 1 = Output 1	0
SDO_PDN[1]	[7]	Configure output value of I2S0 SDO[1] PAD 0 = Output 0 1 = Output 1	0
SDO_PDN[0]	[6]	Configure output value of I2S0 SDO[0] PAD 0 = Output 0 1 = Output 1	0
SCLKO_PDN	[5]	Configure output value of I2S0 SCLK PAD 0 = Output 0 1 = Output 1	0
CDCLKO_PDN	[4]	Configure output value of I2S0 CDCLK PAD 0 = Output 0 1 = Output 1	0
LRCLKO_PDN	[3]	Configure output value of I2S0 LRCLK PAD 0 = Output 0 1 = Output 1	0
SCLKO_EN_PDN	[2]	Configure direction of I2S0 SLCK PAD 0 = Input 1 = Output	0
CDCLKO_EN_PDN	[1]	Configure direction of I2S0 CDCLK PAD 0 = Input 1 = Output	0
LRCLKO_EN_PDN	[0]	Configure direction of I2S0 LRCLK PAD 0 = Input 1 = Output	0

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1.6.3.8 MISC Register (MISC, R/W, Address = 0xEEE2_0208)

MISC	Bit	Description	Initial State
Reserved	[31:4]	Reserved	0
Audio decoder select	[3]	Specifies address range of DMEM 1 = 0xC010_0000 ~ 0xC011_7FFC, when RP is used for decoder 0 = 0xC001_0000 ~0xC002_7FFC, when ARM is used for decoder	0
System timer debug	[2]	Specifies usage of Xi2s0SDO1 and Xi2s0SDO2 pad 1 = Xi2s0SDO1 is used as monitor of system timer's tick, and Xi2s0SDO1 is used as monitor of system timer's interrupt 0 = Xi2s0SDO1 is used as I2SD1, and Xi2s0SDO2 is used as I2SD2	0
Endian converter	[1]	Specifies the endian converter for IBUF1 write path. 1 = Big endian 0 = Little endian	0
Endian converter	[0]	Specifies the endian converter for IBUF0 write path 1 = Big endian 0 = Little endian	0

There are endian converters between external and internal audio subsystems (refer to *Figure 1-1*. To set them, AUDIO_ENDIAN SFR at Clock Management Unit (CMU) is used.

* ENDIAN converters setting guide

Register[Bit]	Path	Guide value
AUDIO_ENDIAN[3]	RP read	1
AUDIO_ENDIAN[2]	RP write	0
AUDIO_ENDIAN[1]	ARM read	0
AUDIO_ENDIAN[0]	ARM write	0
MISC[1]	IBUF1 write	1
MISC[0]	IBUF0 write	1

Since having ENDIAN converters, Read/write accesses must always be in 32-bit units (byte or half word accesses are not allowed).

For more details on I2S V51, refer to the I2S V51 User's Manual.

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2 IIS MULTI AUDIO INTERFACE

2.1 OVERVIEW OF IIS MULTI AUDIO INTERFACE

Inter-IC Sound (IIS) is one of the popular digital audio interface. The IIS bus handles audio data and the other signals, namely, sub-coding and control, are transferred separately. It is possible to transmit data between two IIS bus. To minimize the number of pins required and to keep wiring simple, basically, a 3-line serial bus is used. This consists of a line for two time-multiplexed data channels, a word select line and a clock line.

IIS interface transmits or receives sound data from external stereo audio codec. To transmit and receive data, 32bitsx64 FIFOs (First-In-First-Out) for each channel are included and DMA transfer mode to transmit and receive samples can be supported. IIS-specific clock can be supplied from internal system clock controller through IIS clock divider or direct clock source.

IIS V5.1 can handle up to 2 sound sources. For example, OS (Operating Sound)-controlled sound can be delivered to primary sound path and OS-independent sound can be delivered to secondary sound path. IIS V5.1 can mix primary sound source and secondary sound source.

2.2 KEY FEATURES OF IIS MULTI AUDIO INTERFACE

- Mixes up to two sound sources: Primary and Secondary sound source.
- Primary sound source can drive up to 5.1ch IIS-bus for audio interface with external DMA-based operation
- Secondary sound source can support stereo sound channels with internal DMA
- Serial, 8/16/24-bit per channel data transfers
- Supports IIS, MSB-justified and LSB-justified data format
- IIS v5.1 interrupt can wake-up system from IDLE and DEEP_IDLE mode.
- Master /slave mode support
- Auxiliary clock out support for codec chip

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2.3 BLOCK DIAGRAM OF IIS MULTI AUDIO INTERFACE

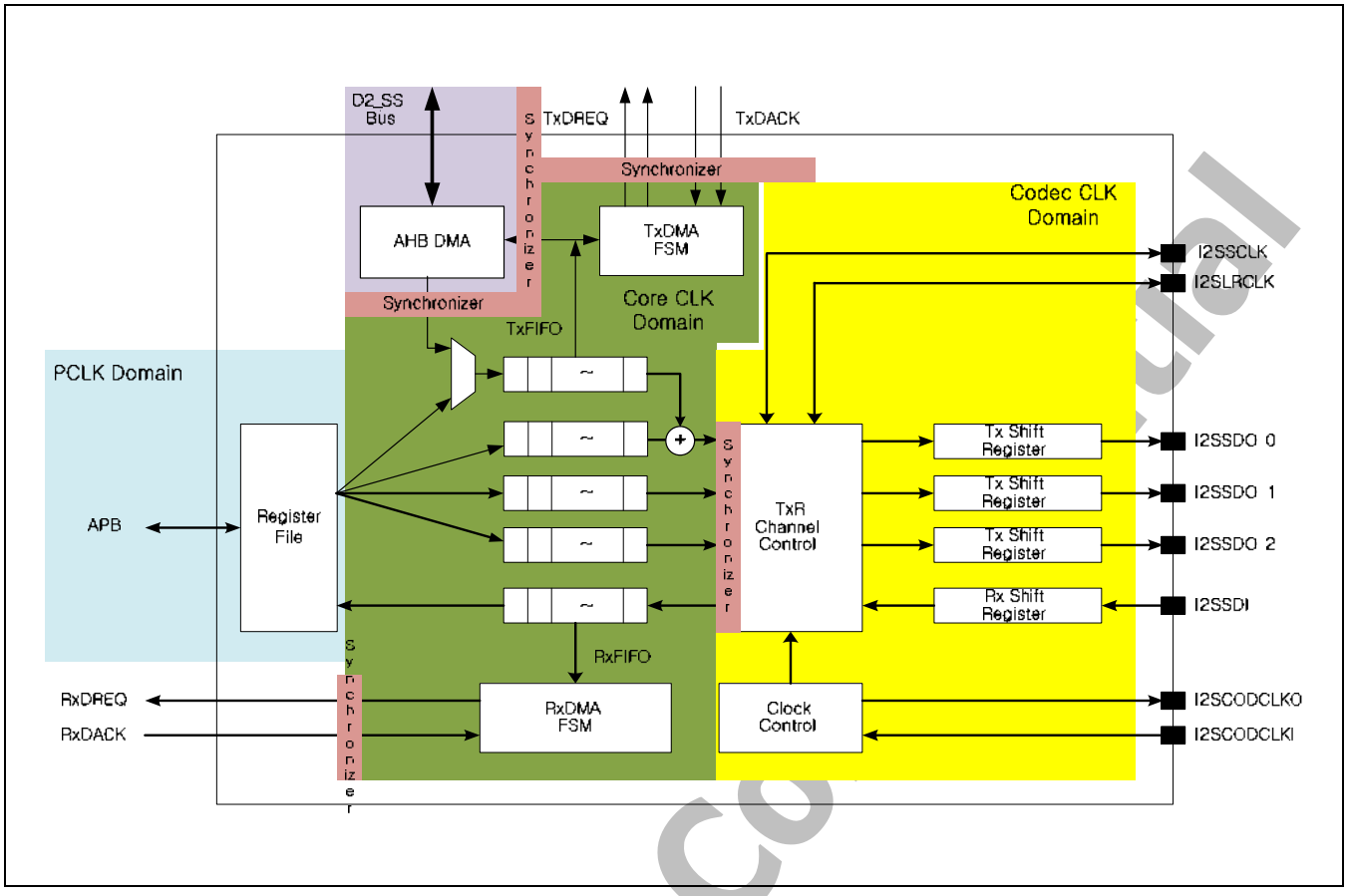

Figure 2-1 IIS-Bus Block Diagram

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2.4 FUNCTIONAL DESCRIPTIONS

IIS interface consists of register bank, FIFOs, shift registers, clock control, DMA finite state machine, and channel control block as shown in *Figure 2-1*. Note that each FIFO has 32-bit width and 64-depth structure, which contains left/right channel data. Thus, FIFO access and data transfer are handled with left/right pair unit. Figure 2-1 shows the functional block diagram of IIS interface.

2.4.1 MASTER/SLAVE MODE

Master/Slave mode shows direction of I2SLRCLK and I2SSCLK. If IIS bus interface transmits I2SLRCLK and I2SSCLK to IIS codec, IIS bus is master mode. If IIS bus interface receives I2SLRCLK and I2SSCLK from IIS codec, IIS bus is slave mode. To select master or slave mode, set MSS bit of IISMOD register.

TX/RX mode indicates the direction of data flow. If IIS bus interface transmits data to IIS codec, this indicates TX mode. Conversely, IIS bus interface receives data from IIS codec, this indicates RX mode.

Figure 2-2 shows AUDIO BUS CLK. For more information, refer to 10.01.S5PV210_Low Power Audio Subystem.

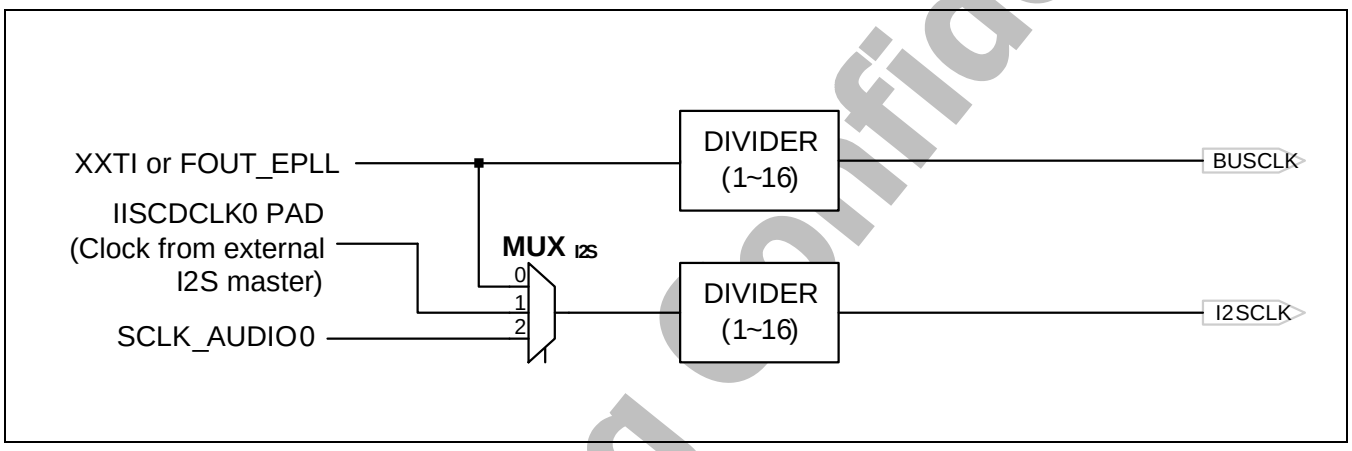

Figure 2-2 Clock Controller in Audio Sub-System

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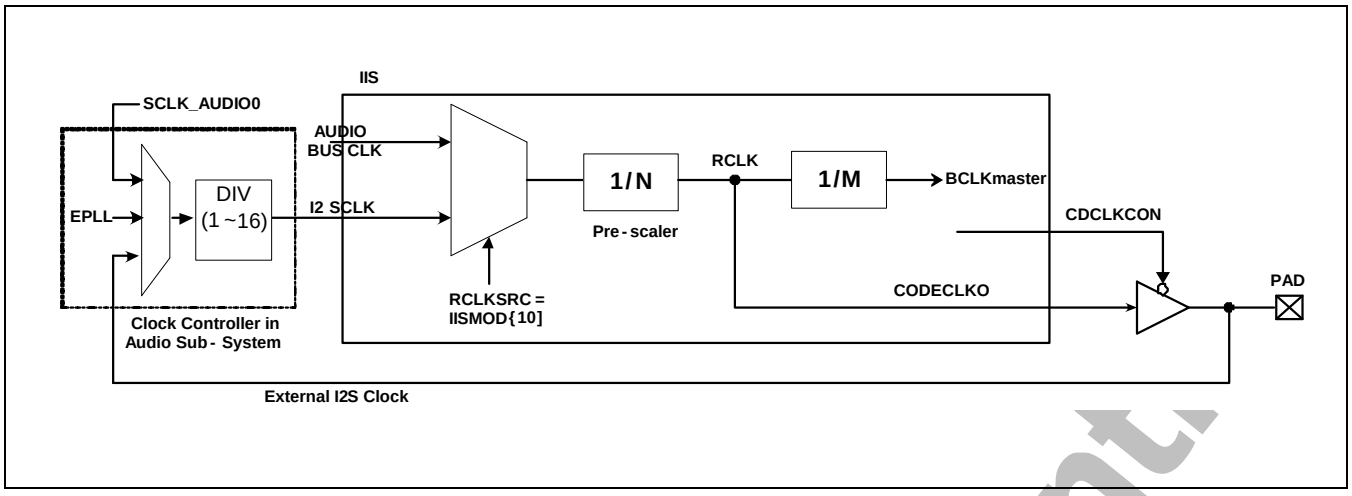

Figure 2-3 IIS Clock Control Block Diagram

Figure 2-3 shows the route of the root clock with setting in IIS clock control block and system controller. RCLK indicates root clock and RCLKSRC chooses a clock source of RCLK between AUDIO BUS CLK and I2SCLK. The IIS pre-scaler (clock divider) is employed to generate a root clock with divided frequency from source clock.

In master mode, the root clock is divided to generate I2SSCLK and I2SLRCLK. In slave mode, this clock is not used to generate I2SSCLK and I2SLRCLK.

CDCLKCON controls direction of CDCLK GPIO pad. The direction is set by CDCLKCON SFR bit (IISMOD[12]). When CDCLKCON SRF bit is 0, auxiliary clock out is supported for Codec chip at both cases of Master/Slave mode. In this case, RCLK can be supplied to external IIS CODEC chip. When CDCLKCON SRF bit is 1, External I2S clock is supplied from external device. This is useful when internal clock sources are not adequate for generating exact I2SSCLK and I2SLRCLK.

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Figure 2-4 and *Table 2-1* shows typical usage example of Master EPLL out, Master External clock and Slave.

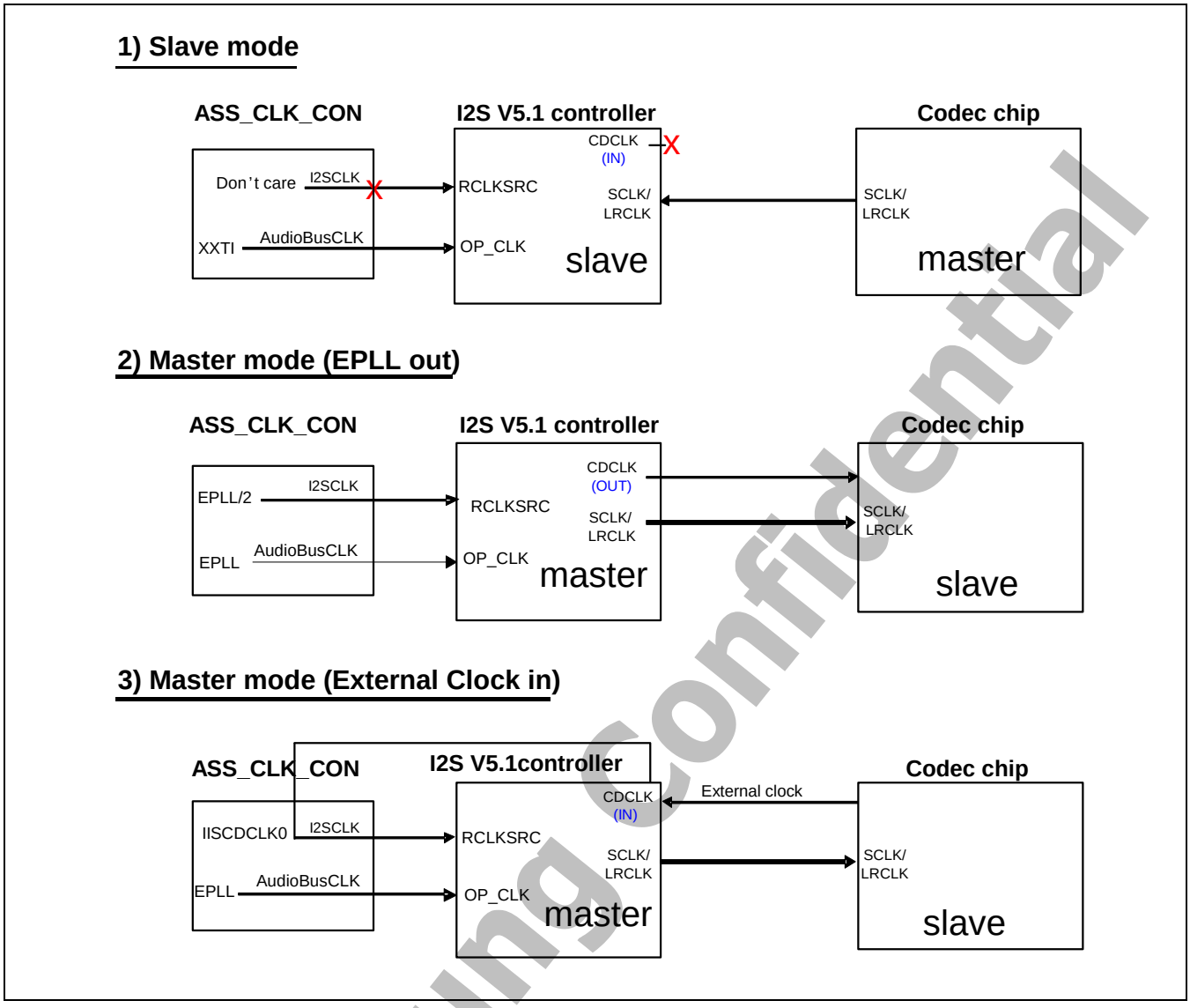

Figure 2-4 Master/Slave Modes of IIS

Table 2-1 Typical Usage of Master/Slave Modes

Mode	AudioSS CLK_CON		IIS v5.1 IISMOD			
	AudioBusClk	I2SCLK	MSS	RCLKSRC	OP_CLK	CDCLKCON
Slave mode	XXTI or EPLL	Gating	1 (Slave)	1 (I2SCLK)	3 (AudioBusClk)	1 (In)
Master mode (EPLL out)	EPLL	EPLL/2	0 (Master)	1 (I2SCLK)	3 (AudioBusClk)	0 (Out)
Master mode (External clock in)	EPLL	IISCDCLK0	0 (Master)	1 (I2SCLK)	3 (AudioBusClk)	1 (In)

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2.4.1.1 External DMA Transfer

To transfer up to 5.1 channel primary sound from s/w mixer to IIS, use external DMA or SFR interface. To play primary sound for 5.1 channels or record 2 channel sound, IIS has TXFIFO0, TXFIFO1, TXFIFO2, TXFIFO_S and RXFIFO registers. IIS will mix primary sound in TXFIFO0 and secondary sound in TXFIFO_S and output mixed sound stream to external codec logic.

In the external DMA transfer mode, use external DMA controller to access the transmitter or receiver FIFO. The transmitter or receiver FIFO state activates DMA service request internally. The FTXEMPT, FRXEMPT, FTXFULL, and FRXFULL bits of I2SCON register represent the transmitter or receiver FIFO data state. Especially, FTXEMPT and FRXFULL bit are the ready flag for DMA service request; the transmit DMA service request is activated when TXFIFO is not empty and the receiver DMA service request is activated when RXFIFO is not full.

The external DMA transfer uses only handshaking method for single data. Note that during external DMA acknowledge activation; the data read or write operation should be performed.

* Reference: DMA request point

- TX mode: (FIFO is not full) & (TXDMACTIVE is active)
- RX mode: (FIFO is not empty) & (RXDMACTIVE is active)

2.4.1.2 Internal DMA Transfer

To transfer up to 2 channel secondary sound to IIS, use internal DMA or SFR interface. To play secondary sound for 2 channels, internal DMA in IIS gets sound data from address range between 0xC000_0000 and 0xC01F_FFFF (when ARM decodes encoded music file.) or between OBUF0 and OBUF1 (when RP decodes encoded music file.) to TXFIFO_S. IIS will mix primary sound in TXFIFO0 and secondary sound in TXFIFO_S and output mixed sound stream to external codec logic.

Like external DMA transfer mode, in the internal DMA transfer mode, the internal DMA is activated when TXFIFO_S is not full. After activation, internal DMA runs according to SFR configurations and signals an interrupt after completion.

- It only supports single transfer in both Internal & External DMA transfer mode.
- Refer OBUF0 and OBUF1 at 10.01.S5PV210_Low Power Audio Subsystem chapter.

2.4.1.3 Sound Mixing

IIS can mix primary sound in TXFIFO0 and secondary sound in TXFIFO_S when two sound sources have the same sampling rate and PCM format.

- If overflow occurs, then mixer saturates output value.
- Mixer can handle Different Bit Length. (Controlled by BLC bit at IISMOD SFR)

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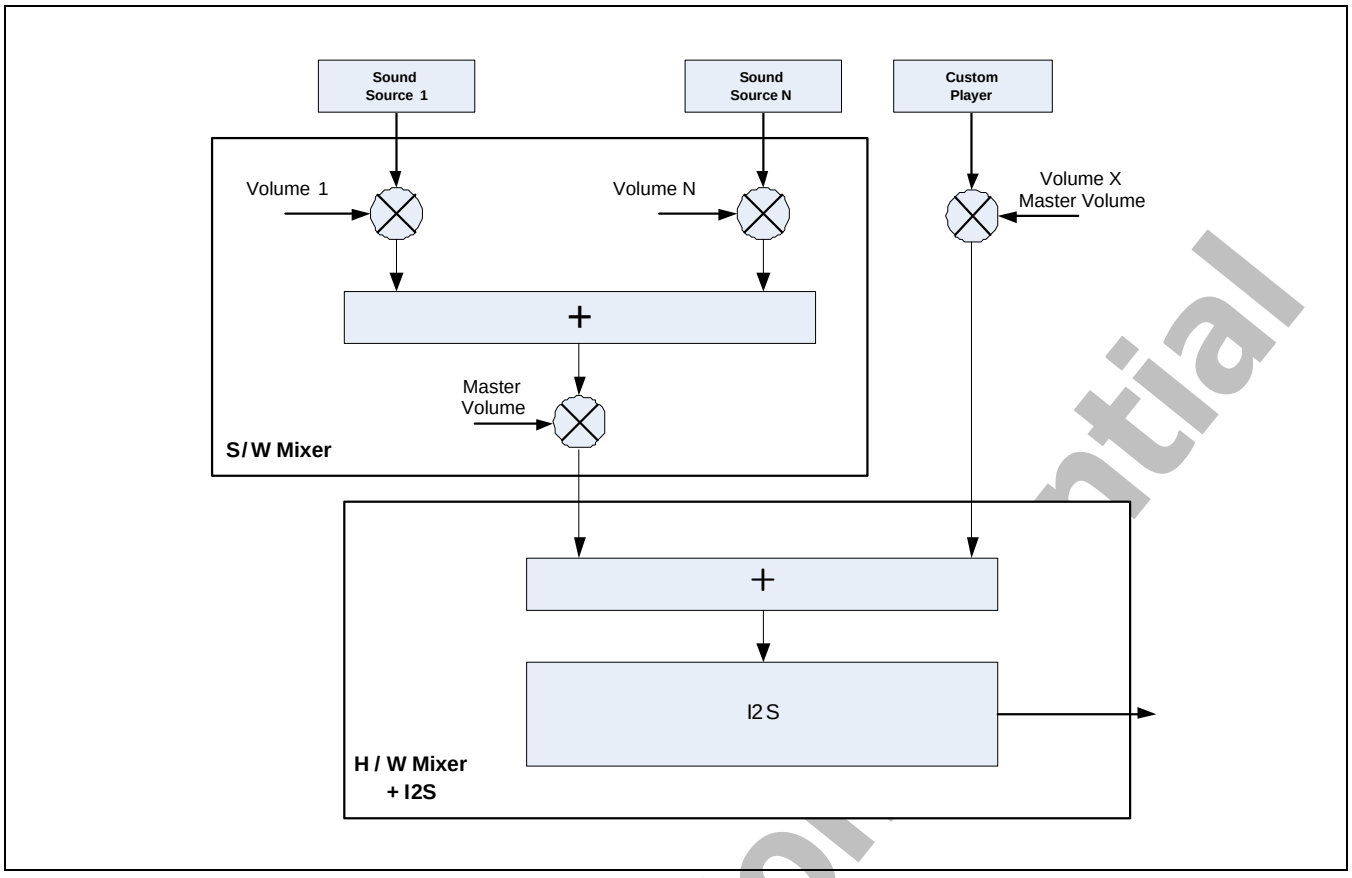

Figure 2-5 Concept of Mixer in IIS

This function has two limitations:

1. Normalization should be pre-processed in S/W configurations or settings.
2. Synchronization between two sound sources is not guaranteed.

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2.5 AUDIO SERIAL DATA FORMAT

2.5.1 IIS-BUS FORMAT

The IIS bus has four lines including serial data input I2SSDI, serial data output I2SSDO, left/right channel select clock I2SLRCLK, and serial bit clock I2SSCLK; master generates I2SLRCLK and I2SSCLK.

Serial data is transmitted in 2's complement with the MSB first with a fixed position, whereas the position of the LSB depends on the word length. The transmitter sends the MSB of the next word at one clock period after the I2SLRCLK is changed. Serial data sent by the transmitter can be synchronized either with the trailing or with the leading edge of the clock signal.

The LR channel select line indicates the direction of left or right channel being transmitted. I2SLRCLK may be changed either on a trailing or leading edge of the serial clock, but it does not need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The I2SLRCLK line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word.

2.5.2 MSB (LEFT) JUSTIFIED

MSB-Justified (Left-Justified) format is similar to IIS bus format, except that in MSB-justified format, the transmitter always sends the MSB of the next word at the same time whenever the I2SLRCLK is changed.

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2.5.3 LSB (RIGHT) JUSTIFIED

LSB-Justified (Right-Justified) format is opposite to the MSB-justified format. In other word, the transferring serial data is aligned with ending point of I2SLRCLK transition.

Figure 2-6 shows the audio serial format of IIS, MSB-justified, and LSB-justified. Note that in this figure, the word length is 16-bit and I2SLRCLK makes transition every 24 cycle of I2SSCLK (BFS is 48 fs, where fs is sampling frequency; I2SLRCLK frequency).

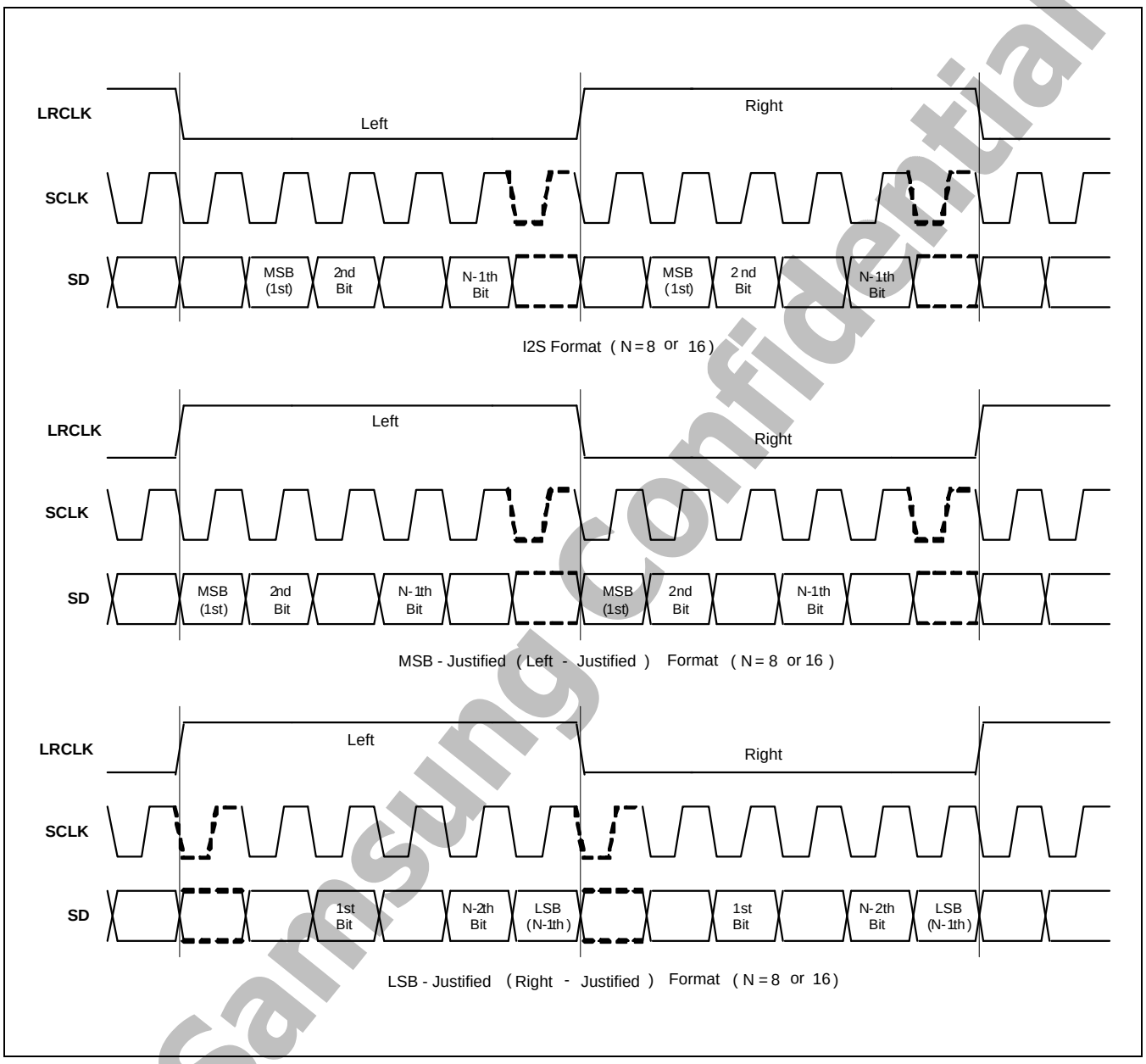

Figure 2-6 IIS Audio Serial Data Formats

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2.6 PCM BIT LENGTH (BLC), RFS DIVIDER AND BFS DIVIDER FOR SAMPLING FREQUENCY (IISLRCLK), SERIAL BITCLK(IISSCLK), AND ROOT CLOCK(RCLK)

When IIS interface Controller operates as master, IIS interface Controller generates IISLRCLK and IISSCLK that is Root Clock is divided using RFS and BFS value. To decide Sampling Frequency – IISLRCLK -, BLC, BFS, and RFS are selected first. Optionally, IIS interface Controller clocks out Root clock as IISCDCLK for codec master clock (if source of root clock is not IISEXTCDCLK).

In slave mode, you must set the value of BLC, BFS and RFS similar to master (ex: Codec). Because IIS interface controller needs these value for correct operation.

2.6.1 PCM WORD LENGTH AND BFS DIVIDER

PCM Word Length (BLC) value is selected first, because the value affects BFS value. *Table 2-2* shows BFS available value as BLC.

Table 2-2 Allowed BFS Value as BLC

PCM Bit length(BLC)	8-bit	16-bit	24-bit
Available BFS value	16fs, 24fs, 32fs, 48fs	32fs, 48fs	48fs

2.6.2 BFS DIVIDER AND RFS DIVIDER

RFS value is selected when BFS is selected *Table 2-3* shows RFS available value as BFS.

Table 2-3 Allowed RFS Value as BFS

BFS Divider	16fs, 32fs	24fs, 48fs
Available RFS value	256fs, 384fs, 512fs, 768fs.	384fs, 768fs.

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2.6.3 RFS DIVIDER AND ROOT CLOCK

Table 2-4 shows relationship between ROOT CLOCK, IISLRCLK and RFS. RCLK is clock divided by IIS pre-scaler (IISPSR) that is selected by IMS

Table 2-4 Root Clock Table (MHz)

IISLRCK / RFS	8.000 kHz	11.025 kHz	16.000 kHz	22.050 kHz	32.000 kHz	44.100 kHz	48.000 kHz	64.000 kHz	88.200 kHz	96.000 kHz
256fs	2.0480	2.8224	4.0960	5.6448	8.1920	11.2896	12.2880	16.3840	22.5792	24.5760
384fs	3.0720	4.2336	6.1440	8.4672	12.2880	16.9344	18.4320	24.5760	33.8688	36.8640
512fs	4.0960	5.6448	8.1920	11.2896	16.3840	22.5792	24.5760	32.7680	45.1584	49.1520
768fs	6.1440	8.4672	12.2880	16.9344	24.5760	33.8688	36.8640	49.1520	67.7376	73.7280

Root Clock Frequency = fs * (256, 384, 512 or 768)

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2.7 PROGRAMMING GUIDE

The IIS bus interface can be accessed either by the processor using programmed I/O instructions or by the DMA controller.

2.7.1 INITIALIZATION

1. Before you use IIS bus interface, you must configure GPIOs to IIS mode. Check signal's direction. I2SLRCLK, I2SSCLK and I2SCDCLK is inout-type. The I2SSDI and I2SSDO is input and output respectively.
2. Select clock source. S5PV210 has three clock sources, namely, Audio bus clock, EPLL and external codec. For more information, refer *Figure 2-2* and *Figure 2-3*.

2.7.2 PLAY MODE (TX MODE) WITH DMA

1. TXFIFO is flushed before operation. If you do not distinguish Master/Slave mode from TX/RX mode, you must study Master/Slave mode and TX/RX mode. Refer Master/Slave chapter.
2. Configure I2SMOD register and I2SPSR (IIS pre-scaler register).
3. To operate system in stability, the internal TXFIFO should be almost full before transmission. To satisfy this, start TXDMA before asserting I2SACTIVE.
4. Basically, IIS bus does not support the interrupt. Therefore, you can only check state by polling through accessing SFR.
5. If TXFIFO is full, you can assert I2SACTIVE.

2.7.3 RECORDING MODE (RX MODE) WITH DMA

1. RXFIFO is flushed before operation. Also, if you don't distinguish between Master/Slave mode and TX/RX mode, you must study Master/Slave mode and TX/RX mode. Refer Master/Slave chapter.
2. Configure I2SMOD register and I2SPSR (IIS pre-scaler register).
3. To operate system in stability, the internal RXFIFO should have at least one data before DMA operation. To satisfy this, assert I2SACTIVE before starting RXDMA.
4. Check RXFIFO state by polling through accessing SFR.
5. If RXFIFO is not empty, start RXDMACTIVE.

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2.7.4 EXAMPLE CODE

2.7.4.1 TX Channel

The IIS TX channel provides a single stereo compliant output. The transmit channel can operate in master or Slave mode. Data is transferred between the processor and the IIS controller via an APB access or a DMA access.
The processor must write words in multiples of two (i.e. for left and right audio sample). The words are serially shifted out timed with respect to the audio bitclk, SCLK and word select clock, LRCLK.

TX Channel has 64X32 bits wide FIFO where the processor or DMA can write upto 16 left/right data samples after enabling the channel for transmission.
An Example sequence is as follows:

Ensure the Audio bus clock and CDCLK are coming correctly to the IIS controller and FLUSH the TX FIFO using the TFLUSH bit in the I2SFIC Register (IIS FIFO Control Register).

Please ensure that IIS Controller is configured in one of the following modes.

- TX only mode
- TX/RX simultaneous mode

This can be done by programming the TXR bit in the I2SMOD Register (IIS Mode Register).

1. Then Program the following parameters according to the need
   - MSS, RCLKSRC
   - SDF
   - BFS
   - BLC
   - LRP
     For Programming, the above-mentioned fields please refer I2SMOD Register (IIS Mode Register).
2. Once ensured that the input clocks for IIS controller are up and running and step 1 and 2 have been completed we can write to TX FIFO.

The write to the TX FIFO has to be carried out thorough the I2STXD Register (IIS TX FIFO Register)
This 32-bit data will occupy position 0 of the FIFO and any further data will be written to position 2, 3 and so on.

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The Data is aligned in the TX FIFO for 8-bit/channel or 16-bit/channel BLC as shown in the *Figure 2-7*.

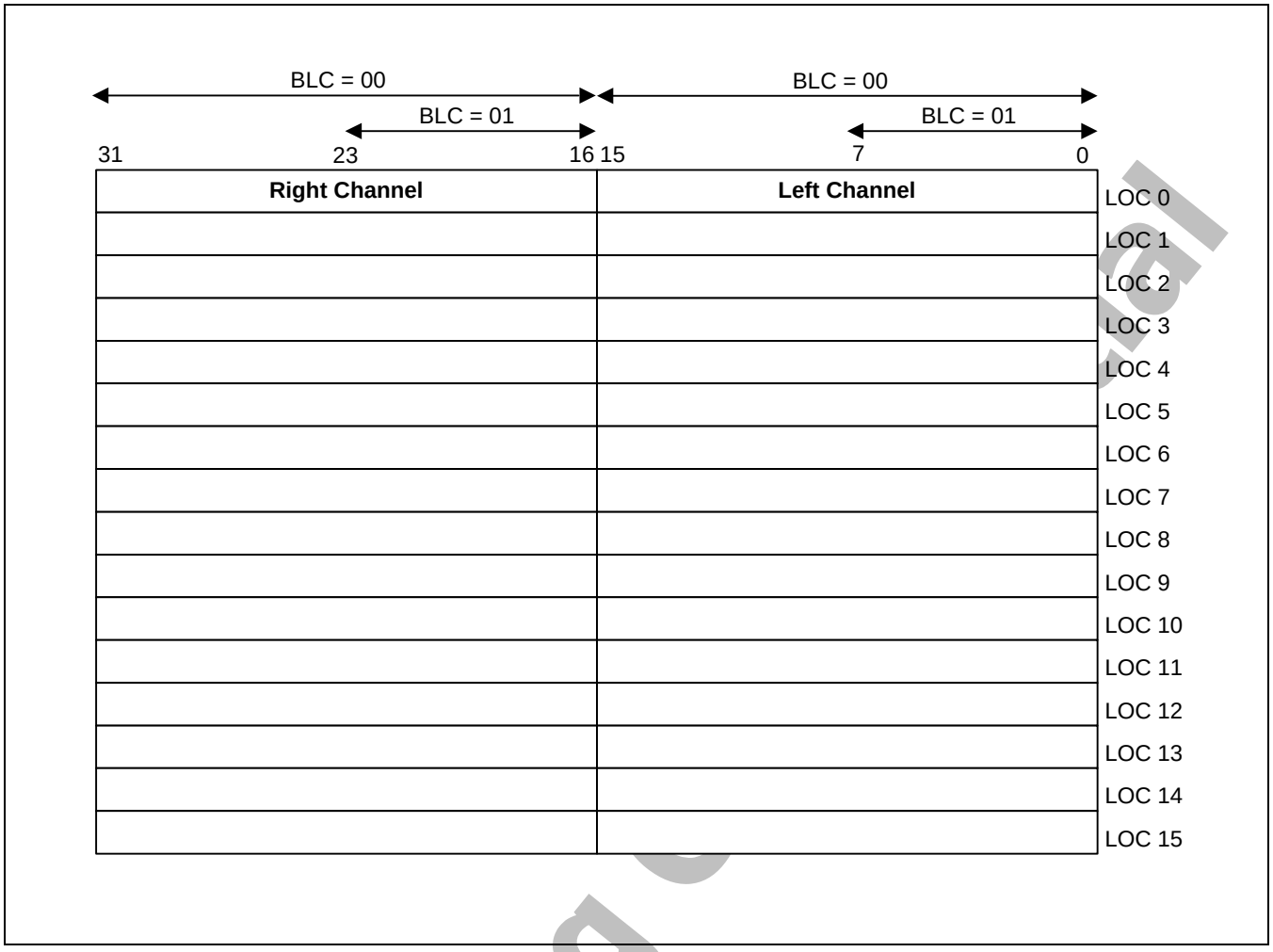

Figure 2-7 TX FIFO Structure for BLC = 00 or BLC = 01

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The Data is aligned in the TX FIFO for 24-bit/channel BLC as shown in *Figure 2-8*.

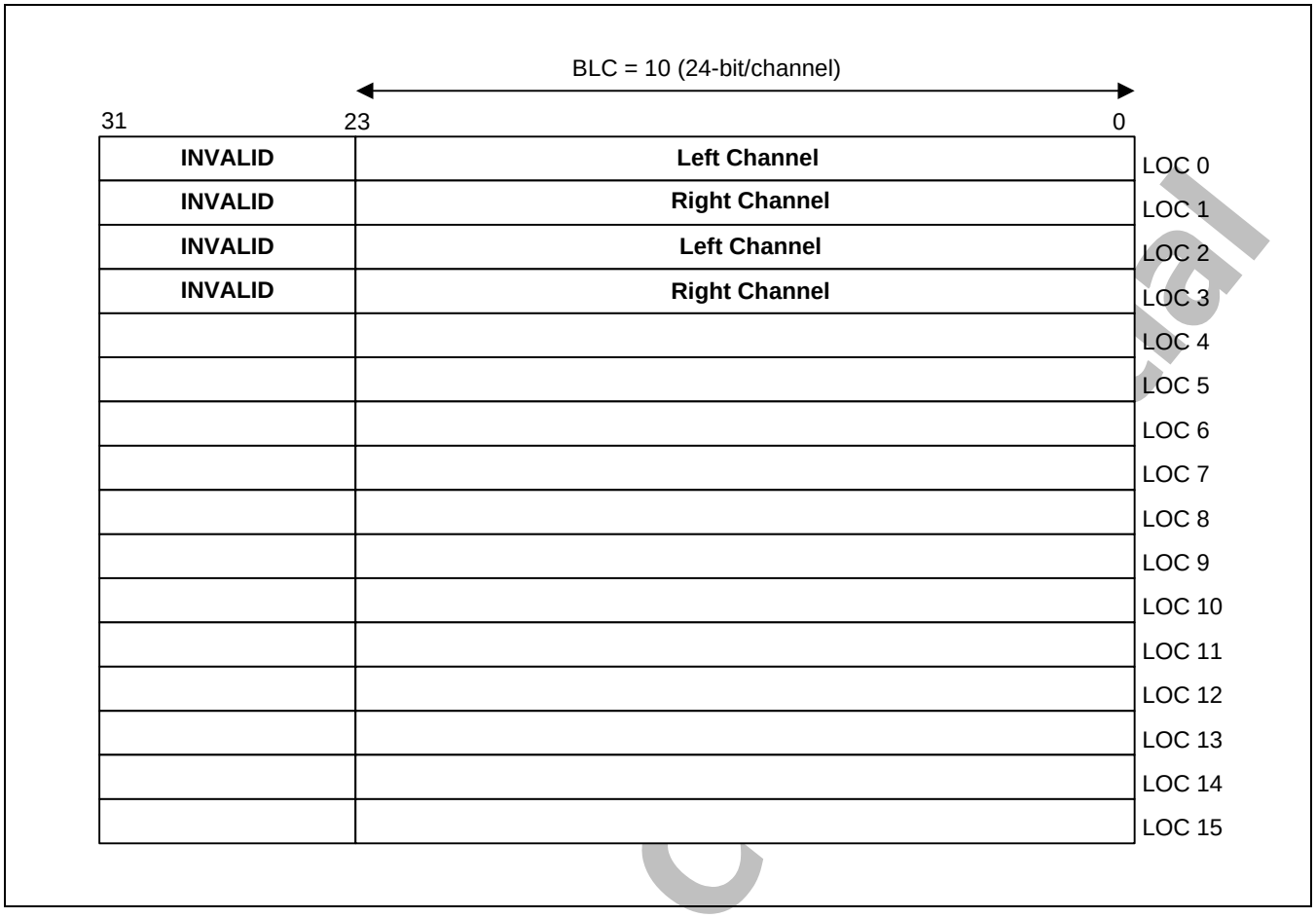

Figure 2-8 TX FIF0 Structure for BLC = 10 (24-bit/channel)

Once the data is written to the TX FIFO the TX channel can be made active by enabling the I2SACTIVE bit in the I2SCON Register (IIS Control Register).
The data is then serially shifted out with respect to the bit clock SCLK and word select clock LRCLK.

The TXCHPAUSE in the I2SCON Register (IIS Control Register) can stop the serial data transmission on the I2SSDO.The transmission is stopped once the current Left/Right channel is transmitted.
If the control registers in the I2SCON Register (IIS Control Register) and I2SMOD Register (IIS Mode Register) are to be reprogrammed then it is advisable to disable the TX channel.

If the TX channel is enabled while the FIFO is empty, no samples are read from the FIFO.
The Status of TX FIFO can be checked by checking the bits in the I2SFIC Register (IIS FIFO Control Register).

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2.7.4.2 RX Channel

The IIS RX channel provides a single stereo compliant output. The receive channel can operate in master or slave mode. Data is received from the input line and transferred into the RX FIFO. The processor can then read this data via an APB read or a DMA access can access this data.

RX Channel has 64 X 32-bit wide RX FIFO where the processor or DMA can read upto 16 left/right data samples after enabling the channel for reception.

An Example sequence is as follows:

Ensure the Audio bus clock and CDCLK are coming correctly to the IIS controller and FLUSH the RX FIFO using the RFLUSH bit in the I2SFIC Register (IIS FIFO Control Register) and the I2S controller is configured in any of the modes

- Receive only.
- Receive/Transmit simultaneous mode

This can be done by Programming the TXR bit in the I2SMOD Register (IIS Mode Register)

1. Then Program the following parameters according to the need
   - MSS, RCLKSRC
   - SDF
   - BFS
   - BLC
   - LRP
     For Programming, the above mentioned fields please refer I2SMOD Register (IIS Mode Register)
2. Once ensured that the input clocks for IIS controller are up and running and step 1 and 2 have been completed user must put the I2SACTIVE high to enable any reception of data, the IIS Controller receives data on the LRCLK change.

The Data must be read from the RX FIFO using the I2SRXD Register (IIS RX FIFO Register) only after looking at the RX FIFO count in the I2SFIC Register (IIS FIFO Control Register). The count would only increment once the complete left channel and right have been received. The Data is aligned in the RX FIFO for 8-bits/channel or 16-bits/channel BLC as shown in *Figure 2-9* .

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Figure 2-9 RX FIFO Structure for BLC = 00 or BLC = 01

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The Data is aligned in the RX FIFO for 24-bit/channel BLC as shown in *Figure 2-10*.

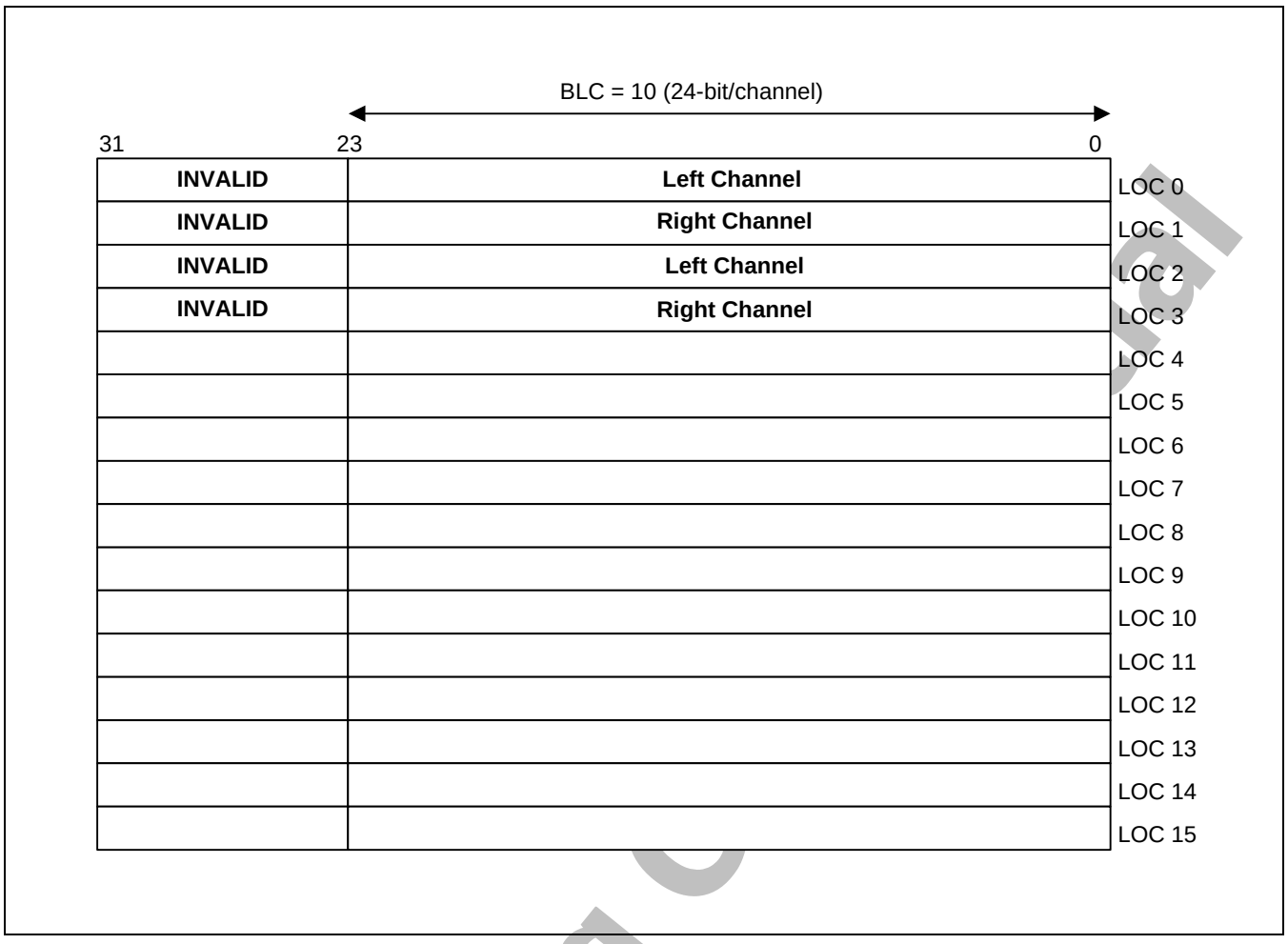

Figure 2-10 RX FIF0 Structure for BLC = 10 (24-bit/channel)

The RXCHPAUSE in the I2SCON register can stop the serial data reception on the I2SSDI. The reception is stopped once the current Left/Right channel is received.
If the control registers in the I2SCON Register (IIS Control Register) and I2SMOD Register (IIS Mode Register) are to be reprogrammed then it is advisable to disable the RX channel.

The Status of RX FIFO can be checked by checking the bits in the I2SFIC Register (IIS FIFO Control Register).

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2.8 IO DESCRIPTION

Signal	I/O	Description	Pad	Type
Xi2s0SCLK	I/O	IIS Serial clock (Bit clock)	Xi2s0SCLK	Dedicated
Xi2s0LRCLK	I/O	IIS LR channel clock	Xi2s0LRCLK	Dedicated
Xi2s0CDCLK	I/O	Auxiliary clock out for codec chip, IIS external clock input	Xi2s0CDCLK	Dedicated
Xi2s0SDI	I	IIS serial data input	Xi2s0SDI	Dedicated
Xi2s0SDO0	O	IIS serial data out 0	Xi2s0SDO0	Dedicated
Xi2s0SDO1	O	IIS serial data out 1	Xi2s0SDO1	Dedicated
Xi2s0SDO2	O	IIS serial data out 2	Xi2s0SDO2	Dedicated

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2.9 REGISTER DESCRIPTION

2.9.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
IISCON	0xEEE3_0000	R/W	Specifies the IIS interface control register	0x000
IISMOD	0xEEE3_0004	R/W	Specifies the IIS interface mode register	0x0
IISFIC	0xEEE3_0008	R/W	Specifies the IIS interface primary Tx FIFO & Rx FIFO control register	0x0
IISPSR	0xEEE3_000C	R/W	Specifies the IIS interface clock divider control register	0x0
IISTXD	0xEEE3_0010	W	Specifies the IIS interface transmit primary sound data register	0x0
IISRXD	0xEEE3_0014	R	Specifies the IIS interface receive data register	0x0
IISFICS	0xEEE3_0018	R/W	Specifies the IIS interface secondary TXFIFO_S control register	0x0
IISTXDS	0xEEE3_001C	W	Specifies the IIS interface secondary transmit data register	0x0
IISAHB	0xEEE3_0020	R/W	Specifies the IIS AHB DMA control register	0x0
IISSTR0	0xEEE3_0024	R/W	Specifies the IIS AHB DMA start address0 register	0x0
IISSIZE	0xEEE3_0028	R/W	Specifies the IIS AHB DMA size register	0x7FFF_0000
IISTRNCNT	0xEEE3_002C	R	Specifies the IIS AHB DMA transfer count register	0x0
IISLVL0ADDR	0xEEE3_0030	R/W	Specifies the IIS AHA DMA Interrupt level 0 register	0x0000_0000
IISLVL1ADDR	0xEEE3_0034	R/W	Specifies the IIS AHA DMA Interrupt level 1 register	0x0000_0000
IISLVL2ADDR	0xEEE3_0038	R/W	Specifies the IIS AHA DMA Interrupt level 2 register	0x0000_0000
IISLVL3ADDR	0xEEE3_003C	R/W	Specifies the IIS AHA DMA Interrupt level 3 register	0x0000_0000
IISSTR1	0xEEE3_0040	R/W	Specifies the IIS AHB DMA start address1 register	0x0

NOTE: All registers of IIS interface are accessible by word unit with STR/LDR instructions.

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2.9.1.1 IIS Interface Control Register (IISCON, R/W, Address = 0xEEE3_0000)

IISCON	Bit	Description	R/W	Initial State
SW_RST	[31]	IIS s/w reset control. This should be set to 1 after IIS clock is stable. 0 = Reset IIS module (default) 1 = Un-reset IIS module Before reading SFR of IIS, user must set this bit.	R/W	0
Reserved	[30:27]	-	R	0x0
FRXOFSTATUS	[26]	RX FIFO Over Flow Interrupt Status. And this is used by interrupt clear bit. When this is high, you can do interrupt clear by writing '1'. 0 = Interrupt does not occur. 1 = Interrupt occurs	R/W	0
FRXOFINTEN	[25]	Enables RX FIFO Overflow Interrupt 0 = Disables RXFIFO Overflow INT 1 = Enables RXFIFO Overflow INT	R/W	0
FTXSUR STATUS	[24]	Secondary TX FIFO_S under-run interrupt status. This is used by interrupt clear bit. When this is high, you can clear interrupt clear by writing '1'. 0 = Interrupt does not occur. 1 = Interrupt occurs.	R/W	0
FTXSURINTEN	[23]	Secondary TX FIFO_S Under-run Interrupt Enable 0 = TXFIFO_S Under-run INT disable 1 = TXFIFO_S Under-run INT enable	R/W	0
FTXSEMPT	[22]	Secondary TX FIFO_S empty Status Indication 0 = TX FIFO_S is not empty(Ready to transmit Data) 1 = TX FIFO_S is empty (Not Ready to transmit Data)	R	0
FTXSFULL	[21]	Secondary TX FIFO_S full Status Indication 0 = TX FIFO_S is not full 1 = TX FIFO_S is full	R	0
TXSDMAPAUSE	[20]	Tx External DMA operation for secondary TX FIFIO_S pause command. Note that when this bit is activated, the External DMA request will be halted after current on-going External DMA transfer is completed. 0 = No pause External DMA operation for TX FIFO_S 1 = Pause External DMA operation for TX FIFO_S Note: IISDMAEN SFR performs Internal DMA stop control.	R/W	0
Reserved	[19]	Reserved. This value must be 0.	R/W	0
TXSDMACTIVE	[18]	Tx External DMA active for secondary TX FIFO_S (start External DMA request). Note that when this bit is set from high to low, the External DMA operation will be forced to stop immediately. 0 = Inactive 1 = Active	R/W	0

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IISCON	Bit	Description	R/W	Initial State
FTXURSTATUS	[17]	Primary TX FIFOx under-run interrupt status. This is used by interrupt clear bit. When this is high, you can clear interrupt by writing '1'. 0 = Interrupt didn't be occurred. 1 = Interrupt was occurred.	R/W	0
FTXURINTEN	[16]	Primary TX FIFOx Under-run Interrupt Enable 0 = TXFIFO Under-run INT disable 1 = TXFIFO Under-run INT enable	R/W	0
FTX2EMPT	[15]	Primary TX FIFO2 empty Status Indication 0 = TX FIFO2 is not empty(Ready to transmit Data) 1 = TX FIFO2 is empty (Not Ready to transmit Data)	R	0
FTX1EMPT	[14]	Primary TX FIFO1 empty Status Indication 0 = TX FIFO1 is not empty (Ready to transmit Data) 1 = TX FIFO1 is empty (Not Ready to transmit Data)	R	0
FTX2FULL	[13]	Primary TX FIFO2 full Status Indication 0 = TX FIFO2 is not full 1 = TX FIFO2 is full	R	0
FTX1FULL	[12]	Primary TX FIFO1 full Status Indication 0 = TX FIFO1 is not full 1 = TX FIFO1 is full	R	0
LRI	[11]	Left/Right channel clock indication. Note that LRI meaning is dependent on the value of LRP bit of I2SMOD register. 0 = Left (when LRP bit is low) or right (when LRP bit is high) 1 = Right (when LRP bit is low) or left (when LRP bit is high)	R	0
FTX0EMPT	[10]	Primary Tx FIFO0 empty status indication. 0 = FIFO is not empty (ready for transmit data to channel) 1 = FIFO is empty (not ready for transmit data to channel)	R	0
FRXEMPT	[9]	Rx FIFO empty status indication. 0 = FIFO is not empty 1 = FIFO is empty	R	0
FTX0FULL	[8]	Primary Tx FIFO0 full status indication. 0 = FIFO is not full 1 = FIFO is full	R	0
FRXFULL	[7]	Rx FIFO full status indication. 0 = FIFO is not full (ready for receive data from channel) 1 = FIFO is full (not ready for receive data from channel)	R	0
TXDMAPAUSE	[6]	Tx DMA operation pause command for primary TX FIFOx. Note that when this bit is activated, the DMA request will be halted after current on-going DMA transfer is completed. 0 = No pause DMA operation for TX FIFOx 1 = Pause DMA operation for TX FIFOx	R/W	0

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IISCON	Bit	Description	R/W	Initial State
RXDMAPAUSE	[5]	Rx DMA operation pause command. Note that when this bit is activated, the DMA request will be halted after current on-going DMA transfer is completed. 0 = No pause DMA operation 1 = Pause DMA operation	R/W	0
TXCHPAUSE	[4]	Tx channel operation pause command for primary TX FIFOx. Note that when this bit is activated, the channel operation will be halted after left-right channel data transfer is completed. 0 = No pause operation for TX FIFOx and TX_S FIFO 1 = Pause operation for TX FIFOx an TX_S FIFO	R/W	0
RXCHPAUSE	[3]	Rx channel operation pause command. Note that when this bit is activated, the channel operation will be halted after left-right channel data transfer is completed. 0 = No pause operation 1 = Pause operation	R/W	0
TXDMACTIVE	[2]	Tx DMA active for primary TX FIFOx (start DMA request). Note that when this bit is set from high to low, the DMA operation will be forced to stop immediately. 0 = Inactive 1 = Active	R/W	0
RXDMACTIVE	[1]	Rx DMA active (start DMA request). Note that when this bit is set from high to low, the DMA operation will be forced to stop immediately. 0 = Inactive 1 = Active	R/W	0
I2SACTIVE	[0]	IIS interface active (start operation). 0 = Inactive 1 = Active	R/W	0

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2.9.1.2 IIS Interface Mode Register (IISMOD, R/W, Address = 0xEEE3_0004)

IISMOD	Bit	Description	R/W	Initial State
OP_CLK	[31:30]	Operation clock for IIS logic. 00 = Codec clock out 01 = Codec clock in 10 = Bit clock out 11 = Audio bus clock	R/W	00
Reserved	[29]	-	R	0
OP_MUX_SEL	[28]	Mux selection for secondary TX FIFO_S 0 = TX FIFO_S gets data from APB SFR interface 1 = TX FIFO_S gets data form internal DMA interface Before trying to change this field from 1 to 0, s/w must poll IISTRNCNT register to confirm that all the transfer is done according to internal DMA setting. There is no restriction on switching from 0 to 1.	R/W	0
BLC_S	[27:26]	Bit Length Control Bit which decides transmission of 8/16/24 bits per audio channel for Secondary TX FIFO_S 00 = 16 Bits per channel 01 = 8 Bits Per Channel 10 = 24 Bits Per Channel 11 = Reserved	R/W	00
BLC_P	[25:24]	Bit Length Control Bit Which decides transmission of 8/16/24 bits per audio channel for Primary TX FIFOx 00 = 16 Bits per channel 01 = 8 Bits Per Channel 10 = 24 Bits Per Channel 11 = Reserved	R/W	00
Reserved	[23:22]	-	R	00
CDD2	[21:20]	Channel-2 Data Discard. Discard means zero padding. It only supports 8/16 bit mode. 00 = No Discard 01 = I2STXD[15:0] Discard 10 = I2STXD[31:16] Discard 11 = Reserved	R/W	00
CDD1	[19:18]	Channel-1 Data Discard. Discard means zero padding. It only supports 8/16 bit mode. 00 = No Discard 01 = I2STXD[15:0] Discard 10 = I2STXD[31:16] Discard 11 = Reserved	R/W	00
DCE	[17:16]	Enables Data Channel. [17]: Enables SD2 channel [16]: Enables SD1 channel	R/W	00
Reserved	[15]	-	R	0

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IISMOD	Bit	Description	R/W	Initial State
BLC	[14:13]	Bit Length Control Bit Which decides transmission of 8/16/24 bits per audio channel for final mixed sound Tx output or Rx input. 00 = 16 Bits per channel 01 = 8 Bits Per Channel 10 = 24 Bits Per Channel 11 = Reserved	R/W	00
CDCLKCON	[12]	Determine direction of codec clock source (I2S_CDCLK) 0 = Supply RCLK to I2S_CDCLK (external codec chip) 1 = Get clock (to CLKAUDIO) from I2S_CDCLK (external codec chip) (Refer to *Figure 2-3*)	R/W	0
MSS	[11]	Master or slave mode select 0 = Master mode 1 = Slave mode	R/W	0
RCLKSRC	[10]	Select RCLK clock source 0 = Using Audio bus clock 1 = Using I2SCLK (Refer to *Figure 2-3*)	R/W	0
TXR	[9:8]	Transmit or receive mode select. 00 = Transmit only mode 01 = Receive only mode 10 = Transmit and receive simultaneous mode 11 = Reserved	R/W	00
LRP	[7]	Left/Right channel clock polarity select. 0 = Low for left channel and high for right channel 1 = High for left channel and low for right channel	R/W	0
SDF	[6:5]	Serial data format. 00 = IIS format 01 = MSB-justified (left-justified) format 10 = LSB-justified (right-justified) format 11 = Reserved	R/W	00
RFS	[4:3]	IIS root clock (codec clock) frequency select. 00 = 256 fs, where fs is sampling frequency 01 = 512 fs 10 = 384 fs 11 = 768 fs Note: Even in the slave mode, this bit should be set for correct operation.	R/W	00
BFS	[2:1]	Bit clock frequency select. 00 = 32 fs, where fs is sampling frequency 01 = 48 fs 10 = 16 fs 11 = 24 fs Note: Even in the slave mode, this bit should be set for correct operation.	R/W	00

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IISMOD	Bit	Description	R/W	Initial State
Reserved	[0]	-	R	0

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2.9.1.3 IIS Interface FIFO Control Register (IISFIC, R/W, Address = 0xEEE3_0008)

IISFIC	Bit	Description	R/W	Initial State
Reserved	[31]	-	W	0
FTX2CNT	[30:24]	Primary TX FIFO2 data count. FIFO has 64 depth, so value ranges from 0 to 64. N: Data count N of FIFO	R	0x00
Reserved	[23]	-	R	0
FTX1CNT	[22:16]	Primary TX FIFO1 data count. FIFO has 64 depth, so value ranges from 0 to 64. N: Data count N of FIFO	R	0x00
TFLUSH	[15]	Primary TX FIFO flush command. 0 = No flush 1 = Flush	R/W	0
FTX0CNT	[14:8]	Primary TX FIFO0 data count. FIFO has 64 dept, so value ranges from 0 to 64. N: Data count N of FIFO	R	0x00
RFLUSH	[7]	RX FIFO flush command. 0 = No flush 1 = Flush	R/W	0
FRXCNT	[6:0]	RX FIFO data count. FIFO has 64 dept, so value ranges from 0 to 64. N: Data count N of FIFO	R	0x00

2.9.1.4 IIS Interface Clock Divider Control Register (IISPSR, R/W, Address = 0xEEE3_000C)

IISPSR	Bit	Description	R/W	Initial State
Reserved	[31:16]	-	R	0x00
PSRAEN	[15]	Pre-scaler (Clock divider) a active. 0 = Inactive 1 = Active	R/W	0
Reserved	[14]	-	R	0
PSVALA	[13:8]	Pre-scaler (Clock divider) a division value. N: Division factor is N+1	R/W	0x00
Reserved	[7:0]	-	R	0x00

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2.9.1.5 IIS Interface Transmit Data Register (IISTXD, W, Address = 0xEEE3_0010)

IISTXD	Bit	Description	R/W	Initial State
IISTXD	[31:0]	Primary TX FIFO write data. Note that the left/right channel data is allocated as the following bit fields. R[31:16], L[15:0] when 16-bit BLC R[23:16], L[7:0] when 8-bit BLC Refer Figure 10.2-7 when 24-bit BLC	W	0x00

2.9.1.6 IIS Interface Receive Data Register (IISRXD, R, Address = 0xEEE3_0014)

IISRXD	Bit	Description	R/W	Initial State
IISRXD	[31:0]	RX FIFO read data. Note that the left/right channel data is allocated as the following bit fields. R[31:16], L[15:0] when 16-bit BLC R[23:16], L[7:0] when 8-bit BLC Refer Figure 10.2-9 when 24-bit BLC	R	0x00

2.9.1.7 IIS Interface TXFIFO_S Control Register (IISFICS, R/W, Address = 0xEEE3_0018)

IISFICS	Bit	Description	R/W	Initial State
Reserved	[31:16]	-	R	0x00
TFLUSHS	[15]	Secondary TX FIFO_S flush command. 0 = No flush 1 = Flush	R/W	0
FTXSCNT	[14:8]	Secondary TX FIFO_S data count. FIFO has 64 depth, so value ranges from 0 to 64. N: Data count N of FIFO	R	0x00
Reserved	[7:0]	-	R	0x00

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2.9.1.8 IIS Interface Transmit Data Register for TXFIFO_S (IISTXDS, W, Address = 0xEEE3_001C)

IISTXDS	Bit	Description	R/W	Initial State
IISTXDS	[31:0]	Secondary TX FIFO_S write data. Note that the left/right channel data is allocated as the following bit fields. R[31:16], L[15:0] when 16-bit BLC R[23:16], L[7:0] when 8-bit BLC Refer Figure 10.2-7 when 24-bit BLC	W	0x00

2.9.1.9 IIS AHB DMA Control Register (IISAHB, R/W, Address = 0xEEE3_0020)

IISAHB	Bit	Description	R/W	Initial State
Reserved	[31:28]	-	R	0x00
IISLVL3EN	[27]	Enables buffer level 3 interrupt. 0 = Disables IISLVL3INT. 1 = Enables IISLVL3INT.	R/W	0
IISLVL2EN	[26]	Enables buffer level 2 interrupt. 0 = Disables IISLVL2INT. 1 = Enables IISLVL2INT.	R/W	0
IISLVL1EN	[25]	Enable buffer level 1 interrupt. 0 = Disables IISLVL1INT. 1 = Enables IISLVL1INT.	R/W	0
IISLVL0EN	[24]	Enable buffer level 0 interrupt. 0 = Disables IISLVL0INT. 1 = Enables IISLVL0INT.	R/W	0
IISLVL3INT	[23]	Buffer level 3 interrupt status flag. During operation of DMA, when generated address in DMA matches with IISLVL3ADDR, this flag will be set. To clear this flag, use IISLVL3CLR field.	R	0
IISLVL2INT	[22]	Buffer level 2 interrupt status flag. During operation of DMA, when generated address in DMA matches with IISLVL2ADDR, this flag will be set. To clear this flag, use IISLVL2CLR field.	R	0
IISLVL1INT	[21]	Buffer level 1 interrupt status flag. During operation of DMA, when generated address in DMA matches with IISLVL1ADDR, this flag will be set. To clear this flag, use IISLVL1CLR field.	R	0
IISLVL0INT	[20]	Buffer level 0 interrupt status flag. During operation of DMA, when generated address in DMA matches with IISLVL0ADDR, this flag will be set. To clear this flag, use IISLVL0CLR field.	R	0
IISLVL3CLR	[19]	Clear IISLVL3INT flag When IISLVL3INT is set, setting IISLVL3CLR to 1 will clear IISLVL3INT to 0. Writing zero has no effect.	R/W	0

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IISAHB	Bit	Description	R/W	Initial State
IISLVL2CLR	[18]	Clear IISLVL2INT flag When IISLVL2INT is set, setting IISLVL2CLR to 1 will clear IISLVL2INT to 0. Writing zero has no effect.	R/W	0
IISLVL1CLR	[17]	Clear IISLVL1INT flag When IISLVL1INT is set, setting IISLVL1CLR to 1 will clear IISLVL1INT to 0. Writing zero has no effect.	R/W	0
IISLVL0CLR	[16]	Clear IISLVL0INT flag When IISLVL0INT is set, setting IISLVL0CLR to 1 will clear IISLVL0INT to 0. Writing zero is has effect.	R/W	0
Reserved	[15:8]	-	R	0x00
IISDMA_STR ADDRRST	[7]	DMA start address reset Before starting address toggle, write 1 to this bit. After reset, this bit is auto-cleared.	W	0x0
IISDMA_STR ADDRTOG	[6]	DMA start address toggle 0 = Disables start address toggling (IISSTR0 → IISSTR0 → …) 1 = Enables start address toggling (IISSTR0 → IISSTR1 → IISSTR0 → IISSTR1 → …)	R/W	0
IISDMARLD-	[5]	Auto-reload IIS internal DMA Configuration when DMA operation is done and re-start IIS internal DMA automatically. 0 = Disables auto-reload function 1 = Enables auto-reload function Before switching to 0 from 1, s/w must check if DMA_EN is set.	R/W	0
IISINTMASK	[3]	Disables interrupt request signal 0 = Enables interrupt request when DMA auto-reload is on. 1 = Disables interrupt request when DMA auto-reload is on. After DMA transfers all of data related to DMA configuration, interrupt signal will occur. If IISINTMASK bit is set, IISDMAINT & interrupt signal will NOT be set. IISINTMASK does NOT effect IISLVLxINT & under-run interrupt.	R/W	0
IISDMAINT	[2]	DMA interrupt status flag. After DMA operation is end, this flag will be set. To clear this flag, use IISDMACLR field. When ARM is used for decoder, do not use this interrupt as controlling timing of filling buffer. In that case, use level 0~3 interrupts. This interrupt is just used for ending condition.	R	0
IISDMACLR	[1]	Clear DMA interrupt status flag When IISINT is set, setting IISDMACLR to 1 will clear IISDMAINT to 0. Writing to zero is no meaning.	R/W	0

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IISAHB	Bit	Description	R/W	Initial State
IISDMAEN	[0]	Enable IIS internal DMA Users can use internal DMA in IIS after this bit field is ON. Internal DMA can issue 32-bit single read transaction for AHB and TXFIFO0 will hold data returned by DMA. Warning> If IISDMARLD is set, IISDMAEN bit will be automatically cleared when reload operation is in progress. After auto-reload operation is done, IISDMAEN bit will be automatically set. When auto-reload operation is in progress, s/w intervention on this field will cause mal-function of internal DMA operations. To manipulate IISAHB register, s/w must check that IISDMAEN is in stable state.	R/W	0

2.9.1.10 IIS AHB DMA Start Address0 Register (IISSTR0, R/W, Address = 0xEEE3_0024)

IISSTR0	Bit	Description	R/W	Initial State
IISSTR	[31:0]	Start address0 of IIS internal DMA operation. When DMAEN is ON, internal DMA in IIS will start DMA operation based on IISSTR0 address. Internal DMA can handle word-aligned address only but to get best performance, IISSTR0 should be 64 word-aligned address.	R/W	0x00

2.9.1.11 IIS AHB DMA Start Address1 Register (IISSTR1, R/W, Address = 0xEEE3_0040)

IISSTR1	Bit	Description	R/W	Initial State
IISSTR1	[31:0]	Start address1 of IIS internal DMA operation. When DMAEN is ON, internal DMA in IIS will start DMA operation based on IISSTR1 address. Internal DMA can handle word-aligned address only, but to achieve best performance, IISSTR1 should be 64 word-aligned address.	R/W	0x00

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2.9.1.12 IIS AHB DMA Size Register (IISSIZE, R/W, Address = 0xEEE3_0028)

IISSIZE	Bit	Description	R/W	Initial State
TRNS_SIZE	[31:16]	Transfer block size for IIS internal DMA When IIS internal DMA is enabled, IIS internal DMA will transfer TRNS_SIZE word(s) data from memory before DMA done interrupt occurs. Valid ranges for TRNS_SIZE will be from 0x0001 to 0xA000. 0x0001 – 0xA000 : IMEM and DMEM at AUDIO Sub-System (160Kbytes)	R/W	0x7FFF
Reserved	[15:0]	-	R	0x0000

2.9.1.13 IIS AHB DMA Transfer Count Register (IISTRNCNT, R, Address = 0xEEE3_002C)

IISTRNCNT	Bit	Description	R/W	Initial State
Reserved	[31:24]	-	R	
IISTRNCNT	[23:0]	Number of transferred data using IIS internal DMA. (word unit) User program can terminate IIS internal DMA operation by turning DMA_EN off. After DMA_EN is 0, user program reads IISTRNCNT value to know where IIS internal DMA stops.	R	

2.9.1.14 IIS AHB DMA Level 0 Interrupt Address Register (IISLVL0ADDR, R/W, Address = 0xEEE3_0030)

IISLVL0ADDR	Bit	Description	R/W	Initial State
IISLVL0ADDR	[31:10]	AHB DMA level 0 interrupt address While IISLVL0EN in IISAHB register is set, AHB DMA is comparing this register to generated address in DMA. When two values match, IISLVL0INT in IISAHB will be set. Valid address range for IISLVL0ADDR is from 0xC000_0000 to 0xC01F_FFFF.	R	0x00
Reserved	[9:1]	-	R	0x00
IISLVL0STOP	[0]	Enables Precise stop 0 = Do not stop DMA operation 1 = Stop DMA operation when DMA working address is matched with IISLVL0ADDR. IISDMAEN in IISAHB will be turned off automatically.	R/W	0

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2.9.1.15 IIS AHB DMA Level 1 Interrupt Address Register (IISLVL1ADDR, R/W, Address = 0xEEE3_0034)

IISLVL1ADDR	Bit	Description	R/W	Initial State
IISLVL1ADDR	[31:10]	AHB DMA level 1 interrupt address While IISLVL1EN in IISAHB register is set, AHB DMA is comparing this register to generated address in DMA. When two values match, IISLVL1INT in IISAHB will be set. Valid address range for IISLVL1ADDR is from 0xC000_0000 to 0xC01F_FFFF.	R	0x00
Reserved	[9:1]	-	R	0x00
IISLVL1STOP	[0]	Enables Precise stop 0 = Do not stop DMA operation 1 = Stop DMA operation when DMA working address is matched with IISLVL1ADDR. IISDMAEN in IISAHB will be turned off automatically.	R/W	0

2.9.1.16 IIS AHB DMA Level 2 Interrupt Address Register (IISLVL2ADDR, R/W, Address = 0xEEE3_0038)

IISLVL2ADDR	Bit	Description	R/W	Initial State
IISLVL2ADDR	[31:10]	AHB DMA level 2 interrupt address While IISLVL2EN in IISAHAB register is set, AHB DMA is comparing this register to generated address in DMA. When two values match, IISLVL2INT in IISAHB will be set. Valid address range for IISLVL2ADDR is from 0xC000_0000 to 0xC01F_FFFF.	R	0x00
Reserved	[9:1]	-	R	0x00
IISLVL2STOP	[0]	Enables Precise stop 0 = Do not stop DMA operation 1 = Stop DMA operation when DMA working address is matched with IISLVL2ADDR. IISDMAEN in IISAHB will be turned off automatically.	R/W	0

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2.9.1.17 IIS AHB DMA Level 3 Interrupt Address Register (IISLVL3ADDR, R/W, Address = 0xEEE3_003C)

IISLVL3ADDR	Bit	Description	R/W	Initial State
IISLVL3ADDR	[31:10]	AHB DMA level 3 interrupt address While IISLVL3EN in IISAHB register is set, AHB DMA is comparing this register to generated address in DMA. When two values match, IISLVL3INT in IISAHB will be set. Valid address range for IISLVL3ADDR is from 0xC000_0000 to 0xC01F_FFFF.	R	0x00
Reserved	[9:1]	-	R	0x00
IISLVL3STOP	[0]	Enables Precise stop 0 = Do not stop DMA operation 1 = Stop DMA operation when DMA working address is matched with IISLVL3ADDR. IISDMAEN in IISAHB will be turned off automatically.	R/W	0

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3 IIS-BUS INTERFACE

3.1 OVERVIEW OF IIS-BUS INTERFACE

Inter-IC Sound (IIS) is one of the popular digital audio interface. The IIS bus handles audio data and other signals, namely, sub-coding and control, are transferred separately. It is possible to transmit data between two IIS bus. To minimize the number of pins required and to keep wiring simple, basically, a 3-line serial bus is used. This consists of a line for two time-multiplexed data channels, a word select line and a clock line.

IIS interface transmits or receives sound data from external stereo audio codec. To transmit and receive data, two 32x64 FIFOs (First-In-First-Out) data structures are included and DMA transfer mode to transmit and receive samples can be supported. IIS-specific clock can be supplied from internal system clock controller through IIS clock divider or direct clock source.

3.2 KEY FEATURES OF IIS-BUS INTERFACE

- 2-ports stereo(2ch) IIS-bus for audio interface with DMA-based operation
- Serial, 8/16/24-bit per channel data transfers
- Supports master/slave mode
- Supports IIS, MSB-justified and LSB-justified data format

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3.3 BLOCK DIAGRAM OF IIS-BUS INTERFACE

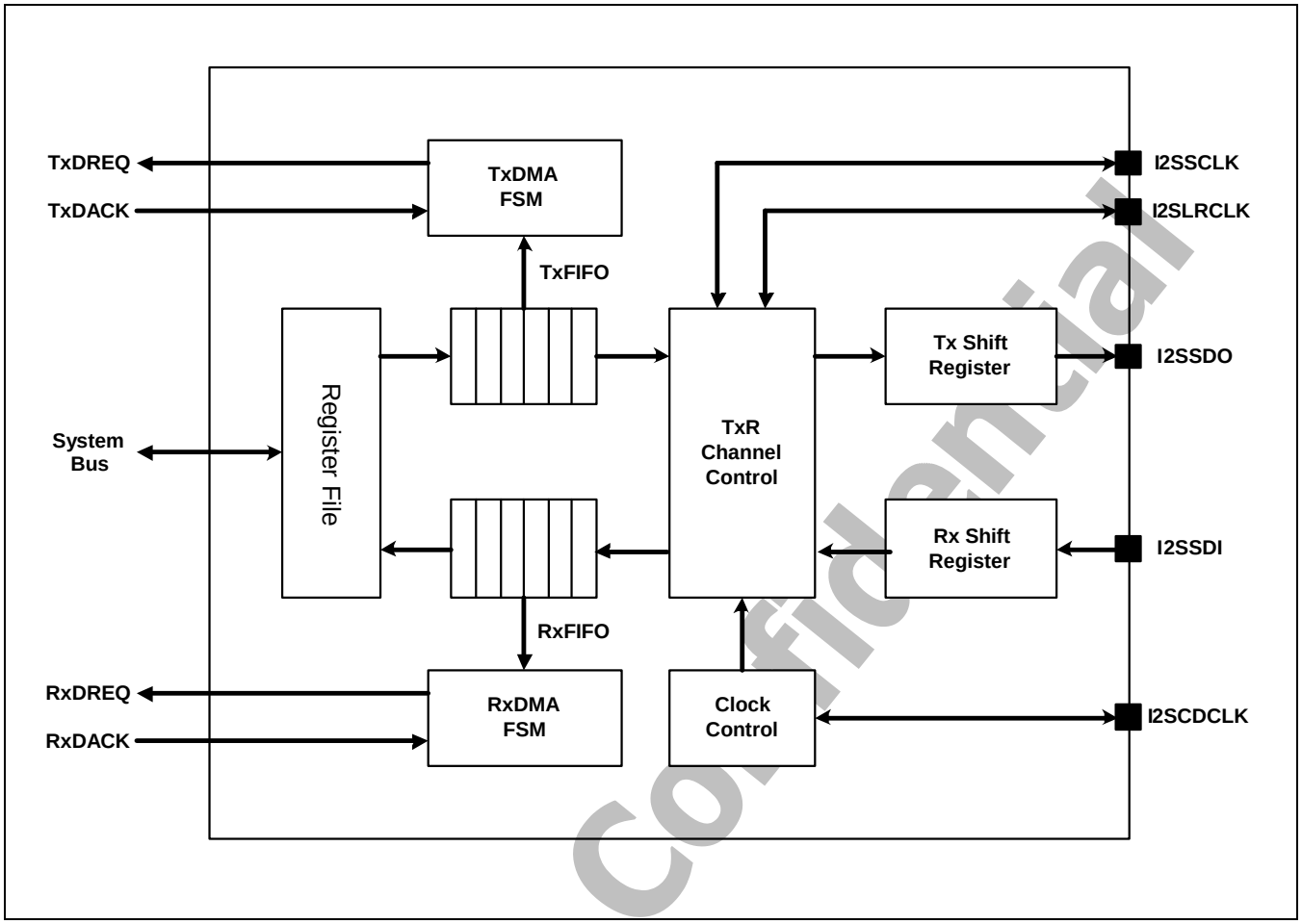

Figure 3-1 IIS-Bus Block Diagram

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3.4 FUNCTIONAL DESCRIPTIONS

IIS interface consists of register bank, FIFOs, shift registers, clock control, DMA finite state machine, and channel control block as shown in *Figure 3-1*. Note that each FIFO has 32-bit width and 64 depth structure, which contains left/right channel data. Thus, FIFO access and data transfer are handled with left/right pair unit. *Figure 3-1* shows the functional block diagram of IIS interface.

3.4.1 MASTER/SLAVE MODE

To select master or slave mode, set IMS bit of IISMOD register. In master mode, I2SSCLK and I2SLRCLK are generated internally and supplied to external device. Therefore, a root clock is required to generate I2SSCLK and I2SLRCLK. The IIS pre-scaler (clock divider) is employed to generate a root clock with divided frequency from internal system clock. In external master mode, the root clock can be directly fed from IIS external. The I2SSCLK and I2SLRCLK are supplied from the pin (GPIOs) in slave mode. That is, whatever source clock is, Only Master can generate I2SLRCLK and I2SSCLK.

Master/Slave mode is different compared to TX/RX. Master/Slave mode presents the direction of I2SLRCLK and I2SSCLK. The direction of I2SCDCLK (This is only auxiliary.) is not important. If IIS bus interface transmits clock signals to IIS codec, IIS bus is master mode. But if IIS bus interface receives clock signal from IIS codec, IIS bus is slave mode. TX/RX mode indicates the direction of data flow. If IIS bus interface transmits data to IIS codec, this indicates TX mode. Conversely, IIS bus interface receives data from IIS codec this indicates RX mode.

Figure 3-2 shows the route of the root clock with internal master or external master mode setting in IIS clock control block and system controller. Note that RCLK indicates root clock and this clock can be supplied to external IIS codec chip in internal master mode.

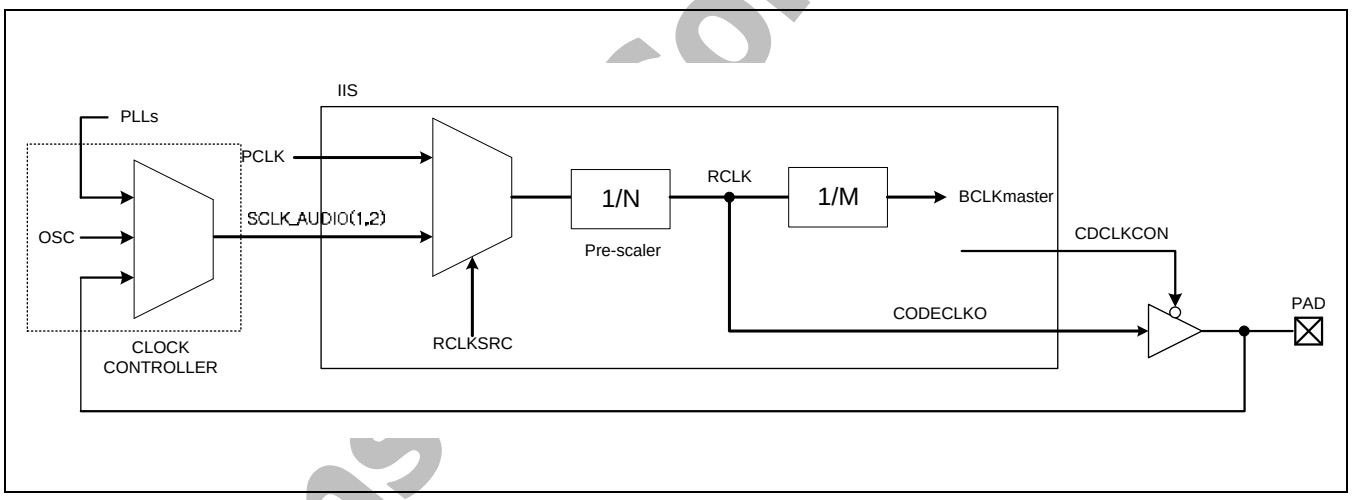

Figure 3-2 IIS Clock Control Block Diagram

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3.4.2 DMA TRANSFER

In the DMA transfer mode, use external DMA controller to access the transmitter or receiver FIFO. The transmitter or receiver FIFO state activates the DMA service request internally. The FTXEMPT, FRXEMPT, FTXFULL, and FRXFULL bits of I2SCON register represent the transmitter or receiver FIFO data state. Especially, FTXEMPT and FRXFULL bit are the ready flag for DMA service request; the transmit DMA service request is activated when TXFIFO is not empty and the receiver DMA service request is activated when RXFIFO is not full.

The DMA transfer uses only handshaking method for single data. Note that during DMA acknowledge activation; the data read or write operation should be performed.

* Reference: DMA request point

- TX mode: (FIFO is not full) & (TXDMACTIVE is active)
- RX mode: (FIFO is not empty) & (RXDMACTIVE is active)

3.4.3 AUDIO SERIAL DATA FORMAT

3.4.3.1 IIS-bus Format

The IIS bus has four lines including serial data input I2SSDI, serial data output I2SSDO, left/right channel select clock I2SLRCLK, and serial bit clock I2SSCLK; master generates I2SLRCLK and I2SSCLK.

Serial data is transmitted in 2's complement with the MSB first with a fixed position, whereas the position of the LSB depends on the word length. The transmitter sends the MSB of the next word at one clock period after the I2SLRCLK is changed. Serial data sent by the transmitter can be synchronized either with the trailing or with the leading edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge.

The LR channel select line indicates the channel being transmitted. I2SLRCLK may be changed either on a trailing or leading edge of the serial clock, but it does not need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The I2SLRCLK line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word.

3.4.3.2 MSB (Left) Justified

MSB-Justified (Left-Justified) format is similar to IIS bus format, except that in MSB-justified format, the transmitter always sends the MSB of the next word at the same time whenever the I2SLRCLK is changed.

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3.4.3.3 LSB (Right) Justified

LSB-Justified (Right-Justified) format is opposite to the MSB-justified format. In other word, the transferring serial data is aligned with ending point of I2SLRCLK transition.

Figure 3-3 shows the audio serial format of IIS, MSB-justified, and LSB-justified. Note that in this figure, the word length is 16-bit and I2SLRCLK makes transition every 24 cycle of I2SSCLK (BFS is 48 fs, where fs is sampling frequency; I2SLRCLK frequency).

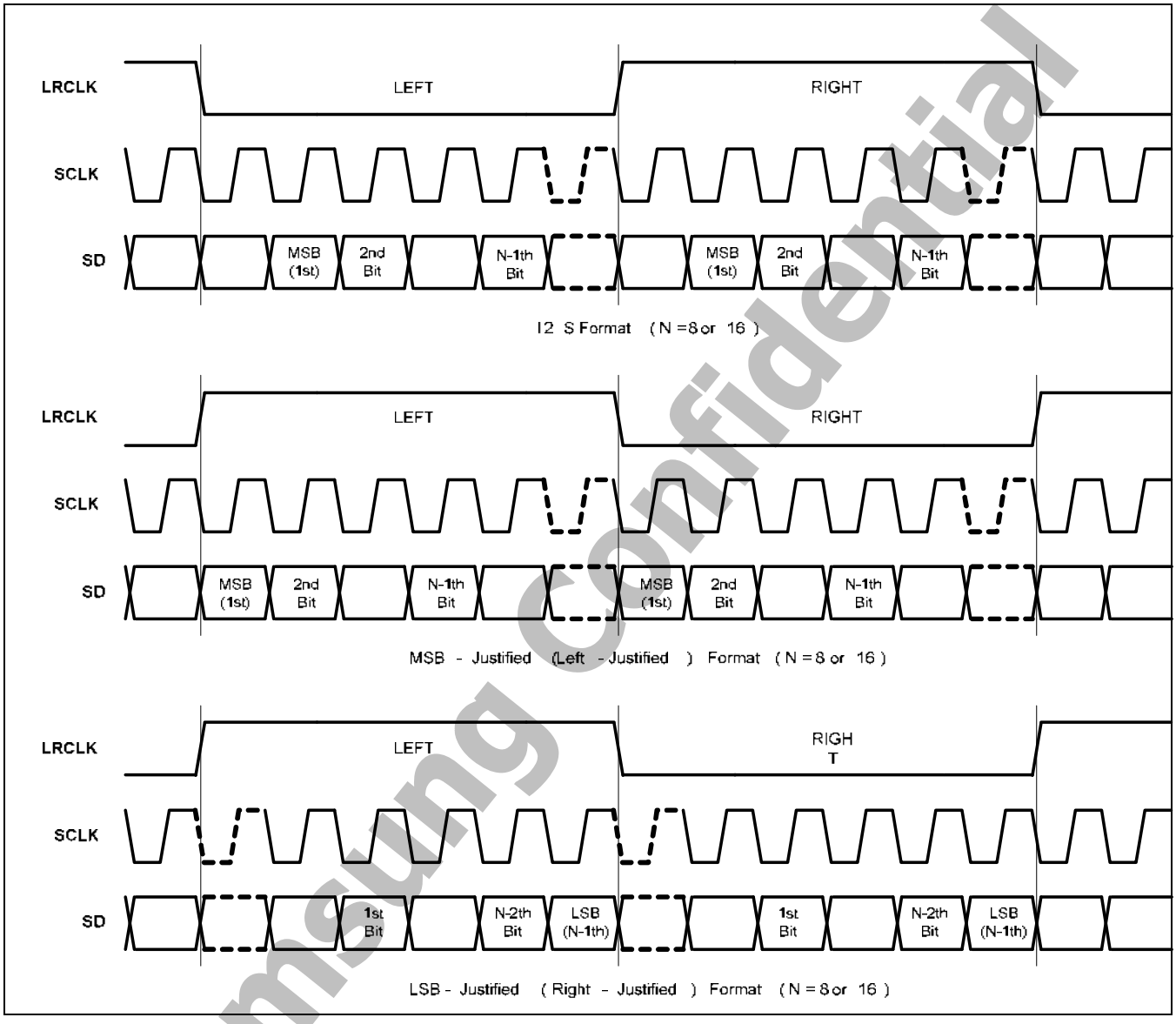

Figure 3-3 IIS Audio Serial Data Formats

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3.4.3.4 Sampling Frequency and Master Clock

When IIS interface Controller operates as master, IIS interface Controller generates IISLRCLK and IISSCLK that are divided as Root Clock by RFS and BFS value. To decide Sampling Frequency – IISLRCLK -, BLC, BFS, and RFS are selected first. Optionally, IIS interface Controller clocks out Root clock as IISCDCLK for codec master clock (if source of root clock is not IISEXTCDCLK).

In slave mode, you must set the value of BLC, BFS and RFS similar to master (ex: Codec). Because IIS interface controller needs these value for correct operation.

3.4.4 PCM WORD LENGTH AND BFS DIVIDER

PCM Word Length (BLC) setting should be preceded before setting the BFS value. *Table 3-1* shows BFS available value as BLC.

Table 3-1 Allowed BFS Value as BLC

PCM Bit length(BLC)	8bit	16bit	24bit
Available BFS value	16fs, 24fs, 32fs, 48fs	32fs, 48fs	48fs

3.4.5 BFS DIVIDER AND RFS DIVIDER

RFS value is selected as BFS selected. *Table 3-2* shows RFS available value as BFS.

Table 3-2 Allowed RFS Value as BFS

BFS Divider	16fs, 32fs	24fs, 48fs
Available RFS value	256fs, 384fs, 512fs, 768fs.	384fs, 768fs.

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3.4.6 RFS DIVIDER AND ROOT CLOCK

Root Clock is made for sampling frequency proper RFS value as shown in *Table 3-3*. RCLK is clock divided by IIS pre-scaler(IISPSR) that is selected by IMS

Table 3-3 Root Clock Table (MHz)

IISLRCK / RFS	8.000 kHz	11.025 kHz	16.000 kHz	22.050 kHz	32.000 kHz	44.100 kHz	48.000 kHz	64.000 kHz	88.200 kHz	96.000 kHz
256fs	2.0480	2.8224	4.0960	5.6448	8.1920	11.2896	12.2880	16.3840	22.5792	24.5760
384fs	3.0720	4.2336	6.1440	8.4672	12.2880	16.9344	18.4320	24.5760	33.8688	36.8640
512fs	4.0960	5.6448	8.1920	11.2896	16.3840	22.5792	24.5760	32.7680	45.1584	49.1520
768fs	6.1440	8.4672	12.2880	16.9344	24.5760	33.8688	36.8640	49.1520	67.7376	73.7280

Root Clock Frequency = fs * (256, 384, 512 or 768)

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3.5 PROGRAMMING GUIDE

The IIS bus interface can be accessed either by the processor using programmed I/O instructions or by the DMA controller.

3.5.1 INITIALIZATION

1. Before you use IIS bus interface, you must configure GPIOs to IIS mode, that is, I2SSDI is input and I2SSDO is output. I2SLRCLK, I2SSCLK and I2SCDCLK is inout-type.
2. Select clock source. S5PV210 has three clock sources, namely, PCLK, EPLL and external codec. For more information, refer *Figure 3-2.*

3.5.2 PLAY MODE (TX MODE) WITH DMA

1. TXFIFO is flushed before operation. If you do not distinguish Master/Slave mode from TX/RX mode, you must study Master/Slave mode and TX/RX mode. Refer Master/Slave chapter.
2. Configure I2SMOD register and I2SPSR (IIS pre-scaler register).
3. To operate system in stability, the internal TXFIFO should be almost full before transmission. For TXFIFO to be almost full start DMA operation.
4. IIS bus does not support the interrupt. Therefore, you can only check state by polling through accessing SFR.
5. After TXFIFO is full, then I2SACTIVE must be asserted.

3.5.3 RECORDING MODE (RX MODE) WITH DMA

1. RXFIFO is flushed before operation. Also, if you don't distinguish between Master/Slave mode and TX/RX mode, you must study Master/Slave mode and TX/RX mode. Refer Master/Slave chapter.
2. Configure I2SMOD register and I2SPSR (IIS pre-scaler register).
3. To operate system in stability, the internal RXFIFO should have at least one data before DMA operation. You must assert I2SACTIVE before DMA operation.
4. Check RXFIFO state by polling through accessing SFR.
5. If RXFIFO is not empty, start RXDMACTIVE.

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3.5.4 EXAMPLE CODE

3.5.4.1 Tx Channel

The I2S TX channel provides a single stereo compliant output. The transmit channel can operate in master or Slave mode. Data is transferred between the processor and the I2S controller via an APB access or a DMA access.

The processor must write words in multiples of two (i.e. for left and right audio sample).The words are serially shifted out timed with respect to the audio serial bitclk, SCLK and word select clock, LRCLK.

TX Channel has 64X32-bit wide FIFO where the processor or DMA can write upto 16 left/right data samples After enabling the channel for transmission.

An Example sequence is as follows:

Ensure the PCLK and CDCLK are coming correctly to the I2S controller and FLUSH the TX FIFO using the TFLUSH bit in the Please ensure that I2S Controller is configured in one of the following modes.

- TX only mode
- TX/RX simultaneous mode

The Data is aligned in the TX FIFO for 8-bits/channel or 16-bits/channel BLC as shown in *Figure 3-4*.

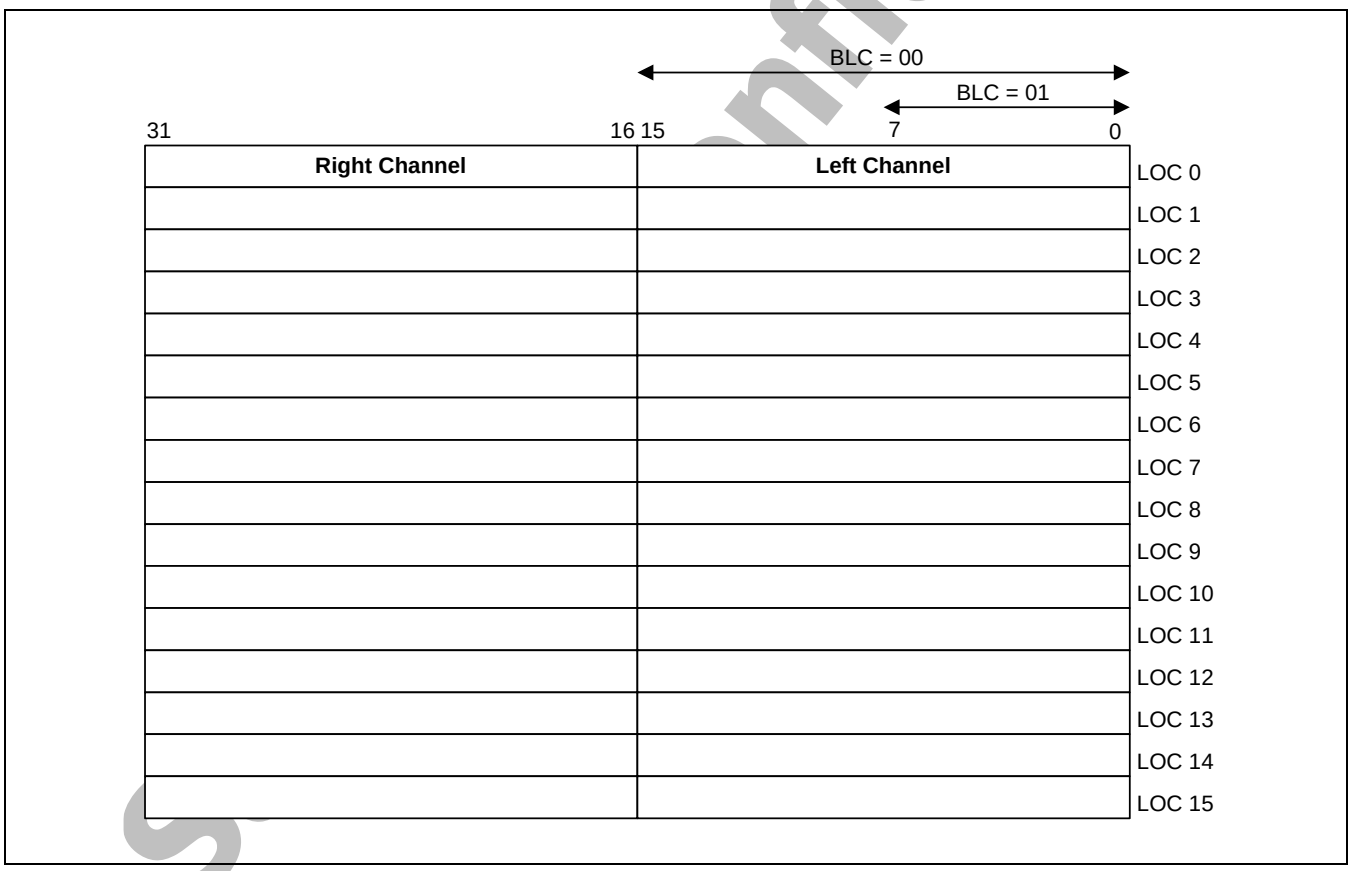

Figure 3-4 TX FIFO Structure for BLC = 00 or BLC = 01

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The Data is aligned in the TX FIFO for 24-bit/channel BLC as shown in *Figure 3-5*.

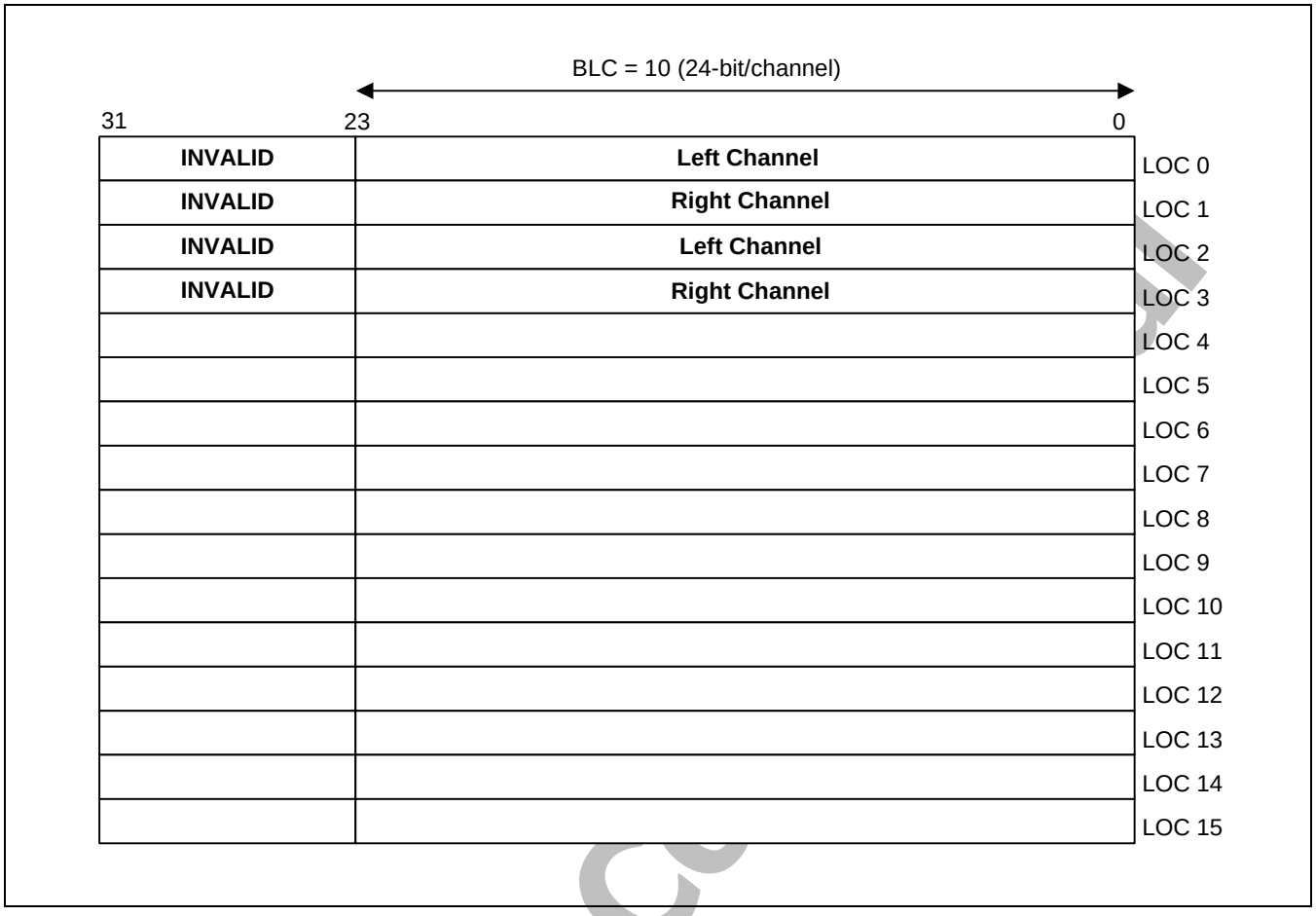

Figure 3-5 TX FIF0 Structure for BLC = 10 (24-bit/channel)

Once the data is written to the TX FIFO the TX channel can be made active by enabling the I2SACTIVE bit in the I2SCON Register (I2S Control Register).

The data is then serially shifted out with respect to the serial bit clock SCLK and word select clock LRCLK.

The TXCHPAUSE in the I2SCON Register (I2S Control Register) can stop the serial data transmission on the I2SSDO.The transmission is stopped once the current Left/Right channel is transmitted.

If the control registers in the I2SCON Register (I2S Control Register) and I2SMOD Register (I2S Mode Register) are to be reprogrammed then it is advisable to disable the TX channel.

If the TX channel is enabled while the FIFO is empty, no samples are read from the FIFO.

The Status of TX FIFO can be checked by checking the bits in the I2SFIC Register (I2S FIFO Control Register).

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3.5.4.2 RX Channel

The I2S RX channel provides a single stereo compliant output. The receive channel can operate in master or slave mode. Data is received from the input line and transferred into the RX FIFO. The processor can then read this data via an APB read or a DMA access can access this data.

RX Channel has a 64X32-bit wide RX FIFO where the processor or DMA can read UPTO 16 left/right data samples after enabling the channel for reception.

An Example sequence is as follows:

Ensure the PCLK and CDCLK are coming correctly to the I2S controller and FLUSH the RX FIFO using the RFLUSH bit in the I2SFIC Register (I2S FIFO Control Register) and the I2S controller is configured in any of the modes

- Receive only.
- Receive/Transmit simultaneous mode

This can be done by Programming the TXR bit in the I2SMOD Register (I2S Mode Register)

1. Then Program the following parameters according to the need
   - MMS, RCLKSRC
   - SDF
   - BFS
   - BLC
   - LRP
     For Programming, the above mentioned fields please refer I2SMOD Register (I2S Mode Register)
2. Once ensured that the input clocks for I2S controller are up and running and step 1 and 2 have been completed user must put the I2SACTIVE high to enable any reception of data, the I2S Controller receives data on the LRCLK change.

Read the data from the RX FIFO using the I2SRXD Register (I2S RX FIFO Register) after looking at the RX FIFO count in the I2SFIC Register (I2S FIFO Control Register). The count would only increment once the complete left channel and right have been received.

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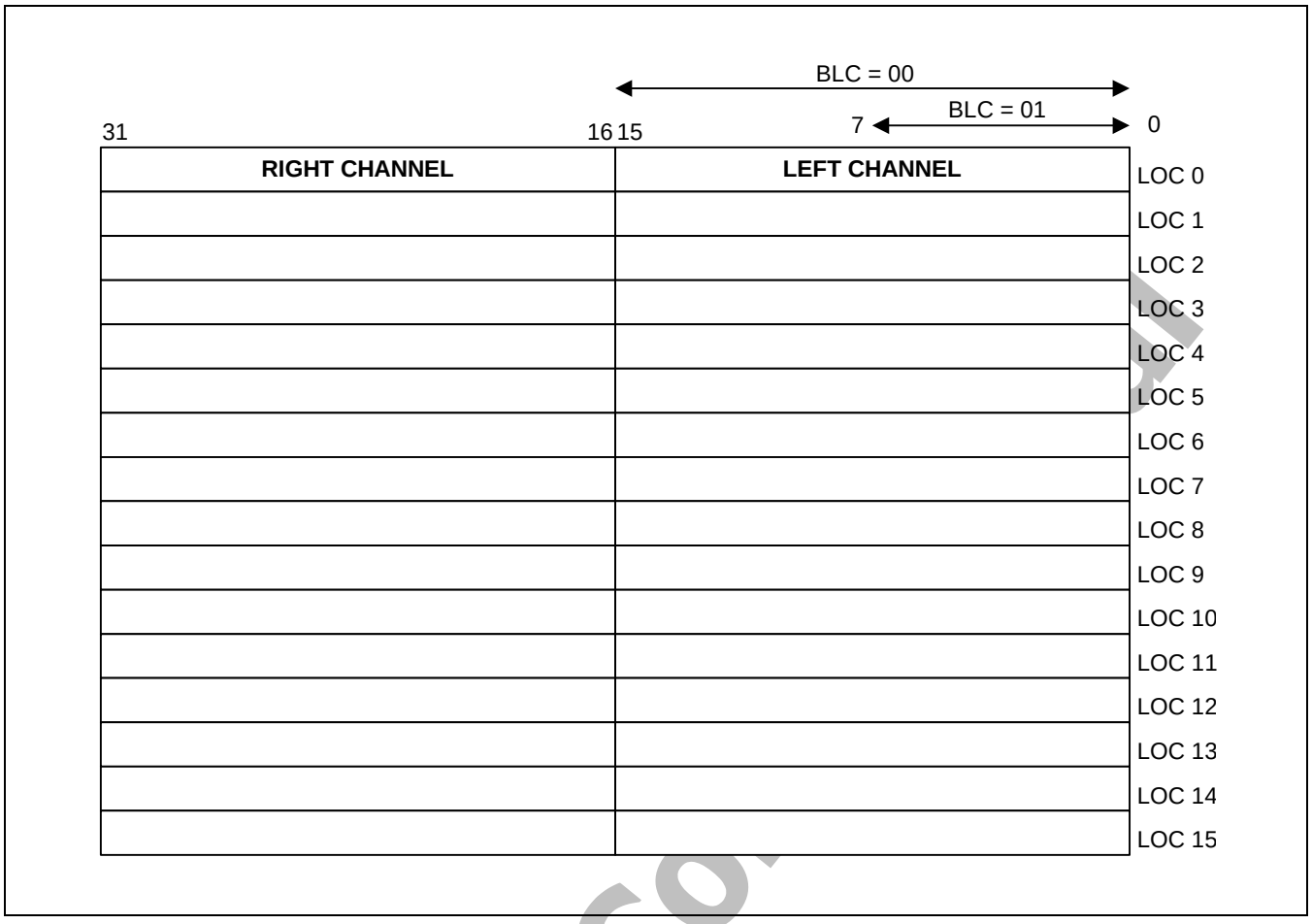

Figure 3-6 RX FIFO Structure for BLC = 00 or BLC = 01

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The Data is aligned in the RX FIFO for 24-bit/channel BLC as shown *Figure 3-7*.

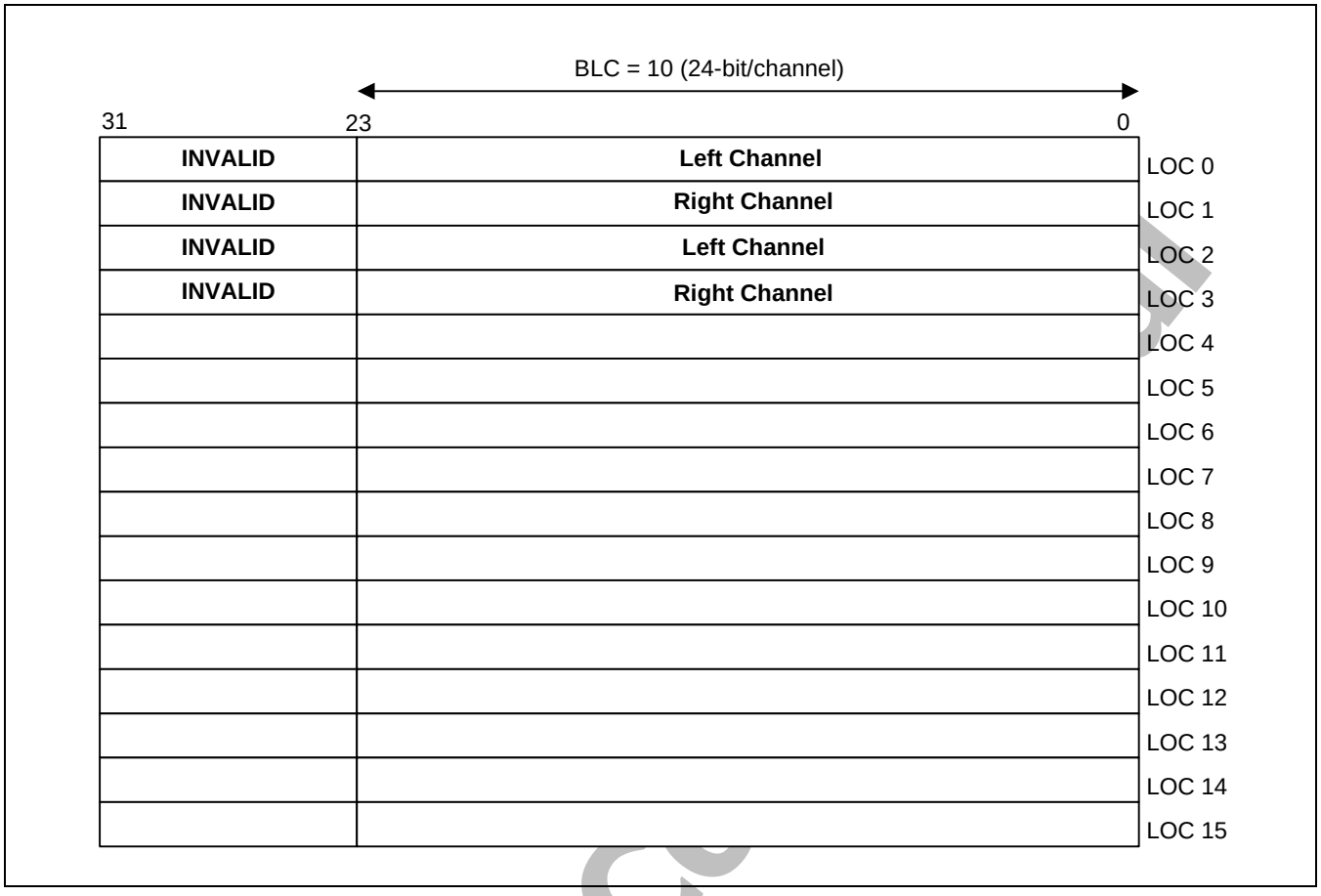

Figure 3-7 RX FIF0 Structure for BLC = 10 (24-bits/channel)

The RXCHPAUSE in the I2SCON register can stop the serial data reception on the I2SSDI.The reception is stopped once the current Left/Right channel is received.

If the control registers in the I2SCON Register (I2S Control Register) and I2SMOD Register (I2S Mode Register) are to be reprogrammed then it is advisable to disable the RX channel.

Check the status of RX FIFO by checking the bits in the I2SFIC Register (I2S FIFO Control Register).

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3.6 I/O DESCRIPTION

Each I2S (v3.2) external pads are shared with I2S and PCM. In order to use these pads for I2S, GPIO must be set before the I2S started. For mode information, refer to the GPIO chapter of this manual for proper GPIO setting

PAD Name	I/O	Description	Pad	Type
Xi2s1CDCLK, Xpcm2EXTCLK	I/O	I2S Codec clock input/output		dedicated
Xi2s1SCLK, Xpcm2SCLK	I/O	I2S Bit clock input/output		dedicated
Xi2s1LRCK, Xpcm2FSYNC	I/O	I2S LR channel clock input/output		dedicated
Xi2s1SDI, Xpcm2SIN	I	I2S serial data input		dedicated
Xi2s1SDO, Xpcm2SOUT	O	I2S serial data out		dedicated

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3.7 REGISTER DESCRIPTION

3.7.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
I2S1				
IISCON	0xE210_0000	R/W	Specifies the IIS interface control register	0xE00
IISMOD	0xE210_0004	R/W	Specifies the IIS interface mode register	0x0
IISFIC	0xE210_0008	R/W	Specifies the IIS interface FIFO control register	0x0
IISPSR	0xE210_000C	R/W	Specifies the IIS interface clock divider control register	0x0
IISTXD	0xE210_0010	W	Specifies the IIS interface transmit data register	0x0
IISRXD	0xE210_0014	R	Specifies the IIS interface receive data register	0x0
I2S2				
IISCON	0xE2A0_0000	R/W	Specifies the IIS interface control register	0xE00
IISMOD	0xE2A0_0004	R/W	Specifies the IIS interface mode register	0x0
IISFIC	0xE2A0_0008	R/W	Specifies the IIS interface FIFO control register	0x0
IISPSR	0xE2A0_000C	R/W	Specifies the IIS interface clock divider control register	0x0
IISTXD	0xE2A0_0010	W	Specifies the IIS interface transmit data register	0x0
IISRXD	0xE2A0_0014	R	Specifies the IIS interface receive data register	0x0

NOTE: All registers of IIS interface are accessible by word unit with STR/LDR instructions.

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3.7.1.1 IIS-BUS Interface Special Registers (IISCON)

- IISCON, R/W, Address = 0xE210_0000
- IISCON, R/W, Address = 0xE2A0_0000

IISCON	Bit	Description	R/W	Initial State
Reserved	[31:20]	Reserved. Program to zero.	R/W	12'b0
FRXOFSTATUS	[19]	RX FIFO OverFlow Interrupt Status. And this is used by interrupt clear bit. When this is high, you can do interrupt clear by writing '1'. 0 = Interrupt didn't be occurred. 1 = Interrupt was occurred.	R/W	1'b0
FRXOFINTEN	[18]	RX FIFO OverFlow Interrupt Enable 0 = RXFIFO Under-run INT disable 1 = RXFIFO Under-run INT enable	R/W	1'b0
FTXURSTATUS	[17]	TX FIFO under-run interrupt status. And this is used by interrupt clear bit. When this is high, you can do interrupt clear by writing '1'. 0 = Interrupt didn't be occurred. 1 = Interrupt was occurred.	R/W	1'b0
FTXURINTEN	[16]	TX FIFO Under-run Interrupt Enable 0 = TXFIFO Under-run INT disable 1 = TXFIFO Under-run INT enable	R/W	1'b0
Reserved	[15:12]	Reserved. Program to zero.	R/W	4'b0
LRI	[11]	Left/Right channel clock indication. Note that LRI meaning is dependent on the value of LRP bit of I2SMOD register. 0 = Left (when LRP bit is low) or right (when LRP bit is high) 1 = Right (when LRP bit is low) or left (when LRP bit is high)	R	1'b1
FTXEMPT	[10]	Tx FIFO empty status indication. 0 = FIFO is not empty (ready for transmit data to channel) 1 = FIFO is empty (not ready for transmit data to channel)	R	1'b1
FRXEMPT	[9]	Rx FIFO empty status indication. 0 = FIFO is not empty 1 = FIFO is empty	R	1'b1
FTXFULL	[8]	Tx FIFO full status indication. 0 = FIFO is not full 1 = FIFO is full	R	1'b0
FRXFULL	[7]	Rx FIFO full status indication. 0 = FIFO is not full (ready for receive data from channel) 1 = FIFO is full (not ready for receive data from channel)	R	1'b0

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IISCON	Bit	Description	R/W	Initial State
TXDMAPAUSE	[6]	Tx DMA operation pause command. Note that when this bit is activated at any time, the DMA request will be halted after current on-going DMA transfer is completed. 0 = No pause DMA operation 1 = Pause DMA operation	R/W	1'b0
RXDMAPAUSE	[5]	Rx DMA operation pause command. Note that when this bit is activated at any time, the DMA request will be halted after current on-going DMA transfer is completed. 0 = No pause DMA operation 1 = Pause DMA operation	R/W	1'b0
TXCHPAUSE	[4]	Tx channel operation pause command. Note that when this bit is activated at any time, the channel operation will be halted after left-right channel data transfer is completed. 0 = No pause operation 1 = Pause operation	R/W	1'b0
RXCHPAUSE	[3]	Rx channel operation pause command. Note that when this bit is activated at any time, the channel operation will be halted after left-right channel data transfer is completed. 0 = No pause operation 1 = Pause operation	R/W	1'b0
TXDMACTIVE	[2]	Tx DMA active (start DMA request). Note that when this bit is set from high to low, the DMA operation will be forced to stop immediately. 0 = Inactive 1 = Active	R/W	1'b0
RXDMACTIVE	[1]	Rx DMA active (start DMA request). Note that when this bit is set from high to low, the DMA operation will be forced to stop immediately. 0 = Inactive 1 = Active	R/W	1'b0
I2SACTIVE	[0]	IIS interface active (start operation). 0 = Inactive 1 = Active	R/W	1'b0

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3.7.1.2 IIS-BUS Interface Special Registers (IISMOD)

- IISMOD, R/W, Address = 0xE210_0004
- IISMOD, R/W, Address = 0xE2A0_0004

IISMOD	Bit	Description	R/W	Initial State
Reserved	[31:15]	Reserved. Program to zero.	R/W	1'b0
BLC	[14:13]	Bit Length Control Bit Which decides transmission of 8/16 bits per audio channel 00 = 16 Bits per channel 01 = 8 Bits Per Channel 10 = 24 Bits Per Channel 11 = Reserved	R/W	2'b00
CDCLKCON	[12]	Determine codec clock source 0 = Use internal codec clock source 1 = Get codec clock source from external codec chip * 0 means External CDCLK Input pad enable (Refer to *Figure 3-2*)	R/W	1'b0
MSS	[11]	IIS master or slave mode select. 0 = Master mode 1 = Slave mode	R/W	1'b0
RCLKSRC	[10]	Select RCLK clock source 0 = PCLK is internal source clock for IIS 1 = SCLK_AUDIO (SCLK_AUDIO1 for I2S1, SCLK_AUDIO2 for I2S2) (Refer to *Figure 3-2*)	R/W	1'b0
TXR	[9:8]	Transmit or receive mode select. 00 = Transmit only mode 01 = Receive only mode 10 = Transmit and receive simultaneous mode 11 = Reserved	R/W	2'b00
LRP	[7]	Left/Right channel clock polarity select. 0 = Low for left channel and high for right channel 1 = High for left channel and low for right channel	R/W	1'b0
SDF	[6:5]	Serial data format. 00 = IIS format 01 = MSB-justified (left-justified) format 10 = LSB-justified (right-justified) format 11 = Reserved	R/W	2'b00
RFS	[4:3]	IIS root clock (codec clock) frequency select. 00 = 256 fs, where fs is sampling frequency 01 = 512 fs 10 = 384 fs 11 = 768 fs	R/W	2'b00

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IISMOD	Bit	Description	R/W	Initial State
BFS	[2:1]	Bit clock frequency select. 00 = 32 fs, where fs is sampling frequency 01 = 48 fs 10 =16 fs 11 = 24 fs	R/W	2'b00
Reserved	[0]	Reserved. Program to zero.	R/W	1'b0

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3.7.1.3 IIS-BUS Interface Special Registers (IISFIC)

- IISFIC, R/W, Address = 0xE210_0008
- IISFIC, R/W, Address = 0xE2A0_0008

IISFIC	Bit	Description	R/W	Initial State
Reserved	[31:16]	Reserved. Program to zero.	R/W	16'b0
TFLUSH	[15]	TX FIFO flush command. 0 = No flush 1 = Flush	R/W	1'b0
FTXCNT	[14:8]	TX FIFO data count. FIFO has 64 dept, so value ranges from 0 to 64. N: Data count N of FIFO	R	7'b0
RFLUSH	[7]	RX FIFO flush command. 0 = No flush 1 = Flush	R/W	1'b0
FRXCNT	[6:0]	RX FIFO data count. FIFO has 64 dept, so value ranges from 0 to 64. N: Data count N of FIFO	R	7'b0

3.7.1.4 IIS-BUS Interface Special Registers (IISPSR)

- IISPSR, R/W, Address = 0xE210_000C
- IISPSR, R/W, Address = 0xE2A0_000C

IISPSR	Bit	Description	R/W	Initial State
Reserved	[31:16]	Reserved. Program to zero.	R/W	16'b0
PSRAEN	[15]	Pre-scaler (Clock divider) A active. 0 = Inactive 1 = Active	R/W	1'b0
Reserved	[14]	Reserved. Program to zero.	R/W	1'b0
PSVALA	[13:8]	Pre-scaler (Clock divider) A division value. N: Division factor is N+1	R/W	6'b0
Reserved	[7:0]	Reserved. Program to zero.	R/W	8'b0

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3.7.1.5 IIS-BUS Interface Special Registers (IISTXD)

- IISTXD, W, Address = 0xE210_0010
- IISTXD, W, Address = 0xE2A0_0010

IISTXD	Bit	Description	R/W	Initial State
IISTXD	[31:0]	TX FIFO write data. Note that the left/right channel data is allocated as the following bit fields. R[31:16], L[15:0] when 16-bit BLC R[23:16], L[7:0] when 8-bit BLC	W	32'b0

3.7.1.6 IIS-BUS Interface Special Registers (IISRXD)

- IISRXD, R, Address = 0xE210_0014
- IISRXD, R, Address = 0xE2A0_0014

IISRXD	Bit	Description	R/W	Initial State
IISRXD	[31:0]	RX FIFO read data. Note that the left/right channel data is allocated as the following bit fields. R[31:16], L[15:0] when 16-bit BLC R[23:16], L[7:0] when 8-bit BLC	R	32'b0

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4 AC97 CONTROLLER

This chapter describes the functions and usage of AC97 Controller in S5PV210 RISC microprocessor.

4.1 OVERVIEW OF AC97 CONTROLLER

The AC97 Controller Unit in the S5PV210 supports the features of AC97 revision 2.0. AC97 Controller uses audio controller link (AC-link) to communicate with AC97 Codec. Controller sends the stereo PCM data to Codec. The external digital-to-analog converter (DAC) in the Codec converts the audio sample to an analog audio waveform. Controller receives the stereo PCM data and the mono Mic data from Codec then store in memories. This chapter describes the programming model for the AC97 Controller Unit. The prerequisite in this chapter requires an understanding of the AC97 revision 2.0 specifications.

4.2 KEY FEATURES OF AC97 CONTROLLER

The AC97 Controller includes the following features:

- Independent channels for stereo PCM In, stereo PCM Out, mono MIC In.
- DMA-based operation and interrupt based operation.
- All of the channels support only 16-bit samples.
- Variable sampling rate AC97 Codec interface (48 kHz and below)
- 16-bit, 16 entry FIFOs per channel
- Only primary Codec support

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4.3 AC97 CONTROLLER OPERATION

This section explains the AC97 Controller operation, namely, AC-Link, Power-down sequence and Wake-up sequence.

4.3.1 BLOCK DIAGRAM OF AC97 CONTROLLER

Figure 4-1 shows the functional block diagram of S5PV210 AC97 Controller. The AC97 signals from the AC-link, which is a point-to-point synchronous serial inter-connecting that supports full-duplex data transfers. All digital audio streams and command/status information are communicated via AC-link.

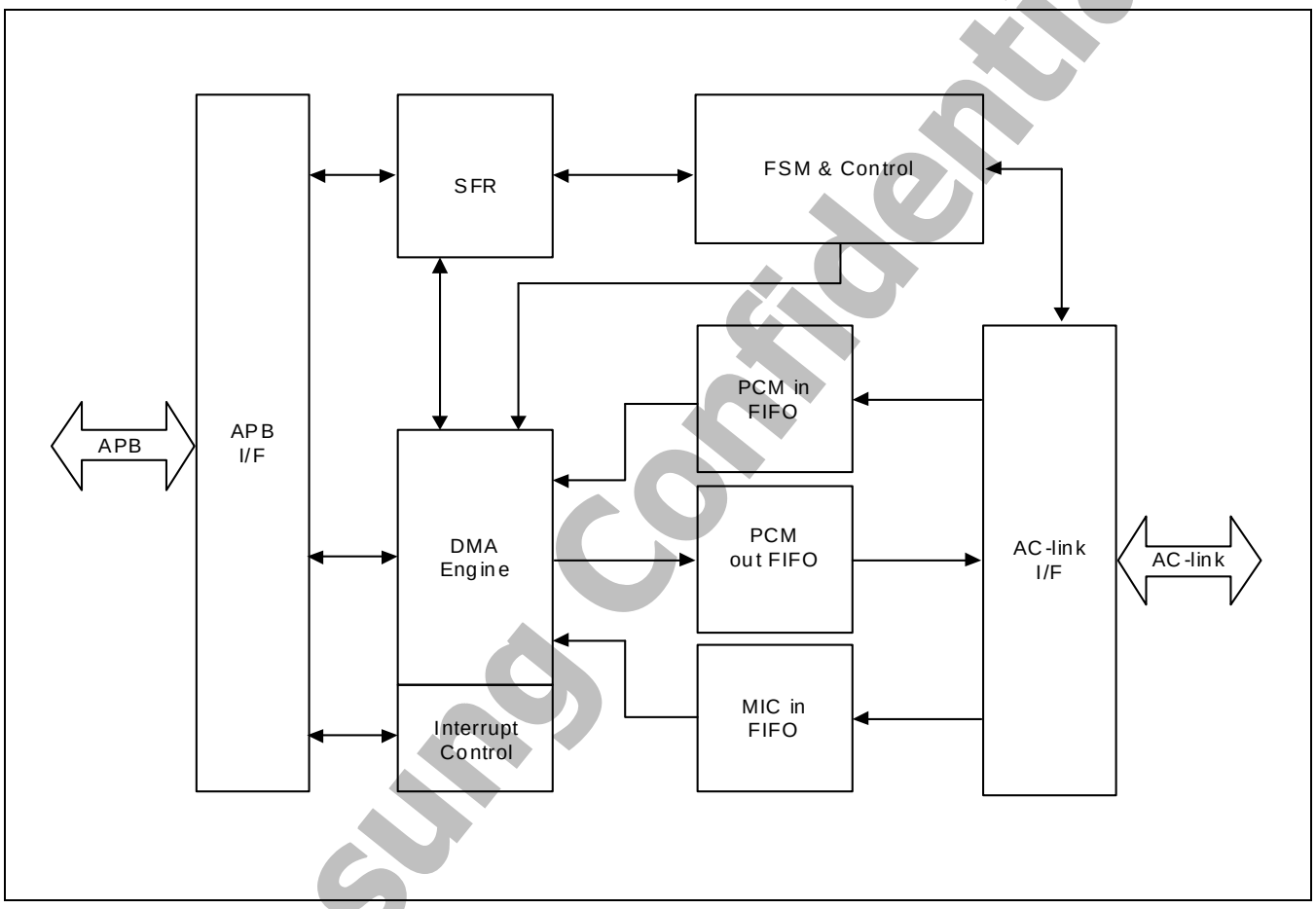

Figure 4-1 AC97 Block Diagram

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4.3.2 INTERNAL DATA PATH

Figure 4-2 shows the internal data path of S5PV210 AC97 Controller. It includes stereo Pulse Code Modulated (PCM) In, Stereo PCM Out and mono Mic-in buffers, which consist of 16-bit and 16 entries buffer. It also has 20-bit I/O shift register via AC-link.

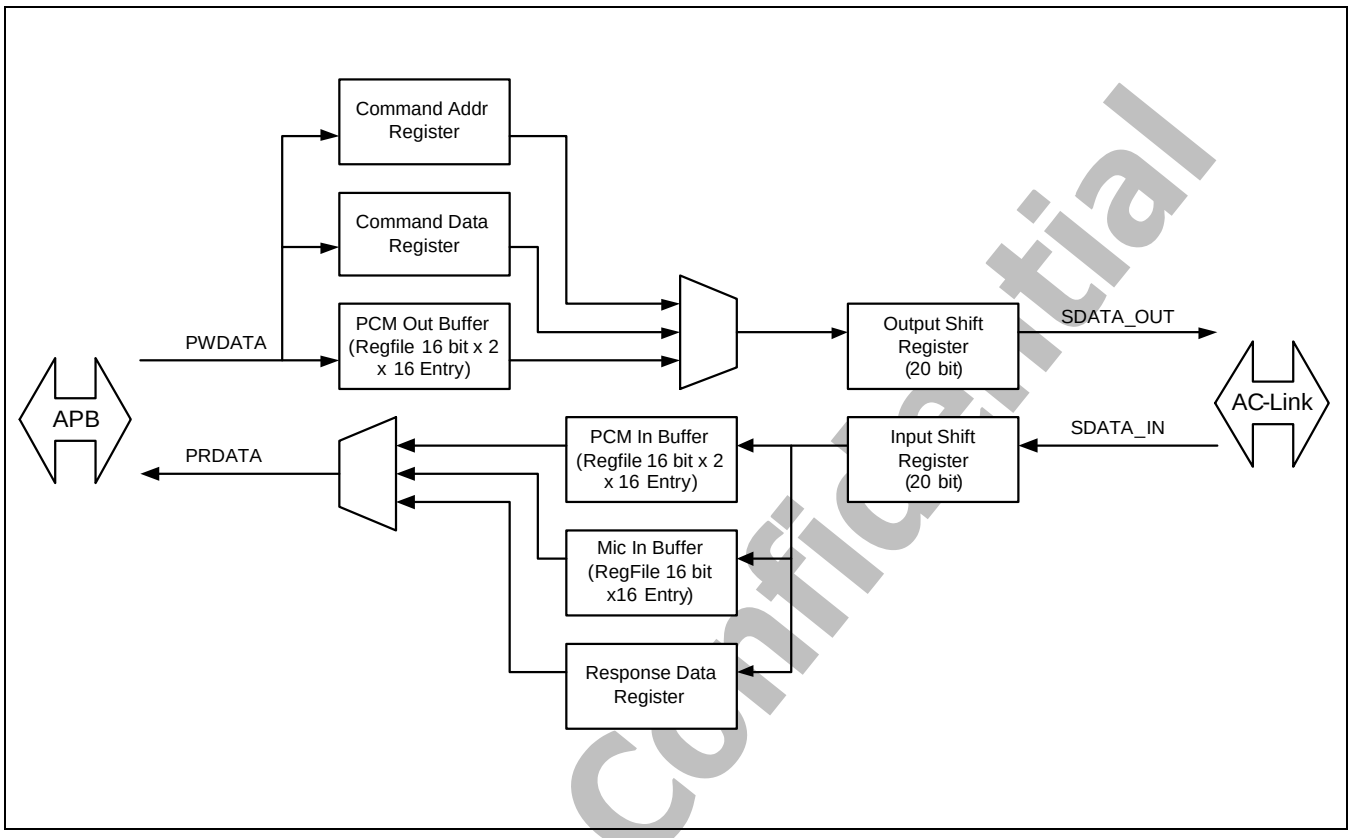

Figure 4-2 Internal Data Path

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4.3.3 OPERATION FLOW CHART

When you initialize the AC97 controller, you must assert system reset or cold reset, because the previous state of the external AC97 audio-codec is not known. This assures that GPIO is already ready. Then you enable the codec ready interrupt. You can check codec ready interrupt by polling or interrupt. When interrupt occurs, you must de-assert codec ready interrupt. Use DMA or PIO (directly to write data to register) to transmit data from memory to register or from register to memory. If internal FIFOs (TX FIFO or RX FIFO) are not empty, then let data be transmitted.

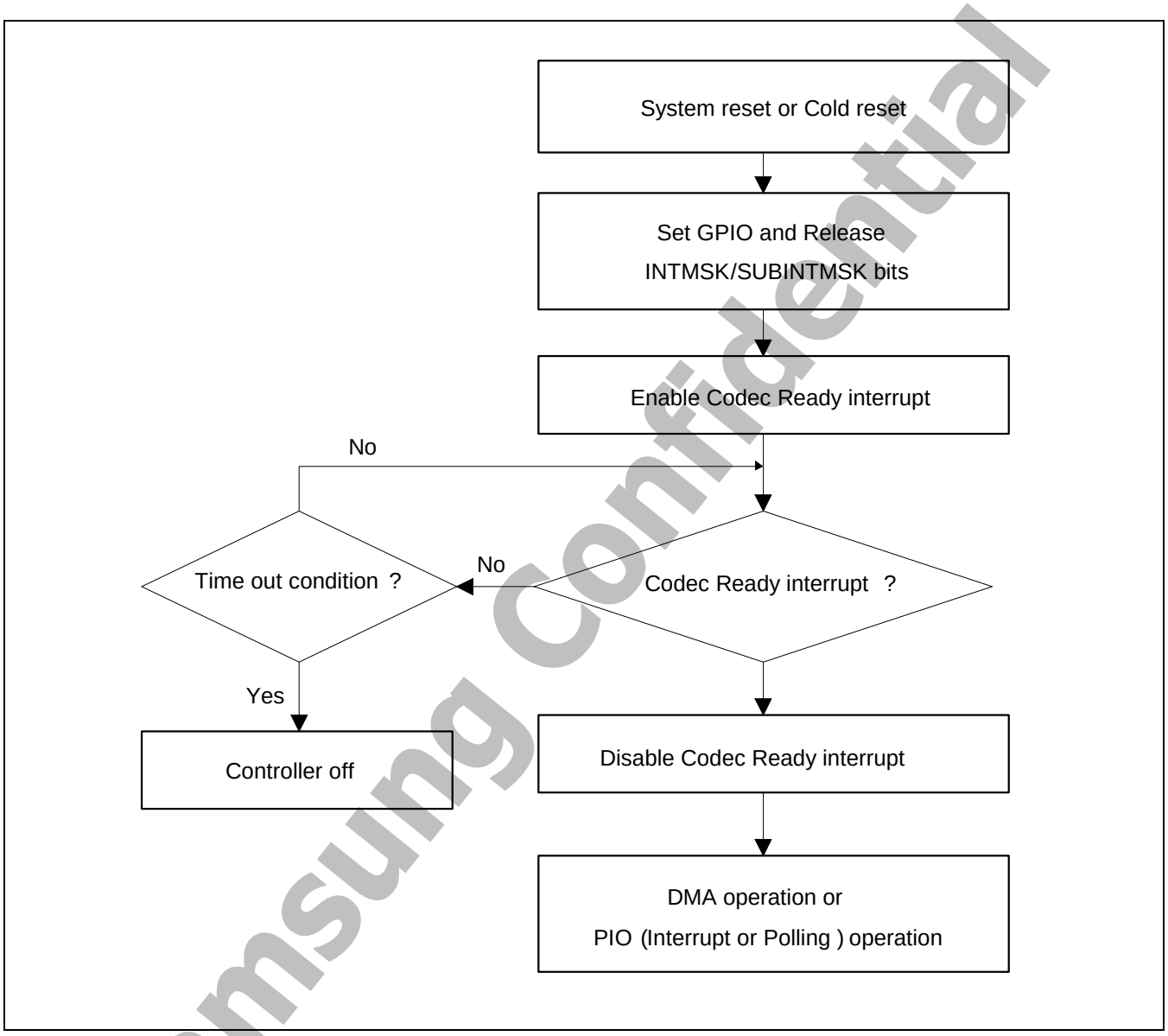

Figure 4-3 AC97 Operation Flow Chart

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4.3.4 AC-LINK DIGITAL INTERFACE PROTOCOL

Each AC97 Codec incorporates a five-pin digital serial interface that links it to the S5PV210 AC97 Controller. AC-link is a full-duplex, fixed-clock and PCM digital stream. It employs a time division multiplexed (TDM) scheme to handle control register accesses and multiple input and output audio streams. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams. Each stream has 20-bit sample resolution and requires a DAC and an analog-to-digital converter (ADC) with a minimum 16-bit resolution.

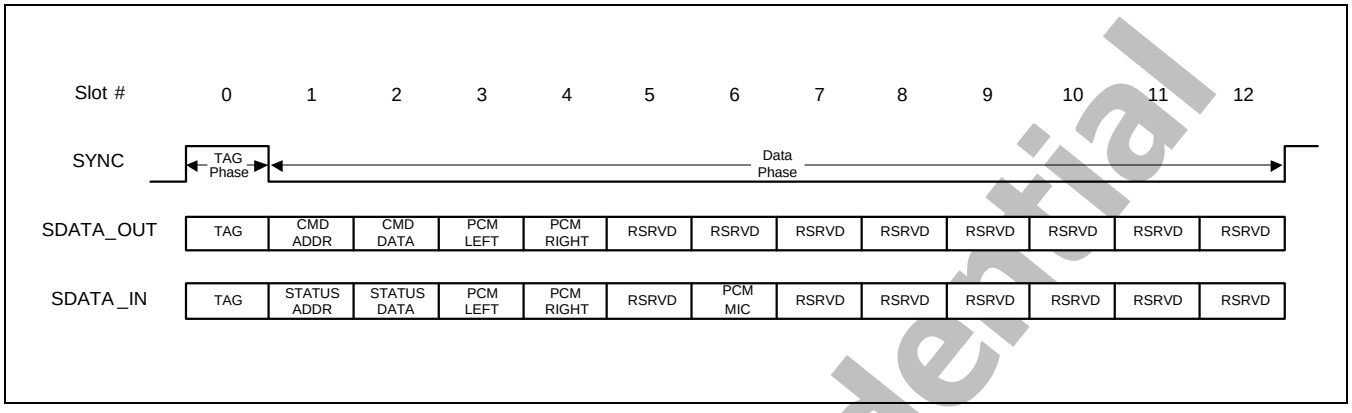

Figure 4-4 Bi-directional AC-link Frame with Slot Assignments

Figure 4-4 shows the slot definitions supported by S5PV210 AC97 Controller. The S5PV210 AC97 Controller provides synchronization for all data transaction on the AC-link.

A data transaction is made up of 256 bits of information broken into groups of 13 time slots and is called a frame. Time slot 0 is called the Tag Phase and it is 16 bits long. The other 12 time slots are called the Data Phase. The Tag Phase contains one bit that identifies a valid frame and 12 bits that identify the time slots in the Data Phase that contain valid data. Each time slot in the Data Phase is 20 bits long. A frame begins when SYNC goes high. The amount of time that SYNC is high corresponds to the Tag Phase. AC97 frames occur at fixed 48 kHz intervals and are synchronous to the 12.288 MHz bit rate clock, BITCLK.

The controller and the Codec use the SYNC and BITCLK to determine when to send transmit data and when to sample received data. A transmitter transitions the serial data stream on each rising edge of BITCLK and a receiver samples the serial data stream on falling edges of BITCLK. The transmitter must tag the valid slots in its serial data stream. The valid slots are tagged in slot 0. Serial data on the AC-link is ordered most significant bit (MSB) to least significant bit (LSB). The Tag Phase's first bit is bit 15 and the first bit of each slot in Data Phase is bit 19. The last bit in any slot is bit 0.

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4.3.4.1 AC-link Output Frame (SDATA_OUT)

Slot 0: Tag Phase

In slot 0, the first bit is a bit (SDATA_OUT, bit 15) which represents the validity of the entire frame. If bit 15 is 1, the current frame contains at least a valid time slot. The next 12-bit positions correspond each 12 time slot contains valid data. Bits 0 and 1 of slot 0 are used as CODEC IO bits for I/O reads and writes to the CODEC registers as described in the next section. In this way, data streams of differing sample rate can be transmitted across AC-link at its fixed 48 kHz audio frame rate.

Slot 1: Command Address Port

In slot 1, it communicates control register address and write/read command information to the AC97 controller. When software accesses the primary CODEC, the hardware configures the frame as follows:

- In slot 0, the valid bit for 1, 2 slots are set.
- In slot 1, bit 19 is set (read) or clear(write). Bits 18-12 (of slot 1) are configured to specify the index to the CODEC register. Others are filled with 0's(reserved).
- In slot 2, it configured with the data which is for writing because of output frame.

Slot 2: Command Data Port

In slot 2, this is the write data with 16-bit resolution ([19:4] is valid data)

Slot 3: PCM Playback Left channel

Slot 3 is audio output frame is the composite digital audio left stream. If a sample has a resolution that is less than 16 bits, the AC97 controller fills all training non-valid bit positions in the slot with zeroes.

Slot 4: PCM Playback Right channel

Slot 4 which is audio output frame is the composite digital audio right stream. If a sample has a resolution that is less than 16 bits, the AC97 controller fills all training non-valid bit positions in the slot with zeroes.

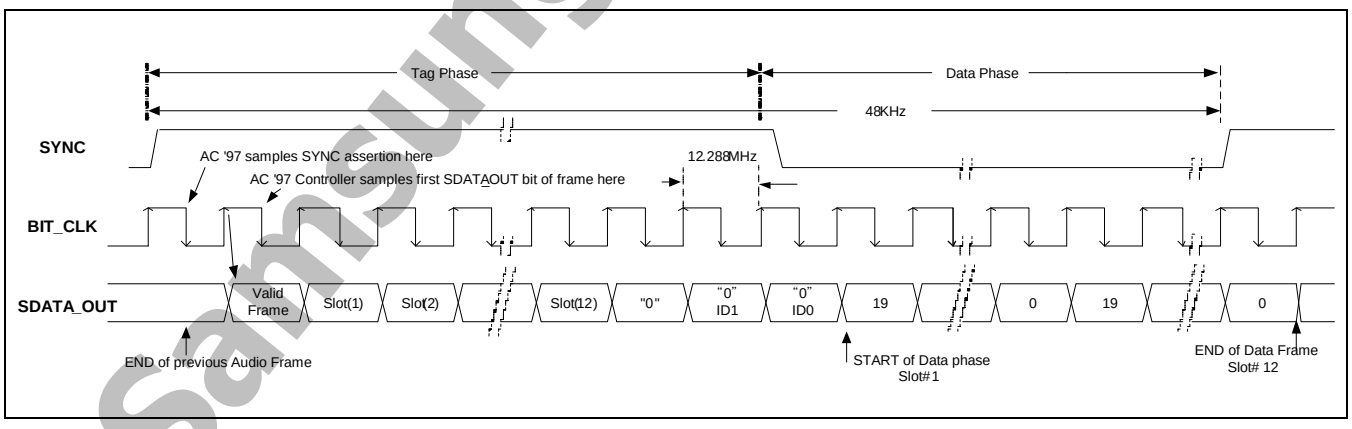

Figure 4-5 AC-link Output Frame

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4.3.5 AC-LINK INPUT FRAME (SDATA_IN)

Slot 0: Tag Phase

In slot 0, the first bit (SDATA_OUT, bit 15) indicates whether the AC97 controller is in the CODEC ready state. If the CODEC Ready bit is 0, it means that the AC97 controller is not ready for normal operation. This condition is normal after the power is de-asserted on reset and the AC97 controller voltage references are settling.

Slot 1: Status Address Port/SLOTREQ bits

The status port monitors the status of the AC97 controller functions. It is not limited to mixer settings and power management. Audio input frame slot 1's stream echoes the control register index for the data to be returned in slot 2, if the controller tags slots 1 and 2 as valid during slot 0. The controller only accepts status data if the accompanying status address matches the last valid command address issued during the most recent read command. For multiple sample rate output, the CODEC examines its sample-rate control registers, its FIFOs' states, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits asserted during the current audio input frame indicate which output slots require data from the controller in the next audio output frame. For fixed 48 kHz operation, the SLOTREQ bits are set active (low), and a sample is transferred in each frame. For multiple sample-rate input, the "tag" bit for each input slot indicates whether valid data is present.

Table 4-1 Input Slot 1 Bit Definitions

Bit	Description
19	Reserved (Filled with zero)
18-12	Control register index (Filled with zeroes if AC97 tags is invalid)
11	Slot 3 request: PCM Left channel
10	Slot 4 request: PCM Right channel
9	Slot 5 request: NA
8	Slot 6 request: MIC channel
7	Slot 7 request: NA
6	Slot 8 request: NA
5	Slot 9 request: NA
4	Slot 10 request: NA
3	Slot 11 request: NA
2	Slot 12 request: NA
1, 0	Reserved (Filled with zero)

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Slot 2: Status Data Port

In slot 2, this is the status data with 16-bit resolution ([19:4] is valid data)

Slot 3: PCM Record Left channel

Slot 3 which is audio input frame is the left channel audio output of the AC97 Codec. If a sample has a resolution that is less than 16 bits, the AC97 Codec fills all training non-valid bit positions in the slot with zeroes.

Slot 4: PCM Record Right channel

Slot 4 which is audio input frame is the right channel audio output of the AC97 Codec. If a sample has a resolution that is less than 16 bits, the AC97 Codec fills all training non-valid bit positions in the slot with zeroes.

Slot 6: Microphone Record Data

The AC97 Controller supports 16-bit resolution for the MIC-in channel.

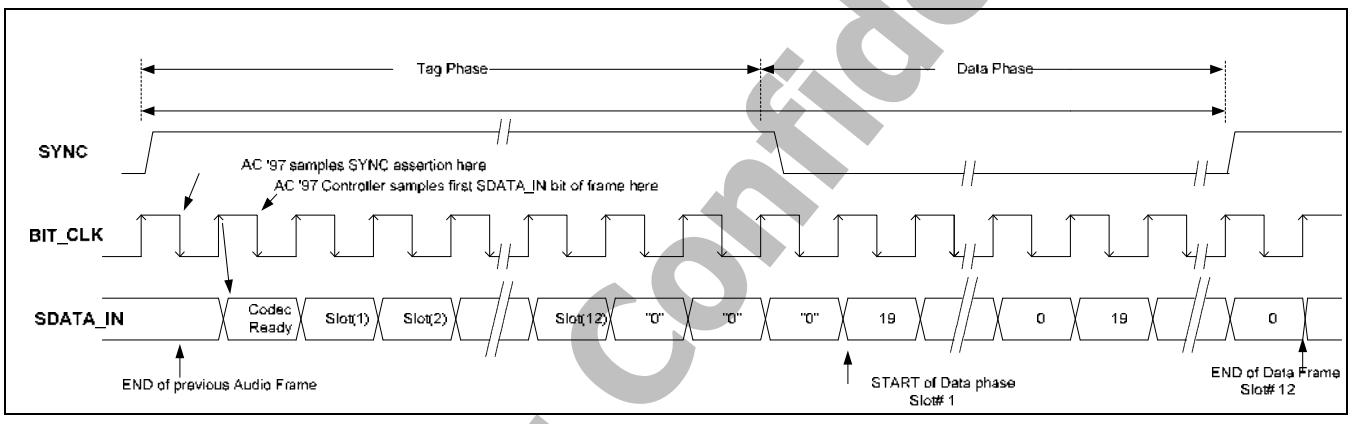

Figure 4-6 AC-link Input Frame

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4.3.6 AC97 POWER-DOWN

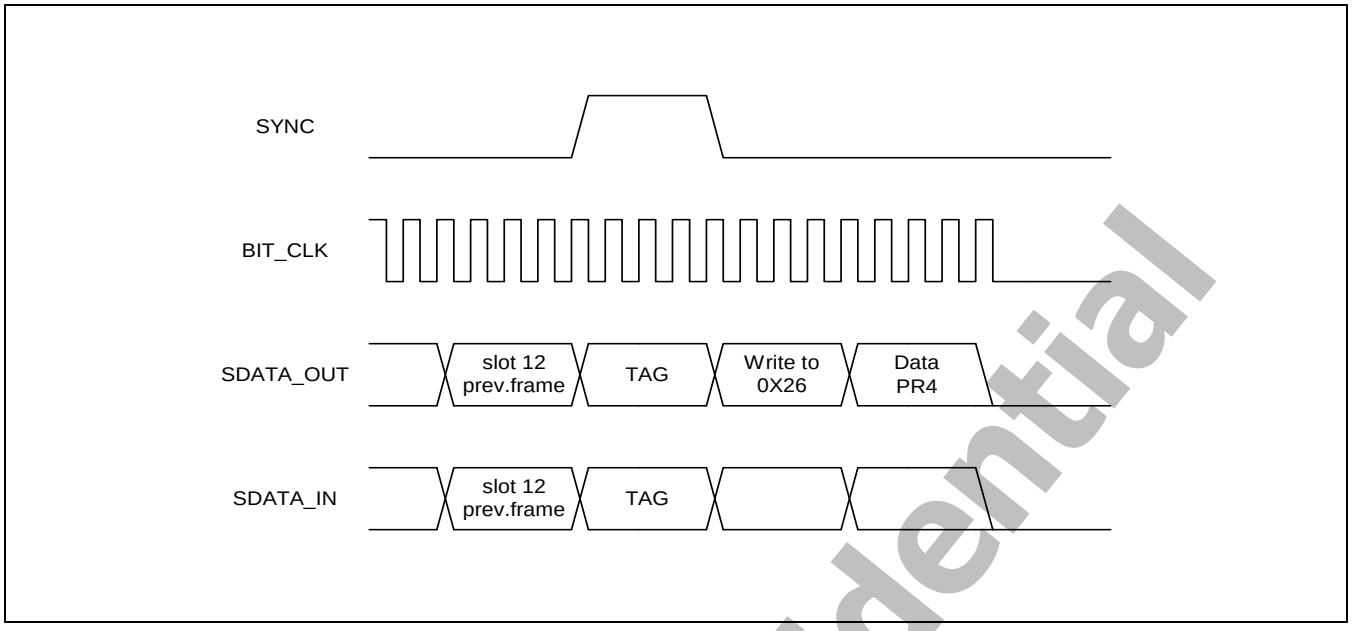

Figure 4-7 AC97 Power-down Timing

4.3.6.1 Powering Down the AC-link

The AC-link signals enter a low power mode when the AC97 Codec Power-down register (0x26) bit PR4 is set to 1 (by writing 0x1000). Then the Primary Codec drives both BITCLK and SDATA_IN to a logic low voltage level. The sequence follows the timing diagram as shown in *Figure 4-7*.

The AC97 Controller transmits the write to Power-down register (0x26) via AC-link. Set up the AC97 Controller so that it does not transmit data to slots 3-12 when it writes to the Power-down register bit PR4 (data 0x1000), and it does not require the Codec to process other data when it receives a power down request. When the Codec processes the request it immediately transitions BITCLK and SDATA_IN to a logic low level. The AC97 Controller drives SYNC and SDATA_OUT to a logic low level after programming the AC_GLBCTRL register.

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4.3.6.2 Waking up the AC-link - Wake Up Triggered by the AC97 Controller

AC-link protocol provides a cold AC97 reset and a warm AC97 reset. The current power-down state ultimately dictates which AC97 reset is used. Registers must stay in the same state during all power-down modes unless a cold AC97 reset is performed. In a cold AC97 reset, the AC97 registers are initialized to their default values. After a power down, the AC-link must wait for a minimum of four audio frame times after the frame in which the power down occurred before it can be reactivated by reasserting the SYNC signal. When AC-link powers up, Codec ready bit (input slot 0, bit 15) indicates that AC-link is ready for operation.

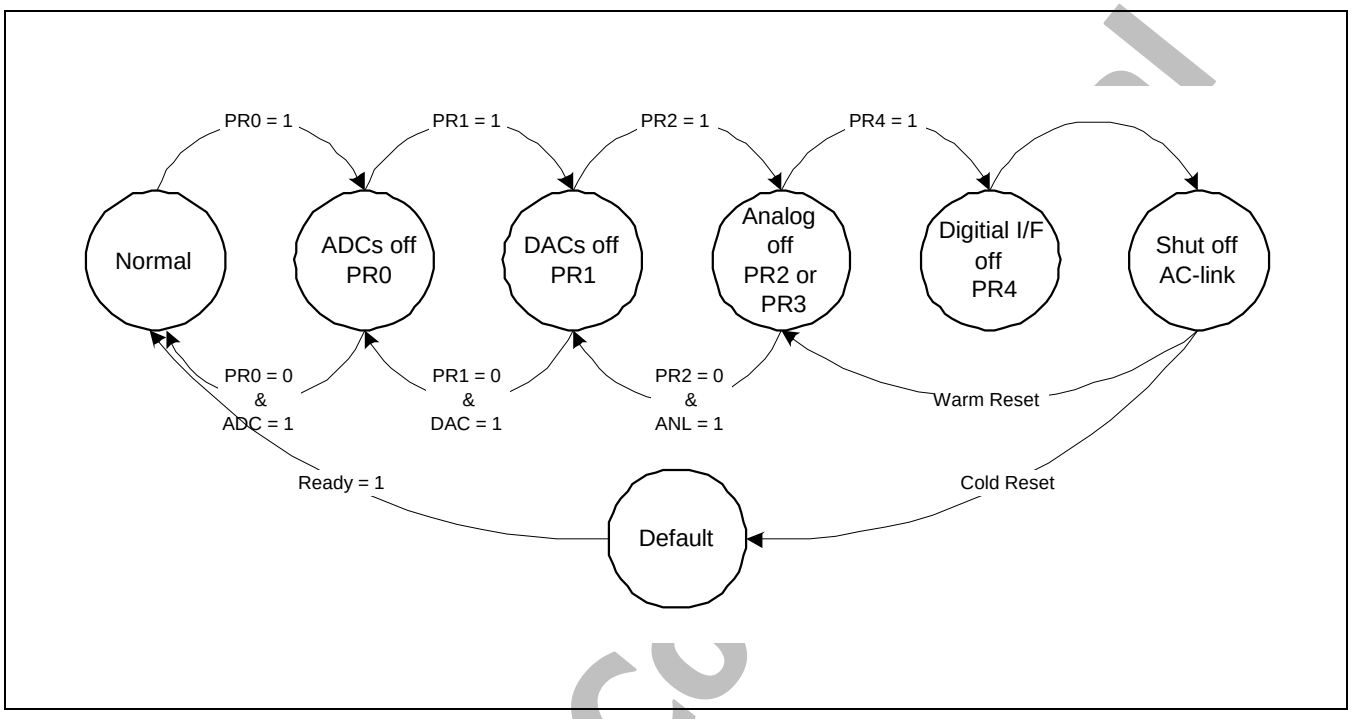

Figure 4-8 AC97 Power down/Power up Flow

4.3.6.3 Cold AC97 Reset

A cold reset is generated when the nRESET pin is asserted through the AC_GLBCTRL. Asserting and deasserting nRESET activates BITCLK and SDATA_OUT. All AC97 control registers are initialized to their default power on reset values. nRESET is an asynchronous AC97 input.

4.3.6.4 Warm AC97 Reset

A Warm AC97 reset reactivates the AC-link without altering the current AC97 register values. A warm reset is generated when BITCLK is absent and SYNC is driven high. In normal audio frames, SYNC is a synchronous AC97 input. When BITCLK is absent, SYNC is treated as an asynchronous input used to generate a warm reset to AC97.The AC97 Controller must not activate BITCLK until it samples SYNC low again. This prevents a new audio frame being falsely detected.

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4.3.6.5 AC97 State Diagram

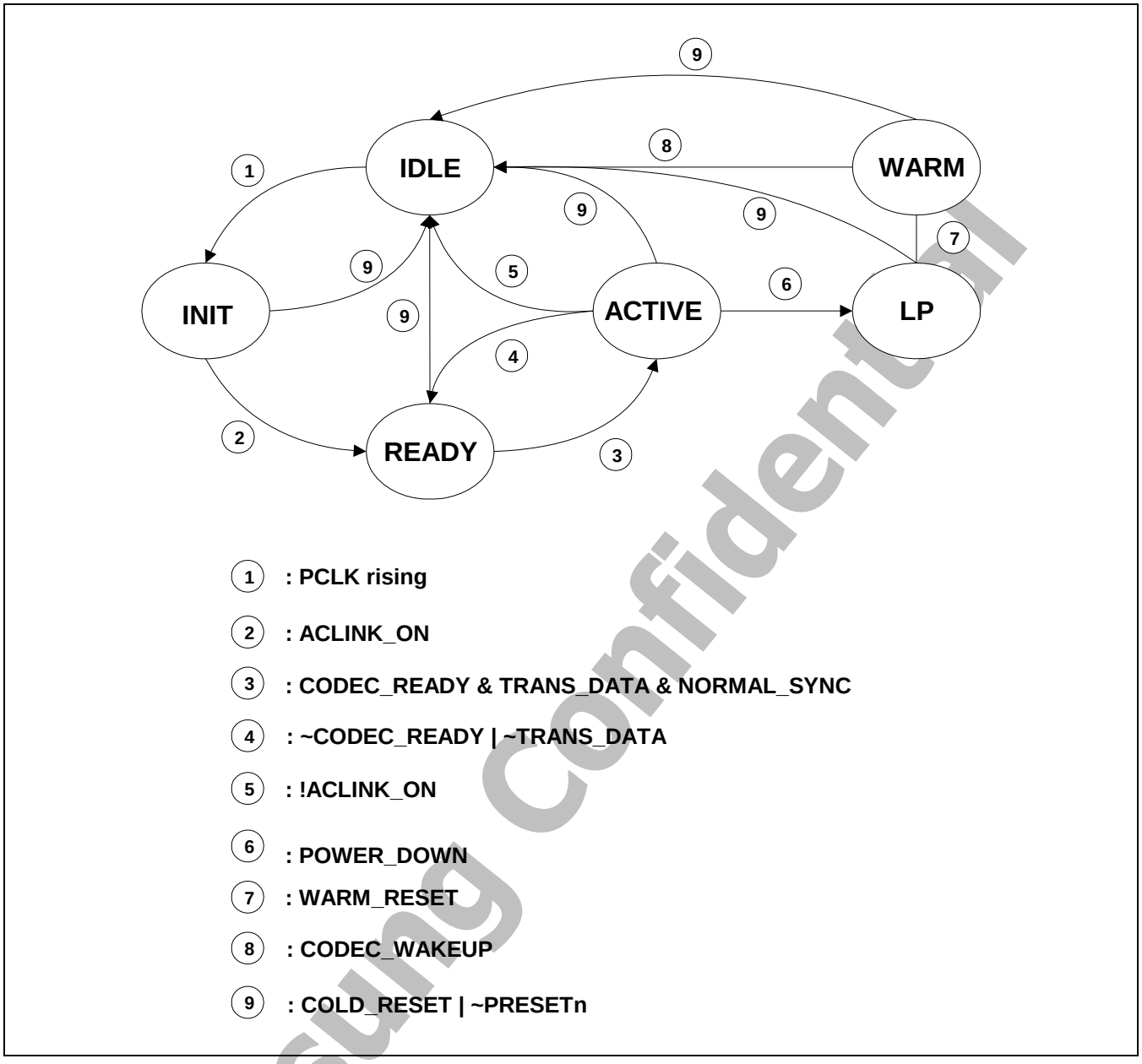

Figure 4-9 AC97 State Diagram

Figure 4-9 shows the state diagram of AC97 controller. It is useful to check AC97 controller state machine. State machine shown in above figure is synchronized by peripheral clock (PCLK). Use AC_GLBSTAT register to monitor state.

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4.4 I/O DESCRIPTION

AC97 external pads are shared with I2S. In order to use these pads for AC97, GPIO must be set before the AC97 starts. For mode information, refer to the GPIO chapter of this manual for exact GPIO setting

Signal	I/O	Description	Pad	Type
AC_nRESET	O	Active-low CODEC reset.	Xi2s1CDCLK	muxed
AC_BIT_CLK	I	12.288MHz bit-rate clock.	Xi2s1SCLK	muxed
AC_SYNC	O	48 kHz frame indicator and synchronizer	Xi2s1LRCK	muxed
AC_SDATA_OUT	O	Serial audio output data.	Xi2s1SDO	muxed
AC_SDATA_IN	I	Serial audio input data.	Xi2s1SDI	muxed

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4.5 REGISTER DESCRIPTION

4.5.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
AC_GLBCTRL	0xE220_0000	R/W	Specifies the AC97 Global Control Register	0x00000000
AC_GLBSTAT	0xE220_0004	R	Specifies the AC97 Global Status Register	0x00000001
AC_CODEC_CMD	0xE220_0008	R/W	Specifies the AC97 Codec Command Register	0x00000000
AC_CODEC_STAT	0xE220_000C	R	Specifies the AC97 Codec Status Register	0x00000000
AC_PCMADDR	0xE220_0010	R	Specifies the AC97 PCM Out/In Channel FIFO Address Register	0x00000000
AC_MICADDR	0xE220_0014	R	Specifies the AC97 MIC In Channel FIFO Address Register	0x00000000
AC_PCMDATA	0xE220_0018	R/W	Specifies the AC97 PCM Out/In Channel FIFO Data Register	0x00000000
AC_MICDATA	0xE220_001C	R/W	Specifies the AC97 MIC In Channel FIFO Data Register	0x00000000

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4.5.1.1 AC97 Global Control Register (AC_GLBCTRL, R/W, Address = 0xE220_0000)

This is the global register of the AC97 controller. There are interrupt control registers, DMA control registers, AC-Link control register, data transmission control register and related reset control register.

AC_GLBCTRL	Bit	Description	Initial State
-	[31]	Reserved.	0
Codec ready interrupt clear	[30]	1 = Interrupt clear(write only)	0
PCM out channel underrun interrupt clear	[29]	1 = Interrupt clear(write only)	0
PCM in channel overrun interrupt clear	[28]	1 = Interrupt clear(write only)	0
MIC in channel overrun interrupt clear	[27]	1 = Interrupt clear(write only)	0
PCM out channel threshold interrupt clear	[26]	1 = Interrupt clear(write only)	0
PCM in channel threshold interrupt clear	[25]	1 = Interrupt clear(write only)	0
MIC in channel threshold interrupt clear	[24]	1 = Interrupt clear(write only)	0
-	[23]	Reserved	0
Codec ready interrupt enable	[22]	0 = Disables 1 = Enables	0
PCM out channel underrun interrupt enable	[21]	0 = Disables 1 = Enables (FIFO is empty)	0
PCM in channel overrun interrupt enable	[20]	0 = Disables 1 = Enables (FIFO is full)	0
Mic in channel overrun interrupt enable	[19]	0 = Disables 1 = Enables (FIFO is full)	0
PCM out channel threshold interrupt enable	[18]	0 = Disables 1 = Enables (FIFO is half empty)	0
PCM in channel threshold interrupt enable	[17]	0 = Disables 1 = Enables (FIFO is half full)	0
MIC in channel threshold interrupt enable	[16]	0 = Disables 1 = Enables (FIFO is half full)	0
-	[15:14]	Reserved.	00
PCM out channel transfer mode	[13:12]	00 = Off 01 = PIO 10 = DMA 11 = Reserved	00
PCM in channel transfer mode	[11:10]	00 = Off 01 = PIO 10 = DMA 11 = Reserved	00
MIC in channel transfer mode	[9:8]	00 = Off	00

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AC_GLBCTRL	Bit	Description	Initial State
		01 = PIO 10 = DMA 11 = Reserved	
-	[7:4]	Reserved.	0000
Transfer data enable using AC-link	[3]	0 = Disables 1 = Enables	0
AC-Link on	[2]	0 = Off 1 = SYNC signal transfer to Codec	0
Warm reset	[1]	0 = Normal 1 = Wake up codec from power down	0
Cold reset	[0]	0 = Normal 1 = Reset Codec and Controller logic Notes: 1. During Cold reset, writing to any AC97 Registers is not affected. 2. When recovering from Cold reset, writing to any AC97 Registers is not affected. Example: For consecutive Cold reset and Warm reset, first set AC_GLBCTRL=0x1 then set AC_GLBCTRL=0x0. After recovering from cold reset set AC_GLBCTRL=0x2 then AC_GLBCTRL=0x0.	0

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4.5.1.2 AC97 Global Status Register (AC_GLBSTAT, R, Address = 0xE220_0004)

This is the status register. When the interrupt occurs, you can check the source of interrupt.

AC_GLBSTAT	Bit	Description	Initial State
-	[31:23]	Reserved.	0x00
Codec ready interrupt	[22]	0 = Not requested 1 = Requested	0
PCM out channel underrun interrupt	[21]	0 = Not requested 1 = Requested	0
PCM in channel overrun interrupt	[20]	0 = Not requested 1 = Requested	0
MIC in channel overrun interrupt	[19]	0 = Not requested 1 = Requested	0
PCM out channel threshold interrupt	[18]	0 = Not requested 1 = Requested	0
PCM in channel threshold interrupt	[17]	0 = Not requested 1 = Requested	0
MIC in channel threshold interrupt	[16]	0 = Not requested 1 = Requested	0
-	[15:3]	Reserved.	0x000
Controller main state	[2:0]	000 = Idle 001 = Init 010 = Ready 011 = Active 100 = LP 101 = Warm	001

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4.5.1.3 AC97 Codec Command Register (AC_CODEC_CMD, R/W, Address = 0xE220_0008)

When you control writing or reading, you must set the Read enable bit. If you want to write data to the AC97 Codec, you set the index (or address) of the AC97 Codec and data.

AC_CODEC_CMD	Bit	Description	Initial State
-	[31:24]	Reserved	0x00
Read enable	[23]	0 = Command write (note) 1 = Status read	0
Address	[22:16]	Codec command address	0x00
Data	[15:0]	Codec command data	0x0000

NOTE: When the commands are written on the AC_CODDEC_CMD register, it is recommended to have more than 1 / 48 kHz delay time between the command and the next command.

4.5.1.4 AC97 Codec Status Register (AC_CODEC_STAT, R, Address = 0xE220_000C)

If the Read enable bit is 1 and Codec command address is valid, Codec status data is also valid.

AC_CODEC_STAT	Bit	Description	Initial State
-	[31:23]	Reserved.	0x00
Address	[22:16]	Codec status address	0x00
Data	[15:0]	Codec status data	0x0000

NOTE: Steps to read data from AC97 codec register via the AC_CODDEC_STAT register:

1. Write command address and data on the AC_CODEC_CMD register with Bit[23] =1.
2. Set a proper delay time. It depends on Codec type.
3. Read command address and data from AC_CODEC_STAT register.

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4.5.1.5 AC97 PCM OUT/IN Channel FIFO Address Register (AC_PCMADDR, R, Address = 0xE220_0010)

To index the internal PCM FIFOs address.

AC_PCMADDR	Bit	Description	Initial State
-	[31:28]	Reserved.	0000
Out read address	[27:24]	PCM out channel FIFO read address	0000
-	[23:20]	Reserved.	0000
In read address	[19:16]	PCM in channel FIFO read address	0000
-	[15:12]	Reserved.	0000
Out write address	[11:8]	PCM out channel FIFO write address	0000
-	[7:4]	Reserved.	0000
In write address	[3:0]	PCM in channel FIFO write address	0000

4.5.1.6 AC97 MIC IN Channel FIFO Address Register (AC_MICADDR, R, Address = 0xE220_0014)

To index the internal MIC-in FIFO address.

AC_MICADDR	Bit	Description	Initial State
-	[31:20]	Reserved.	0000
Read address	[19:16]	MIC in channel FIFO read address	0000
-	[15:4]	Reserved.	0x000
Write address	[3:0]	MIC in channel FIFO write address	0000

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4.5.1.7 AC97 PCM OUT/IN Channel FIFO Data Register (AC_PCMDATA, R/W, Address = 0xE220_0018)

This is PCM out/in channel FIFO data register.

AC_PCMDATA	Bit	Description	Initial State
Right data	[31:16]	PCM out/in right channel FIFO data Read = PCM in right channel Write = PCM out right channel	0x0000
Left data	[15:0]	PCM out/in left channel FIFO data Read = PCM in left channel Write = PCM out left channel	0x0000

4.5.1.8 AC97 MIC IN Channel FIFO Data Register (AC_MICDATA, R/W, Address = 0xE220_001C)

This is MIC-in channel FIFO data register.

AC_MICDATA	Bit	Description	Initial State
-	[31:16]	Reserved	0x0000
Mono data	[15:0]	MIC in mono channel FIFO data	0x0000

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5 PCM AUDIO INTERFACE

5.1 OVERVIEW OF PCM AUDIO INTERFACE

The PCM Audio Interface module provides PCM bi-directional serial interface to an external Codec.

5.2 KEY FEATURES OF PCM AUDIO INTERFACE

The PCM Audio interface includes the following features:

- 16-bit PCM, 3 ports audio interface
- Supports only master mode.
- All PCM serial timings and strobes including the main shift clock, are based on an PCM_EXTCLK
- OSC, EPLL_FOUT or AUDIO_SCLK can be used as PCM_EXTCLK source clock
- Optional timing based on the internal APB PCLK
- Input (16-bit x 32depth) and output (16-bit x 32depth) FIFOs to buffer data
- Optional DMA interface for TX and/or RX

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5.3 PCM AUDIO INTERFACE

The PCM Audio Interface provides a serial interface to an external Codec. The PCM module receives an input PCMCODEC_CLK to generate the serial shift timing. The PCM interface outputs a serial data out, a serial shift clock, and a sync signal. Data is received from the external Codec over a serial input line. The serial data in, serial data out, and sync signal are all synchronized to the serial shift clock.

The serial shift clock, PCMSCLK, is generated from a programmable divide of the input PCMCODEC_CLK. The sync signal, PCMSYNC, is generated based upon a programmable number of serial clocks and is one serial clock wide.

The PCM data words are 16-bit wide, serially shifted out 1-bit per PCMSCLK. Only one 16-bit word is shifted out for each PCMSYNC. The PCMSCLK will continue to toggle even after all 16-bit have been shifted out. The PCMSOUT data iis not valid after the 16-bit word is complete. The next PCMSYNC will signal the start of the next PCM data word.

The TX FIFO provides the 16-bit data word to be serially shifted out. This data is serially shifted out MSB first, one bit per PCMSCLK. The PCM serial output data, PCMSOUT, is clocked out using the rising edge of the PCMSCLK. The MSB bit position relative to the PCMSYNC is programmable to either match the PCMSYNC or one PCMCLK later. After all 16-bit have been shifted out, to indicate the end of the transfer you can generate an interrupt.

At the same time data is being shifted out, the PCMSIN input is used to serially shift data from the external codec. The data is received MSB first and is clocked in on the falling edge of PCMSCLK. The position of the first bit is programmable to be coincident with the PCMSYNC or one PCMSCLK later.

The first 16-bit are serially shifted into the PCM_DATAIN register which is then loaded into the RX FIFO. Subsequent bits are ignored until the next PCMSYNC.

Various Interrupts are available to indicate the status of the RX and TX FIFO. Each FIFO has a programmable flag to indicate when the CPU needs to service the FIFO. In the RX FIFO, there is an interrupt, which will be raised when the FIFO exceeds a certain programmable ALMOST_FULL depth. Similarly there is a programmable ALMOST_EMPTY interrupt for the TX FIFO.

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5.4 PCM TIMING

Figure 5-1 shows the timing relationship for the PCM transfers.

Note in all cases, the PCM shift timing is derived by dividing the input clock, PCMCODEC_CLK. While the timing is based upon the PCMCODEC_CLK, there is no attempt to realign the rising edge of the output PCMSCLK with the original PCMCODEC_CLK input clock. These edges will be skewed by internal delay through the pads as well as the divider logic. This does not represent a problem because the actual shift clock, PCMSCLK, is synchronized with the data. Furthermore, even if the PCMSCLK output is not used, the skew will be significantly less than the period of the PCMCODEC_CLK and does not represent a problem since most PCM interfaces capture data on the falling edge of the clock.

Figure 5-1 shows a PCM transfer with the MSB configured to be coincident with the PCMSYNC. This MSB positioning corresponds to setting the TX_MSB_POS and RX_MSB_POS bits in PCMCTL register to be 0.

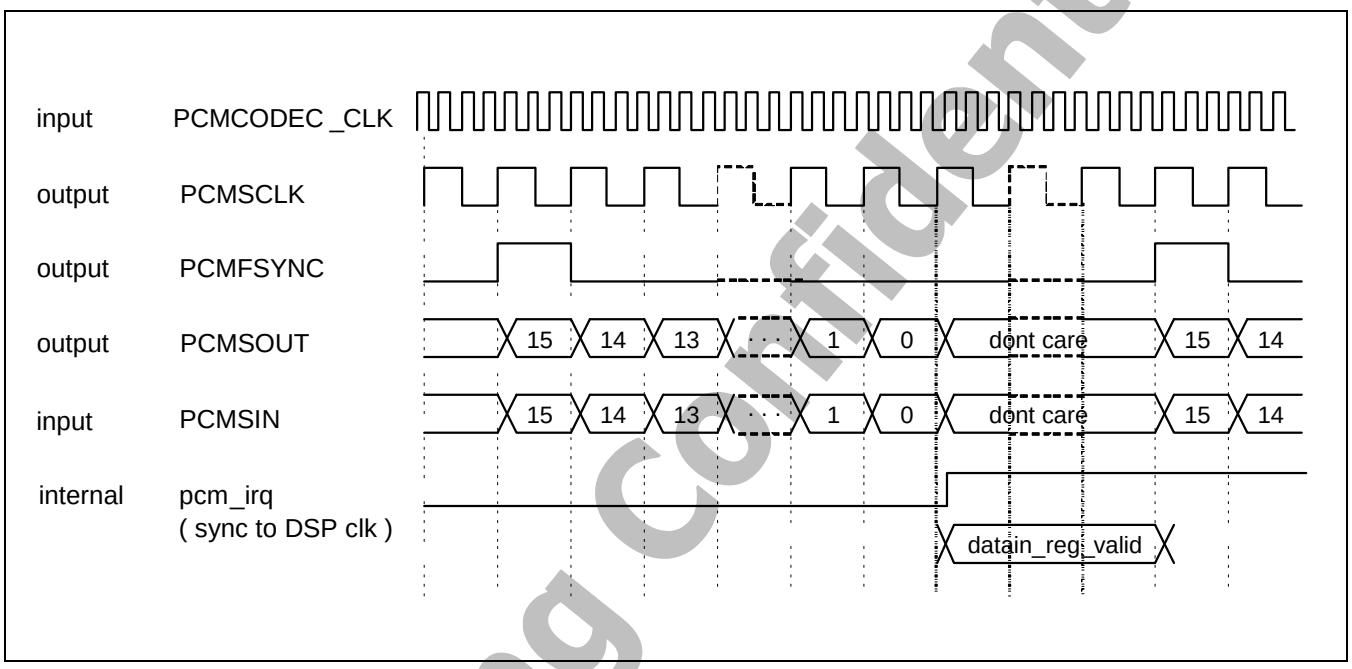

Figure 5-1 PCM timing, POS_MSB_WR/RD = 0

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Figure 5-2 shows a PCM transfer with the MSB configured one shift clock after the PCMSYNC. This MSB positioning corresponds to setting the TX_MSB_POS and RX_MSB_POS bits in PCMCTL register to be 1.

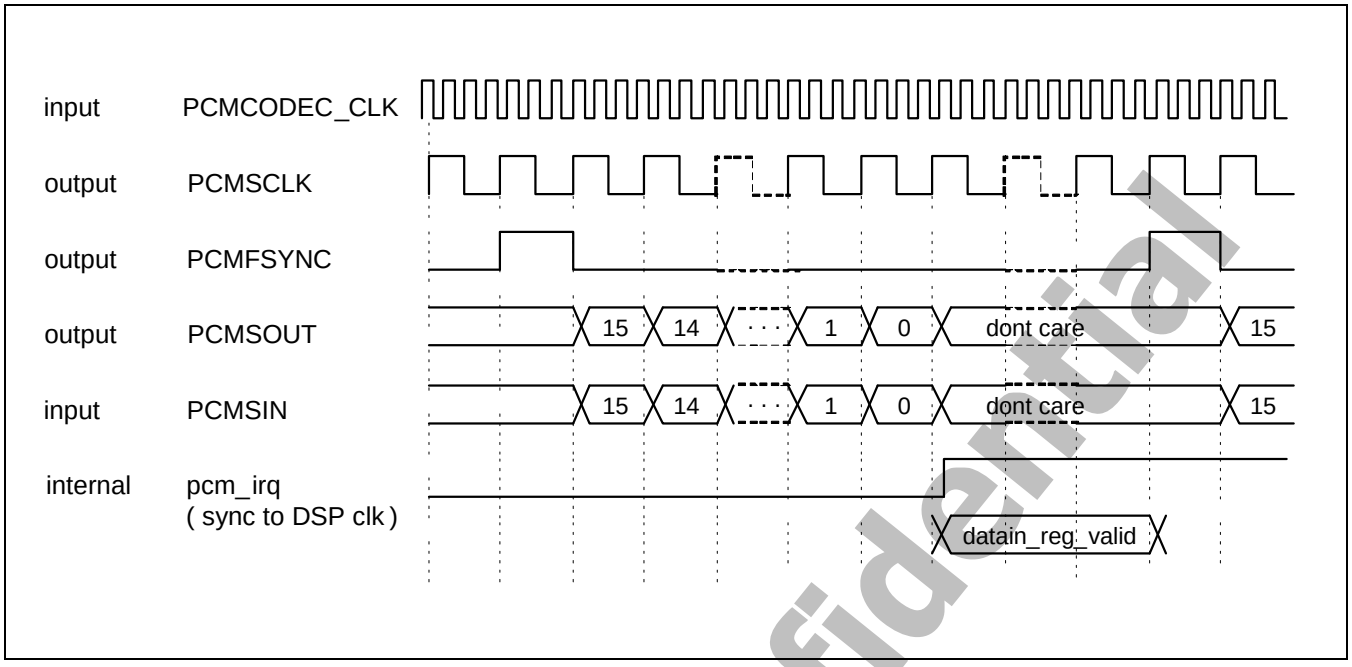

Figure 5-2 PCM timing, POS_MSB_WR/RD = 1

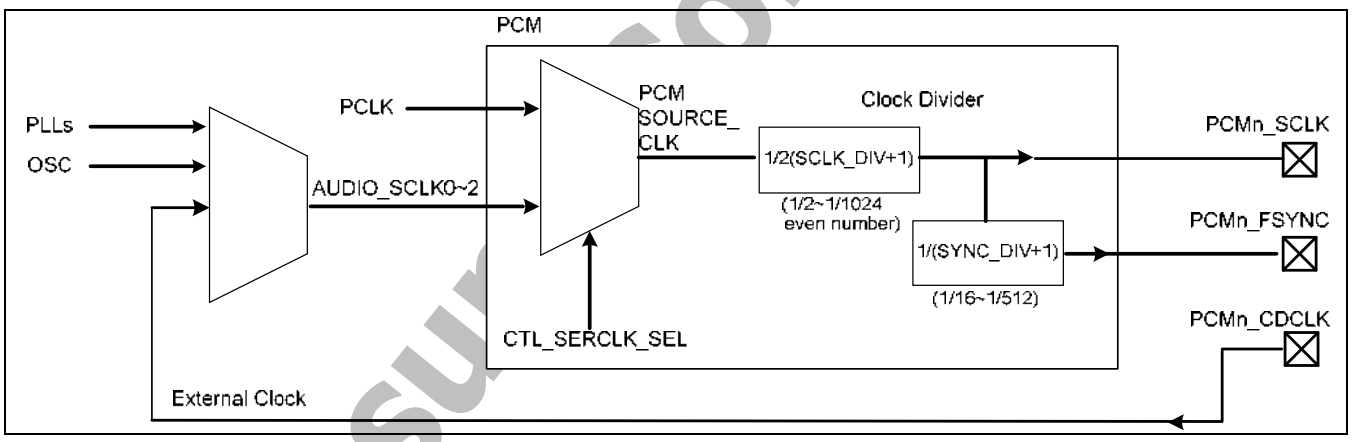

Figure 5-3 Input Clock Diagram for PCM

S5PV210 PCM can select clock either PCLK or External Clock. Refer *Figure 5-3*. To enable clock gating, please refer to the SYSCON part (SCLKCON, PCLKCON)

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5.5 I/O DESCRIPTION

Each PCM external pads are shared with I2S and PCM. In order to use these pads for I2S, GPIO must be set before the PCM started. For mode information, refer to the GPIO chapter of this manual for proper GPIO setting

PAD Name	I/O	Description	Pad	Type
Xi2s0CDCLK, Xi2s1CDCLK, Xpcm0EXTCLK	I/O	PCM Codec clock input/output		dedicated
Xi2s0SCLK, Xi2s1SCLK, Xpcm0SCLK	I/O	PCM Bit clock input/output		dedicated
Xi2s0LRCK, Xi2s1LRCK, Xpcm0FSYNC	I/O	PCM FSYNC channel clock input/output		dedicated
Xi2s0SDI, Xi2s1SDI, Xpcm0SIN	I	PCM serial data input		dedicated
Xi2s0SDO, Xi2s1SDO, Xpcm0SOUT	O	PCM serial data out		dedicated

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5.6 REGISTER DESCRIPTION

5.6.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
PCM0				
PCM_CTL	0xE230_0000	R/W	Specifies the PCM Main Control	0x00000000
PCM_CLKCTL	0xE230_0004	R/W	Specifies the PCM Clock and Shift control	0x00000000
PCM_TXFIFO	0xE230_0008	R/W	Specifies the PCM TXFIFO write port	0x00010000
PCM_RXFIFO	0xE230_000C	R/W	Specifies the PCM RXFIFO read port	0x00010000
PCM_IRQ_CTL	0xE230_0010	R/W	Specifies the PCM Interrupt Control	0x00000000
PCM_IRQ_STAT	0xE230_0014	R	Specifies the PCM Interrupt Status	0x00000000
PCM_FIFO_STAT	0xE230_0018	R	Specifies the PCM FIFO Status	0x00000000
PCM_CLRINT	0xE230_0020	W	Specifies the PCM Interrupt Clear	-
PCM1				
PCM_CTL	0xE120_0000	R/W	Specifies the PCM Main Control	0x00000000
PCM_CLKCTL	0xE120_0004	R/W	Specifies the PCM Clock and Shift control	0x00000000
PCM_TXFIFO	0xE120_0008	R/W	Specifies the PCM TXFIFO write port	0x00010000
PCM_RXFIFO	0xE120_000C	R/W	Specifies the PCM RXFIFO read port	0x00010000
PCM_IRQ_CTL	0xE120_0010	R/W	Specifies the PCM Interrupt Control	0x00000000
PCM_IRQ_STAT	0xE120_0014	R	Specifies the PCM Interrupt Status	0x00000000
PCM_FIFO_STAT	0xE120_0018	R	Specifies the PCM FIFO Status	0x00000000
PCM_CLRINT	0xE120_0020	W	Specifies the PCM Interrupt Clear	-
PCM2				
PCM_CTL	0xE2B0_0000	R/W	Specifies the PCM Main Control	0x00000000
PCM_CLKCTL	0xE2B0_0004	R/W	Specifies the PCM Clock and Shift control	0x00000000
PCM_TXFIFO	0xE2B0_0008	R/W	Specifies the PCM TXFIFO write port	0x00010000
PCM_RXFIFO	0xE2B0_000C	R/W	Specifies the PCM RXFIFO read port	0x00010000
PCM_IRQ_CTL	0xE2B0_0010	R/W	Specifies the PCM Interrupt Control	0x00000000
PCM_IRQ_STAT	0xE2B0_0014	R	Specifies the PCM Interrupt Status	0x00000000
PCM_FIFO_STAT	0xE2B0_0018	R	Specifies the PCM FIFO Status	0x00000000
PCM_CLRINT	0xE2B0_0020	W	Specifies the PCM Interrupt Clear	-

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5.6.1.1 PCM Control Register (PCM_CTL)

The PCM_CTL register is used to control the various aspects of the PCM module. It also provides a status bit for polling control instead of interrupt based control.

- PCM_CTL, R/W, Address = 0xE230_0000
- PCM_CTL, R/W, Address = 0xE120_0000
- PCM_CTL, R/W, Address = 0xE2B0_0000

The bit definitions for the PCM_CTL Control Register are described below:

PCM_CTL	Bit	Description	Initial State
Reserved	[31:19]	Reserved	
TXFIFO _DIPSTICK	[18:13]	Determines when the ALMOST_FULL, ALMOST_EMPTY flags go active for the TXFIFO ALMOST_EMPTY: FIFO_depth < FIFO_dipstick ALMOST_FULL: FIFO_depth > (32 – FIFO_dipstick) Note: if FIFO_dipstick == 0 ALMOST_EMPTY, ALMOST_FULL are invalid Note: for DMA loading of TX FIFO TXFIFO_dipstick >= 2 This is required since the PCM_TXDMA uses ALMOST_FULL as the DMA request (keep requesting data until the FIFO is almost full) In some circumstances, the DMA write one more word after the DMA_req fall to low. Thus the ALMOST_FULL flag most go active with at least space for one extra word in the FIFO	0
RXFIFO _DIPSTICK	[12:7]	Determines when the ALMOST_FULL, ALMOST_EMPTY flags go active for the RXFIFO ALMOST_EMPTY: FIFO_depth < FIFO_dipstick ALMOST_FULL: FIFO_depth > (32 – FIFO_dipstick) Note: if FIFO_dipstick == 0 ALMOST_EMPTY, ALMOST_FULL are invalid Note: for DMA, RXFIFO_DIPSTICK is a don't care DMA unloading of RX FIFO uses the RX_FIFO_EMPTY flag as the DMA request Note: non-DMA IRQ/polling RXFIFO_DIPSTICK should be 0x20 This will have the effect of RX_FIFO_ALMOST_FULL acting as an RX_FIFO_not_empty flag.	0
PCM_TX _DMA_EN	[6]	Enables the DMA interface for the TXFIFO DMA_TX request will occur whenever the TXFIFO is not almost full	0
PCM_RX _DMA_EN	[5]	Enables the DMA interface for the RXFIFO DMA_RX request will occur whenever the RXFIFO is not empty.	0

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PCM_CTL	Bit	Description	Initial State
TX_MSB _POS	[4]	Controls the position of the MSB bit in the serial output stream relative to the PCMSYNC signal 0 = MSB sent during the same clock that PCMSYNC is high 1 = MSB sent on the next PCMSCLK cycle after PCMSYNC is high	0
RX_MSB _POS	[3]	Controls the position of the MSB bit in the serial input stream relative to the PCMSYNC signal 0 = MSB is captured on the falling edge of PCMSCLK during the same cycle that PCMSYNC is high 1 = MSB is captured on the falling edge of PCMSCLK during the cycle after the PCMSYNC is high	0
PCM_TXFIFO _EN	[2]	Enables the TXFIFO When the enable is LOW the internal FIFOs will clear and reinitialize	0
PCM_RXFIFO _EN	[1]	Enables the RXFIFO When the enable is LOW the internal FIFOs will clear and reinitialize	0
PCM_PCM _ENABLE	[0]	PCM enable signal. Enables the serial shift state machines. The enable must be set HIGH for the PCM to operate. When the enable is LOW, the PCM outputs will not toggle (PCMSCLK, PCMSYNC, and PCMSOUT). Additionally when the enable is LOW, the internal divider-counters are held in reset.	0

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5.6.1.2 PCM CLK Control Register (PCM_CLKCTL)

- PCM_CLKCTL, R/W, Address = 0xE230_0004
- PCM_CLKCTL, R/W, Address = 0xE120_0004
- PCM_CLKCTL, R/W, Address = 0xE2B0_0004

The bit definitions for the PCM_CTL Control Register are described below:

PCM_CLKCTL	Bit	Description	Initial State
Reserved	[31:20]	Reserved	0
CTL_SERCLK_EN	[19]	Enables the serial clock division logic. Must be HIGH for the PCM to operate	0
CTL_SERCLK_SEL	[18]	Selects the source of the serial clock 0 = SCLK_AUDIO0,1,2(PCM0, PCM1, PCM2) 1 = PCLK	0
SCLK_DIV	[17:9]	Controls the divider used to create the PCMSCLK based on the PCMCODEC_CLK Final clock will be source_clk / 2*(sclk_div+1)	000
SYNC_DIV	[8:0]	Controls the frequency of the PCMSYNC signal based on the PCMSCLK.	000

5.6.1.3 The PCM Tx FIFO Register (PCM_TXFIFO)

- PCM_TXFIFO, R/W, Address = 0xE230_0008
- PCM_TXFIFO, R/W, Address = 0xE120_0008
- PCM_TXFIFO, R/W, Address = 0xE2B0_0008

The bit definitions for the PCM_TXFIFO Register are described below:

PCM_TXFIFO	Bit	Description	Initial State
Reserved	[31:17]	Reserved	0
TXFIFO_DVALID	[16]	TXFIFO data is valid Write: Not valid Read: TXFIFO read data valid 1 = Valid 0 = Invalid (probably read an empty FIFO)	1
TXFIFO_DATA	[15:0]	TXFIFO DATA Write: TXFIFO_DATA is written into the TXFIFO Read: TXFIFO is read using the APB interface Note: reading the TXFIFO is meant to support debugging. Online the TXFIFO is read by the PCM serial shift engine, not the APB	0

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5.6.1.4 PCM RX FIFO Register (PCM_RXFIFO)

- PCM_RXFIFO, R/W, Address = 0xE230_000C
- PCM_RXFIFO, R/W, Address = 0xE120_000C
- PCM_RXFIFO, R/W, Address = 0xE2B0_000C

The bit definitions for the PCM_RXFIFO Register are described below:

PCM_RXFIFO	Bit	Description	Initial State
Reserved	[31:17]	Reserved	0
RXFIFO_DVALID	[16]	RXFIFO data is valid Write: Not Valid Read: TXFIFO read data valid 1 = Valid 0 = Invalid (probably read an empty FIFO)	1
RXFIFO_DATA	[15:0]	RXFIFO DATA Write: RXFIFO_DATA is written into the RXFIFO Note: writing the RXFIFO is meant to support debugging. Online the RXFIFO is written by the PCM serial shift engine, not the APB Read: TXFIFO is read using the APB interface	0

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5.6.1.5 PCM Interrupt Control Register (PCM_IRQ_CTL)

The PCM_IRQ_CTL register is used to control the various aspects of the PCM interrupts.

- PCM_IRQ_CTL, R/W, Address = 0xE230_0010
- PCM_IRQ_CTL, R/W, Address = 0xE120_0010
- PCM_IRQ_CTL, R/W, Address = 0xE2B0_0010

The bit definitions for the PCM_IRQ_CTL Control Register are described below:

PCM_IRQ_CTL	Bit	Description	Initial State
Reserved	[31:15]	Reserved	0
EN_IRQ_TO _ARM	[14]	Controls whether or not the PCM interrupt is sent to the ARM 1 = PCM IRQ is forwarded to the ARM subsystem 0 = PCM IRQ is NOT forwarded to the ARM subsystem	0
Reserved	[13]	Reserved	0
TRANSFER _DONE	[12]	Interrupt is generated every time the serial shift for a word completes 1 = IRQ source enabled 0 = IRQ source disabled	0
TXFIFO_EMPTY	[11]	Interrupt is generated whenever the TxFIFO is empty 1 = IRQ source enabled 0 = IRQ source disabled	0
TXFIFO_ALMOST _EMPTY	[10]	Interrupt is generated whenever the TxFIFO is ALMOST empty. Almost empty is defined as TX_FIFO_DEPTH < TX_FIFO_DIPSTICK 1 = IRQ source enabled 0 = IRQ source disabled	0
TXFIFO_FULL	[9]	Interrupt is generated whenever the TxFIFO is full 1 = IRQ source enabled 0 = IRQ source disabled	0
TXFIFO_ALMOST _FULL	[8]	Interrupt is generated whenever the TxFIFO is ALMOST full. Almost full is defined as TX_FIFO_DEPTH > (32– TX_FIFO_DIPSTICK) 1 = IRQ source enabled 0 = IRQ source disabled	0
TXFIFO_ERROR _STARVE	[7]	Interrupt is generated for TxFIFO starve ERROR. This occurs whenever the TxFIFO is read when it is still empty. This is considered as an ERROR and will have unexpected results 1 = IRQ source enabled 0 = IRQ source disabled	0

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PCM_IRQ_CTL	Bit	Description	Initial State
TXFIFO_ERROR _OVERFLOW	[6]	Interrupt is generated for TxFIFO overflow ERROR. This occurs whenever the TxFIFO is written when it is already full. This is considered as an ERROR and will have unexpected results 1 = IRQ source enabled 0 = IRQ source disabled	0
RXFIFO_EMPTY	[5]	Interrupt is generated whenever the RXFIFO is empty 1 = IRQ source enabled 0 = IRQ source disabled	0
RXFIFO_ALMOST _EMPTY	[4]	Interrupt is generated whenever the RXFIFO is ALMOST empty. Almost empty is defined as RX_FIFO_DEPTH < RX_FIFO_DIPSTICK 1 = IRQ source enabled 0 = IRQ source disabled	0
RX_FIFO_FULL	[3]	Interrupt is generated whenever the RXFIFO is full 1 = IRQ source enabled 0 = IRQ source disabled	0
RX_FIFO _ALMOST _FULL	[2]	Interrupt is generated whenever the RXFIFO is ALMOST full. Almost full is defined as RX_FIFO_DEPTH > (32– RX_FIFO_DIPSTICK) 1 = IRQ source enabled 0 = IRQ source disabled	0
RXFIFO_ERROR _STARVE	[1]	Interrupt is generated for RXFIFO starve ERROR. This occurs whenever the RXFIFO is read when it is still empty. This is considered as an ERROR and will have unexpected results 1 = IRQ source enabled 0 = IRQ source disabled	0
RXFIFO_ERROR _OVERFLOW	[0]	Interrupt is generated for RXFIFO overflow ERROR. This occurs whenever the RXFIFO is written when it is already full. This is considered as an ERROR and will have unexpected results 1 = IRQ source enabled 0 = IRQ source disabled	0

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5.6.1.6 PCM Interrupt Status Register (PCM_IRQ_STAT)

The PCM_IRQ_STAT register is used to report IRQ status.

- PCM_IRQ_STAT, R, Address = 0xE230_0014
- PCM_IRQ_STAT, R, Address = 0xE120_0014
- PCM_IRQ_STAT, R, Address = 0xE2B0_0014

The bit definitions for the PCM_IRQ_STATUS Register are described below:

PCM_IRQ_STAT	Bit	Description	Initial State
Reserved	[31:14]	Reserved	0
IRQ_PENDING	[13]	Monitoring PCM IRQ. 1 = PCM IRQ is occurred. 0 = PCM IRQ is not occurred.	0
TRANSFER_DONE	[12]	Interrupt is generated every time the serial shift for a word completes 1 = IRQ is occurred. 0 = IRQ is not occurred.	0
TXFIFO_EMPTY	[11]	Interrupt is generated whenever the TX FIFO is empty 1 = IRQ is occurred. 0 = IRQ is not occurred.	0
TXFIFO_ALMOST_EMPTY	[10]	Interrupt is generated whenever the TxFIFO is ALMOST empty. 1 = IRQ is occurred. 0 = IRQ is not occurred.	0
TXFIFO_FULL	[9]	Interrupt is generated whenever the TX FIFO is full 1 = IRQ is occurred. 0 = IRQ is not occurred.	0
TXFIFO_ALMOST_FULL	[8]	Interrupt is generated whenever the TX FIFO is ALMOST full. 1 = IRQ is occurred. 0 = IRQ is not occurred.	0
TXFIFO_ERROR_STARVE	[7]	Interrupt is generated for TX FIFO starve ERROR. This occurs whenever the TX FIFO is read when it is still empty. This is considered as an ERROR and will have unexpected results 1 = IRQ is occurred. 0 = IRQ is not occurred.	0
TXFIFO_ERROR_OVERFLOW	[6]	Interrupt is generated for TX FIFO overflow ERROR. This occurs whenever the TX FIFO is written when it is already full. This is considered as an ERROR and will have unexpected results 1 = IRQ is occurred. 0 = IRQ is not occurred.	0
RXFIFO_EMPTY	[5]	Interrupt is generated whenever the RX FIFO is empty	0

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PCM_IRQ_STAT	Bit	Description	Initial State
		1 = IRQ is occurred. 0 = IRQ is not occurred.	
RXFIFO_ALMOST_EMPTY	[4]	Interrupt is generated whenever the RX FIFO is ALMOST empty. 1 = IRQ is occurred. 0 = IRQ is not occurred.	0
RX_FIFO_FULL	[3]	Interrupt is generated whenever the RX FIFO is full 1 = IRQ is occurred. 0 = IRQ is not occurred.	0
RX_FIFO_ALMOST_FULL	[2]	Interrupt is generated whenever the RX FIFO is ALMOST full. 1 = IRQ is occurred. 0 = IRQ is not occurred.	0
RXFIFO_ERROR_STARVE	[1]	Interrupt is generated for RX FIFO starve ERROR. This occurs whenever the RX FIFO is read when it is still empty. This is considered as an ERROR and will have unexpected results 1 = IRQ is occurred. 0 = IRQ is not occurred.	0
RXFIFO_ERROR_OVERFLOW	[0]	Interrupt is generated for RX FIFO overflow ERROR. This occurs whenever the RX FIFO is written when it is already full. This is considered as an ERROR and will have unexpected results 1 = IRQ is occurred. 0 = IRQ is not occurred.	0

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5.6.1.7 PCM FIFO Status Register (PCM_FIFO_STAT)

The PCM_FIFO_STAT register is used to report FIFO status.

- PCM_FIFO_STAT, R, Address = 0xE230_0018
- PCM_FIFO_STAT, R, Address = 0xE120_0018
- PCM_FIFO_STAT, R, Address = 0xE2B0_0018

The bit definitions for the PCM_IRQ_STATUS Register are described below:

PCM_FIFO_STAT	Bit	Description	Initial State
Reserved	[31:20]	Reserved	0
TXFIFO_COUNT	[19:14]	TXFIFO data count (0~32).	0
TXFIFO_EMPTY	[13]	To indicate whether TXFIFO is empty.	0
TXFIFO_ALMOST_EMPTY	[12]	To indicate whether TXFIFO is almost empty.	0
TXFIFO_FULL	[11]	To indicate whether TXFIFO is full.	0
TXFIFO_ALMOST_FULL	[10]	To indicate whether TXFIFO is almost full.	0
RXFIFO_COUNT	[9:4]	RXFIFO data count (0~32).	0
RXFIFO_EMPTY	[3]	To indicate whether RXFIFO is empty.	0
RXFIFO_ALMOST_EMPTY	[2]	To indicate whether RXFIFO is almost empty.	0
RX_FIFO_FULL	[1]	To indicate whether RXFIFO is full.	0
RX_FIFO_ALMOST_FULL	[0]	To indicate whether RXFIFO is almost full.	0

5.6.1.8 PCM Interrupt Clear Register (PCM_CLRINT)

The PCM_CLRINT register is used to clear the interrupt. Interrupt service routine is responsible for clearing interrupt asserted. Writing any values on this register clears interrupts for both ARM and DSP. Reading this register is not allowed. Clearing interrupt must be prior to resolving the interrupt condition; else, another interrupt that would occur after this interrupt may be ignored.

- PCM_CLRINT, W, Address = 0xE230_0020
- PCM_CLRINT, W, Address = 0xE120_0020
- PCM_CLRINT, W, Address = 0xE2B0_0020

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6 SPDIF TRANSMITTER

6.1 OVERVIEW OF SPDIF TRANSMITTER

SPDIF transmitter is based on IEC60958. This chapter describes a serial, un-directional, self-clocking interface to interconnect digital audio equipment in consumer and professional applications. If you use a consumer digital processing environment in SPDIF standard, the SPDIF interface is primarily intended to carry stereophonic programs, with a resolution of up to 20 bits per sample, an extension to 24 bits per sample being possible. If you use SPDIF in a broadcasting studio environment, the interface is primarily intended to carry monophonic or stereophonic programs, at a 48 kHz sampling frequency and with a resolution of up to 24 bits per sample; it can carry one or two signals sampled at 32 kHz.

In both cases, the clock references and auxiliary information are transmitted with the program. Provision in IEC60958 is made to allow the interface to carry software related data.

6.2 KEY FEATURES OF SPDIF TRANSMITTER

- SPDIFOUT module only supports the consumer application in S5PV210
- Supports linear PCM up to 24-bit per sample
- Supports Non-linear PCM formats such as AC3, MPEG1 and MPEG2
- 2 x 24-bit buffers which is alternately filled with data

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6.3 BLOCK DIAGRAM OF SPDIF TRANSMITTER

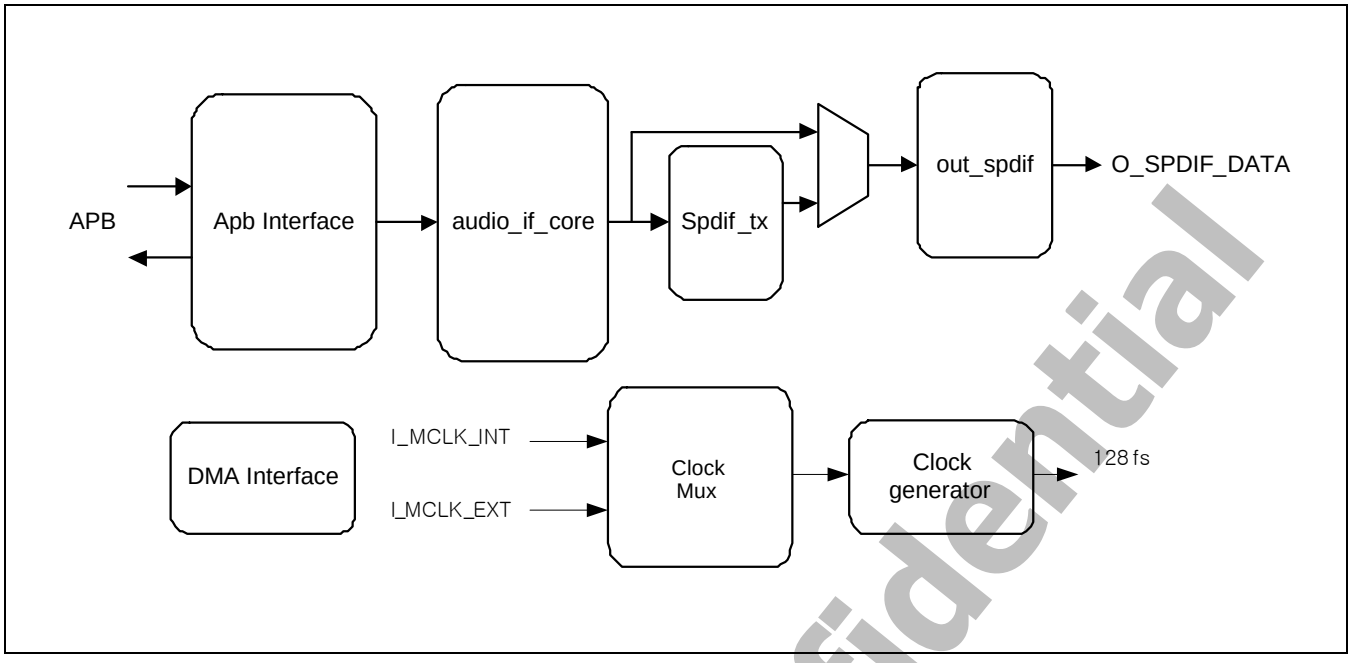

Figure 6-1 Block Diagram of SPDIFOUT

Components in SPDIF Transmitter:

- APB interface block: This block defines register banks to control the driving of SPDIFOUT module and data buffers to store linear or non-linear PCM data.
- DMA interface block: This block requests DMA service to IODMA depending on the status of data buffer in APB Interface block
- Clock Generator block: This block generates 128fs (sampling frequency) clock used in out_spdif block from system audio clock (MCLK)
- Clock Multiplex block: system audio clock (MCLK) can be selected as internal MCLK or external MCLK.
- Audio_if_core block: This block acts as interface block between data buffer and out_spdif block. Finite-state machine controls the flow of PCM data.
- spdif_tx block: This block inserts burst preamble and executes zero-stuffing in the nonlinear PCM stream. Linear PCM data are bypassed by spdif_tx module.
- out_spdif block: This block generates SPDIF format. It inserts 4-bit preamble, 16- or 20- or 24-bit data, user-data bit, validity bit, channel status bit and parity bit into the appropriate position of 32-bit word. It modulates each bit to bi-phase format.

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6.4 FUNCTIONAL DESCRIPTIONS

6.4.1 DATA FORMAT OF SPDIF

6.4.1.1 Frame Format

A frame is uniquely composed of two sub-frames. The transmission rate of frames corresponds exactly to the source sampling frequency.

In the 2-channel operation mode, the time multiplexing transmits samples taken from both channels in consecutive sub-frames. Sub-frames related to channel 1(left or "A" channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However, the preamble is changed to preamble B once every 192 frame. This unit composed of 192 frames defines the block structure used to organize the channel status information. Sub-frames of channel 2(right or "B" in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

In the single channel operation mode in broadcasting studio environment the frame format is identical to the 2-channel mode. Data is carried only in channel 1. In the sub-frames allocated to channel 2, time slot 28 (validity flag) should be set to logical "1" ("1" means not valid).

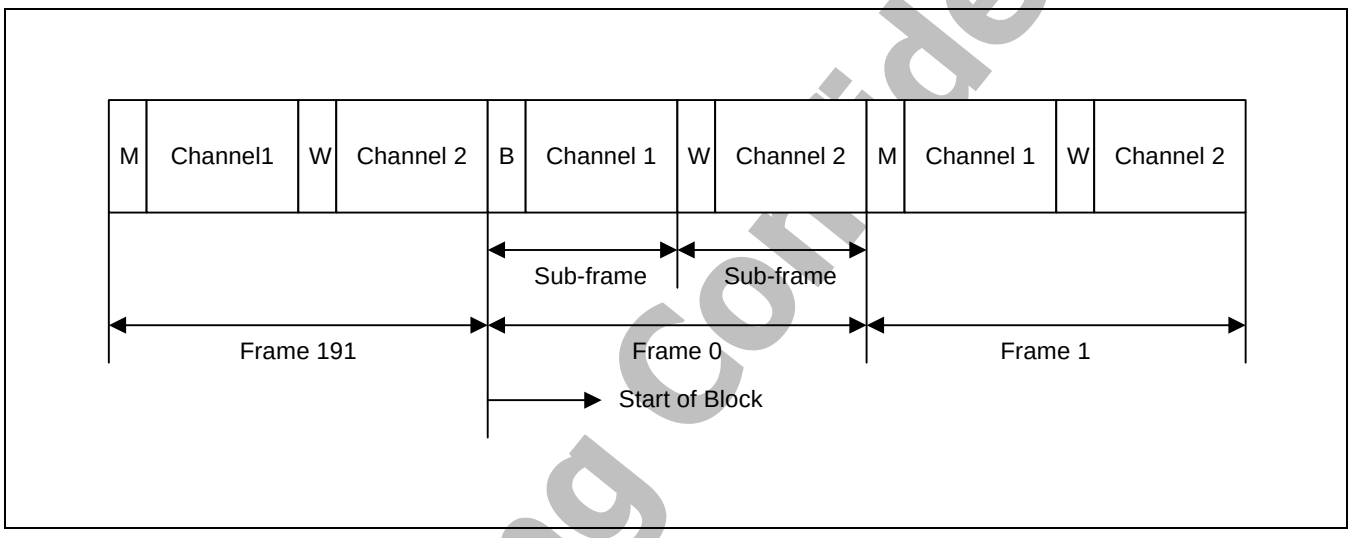

Figure 6-2 SPDIF Frame Format

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6.4.1.2 Sub-frame Format (IEC 60958)

Each sub-frame is divided into 32 time slot, numbered from 0 to 31. Time slot 0 to 3 carries one of the three permitted preambles. These are used to affect synchronization of sub-frames, frames and blocks. Time slots 4 to 27 carry the audio sample word in linear 2's complement representation. The most significant bit is carried by time slot 27. When a 24-bit coding range is used, the least significant bit is in time slot 4. When a 20-bit coding range is sufficient, the least significant bit is in time slot 8 and time slot 4 to 7 may be used for other application. Under these circumstances, the bits in the time slot 4 to 7 are designated auxiliary sample bits.

If the source provides fewer bits than the interface allows (24 or 20), the unused least significant bits shall be set to a logical "0". This procedure supports to connect equipment using different numbers of bits. Time slot 28 carries the validity flag associated with the audio sample word. This flag is set to logical "0" if the audio sample is reliable. Time slot 29 carries one bit of the user data associated with the audio channel transmitted in the same sub-frame. The default value of the user bit is logical "0". Time slot 30 carries one bit of the channel status words associated with the audio channel transmitted in the same sub-frame. Time slot 31 carries a parity bit such that time slots 4 to 31 inclusive will carry an even number of ones and an even number of zeros.

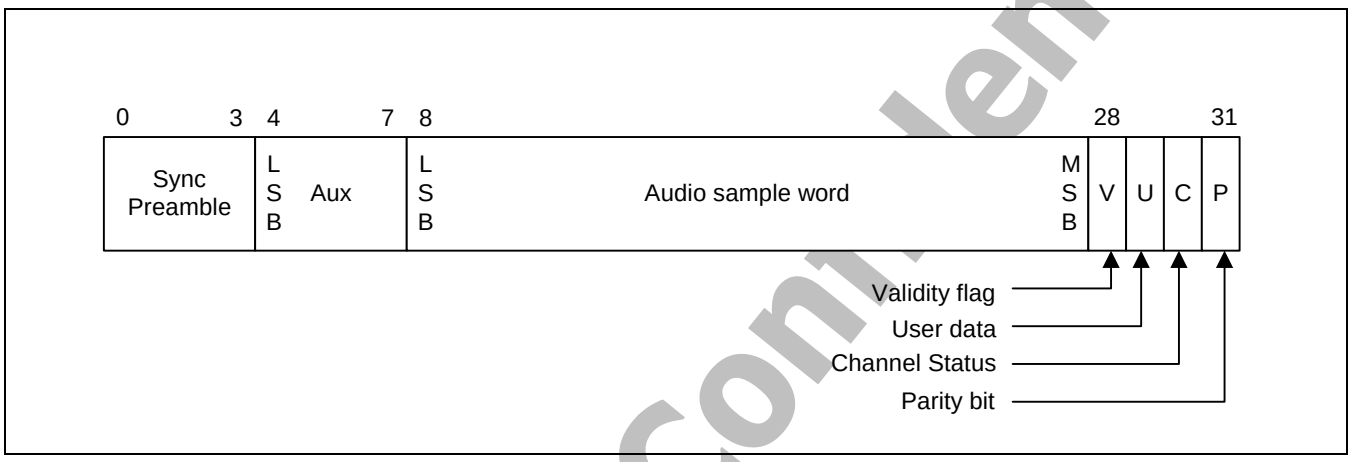

Figure 6-3 SPDIF Sub-frame Format

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6.4.2 CHANNEL CODING

To minimize the dc component on the transmission line, to facilitate clock recovery from the data stream and to make the interface insensitive to the polarity of connections, time slots 4 to 31 are encoded in biphase-mark. A symbol comprising two consecutive binary states represent each bit to be transmitted. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logical "0", is different from the first if the bit is logical "1".

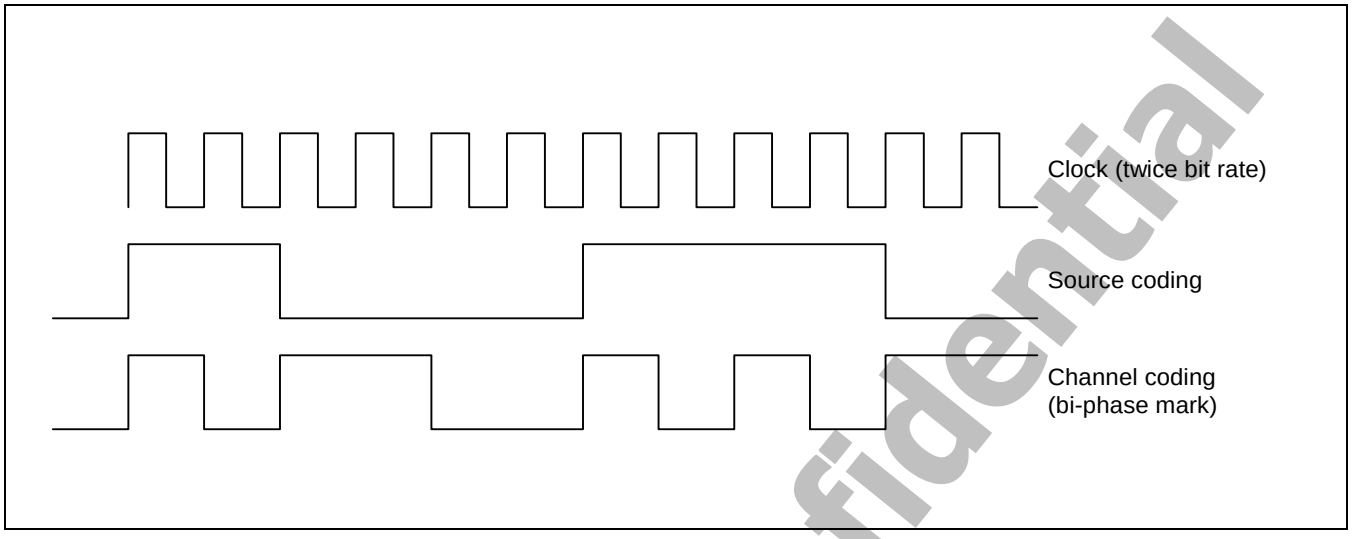

Figure 6-4 Channel Coding

6.4.3 PREAMBLE

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks. A set of three preambles (M, B and W) is used. These preambles are transmitted in the time allocated to four time slots (time slots 0 to 3) and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol.
Similar to bi-phase code, these preambles are dc free and provide clock recovery. They differ in minimum two states from any valid bi-phase sequence.

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6.4.4 NON-LINEAR PCM ENCODED SOURCE (IEC 61937)

The non-linear PCM encoded audio bit stream is transferred using the basic 16-bit data area of the IEC 60958 sub frames, that is, in time slots 12 to 27. Each IEC 60958 frame can transfer 32 bits of the non-PCM data in consumer application mode.

When the SPDIF bit stream conveys linear PCM audio, the symbol frequency is 64 times the PCM sampling frequency (32 time slots per PCM sample time's two channels). When a non-linear PCM encoded audio bit stream is transmitted by the interface, the symbol frequency shall be 64 times the sampling rate of the encoded audio within that bit stream. If a non-linear PCM encoded audio bit stream is transmitted by the interface containing audio with low sampling frequency, the symbol frequency shall be 128 times the sampling rate of the encoded audio within that bit stream.

Each data burst contains a burst-preamble consisting of four 16-bit words (Pa, Pb, Pc, Pd), followed by the burst-payload which contains data of an encoded audio frame.
The burst-preamble consists of four mandatory fields. Pa and Pb represent a synchronization word; Pc gives information about the type of data and some information/control for the receiver; Pd gives the length of the burst-payload, limited to 216(=65,535) bits.
The four preamble words are contained in two sequential SPDIF frames. The frame beginning the data-burst contains preamble word Pa in subframe 1 and Pb in subframe 2. The next frame contains Pc in subframe 1 and Pd in subframe 2. When placed into a SPDIF subframe, the MSB of a 16-bit burst-preamble is placed into time slot 27 and the LSB is placed into time slot 12.

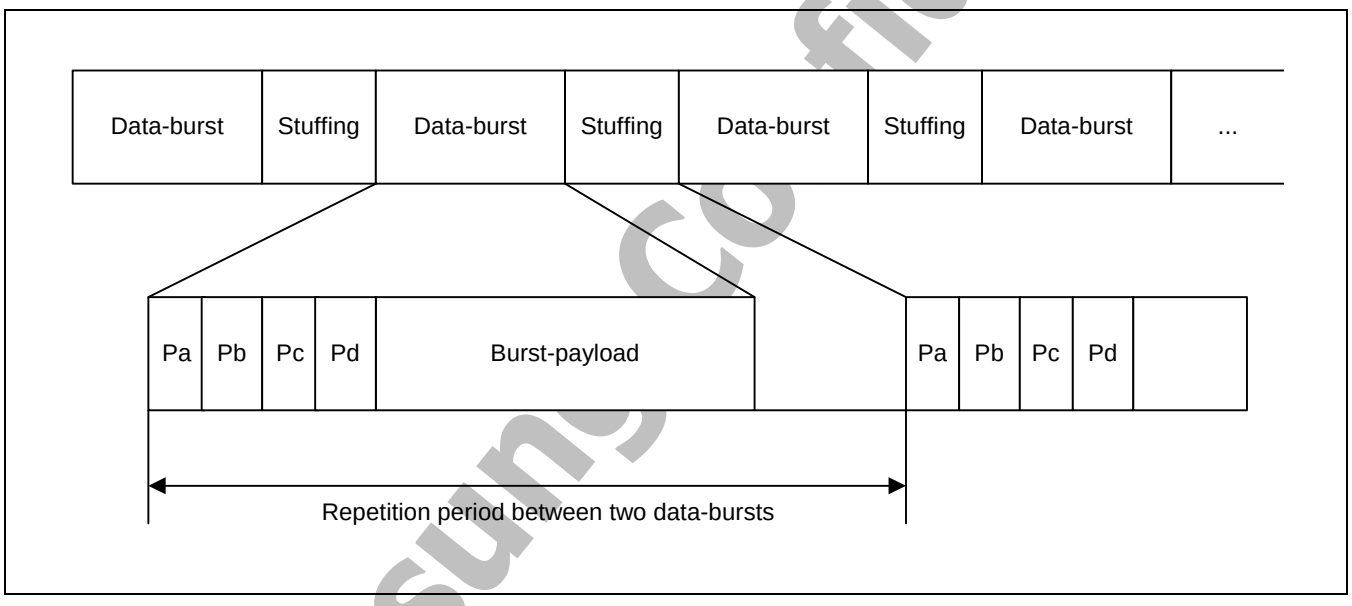

Figure 6-5 Format of Burst Payload

Table 6-1 Burst Preamble Words

Preamble word	Length of field	Contents	Value MSB.. LSB
Pa	16 bits	Sync word 1	0xF872
Pb	16 bits	Sync word 2	0x4E1F
Pc	16 bits	Burst-info	Refer to SPDBSTAS_SHD[15:0]
Pd	16 bits	Length-code	Refer to SPDBSTAS_SHD[31:16]

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6.4.5 SPDIF OPERATION

Since the bit frequency of SPDIF is 128fs (fs: sampling frequency), divide audio main clock (MCLK) depending on the frequency of MCLK to make the main clock of SPDIF. MCLK is divided by 2 in case of 256fs, by 3 in case of 384fs and by 4 in case of 512fs.

SPDIF module in S5PV210 changes the audio sample data format to SPDIF. To change the format, SPDIF module inserts preamble data, channel status data, user data, error check bit and parity bit into the appropriate time slots. Preamble data are fixed in the module and inserted depending on subframe counter. Channel status data are set in the SPDCSTAS register and used by one bit per frame. User data always have zero values.

For non-linear PCM data, insert burst-preamble, which consists of Pa, Pb, Pc and Pd, before burst-payload and zero is padded from the end of burst-payload to the repetition count. Pa(=16'hF872) and Pb(=16'h4E1F) is fixed in the module and Pc and Pd is set in the register SPDBSTAS. To stuff zero, the end of burst-payload is calculated from Pd value and repetition count which depends on data type in the preamble Pc is acquired from register SPDCNT.

Audio data are justified to the LSB. 16-, 20- or 24-bit PCM data and 16-bit stream data are supported. The unoccupied upper bits of 32-bit word are ignored.

Data are fetched via DMA request. If one of two data buffers is empty, DMA service is requested. Audio data stored in the data buffers are transformed into SPDIF format and output to the port. For non-linear PCM data, interrupt is generated after audio data are output up to the value specified in the SPDCNT register. Interrupt sets the registers such as SPDBSTAS and SPDCNT to new values, if data type of new bitstream is different from the previous one.

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6.4.6 SHADOWED REGISTER

Both SPDBSTAS_SHD register and SPDCNT_SHD register are shadowed registers which are related to SPDBSTAS register and SPDCNT register, respectively. They are updated from related registers at every stream end interrupt signal. The usage of shadowed register is as follows.

1. Set burst status and repetition count information to their respective registers.
2. Turn on SPDIF module, and stream end interrupt is asserted immediately.
3. With stream end interrupt, shadowed registers are updated from their related registers and SPDIF starts to transfer data. Now next stream information (burst status and repetition count) can be written to SPDBSTAS and SPDCNT register because previous information is copied to their respective shadowed registers.
4. Set next stream information to SPDBSTAS and SPDCNT register.
5. Wait for stream end interrupt which signals the end of the first stream.
6. With stream end interrupt, the 2nd stream data will start to transfer. Set 3rd stream information to registers.

The usage of user bit registers is similar to stream information registers except that they are not related to SPDIF end interrupt but to user data interrupt. As soon as SPDIF is on, shadowed user bit registers are updated from their related registers and user bit starts to be shifted out with user data interrupt asserted. User can write the next user data to registers with this interrupt. After entire 96 user bits are shifted out, user data interrupt will be asserted again and 3rd user bits can be written to registers with 2nd user bits going out.

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6.5 I/O DESCRIPTION

SPDIF external pads are shared with I2S and PCM. In order to use these pads for SPDIF, GPIO must be set before the SPDIF starts. For more information, refer to the GPIO chapter of this manual for exact GPIO setting

Signal	I/O	Description	Pad	Type
I_MLCK_EXT	I	Global audio main clock (External MCLK)	Xpcm0EXTCLK	muxed
O_SPDIF_DATA	O	SPDIFOUT data output	Xpcm0SCLK	muxed

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6.6 REGISTER DESCRIPTION

6.6.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
SPDCLKCON	0xE110_0000	R/W	Specifies the Clock control register	0x0000_0002
SPDCON	0xE110_0004	R/W	Specifies the Control register	0x0000_0000
SPDBSTAS	0xE110_0008	R/W	Specifies the Burst status register	0x0000_0000
SPDCSTAS	0xE110_000C	R/W	Specifies the Channel status register	0x0000_0000
SPDDAT	0xE110_0010	W	Specifies the SPDIFOUT data buffer	0x0000_0000
SPDCNT	0XE110_0014	R/W	Specifies the Repetition count register	0x0000_0000
SPDBSTAS_SHD	0XE110_0018	R	Specifies the Shadowed Burst Status Register	0x0000_0000
SPDCNT_SHD	0XE110_001C	R	Specifies the Shadowed Repetition Count Register	0x0000_0000
USERBIT1	0XE110_0020	R/W	Specifies the Subcode Q1 ~ Q32	0x0000_0000
USERBIT2	0XE110_0024	R/W	Specifies the Subcode Q33 ~ Q64	0x0000_0000
USERBIT3	0XE110_0028	R/W	Specifies the Subcode Q65 ~ Q96	0x0000_0000
USERBIT1_SHD	0XE110_002C	R	Specifies the Shadowed Register Userbit1	0x0000_0000
USERBIT2_SHD	0XE110_0030	R	Specifies the Shadowed Register Userbit2	0x0000_0000
USERBIT3_SHD	0XE110_0034	R	Specifies the Shadowed Register Userbit3	0x0000_0000
VERSION_INFO	0XE110_0038	R	Specifies the RTL Version Information	0x0000_000C

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6.6.1.1 SPDIFOUT Clock Control Register (SPDCLKCON, R/W, Address = 0XE110_0000)

SPDCLKCON	Bit	Description	Initial State
-	[31:3]	Reserved	0
Main Audio Clock Selection	[2]	0 = Internal clock (I_MCLK_INT) 1 = External clock (I_MCLK_EXT)	0
SPDIFOUT clock down ready (read only)	[1]	0 = Clock-down not ready 1 = Clock-down ready	1
SPDIFOUT power on	[0]	0 = Power off 1 = Power on	0

6.6.1.2 SPDIFOUT Control Register (SPDCON, R/W, Address = 0XE110_0004)

SPDCON	Bit	Description	Initial State
-	[31:27]	Reserved	0
FIFO Level	[26:22]	FIFO Level Monitoring (Read Only) FIFO depth is 16 *0 = Empty of FIFO Level, 16 = Full of FIFO Level	00000
FIFO Level Threshold	[21:19]	FIFO Threshold Level is controllable 000 = 0-FIFO Level 001 = 1-FIFO Level 010 = 4-FIFO Level 011 = 6-FIFO Level 100 = 10-FIFO Level 101 = 12-FIFO Level 110 = 14-FIFO Level 111 = 15-FIFO Level	000
FIFO transfer mode	[18:17]	00 = DMA transfer mode 01 = Polling mode 10 = Interrupt mode 11 = Reserved	00
FIFO_level Interrupt Status	[16]	Read Operation 0 = No interrupt pending. 1 = Interrupt pending. Write Operation 0 = No effect. 1 = Clear this flag.	0
FIFO_level Interrupt Enable	[15]	0 = Interrupt masked 1 = Interrupt enable	0
endian format	[14:13]	00 = big endian o_data = {in_data[23:0]} 01 = 4 byte swap o_data={in_data[15:8], in_data[23:16], in_data[31:24]}	0

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SPDCON	Bit	Description	Initial State
		10 = 3 byte swap o_data={in_data[7:0], in_data[15:8], in_data[23:16]} 11 = 2 byte swap o_data={0x00,in_data[7:0], in_data[15:8]} *in_data: BUS → in port of SPDIF o_data: in port of SPDIF → Logic	
user_data_attach	[12]	0 = User data is stored in USERBIT register. User data of subframe is out from USERBIT1,2,3 (96-bit) 1 = User data is stored in 23rd bit of audio data. User data is out in PCM data's 23th bit.	0
User Data Interrupt Status	[11]	Read Operation 0 = No interrupt pending. 1 = Interrupt pending when 96-bit of user data is out. Write Operation 0 = No effect. 1 = Clear this flag.	0
User Data Interrupt Enable	[10]	0 = Interrupt masked 1 = Interrupt enable	0
Buffer Empty Interrupt Status	[9]	Read Operation 0 = No interrupt pending. 1 = Interrupt pending. Write Operation 0 = No effect. 1 = Clear this flag.	0
Buffer Empty Interrupt Enable	[8]	0 = Interrupt masked 1 = Interrupt enable	0
Stream End Interrupt Status	[7]	Read Operation 0 = No interrupt pending. 1 = Interrupt pending when the number of output audio data reaches repetition count in SPDCNT register. Write Operation 0 = No effect. 1 = Clear this flag.	0
Stream End Interrupt Enable	[6]	0 = Interrupt masked 1 = Interrupt enable	0
software reset	[5]	0 = Normal operation 1 = Software reset Software reset is 1-cycle pulse (auto clear) Enable I_MCLK before software reset assertion because SPDIF uses synchronous reset	0
Main Audio Clock Frequency	[4:3]	00 = 256fs 01 = 384fs 10 = 512fs	0

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SPDCON	Bit	Description	Initial State
		11 = Reserved If you want to use SPDIF on HDMI, 512fs should be selected. Because HDMI in S5PV210 accepts only 512fs or more frequency.	
PCM Data Size	[2:1]	00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = Reserved	0
PCM or Stream	[0]	0 = Stream 1 = PCM	0

6.6.1.3 SPDIFOUT Burst Status Register (SPDBSTAS, R/W, Address = 0XE110_0008)

SPDBSTAS	Bit	Description	Initial State
Burst data length bit	[31:16]	ES size in bits (Burst Preamble Pd) ES size: Elementary Stream size This indicates Burst-payload length	0
Bitstream number	[15:13]	Bit_stream_number, shall be set to 0	0
Data type dependent info	[12:8]	Data type dependent information	0
Error flag	[7]	0 = Error flag indicates a valid burst_payload 1 = Error flag indicates that the burst payload may contain errors	0
-	[6:5]	Reserved	0
Compressed data type	[4:0]	00000 = Null Data 00001 = AC-3 00010 = Reserved 00011 = Pause 00100 = MPEG1 (layer1) 00101 = MPEG1 (layer2, 3), MPEG2-bc 00110 = MPEG2 – extension 00111 = Reserved 01000 = MPEG2 (layer1 – lsf) 01001 = MPEG2 (layer2, layer3 – lsf) Others = Reserved	0

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6.6.1.4 SPDIFOUT Channel Status Register (SPDCSTAS, R/W, Address = 0XE110_000C)

SPDCSTAS	Bit	Description	Initial State
-	[31:30]	Reserved	0
Clock accuracy	[29:28]	10 = Level I, ±50 ppm 00 = Level II, ±1000 ppm 01 = Level III, variable pitch shifted	0
Sampling frequency	[27:24]	0000 = 44.1 kHz 0010 = 48 kHz 0011 = 32 kHz 1010 = 96 kHz	0
Channel number	[23:20]	Bit 20 is LSB	0
Source number	[19:16]	Bit 16 is LSB	0
Category code	[15:8]	Equipment type CD player = 0000_0001 DAT player = L000_0011 DCC player = L100_0011 Mini disc = L100_1001 (L: information about generation status of the material)	0
Channel status mode	[7:6]	00 = Mode 0 Others = Reserved	0
Emphasis	[5:3]	When bit1 = 0, 000 = 2 audio channels without pre-emphasis 001 = 2 audio channels with 50us / 15us pre-emphasis When bit1 = 1, 000 = default state	0
Copyright assertion	[2]	0 = Copyright 1 = No copyright	0
Audio sample word	[1]	0 = Linear PCM 1 = Non-linear PCM	0
Channel status block	[0]	0 = Consumer format 1 = Professional format	0

6.6.1.5 SPDIFOUT Data Buffer (SPDDAT, W, Address = 0XE110_0010)

SPDDAT	Bit	Description	Initial State
-	[31:24]	Reserved	0
SPDIFOUT data	[23:0]	PCM or stream data	0

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6.6.1.6 SPDIFOUT Repetition Count Register (SPDCNT, R/W, Address = 0XE110_0014)

SPDCNT	Bit	Description	Initial State
-	[31:13]	Reserved	0
Stream repetition count	[12:0]	Repetition count according to data type. This bit is valid only for stream data.	0

6.6.1.7 Shadowed SPDIF Burst Status Register (SPDBSTAS_SHD, R, Address = 0XE110_0018)

SPDBSTAS	Bit	Description	Initial State
Burst Data Length Bit	[31:16]	ES size in bits (Burst Preamble Pd) ES size: Elementary Stream size This indicates Burst-payload length	0
Bitstream number	[15:13]	Bit_stream_number, shall be set to 0	0
Data Type Dependent Info	[12:8]	Data type dependent information	0
Error Flag	[7]	0 = Error flag indicating a valid burst_payload 1 = Error flag indicating that the burst payload may contain errors	0
-	[6:5]	Reserved	0
Compressed Data Type	[4:0]	00000 = Null Data 00001 = AC-3 00010 = Reserved 00011 = Pause 00100 = MPEG1 (layer1) 00101 = MPEG1 (layer2, 3), MPEG2-bc 00110 = MPEG2 – extension 00111 = Reserved 01000 = MPEG2 (layer1 – lsf) 01001 = MPEG2 (layer2, layer3 – lsf) Others = Reserved	0

6.6.1.8 Shadowed SPDIF Repetition Count Register (SPDCNT_SHD, R, Address = 0XE110_001C)

SPDCNT	Bit	Description	Initial State
-	[31:13]	Reserved	0
Stream Repetition Count	[12:0]	Repetition count according to data type This bit is valid only for stream data.	0

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6.6.1.9 User Data Register (USERBIT1~3)

- USERBIT1, R/W, Address = 0XE110_0020
- USERBIT2, R/W, Address = 0XE110_0024
- USERBIT3, R/W, Address = 0XE110_0028

USERBIT1~3	Bit	Description	Initial State
User Data Bit (subcode Q for CD)	[31:0]	USERBIT1: Q1 ~ Q32 USERBIT2: Q33 ~ Q64 USERBIT3: Q65 ~ Q96 User Data Bit has the Digital Audio Track information (Track NO, Play Time etc.). 1176 bits of these being taken out in a row.	0

6.6.1.10 Shadowed User Data Register (USERBIT_SHD)

- USERBIT1_SHD, R, Address = 0XE110_002C
- USERBIT2_SHD, R, Address = 0XE110_0030
- USERBIT3_SHD, R, Address = 0XE110_0034

USERBIT_SHD	Bit	Description	Initial State

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7 ADC & TOUCH SCREEN INTERFACE

This chapter describes the functions and usage of ADC and Touch Screen interface.

7.1 OVERVIEW OF ADC & TOUCH SCREEN INTERFACE

The 10-bit or 12-bit CMOS Analog to Digital Converter (ADC) comprises of 10-channel analog inputs. It converts the analog input signal into 10-bit or 12-bit binary digital codes at a maximum conversion rate of 1MSPS with 5MHz A/D converter clock. A/D converter operates with on-chip sample-and-hold function. ADC supports low power mode.

Touch Screen Interface can control input pads (XP, XM, YP, and YM) to obtain X/Y-position on the external touch screen device. Touch Screen Interface contains three main blocks, namely, touch screen pads control logic, ADC interface logic and interrupt generation logic. There are two set of touch screen interfaces, which share one ADC.

7.2 KEY FEATURES OF ADC & TOUCH SCREEN INTERFACE

The ADC & Touch Screen interface includes the following features:

- Resolution: 10-bit / 12-bit (optional)
- Differential Nonlinearity Error: ± 1.0 LSB (Max.)
- Integral Nonlinearity Error: ± 4.0 LSB (Max.)
- Maximum Conversion Rate: 1 MSPS
- Low Power Consumption
- Power Supply Voltage: 3.3V
- Analog Input Range: 0 ~ 3.3V
- On-chip sample-and-hold function
- Normal Conversion Mode
- Separate X/Y position conversion Mode
- Auto (Sequential) X/Y Position Conversion Mode
- Waiting for Interrupt Mode
- IDLE, DIDLE, STOP and DSTOP mode wakeup source
- Two touch screen interfaces

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7.3 TOUCH SCREEN INTERFACE OPERATION

7.3.1 BLOCK DIAGRAM ADC & TOUCH SCREEN INTERFACE

Figure 7-1 is the functional block diagram of A/D converter and Touch Screen Interface.

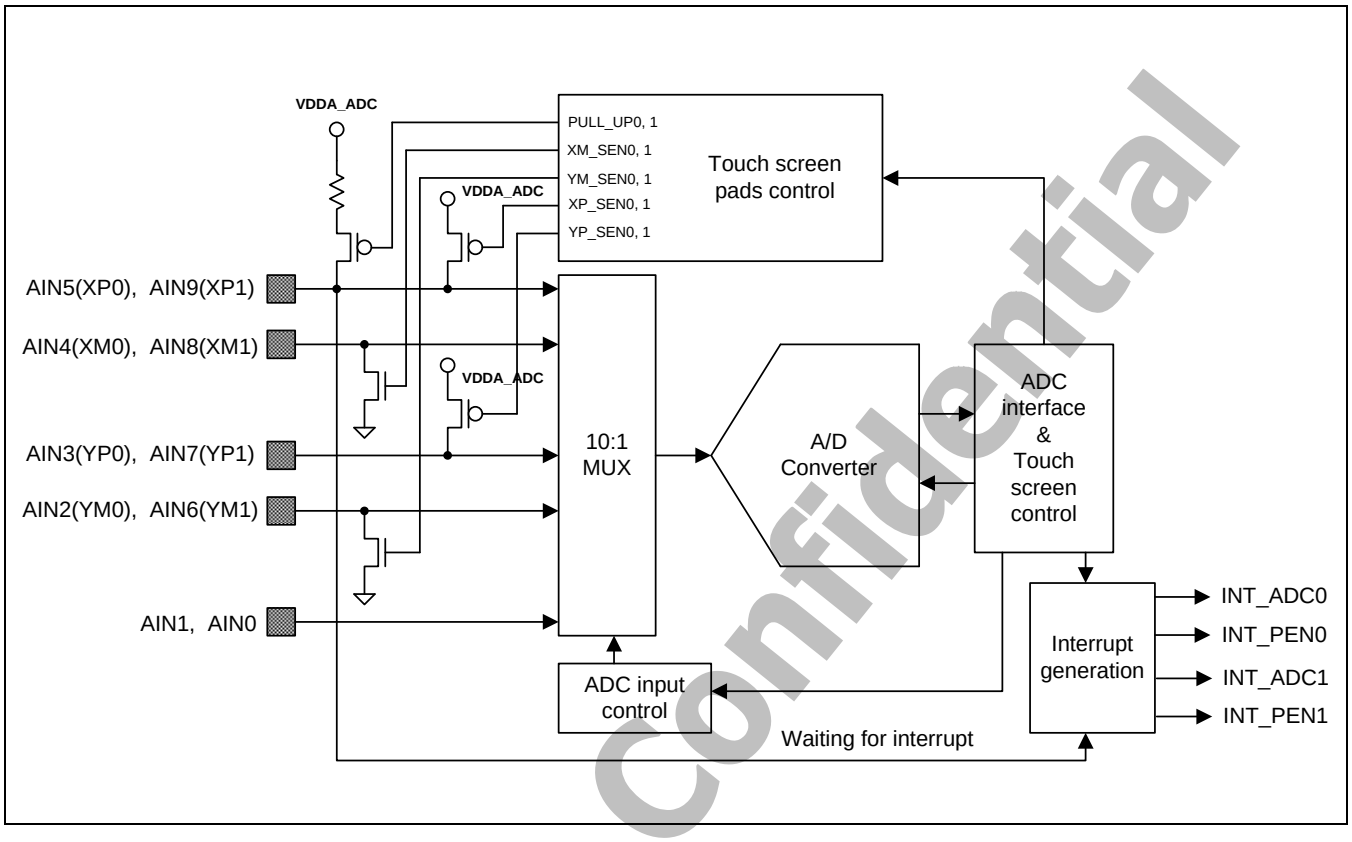

Figure 7-1 ADC and Touch Screen Interface Functional Block Diagram

NOTE: When Touch Screen device is not used, XM, XP, YM or YP can be connected to Analog Input Signal for Normal ADC conversion.

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7.4 FUNCTION DESCRIPTIONS

7.4.1 A/D CONVERSION TIME

When the PCLK frequency is 66MHz and the prescaler value is 65, total 12-bit conversion time is as follows.

- A/D converter freq. = 66MHz/(65+1) = 1MHz
- Conversion time = 1/(1MHz / 5cycles) = 1/200kHz = 5us

NOTE: This A/D converter was designed to operate at maximum 5MHz clock, so the conversion rate can go up to 1MSPS.

7.4.2 TOUCH SCREEN INTERFACE MODE

1. Normal Conversion Mode (AUTO_PST = 0, XY_PST = 0)

The operation of this mode is same as AIN0~AIN9's. To initialize this mode, set the TSADCCON0 (ADC control register) and TSCONn (Touch screen control register). The switches and pull-up resistor should be turned off (all switches are turned off if TSCON0 and TSCON1 are set to 0x58). The converted data can be read out from TSDATX0 (ADC conversion data X register).

NOTE: TSADCCON1 register is useless in normal conversion mode. Therefore, TSSEL bit of TSADCCON0 register should be 0. TSADCCON1 register is meaningless if TSSEL bit is 0.

2. Separate X/Y Position Conversion Mode (AUTO_PST = 0, XY_PST = control)

This mode consists of two states, namely, X-position measurement state and Y-position measurement state.

Steps to operate X-position measurement state;

- Set ‘0x69’ to TSCONn.
  (XY_PST=1, AUTO_PST=0, PULL_UP disable, XP enable, XM enable, YP disable, YM disable)
- Start conversion by setting TSADCCONn.
- The end of X-position conversion can be notified by interrupt (INT_ADCn).
- Read out the converted data (X-position) from TSDATXn.

Steps to operate Y-position measurement state;

- Set ‘0x9a’ to TSCONn.
  (XY_PST=2, AUTO_PST=0, PULL_UP disable XP disable, XM disable, YP enable, YM enable)
- Start conversion by setting TSADCCONn.
- The end of Y-position conversion can be notified by interrupt (INT_ADCn).
- Read out the converted data (Y-position) from TSDATYn.

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7.4.2.1 Touch Screen0 pin Conditions in X/Y Position MEASUREMENT

State	XP0	XM0	YP0	YM0
TS0: X-position measurement	VDDA_ADC	VSSA_ADC	AIN3	Hi-z
TS0: Y-position measurement	AIN5	Hi-z	VDDA_ADC	VSSA_ADC

7.4.2.2 Touch Screen1 pin Conditions in X/Y Position MEASUREMENT

State	XP1	XM1	YP1	YM1
TS1: X-position measurement	VDDA_ADC	VSSA_ADC	AIN7	Hi-z
TS1: Y-position measurement	AIN9	Hi-z	VDDA_ADC	VSSA_ADC

3. Auto (Sequential) X/Y Position Conversion Mode (AUTO_PST = 1, XY_PST = 0)

Steps to operate Auto (Sequential) X/Y Position Conversion Mode:

- Set ‘0x5c’ to TSCONn.
  (XY_PST=0, AUTO_PST=1, PULL_UP disable, XP disable, XM disable, YP disable, YM disable)
- Start conversion by setting TSADCCONn.
- Touch screen controller converts X-Position and writes it to TSDATXn.
- Touch screen controller converts Y-Position and writes it to TSDATYn.
- Touch screen interface generates interrupt (INT_ADCn). In other words, INT_ADCn is occurred only once, not twice.

4. Waiting for Interrupt Mode (TSCONn[7:0] = 0xd3)

Touch screen controller generates an interrupt signal (INT_PENn) when the stylus pen is down or up. The value of TSCONn[7:0] should be '0xd3', that is, pull-up enable, XP disable, XM disable, YP disable and YM enable. After touch screen controller generates interrupt signal (INT_PENn), waiting for interrupt Mode must be cleared (Set 0 to XY_PST).

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7.4.2.3 Touch Screen0 Pin Conditions in Wait for Interrupt Mode

Mode	XP0	XM0	YP0	YM0
TS0: Waiting for Interrupt Mode	VDDA_ADC (Pull-up enable)	Hi-z	Hi-z	VSSA_ADC

7.4.2.4 Touch Screen1 Pin Conditions in Wait for Interrupt Mode

Mode	XP1	XM1	YP1	YM1
TS1: Waiting for Interrupt Mode	VDDA_ADC (Pull-up enable)	Hi-z	Hi-z	VSSA_ADC

7.4.3 STANDBY MODE

Standby mode is activated when TSSEL bit is ‘0’ and STANDBY bit is '1' in TSADCCON0 register. In this mode, A/D conversion operation is halted and TSDATXn and TSDATYn registers hold their values.

7.4.4 TWO TOUCH SCREEN INTERFACES

There are two set of touch screen interfaces, namely, AIN[5] ~ AIN[2] for touch screen 0 and AIN[9] ~ AIN[6] for touch screen 1. There are separate switches for XP, XM, YP and YM control and separate registers to interface with two touch screens. They share one analog digital converter, so interfacing with the two touch screens should be performed in turn. TSSEL bit of TSADCCON0 register is used to select which touch screen is connected to the ADC. Therefore, you must set ‘1’ to TSSEL before an access to TSADCCON1. Similarly, you must set ‘0’ to TSSEL before an access to TSADCCON0.

An access to TSADCCON1 bits is prohibited when TSSEL bit is ‘0’, and an access to TSADCCON0 bits except TSSEL is also prohibited when TSSEL bit is ‘1’. An access to TSSEL bit is always permitted.

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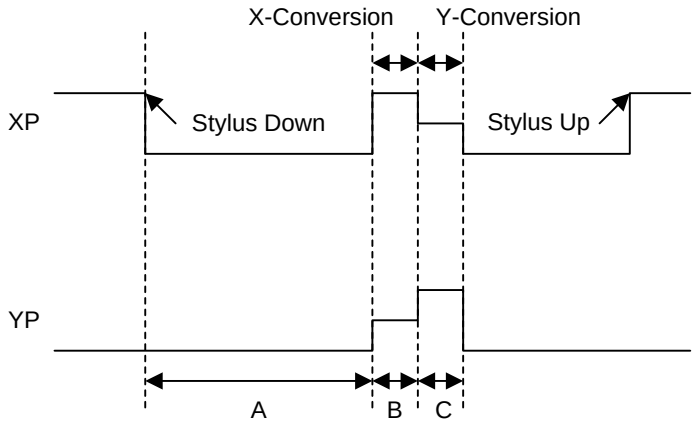
Programming Notes

1. The A/D converted data can be accessed by means of interrupt or polling method. With interrupt method, the overall conversion time - from A/D converter start to converted data read - may be delayed because of the return time of interrupt service routine and data access time. With polling method, to determine the read time for TSDATXn or TSDATYn register, check the TSADCCONn[15] – end of conversion flag – bit.

2. A/D conversion can be activated in different way. After TSADCCONn[1] - A/D conversion start-by-read mode- is set to 1. A/D conversion starts simultaneously when converted data is read.



A = **D** x (1/X-tal clock) or **D** x (1/RTCCLK clock)
B = **D** x (1/PCLK clock) + 5 x (1/PCLK clock)
C = **D** x (1/PCLK clock) + 5 x (1/PCLK clock)

D = Delay value of ADCDLY register

Figure 7-2 ADC and Touch Screen Operation Signal

3. If INT_PEN interrupt is used as an wakeup source in IDLE, DIDLE, STOP and DSTOP mode, XY_PST bit (TSCONn[1:0]) should be set to waiting for interrupt mode (2b'11). UD_SEN bit (TSCONn[8]) determines a stylus pen up wakeup or pen down wakeup.

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7.5 ADC & TOUCH SCREEN INTERFACE INPUT CLOCK DIAGRAM

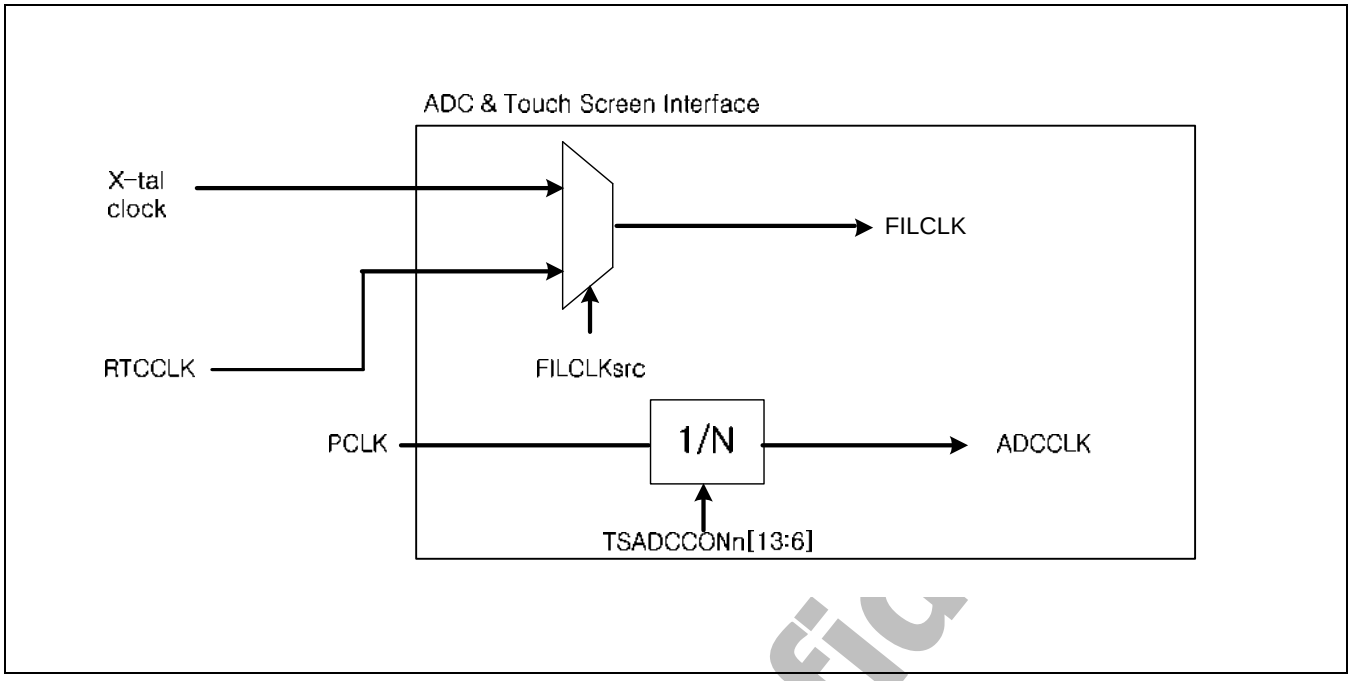

Figure 7-3 Input Clock Diagram for ADC & Touch Screen Interface

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7.6 I/O DESCRIPTIONS

Signal	I/O	Description	Pad	Type
AIN[9]	Input	ADC Channel[9] Analog input	XadcAIN[9]	Analog
AIN[8]	Input	ADC Channel[8] Analog input	XadcAIN[8]	Analog
AIN[7]	Input	ADC Channel[7] Analog input	XadcAIN[7]	Analog
AIN[6]	Input	ADC Channel[6] Analog input	XadcAIN[6]	Analog
AIN[5]	Input	ADC Channel[5] Analog input	XadcAIN[5]	Analog
AIN[4]	Input	ADC Channel[4] Analog input	XadcAIN[4]	Analog
AIN[3]	Input	ADC Channel[3] Analog input	XadcAIN[3]	Analog
AIN[2]	Input	ADC Channel[2] Analog input	XadcAIN[2]	Analog
AIN[1]	Input	ADC Channel[1] Analog input	XadcAIN[1]	Analog
AIN[0]	Input	ADC Channel[0] Analog input	XadcAIN[0]	Analog

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7.7 REGISTER DESCRIPTION

7.7.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
TSADCCON0	0xE170_0000	R/W	Specifies the TS0 - ADC Control Register	0x0000_3FC4
TSCON0	0xE170_0004	R/W	Specifies the TS0 - Touch Screen Control Register	0x0000_0058
TSDLY0	0xE170_0008	R/W	Specifies the TS0 - ADC Start or Interval Delay Register	0x0000_00FF
TSDATX0	0xE170_000C	R	Specifies the TS0 - ADC Conversion Data X Register	-
TSDATY0	0xE170_0010	R	Specifies the TS0 - ADC Conversion Data Y Register	-
TSPENSTAT0	0xE170_0014	R/W	Specifies the TS0 - Pen0 Up or Down Status Register	0x0000_0000
CLRINTADC0	0xE170_0018	W	Specifies the TS0 - Clear ADC0 Interrupt	-
ADCMUX	0xE170_001C	R/W	Specifies the Analog input channel selection	0x0000_0000
CLRINTPEN0	0xE170_0020	W	Specifies the TS0 - Clear Pen0 Down/Up Interrupt	-
TSADCCON1	0xE170_1000	R/W	Specifies the TS1 - ADC Control Register	0x0000_3FC4
TSCON1	0xE170_1004	R/W	Specifies the TS1 - Touch Screen Control Register	0x0000_0058
TSDLY1	0xE170_1008	R/W	Specifies the TS1 - ADC Start or Interval Delay Register	0x0000_00FF
TSDATX1	0xE170_100C	R	Specifies the TS1 - ADC Conversion Data X Register	-
TSDATY1	0xE170_1010	R	Specifies the TS1 - ADC Conversion Data Y Register	-
TSPENSTAT1	0xE170_1014	R/W	Specifies the TS1 - Pen1 Up or Down Status Register	0x0000_0000
CLRINTADC1	0xE170_1018	W	Specifies the TS1 - Clear ADC1 Interrupt	-
CLRINTPEN1	0xE170_1020	W	Specifies the TS1 - Clear Pen1 Up/Down Interrupt	-

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7.7.1.1 ADC Control Register (TSADCCONn)

- TSADCCON0, R/W, Address = 0xE170_0000
- TSADCCON1, R/W, Address = 0xE170_1000

TSADCCONn	Bit	Description	Initial State
TSSEL	[17]	Touch screen selection 0 = Touch screen 0 (AIN2~AIN5) 1 = Touch screen 1 (AIN6~AIN9) This bit exists only in TSADCCON0. Note: An access to TSADCCON1 bits is prohibited when TSSEL bit is 0, and an access to TSADCCON0 bits except TSSEL is prohibited when TSSEL bit is 1. An access to TSSEL bit is always permitted.	0
RES	[16]	ADC output resolution selection 0 = 10bit A/D conversion 1 = 12bit A/D conversion	0
ECFLG	[15]	End of conversion flag(Read only) 0 = A/D conversion in process 1 = End of A/D conversion	0
PRSCEN	[14]	A/D converter prescaler enable 0 = Disable 1 = Enable	0
PRSCVL	[13:6]	A/D converter prescaler value Data value: 5 ~ 255 The division factor is (N+1) when the prescaler value is N. For example, ADC frequency is 3.3MHz if PCLK is 66MHz and the prescaler value is 19. Note: This A/D converter is designed to operate at maximum 5MHz clock, so the prescaler value should be set such that the resulting clock does not exceed 5MHz.	0xFF
Reserved	[5:3]	Reserved	0
STANDBY	[2]	Standby mode select 0 = Normal operation mode 1 = Standby mode Note: In standby mode, prescaler should be disabled to reduce more leakage power consumption.	1
READ_ START	[1]	A/D conversion start by read 0 = Disables start by read operation 1 = Enables start by read operation	0
ENABLE_START	[0]	A/D conversion starts by enable. If READ_START is enabled, this value is not valid. 0 = No operation 1 = A/D conversion starts and this bit is automatically cleared after the start-up.	0

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7.7.1.2 Touch Screen Control Register (TSCONn)

- TSCON0, R/W, Address = 0xE170_0004
- TSCON1, R/W, Address = 0xE170_1004

TSCONn	Bit	Description	Initial State
UD_SEN	[8]	Detect Pen Up or Down status. 0 = Detects pen down. 1 = Detects pen up.	0
YM_SEN	[7]	YM to GND Switch Enable 0 = Switch disable.(YM = Hi-z) 1 = Switch enable(YM = VSSA_ADC)	0
YP_SEN	[6]	YP to VDD Switch Enable 0 = Switch enable. (YP = VDDA_ADC) 1 = Switch disable.(YP = Hi-z)	1
XM_SEN	[5]	XM to GND Switch Enable 0 = Switch disable.(XM = Hi-z) 1 = Switch enable.(XM = VSSA_ADC)	0
XP_SEN	[4]	XP to VDD Switch Enable 0 = Switch enable.(XP = VDDA_ADC) 1 = Switch disable.(XP = Hi-z)	1
PULL_UP	[3]	Pull-up Switch Enable 0 = XP Pull-up Enable. 1 = XP Pull-up Disable.	1
AUTO_PST	[2]	Automatic sequencing conversion of X-Position and Y-Position 0 = Normal ADC conversion. 1 = Auto Sequential measurement of X-position, Y-position.	0
XY_PST	[1:0]	Manually measurement of X-Position or Y-Position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	0

NOTE:

1. While waiting for touch screen Interrupt, XP_SEN bit must be set to '1', namely ‘XP output disable’ and PULL_UP bit must be set to '0', namely 'XP pull-up enable'.
2. AUTO_PST bit should be set '1' only in Automatic & Sequential X/Y Position conversion.

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Touch screen0 pin conditions in X/Y position conversion.

	XP0	XM0	YP0	YM0	ADC ch. select
TS0: X Position	Vref	GND	AIN[3]	Hi-Z	YP0
TS0: Y Position	AIN[5]	Hi-Z	Vref	GND	XP0

Touch screen1 pin conditions in X/Y position conversion.

	XP1	XM1	YP1	YM1	ADC ch. select
TS1: X Position	Vref	GND	AIN[7]	Hi-Z	YP1
TS1: Y Position	AIN[9]	Hi-Z	Vref	GND	XP1

7.7.1.3 ADC Delay Register (TSDLYn)

- TSDLY0, R/W, Address = 0xE170_0008
- TSDLY1, R/W, Address = 0xE170_1008

TSDLYn	Bit	Description	Initial State
FILCLKsrc	[16]	Reference clock source for delay. 0 = X-tal clock. 1 = RTC clock.	0
DELAY	[15:0]	In case of ADC conversion mode (Normal, Separate, Auto conversion); ADC conversion is delayed by counting this value. Counting clock is PCLK. → ADC conversion delay value. In case of waiting for Interrupt mode: When stylus down occurs in waiting for interrupt mode, it generates interrupt signal (INT_PENn) at interval of several ms for Auto X/Y position conversion. If this interrupt occurs in STOP mode, it generates Wake-Up signal, having interval (several ms), for Exiting STOP MODE. Note: Do not use zero value(0x0000)	00ff

NOTE: Before ADC conversion, Touch screen uses X-tal clock.
During ADC conversion PCLK (Max. 66MHz) is used.

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7.7.1.4 ADC Conversion Data X Register (TSDATXn)

- TSDATX0, R, Address = 0xE170_000C
- TSDATX1, R, Address = 0xE170_100C

TSDATXn	Bit	Description	Initial State
UPDOWN	[15]	Up or Down state of stylus pen at Waiting for Interrupt Mode. 0 = Pen down state. 1 = Pen up state.	-
AUTO_PST_VAL	[14]	Monitoring value of AUTO_PST field in TSCONn register. Read only. 0 = Normal ADC conversion. 1 = Sequencing measurement of X-position, Y-position.	-
XY_PST_VAL	[13:12]	Monitoring value of XY_PST field in TSCONn register. Read only. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	-
XPDATA (Normal ADC)	[11:0]	X-Position conversion data value (includes normal ADC conversion data value) Data value: 0x0 ~ 0xFFF	-

7.7.1.5 ADC Conversion Data Y Register (TSDATYn)

- TSDATY0, R, Address = 0xE170_0010
- TSDATY1, R, Address = 0xE170_1010

TSDATYn	Bit	Description	Initial State
UPDOWN	[15]	Up or Down state of stylus pen at Waiting for Interrupt Mode. 0 = Pen down state. 1 = Pen up state.	-
AUTO_PST_VAL	[14]	Monitoring value of AUTO_PST field in TSCONn register. Read only. 0 = Normal ADC conversion. 1 = Sequencing measurement of X-position, Y-position.	-
XY_PST_VAL	[13:12]	Monitoring value of XY_PST field in TSCONn register. Read only. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	-
YPDATA	[11:0]	Y-Position conversion data value Data value: 0x0 ~ 0xFFF	-

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7.7.1.6 Pen Status Register (TSPENSTATn)

- TSPENSTAT0, R/W, Address = 0xE170_0014
- TSPENSTAT1, R/W, Address = 0xE170_1014

TSPENSTATn	Bit	Description	Initial State
TSC_UP	[1]	Pen up interrupt history. (after check, this bit should be cleared manually) 0 = No pen up state. 1 = Pen up interrupt has been occurred.	0
TSC_DN	[0]	Pen down interrupt history. (after check, this bit should be cleared manually) 0 = No pen down state. 1 = Pen down interrupt has been occurred.	0

7.7.1.7 ADC Interrupt Clear Register (CLRINTADCn)

- CLRINTADC0, W, Address = 0xE170_0018
- CLRINTADC1, W, Address = 0xE170_1018

These registers are used to clear the interrupts. Interrupt service routine is responsible to clear interrupts after the interrupt service is completed. Writing any values on this register will clear up the relevant interrupts asserted. When it is read, undefined value will be returned.

CLRINTADCn	Bit	Description	Initial State
INTADCCLR	[0]	INT_ADCn interrupt clear. Cleared if any value is written.	-

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7.7.1.8 ADC Channel Mux Register (ADCMUX, R/W, Address = 0xE170_001C)

ADCMUX	Bit	Description	Initial State
SEL_MUX	[3:0]	Analog input channel select 0000 = AIN 0 0001 = AIN 1 0010 = AIN 2 (YM0) 0011 = AIN 3 (YP0) 0100 = AIN 4 (XM0) 0101 = AIN 5 (XP0) 0110 = AIN 6 (YM1) 0111 = AIN 7 (YP1) 1000 = AIN 8 (XM1) 1001 = AIN 9 (XP1)	0

NOTE:

1. When touch screen is not used, the touch screen ports (AIN2 ~ AIN9) can be used as analog input ports for ADC.
2. SEL_MUX value is invalid when TSADC is set as 1) separate X/Y position conversion mode or 2) auto (sequential) X/Y position conversion mode.

7.7.1.9 Pen Interrupt Clear Register (CLRINTPENn)

- CLRINTPEN0, W, Address = 0xE170_0020
- CLRINTPEN1, W, Address = 0xE170_1020

CLRINTPENn	Bit	Description	Initial State
INTPENCLR	[0]	INT_PENn interrupt clear. Cleared if any value is written.	-

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8 KEYPAD INTERFACE

8.1 OVERVIEW OF KEYPAD INTERFACE

The Key Pad Interface block in S5PV210 facilitates communication with external keypad devices. The ports multiplexed with GPIO ports provide up to 14 rows and 8 columns. You can use keypad interface on port0 and port1. port0 is mapped for 8x8 key interface and port1 for 14x8. You can also make your own mapping that can be mix of port0 and port1. The events of key press or key release are delivered to the CPU by an interrupt. If one of the interrupt from row lines occurs, the software must scan the column lines using the proper procedure to detect one or multiple key press or release.

It provides interrupt status register bits at the time of key pressed or key released or both cases (when two interrupt conditions are enabled). To prevent the switching noises, keypad interface comprise of internal debouncing filter.

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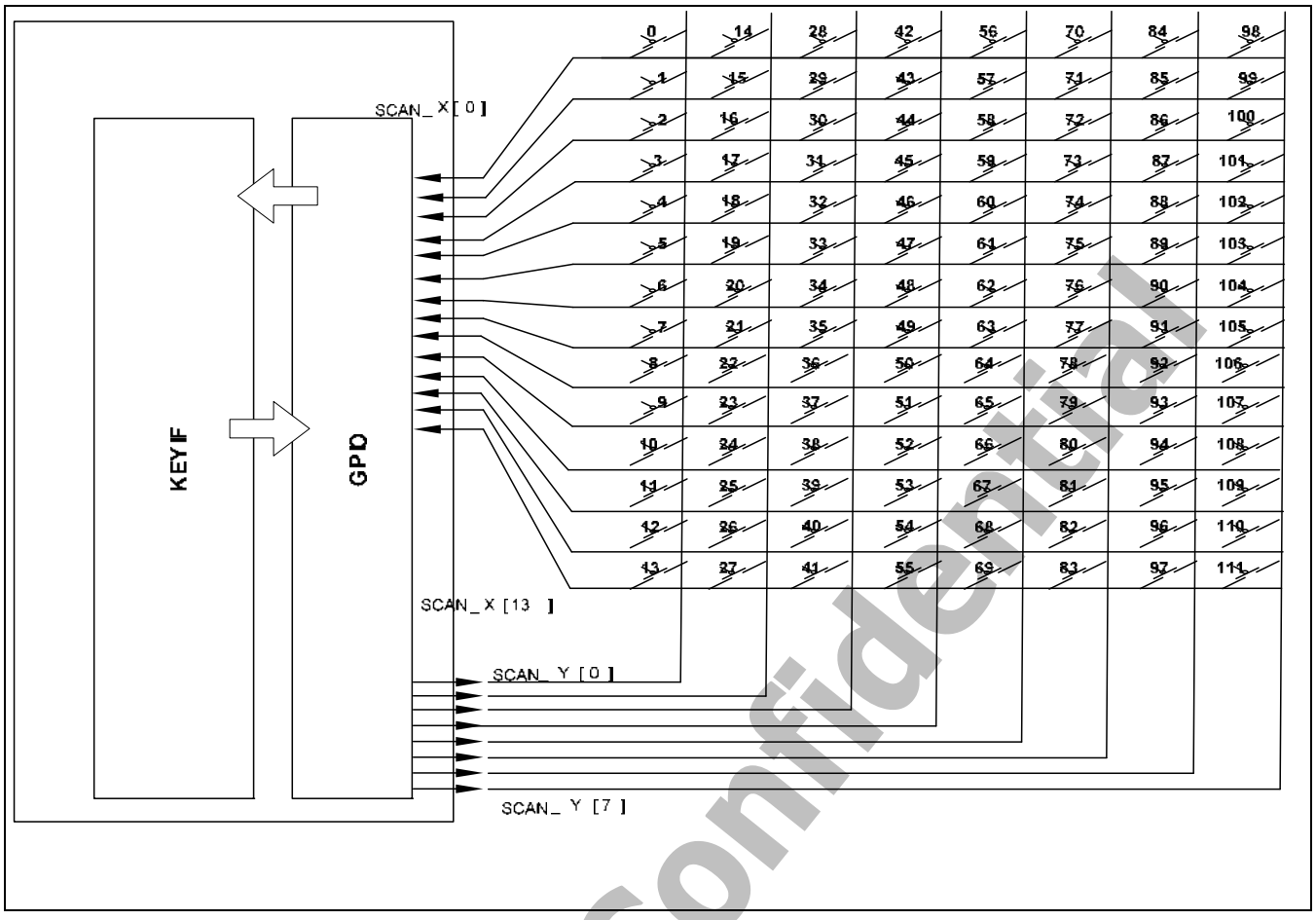

Figure 8-1 Key Matrix Interface External Connection Guide

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8.2 DEBOUNCING FILTER

The debouncing filter is supported for keypad interrupt of any key input. The filtering width is approximately 62.5usec ("FCLK" two-clock, when the FCLK is 32kHz). The keypad interrupt (key pressed or key released) to the CPU is an ANDed signal of the all row input lines after filtering.

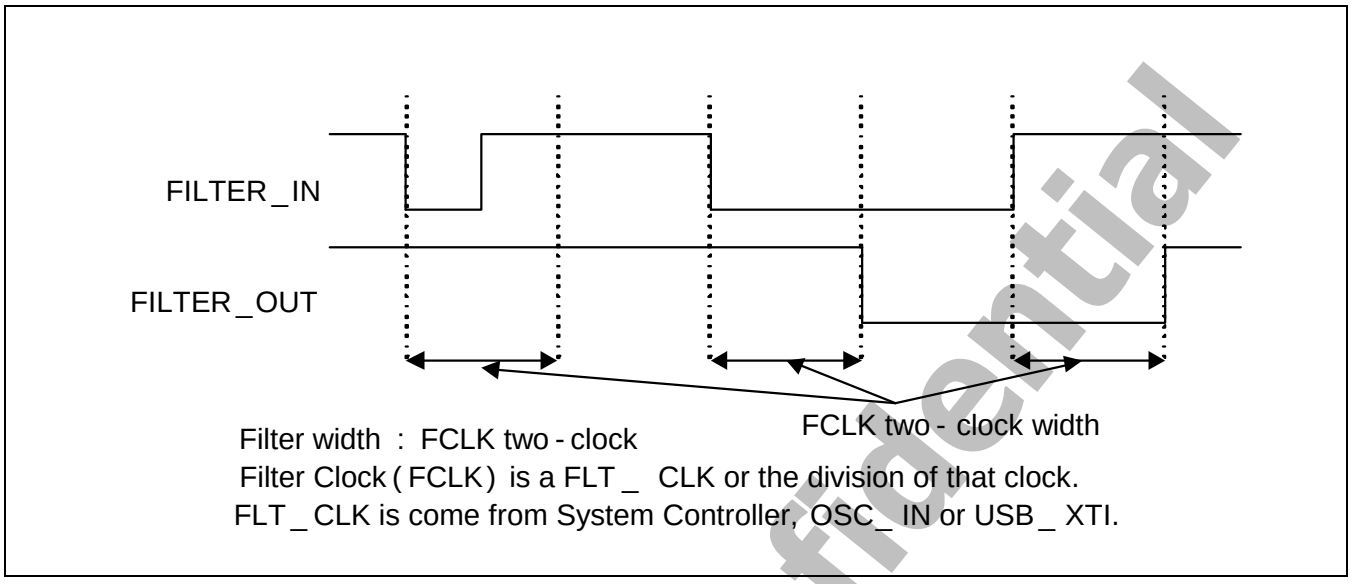

Figure 8-2 Internal Debouncing Filter Operation

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8.3 FILTER CLOCK

KEYPAD interface debouncing filter clock (FCLK) is divided from FLT_CLK, that is OSC_IN. User can set compare value for 10-bit up-counter (KEYIFFC). When filter enable bit(FC_EN) is HIGH, filter clock divider is ON. The frequency of FCLK is frequency of FLT_CLK / ((KEYIFFC + 1) x 2). On the contrary, if FC_EN is Low, filter clock divider does not divide FLT_CLK.

8.4 WAKEUP SOURCE

KEYPAD inputs using Port0 can be used as a wakeup source. When the Key input is used for wakeup source from IDLE, STOP or SLEEP mode, KEYPAD interface register setting is not required. GPIO register setting (GPH2CON, GPH3CON) for KEYPAD interface and SYSCON register (PWR_CFG) for masking are required for wakeup. Therefore, to use 14x8 KEYIF which can be used by wakeup source, you must input mix rows of port0 and port1. For example, port0 for ROW[0:7], port1 for ROW[8:13]. In this case, the only keys using port0 can be wakeup source.

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8.5 KEYPAD SCANNING PROCEDURE

At initial state, all column lines (outputs) are low level. But column data output tri-state enable bits are all high, so, when the tri-state enable mode is not used, these bits should be written to zeros. If state is no key pressed, all row lines (inputs) are high (used pull-up pads). If any key is pressed, the corresponding row and column lines are shortened together and a low level is driven on the corresponding row line, generating a keypad interrupt. The CPU (software) outputs a LOW on one column line and Hi-Z on the others by setting KEYIFCOLEN and KEYIFCOL fields in KEYIFCOL register. Each write time, the CPU reads the value of the KEYIFROW register and detects if one key of the corresponding column line is pressed. Because the KEYIF has pull-up PAD, each KEYIFROW bits will be read as HIGH, except pressed ROW bit. When the scanning procedure ends, the pressed key (one or more) can be detected.

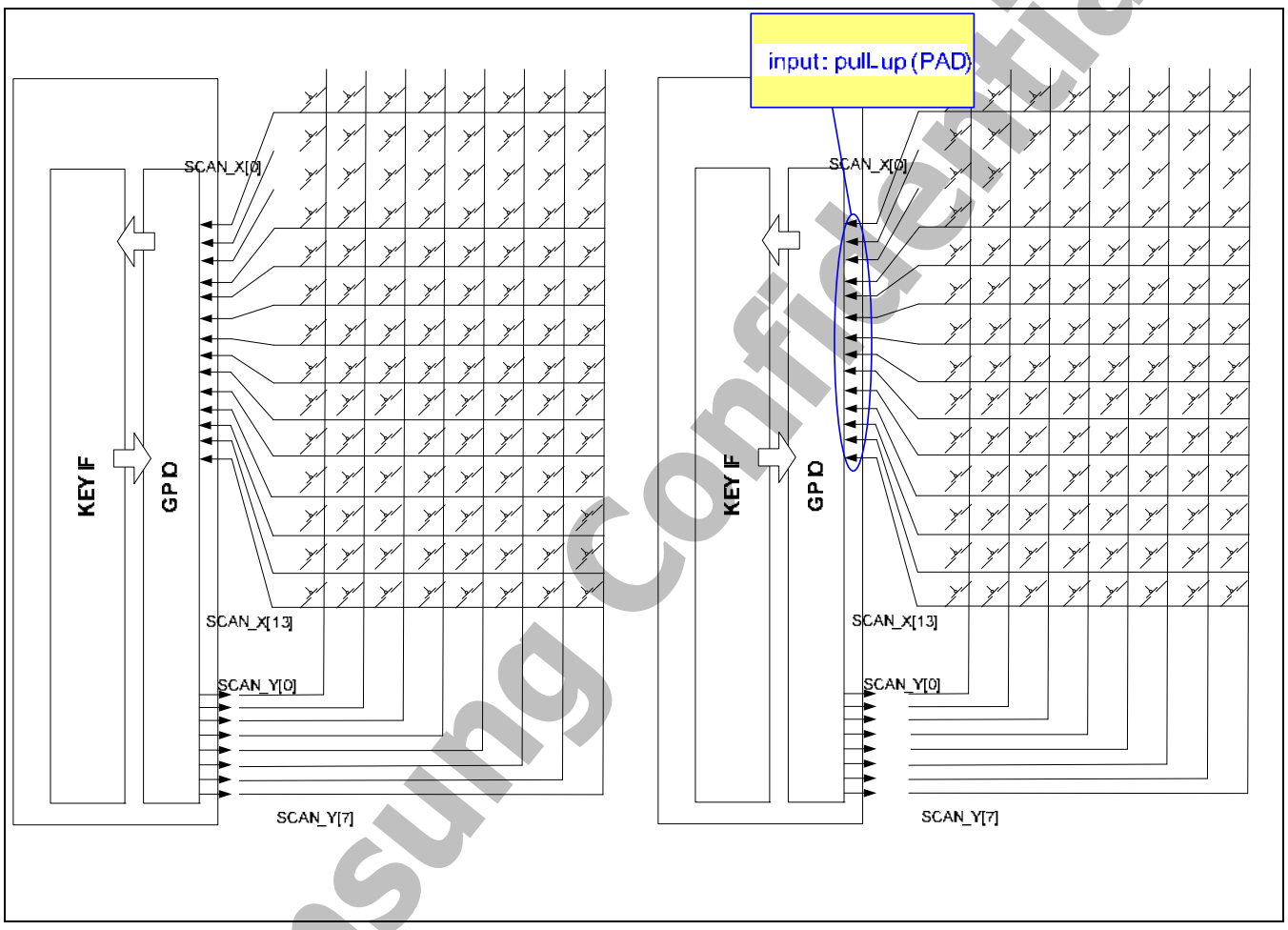

Figure 8-3 Keypad Scanning Procedure

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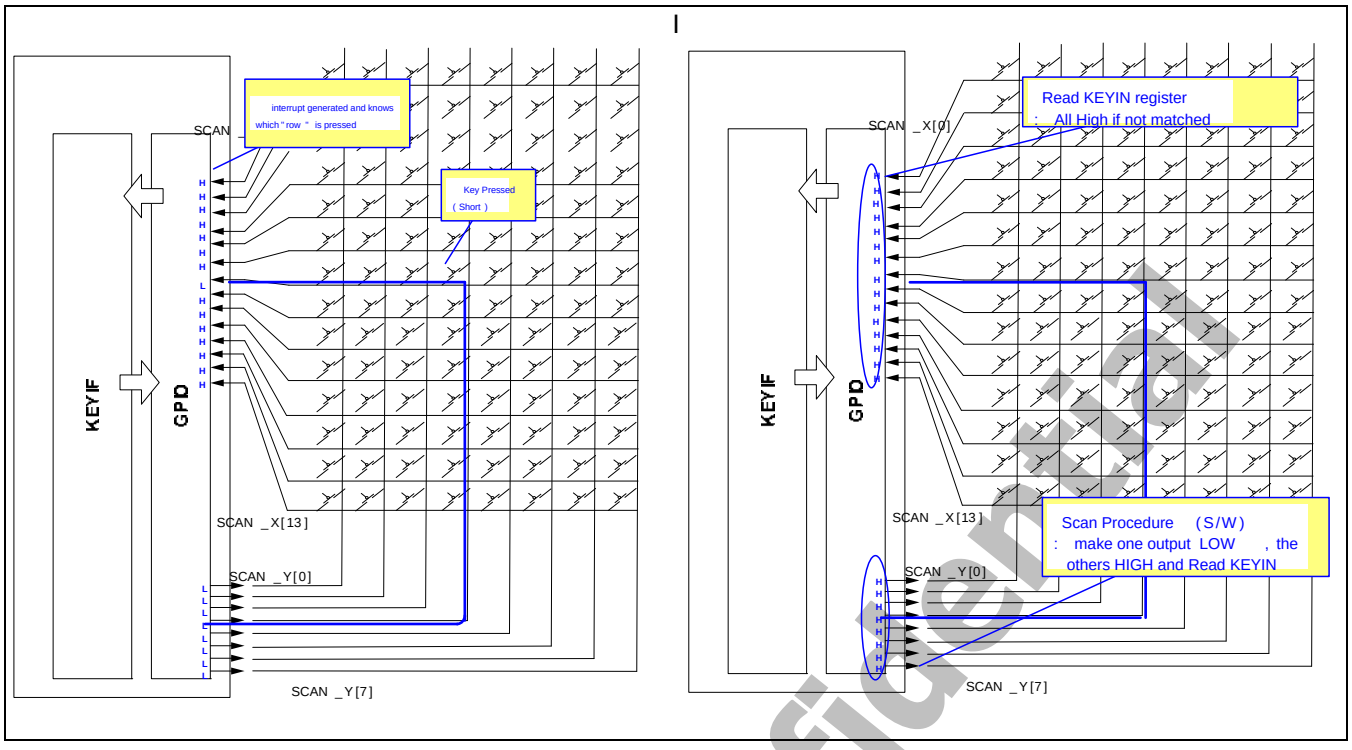

Figure 8-4 Keypad Scanning Procedure II

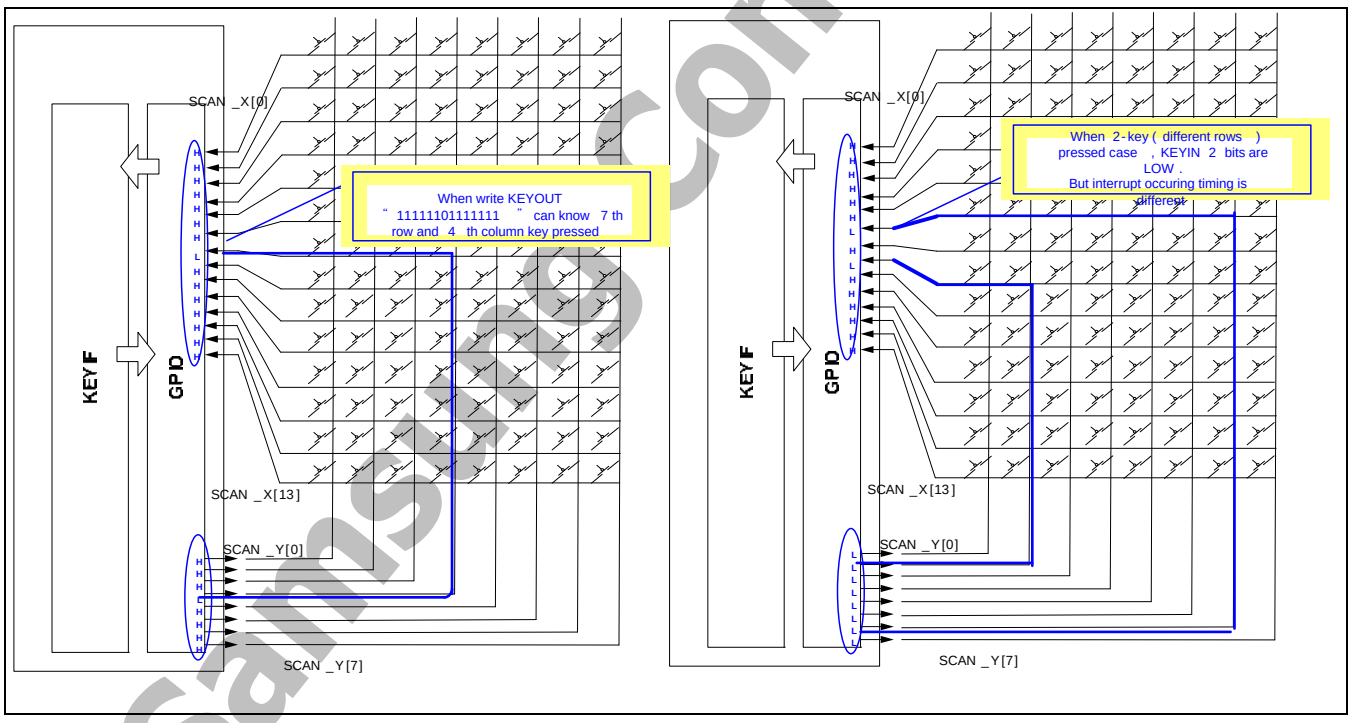

Figure 8-5 Keypad Scanning Procedure III

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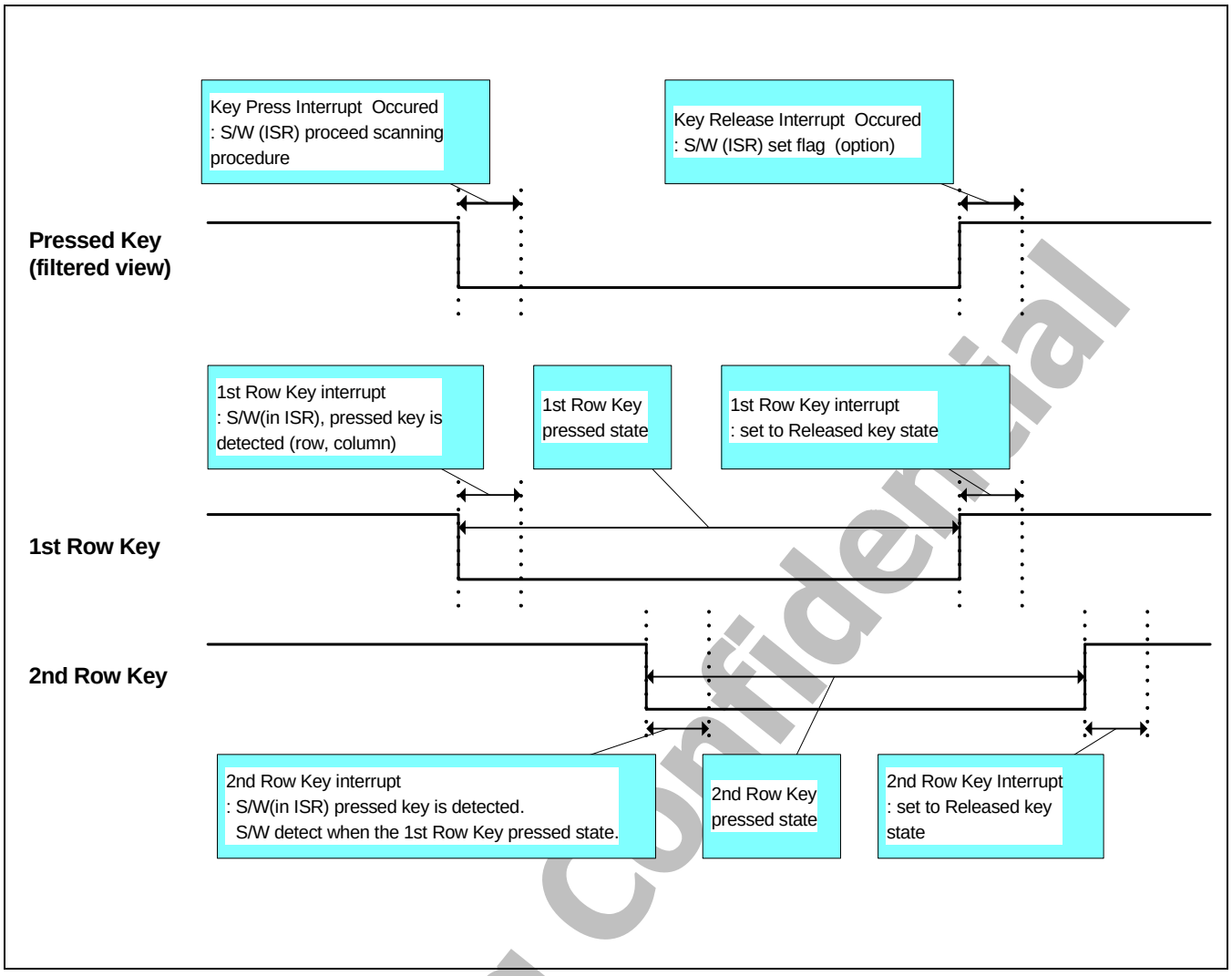

Figure 8-6 Keypad Scanning Procedure when the two-key Pressed with Different Row

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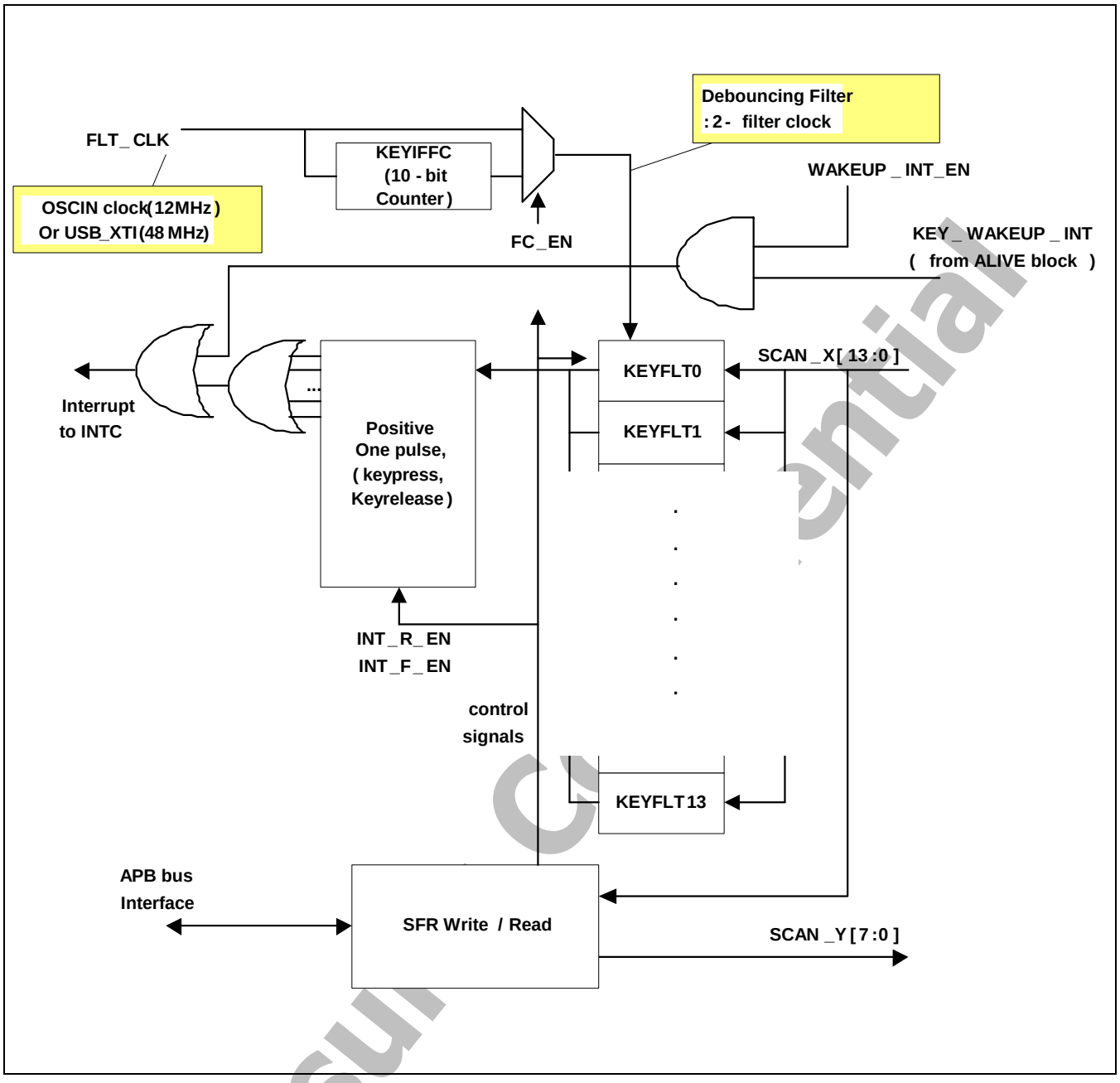

Figure 8-7 Keypad I/F Block Diagram

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8.6 I/O DESCRIPTION

Table 8-1 Keypad interface I/O Description

Signal	I/O	Description	Pad		Type
			Port0	Port1	
ROW_IN[13]	I	KEYPAD Interface Row[13] Data		XmsmADVN (GPJ4[4])	muxed
ROW_IN[12]	I	KEYPAD Interface Row[12] Data		XmsmIRQn (GPJ4[3])	muxed
ROW_IN[11]	I	KEYPAD Interface Row[11] Data		XmsmRn (GPJ4[2])	muxed
ROW_IN[10]	I	KEYPAD Interface Row[10] Data		XmsnWEn (GPJ4[1])	muxed
ROW_IN[9]	I	KEYPAD Interface Row[9] Data		XmsmCSn (GPJ4[0])	muxed
ROW_IN[8]	I	KEYPAD Interface Row[8] Data		XmsmDATA[15] (GPJ3[7])	muxed
ROW_IN[7]	I	KEYPAD Interface Row[7] Data	XEINT[31] (GPH3[7])	XmsmDATA[14] (GPJ3[6])	muxed
ROW_IN[6]	I	KEYPAD Interface Row[6] Data	XEINT[30] (GPH3[6])	XmsmDATA[13] (GPJ3[5])	muxed
ROW_IN[5]	I	KEYPAD Interface Row[5] Data	XEINT[29] (GPH3[5])	XmsmDATA[12] (GPJ3[4])	muxed
ROW_IN[4]	I	KEYPAD Interface Row[4] Data	XEINT[28] (GPH3[4])	XmsmDATA[11] (GPJ3[3])	muxed
ROW_IN[3]	I	KEYPAD Interface Row[3] Data	XEINT[27] (GPH3[3])	XmsmDATA[10] (GPJ3[2])	muxed
ROW_IN[2]	I	KEYPAD Interface Row[2] Data	XEINT[26] (GPH3[2])	XmsmDATA[9] (GPJ3[1])	muxed
ROW_IN[1]	I	KEYPAD Interface Row[1] Data	XEINT[25] (GPH3[1])	XmsmDATA[8] (GPJ3[0])	muxed
ROW_IN[0]	I	KEYPAD Interface Row[0] Data	XEINT[24] (GPH3[0])	XmsmDATA[7] (GPJ2[0])	muxed
COL_OUT[7]	O	KEYPAD Interface Column[7] Data	XEINT[23] (GPH2[7])	XmsmDATA[6] (GPJ2[0])	muxed
COL_OUT [6]	O	KEYPAD Interface Column[6] Data	XEINT[22] (GPH2[6])	XmsmDATA[5] (GPJ2[0])	muxed
COL_OUT [5]	O	KEYPAD Interface Column[5] Data	XEINT[21] (GPH2[5])	XmsmDATA[4] (GPJ2[0])	muxed
COL_OUT [4]	O	KEYPAD Interface Column[4] Data	XEINT[20] (GPH2[4])	XmsmDATA[3] (GPJ2[0])	muxed

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Signal	I/O	Description	Pad		Type
			Port0	Port1	
COL_OUT [3]	O	KEYPAD Interface Column[3] Data	XEINT[19] (GPH2[3])	XmsmDATA[2] (GPJ2[0])	Muxed
COL_OUT [2]	O	KEYPAD Interface Column[2] Data	XEINT[18] (GPH2[2])	XmsmDATA[1] (GPJ2[0])	muxed
COL_OUT [1]	O	KEYPAD Interface Column[1] Data	XEINT[17] (GPH2[1])	XmsmDATA[0] (GPJ2[0])	muxed
COL_OUT [0]	O	KEYPAD Interface Column[0] Data	XEINT[16] (GPH2[0])	XmsmADDR[13] (GPJ2[0])	muxed

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8.7 REGISTER DESCRIPTION

8.7.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
KEYIFCON	0xE160_0000	R/W	Specifies the KEYPAD interface control register	0x00000000
KEYIFSTSCLR	0xE160_0004	R/W	Specifies the KEYPAD interface status and clear register	0x00000000
KEYIFCOL	0xE160_0008	R/W	Specifies the KEYPAD interface column data output register	0x0000FF00
KEYIFROW	0xE160_000C	R	Specifies the KEYPAD interface row data input register	Reflects input ports
KEYIFFC	0xE160_0010	R/W	Specifies the KEYPAD interface debouncing filter clock division register	0x00000000

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8.7.1.1 KEYPAD Interface Control Registers (KEYIFCON, R/W, Address = 0xE160_0000)

KEYIFCON	Bit	Description	Initial State
Reserved	[31:5]	Reserved for future use	-
WAKEUPEN	[4]	KEYPAD input Stop / Idle mode wakeup enable. Wakeup signal is to System Controller. 0 = Disables 1 = Key input Low Level (while key-pressed) wakeup	1'b0
FC_EN	[3]	10-bit counter (for debouncing digital filter clock) enable 0 = Disables: No use division counter 1 = Enables: use division counter	1'b0
DF_EN	[2]	KEYPAD input port debouncing filter enable 0 = Disables 1 = Enables	1'b0
INT_R_EN	[1]	KEYPAD input port rising edge (key-released) interrupt 0 = Disables 1 = Enables	1'b0
INT_F_EN	[0]	KEYPAD input port falling edge (key-pressed) interrupt 0 = Disables 1 = Enables	1'b0

NOTE: Both edge interrupt is selected when both INT_F_EN and INT_R_EN are set.

8.7.1.2 KEYPAD Interrupt Status and Clear Register (KEYIFSTSCLR, R/W, Address = 0xE160_0004)

KEYIFSTSCLR	Bit	Description	Initial State
R_INT	[29:16]	KEYPAD input "release" interrupt (rising edge) status(read) and clear(write) Read: 1 = Released interrupt occurred 0 = Not occurred Write: Released interrupt is cleared when write '1' The R_INT[13:0] indicate that each key pressed from 0 to 13 has a dedicated interrupt from R_INT[16] to R_INT[29]	14'b0
P_INT	[13:0]	KEYPAD input "press" interrupt (falling edge) status(read) and clear(write) Read: 1 = Pressed interrupt occurred 0 = Not occurred Write: Pressed interrupt is cleared when write '1' The P_INT[13:0] indicate that each key released from 0 to 13 has a dedicated interrupt from P_INT[0] to P_INT[13]	14'b0

NOTE: Keypad wakeup interrupt is also cleared when the write access to the KEYIFSTSCLR.

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8.7.1.3 KEYPAD Interface Column Data Output Register (KEYIFCOL, R/W, Address = 0xE160_0008)

KEYIFCOL	Bit	Description	Initial State
Reserved	[31:16]	Reserved for future use	-
KEYIFCOLEN	[15:8]	KEYPAD interface column data output tri-state enable register Each bit is for each KEYIFCOL bit. 0 = Output pad tri-state buffer enable(Normal output), 1 = Output pad Tri-state buffer disable(High-Z output) (@ reset)	8'b1111_1111
KEYIFCOL	[7:0]	KEYPAD interface column data output register	8'b0

8.7.1.4 KEYPAD Interface Row Data Input Register (KEYIFROW, R, Address = 0xE160_000C)

KEYIFROW	Bit	Description	Initial State
Reserved	[31:16]	Reserved for future use	-
KEYIFROW	[13:0]	KEYPAD interface row data input register (read only) This register values from input ports are not filtered data.	Reflects input ports

8.7.1.5 KEYPAD Interface Debouncing Filter Clock Division Register (KEYIFFC, R/W, Address = 0xE160_0010)

KEYIFFC	Bit	Description	Initial State
Reserved	[31:10]	Reserved for future use	-
KEYIFFC	[9:0]	KEYPAD interface debouncing filter clock division register. User can set compare value for 10-bit up-counter. This register value means when FC_EN bit is HIGH. FCLK = FLT_CLK / (KEYIFFC[9:0] + 1) (FLT_CLK is from FINpll)	10'b0

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Section 11

SECURITY

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1 SECURITY-SYSTEM

1.1 OVERVIEW OF SECURITY-SYSTEM

S5PV210 supports following security features

- Secure Booting
- Security Engines

Table 1-1 shows the detail security features of S5PV210.

S5PV210 provides on chip 64KB boot ROM, 96KB RAM and the 128-bit e-Fuse for secure booting. For more information, refer to 'Section 02.06 Booting sequence'.

Additionally, users can design security solution more conveniently using H/W security engine such as DES/ 3DES, AES, SHA-1, PRNG and PKA.

Table 1-1 Security Features of S5PV210

	Description
Secure Booting	On chip 64KB secure boot ROM On chip 96KB secure SRAM 128-bit e-fuse ROM for secure context
Security Engines	DES/ 3DES, AES, SHA-1, PRNG and PKA

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2 ADVANCED CRYPTO ENGINE

2.1 OVERVIEW OF ADVANCED CRYPTO ENGINE

Security subsystem (SSS) represents a small system with internal buses and small security IPs that should be attached to a chip as an IP. The security IPs in SSS can process the independent security function.

SSS comprises of the following internal components:

- AES
- DES and 3DES
- SHA-1, MD5, HMAC, and PRNG
- Public Key Accelerator (PKA)
- Feed Controller (FeedCtrl)

FeedCtrl comprises of the following components:

- Block Cipher Receiving DMA (BRDMA)
- Block Cipher Transmission DMA (BTDMA)
- Hash Receiving DMA (HRDMA)
- PKA Bi-directional DMA (PKDMA)
- FIFO and FIFO Interconnections
- Interrupt Controller
- FIFO Controller

SSS comprises of the following external interfaces:

- One bus slave port (for SFR setting)
- Four bus master ports (for DMA operations)
- Two interrupts: MA interrupt (to notify the end of DMA operations) and Hash interrupt (to notify the end of Hash or PRNG operations)

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Each security IP can be accessed through two access modes, namely:

- CPU mode
  - For AES, DES, 3DES, SHA-1, MD5, and PKA
  - Every input and output data should be carried out by the host processor.
- FIFO mode
  - For AES, DES, 3DES, SHA-1, and MD5
  - DMA supplies input data to each IP through FIFO.
  - DMA drains output data from each IP (except SHA-1 and MD5) through FIFO.
  - Block ciphers and hashes can share input data.
  - Output data of block ciphers can be used as input of the hash.

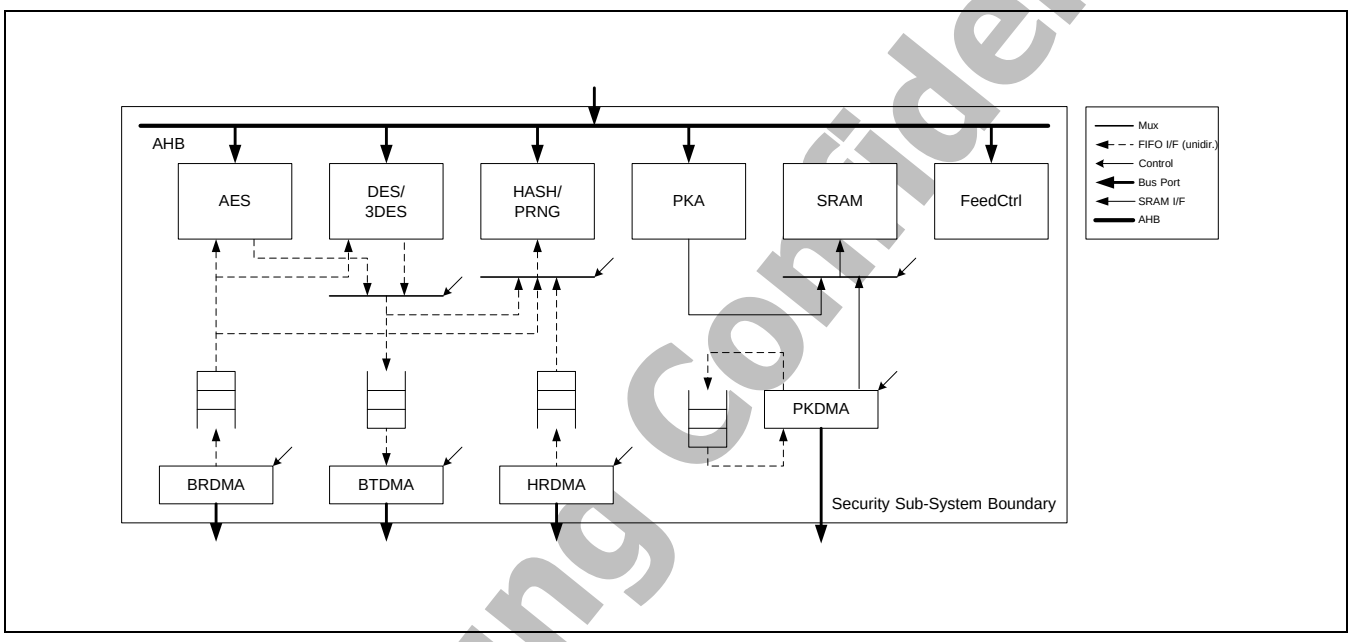

Figure 2-1 Block Diagram of SSS

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2.1.1 KEY FEATURES OF SSS

The key features of SSS include:

- AES (ECB, CBC, and CTR modes)
- DES (ECB and CBC modes)
- 3DES (ECB, CBC, EDE, and EEE modes)
- SHA-1 (with hardware padding) and SHA-1 HMAC
- MD5 (w/ hardware padding) and MD5 HMAC
- Pseudo Random Number Generator (PRNG)
- Public Key Accelerator (PKA)
- DMA Support for AES, DES, 3DES, SHA-1, MD5, and PKA
- Block Ciphers combined with Hashing
  - Concurrent AES/ DES and SHA1/ MD5
  - SHA-1/ MD5 after AES/ DES

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2.2 FUNCTIONAL DESCRIPTION OF SSS

2.2.1 CPU MODE

Using the SFR, you can access the full functions of AES, DES, Hash, or PRNG. You can also supply the input data, trigger an operation, and extract the output data.

2.2.2 FIFO MODE

BRDMA supplies input data to block ciphers such as AES or DES, as shown in *Figure 2-2*. On the other hand, BTDMA receives output data from AES or DES. Only one block (either AES or DES) can use the DMA. The other block that does not occupy the DMA can be used in CPU or buffered CPU modes.

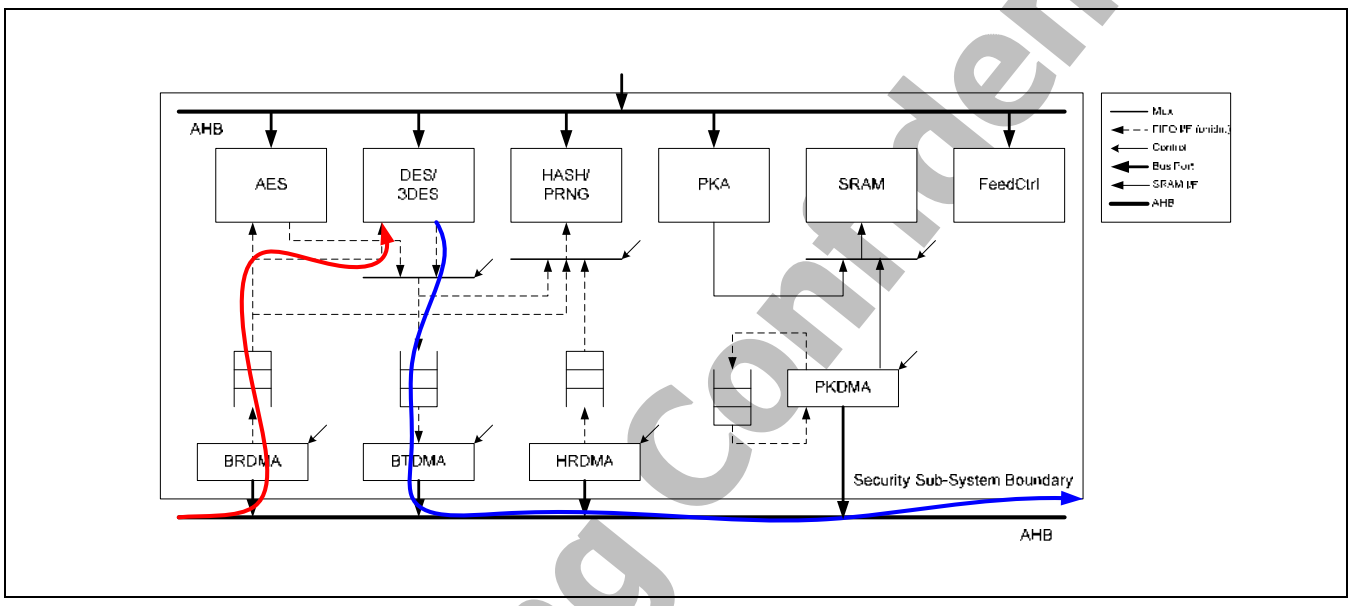

Figure 2-2 DES or 3DES Only Data Flow

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Figure 2-3 shows that the AES block uses BRDMA and BTDMA. The hash block uses HRDMA, which represents Hash Receiving DMA. HRDMA can work independently of BRDMA or BTDMA. In this case, the hash processes different data stream than block ciphers.

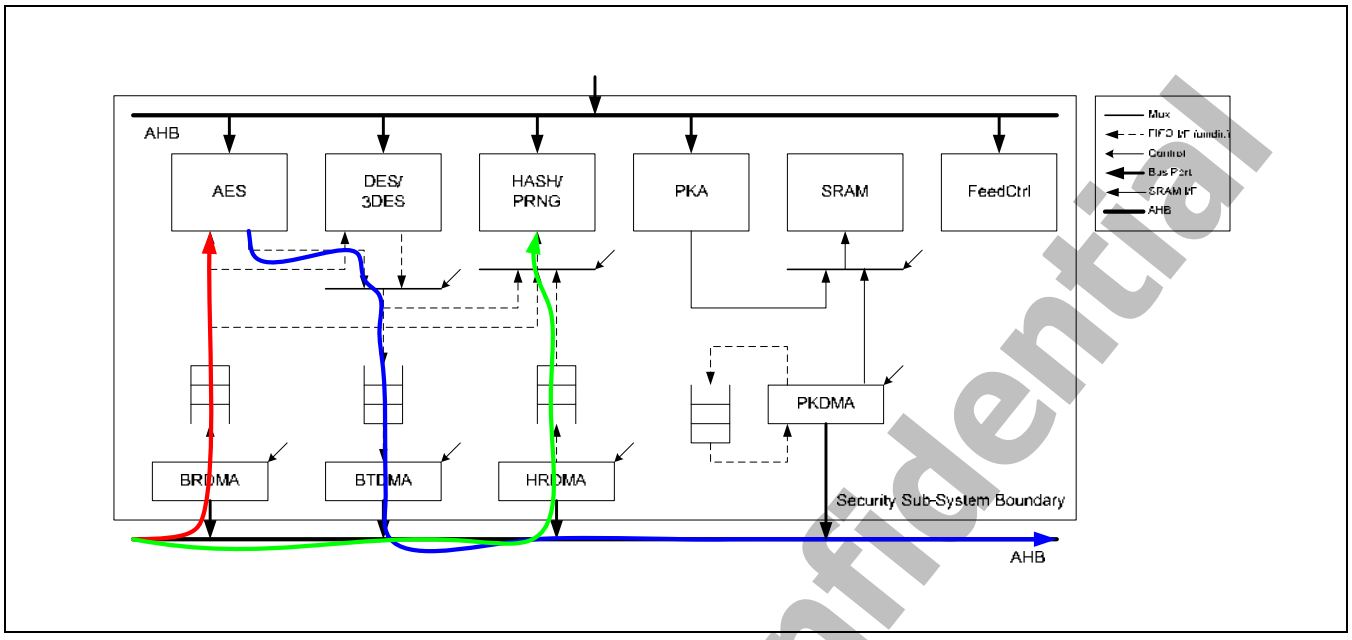

Figure 2-3 AES and Hash parallel data flow

Figure 2-4 shows the configuration of AES and hash with shared input data from external memory.

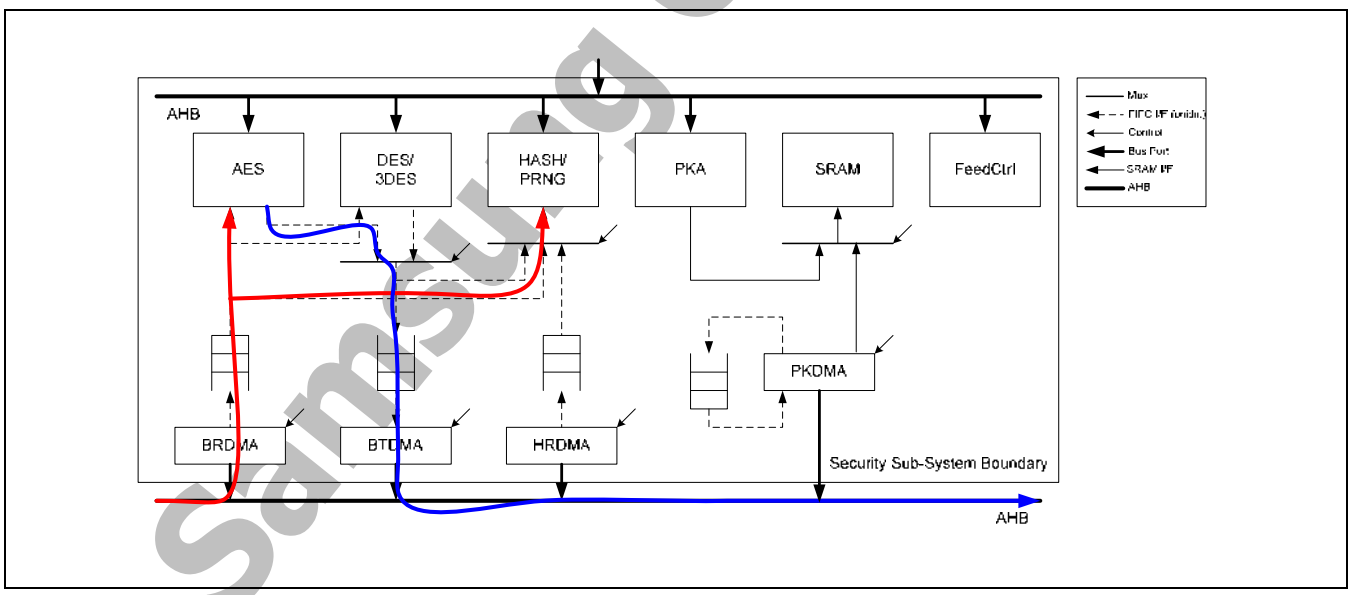

Figure 2-4 Data flow of AES and Hash with Shared Input

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Figure 2-5 shows the configuration of hash when it processes the output of AES.

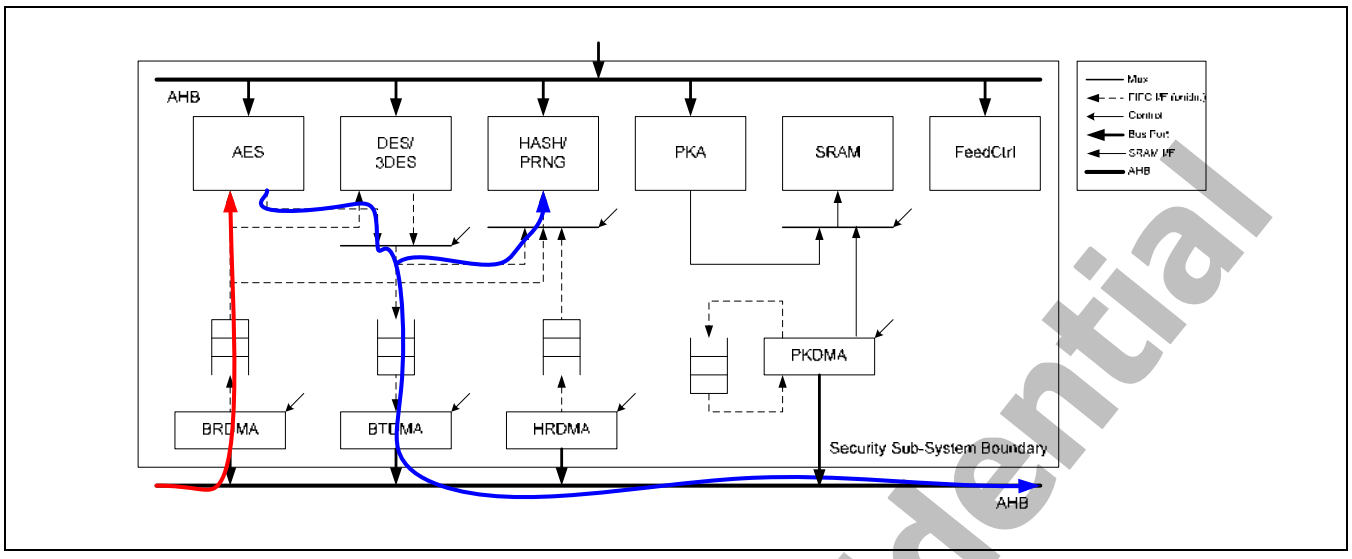

Figure 2-5 Data Flow of Hashing the Output of AES

For the above two cases, HRDMA cannot be used.

2.2.2.1 FIFO Configuration

The FCFIFOCTRL register affects FIFO configuration. The DESSEL bit of FCFIFOCTRL selects between DES and AES. Also, the HASHINSEL bits select hash input data from three possible inputs that comes from HRDMA, input of block cipher, and output of block cipher.

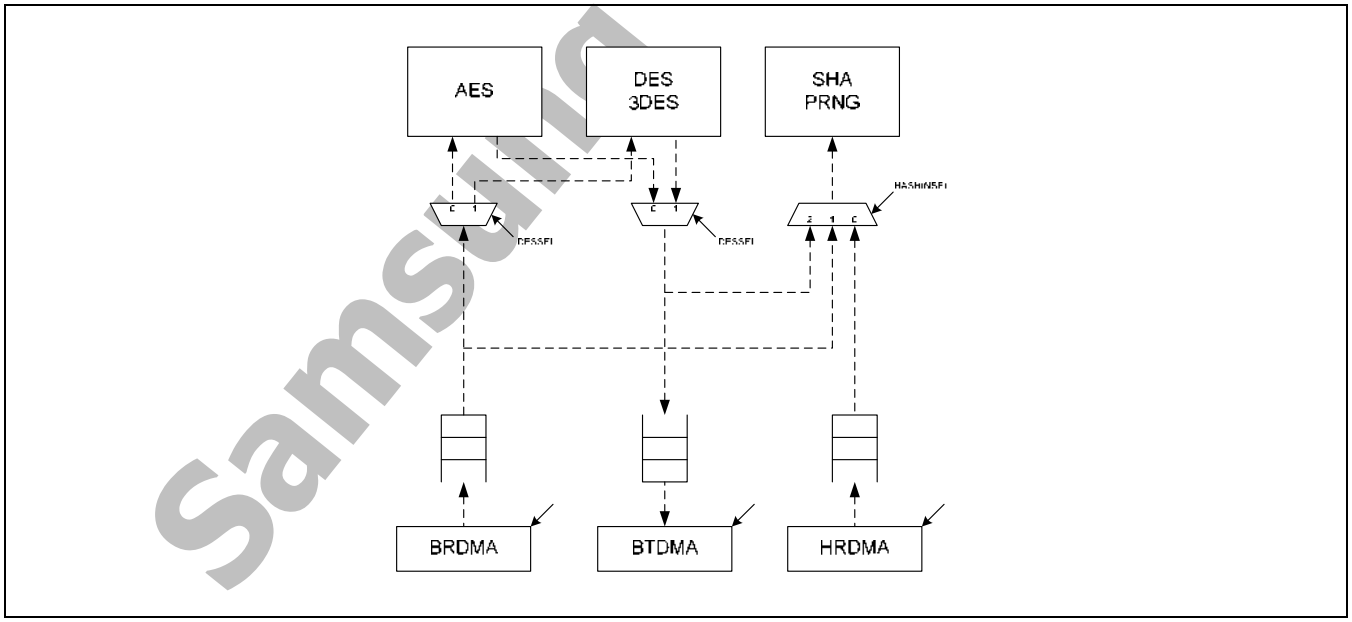

Figure 2-6 FIFO and FIFO Interconnections

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2.2.2.2 DMA Configuration

Each DMA has three main parameters, namely:

- STARTADDR (32-bit): Specifies the start address of DMA. The address does not need to be aligned by 32-bit. Its value increases by four after every transaction.
- LENGTH (32-bit): Specifies the block length of DMA. The length need not be aligned by 32-bit. Its value decreases by four after every transaction.
- FLUSH (1-bit): If this bit is high, then data flushes out from FIFO and DMA. After flushing, the start address keeps the stopped address and the length is 0. The flushing state should be released by writing value '0' to this bit.

2.2.2.3 Interrupt Controller (for DMA Interrupt)

Figure 2-7 shows the interrupt controller scheme for one interrupt signal. Each of the four DMA interrupt signals have the following control scheme, that is, each interrupt signal is generated by a DMA in pulse form and latched by the FCINTPEND register to form a level sensitive interrupt signal.

The latched signal is masked by FCINTENSET register in bit-by-bit form. Each bit in FCINTENSET can be set by writing '1' to the corresponding bit in FCINTENSET, and cleared by writing '1' to the corresponding bit in FCINTENCLR.

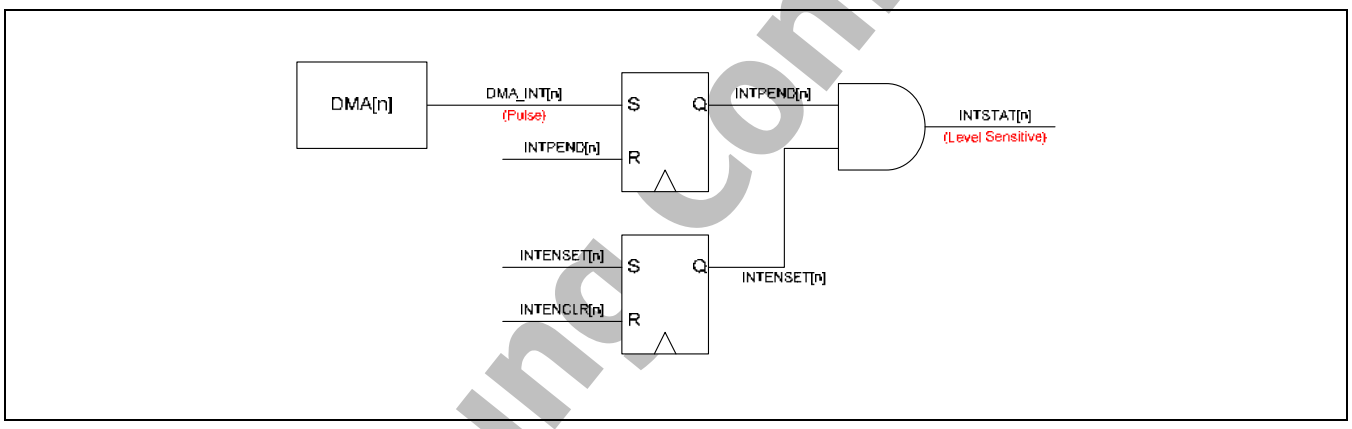

Figure 2-7 Interrupt Controller Scheme for one Interrupt Signal

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2.2.3 BYTE SWAPPING OPTIONS

SSS supports byte-swapping options for various data. Byte swapping in this context means byte order reversion in a 32-bit word boundary.

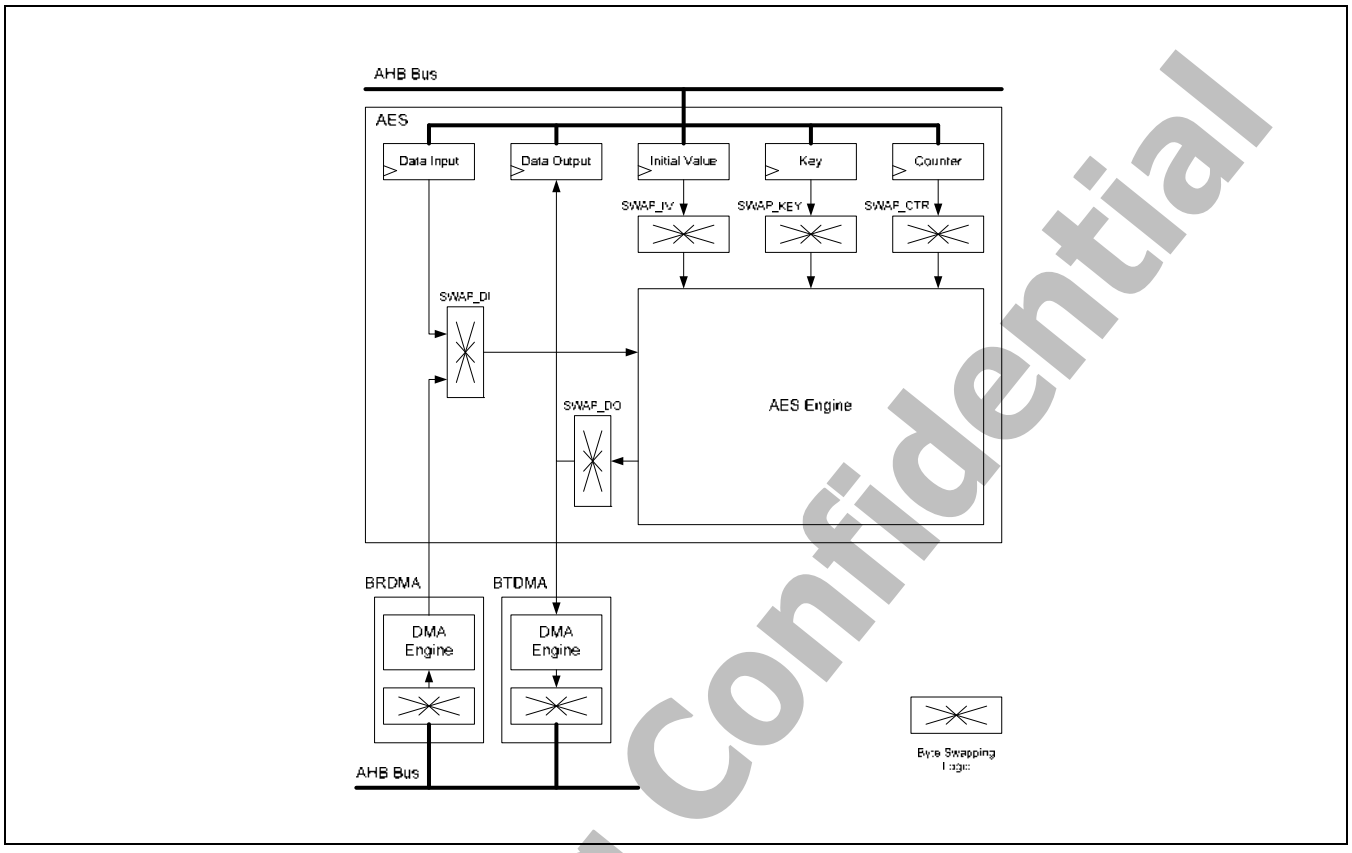

Figure 2-8 AES Byte Swapping Scheme

According to *Figure 2-8*, AES has five swapping options for every data (be it data input, data output, initial value, key, and counter).

Moreover, all DMA (BRDMA and BTDMA) have their own swapping option. The byte-swapping option of DMA should follow the bus endian.

1. For little endian bus, the DMA should swap data.
2. For big endian bus, the DMA should not swap data.

The only reason why option 2 must be used is that S5PV210 supports little endian case.

In case DES, Hash, and PKA contain different numbers of data, the same scheme will be applied.

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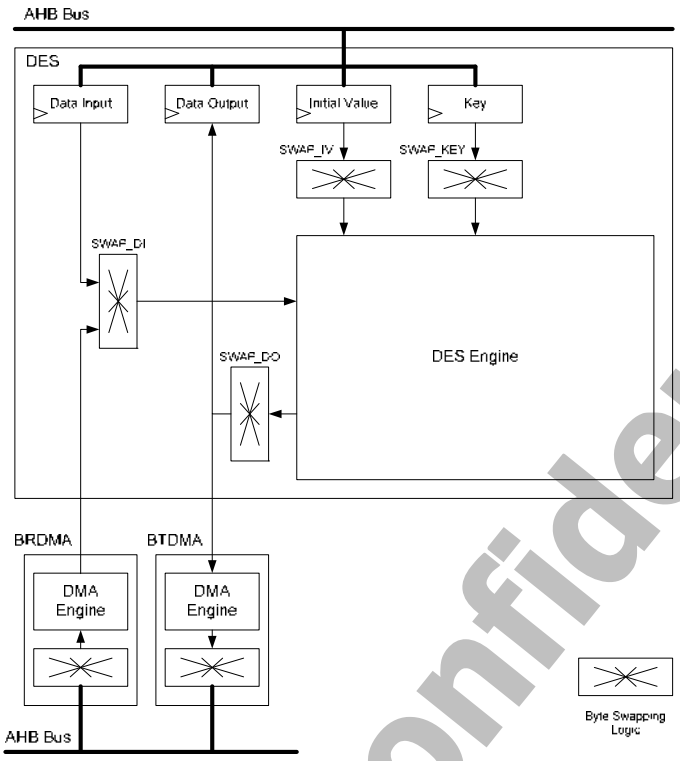

Figure 2-9 DES Byte Swapping Scheme

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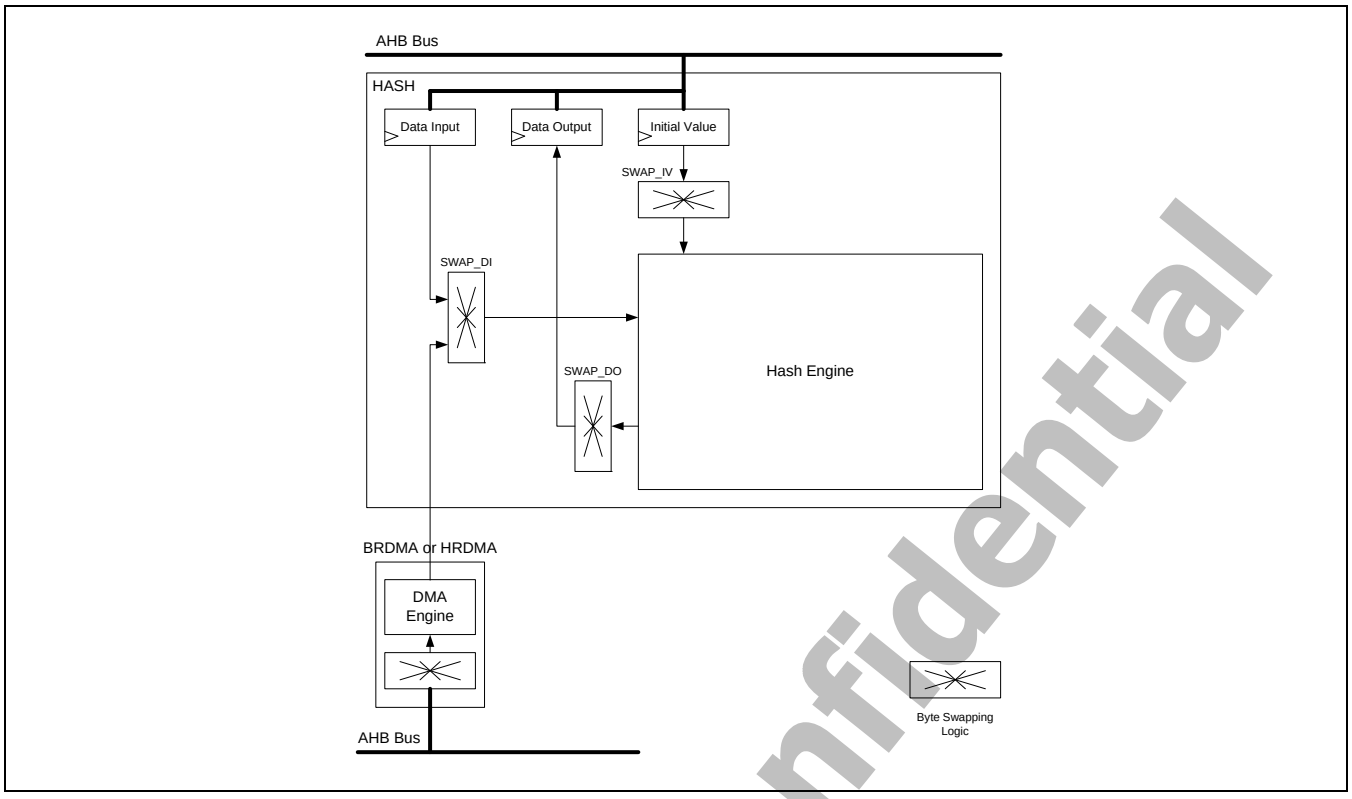

Figure 2-10 Hash Byte Swapping Scheme

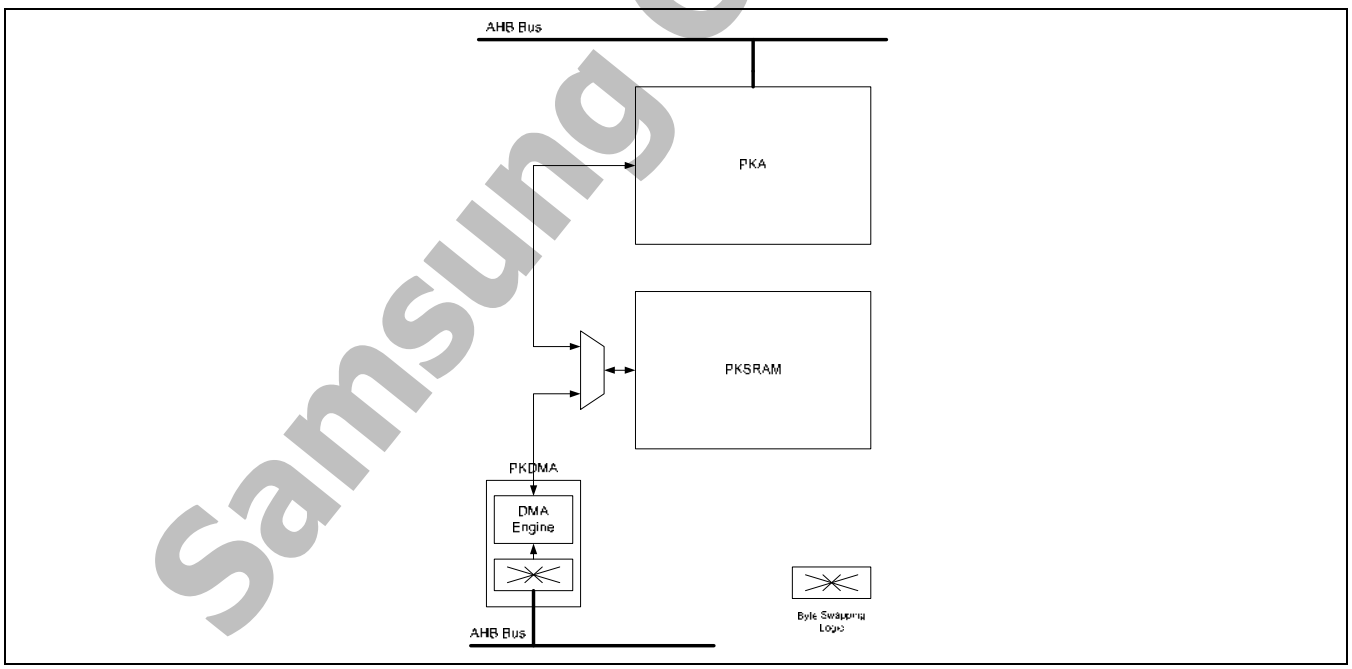

Figure 2-11 PKA Byte Swapping Scheme

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2.3 REGISTER DESCRIPTION

2.3.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
Feed				
FCINTSTAT	0xEA00_0000	R	Specifies the interrupt status of feed control.	0x0000_0000
FCINTENSET	0xEA00_0004	R/W	Specifies the interrupt enable set register of feed control. Value '1' should be written to set the corresponding bit.	0x0000_0000
FCINTENCLR	0xEA00_0008	R/W	Specifies the interrupt enable clear register of feed control. Value '1' should be written to clear the corresponding bit.	0x0000_0000
FCINTPEND	0xEA00_000C	R/W	Specifies the pending interrupts of feed control.	0x0000_0000
FCFIFOSTAT	0xEA00_0010	R	Specifies the FIFO status of feed control.	0x0000_0055
FCFIFOCTRL	0xEA00_0014	R/W	Specifies the FIFO control of feed control.	0x0000_0000
FCBRDMAS	0xEA00_0020	R/W	Specifies the start address of block cipher receiving DMA.	0x0000_0000
FCBRDMAL	0xEA00_0024	R/W	Specifies the length of block cipher receiving DMA.	0x0000_0000
FCBRDMAC	0xEA00_0028	R/W	Specifies the control of block cipher receiving DMA.	0x0000_0000
FCBTDMAS	0xEA00_0030	R/W	Specifies the start address of block cipher transmitting DMA.	0x0000_0000
FCBTDMAL	0xEA00_0034	R/W	Specifies the length of block cipher transmitting DMA.	0x0000_0000
FCBTDMAC	0xEA00_0038	R/W	Specifies the control of block cipher transmitting DMA.	0x0000_0000
FCHRDMAS	0xEA00_0040	R/W	Specifies the start address of hash receiving DMA.	0x0000_0000
FCHRDMAL	0xEA00_0044	R/W	Specifies the length of hash receiving DMA.	0x0000_0000
FCHRDMAC	0xEA00_0048	R/W	Specifies the control of hash receiving DMA.	0x0000_0000
FCPKDMAS	0xEA00_0050	R/W	Specifies the start address of PKA DMA.	0x0000_0000
FCPKDMAL	0xEA00_0054	R/W	Specifies the length of PKA DMA.	0x0000_0000
FCPKDMAC	0xEA00_0058	R/W	Specifies the control of PKA DMA.	0x0000_0000
FCPKDMAO	0xEA00_005C	R/W	Specifies the offset in PKA SRAM.	0x0000_0000
AES				
AES_control	0xEA00_4000	R/W	Specifies the AES control register.	0x0000_0000
AES_status	0xEA00_4004	R/W	Specifies the AES status register.	0x0000_0002

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Register	Address	R/W	Description	Reset Value
AES_indata_01	0xEA00_4010	W	Specifies the Input data to be used in encryption/decryption: [127:96].	0x0000_0000
AES_indata_02	0xEA00_4014	W	Specifies the Input data to be used in encryption/decryption: [95:64].	0x0000_0000
AES_indata_03	0xEA00_4018	W	Specifies the Input data to be used in encryption/decryption: [63:32].	0x0000_0000
AES_indata_04	0xEA00_401C	W	Specifies the Input data to be used in encryption/decryption: [31:0].	0x0000_0000
AES_outdata_01	0xEA00_4020	R	Specifies the Output data to be used in encryption/decryption: [127:96].	0x0000_0000
AES_outdata_02	0xEA00_4024	R	Specifies the Output data to be used in encryption/decryption: [95:64].	0x0000_0000
AES_outdata_03	0xEA00_4028	R	Specifies the Output data to be used in encryption/decryption: [63:32].	0x0000_0000
AES_outdata_04	0xEA00_402C	R	Specifies the Output data to be used in encryption/decryption: [31:0].	0x0000_0000
AES_ivdata_01	0xEA00_4030	W	Specifies the Initialization vector to be used in encryption/decryption: [127:96].	0x0000_0000
AES_ivdata_02	0xEA00_4034	W	Specifies the Initialization vector to be used in encryption/decryption: [95:64].	0x0000_0000
AES_ivdata_03	0xEA00_4038	W	Specifies the Initialization vector to be used in encryption/decryption: [63:32].	0x0000_0000
AES_ivdata_04	0xEA00_403C	W	Specifies the Initialization vector to be used in encryption/decryption: [31:0].	0x0000_0000
AES_cntdata_01	0xEA00_4040	W	Specifies the Counter data be used in encryption/decryption: [127:96].	0x0000_0000
AES_cntdata_02	0xEA00_4044	W	Specifies the Counter data to be used in encryption/decryption: [95:64].	0x0000_0000
AES_cntdata_03	0xEA00_4048	W	Specifies the Counter data to be used in encryption/decryption: [63:32].	0x0000_0000
AES_cntdata_04	0xEA00_404C	W	Specifies the Counter data to be used in encryption/decryption: [31:0].	0x0000_0000
AES_keydata_01	0xEA00_4080	W	Specifies the Key data to be used in encryption/decryption: [255:224].	0x0000_0000
AES_keydata_02	0xEA00_4084	W	Specifies the Key data to be used in encryption/decryption: [223:192].	0x0000_0000
AES_keydata_03	0xEA00_4088	W	Specifies the Key data to be used in encryption/decryption: [191:160].	0x0000_0000
AES_keydata_04	0xEA00_408C	W	Specifies the Key data to be used in encryption/decryption: [159:128].	0x0000_0000
AES_keydata_05	0xEA00_4090	W	Specifies the Key data to be used in encryption/decryption: [127:96].	0x0000_0000

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Register	Address	R/W	Description	Reset Value
AES_keydata_06	0xEA00_4094	W	Specifies the Key data to be used in encryption/decryption: [95:64].	0x0000_0000
AES_keydata_07	0xEA00_4098	W	Specifies the Key data to be used in encryption/decryption: [63:32].	0x0000_0000
AES_keydata_08	0xEA00_409C	W	Specifies the Key data to be used in encryption/decryption : [31:0].	0x0000_0000
TDES				
TDES_CONF	0xEA00_5000	R/W	Specifies the TDES configuration register.	0x0000_0000
TDES_STAT	0xEA00_5004	R/W	Specifies the TDES status register.	0x0000_0002
TDES_KEY1_0	0xEA00_5010	W	Specifies the TDES Input Key 1 [63:32].	0x0000_0000
TDES_KEY1_1	0xEA00_5014	W	Specifies the TDES Input Key 1 [31:0].	0x0000_0000
TDES_KEY2_0	0xEA00_5018	W	Specifies the TDES Input Key 2 [63:32].	0x0000_0000
TDES_KEY2_1	0xEA00_501C	W	Specifies the TDES Input Key 2 [31:0].	0x0000_0000
TDES_KEY3_0	0xEA00_5020	W	Specifies the TDES Input Key 3 [63:32].	0x0000_0000
TDES_KEY3_1	0xEA00_5024	W	Specifies the TDES Input Key 3 [31:0].	0x0000_0000
TDES_IV_0	0xEA00_5028	W	Specifies the TDES Initial vector [63:32].	0x0000_0000
TDES_IV_1	0xEA00_502C	W	Specifies the TDES Initial vector [31:0].	0x0000_0000
TDES_INPUT_0	0xEA00_5030	W	Specifies the TDES Input Data [63:32].	0x0000_0000
TDES_INPUT_1	0xEA00_5034	W	Specifies the TDES Input Data [31:0].	0x0000_0000
TDES_OUTPUT_0	0xEA00_5038	R	Specifies the TDES output Data [63:32].	0x0000_0000
TDES_OUTPUT_1	0xEA00_503C	R	Specifies the TDES output Data [31:0].	0x0000_0000
HASH and PRNG				
HASH_CONTROL_1	0xEA00_6000	R/W	Specifies the hash control register 1.	0x0000_0000
HASH_CONTROL_2	0xEA00_6004	W	Specifies the hash control register 2.	0x0000_0000
HASH_FIFO_MODE_EN	0xEA00_6008	R/W	Enables FIFO mode.	0x0000_0000
HASH_BYTE_SWAP	0xEA00_600C	R/W	Specifies the byte swap configuration register.	0x0000_0000
HASH_STATUS	0xEA00_6010	R	Specifies the status register.	0x0000_0001
HASH_MSG_SIZE_LOW	0xEA00_6014	R/W	Specifies the message size in bytes (lower 32-bits).	0x0000_0000
HASH_MSG_SIZE_HIGH	0xEA00_6018	R/W	Specifies the message size in bytes (higher 32-bits).	0x0000_0000
HASH_DATA_IN_1	0xEA00_6020	W	Specifies the key/message input register 1. Only effective when the FIFO mode is disabled.	-

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Register	Address	R/W	Description	Reset Value
HASH_DATA_IN_2	0xEA00_6024	W	Specifies the key/message input register 2. Only effective when the FIFO mode is disabled.	-
HASH_DATA_IN_3	0xEA00_6028	W	Specifies the key/message input register 3. Only effective when the FIFO mode is disabled.	-
HASH_DATA_IN_4	0xEA00_602C	W	Specifies the key/message input register 4. Only effective when the FIFO mode is disabled.	-
HASH_DATA_IN_5	0xEA00_6030	W	Specifies the key/message input register 5. Only effective when the FIFO mode is disabled.	-
HASH_DATA_IN_6	0xEA00_6034	W	Specifies the key/message input register 6. Only effective when the FIFO mode is disabled.	-
HASH_DATA_IN_7	0xEA00_6038	W	Specifies the key/message input register 7. Only effective when the FIFO mode is disabled.	-
HASH_DATA_IN_8	0xEA00_603C	W	Specifies the key/message input register 8. Only effective when the FIFO mode is disabled.	-
HASH_SEED_IN_1	0xEA00_6040	W	Specifies the PRNG seed data input 1.	-
HASH_SEED_IN_2	0xEA00_6044	W	Specifies the PRNG seed data input 2.	-
HASH_SEED_IN_3	0xEA00_6048	W	Specifies the PRNG seed data input 3.	-
HASH_SEED_IN_4	0xEA00_604C	W	Specifies the PRNG seed data input 4.	-
HASH_SEED_IN_5	0xEA00_6050	W	Specifies the PRNG seed data input 5.	-
HASH_RESULT_1	0xEA00_6060	R	Specifies the Hash/HMAC/Partial result 1.	0x6745_2301
HASH_RESULT_2	0xEA00_6064	R	Specifies the Hash/HMAC/Partial result 2.	0xefcd_ab89
HASH_RESULT_3	0xEA00_6068	R	Specifies the Hash/HMAC/Partial result 3.	0x98ba_dcfe
HASH_RESULT_4	0xEA00_606C	R	Specifies the Hash/HMAC/Partial result 4.	0x1032_5476
HASH_RESULT_5	0xEA00_6070	R	Specifies the Hash/HMAC/Partial result 5.	0xc3d2_e1f0
HASH_PRNG_1	0xEA00_6080	R	Specifies the PRNG output 1.	0x0000_0000
HASH_PRNG_2	0xEA00_6084	R	Specifies the PRNG output 2.	0x0000_0000
HASH_PRNG_3	0xEA00_6088	R	Specifies the PRNG output 3.	0x0000_0000
HASH_RESULT_4	0xEA00_606C	R	Specifies the Hash/HMAC/Partial result 4.	0x1032_5476
HASH_PRNG_5	0xEA00_6090	R	Specifies the PRNG output 5.	0x0000_0000
HASH_IV_1	0xEA00_60A0	W	Specifies the Custom IV input 1.	-
HASH_IV_2	0xEA00_60A4	W	Specifies the Custom IV input 2.	-
HASH_IV_3	0xEA00_60A8	W	Specifies the Custom IV input 3.	-
HASH_IV_4	0xEA00_60AC	W	Specifies the Custom IV input 4.	-

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Register	Address	R/W	Description	Reset Value
HASH_IV_5	0xEA00_60B0	W	Specifies the Custom IV input 5.	-
HASH_PRE_MSG_LENG_HIGH	0xEA00_60C0	W	Specifies the Pre-message length [63:32].	0
HASH_PRE_MSG_LENG_LOW	0xEA00_60C4	W	Specifies the Pre-message length [31:0].	0
PKA				
PKA_SFR0	0xEA00_7000	R/W	CHNK_SZ / PREC_ID	0x0000_0000
PKA_SFR1	0xEA00_7004	R/W	PLDM_ON / EXEC_ON	0x0000_0000
PKA_SFR2	0xEA00_7008	R/W	SEG_ID (A, B, M, S)	0x0000_0000
PKA_SFR3	0xEA00_700C	R/W	SEG_SIGN	0x0000_0000
PKA_SFR4	0xEA00_7010	R/W	SEG_SIZE, FUNC_ID	0x0000_0000

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2.3.1.1 Feed Control (FCINTSTAT, R, Address = 0xEA00_0000)

FCINTSTAT	Bit	Description	R/W	Initial State
Reserved	[31:4]	Reserved		0
BRDMAINT	[3]	Specifies the interrupt signal of block cipher receiving DMA.		0
BTDMAINT	[2]	Specifies the interrupt signal of block cipher transmitting DMA.		0
HRDMAINT	[1]	Specifies the interrupt signal of hash receiving DMA.		0
PKDMAINT	[0]	Specifies the interrupt signal of PKA DMA.		0

2.3.1.2 Feed Control (FCINTENSET, R/W, Address = 0xEA00_0004)

FCINTENSET	Bit	Description	R/W	Initial State
Reserved	[31:4]	Reserved		0
BRDMAINTENSET	[3]	Specifies the interrupt enable set signal of block cipher receiving DMA.		0
BTDMAINTENSET	[2]	Specifies the interrupt enable set signal of block cipher transmitting DMA.		0
HRDMAINTENSET	[1]	Specifies the interrupt enable set signal of hash receiving DMA.		0
PKDMAINTENSET	[0]	Specifies the interrupt enable signal of PKA DMA.		0

2.3.1.3 Feed Control (FCINTENCLR, R/W, Address = 0xEA00_0008)

FCINTENCLR	Bit	Description	R/W	Initial State
Reserved	[31:4]	Reserved		0
BRDMAINTENCLR	[3]	Specifies the interrupt enable clear signal of block cipher receiving DMA.		0
BTDMAINTENCLR	[2]	Specifies the interrupt enable clear signal of block cipher transmitting DMA.		0
HRDMAINTENCLR	[1]	Specifies the interrupt enable clear signal of hash receiving DMA.		0
PKDMAINTENCLR	[0]	Specifies the interrupt enable clear signal of PKA DMA.		0

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2.3.1.4 Feed Control (FCINTPEND, R/W, Address = 0xEA00_000C)

FCINTPEND	Bit	Description	R/W	Initial State
Reserved	[31:4]	Reserved		0
BRDMAINTP	[3]	Specifies the Pending Interrupt signal of Block cipher Receiving DMA.		0
BTDMAINTP	[2]	Specifies the Pending Interrupt signal of Block cipher Transmitting DMA.		0
HRDMAINTP	[1]	Specifies the Pending Interrupt signal of Hash Receiving DMA.		0
PKDMAINTP	[0]	Specifies the Pending Interrupt signal of PKA DMA.		0

2.3.1.5 Feed Control (FCFIFOSTAT, R, Address = 0xEA00_0010)

FCFIFOSTAT	Bit	Description	R/W	Initial State
Reserved	[31:8]	Reserved		0
BRFIFOFUL	[7]	Specifies the Full state of Block cipher Receiving FIFO.		0
BRFIFOEMP	[6]	Specifies the Empty state of Block cipher Receiving FIFO.		1
BTFIFOFUL	[5]	Specifies the Full state of Block cipher Transmitting FIFO.		0
BTFIFOEMP	[4]	Specifies the Empty state of Block cipher Transmitting FIFO.		1
HRFIFOFUL	[3]	Specifies the Full state of Hash Receiving FIFO.		0
HRFIFOEMP	[2]	Specifies the Empty state of Hash Receiving FIFO.		1
PKFIFOFUL	[1]	Specifies the Full state of PKA FIFO.		0
PKFIFOEMP	[0]	Specifies the Empty state of PKA FIFO.		1

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2.3.1.6 Feed Control (FCFIFOCTRL, R/W, Address = 0xEA00_0014)

FCFIFOCTRL	Bit	Description	R/W	Initial State
Reserved	[31:3]	Reserved		0
DESSEL	[2]	Specifies the Destination block cipher of FIFO. AES(=0)/DES(=1)		0
HASHINSEL	[1:0]	Specifies the following: Data from independent source (0) Data from block cipher input (1) Data from block cipher output (2) Reserved (3)		0

2.3.1.7 Feed Control (FCBRDMAS, R/W, Address = 0xEA00_0020)

FCBRDMAS	Bit	Description	R/W	Initial State
STARTADDR	[31:0]	Specifies the Start Address of DMA. The address does not to be aligned by 32-bit. Its value increases by 4 after every transaction.		0

2.3.1.8 Feed Control (FCBRDMAL, R/W, Address = 0xEA00_0024)

FCBRDMAL	Bit	Description	R/W	Initial State
LENGTH	[31:0]	Specifies the Block length of DMA. The length does not to be aligned by 32-bit. Its value decreases by 4 after every transaction.		0

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2.3.1.9 Feed Control (FCBRDMAC, R/W, Address = 0xEA00_0028)

FCBRDMAC	Bit	Description	R/W	Initial State
Reserved	[31:2]	Reserved		0
BYTESWAP	[1]	If this bit is high, then the data read from the bus is byte-swapped in a word boundary. If this bit is low (default), then the data is handed over to the FIFO without byte-swap. For little endian bus, this bit should be '1'.		0
FLUSH	[0]	If this bit is high, then data flushes out from FIFO and DMA. After flushing, the start address keeps the stopped address, and the length is 0. The flushing state should be released by writing value '0' to this bit.		0

2.3.1.10 Feed Control (FCBTDMAS, R/W, Address = 0xEA00_0030)

FCBTDMAS	Bit	Description	R/W	Initial State
STARTADDR	[31:0]	Specifies the Start Address of DMA. The address needs not to be aligned by 32-bit. Its value increases by 4 after every transaction.		0

2.3.1.11 Feed Control (FCBTDMAL, R/W, Address = 0xEA00_0034)

FCBTDMAL	Bit	Description	R/W	Initial State
LENGTH	[31:0]	Specifies the Block length of DMA. The length needs not to be aligned by 32-bit. Its value decreases by 4 after every transaction.		0

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2.3.1.12 Feed Control (FCBTDMAC, R/W, Address = 0xEA00_0038)

FCBTDMAC	Bit	Description	R/W	Initial State
Reserved	[31:2]	Reserved		0
BYTESWAP	[1]	If this bit is high, then the data written to the bus is byte-swapped in a word boundary. If this bit is low (default), then the data is handed over to the FIFO without byte-swap. For little endian bus, this bit should be '1'.		0
FLUSH	[0]	If this bit is high, then data flushes out from FIFO and DMA. After flushing, the start address keeps the stopped address, and the length is 0. The flushing state should be released by writing value '0' to this bit.		0

2.3.1.13 Feed Control (FCHRDMAS, R/W, Address = 0xEA00_0040)

FCHRDMAS	Bit	Description	R/W	Initial State
STARTADDR	[31:0]	Specifies the Start Address of DMA. The address does not to be aligned by 32-bit. Its value increases by 4 after every transaction.		0

2.3.1.14 Feed Control (FCHRDMAL, R/W, Address = 0xEA00_0044)

FCHRDMAL	Bit	Description	R/W	Initial State
LENGTH	[31:0]	Specifies the Block length of DMA. The length needs not to be aligned by 32-bit. Its value decreases by 4 after every transaction.		0

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2.3.1.15 Feed Control (FCHRDMAC, R/W, Address = 0xEA00_0048)

FCHRDMAC	Bit	Description	R/W	Initial State
Reserved	[31:2]	Reserved		0
BYTESWAP	[1]	If this bit is high, then the data read from the bus is byte-swapped in a word boundary. If this bit is low (default), then the data is handed over to the FIFO without byte-swap. For little endian bus, this bit should be '1'.		0
FLUSH	[0]	If this bit is high, then data flushes out from FIFO and DMA. After flushing, the start address keeps the stopped address, and the length is 0. The flushing state should be released by writing value '0' to this bit.		0

2.3.1.16 Feed Control (FCPKDMAS, R/W, Address = 0xEA00_0050)

FCPKDMAS	Bit	Description	R/W	Initial State
STARTADDR	[31:0]	Specifies the Start Address of DMA. The address needs to be aligned by 32-bit. Its value increases by 4 after every transaction.		0

2.3.1.17 Feed Control (FCPKDMAL, R/W, Address = 0xEA00_0054)

FCPKDMAL	Bit	Description	R/W	Initial State
LENGTH	[31:0]	Specifies the Block length of DMA. The length needs to be aligned by 32-bit. Its value decreases by 4 after every transaction.		0

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2.3.1.18 Feed Control (FCPKDMAC, R/W, Address = 0xEA00_0058)

FCPKDMAC	Bit	Description	R/W	Initial State
Reserved	[31:4]	Reserved		0
BYTESWAP	[3]	If this bit is high, then the data read from or written to the bus is byte-swapped in a word boundary. If this bit is low (default), then the data is handed over to the FIFO without byte-swap.		0
DESCEND	[2]	If this bit is low (default), then offset value in FCPKDMAO increases by 4 after every transfer. If this bit is high, then offset value in FCPKDMAO decreases by 4 after every transfer.		0
TRANSMIT	[1]	Selects receiving (0) or transmitting (1).		0
FLUSH	[0]	If this bit is high, then data flushes out from FIFO and DMA. After flushing, the start address keeps the stopped address, and the length is 0. The flushing state should be released by writing value ‘0’ to this bit.		0

2.3.1.19 Feed Control (FCPKDMAO, R/W, Address = 0xEA00_005C)

FCPKDMAO	Bit	Description	R/W	Initial State
Reserved	[31:12]	Reserved		0
SRAMOFFSET	[11:0]	Specifies the Address offset in PKA SRAM. The address needs to be aligned by 32-bit. Its value increases by 4 after every transfer (decreases by 4, if DESCEND in FCPKDMAC is high).		0

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2.3.1.20 AES Control (AES_control, R/W, Address = 0xEA00_4000)

AES_control	Bit	Description	R/W	Initial State
Reserved	[31:12]	-	-	-
AES_ByteSwap_DI	[11]	0 = Disables Input data byte swap 1 = Enables Input data byte swap	R/W	
AES_ByteSwap_DO	[10]	0 = Disables Output data byte swap 1 = Enables Output data byte swap	R/W	
AES_ByteSwap_IV	[9]	0 = Disables Initial value byte swap 1 = Enables Initial value byte swap	R/W	
AES_ByteSwap_CNT	[8]	0 = Disables Counter data byte swap 1 = Enables Counter data byte swap	R/W	
AES_ByteSwap_Key	[7]	0 = Disables Key byte swap 1 = Enables Key byte swap	R/W	
Key Change Mode	[6]	Specifies the AES key change mode selection signal. 0 = Key is not changed 1 = Key is changed		0
AES Key Size	[5:4]	Specifies the AES key size selection signal. 00 = 128-bit key 01 = 192-bit key 10 = 256-bit key		00
FIFO Mode	[3]	Specifies the ARM/ FIFO mode selection signal. 0 = ARM mode (ARM Slave) 1 = FIFO mode		0
AES Chain Mode	[2:1]	Specifies the AES chain mode selection signal. 00 = ECB mode 01 = CBC mode 10 = CTR mode		00
AES Mode	[0]	Specifies the Encryption/ Decryption mode selection signal. 0 = Encryption 1 = Decryption		0

NOTE:

1. AES_control[0]: In case of CTR mode, AES core should always work in encryption mode, even in decryption. Therefore, AES_control[0] should always be '0'.
2. AES_control[6]: The Key Change Mode Bit is used if the key is exactly the same as it was before decryption or encryption. If the AES_control[6] is high, this means the key changes for every block, which consumes double the time of decryption. If a new key should be applied, at least the first block should be processed with AES_control[6] high.

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2.3.1.21 AES Control (AES_status, R/W, Address = 0xEA00_4004)

AES_status	Bit	Description	R/W	Initial State
Reserved	[31:3]	-	-	-
Busy	[2]	Specifies the AES busy signal. 0 = Idle 1 = Busy		0
Input Ready	[1]	Specifies the AES input ready signal. 0 = AES input buffer is not empty 1 = AES input buffer is empty, and the host is permitted to write the next block of data		1
Output Ready	[0]	Specifies the AES output ready signal. 0 = AES output is not available 1 = AES output is available to the host for retrieval		0

NOTE: To clear the Output Ready bit, write 0x1 at that bit, AES_status[0].

2.3.1.22 AES Control (AES_indata_01, W, Address = 0xEA00_4010)

AES_indata_01	Bit	Description	R/W	Initial State
AES_indata_01	[31:0]	Specifies the Input data [127:96].		0

2.3.1.23 AES Control (AES_indata_02, W, Address = 0xEA00_4014)

AES_indata_02	Bit	Description	R/W	Initial State
AES_indata_02	[31:0]	Specifies the Input data [95:64].		0

2.3.1.24 AES Control (AES_indata_03, W, Address = 0xEA00_4018)

AES_indata_03	Bit	Description	R/W	Initial State
AES_indata_03	[31:0]	Specifies the Input data [63:32].		0

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2.3.1.25 AES Control (AES_indata_04, W, Address = 0xEA00_401C)

AES_indata_04	Bit	Description	R/W	Initial State
AES_indata_04	[31:0]	Specifies the Input data [31:0].		0

2.3.1.26 AES Control (AES_outdata_01, R, Address = 0xEA00_4020)

AES_outdata_01	Bit	Description	R/W	Initial State
AES_outdata_01	[31:0]	Specifies the Output data [127:96].		0

2.3.1.27 AES Control (AES_outdata_02, R, Address = 0xEA00_4024)

AES_outdata_02	Bit	Description	R/W	Initial State
AES_outdata_02	[31:0]	Specifies the Output data [95:64].		0

2.3.1.28 AES Control (AES_outdata_03, R, Address = 0xEA00_4028)

AES_outdata_03	Bit	Description	R/W	Initial State
AES_outdata_03	[31:0]	Specifies the Output data [63:32].		0

2.3.1.29 AES Control (AES_outdata_04, R, Address = 0xEA00_402C)

AES_outdata_04	Bit	Description	R/W	Initial State
AES_outdata_04	[31:0]	Specifies the Output data [31:0].		0

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2.3.1.30 AES Control (AES_ivdata_01, W, Address = 0xEA00_4030)

AES_ivdata_01	Bit	Description	R/W	Initial State
AES_ivdata_01	[31:0]	Specifies the Initialization vector [127:96].		0

2.3.1.31 AES Control (AES_ivdata_02, W, Address = 0xEA00_4034)

AES_ivdata_02	Bit	Description	R/W	Initial State
AES_ivdata_02	[31:0]	Specifies the Initialization vector [95:64].		0

2.3.1.32 AES Control (AES_ivdata_03, W, Address = 0xEA00_4038)

AES_ivdata_03	Bit	Description	R/W	Initial State
AES_ivdata_03	[31:0]	Specifies the Initialization vector [63:32].		0

2.3.1.33 AES Control (AES_ivdata_04, W, Address = 0xEA00_403C)

AES_ivdata_04	Bit	Description	R/W	Initial State
AES_ivdata_04	[31:0]	Specifies the Initialization vector [31:0].		0

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2.3.1.34 AES Control (AES_cntdata_01, W, Address = 0xEA00_4040)

AES_cntdata_01	Bit	Description	R/W	Initial State
AES_cntdata_01	[31:0]	Specifies the Counter data [127:96].		0

2.3.1.35 AES Control (AES_cntdata_02, W, Address = 0xEA00_4044)

AES_cntdata_02	Bit	Description	R/W	Initial State
AES_cntdata_02	[31:0]	Specifies the Counter data [95:64].		0

2.3.1.36 AES Control (AES_cntdata_03, W, Address = 0xEA00_4048)

AES_cntdata_03	Bit	Description	R/W	Initial State
AES_cntdata_03	[31:0]	Specifies the Counter data [63:32].		0

2.3.1.37 AES Control (AES_cntdata_04, W, Address = 0xEA00_404C)

AES_cntdata_04	Bit	Description	R/W	Initial State
AES_cntdata_04	[31:0]	Specifies the Counter data [31:0].		0

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2.3.1.38 AES Control (AES_keydata_01, W, Address = 0xEA00_4080)

AES_keydata_01	Bit	Description	R/W	Initial State
AES_keydata_01	[31:0]	Specifies the Input key data [255:224].		0

2.3.1.39 AES Control (AES_keydata_02, W, Address = 0xEA00_4084)

AES_keydata_02	Bit	Description	R/W	Initial State
AES_keydata_02	[31:0]	Specifies the Input key data [223:192].		0

2.3.1.40 AES Control (AES_keydata_03, W, Address = 0xEA00_4088)

AES_keydata_03	Bit	Description	R/W	Initial State
AES_keydata_03	[31:0]	Specifies the Input key data [191:160].		0

2.3.1.41 AES Control (AES_keydata_04, W, Address = 0xEA00_408C)

AES_keydata_04	Bit	Description	R/W	Initial State
AES_keydata_04	[31:0]	Specifies the Input key data [159:128].		0

2.3.1.42 AES Control (AES_keydata_05, W, Address = 0xEA00_4090)

AES_keydata_05	Bit	Description	R/W	Initial State
AES_keydata_05	[31:0]	Specifies the Input key data [127:96].		0

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2.3.1.43 AES Control (AES_keydata_06, W, Address = 0xEA00_4094)

AES_keydata_06	Bit	Description	R/W	Initial State
AES_keydata_06	[31:0]	Specifies the Input key data [95:64].		0

2.3.1.44 AES Control (AES_keydata_07, W, Address = 0xEA00_4098)

AES_keydata_07	Bit	Description	R/W	Initial State
AES_keydata_07	[31:0]	Specifies the Input key data [63:32].		0

2.3.1.45 AES Control (AES_keydata_08, W, Address = 0xEA00_409C)

AES_keydata_08	Bit	Description	R/W	Initial State
AES_keydata_08	[31:0]	Specifies the Input key data [31:0].		0

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2.3.1.46 TDES Control (TDES_CONF, R/W, Address = 0xEA00_5000)

TDES_CONF	Bit	Description	R/W	Initial State
Reserved	[31:10]	-	-	-
TDES_ByteSwap_DI	[9]	0 = Disables data input byte swap 1 = Enables data input byte swap	R/W	0
TDES_ByteSwap_DO	[8]	0 = Disables data output byte swap 1 = Enables data output byte swap	R/W	0
TDES_ByteSwap_IV	[7]	0 = Disables initial value byte swap 1 = Enables initial value byte swap	R/W	0
TDES_ByteSwap_Key	[6]	0 = Disables key byte swap 1 = Enables key byte swap	R/W	0
TDES_FiFo	[5]	0 = CPU 1 = FiFo	R/W	0
TDES_EEE	[4]	0 = TDES EDE mode 1 = TDES EEE mode	R/W	0
TDES_Select	[3]	0 = DES 1 = TDES	R/W	0
Reseved	[2]	-	-	-
TDES_Mode	[1]	0 = ECB mode 1 = CBC mode	R/W	0
TDES_Enc	[0]	0 = Encryption 1 = Decryption	R/W	0

2.3.1.47 TDES Control (TDES_STAT, R/W, Address = 0xEA00_5004)

TDES_CONF	Bit	Description	R/W	Initial State
Reserved	[31:3]	-	-	-
TDES_Busy	[2]	0 = Idle 1 = Busy	R	0
TDES_Ready	[1]	0 = Input buffer full 1 = Input buffer empty	R	1
TDES_Valid	[0]	0 = Output Invalid 1 = Output Valid	R/W	0

NOTE: To clear the TDES_Valid bit, write 0x1 at that bit, TDES_STAT[0].

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2.3.1.48 TDES Control (TDES_KEY1_0, W, Address = 0xEA00_5010)

TDES_KEY1_0	Bit	Description	R/W	Initial State
TDES_KEY1_0	[31:0]	Specifies the Input key 1 [63:32].		0

2.3.1.49 TDES Control (TDES_KEY1_1, W, Address = 0xEA00_5014)

TDES_KEY1_1	Bit	Description	R/W	Initial State
TDES_ KEY1_1	[31:0]	Specifies the Input key 1 [31:0].		0

2.3.1.50 TDES Control (TDES_KEY2_0, W, Address = 0xEA00_5018)

TDES_KEY2_0	Bit	Description	R/W	Initial State
TDES_KEY2_0	[31:0]	Specifies the Input key 2 [63:32].	W	0

2.3.1.51 TDES Control (TDES_KEY2_1, W, Address = 0xEA00_501C)

TDES_KEY2_1	Bit	Description	R/W	Initial State
TDES_KEY2_1	[31:0]	Input key 2 [31:0]	W	0

2.3.1.52 TDES Control (TDES_KEY3_0, W, Address = 0xEA00_5020)

TDES_KEY3_0	Bit	Description	R/W	Initial State
TDES_KEY3_0	[31:0]	Specifies the Input key 3 [63:32]	W	0

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2.3.1.53 TDES Control (TDES_KEY3_1, W, Address = 0xEA00_5024)

TDES_KEY3_1	Bit	Description	R/W	Initial State
TDES_KEY3_1	[31:0]	Specifies the Input key 3 [31:0].	W	0

2.3.1.54 TDES Control (TDES_IV_0, W, Address = 0xEA00_5028)

TDES_IV_0	Bit	Description	R/W	Initial State
TDES_IV_0	[31:0]	Specifies the Input Initial vector [63:32].	W	0

2.3.1.55 TDES Control (TDES_IV_1, W, Address = 0xEA00_502C)

TDES_IV_1	Bit	Description	R/W	Initial State
TDES_IV_1	[31:0]	Specifies the Input Initial vector [31:0].	W	0

2.3.1.56 TDES Control (TDES_INPUT_0, W, Address = 0xEA00_5030)

TDES_INPUT_0	Bit	Description	R/W	Initial State
TDES_INPUT_0	[31:0]	Specifies the Input data [63:32].	W	0

2.3.1.57 TDES Control (TDES_INPUT_1, W, Address = 0xEA00_5034)

TDES_INPUT_1	Bit	Description	R/W	Initial State
TDES_INPUT_1	[31:0]	Specifies the Input data [31:0].	W	0

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2.3.2 TDES CONTROL (TDES_OUTPUT_0, R, ADDRESS = 0XEA00_5038)

TDES_OUTPUT_0	Bit	Description	R/W	Initial State
TDES_OUTPUT_0	[31:0]	Specifies the Output data [63:32].	R	0

2.3.2.1 TDES Control (TDES_OUTPUT_1, R, Address = 0xEA00_503C)

TDES_OUTPUT_1	Bit	Description	R/W	Initial State
TDES_OUTPUT_1	[31:0]	Specifies the Output data [31:0].	R	0

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2.3.2.2 HASH and PRNG Control (HASH_CONTROL_1, R/W, Address = 0xEA00_6000)

HASH_CONTROL_1	Bit	Description	R/W	Initial State
Engine_Selection	[3:0]	4'b0000: SHA1_HASH 4'b0001: SHA1_HMAC_INNER 4'b1001: SHA1_HMAC_OUTER 4'b0010: MD5_HASH 4'b0011: MD5_HMAC_INNER 4'b1011: MD5_HMAC_OUTER 4'b0100: PRNG		0000
START_INIT_BIT	[4]	Starts/initializes the hash/HMAC/PRNG (software reset). Automatically cleared by hardware.		0
USER_IV_EN	[5]	Uses customized IV. Automatically cleared by hardware.		0

2.3.2.3 HASH and PRNG Control (HASH_CONTROL_2, W, Address = 0xEA00_6004)

HASH_CONTROL_2	Bit	Description	R/W	Initial State
HASH_PAUSE	[3]	Pauses a hash operation. Automatically cleared by hardware.		0

2.3.2.4 HASH and PRNG Control (HASH_FIFO_MODE_EN, R/W, Address = 0xEA00_6008)

HASH_FIFO_MODE_EN	Bit	Description	R/W	Initial State
HASH_FIFO_MODE_EN	[0]	0 = Disables FIFO mode (default) 1 = Enables FIFO mode		0

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2.3.2.5 HASH and PRNG Control (HASH_BYTE_SWAP, R/W, Address = 0xEA00_600C)

HASH_BYTE_SWAP	Bit	Description	R/W	Initial State
HASH_SWAP_DI	[3]	Specifies the Byte swap of data input. 0 = Does not swap (default) 1 = Swap		0
HASH_SWAP_DO	[2]	Specifies the Byte swap of data output (hash result). 0 = Does not swap (default) 1 = Swap		0
HASH_SWAP_IV	[1]	Specifies the Byte swap of custom IVs. 0 = Does not swap (default) 1 = Swap		0

NOTE:

1. If HASH_SWAP_DI or HASH_SWAP_IV is 0, data will enter the hash core in the same order as HWDATA [31:0]. Otherwise, the 32-bit word is byte-swapped before entering the hash core. Note that the hash core is designed with "big endian" in mind, so you should turn on byte swapping if the bus is little endian.
2. SHA1(abcd) = 81fe8bfe_87576c3e_cb22426f_8e578473_82917acf
   READ(HASH_RESULT_1) → HRDATA = 0x81fe8bfe (when HASH_SWAP_DO = 0)
   READ(HASH_RESULT_1) → HRDATA = 0xfe8bfe81 (when HASH_SWAP_DO = 1)
   MD5(abcd) = e2fc714c_4727ee93_95f324cd_2e7f331f
   READ(HASH_RESULT_1) → HRDATA = 0xe2fc714c (when HASH_SWAP_DO = 0)
   READ(HASH_RESULT_1) → HRDATA = 0x4c71fce2 (when HASH_SWAP_DO = 1)
3. You must correctly configure the byte swapping before starting a hash/HMAC operation. (This step is omitted in the example code for simplicity.)

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2.3.2.6 HASH and PRNG Control (HASH_STATUS, R, Address = 0xEA00_6010)

HASH_STATUS	Bit	Description	R/W	Initial State
BUFFER_READY	[0]	Specifies the status of the internal SHA1 buffer. 0 = Buffer is full. 1 = Buffer still has empty spaces (not full).		1
SEED_SETTING_DONE	[1]	1 = Seed setup is done. 0 = Seed setup is not done.		0
PRNG_BUSY	[2]	Specifies the PRNG engine status. 1 = Busy 0 = Idle		0
PARTIAL_DONE	[4]	[R/W] The partial result is done Write “1” in this bit to clear it.		0
PRNG_DONE	[5]	[R/W] PRNG is done Write “1” in this bit to clear it.		0
MSG_DONE	[6]	[R/W] Hash/HMAC is done Write “1” in this bit to clear it.		0
PRNG_ERROR	[7]	Specifies the PRNG error bit. This bit goes HIGH if a PRNG request occurs without a complete seed setup. In order to clear this bit, you must perform a complete seed setup operation.		0

2.3.2.7 HASH and PRNG Control (HASH_MSG_SIZE_LOW, R/W, Address = 0xEA00_6014)

HASH_MSG_SIZE_LOW	Bit	Description	R/W	Initial State
HASH_MSG_SIZE_LOW	[31:0]	Specifies the message size in bytes (lower 32-bits).		0

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2.3.2.8 HASH and PRNG Control (HASH_MSG_SIZE_HIGH, R/W, Address = 0xEA00_6018)

HASH_MSG_SIZE_HIGH	Bit	Description	R/W	Initial State
HASH_MSG_SIZE_HIGH	[31:0]	Specifies the message size in bytes (higher 32-bits).		0

2.3.2.9 HASH and PRNG Control (HASH_DATA_IN, W, Address = 0xEA00_6020~0xEA00_603C)

HASH_DATA_IN	Bit	Description	R/W	Initial State
HASH_DATA_IN	[31:0]	Specifies the key/message input register 1 ~ 8. Only effective when the FIFO mode is disabled. Supports burst up to 8 words.		-

2.3.2.10 HASH and PRNG Control (HASH_SEED_IN_1, W, Address = 0xEA00_6040)

HASH_SEED_IN_1	Bit	Description	R/W	Initial State
HASH_SEED_IN_1	[31:0]	Specifies the PRNG seed buffer [159:128].		-

2.3.2.11 HASH and PRNG Control (HASH_SEED_IN_2, W, Address = 0xEA00_6044)

HASH_SEED_IN_2	Bit	Description	R/W	Initial State
HASH_SEED_IN_2	[31:0]	Specifies the PRNG seed buffer [127:96].		-

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2.3.2.12 HASH and PRNG Control (HASH_SEED_IN_3, W, Address = 0xEA00_6048)

HASH_SEED_IN_3	Bit	Description	R/W	Initial State
HASH_SEED_IN_3	[31:0]	Specifies the PRNG seed buffer [95:64].		-

2.3.2.13 HASH and PRNG Control (HASH_SEED_IN_4, W, Address = 0xEA00_604C)

HASH_SEED_IN_4	Bit	Description	R/W	Initial State
HASH_SEED_IN_4	[31:0]	Specifies the PRNG seed buffer [63:32].		-

2.3.2.14 HASH and PRNG Control (HASH_SEED_IN_5, W, Address = 0xEA00_6050)

HASH_SEED_IN_5	Bit	Description	R/W	Initial State
HASH_SEED_IN_5	[31:0]	Specifies the PRNG seed buffer [31:0].		-

2.3.2.15 HASH and PRNG Control (HASH_RESULT_1, R, Address = 0xEA00_6060)

HASH_RESULT_1	Bit	Description	R/W	Initial State
HASH_RESULT_1	[31:0]	Specifies the Hash/HMAC/Partial result 1.		0x6745_2301

2.3.2.16 HASH and PRNG Control (HASH_RESULT_2, R, Address = 0xEA00_6064)

HASH_RESULT_2	Bit	Description	R/W	Initial State
HASH_RESULT_2	[31:0]	Specifies the Hash/HMAC/Partial result 2.		0xefcd_ab89

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2.3.2.17 HASH and PRNG Control (HASH_RESULT_3, R, Address = 0xEA00_6068)

HASH_RESULT_3	Bit	Description	R/W	Initial State
HASH_RESULT_3	[31:0]	Specifies the Hash/HMAC/Partial result 3.		0x98ba_dcfe

2.3.2.18 HASH and PRNG Control (HASH_RESULT_4, R, Address = 0xEA00_606C)

HASH_RESULT_4	Bit	Description	R/W	Initial State
HASH_RESULT_4	[31:0]	Specifies the Hash/HMAC/Partial result 4.		0x1032_5476

2.3.2.19 HASH and PRNG Control (HASH_RESULT_5, R, Address = 0xEA00_6070)

HASH_RESULT_5	Bit	Description	R/W	Initial State
HASH_RESULT_5	[31:0]	Specifies the Hash/HMAC/Partial result 5.		0xc3d2_e1f0

2.3.2.20 HASH and PRNG Control (HASH_PRNG_1, R, Address = 0xEA00_6080)

HASH_PRNG_1	Bit	Description	R/W	Initial State
HASH_PRNG_1	[31:0]	Specifies the PRNG output 1.		0

2.3.2.21 HASH and PRNG Control (HASH_PRNG_2, R, Address = 0xEA00_6084)

HASH_PRNG_2	Bit	Description	R/W	Initial State
HASH_PRNG_2	[31:0]	Specifies the PRNG output 2.		0

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2.3.2.22 HASH and PRNG Control (HASH_PRNG_3, R, Address = 0xEA00_6088)

HASH_PRNG_3	Bit	Description	R/W	Initial State
HASH_PRNG_3	[31:0]	Specifies the PRNG output 3.		0

2.3.2.23 HASH and PRNG Control (HASH_PRNG_4, R, Address = 0xEA00_608C)

HASH_PRNG_4	Bit	Description	R/W	Initial State
HASH_PRNG_4	[31:0]	Specifies the PRNG output 4.		0

2.3.2.24 HASH and PRNG Control (HASH_PRNG_5, R, Address = 0xEA00_6090)

HASH_PRNG_5	Bit	Description	R/W	Initial State
HASH_PRNG_5	[31:0]	Specifies the PRNG output 5.		0

2.3.2.25 HASH and PRNG Control (HASH_IV_1, W, Address = 0xEA00_60A0)

HASH_IV_1	Bit	Description	R/W	Initial State
HASH_IV_1	[31:0]	Specifies the Custom IV input 1.		-

2.3.2.26 HASH and PRNG Control (HASH_IV_2, W, Address = 0xEA00_60A4)

HASH_IV_2	Bit	Description	R/W	Initial State
HASH_IV_2	[31:0]	Specifies the Custom IV input 2.		-

2.3.2.27 HASH and PRNG Control (HASH_IV_3, W, Address = 0xEA00_60A8)

HASH_IV_3	Bit	Description	R/W	Initial State
HASH_IV_3	[31:0]	Specifies the Custom IV input 3.		-

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2.3.2.28 HASH and PRNG Control (HASH_IV_4, W, Address = 0xEA00_60AC)

HASH_IV_4	Bit	Description	R/W	Initial State
HASH_IV_4	[31:0]	Specifies the Custom IV input 4.		-

2.3.2.29 HASH and PRNG Control (HASH_IV_5, W, Address = 0xEA00_60B0)

HASH_IV_5	Bit	Description	R/W	Initial State
HASH_IV_5	[31:0]	Specifies the Custom IV input 5.		-

2.3.2.30 HASH and PRNG Control (HASH_PRE_MSG_LENG_HIGH, W, Address = 0xEA00_60C0)

HASH_PRE_MSG_LENG_HIGH	Bit	Description	R/W	Initial State
HASH_PRE_MSG_LENG_HIGH	[31:0]	Specifies the pre-message length [63:32].		0

2.3.2.31 HASH and PRNG Control (HASH_PRE_MSG_LENG_LOW, W, Address = 0xEA00_60C4)

HASH_PRE_MSG_LENG_LOW	Bit	Description	R/W	Initial State
HASH_PRE_MSG_LENG_LOW	[31:0]	Specifies the pre-message length [31:0].		0

NOTE:

1. **HASH_CONTROL_1**
   ENGINE_SELECTION, START_INIT_BIT and USER_IV_EN can be set at the same time.
   If custom IVs are used, HASH_IV_1 ~ HASH_IV_5 must be initialized before USER_IV_EN is set.
2. **HASH_CONTROL_2**
   LAST_WORD and LAST_BYTE_SEL[1:0] are removed from the register map. Instead, HASH_MSG_SIZE_LOW and HASH_MSG_SIZE_HIGH are added (see below).

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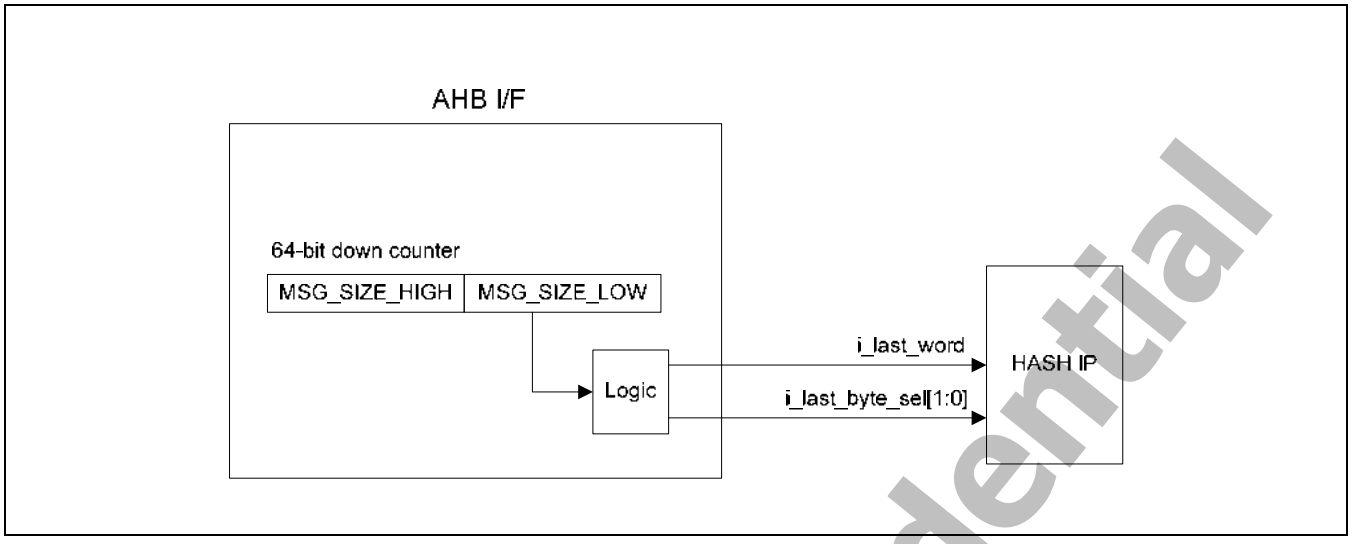
HASH_MSG_SIZE_LOW & HASH_MSG_SIZE_HIGH



As shown in the above diagram, the two registers form a 64-bit counter. When you write values into them, they are initialized with HWDATA. As data words are written through AHB or FIFO, the counter decreases by itself. When the counter is about to become zero, the internal logic generates correct “i_last_word” and “i_last_byte_sel” signals for the IP.

Note that the unit of this counter is byte. The maximum counting range is (264 – 1) bytes, which is large than specified in the SHA1 specification.

In certain cases, you can use HASH_MSG_SIZE_HIGH and HASH_MSG_SIZE_LOW. A typical example would be multi-part hashing (partial result is involved) without knowing the total message size in advance. In this case, you can initialize the counter with a “big” number (such as 64’h80000000_00000000) for all the parts except the last one. While processing the last part, through which the message will be known, you should initialize this counter with the real message size.

HASH_IV_1 ~ HASH_IV_5

The values in these five registers are sampled and saved by the hardware only when both USER_IV_EN (HASH_CONTROL_1[5]) and START_INIT_BIT (HASH_CONTROL_1[4]) are high. Since USER_IV_EN and START_INIT_BIT are automatically cleared by hardware, these five registers do not need to be cleared after they are used.

HASH_PRE_MSG_LENG_HIGH & HASH_PRE_MSG_LENG_LOW

In contrast to HASH_IV_1 ~ HASH_IV_5, these two registers always affect the hardware. Therefore, they must be set to zero when “Pre-message length” is not used.

NOTE: The unit is bit.

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2.3.2.32 PKA Control (PKA_SFR0, R/W, Address = 0xEA00_7000)

PKA_SFR0	Bit	Description	R/W	Initial State
PREC_ID	[1:0]	Sets the precision. 00 = Single precision, that is, x1 [Default] 01 = Double precision, that is, x2 10 = Triple precision, that is, x3 11 = Quadruple precision, that is, x4		00
Reserved	[2]	-		-
CHNK_SZ	[6:3]	Sets the chunk size. 0000 = (don't use) [Default] 0001 = (don't use) 0010 = (don't use) 0011 = 128-bits 0100 = 160-bits 0101 = 192-bits 0110 = 224-bits 0111 = 256-bits 1000 = 288-bits 1001 = 320-bits 1010 = 352-bits 1011 = 384-bits 1100 = 416-bits 1101 = 448-bits 1110 = 480-bits 1111 = 512-bits		0000
Reserved	[31:7]	-		-

NOTE: Operand's bit length = (Chunk's size)*(Precision)
For example, (160-bits)*Single=160-bits, (512-bits)*Double=1024-bits, (512-bits)*Quadruple=2048-bits

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2.3.2.33 PKA Control (PKA_SFR1, R/W, Address = 0xEA00_7004)

PKA_SFR1	Bit	Description	R/W	Initial State
EXEC_ON	[0]	Controls and monitors the execution of PKA 0 = PKA stays in idle state [Default] 1 = PKA starts to run and continues running		0
Reserved	[2:1]	-		-
PLDM_ON (note)	[3]	Controls the pre-loading of the least significant chunk of modulus M 0 = Does not pre-load the least significant chunk of modulus M [Default] 1 = Pre-loads the least significant chunk of modulus M		0

NOTE: If PLDM_ON is set to '1', PKA loads modulus M's least significant chunk data from memory to PKA's internal register at the initial time of multiplication. For the whole modular exponentiation, only the first modular multiplication needs to pre-load the least significant chunk of modulus M. When PKA performs a number of modular multiplications except the first one, the least significant chunk of modulus M is pre-loaded during the previous modular multiplication. When PLDM_ON is '0', the processing time for a multiplication becomes shorter. The saved clock cycles after setting PLDM_ON to '0' is c/32 + 5.

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2.3.2.34 PKA Control (PKA_SFR2, R/W, Address = 0xEA00_7008)

PKA_SFR2	Bit	Description	R/W	Initial State
S_ SEG_ID	[4:0]	Memory Segment ID for input operand S in PKA-2 mode 00000 = Segment 0 [Default] 00001 = Segment 1 00010 = Segment 2 00011 = Segment 3 00100 = Segment 4 00101 = Segment 5 00110 = Segment 6 00111 = Segment 7 01000 = Segment 8 01001 = Segment 9 01010 = Segment 10 01011 = Segment 11 01100 = Segment 12 01101 = Segment 13 01110 = Segment 14 01111 = Segment 15 10000 = Segment 16 10001 = Segment 17 10010 = Segment 18 10011 = Segment 19 10100 = Segment 20 10101 = Segment 21 10110 = Segment 22 10111 = Segment 23 11000 = Segment 24 11001 = Segment 25 11010 = Segment 26 11011 = Segment 27 11100 = Segment 28 11101 = Segment 29 11110 = (dedicated to the hardware's internal usage) 11111 = (dedicated to the hardware's internal usage)		00000
Reserved	[7:5]	-		-

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2.3.2.35 PKA Control (PKA_SFR3, R/W, Address = 0xEA00_700C)

PKA_SFR3	Bit	Description	R/W	Initial State
Reserved	[31:30]			-
SEG_SIGN	[29:0]	Specifies the signs of numbers stored in the segments. - 0 at the ith bit: The number in the ith segment is positive [Default] - 1 at the ith bit: The number in the ith segment is negative xx_xxxx_xxxx_xxxx_xxxx_xxxx_xxx0: Segment 0 is positive xx_xxxx_xxxx_xxxx_xxxx_xxxx_xxx1: Segment 0 is negative xx_xxxx_xxxx_xxxx_xxxx_xxxx_xx0x: Segment 1 is positive xx_xxxx_xxxx_xxxx_xxxx_xxxx_xx1x: Segment 1 is negative xx_xxxx_xxxx_xxxx_xxxx_xxxx_x0xx: Segment 2 is positive xx_xxxx_xxxx_xxxx_xxxx_xxxx_x1xx: Segment 2 is negative xx_xxxx_xxxx_xxxx_xxxx_xxxx_0xxx: Segment 3 is positive xx_xxxx_xxxx_xxxx_xxxx_xxxx_1xxx: Segment 3 is negative xx_xxxx_xxxx_xxxx_xxxx_xxx0_xxxx: Segment 4 is positive xx_xxxx_xxxx_xxxx_xxxx_xxx1_xxxx: Segment 4 is negative xx_xxxx_xxxx_xxxx_xxxx_xx0x_xxxx: Segment 5 is positive xx_xxxx_xxxx_xxxx_xxxx_xx1x_xxxx: Segment 5 is negative xx_xxxx_xxxx_xxxx_xxxx_x0xx_xxxx: Segment 6 is positive xx_xxxx_xxxx_xxxx_xxxx_x1xx_xxxx: Segment 6 is negative xx_xxxx_xxxx_xxxx_xxxx_0xxx_xxxx: Segment 7 is positive xx_xxxx_xxxx_xxxx_xxxx_1xxx_xxxx: Segment 7 is negative xx_xxxx_xxxx_xxxx_xxxx_xxx0_xxxx_xxxx: Segment 8 is positive xx_xxxx_xxxx_xxxx_xxxx_xxx1_xxxx_xxxx: Segment 8 is negative xx_xxxx_xxxx_xxxx_xxxx_xx0x_xxxx_xxxx: Segment 9 is positive xx_xxxx_xxxx_xxxx_xxxx_xx1x_xxxx_xxxx: Segment 9 is negative		0

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PKA_SFR3	Bit	Description	R/W	Initial State
		xx_xxxx_xxxx_xxxx_xxxx_x0xx_xxxx_xxxx: Segment 10 is positive xx_xxxx_xxxx_xxxx_xxxx_x1xx_xxxx_xxxx: Segment 10 is negative xx_xxxx_xxxx_xxxx_xxxx_0xxx_xxxx_xxxx: Segment 11 is positive xx_xxxx_xxxx_xxxx_xxxx_1xxx_xxxx_xxxx: Segment 11 is negative xx_xxxx_xxxx_xxxx_xxx0_xxxx_xxxx_xxxx: Segment 12 is positive xx_xxxx_xxxx_xxxx_xxx1_xxxx_xxxx_xxxx: Segment 12 is negative xx_xxxx_xxxx_xxxx_xx0x_xxxx_xxxx_xxxx: Segment 13 is positive xx_xxxx_xxxx_xxxx_xx1x_xxxx_xxxx_xxxx: Segment 13 is negative xx_xxxx_xxxx_xxxx_x0xx_xxxx_xxxx_xxxx: Segment 14 is positive xx_xxxx_xxxx_xxxx_x1xx_xxxx_xxxx_xxxx: Segment 14 is negative xx_xxxx_xxxx_xxxx_0xxx_xxxx_xxxx_xxxx: Segment 15 is positive xx_xxxx_xxxx_xxxx_1xxx_xxxx_xxxx_xxxx: Segment 15 is negative xx_xxxx_xxxx_xxx0_xxxx_xxxx_xxxx_xxxx: Segment 16 is positive xx_xxxx_xxxx_xxx1_xxxx_xxxx_xxxx_xxxx: Segment 16 is negative xx_xxxx_xxxx_xx0x_xxxx_xxxx_xxxx_xxxx: Segment 17 is positive xx_xxxx_xxxx_xx1x_xxxx_xxxx_xxxx_xxxx: Segment 17 is negative xx_xxxx_xxxx_x0xx_xxxx_xxxx_xxxx_xxxx: Segment 18 is positive xx_xxxx_xxxx_x1xx_xxxx_xxxx_xxxx_xxxx: Segment 18 is negative xx_xxxx_xxxx_0xxx_xxxx_xxxx_xxxx_xxxx: Segment 19 is positive xx_xxxx_xxxx_1xxx_xxxx_xxxx_xxxx_xxxx: Segment 19 is negative xx_xxxx_xxx0_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 20 is positive xx_xxxx_xxx1_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 20 is negative xx_xxxx_xx0x_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 21 is positive xx_xxxx_xx1x_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 21		

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PKA_SFR3	Bit	Description	R/W	Initial State
		is negative xx_xxxx_x0xx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 22 is positive xx_xxxx_x1xx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 22 is negative xx_xxxx_0xxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 23 is positive xx_xxxx_1xxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 23 is negative xx_xxx0_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 24 is positive xx_xxx1_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 24 is negative xx_xx0x_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 25 is positive xx_xx1x_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 25 is negative xx_x0xx_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 26 is positive xx_x1xx_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 26 is negative xx_0xxx_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 27 is positive xx_1xxx_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 27 is negative x0_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 28 is positive x1_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 28 is negative 0x_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 29 is positive 1x_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx: Segment 29 is negative		

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2.3.2.36 PKA Control (PKA_SFR4, R/W, Address = 0xEA00_7010)

PKA_SFR4	Bit	Description	R/W	Initial State
FUNC_ID	[0]	Selects the function to be executed. 0 = Montgomery multiplication (A by B) [Default] 1 = Montgomery multiplication (A by 1)		0
Reserved	[4:1]	-		-
SEG_SIZE	[6:5]	Size of the memory segments. 00 = Full-size (that is, 256 bytes) [Default] 01 = Half-size (that is, 128 bytes) 10 = Quarter-size (that is, 64 bytes)		00
Reserved	[31:7]	-		-

NOTE: Selecting the half-size and quarter-size segments is only possible in PKA-2 mode.

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Section 12

ETC

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1 ELECTRICAL DATA

1.1 ABSOLUTE MAXIMUM RATINGS

Any Stress beyond “Absolute Maximum Ratings” listed in *Table 1-1* can cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to absolute-maximum rated conditions for extended periods can affect device reliability.

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Table 1-1 Absolute Maximum Rating

Parameter	Symbol	Minimum	Maximum	Unit
DC Supply Voltage	VDD_ALIVE,VDD_APLL,VDD_MPLL, VDD_EPLL,VDD_VPLL,VDD_ARM, VDD_INT,VDD_UOTG_D, VDD_UHOST_D,VDD_HDMI,VDD_HDMI_PLL, VDD_MIPI_D,VDD_MIPI_PLL	-0.5	1.8	V
	VDD_M1,VDD_M2, VDD_MIPI_A	-0.5	2.5	
	VDD_M0,VDD_SYS0,VDD_SYS1, VDD_EXT0,VDD_EXT1,VDD_EXT2, VDD_CKO,VDD_RTC,VDD_LCD, VDD_CAM,VDD_AUD,VDD_MODEM, VDD_KEY,VDD_DAC_A,VDD_DAC, , VDD_HDMI_OSC, VDD_UOTG_A	-0.5	4.6	
DC Input Voltage	1.1V Input buffer	-0.5	1.8	
	1.8V Input buffer	-0.5	2.5	
	3.3V Input buffer	-0.5	4.6	
	5.0V Input buffer	-0.5	8.0	
DC Output Voltage	1.1V Input buffer	-0.5	1.8	
	1.8V Input buffer	-0.5	2.5	
	3.3V Input buffer	-0.5	4.6	
DC In/Out Current	-	± 20		mA
Storage Temperature	TSTG	- 40 to 150		°C

NOTE: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the operational sections of this standard is not implied. And VDD_ODRAMA_IO, VDD_ODRAMB_IO, VDD_MDDR_IO, VDD_ONAND_IO absolute maximum rate is written in each MCP spec. Please refer those.

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1.2 RECOMMENDED OPERATING CONDITIONS

Operate S5PV210 based on the operating conditions listed in *Table 1-2*.

Table 1-2 Recommended Operating Conditions

Parameter	Pin Name	Minimum	Typical	Maximum	Unit
DC Supply Voltage for Alive Block (1)	VDD_ALIVE	1.045	1.1	1.26	V
DC Supply Voltage for Core Block (1)	VDD_APLL VDD_MPLL VDD_EPLL VDD_VPLL	1.045	1.1	1.26	
	VDD_ARM	0.9	1.25 (2)	1.31	
	VDD_INT	0.95	1.1 (2)	1.155	
DC Supply Voltage for Memory Interface0 (NOR/NAND/OneNAND)	VDD_M0	1.7	1.8/2.5/3.3	3.6	
DC Supply Voltage for Memory Interface1 (DRAM) (3)	VDD_M1	1.7	1.8	1.9	
DC Supply Voltage for Memory Interface2 (DRAM) (3)	VDD_M2	1.7	1.8	1.9	
DC Supply Voltage for SYS0 Block (XEINT0~7, XOM, XnRESET, XusbXtal, JTAG)	VDD_SYS0	1.7	1.8/2.5/3.0	3.6	
DC Supply Voltage for SYS1 Block (XEINT8~15)	VDD_SYS1	1.7	1.8/2.5/3.0	3.6	
DC Supply Voltage for EXT0	VDD_EXT0	1.7	1.8/2.5/3.0	3.6	
DC Supply Voltage for EXT1	VDD_EXT1	1.7	1.8/2.5/3.0	3.6	
DC Supply Voltage for EXT2	VDD_EXT2	1.7	1.8/2.5/3.0	3.6	
DC Supply Voltage for CKO	VDD_CKO	1.7	2.5/3.0	3.6	
DC Supply Voltage for RTC	VDD_RTC	1.7	2.5/3.0	3.6	
DC Supply Voltage for LCD	VDD_LCD	1.7	2.5/3.0	3.6	
DC Supply Voltage for CAM	VDD_CAM	1.7	2.5/3.0	3.6	
DC Supply Voltage for AUD	VDD_AUD	1.7	2.5/3.0	3.6	
DC Supply Voltage for MODEM	VDD_MODEM	1.7	2.5/3.0	3.6	
DC Supply Voltage for KEY	VDD_KEY	1.7	2.5/3.0	3.6	
DC Supply Voltage for ADAC	VDD_DAC_A	3.0	3.3	3.6	
DC Supply Voltage for DAC	VDD_DAC	3.0	3.3	3.6	
DC Supply Voltage for HDMI Core	VDD_HDMI	1.05	1.1	1.15	
DC Supply Voltage for HDMI PLL	VDD_HDMI_PLL	1.05	1.1	1.15	

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Parameter	Pin Name	Minimum	Typical	Maximum	Unit
DC Supply Voltage for HDMI OSC	VDD_HDMI_OSC	3.0	3.3	3.6	
DC Supply Voltage for MIPI I/O	VDD_MIPI_A	1.7	1.8	1.9	
DC Supply Voltage for MIPI Core	VDD_MIPI_D	1.05	1.1	1.15	
DC Supply Voltage for MIPI PLL	VDD_MIPI_PLL	1.05	1.1	1.15	
DC Supply Voltage for USB OTG I/O	VDD_UOTG_A	3.0	3.3	3.6	
DC Supply Voltage for USB OTG Core	VDD_UOTG_D	1.05	1.1	1.15	
DC Supply Voltage for USB HOST I/O	VDD_UHOST_A	3.0	3.3	3.6	
DC Supply Voltage for USB HOST Core	VDD_UHOST_D	1.05	1.1	1.15	
DC Supply Voltage for ADC	VDD_ADC	3.0	3.3	3.6	
DC Supply Voltage for OneDARAM™ A-port IO of MCP	VDD_ODRAMA_IO(4)	1.7	1.8	1.9	
DC Supply Voltage for OneDRAM™ B-port IO of MCP	VDD_ODRAMB_IO(4)	1.7	1.8	1.9	
DC Supply Voltage for OneDRAM™ Core of MCP	VDD_ODRAM(5)	1.7	1.8	1.9	
DC Supply Voltage for Mobile DRAM IO of MCP	VDD_MDDR_IO(6)	1.7	1.8	1.9	
DC Supply Voltage for Mobile DRAM Core of MCP	VDD_MDDR(7)	1.7	1.8	1.9	
DC Supply Voltage for OneNAND IO of MCP	VDD_ONAND_IO(8)	1.7	1.8	1.9	
DC Supply Voltage for OneNAND Core of MCP	VDD_ONAND(9)	1.7	1.8	1.9	
Operating Temperature	TA	-25 to 85			°C

NOTE:

1 In case of Engineering sample, the typical voltage is 1.2 V.

2 The recommendatory voltage level to apply DVFS(Dynamic Voltage Frequency Scaling);

Operation Freq.	ARM	1GHz	800MHz	400MHz	200MHz	100MHz
	BUS	200MHz	200MHz	200MHz	200MHz	100MHz
VDD_ARM		1.25V±5%	1.2V±5%	1.05V±5%	0.95V±5%	0.95V±5%
VDD_INT		1.1V±5%	1.1V±5%	1.1V±5%	1.1V±5%	1.0V±5%

Caution: In case over 680MHz, VDD_ARM should be higher than VDD_INT.
In DDR2 memory, DVFS does not support because of the DLL.

3 VDD_M1/M2 power depends on MCP voltage

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4 In the MCP, pin Name is "VDDQa" & "VDDQb"
5 In the MCP, pin Name is "VDD"
6 In the MCP, pin Name is "VDDQd"
7 In the MCP, pin Name is "VDD"
8 In the MCP, pin Name is "VCCQo"
9 In the MCP, pin Name is "VCCo"

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1.3 D.C. ELECTRICAL CHARACTERISTICS

The entire DC characteristics listed in *Table 1-3* for each pin include input sense levels, output drive levels, and currents.

Use these parameters to determine maximum DC loading and to determine maximum transition times for a given load. *Table 1-3* shows the DC operating conditions for the high- and low-strength input, output, and I/O pins.

Table 1-3 I/O DC Electrical Characteristics

VDD = 1.65V~3.60V, Tj = -25 to 85°C (Junction temperature)

Parameter		Condition		Minimum	Typical	Maximum	Unit
Vtol	Tolerant external voltage**	VDD Power Off				3.6	V
		VDD Power On	VDD=3.3V			3.6	V
			VDD=1.8V			3.6	
Vih	High Level Input Voltage						
	LVCMOS Interface			0.7VDD		VDD+0.3V	V
Vil	Low Level Input Voltage						
	LVCMOS Interface			-0.3V		0.3VDD	V
ΔV	Hysteresis Voltage			0.1VDD			V
Iih	High Level Input Current						
	Input Buffer	Vin=VDD (VDD=min)		-10		10	uA
	Input Buffer with pull-down			45(1)			uA
Iil	Low Level Input Current						
	Input Buffer	Vin=VSS (Vss=min)		-10		10	uA
	Input Buffer with pull-up					-45(1)	uA
Voh	Output high voltage(2)	Driver Strength		0.8xVDD			V
Vol	Output Low voltage(2)	Driver Strength				0.2xVDD	V
Ioz	Tri-State Output Leakage Current	Vout=VSS or VDD		-10		10	uA
CIN	Input capacitance	Any input and Bidirectional buffers				5	pF
COUT	Output capacitance	Any output buffer				5	pF

NOTE:
1. The values of Ioh & Iol are valid only for 3.3V range.
2. The value of IOH and IOL is for min. driver strength.

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Table 1-4 RTC OSC Electrical Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VIH	DC input logic high	0.7*VDDrtc			V
VIL	DC input logic low			0.3*VDDrtc	V
IIH	High level input current	-10		10	μA
IIL	Low level input current	-10		10	μA

Table 1-5 USB DC Electrical Characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
VIH	High level input voltage		2.0		V
VIL	Low level input voltage			0.8	V
IIH	High level input current	Vin = 3.3v	-10	10	μA
IIL	Low level input current	Vin = 0.0v	-10	10	μA
VOH	Static Output High	14.25Kohm to GND	2.8	3.6	V
VOL	Static Output Low	1.425Kohm to 3.6V		0.3	V
VBUS	Valid level voltage		4.4	5.25	V

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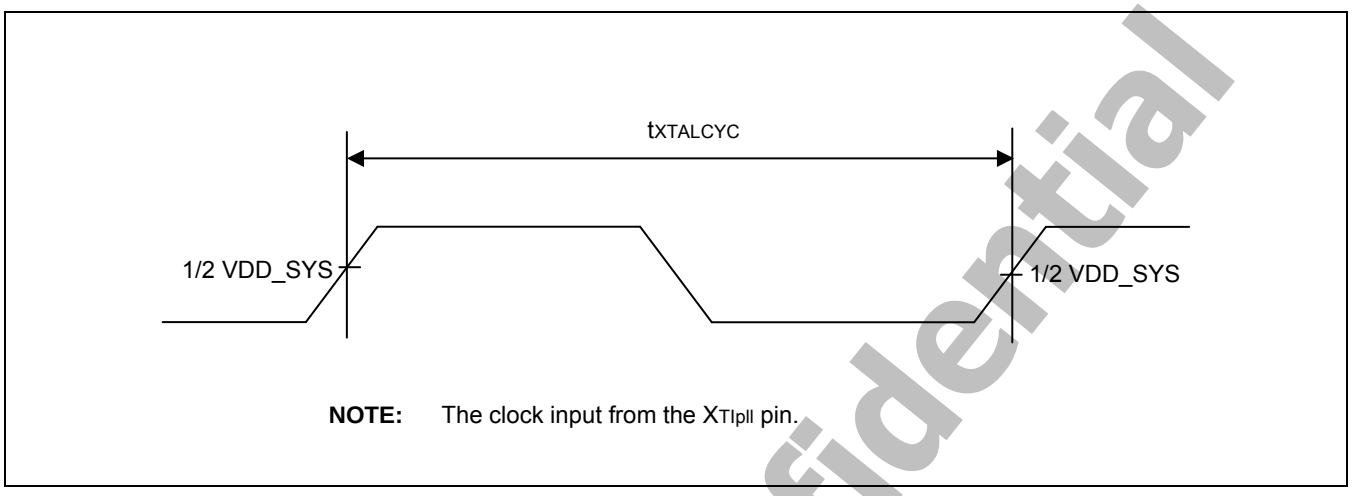
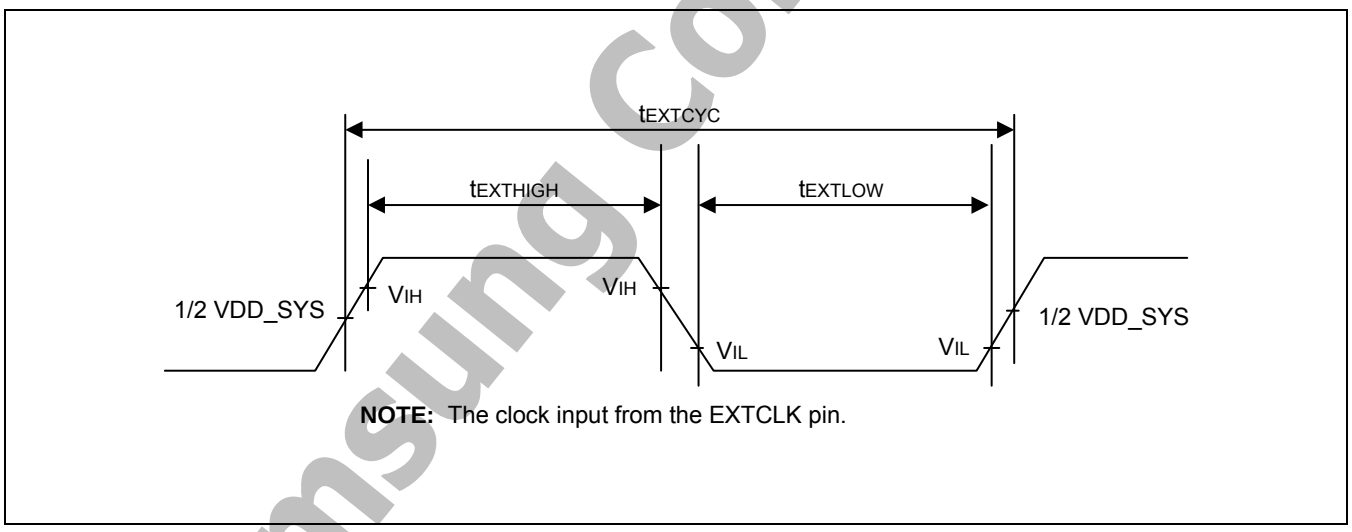
1.4 CLK ALTERNATING-CURRENT ELECTRICAL CHARACTERISTICS

Pin's Alternating-Current (AC) characteristics include input and output capacitance. These factors determine the loading for external drivers and other load analyses.



NOTE: The clock input from the XTIpll pin.

Figure 1-1 XTIpll Clock Timing



NOTE: The clock input from the EXTCLK pin.

Figure 1-2 EXTCLK Clock Input Timing

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Table 1-6 Clock Timing Constants

(VDDINT = 1.1V ± 5%, TA = -25 to 85°C, VDDSYS = 3.3V ± 5%, 2.5V ± 5%, 1.8V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Duration for crystal oscillator clock input	$t_{XTALCYC}$	20			ns
High width for external clock input	$t_{EXTHIGH}$	10			ns
Low width for external clock input	t_{EXTLOW}	10			ns
APLL lock time	t_{APLL}			100	usec
MPLL lock time	t_{MPLL_LT}			400	Fref*
EPLL lock time	t_{EPLL_LT}			3000	Fref
VPLL lock time	t_{VPLL_LT}			400	Fref

* Fref = Fin/P(refer to CMU manual)

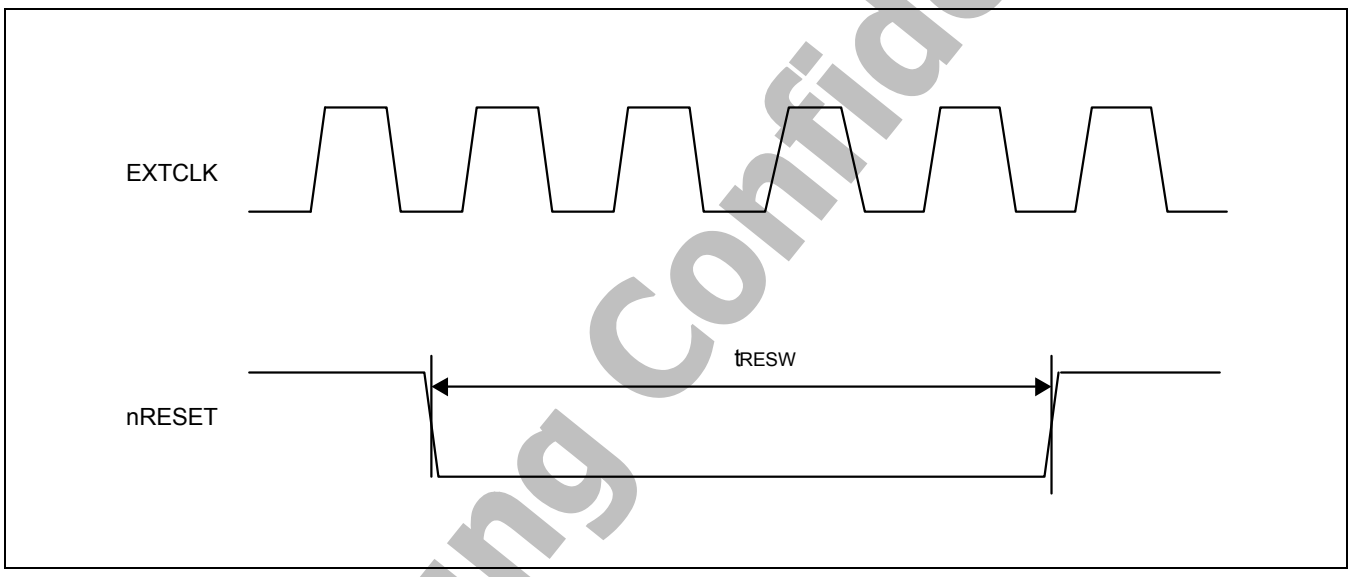

Figure 1-3 Manual Reset Input Timing

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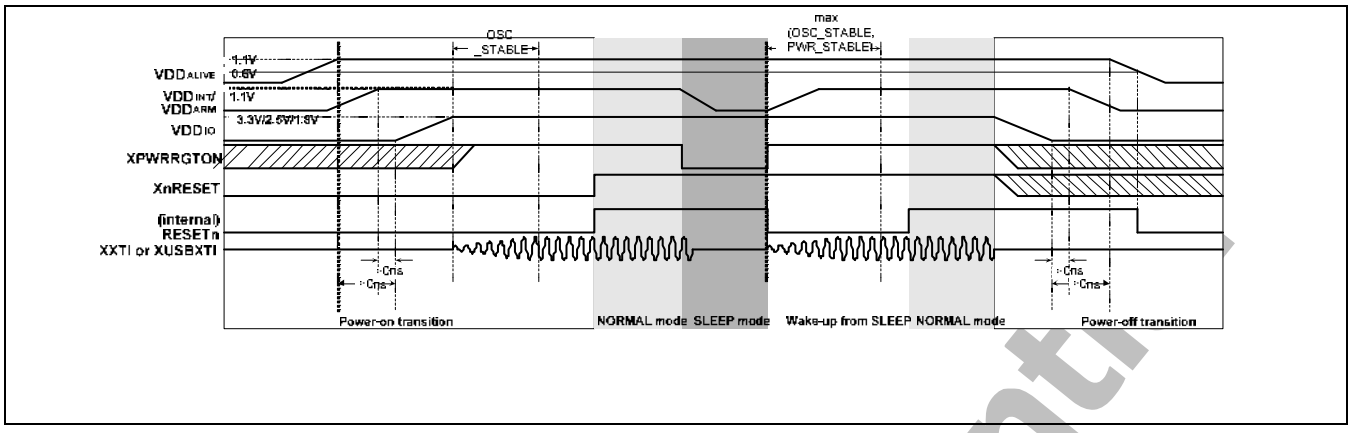

Figure 1-4 Power-On Reset Sequence

OSC STABLE in Figure 1-4 indicates the time required for the oscillator pad to be stabilized.

Table 1-7 Power on Reset Timing Specifications

(VDDINT= 1.1V ± 5%, TA = -25 to 85°C, VDDSYS = 3.3V ± 5%, 2.5V ± 5%, 1.8V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Reset assert time after clock stabilization	t_{RESW}	4		-	XTIpll or EXTCLK

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1.5 ROM/ SRAM AC ELECTRICAL CHARACTERISTICS

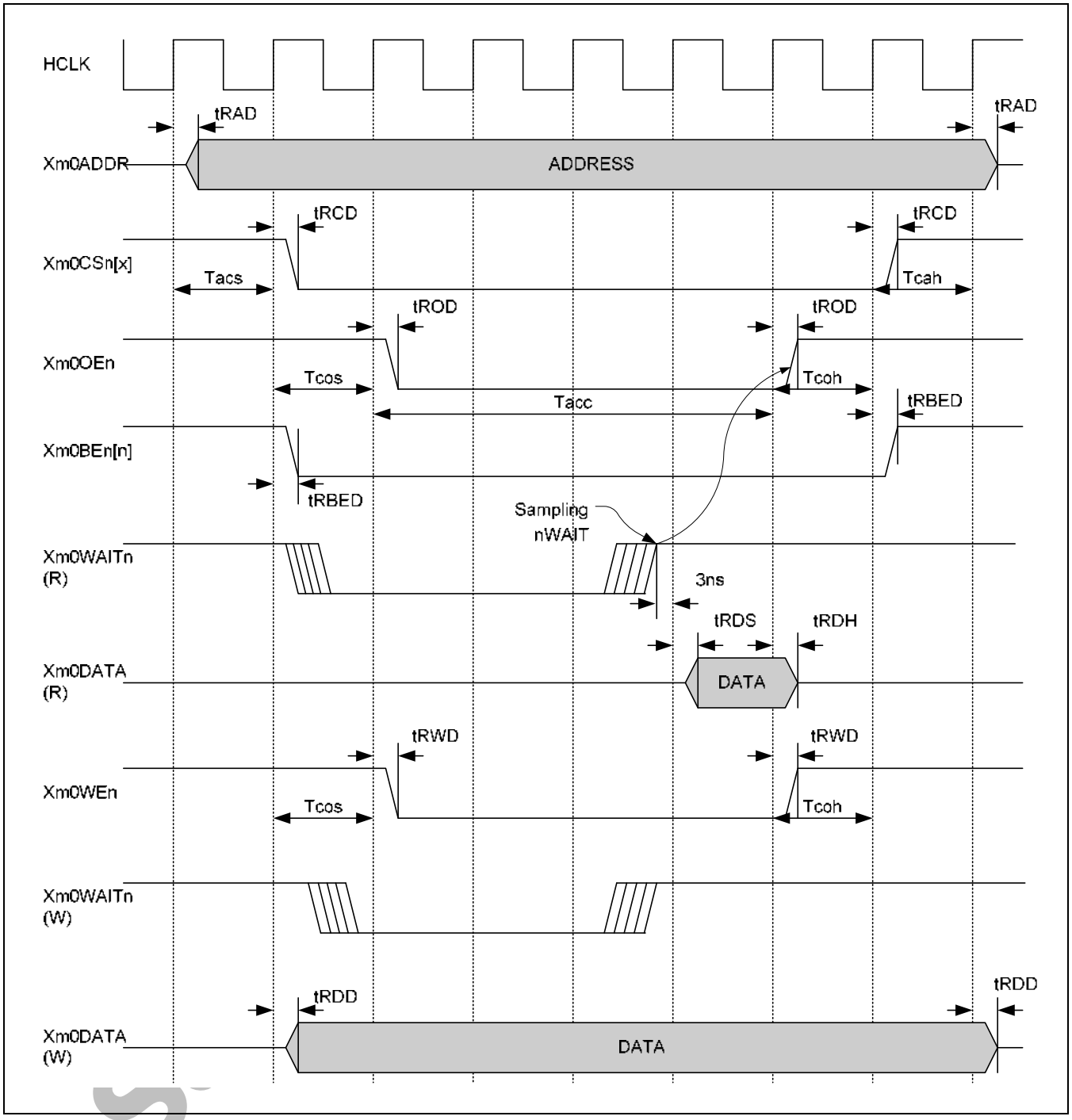

Figure 1-5 ROM/ SRAM Timing
(Tacs = 0, Tcos = 0, Tacc = 2, Tcoh = 0, Tcah = 0, PMC = 0, ST = 0, DW = 16-bit)

Table 1-8 ROM/SRAM Bus Timing Constants

(VDDINT = 1.1V ± 5%, TA = -25 to 85°C, VDDM0 = 1.7V - 3.6V)

Parameter	Symbol	Minimum	Maximum	Unit
ROM/SRAM Address Delay	t_{RAD}	1.77	5.22	ns
ROM/SRAM Chip Select 0 Delay	t_{RCD}	3.39	8.06	ns
ROM/SRAM Chip Select 1 Delay	t_{RCD}	3.48	8.33	ns
ROM/SRAM Chip Select 2 Delay	t_{RCD}	4.13	7.29	ns
ROM/SRAM Chip Select 3 Delay	t_{RCD}	3.14	7.22	ns
ROM/SRAM Chip Select 4 Delay	t_{RCD}	2.16	4.21	ns
ROM/SRAM Chip Select 5 Delay	t_{RCD}	2.30	4.53	ns
ROM/SRAM nOE(Output Enable) Delay	t_{ROD}	2.78	5.46	ns
ROM/SRAM nWE(Write Enable) Delay	t_{RWD}	2.02	3.96	ns
ROM/SRAM Byte Enable Delay	t_{RBED}	2.95	6.52	ns
ROM/SRAM Output Data Delay	t_{RDD}	3.50	7.41	ns
ROM/SRAM Read Data Setup Time	t_{RDS}	2.00	-	ns
ROM/SRAM Write Data Hold Time	t_{RDH}	1.00	-	ns

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1.6 ONENAND AC ELECTRICAL CHARACTERISTICS

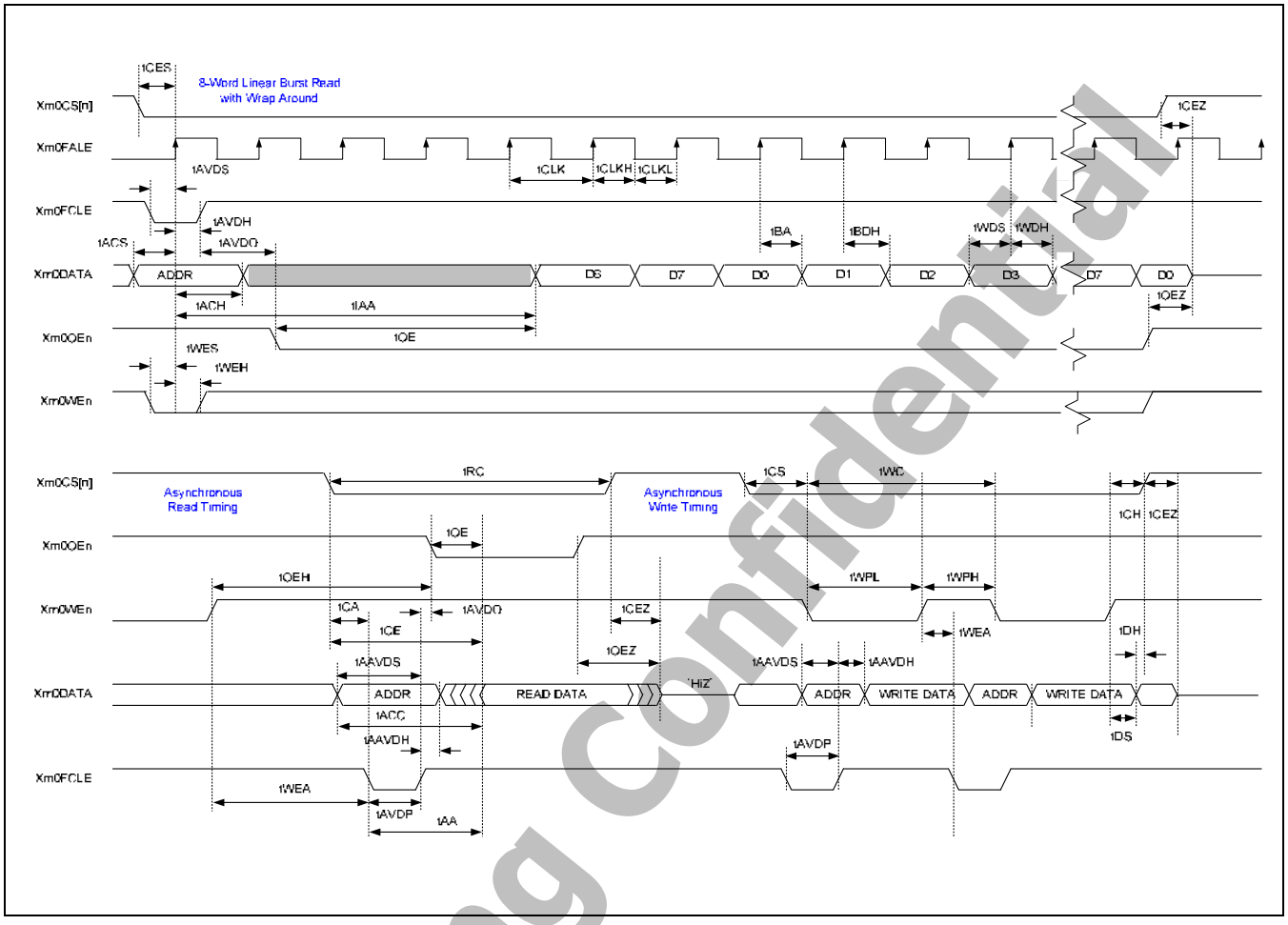

Figure 1-6 OneNand Flash Timing

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Table 1-9 OneNAND Bus Timing Constants

(VDDINT = 1.1V ± 5%, TA = -25 to 85°C, VDDM0 = 1.7V - 1.9V)

Parameter	Symbol	Minimum	Maximum	Unit
OneNAND SMCLK cycle	t_{CLK}	12	-	ns
OneNAND Clock High time	t_{CLKH}	5	-	ns
OneNAND Clock Low time	t_{CLKL}	5	-	ns
OneNAND CSn Setup time to SMCLK	t_{CES}	4.5	-	ns
OneNAND Initial Access time	t_{IAA}	-	70	ns
OneNAND Burst Access time valid SMCLK to Output delay	t_{BA}	-	9	ns
OneNAND Data Hold time from next clock cycle	t_{BDH}	2	-	ns
OneNAND Output Enable to Data	t_{OE}	-	20	ns
OneNAND CSn Disable to Output High Z	t_{CEZ}	-	20	ns
OneNAND OEn Disable to Output High Z	t_{OEZ}	-	15	ns
OneNAND Address Setup time to SMCLK	t_{ACS}	4	-	ns
OneNAND Address Hold time to SMCLK	t_{ACH}	6	-	ns
OneNAND ADRVALID Setup time to SMCLK	t_{AVDS}	4	-	ns
OneNAND ADRVALID Hold time to SMCLK	t_{AVDH}	6	-	ns
OneNAND Write Data Setup time to SMCLK	t_{WDS}	4	-	ns
OneNAND Write Data Hold time to SMCLK	t_{WDH}	2	-	ns
OneNAND WEn Setup time to SMCLK	t_{WES}	4	-	ns
OneNAND WEn Hold time to SMCLK	t_{WEH}	6	-	ns
OneNAND ADRVALID high to OEn low	t_{AVDO}	0	-	ns
OneNAND Access time from CSn low	t_{CE}	-	76	ns
OneNAND Asynchronous Access time from ADRVALID low	t_{AA}	-	76	ns
OneNAND Asynchronous Access time from address valid	t_{ACC}	-	76	ns
OneNAND Read Cycle time	t_{RC}	76	-	ns
OneNAND ADRVALID low pulse width	t_{AVDP}	12	-	ns
OneNAND Address Setup to rising edge of ADRVALID	t_{AAVDS}	5	-	ns
OneNAND Address Hold to rising edge of ADRVALID	t_{AAVDH}	7	-	ns
OneNAND CSn Setup to ADRVALID falling edge	t_{CA}	0	-	ns
OneNAND WEn Disable to ADRVALID enable	t_{WEA}	15	-	ns
OneNAND Address to OEn low	t_{ASO}	10	-	ns
OneNAND WEn Cycle time	t_{WC}	70	-	ns
OneNAND Data Setup time	t_{DS}	30	-	ns

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Parameter	Symbol	Minimum	Maximum	Unit
OneNAND Data Hold time	t_{DH}	0	-	ns
OneNAND CSn Setup time	t_{CS}	0	-	ns
OneNAND CSn Hold time	t_{CH}	0	-	ns
OneNAND WEn Pulse width low	t_{WPL}	40	-	ns
OneNAND WEn Pulse width high	t_{WPH}	30	-	ns

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1.7 NFCON AC ELECTRICAL CHARACTERISTICS

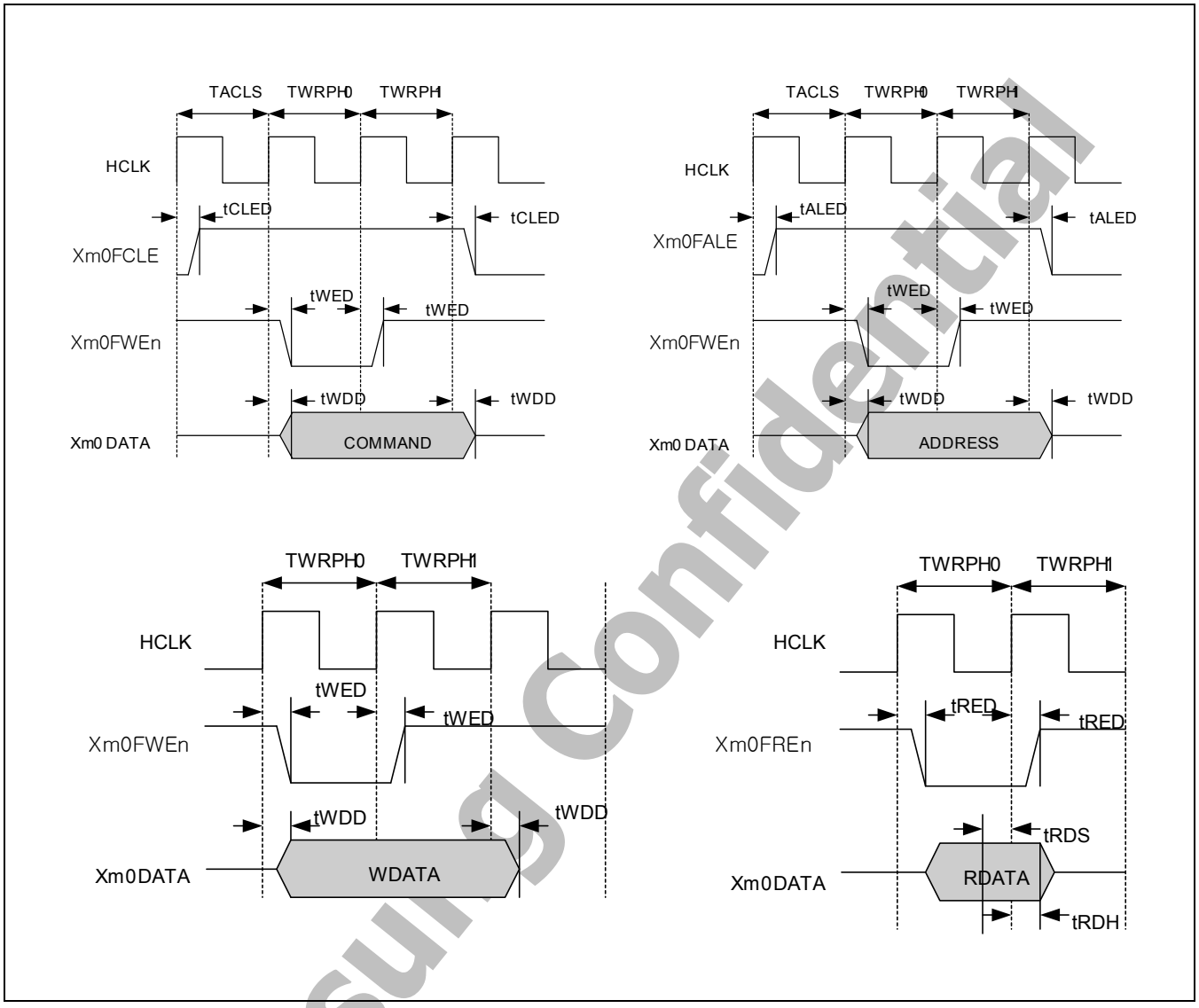

Figure 1-7 NAND Flash Timing

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Table 1-10 NFCON Bus Timing Constants

(VDDINT = 1.1V ± 5%, TA = -25 to 85°C, VDDM0 = 1.7V - 3.6V)

Parameter	Symbol	Minimum	Maximum	Unit
NFCON Chip Enable delay	t_{CED}	-	8.40	ns
NFCON CLE delay	t_{CLED}	-	4.45	ns
NFCON ALE delay	t_{ALED}	-	5.36	ns
NFCON Write Enable delay	t_{WED}	-	8.15	ns
NFCON Read Enable delay	t_{RED}	-	8.21	ns
NFCON Write Data delay	t_{WDD}	-	5.39	ns
NFCON Read Data Setup requirement time	t_{RDS}	1.00	-	ns
NFCON Read Data Hold requirement time	t_{RDH}	0.20	-	ns

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1.8 LPDDR1 (MDDR) SDRAM ELECTRICAL CHARACTERISTICS

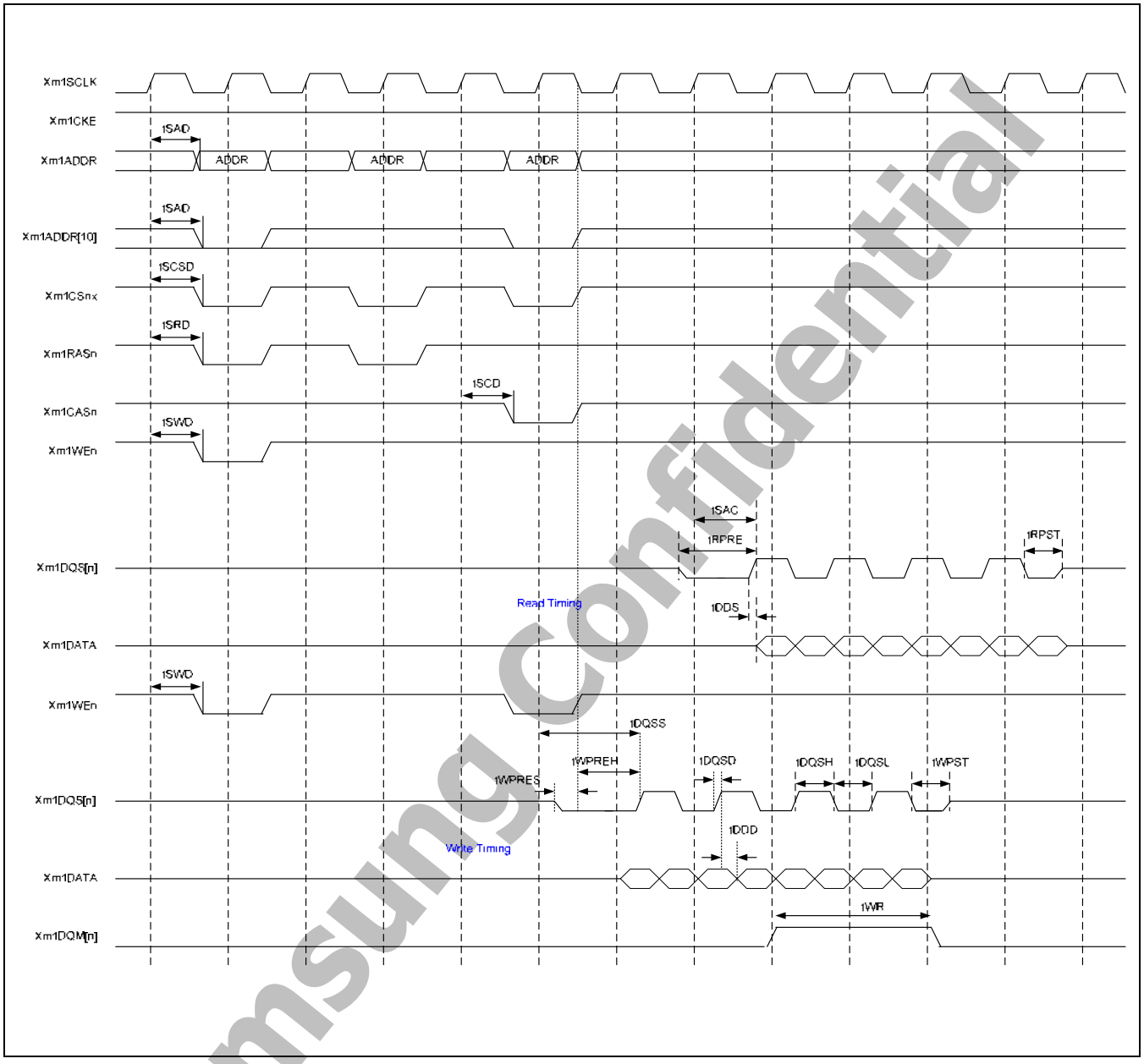

Figure 1-8 LPDDR1 SDRAM Read / Write Timing (Trp = 2, Trcd = 2, Tcl = 2, DW = 16-bit)

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Table 1-11 Memory Port 1, 2 Interface Timing Constants (LPDDR1 SDRAM)

(VDDINT = 1.1V ± 5%, TA = -25 to 85°C, VDDM1,VDDM2 = 1.7V – 1.9V)

Parameter	Symbol	Minimum	Maximum	Unit
DDR SDRAM Address Delay	t_{SAD}	2.48	3.51	ns
DDR SDRAM Chip Select Delay	t_{SCSD}	2.62	3.72	ns
DDR SDRAM Row active Delay	t_{SRD}	2.63	3.73	ns
DDR SDRAM Column active Delay	t_{SCD}	2.62	3.72	ns
DDR SDRAM Write enable Delay	t_{SWD}	2.62	3.73	ns
DDR SDRAM Output data access time from CK	t_{SAC}	2.00	5.50	ns
DDR SDRAM Row Precharge time	t_{RP}	18.00	-	ns
DDR SDRAM RAS to CAS delay	t_{RCD}	18.00	-	ns
DDR SDRAM Write recovery time	t_{WR}	12.00	-	ns
DDR SDRAM Clock low level width	t_{CL}	0.45	0.55	tCK
DDR SDRAM Read Preamble	t_{RPRE}	0.90	1.10	tCK
DDR SDRAM Read Postamble	t_{RPST}	0.40	0.60	tCK
DDR SDRAM Write Postamble time	t_{WPST}	0.40	0.60	tCK
DDR SDRAM Clock to valid DQS-In	t_{DQSS}	0.75	1.25	tCK
DDR SDRAM DQS-In Setup time	t_{WPRES}	1.30	-	ns
DDR SDRAM DQS-In Hold time	t_{WPREH}	1.30	-	ns
DDR SDRAM DQS-In high level width	t_{DQSH}	0.35	0.60	tCK
DDR SDRAM DQS-In low level width	t_{DQSL}	0.35	0.60	tCK
DDR SDRAM read Data Setup time	t_{DDS}	-	0.50	ns

Load Capacitance	
Xm1,Xm2 signal line	< 15pF

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1.9 MODEMIF AC ELECTRICAL CHARACTERISTICS

For more information, Refer to Section 8-6 S5PV210_Modem Interface user's manual.

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1.10 LCD CONTROLLER AC ELECTRICAL CHARACTERISTICS

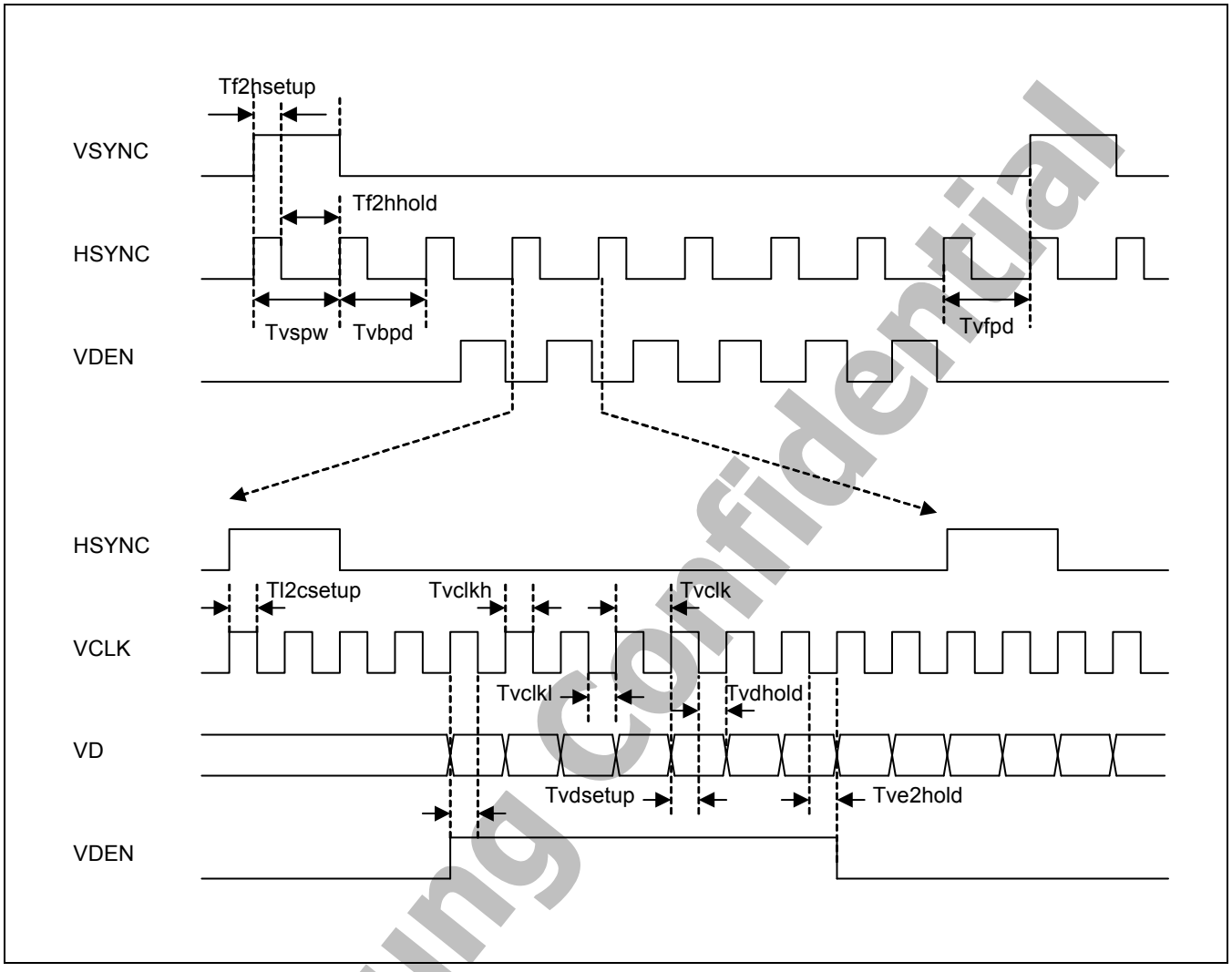

Figure 1-9 LCD Controller Timing

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Table 1-12 TFT LCD Controller Module Signal Timing Constants

(VDDINT = 1.1V ± 5%, TA = -25 to 85°C, VDDlcd = 1.7V - 3.6V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
VCLK pulse width	Tvclk	12	-	-	ns
VCLK pulse width high	Tvclkh	0.3	-	-	Pvclk(1)
VCLK pulse width low	Tvclkl	0.3	-	-	Pvclk
Vertical sync pulse width	Tvspw	VSPW + 1	-	-	Phclk(2)
Vertical back porch delay	Tvbpd	VBPD+1	-	-	Phclk
Vertical front porch dealy	Tvfpd	VFPD+1	-	-	Phclk
Hsync setup to VCLK falling edge	Tl2csetup	0.3	-	-	Pvclk
VDEN setup to VCLK falling edge	Tde2csetup	0.3	-	-	Pvclk
VDEN hold from VCLK falling edge	Tde2chold	0.3	-	-	Pvclk
VD setup to VCLK falling edge	Tvd2csetup	0.3	-	-	Pvclk
VD hold from VCLK falling edge	Tvd2chold	0.3	-	-	Pvclk
VSYNC setup to HSYNC falling edge	Tf2hsetup	HSPW + 1	-	-	Pvclk
VSYNC hold from HSYNC falling edge	Tf2hhold	HBPD + HFPD + HOZVAL + 3	-	-	Pvclk

NOTE:

1. VCLK period
2. HSYNC period

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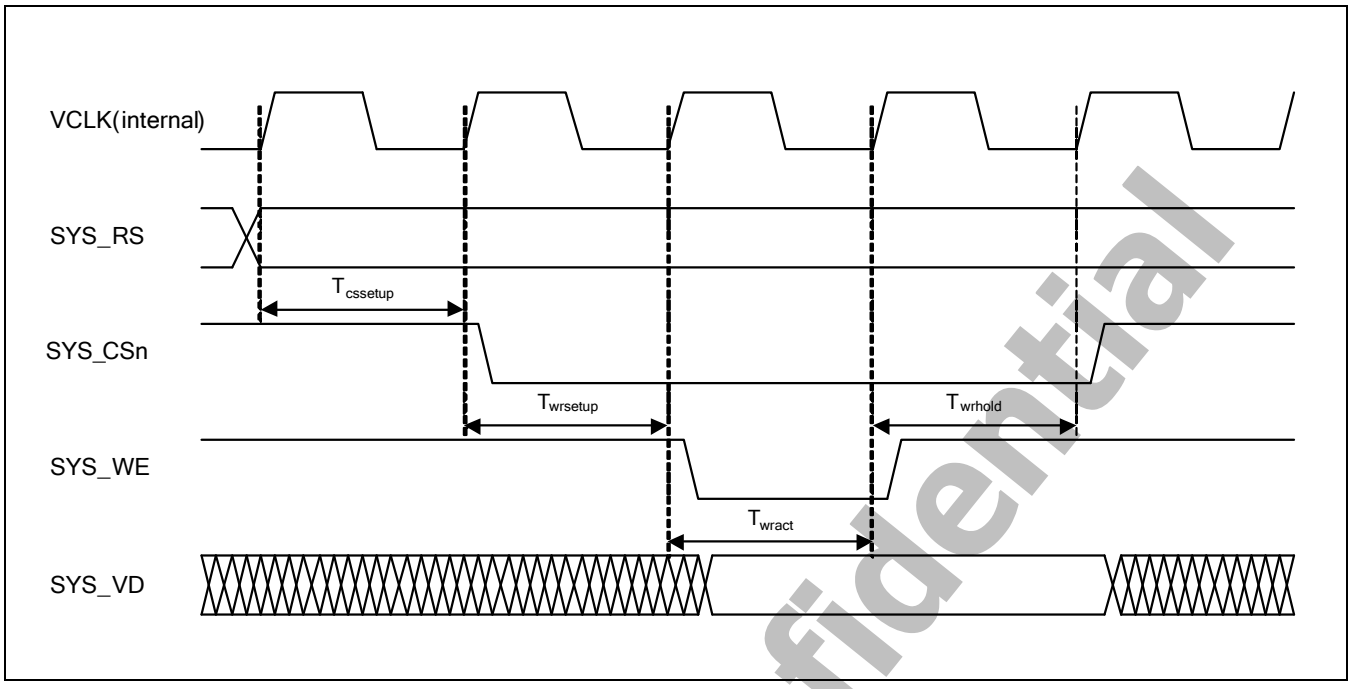

Figure 1-10 LCD I80 Interface Timing

Table 1-13 LCD I80 Interface Signal Timing Constants

(VDDINT = 1.1V ± 5%, TA = -25 to 85°C, VDDlcd = 1.7V - 3.6V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SYS_RS to SYS_CSn Low	Tcssetup	-	LCD_CS_SETUP + 1	-	Pvclk*
SYS_CSn Low to SYS_WR Low	Twrsetup	-	LCD_WR_SETUP	-	Pvclk
SYS_WE Pulse Width	Twract	-	LCD_WR_ACT	-	Pvclk
SYS_WE Hight to SYS_CSn High	Twrhold	-	LCD_WR_HOLD	-s	Pvclk

NOTE: Internal VCLK period

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1.11 CAMERA INTERFACE AC ELECTRICAL CHARACTERISTICS

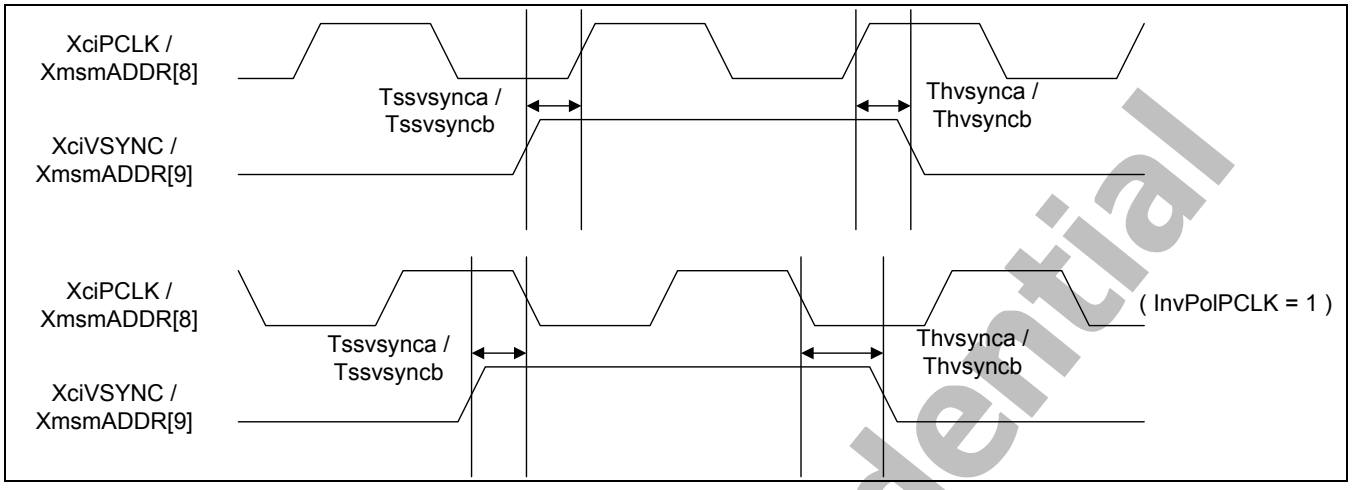

Figure 1-11 Camera Interface VSYNC Timing

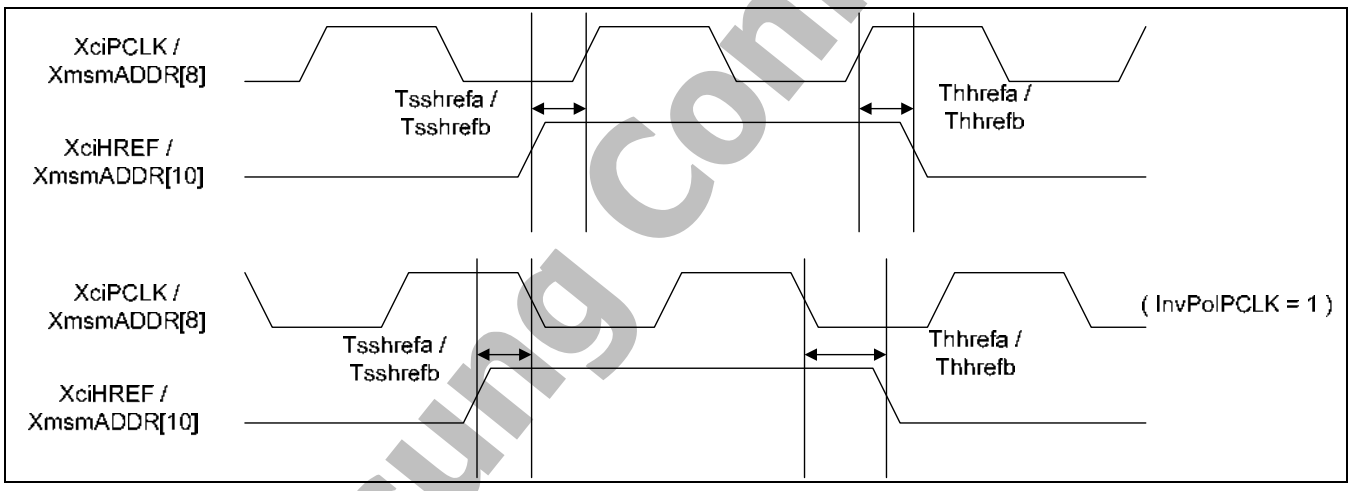

Figure 1-12 Camera Interface HREF Timing

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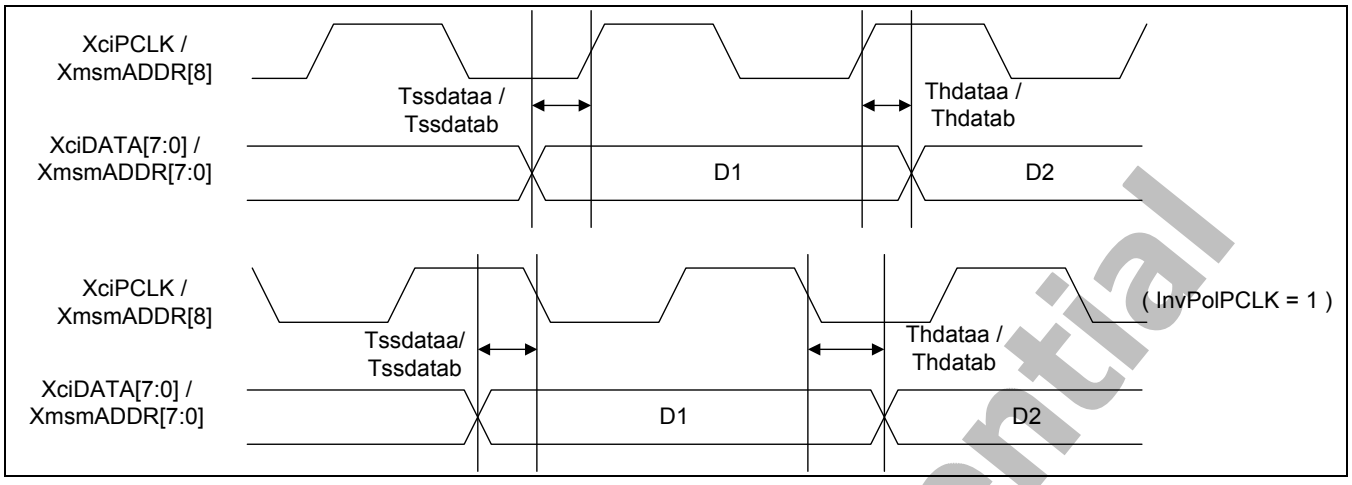

Figure 1-13 Camera Interface Data Timing

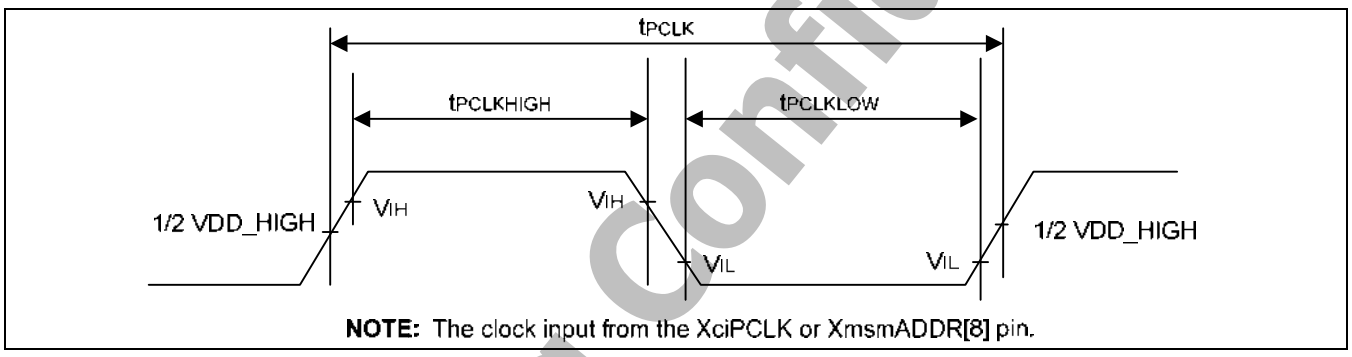

Figure 1-14 Camera Interface PCLK timing

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Table 1-14 Camera Controller Module Signal Timing Constants

(VDDINT= 1.1V ± 5%, TA = -25 to 85°C, VDDext = 1.7V - 3.6V)

Parameter	Symbol	Minimum	Typ	Maximum	Unit
XciVSYNC(CAM_VSYNC_A) input Setup time	Tssvsynca	0	-	PA - 0.26	ns
XciVSYNC(CAM_VSYNC_A) input Hold time	Thvsynca	0.26	-	PA	ns
XciHREF(CAM_HREF_A) input Setup time	Tsshrefa	0.35	-	PA	ns
XciHREF(CAM_HREF_A) input Hold time	Thhrefa	0	-	PA - 0.35	ns
XciDATA(CAM_DATA_A) input Setup time	Tssdataa	0	-	PA - 4.8	ns
XciDATA(CAM_DATA_A) input Hold time	Thdataa	4.8	-	PA	ns

NOTE: PA denotes period (ns) of CAM_PCLK_A

Parameter	Symbol	Minimum	Typ	Maximum	Unit
XmsmADDR[9](CAM_VSYNC_B) input Setup time	Tssvsyncb	0	-	PB	ns
XmsmADDR[9] (CAM_VSYNC_B) input Hold time	Thvsyncb	0	-	PB	ns
XmsmADDR[10] (CAM_HREF_B) input Setup time	Tsshrefb	0.08	-	PB	ns
XmsmADDR[10] (CAM_HREF_B) input Hold time	Thhrefb	0	-	PB - 0.08	ns
XmsmADDR[7:0] (CAM_DATA_B) input Setup time	Tssdatab	0	-	PB - 4.93	ns
XmsmADDR[7:0] (CAM_DATA_B) input Hold time	Thdatab	4.93	-	PB	ns

NOTE: PB denotes period (ns) of CAM_PCLK_B

Parameter	Symbol	Minimum	Typ	Maximum	Unit
PCLK period	tPCLK	12	-	-	ns
PCLK input high level pulse width	tPCLKHIGH	3	-	-	ns
PCLK input low level pulse width	tPCLKLOW	3	-	-	ns

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1.12 SDMMC AC ELECTRICAL CHARACTERISTICS

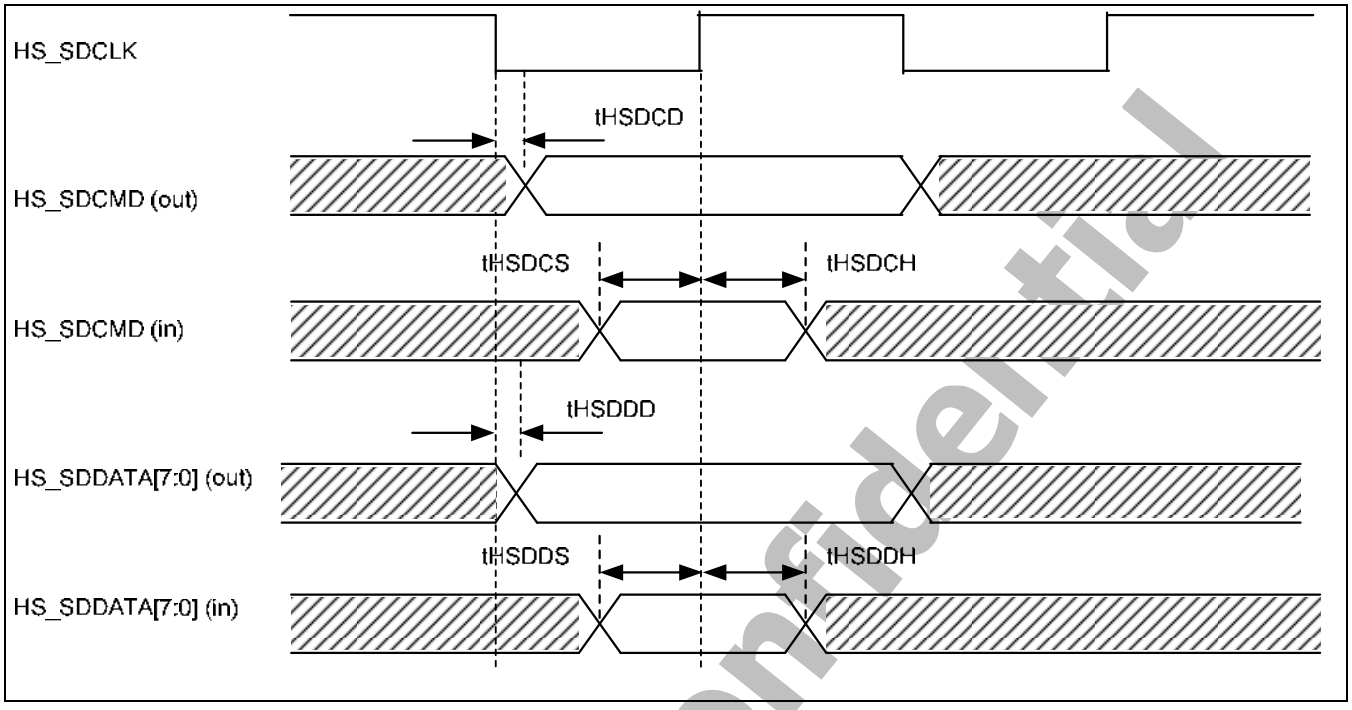

Figure 1-15 High Speed SDMMC Interface Timing

Table 1-15 High Speed SDMMC Interface Transmit/Receive Timing Constants

(VDDINT = 1.1V ± 5%, TA = -25 to 85°C, VDDmmc = 3.3V ± 5%, 2.5V ± 5%, 1.8V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SD Command output Delay time	t_{SDCD}	-	-	4.0	ns
SD Command input Setup time	t_{SDCS}	4.0	-	-	ns
SD Command input Hold time	t_{SDCH}	0	-	-	ns
SD Data output Delay time	t_{SDDD}	-	-	4.0	ns
SD Data input Setup time	t_{SDDS}	4.0	-	-	ns
SD Data input Hold time	t_{SDDH}	0	-	-	ns

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1.13 SPI AC ELECTRICAL CHARACTERISTICS

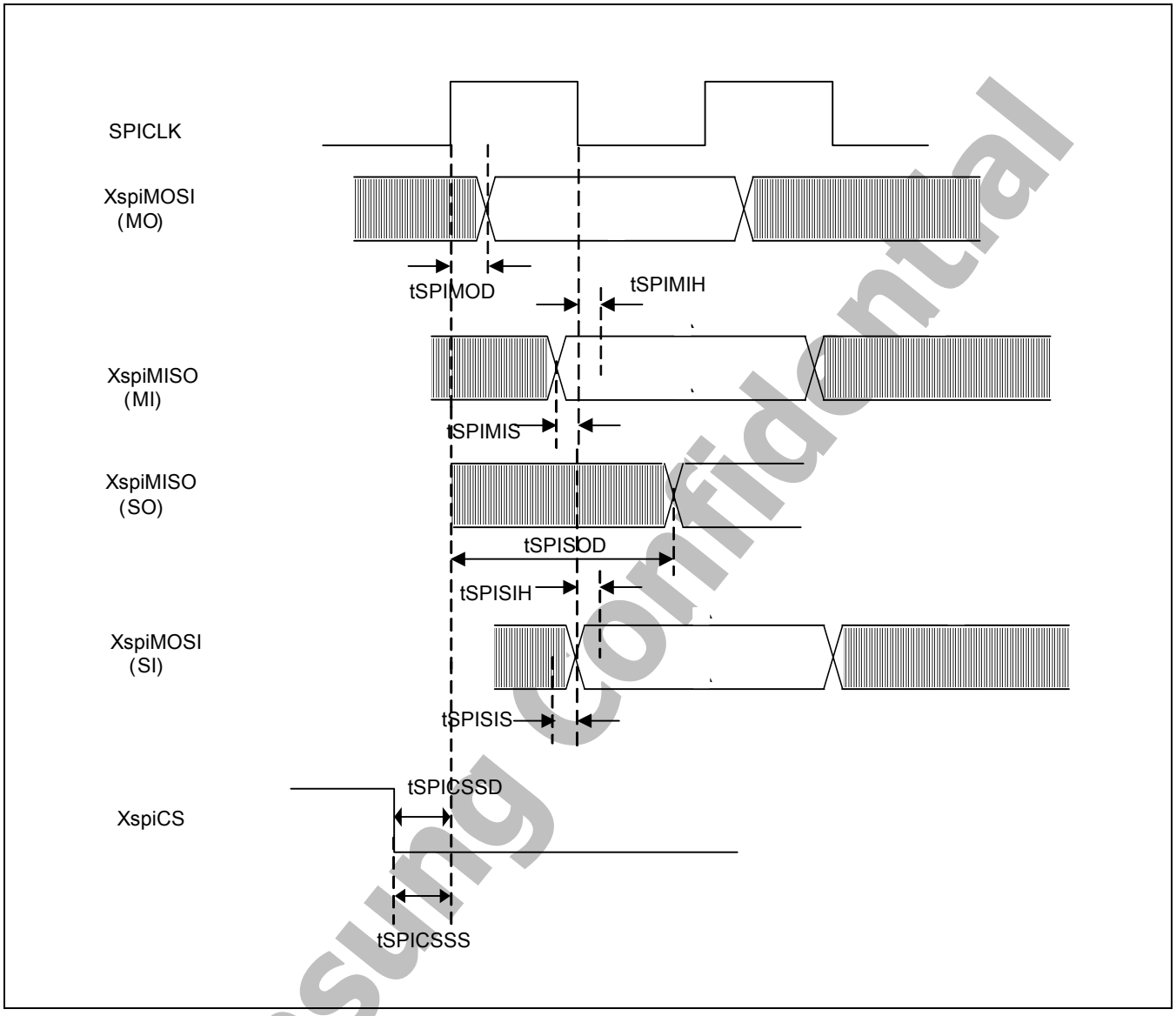

Figure 1-16 SPI Interface Timing (CPHA = 0, CPOL = 1)

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Table 1-16 SPI Interface Transmit/ Receive Timing Constants

(VDDINT = 1.1V ± 5%, TA = -25 to 85°C, VDDext = 1.8V ± 10%, load = 15pF)

Parameter		Symbol	Minimum	Typical	Maximum	Unit
Ch 0	SPI MOSI Master Output Delay time	t_{SPIMOD}	-	-	5	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	12	-	-	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		7	-	-	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		2	-	-	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-3	-	-	ns
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	-	-	ns
	SPI MOSI Slave Input Setup time	t_{SPISIS}	2	-	-	ns
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	-	-	ns
	SPI MISO Slave Output Delay time	t_{SPISOD}	-	-	17	ns
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	7	-	-	ns
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	5	-	-	ns
Ch 1	SPI MOSI Master Output Delay time	t_{SPIMOD}	-	-	4	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	13	-	-	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		8	-	-	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		3	-	-	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-2	-	-	ns
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	-	-	ns
	SPI MOSI Slave Input Setup time	t_{SPISIS}	3	-	-	ns
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	-	-	ns
	SPI MISO Slave Output Delay time	t_{SPISOD}	-	-	18	ns
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	7	-	-	ns
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	5	-	-	ns

NOTE: SPICLKout = 50MHz

$t_{SPIMIS,CH0}$ = 12 - (cycle period / 4) x FB_CLK_SEL

$t_{SPIMIS,CH1}$ = 13 - (cycle period / 4) x FB_CLK_SEL

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(VDDINT = 1.1V ± 5%, TA = -25 to 85°C, VDDext = 3.3V ± 10%, load = 30pF)

Parameter		Symbol	Minimum	Typical	Maximum	Unit
Ch 0	SPI MOSI Master Output Delay time	t_{SPIMOD}	-	-	6	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	13	-	-	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		8	-	-	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		3	-	-	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-2	-	-	ns
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	-	-	ns
	SPI MOSI Slave Input Setup time	t_{SPISIS}	4	-	-	ns
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	-	-	ns
	SPI MISO Slave Output Delay time	t_{SPISOD}	-	-	18	ns
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	8	-	-	ns
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	6	-	-	ns
Ch 1	SPI MOSI Master Output Delay time	t_{SPIMOD}	-	-	5	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	14	-	-	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		9	-	-	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		4	-	-	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		-1	-	-	ns
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	-	-	ns
	SPI MOSI Slave Input Setup time	t_{SPISIS}	4	-	-	ns
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	-	-	ns
	SPI MISO Slave Output Delay time	t_{SPISOD}	-	-	19	ns
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	8	-	-	ns
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	6	-	-	ns

NOTE: SPICLKout = 50MHz
$t_{SPIMIS,CH0}$ = 12 - (cycle period / 4) x FB_CLK_SEL
$t_{SPIMIS,CH1}$ = 13 - (cycle period / 4) x FB_CLK_SEL

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1.14 I2C AC ELECTRICAL CHARACTERISTICS

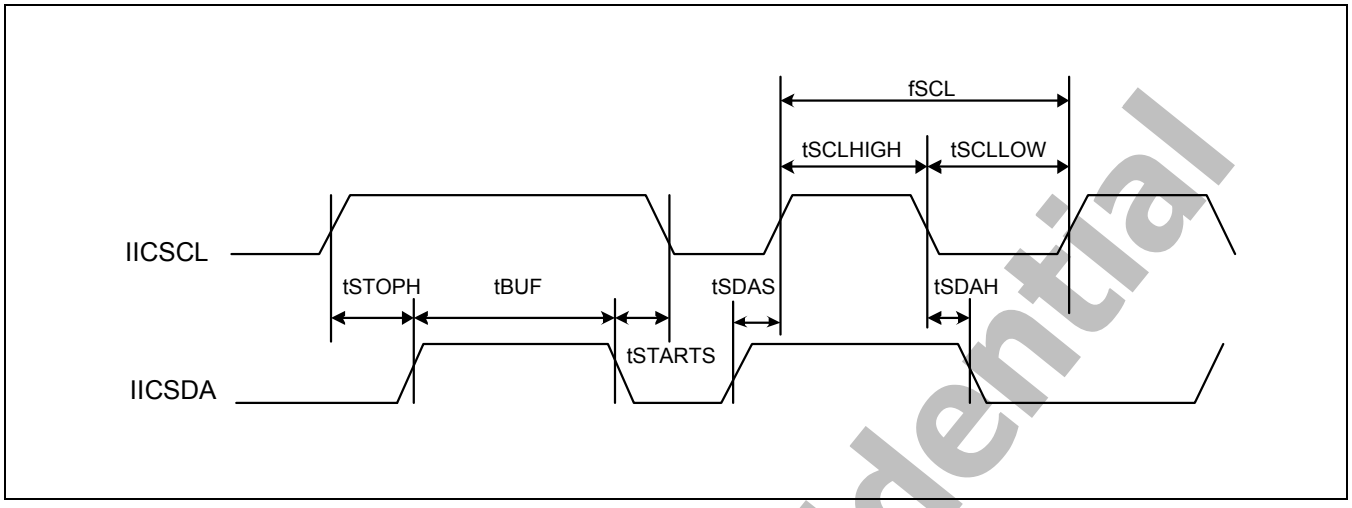

Figure 1-17 IIC Interface Timing

Table 1-17 IIC BUS Controller Module Signal Timing

(VDDINT = 1.1V±5%, TA = -25 to 85℃, VDDext = 3.3V±10%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SCL clock frequency	f_{SCL}	-	-	std. 100 fast 400	kHz
SCL high level pulse width	$t_{SCLHIGH}$	std. 4.0 fast 0.6	-	-	us
SCL low level pulse width	t_{SCLLOW}	std. 4.7 fast 1.3	-	-	us
Bus free time between STOP and START	t_{BUF}	std 4.7 fast 1.3	-	-	us
START hold time	t_{STARTS}	std. 4.0 fast 0.6	-	-	us
SDA hold time	t_{SDAH}	std. 0 fast 0	-	std.-fast 0.9	us
SDA setup time	t_{SDAS}	std. 250 fast 100	-	-	ns
STOP setup time	t_{STOPH}	std. 4.0 fast 0.6	-	-	us

NOTE: std. refers to Standard Mode and fast refers to Fast Mode.

1. The IIC data hold time (tSDAH) is minimum 0ns.
   (IIC data hold time is minimum 0ns for standard/ fast bus mode IIC specification v2.1)
   Check whether the data hold time of your IIC device is 0 ns or not.
2. The IIC controller supports IIC bus device only (standard/fast bus mode), and does not support C bus device.

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1.15 TSI AC ELECTRICAL CHARACTERISTICS

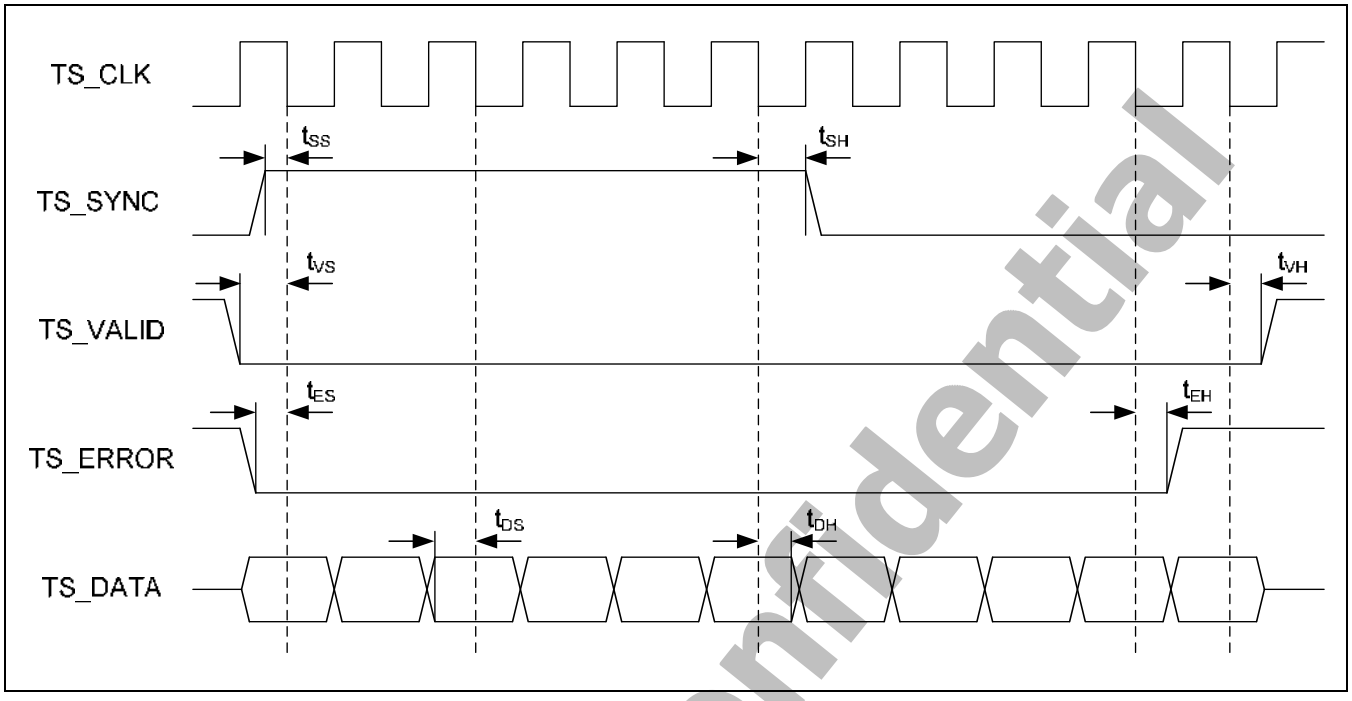

Figure 1-18 Transport Stream Interface Timing

Table 1-18 Transport Stream Interface Timing Constants

(VDDINT = 1.1V ± 5%, TA = -25 to 85°C, VDDext = 1.8V ± 10%, load = 35pF)

Parameter	Symbol	Minimum	Maximum	Unit
TSI synchronization signal setup time	t_{SS}	3	-	ns
TSI synchronization signal hold time	t_{SH}	3	-	ns
TSI valid signal setup time	t_{VS}	3	-	ns
TSI valid signal hold time	t_{VH}	3	-	ns
TSI error signal setup time	t_{ES}	3	-	ns
TSI error signal hold time	t_{EH}	3	-	ns
TSI input data setup time	t_{DS}	3	-	ns
TSI input data hold time	t_{DH}	3	-	ns

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