



L8001

Preliminary

CMOS IC

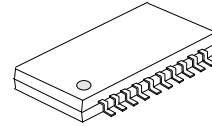
FET BIAS CONTROLLER

DESCRIPTION

The UTC **L8001** is specially designed integrated circuit for satellite receiver front-end block. It provides stable drain and gate bias conditions for GaAs or HEMT FETs.

The UTC **L8001**, provide six FETs bias control respectively. By adjusting two external resistors, it can change the FET's bias current to optimize the satellite receiver front end block performances.

It generates the required negative voltage to bias the gate of GaAs FET, and internally provides protection circuit that can protect the FET devices during supply voltage transient. So it is very popular in satellite receiver front end block.



SSOP-20(150mil)

FEATURES

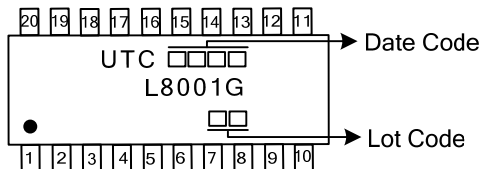
- * Built in FET device protection circuit
- * Adjustable FET device operating current
- * Stable bias control for GaAs and HEMT FETs
- * Drive up to six FETs
- * Wide supply voltage range

ORDERING INFORMATION

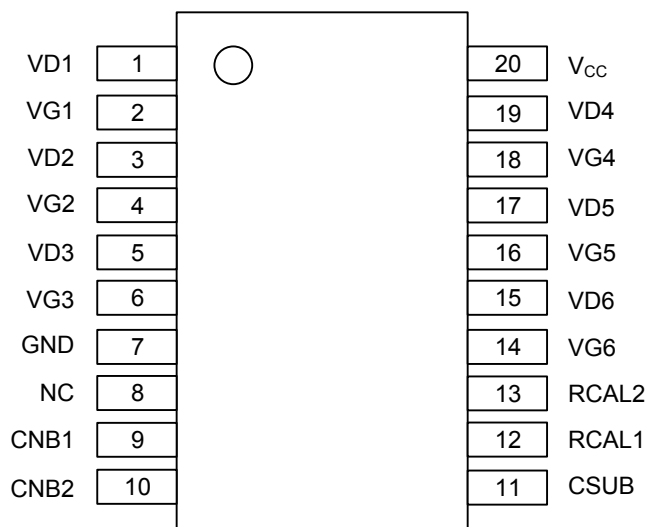
| Ordering Number | Package | Packing |
|-----------------|---------|-----------|
| L8001G-R20-R | SSOP-20 | Tape Reel |

| | |
|---|--|
| <p>L8001G-R20-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Green Package | <ul style="list-style-type: none"> (1) R: Tape Reel (2) SSOP-20 (3) G: Halogen Free and Lead Free |
|---|--|

MARKING



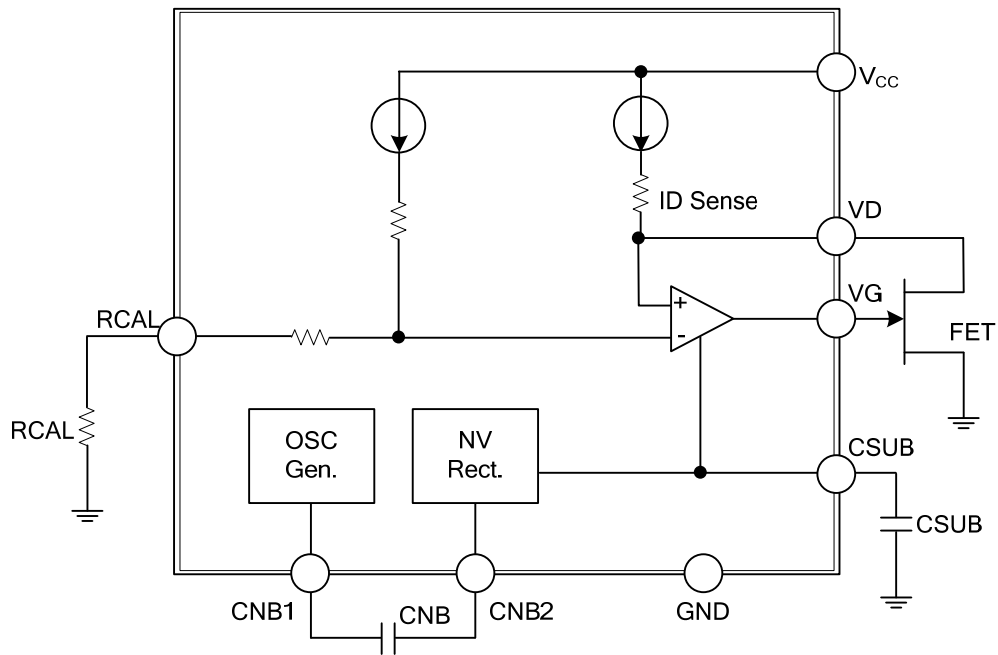
■ PIN CONFIGURATION



■ PIN DESCRIPTION

| PIN NO. | PIN NAME | DESCRIPTION |
|---------|-----------------|--|
| 1 | VD1 | 1 st Drain output voltage |
| 2 | VG1 | 1 st Gate output voltage |
| 3 | VD2 | 2 nd Drain output voltage |
| 4 | VG2 | 2 nd Gate output voltage |
| 5 | VG3 | 3 rd Gate output voltage |
| 6 | VD3 | 3 rd Drain output voltage |
| 7 | GND | Ground |
| 8 | NC | No connect |
| 9 | CNB1 | OSC output |
| 10 | CNB2 | Rectifier Input |
| 11 | CSUB | Negative voltage output |
| 12 | RCAL1 | VD1/VD2/VD3 current set resistor connect |
| 13 | RCAL2 | VD4/VD5/VD6 current set resistor connect |
| 14 | VG6 | 6 th Gate output voltage |
| 15 | VD6 | 6 th Drain output voltage |
| 16 | VG5 | 5 th Gate output voltage |
| 17 | VD5 | 5 th Drain output voltage |
| 18 | VG4 | 4 th Gate output voltage |
| 19 | VD4 | 4 th Drain output voltage |
| 20 | V _{CC} | Supply voltage |

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---------------------------|-----------|---------|------|
| Supply Voltage | V_{CC} | -0.6~8 | V |
| Supply Current | I_{CC} | 100 | mA |
| Maximum Drain Current | | 15 | mA |
| Maximum CSUB Sink Current | | -500 | uA |
| Operating Temperature | T_{OPR} | -40~80 | °C |
| Storage Temperature | T_{STG} | -50~150 | °C |

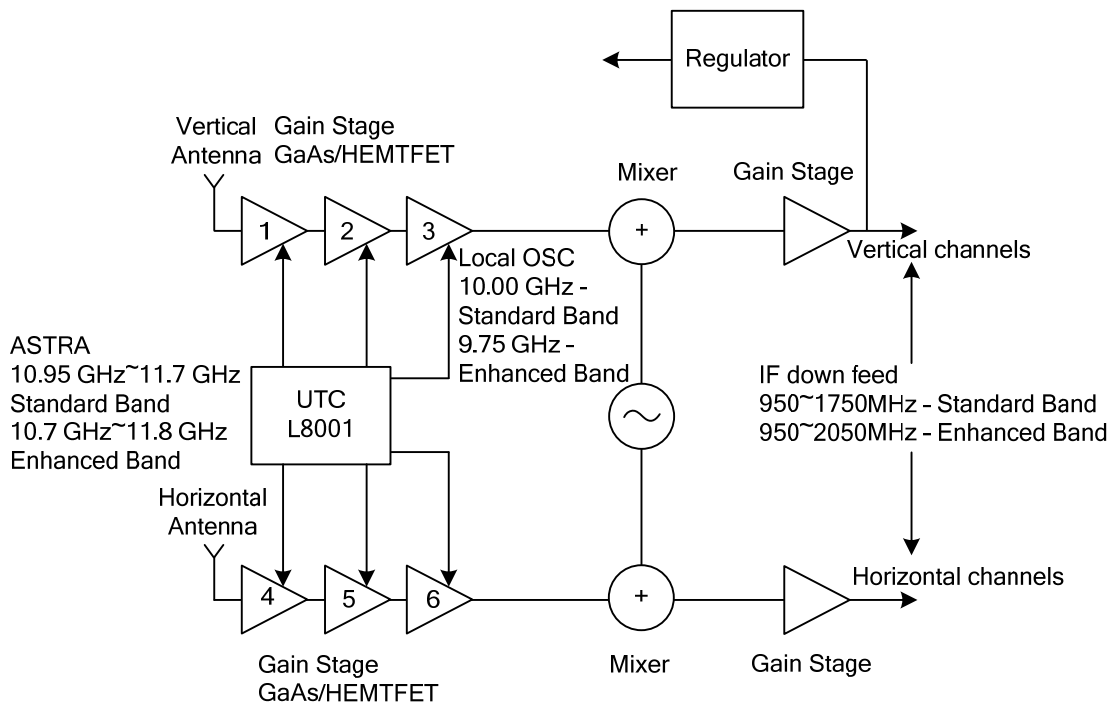
Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

($V_{CC}=3.3V$, $I_D=10mA$, $R_{CAL1}=8.2K\Omega$, $R_{CAL2}=8.2K\Omega$, $T_A=25^\circ C$, unless otherwise stated)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|-----------------|----------------------------------|------|------|------|----------|
| Supply Voltage | V_{CC} | | 3.3 | | 6 | V |
| Supply Current | I_{CC} | No FET | | | 10 | mA |
| Negative Voltage | V_{SUB} | $I_{SUB}=0uA$, $V_{CC}=6V$ | -3.0 | -2.5 | -1 | V |
| | | $I_{SUB}=-200uA$ | | | -1 | V |
| Oscillator Freq. | f_O | | 200 | 350 | 800 | KHz |
| Drain Current | I_D | | 8 | 10 | 12 | mA |
| Drain Current Change with V_{CC} | ΔI_{DV} | $V_{CC}=3.3\sim 6V$ | | 0.2 | | %/V |
| VD1/VD2(VD3/VD4) Drain Offset Current | ΔI_{DC} | | | 0.2 | | mA |
| Drain Current Change with Temp. | ΔI_{DT} | $T=-40\sim 80^\circ C$ | | 0.1 | | %/°C |
| Drain Voltage | V_D | $I_D=10mA$ | 1.8 | 2 | 2.2 | V |
| Drain Voltage Change with V_{CC} | ΔV_{DV} | $V_{CC}=3.3\sim 6V$ | | 0.5 | | %/V |
| Drain Voltage Change | ΔV_{DT} | $T=-40\sim 80^\circ C$ | | 50 | | ppm |
| Dynamic Gate Voltage Range | V_G | Csub without loading | -2.5 | | 0.7 | V |
| Drain Output Noise Voltage | V_{dn} | With drain bypass capacitor=10nF | | | 0.05 | V_{PP} |
| Gate Output Noise Voltage | V_{GN} | With gate bypass capacitor=10nF | | | 0.03 | V_{PP} |

■ TYPICAL APPLICATION CIRCUIT



UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.