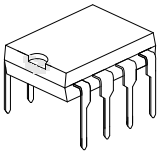
UPS3652

LINEAR INTEGRATED CIRCUIT

HIGH PERFORMANCE CURRENT MODE POWER SWITCH



DIP-8

■ DESCRIPTION

The UTC **UPS3652** is an integrated PWM controller and PowerMOSFET specifically designed for switching operation with minimal external components. The UTC **UPS3652** is designed to provide several special enhancements to satisfy the needs, for example, Power-Saving mode for low standby power (<0.3W), Frequency Hopping , Constant Output Power Limiting , Slope Compensation ,Over Current Protection (OCP), Over Voltage Protection (OVP), Over Load Protection (OLP), Under Voltage Lock Out (UVLO), Short Circuit Protection (SCP) , Over Temperature Protection (OTP), etc. IC will be shutdown or can auto-restart in situations.

■ FEATURE

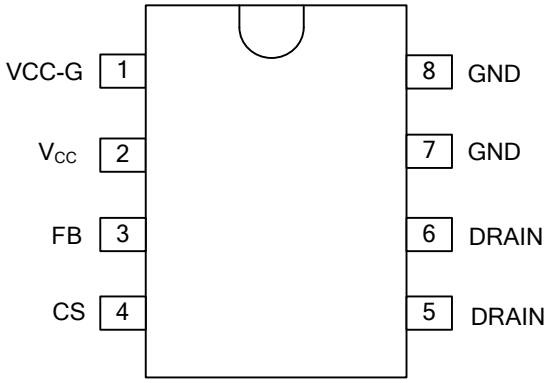
* Internal PowerMOSFET (650V)
* Programming Gate Driver Capability
* Frequency hopping for Improved EMI Performance.
* Lower than 0.3W Standby Power Design
* Linearly decreasing frequency to 26KHz during light load
* Internal Soft start
* Internal Slope Compensation
* Constant Power Limiting for universal AC input Range
* Gate Output Maximum Voltage Clamp(15V)
* Over temperature protection
* Overload protection
* Over voltage protection
* Leading edge blanking
* Cycle-by-Cycle current limiting
* Under Voltage Lock Out
* Short Circuit Protection

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UPS3652L-D08-T	UPS3652G-D08-T	DIP-8	Tube

UPS3652L-D08-T (1)Packing Type (2)Package Type (3)Lead Free	(1) T: Tube (2) D08: DIP-8 (3) L: Lead Free, G: Halogen Free

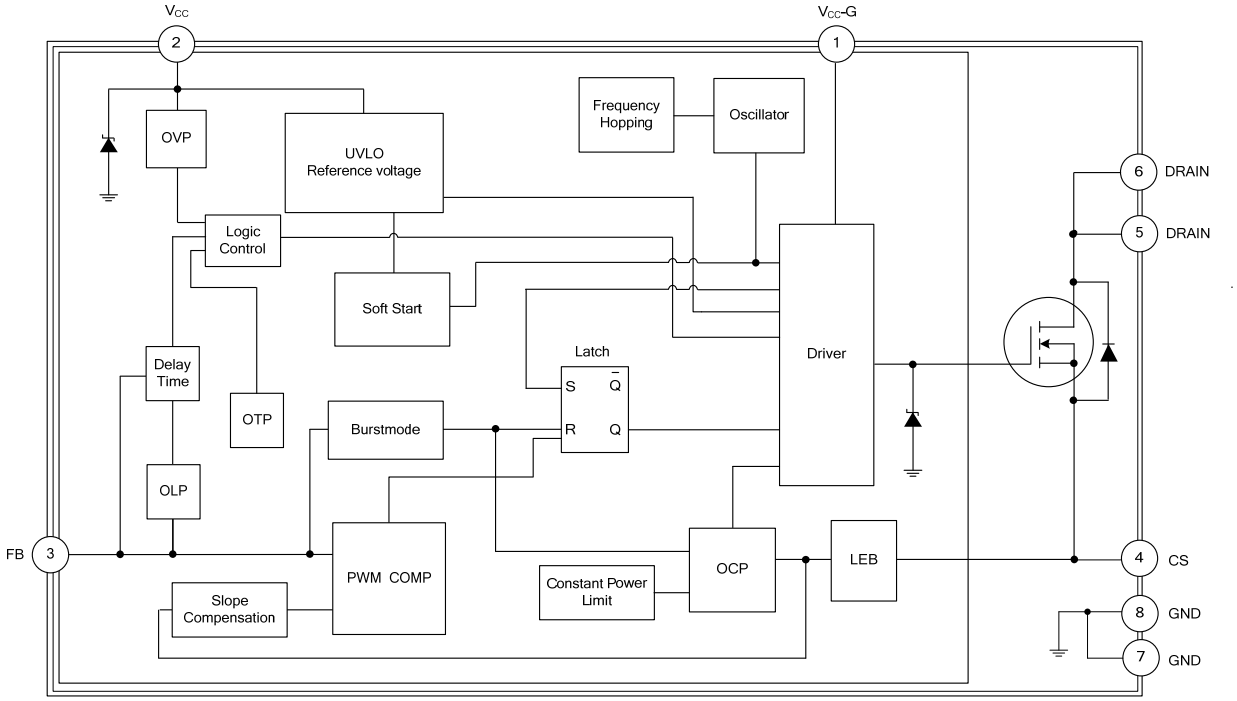
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{CC}-G	Supply voltage
2	V_{CC}	Supply voltage
3	FB	Feedback
4	CS	Current sense input
5	DRAIN	Power MOSFET drain
6	DRAIN	Power MOSFET drain
7	GND	Ground
8	GND	Ground

■ BLOCK DIAGRAM



Notes: OLP (Over Load Protection)
OVP (Over Voltage Protection)
OTP (Over Temperature Protection)
OCP (Over Current Protection)
UVLO (Under Voltage Latch-Out)
LEB (Led Edge Blanking)

■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	30	V
Input Voltage to FB Pin	V_{FB}	-0.3 ~ 6.5	V
Input Voltage to CS Pin	V_{CS}	-0.3 ~ 6.5	V
Junction Temperature	T_J	+150	°C
Operating Temperature	T_{OPR}	-40 ~ +125	°C
Storage Temperature	T_{STG}	-50 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ OPERATING RANGE

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	8.6 ~ 22	V

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{CC}=15V, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION							
Start Up Current		I_{ST}	V_{CC} = $V_{THD(ON)}$-1V		22	45	μA
Supply Current with switch		I_{OP}	V_{FB}= 4V		8	10	mA
UNDER-VOLTAGE LOCKOUT SECTION							
Start Threshold Voltage		$V_{THD(ON)}$		13.5	14.2	15	V
Min. Operating Voltage		$V_{CC(MIN)}$		7.5	8.2	9	V
Hysteresis		$V_{CC(HY)}$			6		V
INTERNAL VOLTAGE REFERENCE							
Reference Voltage		V_{REF}	Guarantee by design	6.3	6.5	6.7	V
CONTROL SECTION							
Feedback Source Current		I_{FB}	V_{FB}=0		1.1		mA
V_{FB} Operating Level		V_{FBMAX}				3.5	V
Burst-Mode Out FB Voltage		$V_{FB(OUT)}$	V_{CS} =0		1.1		V
Reduce-Frequency end FB Voltage		$V_{FB(END)}$	V_{CS} =0		1.2		V
Burst-Mode Enter FB Voltage		$V_{FB(IN)}$	V_{CS} =0		0.9		V
Switching frequency	Normal initial	$F_{(SW)}$	V_{FB} = 4V	45	50	55	kHz
	Power-Saving		Before enter burst mode	20		30	kHz
Duty Cycle		D_{MAX}	V_{FB}=4V, V_{CS}=0	64	72	80	%
Frequency Hopping		$F_{J(SW)}$		±2.5	±4	±5.5	kHz
Frequency Variation VS V_{CC} Deviation		F_{DV}	V_{CC}=10 to 20V			5	%
Frequency Variation VS Temperature Deviation		F_{DT}	T=-25 to 105°C			5	%
Soft-Start Time		T_{SOFTS}		2	4	6	ms
PROTECTION SECTION							
OVP threshold		V_{OVP}	V_{FB}=4V		23		V
OLP threshold		$V_{FB(OLP)}$	V_{CS}=0		3.7		V
Delay Time Of OLP		T_{D-OLP}	C_{FB}=47nF(From V_{FB}=3.7V to Drain OFF)	35	65	95	ms
OTP Threshold		$T_{(THR)}$		120	135	155	°C
CURRENT LIMITING SECTION							
Leading Edge Blanking Time		t_{LEB}		270	350	450	nS
Peak Current Limitation		V_{CS}	V_{FB}=4V	0.88	0.95	1.03	V
Threshold Voltage For Valley		$V_{SENSE-L}$	V_{FB}=4V		0.75		V

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER MOS-TRANSISTOR SECTION						
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS}=0V, I_D=250μA	650			V
Turn-on voltage between gate and source	V_{TH}	V_{DS}=V_{GS}, I_D=250μA	2		4	V
Drain-Source Diode Continuous Source Current	I_S				2	A
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=2.25A			5	Ω
Rise Time	t_R	V_{DD} =300V, I_D =4.0A R_G=25Ω (Note 1,2)		45	100	ns
Fall Time	t_F			35	80	ns

Notes: 1. Pulse Test: Pulse width≤300μs, Duty cycle≤2%
2. Essentially independent of operating temperature

■ FUNCTIONAL DESCRIPTION

The internal reference voltages and bias circuit work at V_{CC}> $V_{THD(ON)}$, and shutdown at V_{CC}<$V_{CC(MIN)}$.

(1) Soft-Start

When every IC power on, driver output duty cycle will be decided by inter-slope voltage V_{SOFTS} and V_{CS} on current sense resistor at beginning. After the whole soft-start phase end, and driver duty cycle depend on V_{FB} and V_{CS}. The relation among V_{SOFTS}, V_{FB} and V_{OUT} as followed FIG.3. Furthermore, soft-start phase should end before V_{CC} reach $V_{CC(MIN)}$ during V_{CC} power on. Otherwise, if soft-start phase remain not end before V_{CC} reach $V_{CC(MIN)}$ during V_{CC} power on, IC will enter auto-restart phase and not set up V_{OUT}.

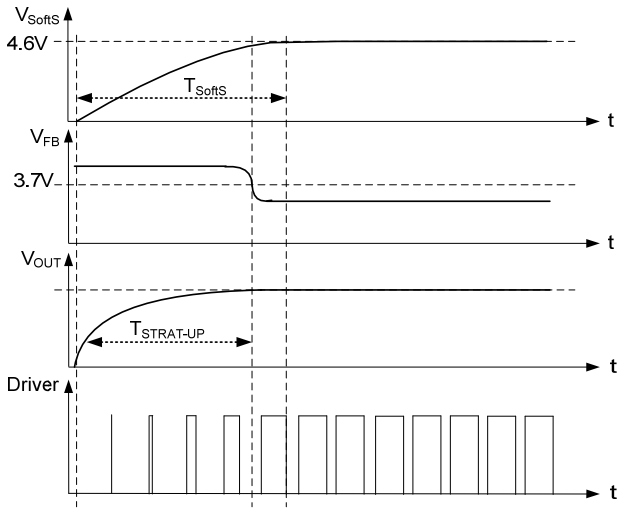


FIG.3 Soft-start phase

(2) Switching Frequency Set

The maximum switching frequency is set to 50kHz. Switching frequency is modulated by output power P_{OUT} during IC operating. At no load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. So lower Switching frequency at lower load, which more and more improve IC's efficiency at light load. At from no load to light load condition, The IC will operate at from Burst mode to Reducing Frequency Mode. The relation curve between f_{SW} and $P_{OUT}/P_{OUT(MAX)}$ as followed FIG.4.

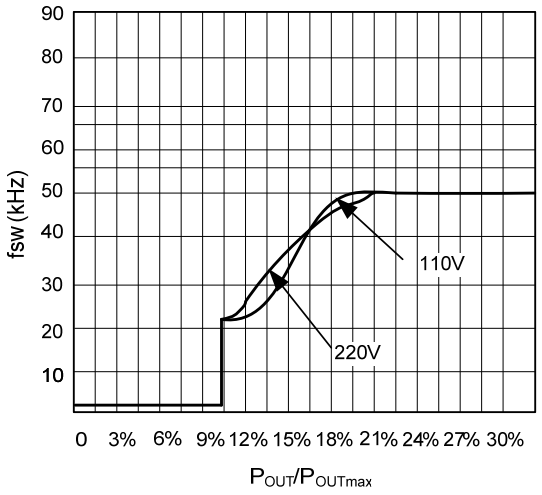


FIG.4 The relation curve between f_{SW} and relative output power P_{OUT}/ $P_{OUT(MAX)}$

■ FUNCTIONAL DESCRIPTION(Cont.)

(3) Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation, this greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

(4) Frequency Hopping For EMI Improvement

The Frequency Hopping is implemented in the IC; there are two oscillators built-in the IC. The first oscillator is to set the normal switching frequency; the switching frequency is modulated with a period signal generated by the 2nd oscillator. The relation between the first oscillator and the 2nd oscillator as followed FIG.5. So the tone energy is evenly spread out, the spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

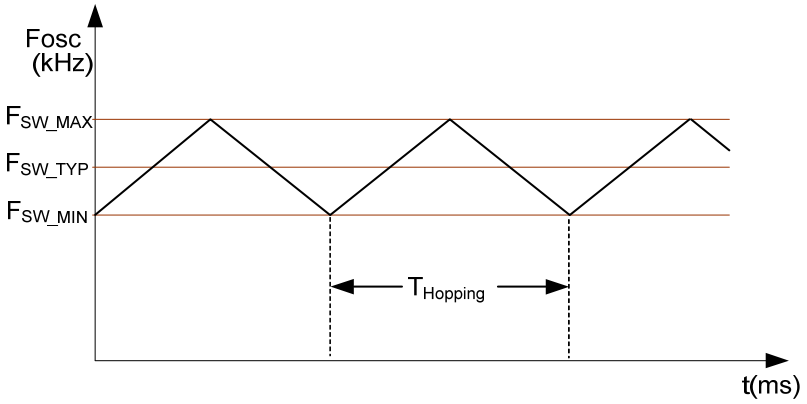


FIG.5 Frequency Hopping

(5) Constant Output Power Limit

When the primary current, across the primary wind of transfer, reaches the limit current, around 1.2A, the output GATE drive will be turned off after a small propagation delay t_D. This propagation delay will introduce an additional current proportional to $t_D \times V_{IN}/Lp$. Since the propagation delay is nearly constant regardless of the input line voltage V_{IN}. Higher input line voltage will result in a larger additional current and hence the output power limit is also higher than that under low input line voltage. To compensate for this output power limit variation across a wide AC input range, the threshold voltage is adjusted by adding a positive ramp. This ramp signal rises from 0.75V to 0.95V, and then flattens out at 0.95V. A smaller threshold voltage forces the output GATE drive to terminate earlier. This reduces the total PWM turn-on time and makes the output power equal to that of low line input. This proprietary internal compensation ensures a constant output power limit for a wide AC input voltage range (90VAC to 264VAC).

(6) Protection section

The IC takes on more protection functions such as OLP, OVP and OTP etc. In case of those failure modes for continual blanking time, the driver is shut down. At the same time, IC enters auto-restart, V_{CC} power on and driver is reset after V_{CC} power on again.

OLP

After power on, IC will shutdown driver if over load state occurs for continual $T_{D\text{-}OLP}$. OLP case as followed FIG.6. The test circuit as followed FIG.8. $T_{D\text{-}OLP} \approx 2C_{FB}/1.4$.

OVP

OVP will shutdown the switching of the power MOSFET whenever $V_{CC} > V_{OVP}$. The OVP case as followed FIG.7. the test circuit as followed FIG.9.

■ FUNCTIONAL DESCRIPTION(Cont.)

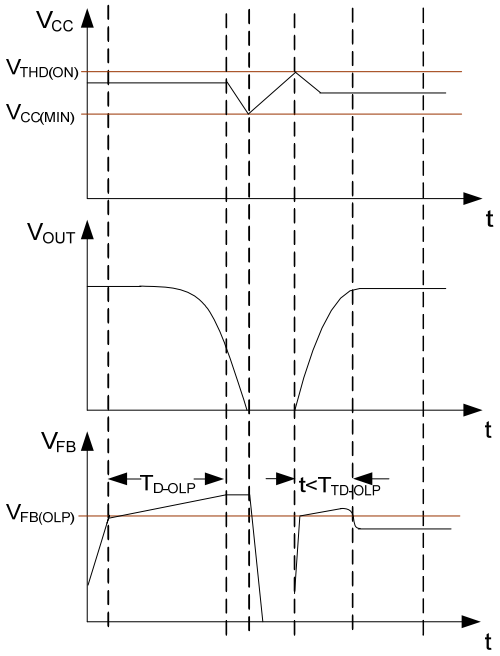


FIG.6 OLP case

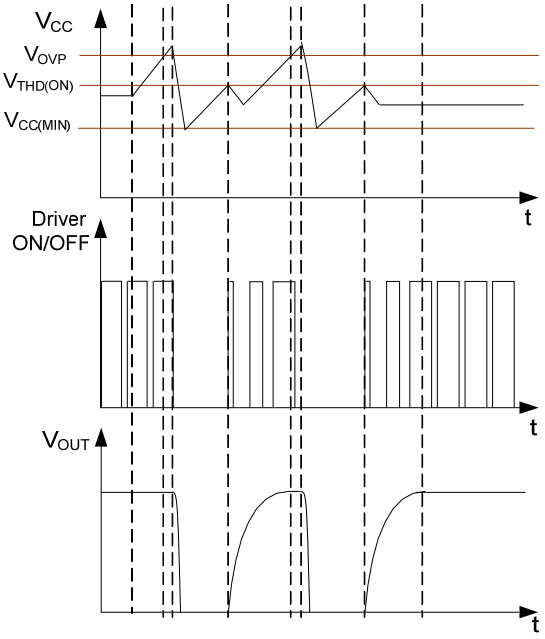


FIG.7 OVP case

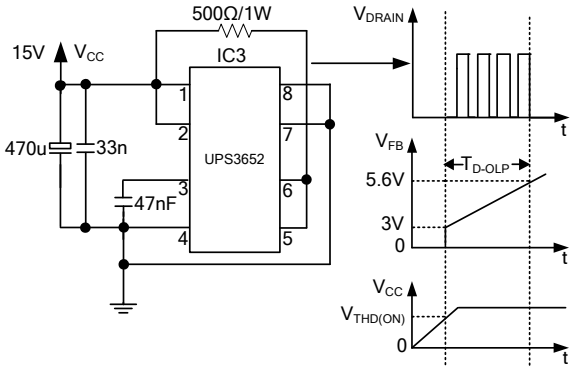


FIG.8 OLP test circuit

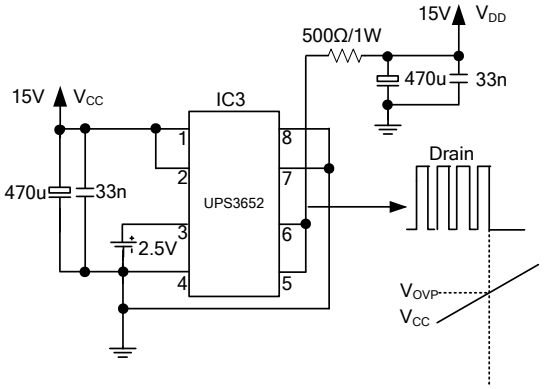


FIG.9 OVP test circuit

OTP

OTP will shut down driver when junction temperature T_J>$T_{(THR)}$ for continual a blanking time.

(7) Driver Output Section

The driver-stage drives the gate of the MOSFET and is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when reaching the MOSFET threshold. This is achieved by a slope control of the rising edge at the driver's output. The output driver is clamped by an internal 15V Zener diode in order to protect power MOSFET transistors against undesirable gate over voltage.

(8) Inside power switch MOS transistor

Specific power MOS transistor parameter is as "POWER MOS TRANSISTOR SECTION" in electrical characteristics table.

■ TYPICAL APPLICATION CIRCUIT

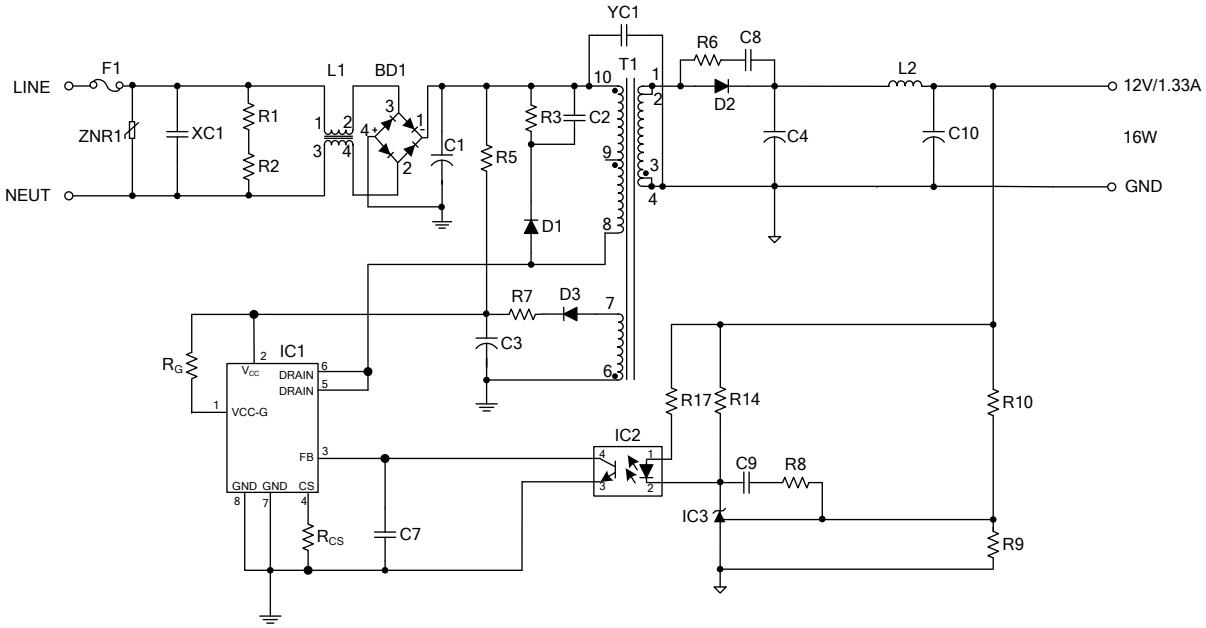


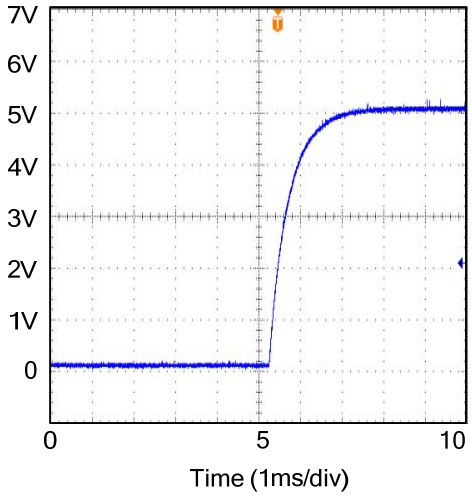
FIG.10 UTC UPS3652 Typical Application Circuit

Table1. Components reference description for UTC UPS3652 application circuit

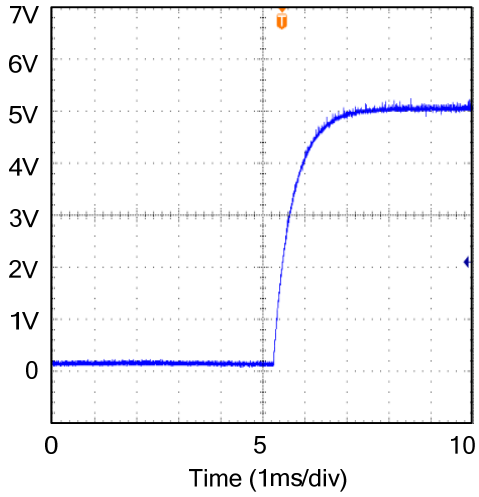
DESIGNATOR	PART TYPE		DESIGNATOR	PART TYPE		DESIGNATOR	PART TYPE
C1	33μF		R1	2.2MΩ		D1	RS1M
C2	0.001μF		R2	2.2MΩ		D2	SR39
C3	22μF		R3	100KΩ		D3	RS1D
C4	470μF		R5	2MΩ		IC1	**UPS3652**
C7	0.01μF		R6	30Ω		IC2	PC-817
C8	0.001μF		R7	15Ω		IC3	TL431
C9	0.1μF		R8	4.7KΩ		YC1	102P/400V
C10	470μF		R9	3.92KΩ		T1	EE22
			R10	15KΩ		L1	UU9.8
			R14	1.8KΩ		L2	2μH
			R17	510Ω		F1	1A/250V
			R_G	0Ω		ZNR1	7D471K
			R_{CS}	1Ω		XC1	0.1μF/250V
						BD1	KBP205

■ TYPICAL CHARACTERISTICS

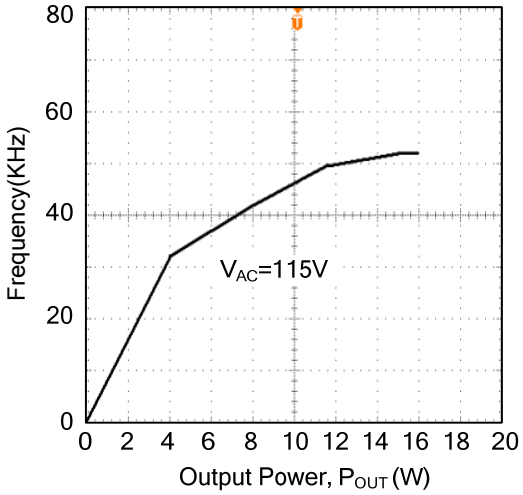
Feedback Voltage During Loadjump From 10% Up To 100% Load (V_{AC}=90V)



Feedback Voltage During Loadjump From 10% Up To 100% Load (V_{AC}=264V)



Frequency vs. Output Power



NO Load Input Power vs. Line Voltage (Normal Mode)