



U74HC374

CMOS IC

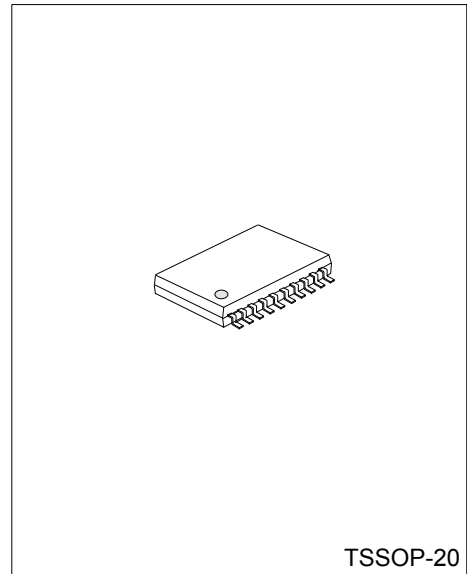
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

DESCRIPTION

The UTC **U74HC374** is an octal edge-triggered D-type flip-flop with 3-state outputs and 8 channels.

FEATURES

- * Operate from 2V to 6V
- * Max t_{PD} of 46ns at 4.5 V , $T_a = 25^{\circ}C$
- * Max I_{CC} of 8 μA , $T_a = 25^{\circ}C$
- * Typical $V_{OL} < 0.17V$ at $V_{CC} = 4.5V, I_{OUT} = -6mA, T_a = 25^{\circ}C$
- * Typical $V_{OH} > 4.3V$ at $V_{CC} = 4.5V, I_{OUT} = 6mA, T_a = 25^{\circ}C$

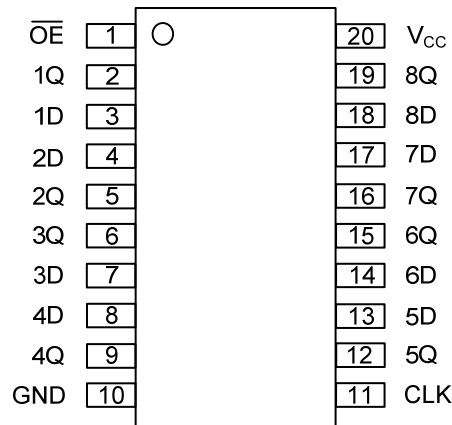


ORDERING INFORMATION

Ordering Number	Package	Packing
U74HC374G-P20-R	TSSOP-20	Tape Reel

<p>U74HC374G-P20-R</p>	<p>(1) R: Tape Reel</p> <p>(2) P20: TSSOP-20</p> <p>(3) G: Halogen Free</p>
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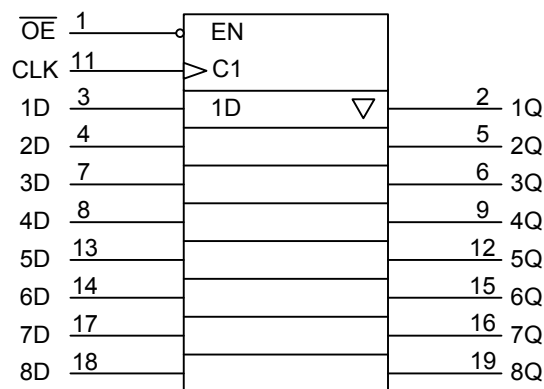
■ PIN CONFIGURATION



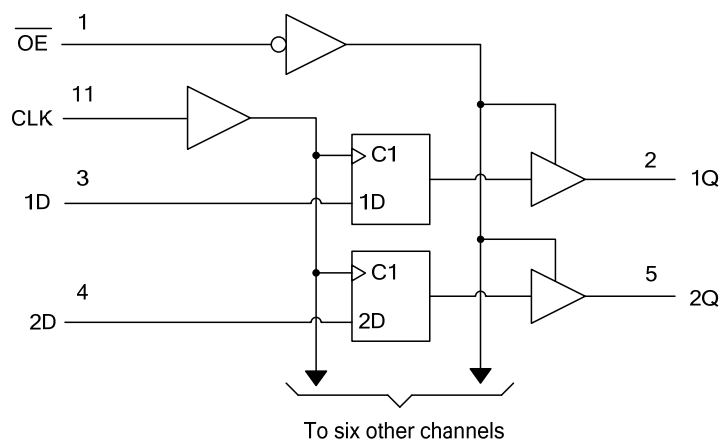
■ FUNCTION TABLE

INPUTS(\overline{OE})	INPUTS(CLK)	INPUTS(D)	OUTPUT(Q)
L	\uparrow	H	H
L	\uparrow	L	L
L	L/H	X	Q0
H	X	X	Z

■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ +7	V
V_{CC} or GND Current	I_{CC}	±70	mA
Output Current	I_{OUT}	±35	mA
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Operating Temperature	T_{OPR}	-40 ~ + 85	°C
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	83	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2	5	6	V
High-Level Input Voltage	V_{IH}	$V_{CC}=2V$	1.5			V
		$V_{CC}=4.5V$	3.15			V
		$V_{CC}=6V$	4.2			V
Low-Level Input Voltage	V_{IL}	$V_{CC}=2V$			0.5	V
		$V_{CC}=4.5V$			1.35	V
		$V_{CC}=6V$			1.8	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
Input Rise or Fall Times	t_R, t_F	$V_{CC}=2V$	0		1000	ns
		$V_{CC}=4.5V$	0		500	ns
		$V_{CC}=6V$	0		400	ns

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	V_{OH}	$V_{CC}=2V, I_{OH}=-20\mu A$	1.9	1.999		V
		$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4	4.499		V
		$V_{CC}=6V, I_{OH}=-20\mu A$	5.9	5.999		V
		$V_{CC}=4.5V, I_{OH}=-6mA$	3.98	4.3		V
		$V_{CC}=6V, I_{OH}=-7.8mA$	5.48	5.8		V
Output Voltage Low-Level	V_{OL}	$V_{CC}=2V, I_{OL}=20\mu A$		0.002	0.1	V
		$V_{CC}=4.5V, I_{OL}=20\mu A$		0.001	0.1	V
		$V_{CC}=6V, I_{OL}=20\mu A$		0.001	0.1	V
		$V_{CC}=4.5V, I_{OL}=6mA$		0.17	0.26	V
		$V_{CC}=6V, I_{OL}=7.8mA$		0.15	0.26	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=6V, V_{IN}=V_{CC}$ or GND		±0.1	±100	nA
3-State Leakage Current	I_{OZ}	$V_{CC}=6V, V_{OUT}=V_{CC}$ or GND		±0.01	±0.5	μA
Quiescent Supply Current	I_{CC}	$V_{CC}=6V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			8	μA
Input Capacitance	C_I	$V_{CC}=2V \sim 6V$		3	10	pF

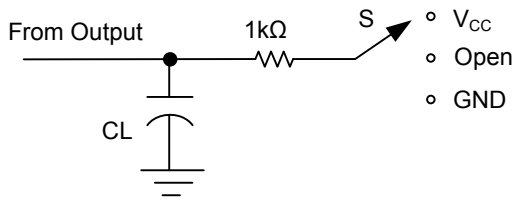
■ SWITCHING CHARACTERISTICS (See TEST CIRCUIT AND WAVEFORMS)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
From CLK to Q	t_{PLH}/t_{PHL}	$C_L = 50\text{pF}$	$V_{CC}=2\text{V}$		63	180	ns
			$V_{CC}=4.5\text{V}$		17	36	ns
			$V_{CC}=6\text{V}$		15	31	ns
		$C_L = 150\text{pF}$	$V_{CC}=2\text{V}$		80	230	ns
			$V_{CC}=4.5\text{V}$		22	46	ns
			$V_{CC}=6\text{V}$		19	39	ns
From \overline{OE} to Q	t_{PZL}/t_{PZH}	$C_L = 50\text{pF}$	$V_{CC}=2\text{V}$		60	150	ns
			$V_{CC}=4.5\text{V}$		16	30	ns
			$V_{CC}=6\text{V}$		14	26	ns
		$C_L = 150\text{pF}$	$V_{CC}=2\text{V}$		70	200	ns
			$V_{CC}=4.5\text{V}$		25	40	ns
			$V_{CC}=6\text{V}$		22	34	ns
From \overline{OE} to Q	t_{PLZ}/t_{PHZ}	$C_L = 50\text{pF}$	$V_{CC}=2\text{V}$		36	150	ns
Any Q	t_T	$C_L = 50\text{pF}$	$V_{CC}=2\text{V}$		28	60	ns
			$V_{CC}=4.5\text{V}$		8	12	ns
			$V_{CC}=6\text{V}$		6	10	ns
		$C_L = 150\text{pF}$	$V_{CC}=2\text{V}$		45	210	ns
			$V_{CC}=4.5\text{V}$		17	42	ns
			$V_{CC}=6\text{V}$		13	36	ns
Maximum Clock Frequency	f_{MAX}	$C_L = 50\text{pF}$	$V_{CC}=2\text{V}$	6	12		MHz
			$V_{CC}=4.5\text{V}$	30	60		MHz
			$V_{CC}=6\text{V}$	35	70		MHz
		$C_L = 150\text{pF}$	$V_{CC}=2\text{V}$	6	12		MHz
			$V_{CC}=4.5\text{V}$	30	60		MHz
			$V_{CC}=6\text{V}$	35	70		MHz
Clock Frequency	f_{CLOCK}	$V_{CC}=2\text{V}$			6	MHz	
		$V_{CC}=4.5\text{V}$			30	MHz	
		$V_{CC}=6\text{V}$			35	MHz	
Pulse Width	t_w	$V_{CC}=2\text{V}$	80			ns	
		$V_{CC}=4.5\text{V}$	16			ns	
		$V_{CC}=6\text{V}$	14			ns	
Setup Time	t_{SU}	$V_{CC}=2\text{V}$	100			ns	
		$V_{CC}=4.5\text{V}$	20			ns	
		$V_{CC}=6\text{V}$	17			ns	
Hold Time	t_h	$V_{CC}=2\text{V}$	10			ns	
		$V_{CC}=4.5\text{V}$	5			ns	
		$V_{CC}=6\text{V}$	5			ns	

■ OPERATING CHARACTERISTICS ($T_a=25^\circ\text{C}$)

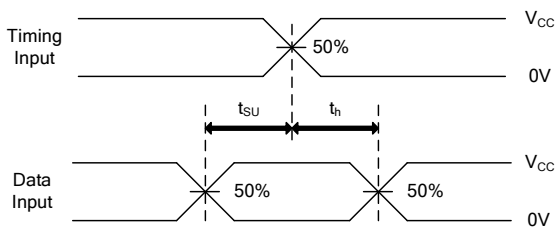
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load		100		pF

■ TEST CIRCUIT AND WAVEFORMS

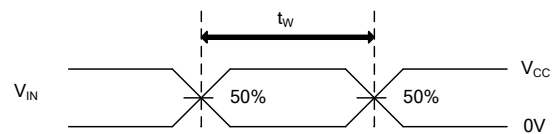


TEST CIRCUIT

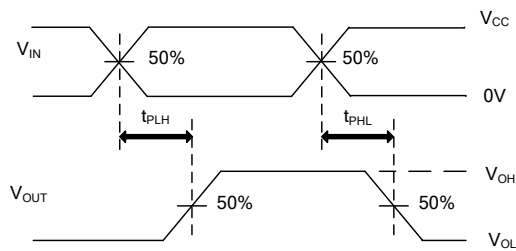
TEST	S
t _{PLH} /t _{PHL}	Open
t _{PHZ} /t _{PZH}	GND
t _{PLZ} /t _{PZL}	V _{CC}



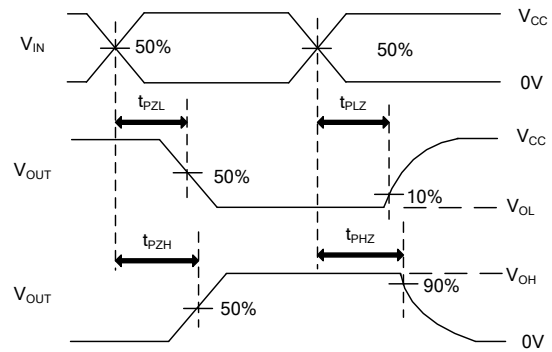
SETUP TIME AND HOLD TIME



PULSE WIDTH



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Note: CL includes probe and jig capacitance.
 PRR ≤ 1MHz, Z_O = 50Ω, t_R ≤ 6ns, t_F ≤ 6ns.

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